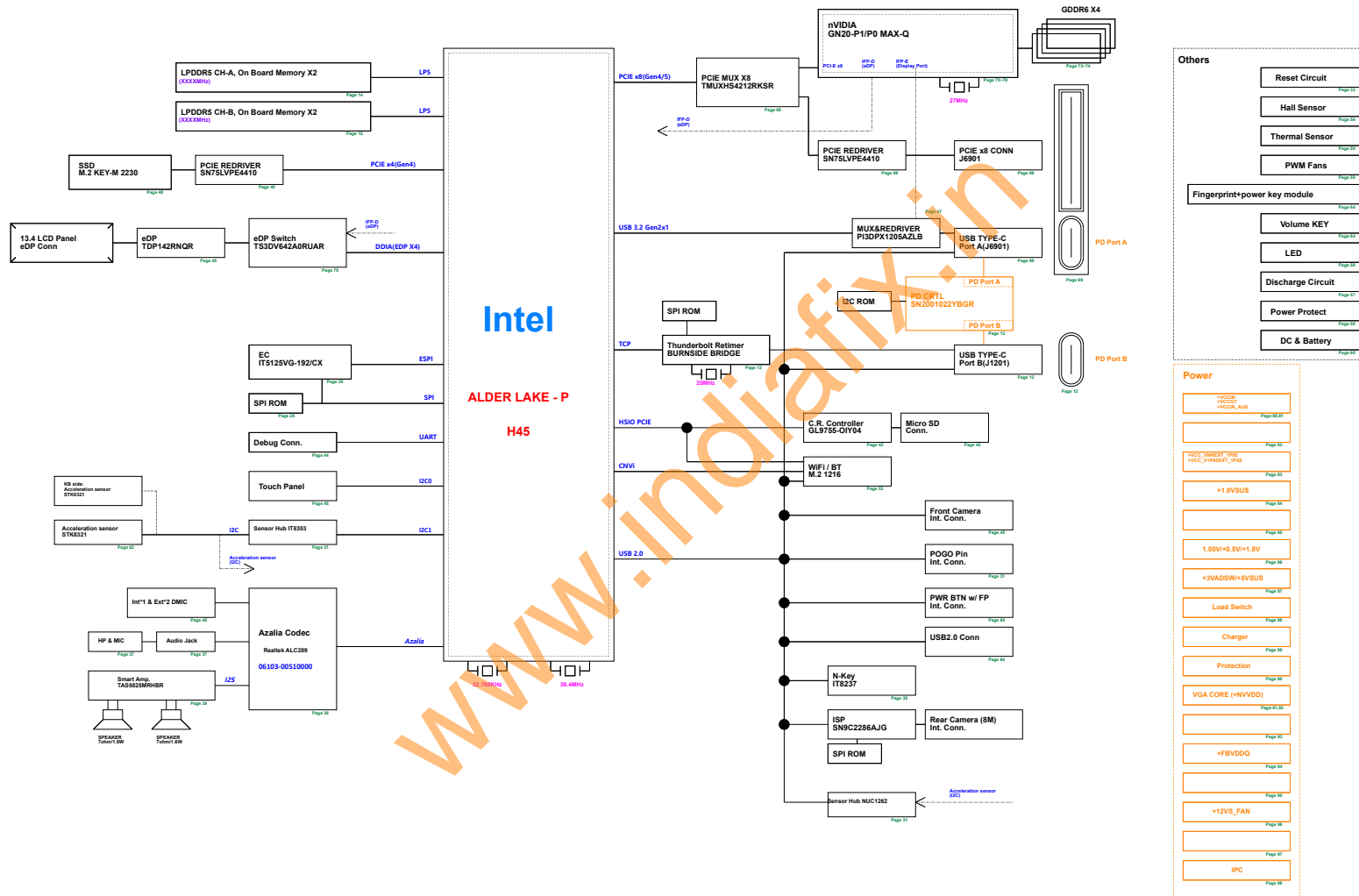


## NR2201 Block Diagram



BOM Optional

EE optional:

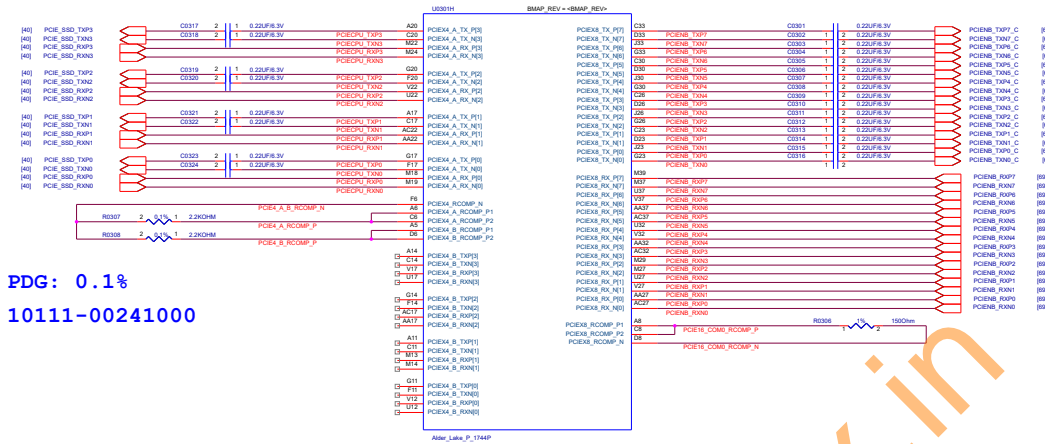
N/A  
/DGPU  
/DGPU\_CPLD  
/DGPU\_ROM  
/DGPU\_GN20P  
/DGPU\_N18P  
/DGPU\_VREF  
/GPU\_KA  
/GPU\_KB  
/VRAM  
/RAM  
/EMI  
/OD  
/TBT  
@

power optional:

N/A  
/VGA  
@  
@/VGA

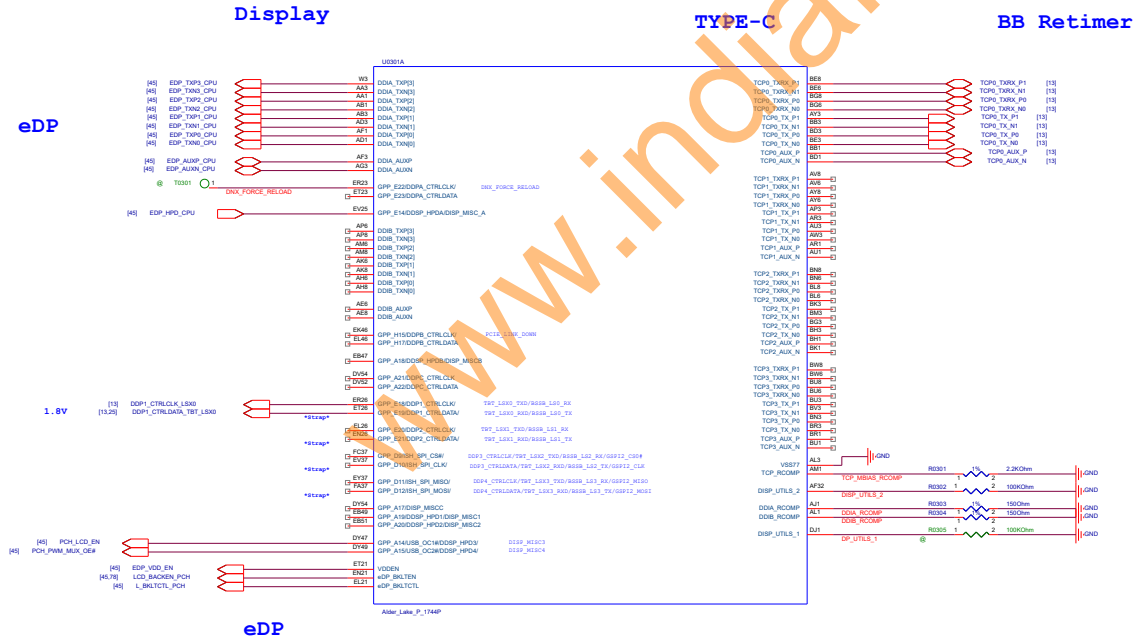
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## PCIE, PEG



PDG: 0.1%

10111-00241000

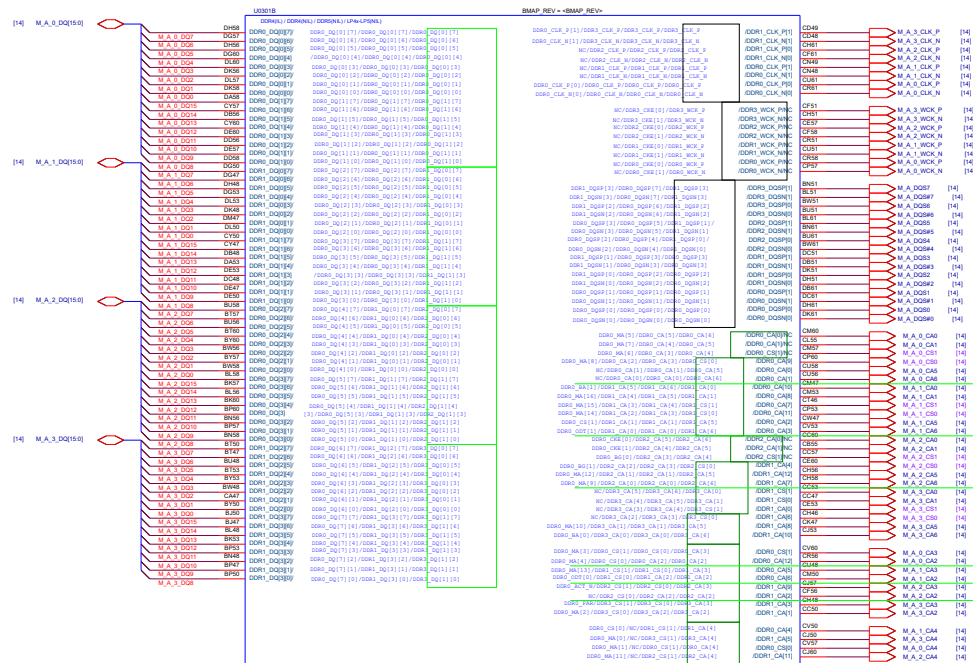


**B: TBT CONN**

eDP RCOMP (DDI RCOMP)  
Trace length > 5 Mils  
Trace Spacing > 12 Mils

## Memory Channel A

## On Board LPDDR5



U1401

U1402

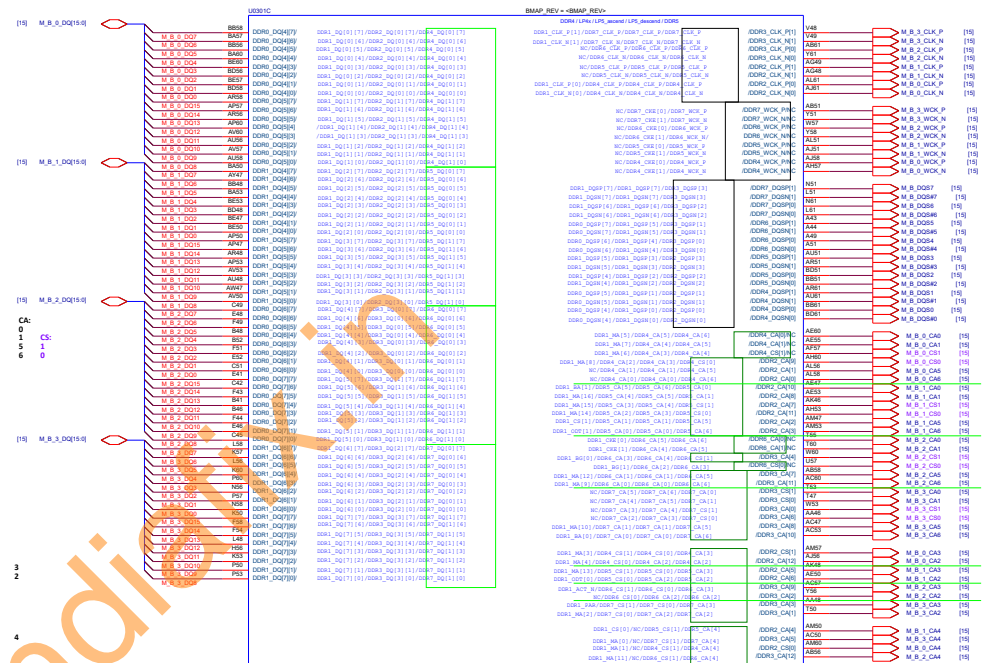
U1501

U1502

Bottom side

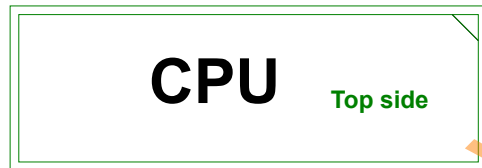
## Memory Channel B

## On Board LPDDR5



## Main Board

Mcu\_Low\_P\_T140P



+1.0V

R4033

100kΩ

%

R4044

60kΩ

M\_A\_RESET#

M\_B\_RESET#

C4001

100nF

3.3V

R4034

100kΩ

R4035

100kΩ

R4036

100kΩ

R4037

100kΩ

R4038

100kΩ

R4039

100kΩ

R4040

100kΩ

R4041

100kΩ

R4042

100kΩ

R4043

100kΩ

R4044

100kΩ

R4045

100kΩ

R4046

100kΩ

R4047

100kΩ

R4048

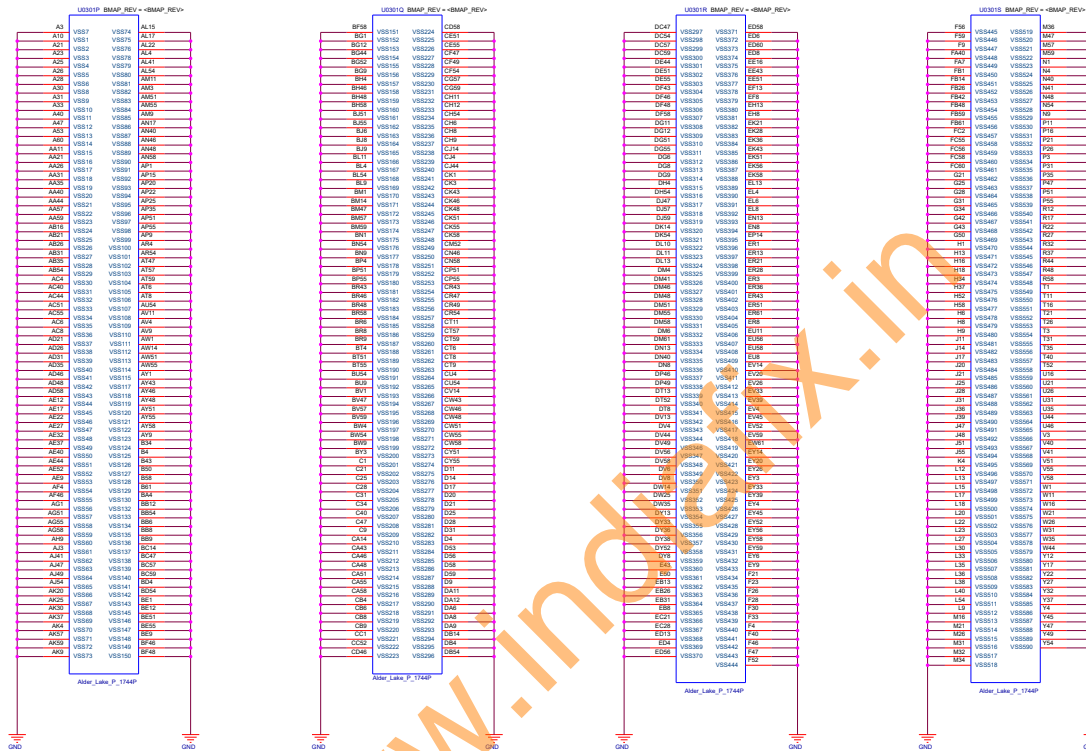
100kΩ

R4049

100kΩ

ASUS		Project Name	Rev
GX5011P2			1.0
Title	CPU DDR		
Size	Dept.	ASUSTAY COMPUTER	Engineer: EE
Date: Monday, October 25, 2021	Sheet	4	of 100





## Configuration

### ADL-P CFG Straps

Processor Internal Pull-Up VCC\_CFG\_PU\_OUT

**Configuration Signals(ADL-P):**  
The CFG signals have a default value of if not terminated on the board.  
Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

CFG[1:0] : Reserved configuration lane.

CFG[2] : PCI Express® Static x8 (010)Lanes Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lane.

CFG[4] : Reserved configuration lane.

CFG[5] : Reserved configuration lane. (For ADL-S)

CFG[6] : Reserved configuration lane.

CFG[8:7] : Reserved configuration lane.

CFG[10:9] : Reserved configuration lanes, but PU

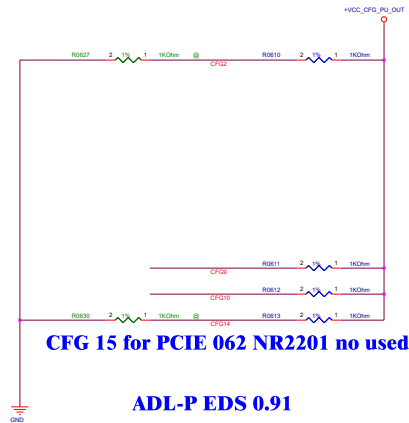
CFG[14] : PEG60 Lane Reversal:

- 1 : (Default) Normal <====
- 0 : Reversed

CFG[15] : PEG62 Lane Reversal:

- 1 : (Default) Normal  $\leftarrow$ mm
- 0 : Reversed

CFG[17:16] : Reserved configuration lanes



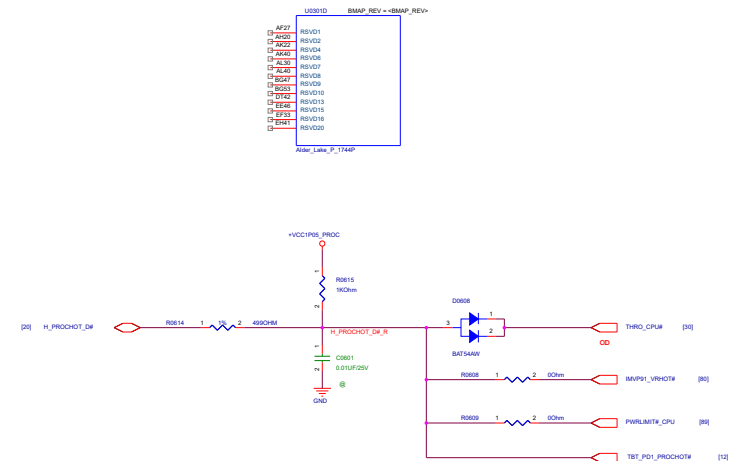
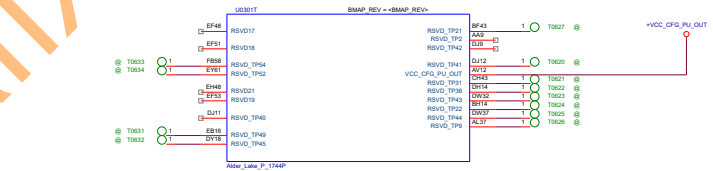
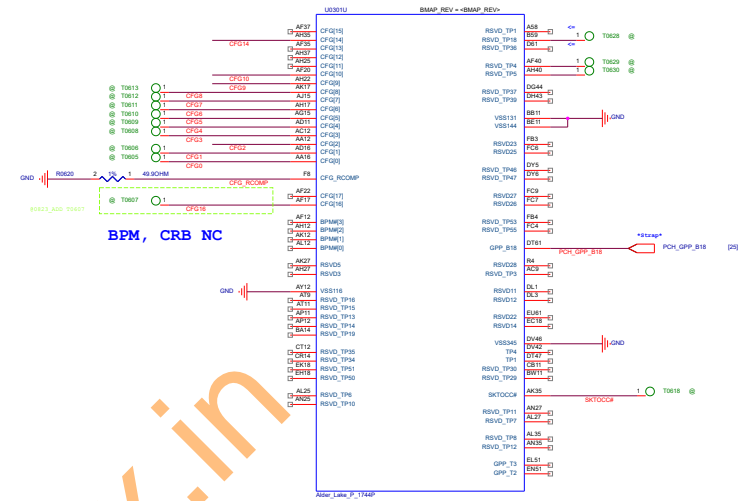
## ADL-P PDG 1.2

## CFG Signals Functionality and Termination

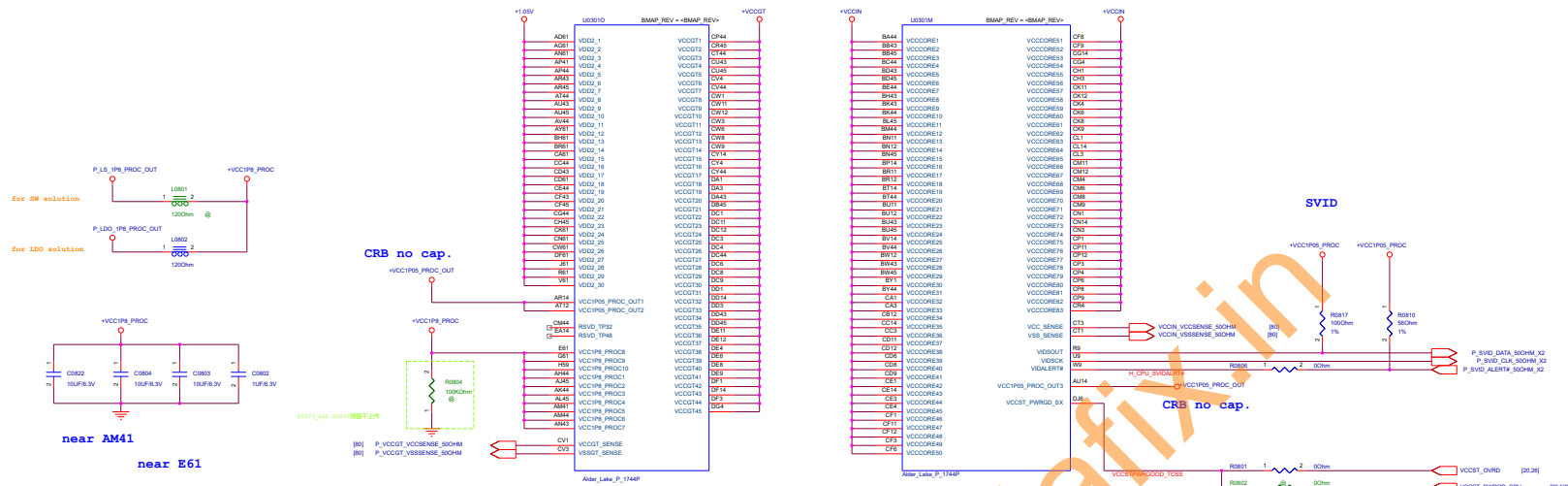
CFG	Description	Termination	Resistor
CFG[0]	RSVD	None	
CFG[1]	RSVD	None	
CFG[2]	PCI Express* Static X8 (PEG 10/11 ) Lane Numbering Reversal <ul style="list-style-type: none"> <li>1: Normal Operation</li> <li>0: Lane Numbers reversed</li> </ul>	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6]	RSVD	NONE	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull -Up to VCC_CFG_PU_OUT <sup>1</sup>	1K Ohm
CFG[13:11]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: <ul style="list-style-type: none"> <li>- 1 - (Default) Normal</li> <li>- 0 - Reversed</li> </ul>	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[15]	PEG62 Lane Reversal: <ul style="list-style-type: none"> <li>- 1 - (Default) Normal</li> <li>- 0 - Reversed</li> </ul>	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[17:16]	RSVD	None	

Note: 1.To ensure reliable boot across HVM.

**Note:** 1.To ensure reliable boot across HVM.



Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[17:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>CFG[1:0]: Reserved configuration</li> <li>CFG[2]: <b>S-Processor Line</b> PCI Express* Static x16 Lanes Numbering Reversal</li> <li>CFG[2]: <b>P-Processor Line</b> PCI Express* Static x8 Lanes Numbering Reversal</li> <li>CFG[2]: <b>M-Processor Line</b> Reserved</li> </ul>	I	GTL	SE	S-Processor Line P-Processor Line M-Processor Line
	<ul style="list-style-type: none"> <li>CFG[3]: Reserved configuration lanes.</li> <li>CFG[4]: Reserved</li> <li>CFG[5] <b>S-Processor Line</b> PCI Express* Bifurcation               <ul style="list-style-type: none"> <li>0 = x8 PCI Express*</li> <li>1 = x16 PCI Express* (default)</li> <li>Reserved</li> </ul> </li> <li>CFG[5] <b>M and P-Processor Line</b> Reserved configuration lanes.</li> <li>CFG[6]: Reserved configuration lanes.</li> <li>CFG[7]: Reserved configuration lanes.</li> <li>CFG[13:8]: Reserved configuration lanes.</li> <li>CFG[14]: <b>S-Processor Line</b> PEG60 Lane Reversal:               <ul style="list-style-type: none"> <li>1 - (Default) Normal</li> <li>0 - Reversed</li> </ul> </li> <li>CFG[14]: <b>P-Processor Line</b> PEG60 Lane Reversal:               <ul style="list-style-type: none"> <li>1 - (Default) Normal</li> <li>0 - Reversed</li> </ul> </li> <li>CFG[15]: <b>P-Processor Line</b> PEG62 Lane Reversal:               <ul style="list-style-type: none"> <li>1 - (Default) Normal</li> <li>0 - Reversed</li> </ul> </li> <li>CFG[14]: <b>M-Processor Line</b> PEG60 Lane Reversal:               <ul style="list-style-type: none"> <li>1 - (Default) Normal</li> <li>0 - Reversed</li> </ul> </li> <li>CFG[17:15]: <b>M and S-Processor Line</b> Reserved configuration lanes.</li> <li>CFG[17:16]: <b>P-Processor Line</b> Reserved configuration lanes.</li> </ul>				



## Processor Power Rails

Power Rail	Description	S Processor Line Controls	P Processor Line Controls	M Processor Line Controls
VCC <sub>CORE</sub>	Processor IA Cores Power Rail	SVID	SVID	SVID
VCC <sub>GT</sub>	Graphic Power Rail	SVID	SVID	SVID
VCC <sub>IN_AUX</sub> <sup>3</sup>	Support internal FIVR's 1, SA, PCIe, Display IO and other internal Blocks	PCH VID	PCH VID	PCH VID
VCC <sub>SA</sub>	Processor System Agent Power Rail	-----	-----	SVID
VCC <sub>IP05_PRO C</sub> <sup>4</sup>	Sustain and Sustain Gated Power Rail	Fixed	Fixed	Fixed
VCC <sub>IP8_PRODC</sub>	PCIe PHY Power 1.8V Rail	Fixed	Fixed	-----
VCC <sub>ANA</sub>	Support internal Analog rails, TCSS, Display, PCIe and other internal Blocks	-----	-----	Fixed
VCC <sub>MIPILP</sub>	DDI PHY power rail for MIPI DSI interface	-----	Fixed	Fixed
VDD2	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	Fixed (Memory technology dependent)	Fixed (Memory technology dependent)

Notes: 1. FIVR = Fully Integrated Voltage Regulator. For details, refer to [Voltage Regulator](#) on page 167.

2. For details regarding each rail's VR, refer to the appropriate PDG ([Related Documents](#) on page 27).

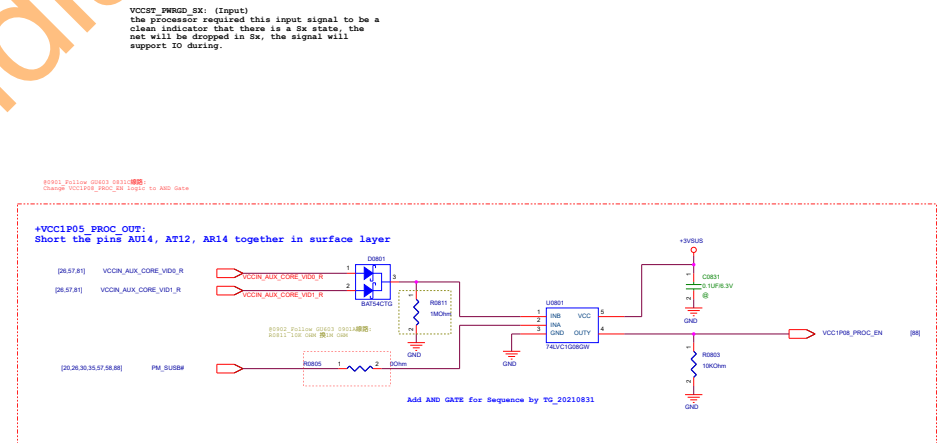
3. VCC<sub>IN\_AUX</sub> has a few discrete voltages defined by PCH VID.

4. VCC<sub>IP05\_PRODC</sub>, for S Processor the power rail is connected to a platform voltage regulator to supply power to the sustaining power rails, for P-Processor line power rail is connected to VCC<sub>IP05\_OUT\_FET</sub> rail through a power gate at platform, to supply power to the sustain gated power rails.

5. VCC<sub>MIPILP</sub>: When MIPI DSI interface is being used, this power rail should be connected to 1.24V rail.

NR2201, ADL-P

```
<= +VCCIN
<= +VCCGT
<= +VCCIN_AUX (Page.26)
<= +VCC1P05_PROC_OUT
<= +VCC1P8_PROC
<= N.C., not be used (Page.26)
<= +1.05V(+VDD2)
```



#### 11.1.1.1.2 VCC1P8\_PROC


Description: VCC1P8\_PROC is the PCIE5 1.8V rail

**Table 735. Reference Layout Design**

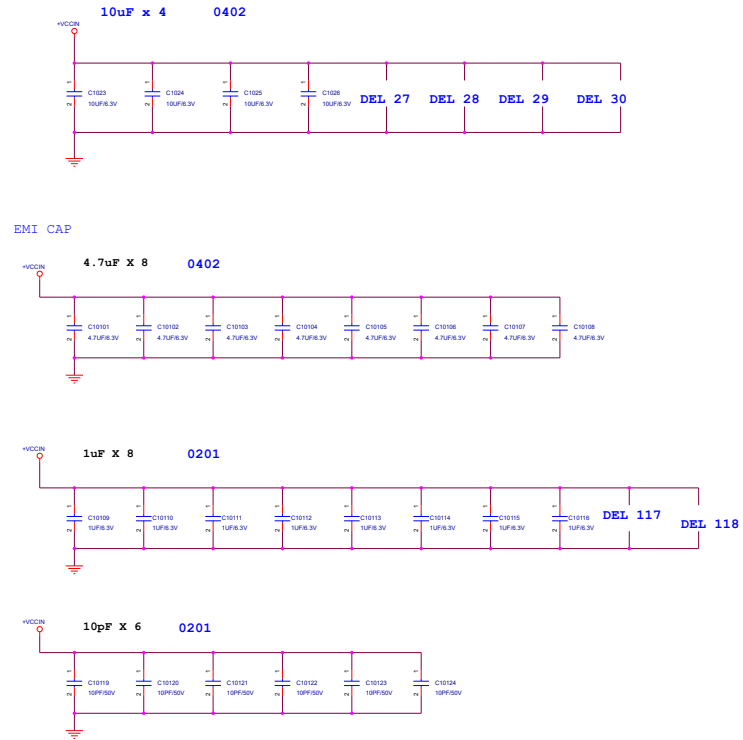
Index	Design Note	Reference Design
1	When using PCIe PEG10 configured to Gen5 or lower, it is recommended to use an LDO solution for this rail. <u>If disabling the PCIE port, these pins can be connected to GND.</u>	VCC1P8_PROC_1

		Project Name <b>GX501IP2</b>		Part <b>R1.0</b>	
Title : <b>CPU_PWR</b>					
Size <b>A2</b>		Dept.: <b>ASUSTek COMPUTER</b>		Engineer: <b>EE</b>	
Date: <b>Monday, October 25, 2021</b>				Sheet <b>8</b> of <b>104</b>	

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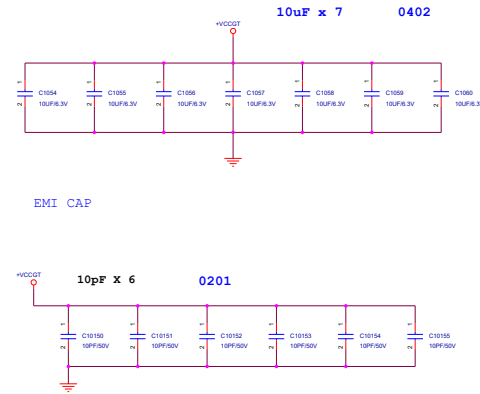
		Project Name	Rev
Title : CPU PWR		GX501IP2	
Rev		1.0	
A2	Dept.: ASUS/TA COMPUTER	Engineer: EE	
Date: Monday, October 25, 2021		Drawn: 0	of 100

## BOTTOM



+VCCGT	1 Phase
--------	---------

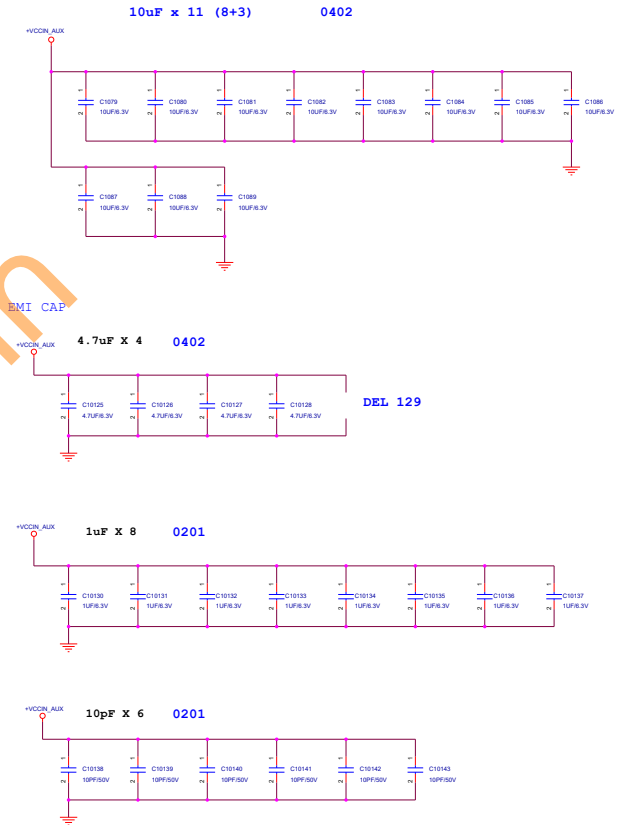
**BOTTOM**



Over 10uF Caps are placed on Power team pages.

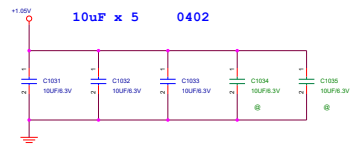
+VCCIN\_AUX 2 Phase

**BOTTOM**

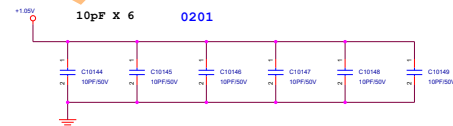


+VDD2 (1.05V)

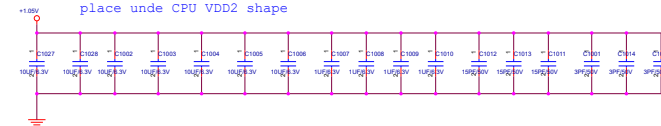
**BOTTOM**



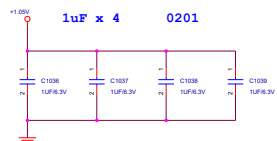
EMI CAP



place unde CPU VDD2 shape

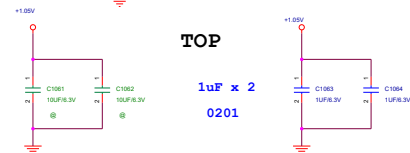


**BOTTOM**



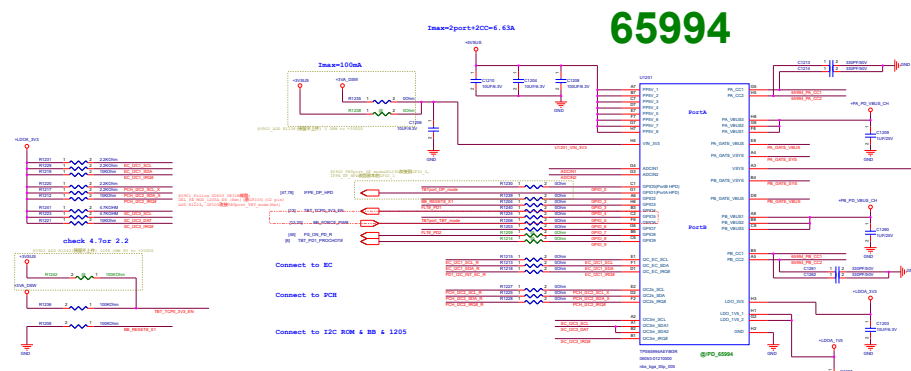
[TOP](#)

TOP

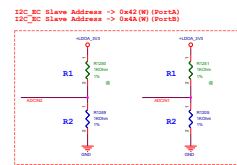


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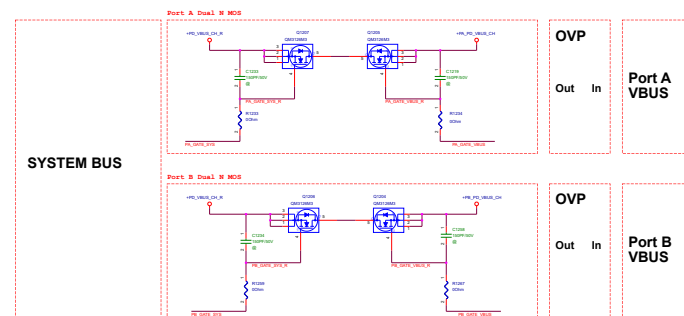
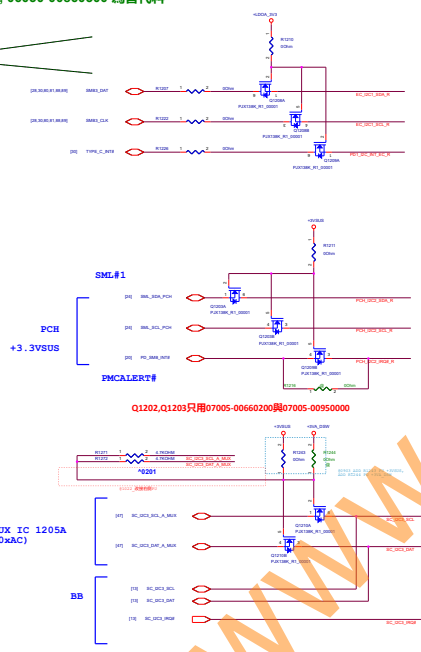
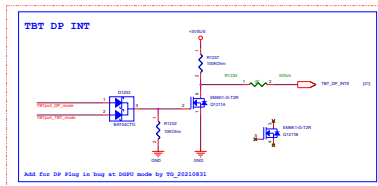
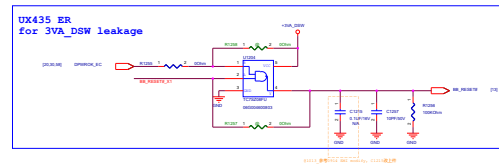
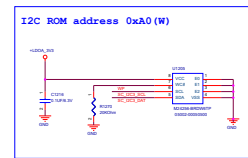
		Project Name	Rev
Title :		GX501IP2	1.0
Size : TBT, TBT IC, DP, R2.0a			
A2	Dept. :	ASUSTEK COMPUTER INC.	Engineer: EE
Date: Monday, October 25, 2021		Drawn: 11	of 100



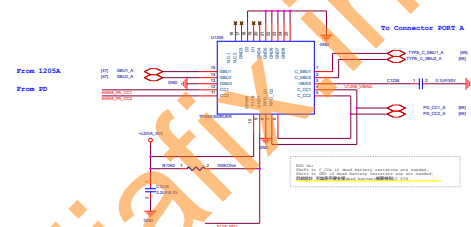
改料號為06050-01210000, PART/SYMBOL不動  
06050-01210000為主料, 06050-00860300 為替代料



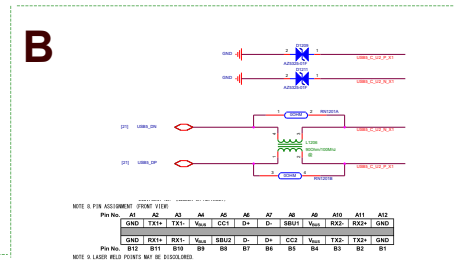
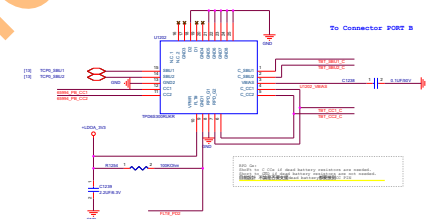
~~65994 for ADL: 06050-00860300~~  
~~After June, use 06050-61170000~~



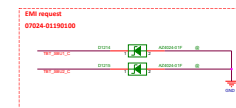
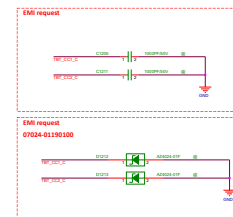
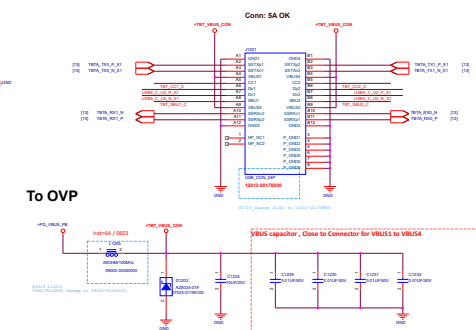
**A: GC CONN**

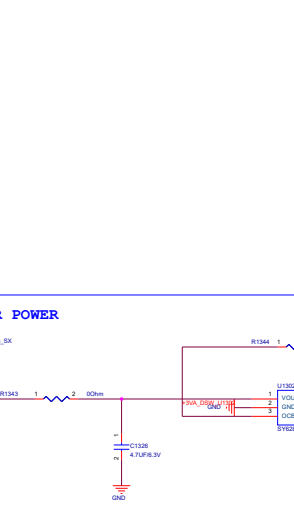
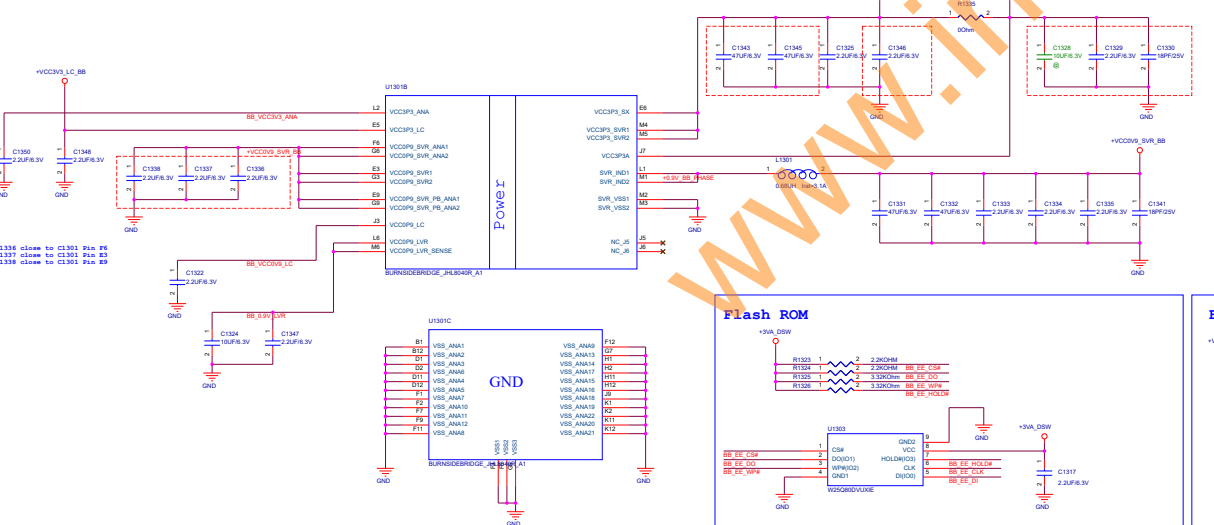
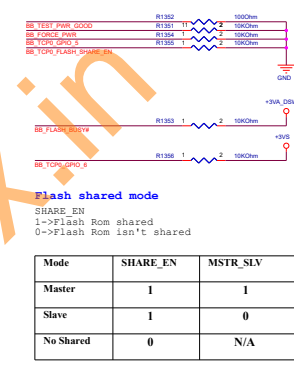
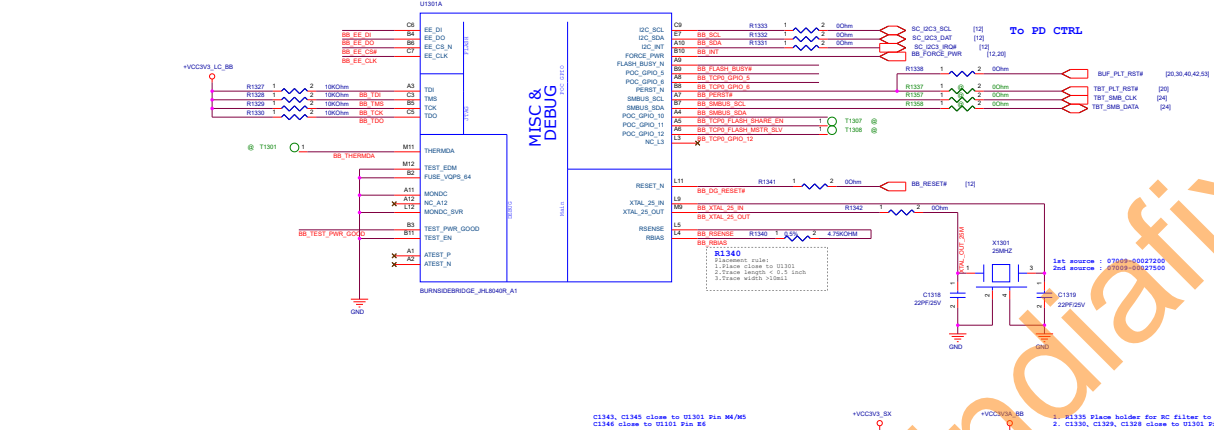
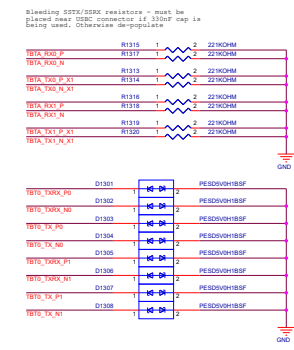
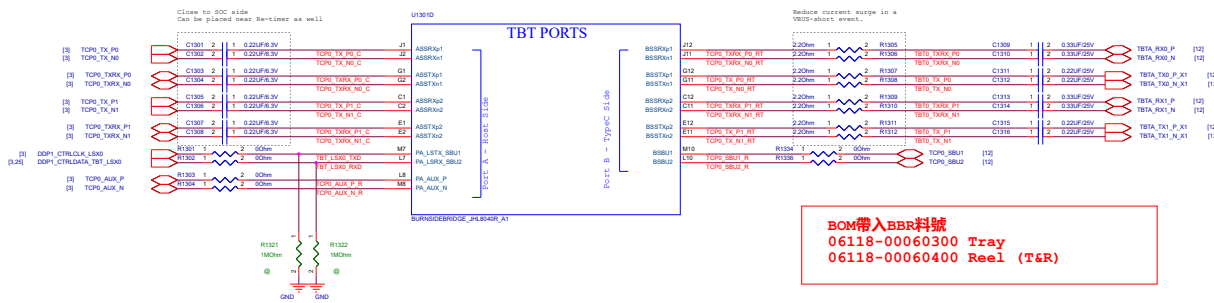


**B: TBT CONN**



### TBT TYPE-C Connector







LPDDR5 Channel A

DRAM 1 of 4

CH #0

CH #1

distribute  
among all DRAMs

Close to U1401

VDD2

VDDQ

VDD1

DRAM 2 of 4

CH #2

CH #3

distribute  
among all DRAMs

Close to U1402

VDD2

VDDQ

VDD1

VDDQ: 0.5V  
VDD2L: 0.9V  
VDD2H: 1.05V  
VDD1: 1.8V

Temp Connection



U1402B

U1402C

U1402D

U1402E

U1402F

U1402G

U1402H

U1402I

U1402J

U1402K

U1402L

U1402M

U1402N

U1402O

U1402P

U1402Q

U1402R

U1402S

U1402T

U1402U

U1402V

U1402W

U1402X

U1402Y

U1402Z

U1402AA

U1402AB

U1402AC

U1402AD

U1402AE

U1402AF

U1402AG

U1402AH

U1402AI

U1402AJ

U1402AK

U1402AL

U1402AM

U1402AN

U1402AO

U1402AP

U1402AQ

U1402AR

U1402AS

U1402AT

U1402AU

U1402AV

U1402AW

U1402AX

U1402AY

U1402AZ

U1402BA

U1402BB

U1402BC

U1402BD

U1402BE

U1402BF

U1402BG

U1402BH

U1402BI

U1402BJ

U1402BK

U1402BL

U1402BM

U1402BN

U1402BO

U1402BP

U1402BQ

U1402BR

U1402BS

U1402BT

U1402BU

U1402BV

U1402BW

U1402BX

U1402BY

U1402BZ

U1402CA

U1402CB

U1402CC

U1402CD

U1402CE

U1402CF

U1402CG

U1402CH

U1402CI

U1402CJ

U1402CK

U1402CL

U1402CM

U1402CN

U1402CO

U1402CP

U1402CQ

U1402CR

U1402CS

U1402CT

U1402CU

U1402CV

U1402CW

U1402CX

U1402CY

U1402CZ

U1402DA

U1402DB

U1402DC

U1402DD

U1402DE

U1402DF

U1402DG

U1402DH

U1402DI

U1402DJ

U1402DK

U1402DL

U1402DM

U1402DN

U1402DO

U1402DP

U1402DQ

U1402DR

U1402DS

U1402DT

U1402DU

U1402DV

U1402DW

U1402DX

U1402DY

U1402DZ

U1402EA

U1402EB

U1402EC

U1402ED

U1402EE

U1402EF

U1402EG

U1402EH

U1402EI

U1402EJ

U1402EK

U1402EL

U1402EM

U1402EN

U1402EO

U1402EP

U1402EQ

U1402ER

U1402ES

U1402ET

U1402EU

U1402EV

U1402EW

U1402EX

U1402EY

U1402EZ

U1402FA

U1402FB

U1402FC

U1402FD

U1402FE

U1402FF

U1402FG

U1402FH

U1402FI

U1402FJ

U1402FK

U1402FL

U1402FM

U1402FN

U1402FO

U1402FP

U1402FQ

U1402FR

U1402FS

U1402FT

U1402FU

U1402FV

U1402FW

U1402FX

U1402FY

U1402FZ

U1402GA

U1402GB

U1402GC

U1402GD

U1402GE

U1402GF

U1402GG

U1402GH

U1402GI

U1402GJ

U1402GK

U1402GL

U1402GM

U1402GN

U1402GO

U1402GP

U1402GQ

U1402GR

U1402GS

U1402GT

U1402GU

U1402GV

U1402GW

U1402GX

U1402GY

U1402GZ

U1402HA

U1402HB

U1402HC

U1402HD

U1402HE

U1402HF

U1402HG

U1402HH

U1402HI

U1402HJ

U1402HK

U1402HL

U1402HM

U1402HN

U1402HO

U1402HP

U1402HQ

U1402HR

U1402HS

U1402HT

U1402HU

U1402HV

U1402HW

U1402HX

U1402HY

U1402HZ

U1402IA

U1402IB

U1402IC

U1402ID

U1402IE

U1402IF

U1402IG

U1402IH

U1402II

U1402IJ

U1402IK

U1402IL

U1402IM

U1402IN

U1402IO

U1402IP

U1402IQ

U1402IR

U1402IS

U1402IT

U1402IU

U1402IV

U1402IW

U1402IX

U1402IY

U1402IZ

U1402JA

U1402JB

U1402JC

U1402JD

U1402JE

U1402JF

U1402JG

U1402JH

U1402JI

U1402JJ

U1402JK

U1402JL

U1402JM

U1402JN

U1402JO

U1402JP

U1402JQ

U1402JR

U1402JS

U1402JT

U1402JU

U1402JV

U1402JW

U1402JX

U1402JY

U1402JZ

U1402KA

U1402KB

U1402KC

U1402KD

U1402KE

U1402KF

U1402KG

U1402KH

U1402KI

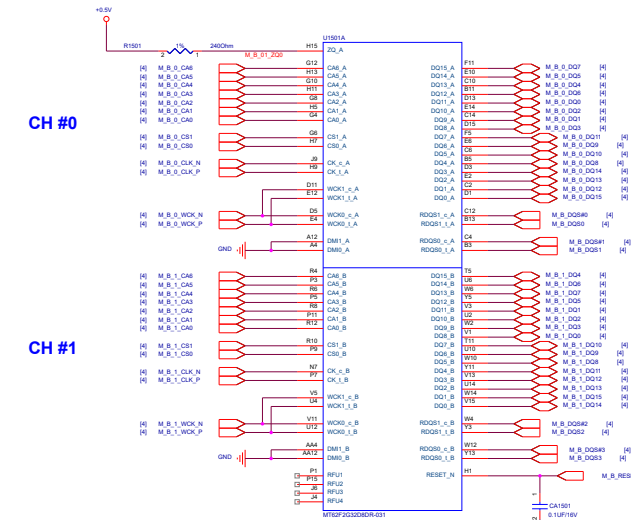
U1402KJ

U1402KK

U

## LPDDR5 Channel B

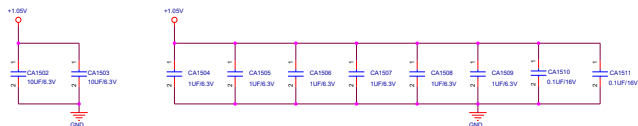
DRAM 3 of 4



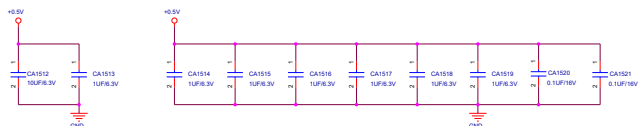
distribute  
among all DRAMs

Close to U1501

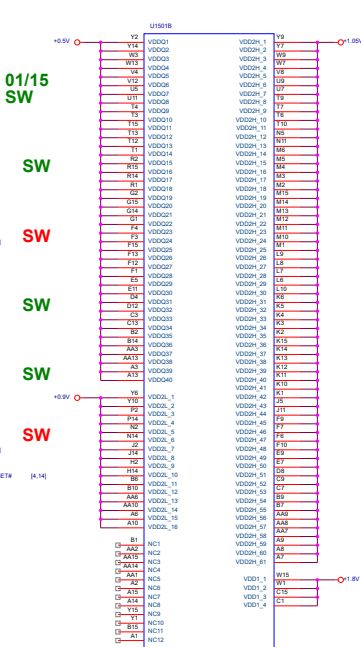
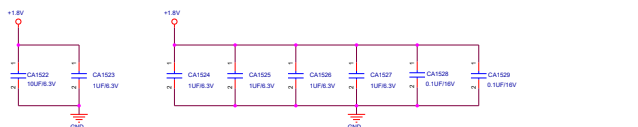
## VDD2



## VDDQ

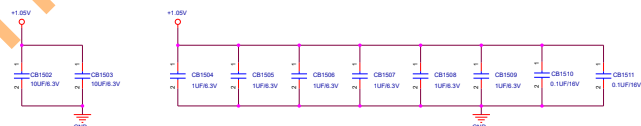


**VDD1**

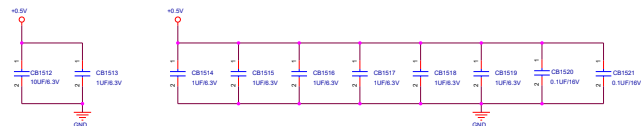


distribute  
among all DRAMs

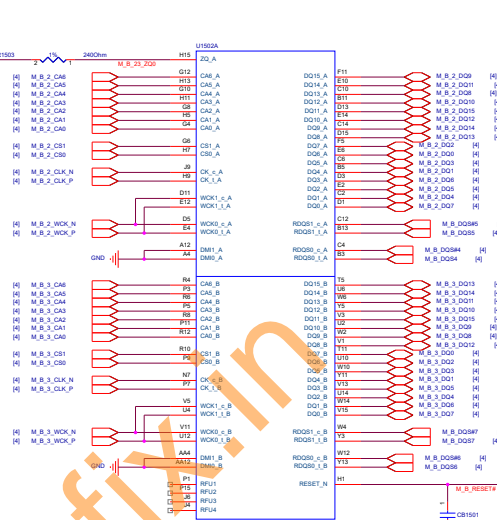
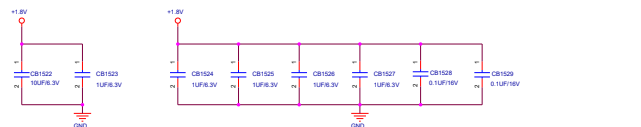
VDD2



## VDDQ

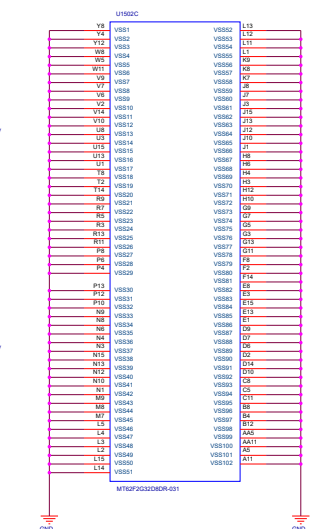
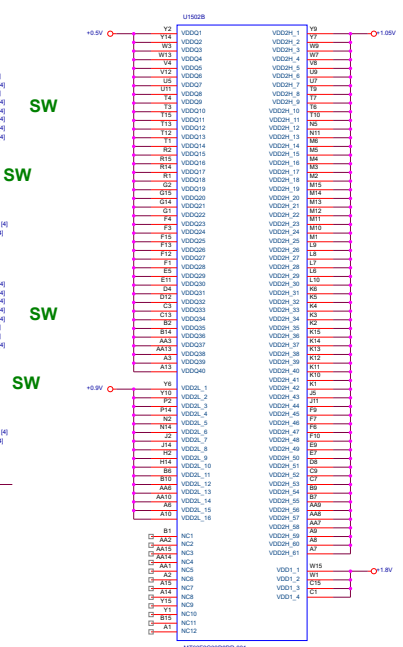


**VDD1**



Close to U1502

**Close**



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		Title : LPDDR5	
ASUS/SAI COMPUTER INC.		Engineer: EE	
Size	Project Name		Rev
A2	OX501IP2		1.0
Date: Monday, October 25, 2021		Printed: 15	of 104

www.indiafix.in

		Title : LPDDR5	
ASUS/SAI COMPUTER INC.		Engineer: EE	
Size	Project Name		Rev
A2	OX501IP2		1.0
Date: Monday, October 25, 2021		Printed: 17	of 104

www.indiafix.in

		Title : LPDDR5	
ASUS/SAI COMPUTER INC.		Engineer: EE	
Size	Project Name		Rev
A2	OX501IP2		1.0
Date: Monday, October 25, 2021		Printed: 15	of 104

www.indiafix.in

		Title : DDR_TERMINATION	
ASUS/SAI COMPUTER INC.		Engineer: EE	
Size	Project Name		Rev
A2	OX501IP2		1.0
Date: Monday, October 25, 2021		Printed: 15	of 104



USB Configuration

USB 2.0	Function
USB2_01	TYPE-C PORT A (USB+GPU DP)
USB2_02	IO BOARD USB2.0 TYPE-A
USB2_03	REAR CAMERA
USB2_04	NC
USB2_05	TYPE-C PORT B (TBT 4)
USB2_06	EXT. POGO CONN
USB2_07	FINGER PRINTER
USB2_08	FRONT CAMERA
USB2_09	N-KEY
USB2_10	WLAN BT

ADL-P HSIO Configuration

HSIO Lanes	PCIe Gen 1/2/3	USB3.2 Gen 1x1/2x1	GbE	UFS 1x2	SATA	NR2201 setting	Device
#00	PCIe #01	USB3.2 #01				USB3.2 #01	Type-C (J6901)
#01	PCIe #02	USB3.2 #02					
#02	PCIe #03	USB3.2 #03					
#03	PCIe #04	USB3.2 #04					
#04	PCIe #05						
#05	PCIe #06		GbE				
#06	PCIe #07		GbE			PCIe #07	Card Reader (UA201)
#07	PCIe #08		GbE			PCIe #08	WLAN (US302)
#08	PCIe #09			Lane0			
#09	PCIe #10			Lane1			
#10	PCIe #11				SATA 0		
#11	PCIe #12				SATA 1		

ADL-P HSIO Lane

Flexible HSIO Lane Multiplexing in PCH-P

PCH-P	Flex HSIO Lanes										
	0	1	2	3	4	5	6	7	8	9	10
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11

WLAN  
US302

Card Reader  
UA201

On Board device  
TX & RX CAP @ WLAN PAGE

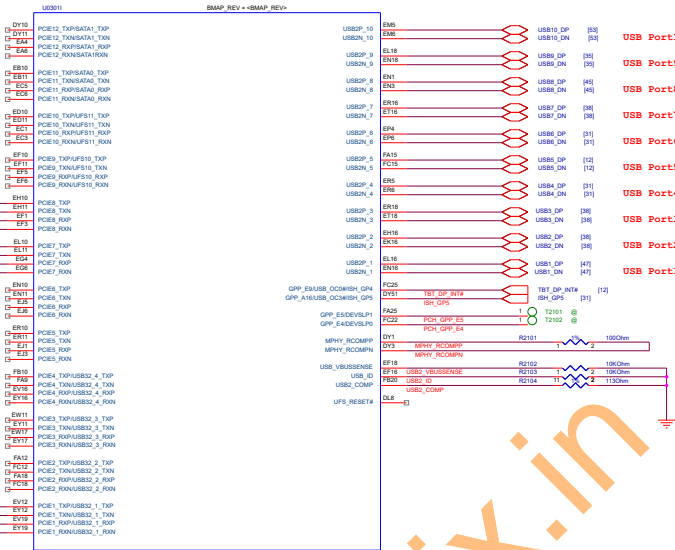
On Board device  
TX & RX CAP @ CR PAGE

A: GC CONN

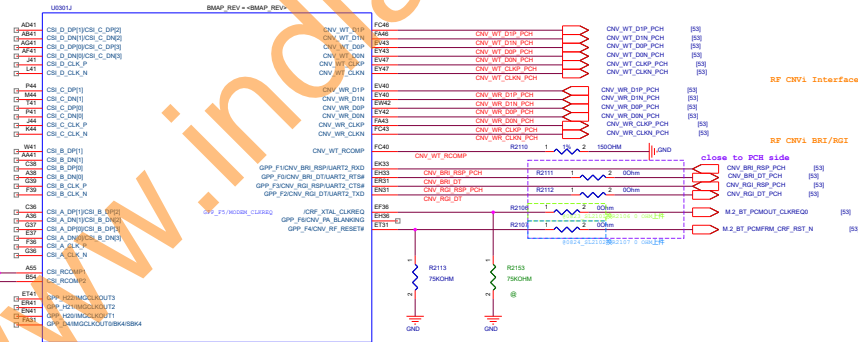
USB3.2 GEN2 Type-C  
(+GPU Display port)

J6901

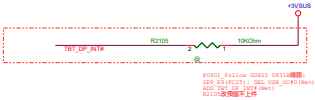
UL\_LUTXDP1  
UL\_LUTXDP1  
UL\_LUTXDP1  
UL\_LUTXDP1



Adax\_Label\_P\_1744P



Adax\_Label\_P\_1744P



BT  
NKEY  
FRONT CAMERA  
Finger Printer  
POGO PIN  
TYPE-C Port B (TBT)  
Sensor Hub NUC126N4AE  
REAR CAMERA @ Daughter Board  
USB 2.0 port @ Daughter Board  
TYPE-C PORT A (+dGPU DP)

\*Strap\*  
CNV\_BRL\_DT  
CNV\_RGL\_DT



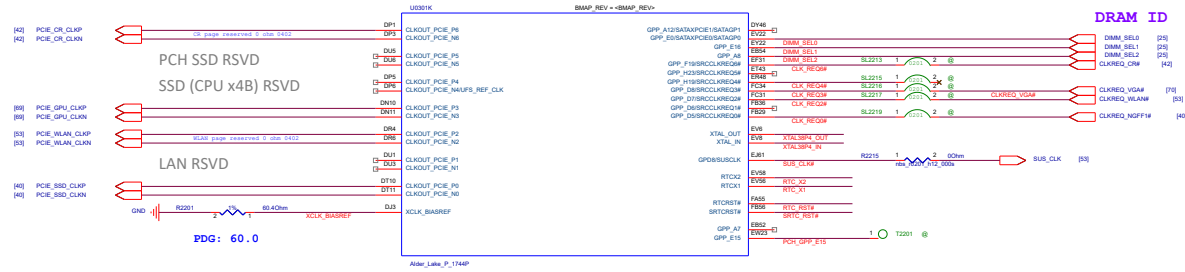
The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express\* Root Ports while using any of the CLKOUT\_PCIE\_P/N differential pairs

Card reader

GPU (CPU x8)

WLAN

SSD (CPU x4A)



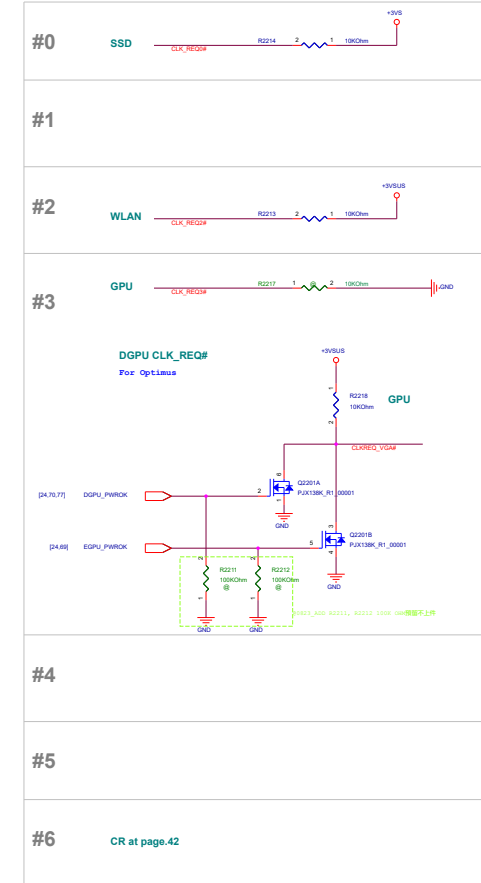
CLKOUT_0	Function	PCIe* Gen1/2/3 support	PCIe* Gen4 support
CLKOUT_1	CPU SSD A	V	V
CLKOUT_2	WLAN	V	
CLKOUT_3	GPU	V	V
CLKOUT_4		V	V
CLKOUT_5		V	
CLKOUT_6	Card Reader	V	

- CLKOUT\_PCIE\_P/N [6:0] = Can be used for PCIe\* Gen1, Gen2, and Gen3 support  
- CLKOUT\_PCIE\_P/N [4, 3, 0] = Must be used for PCIe\* Gen4 support

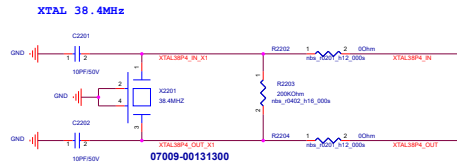
CLKREQ_0	Function	External PU 10K
CLKREQ_1	CPU SSD	V
CLKREQ_2	WLAN	V
CLKREQ_3	GPU	V
CLKREQ_4		
CLKREQ_5		
CLKREQ_6	Card Reader	V

The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express\* Root Ports while using any of the CLKOUT\_PCIE\_P/N differential pairs

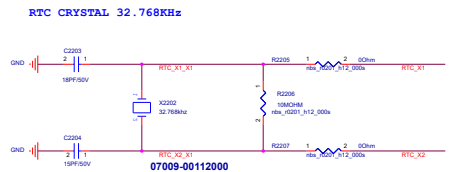
## PCH CLKREQ Setting:



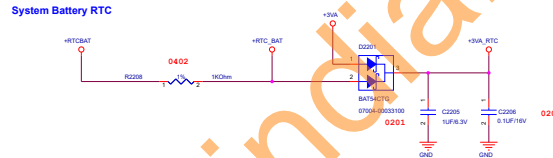
PDG: 15PF



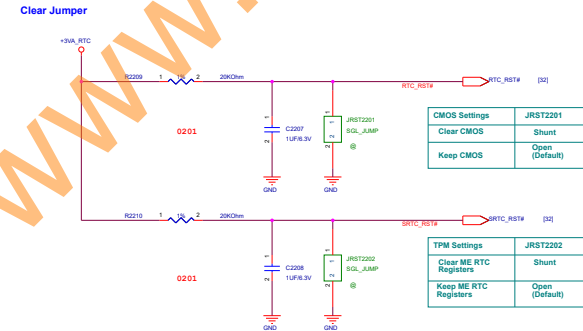
PDG: 18PF




## System Battery RTC

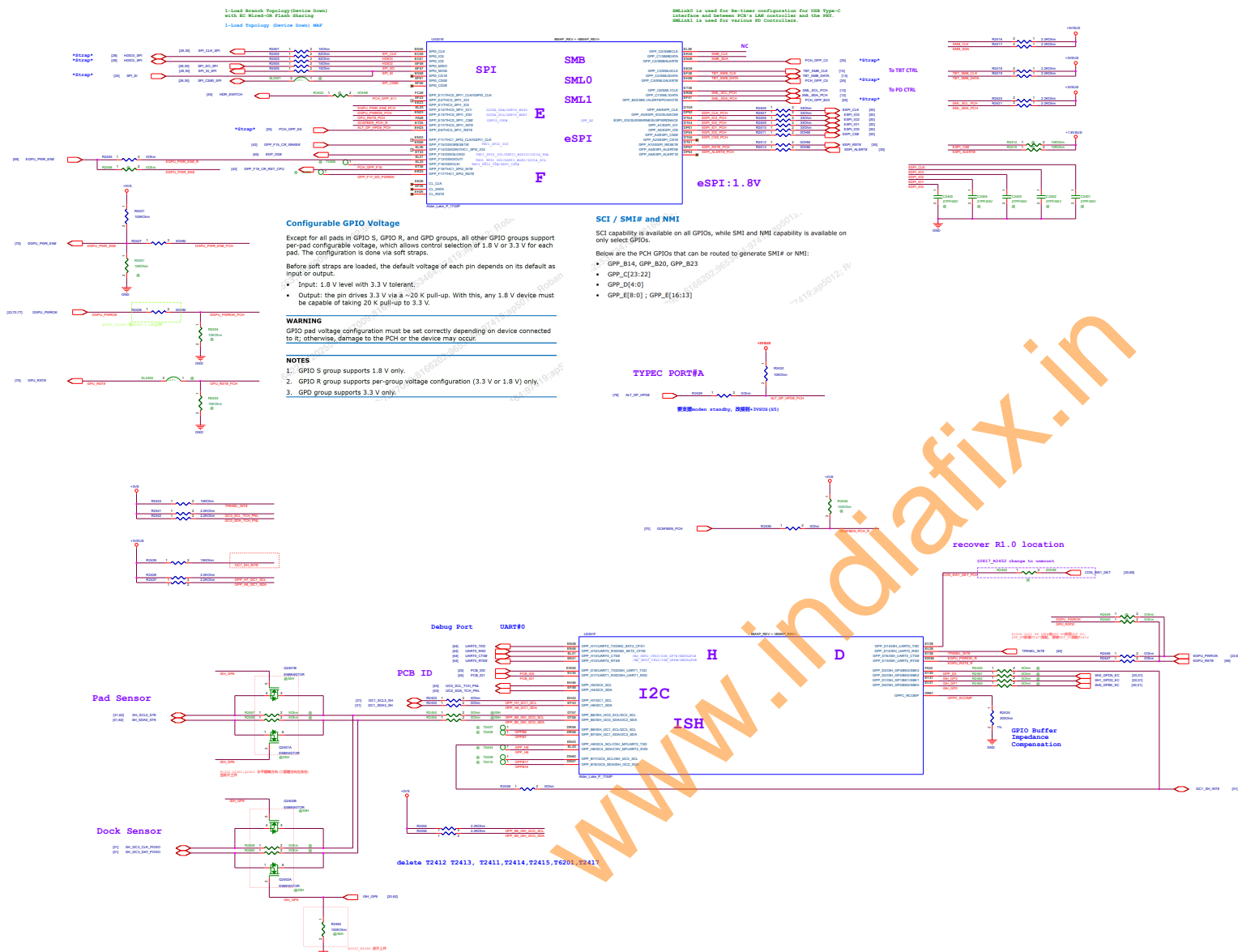


## Clear Jumper



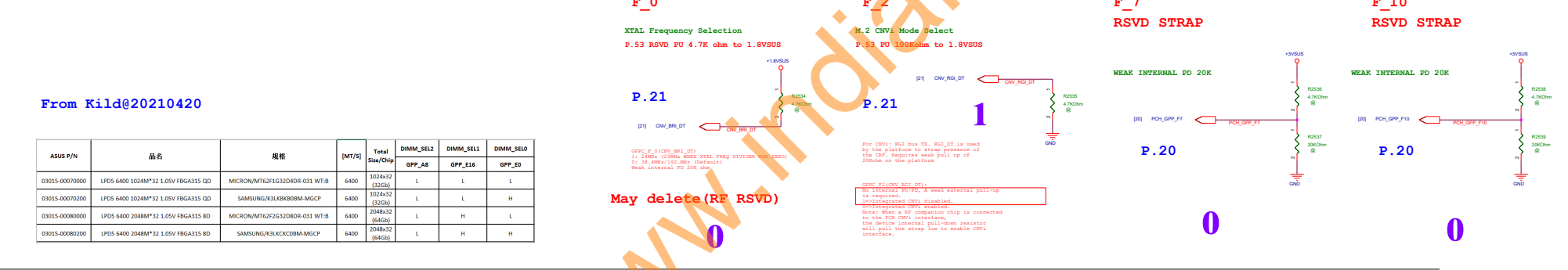
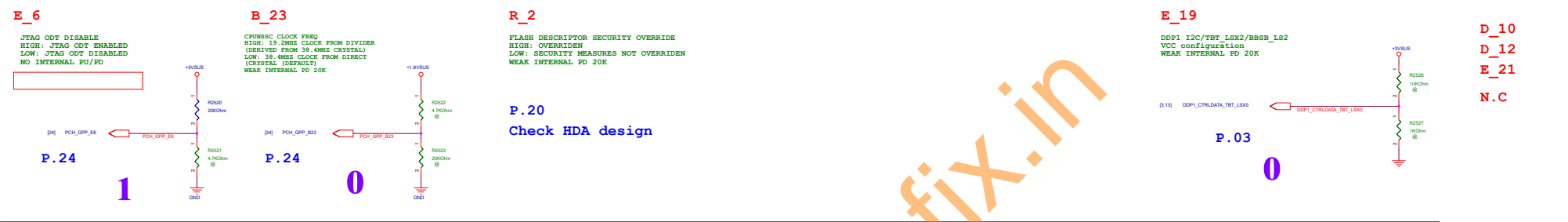
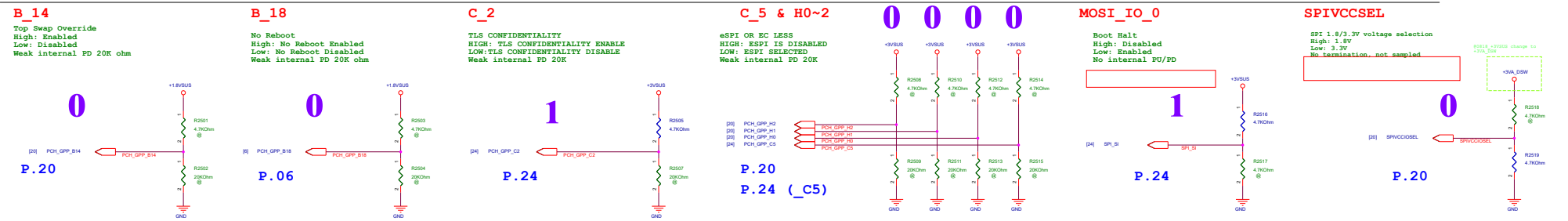
www.indiafix.in

		Project Name	Rev
Title :		GX501IP2	1.0
Size : PCH(4)			
Rev	Dept. :	ASUSTEK COMPUTER	Engineer: EE
A2			
Date: Monday, October 25, 2021	Sheet	23	of 100



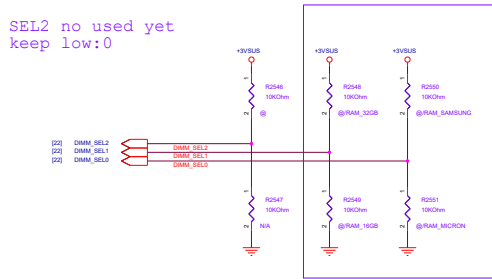
Pin Straps

Main Board

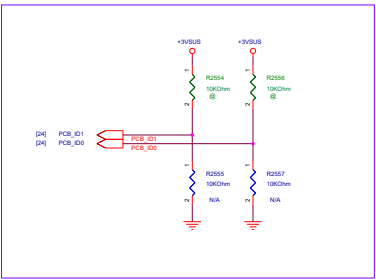


ID pin

SEL2 no used yet  
keep low:0



	LPDDR5 Memory Down pool (TBD)	DIMM_SEL2	DIMM_SEL1	DIMM_SEL0	System Capacity
#0	Micron 32Gb 03015-00070000 LPD5 6400 1024M*32 1.05V FBGA315 QD MICRON/MT62F1G32D40R-031 WT-B	0	0	0	16GB
#1	Samsung 32Gb 03015-00070400 LPD5 6400 1024M*32 1.05V FBGA315 DD SAMSUNG/K3LKBK80BM-MGCP	0	0	1	16GB
#2	Micron 64Gb 03015-00080000 LPD5 6400 2048M*32 1.05V FBGA315 BD MICRON/MT62F2G32D80R-031 WT-B	0	1	0	32GB
#3	Samsung 64Gb 03015-00080400 LPD5 6400 2048M*32 1.05V FBGA315 QD SAMSUNG/K3LKBK80BM-MGCP	0	1	1	32GB




BOM Optional

BOM Optional

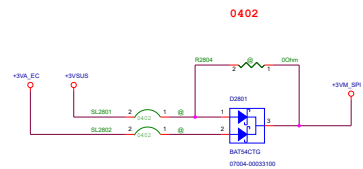
ASUS	Project Name	Rev
GX5011P2		1.0
Title: PCH(S)		
Size	Dept.: ASUS/TA COMPUTER	Engineer: EE
A2	Date: Monday, October 25, 2021	Drawn: 25 of 100



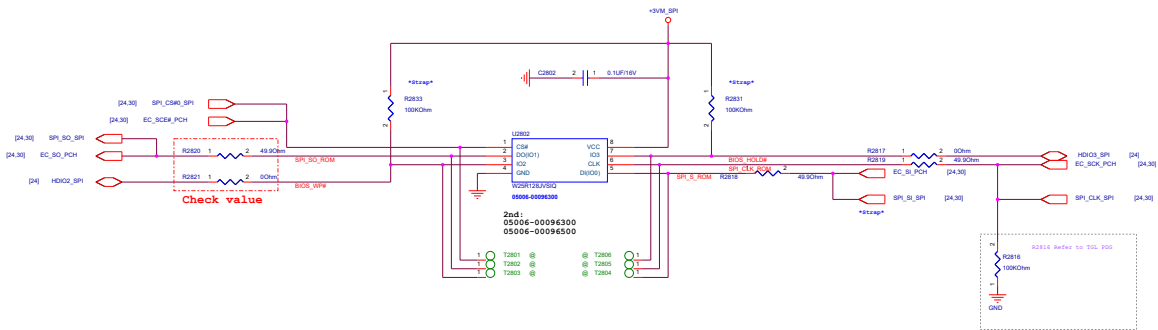
www.indiafix.in

		Project Name	Rev
Title :		GX501IP2	1.0
Size		PCH-CPT(8) POWER.GND	
A2	Dept.:	ASUSTEK COMPUTER	Engineer: EE
Date: Monday, October 25, 2021		Sheet	27 of 100

SPI Power

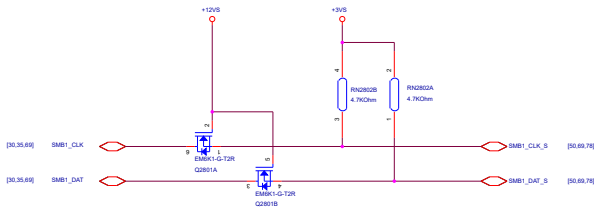


1st SPI ROM



EC (SMB1) @EC side PU +3VA\_EC

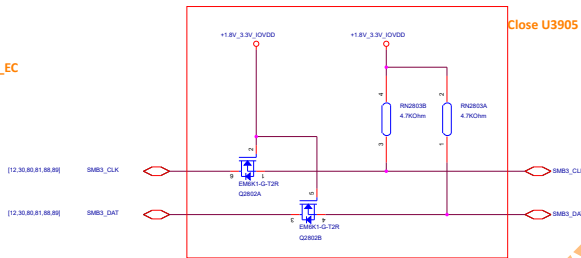
P69: GC CONN  
P35: N KEY



P50: Thermal Sensors(CPU, GPU, VRAM)  
P69: GC CONN PCIE redriver  
P78: GPU

EC (SMB3) @EC side PU +3VA\_EC

P12: PD Controller  
P80 81: IMVP9.1 controller  
P89: Slave charger



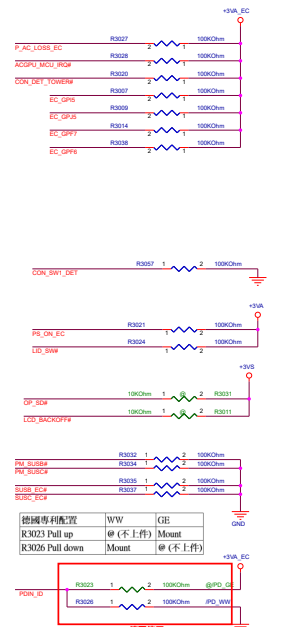
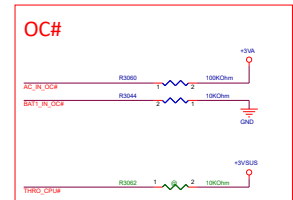
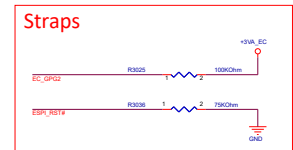
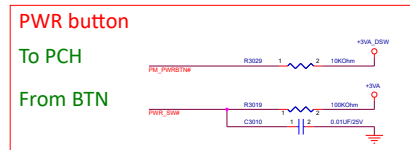
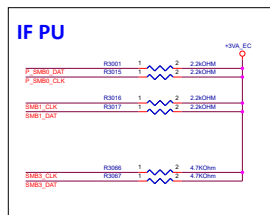
P39: Audio AMP

ASUS		Project Name	Rev
GX501IP2			1.0
Title: SPI ROM.SMB			
Rev	Dept.: ASUS/TA COMPUTER	Engineer:	NR EE RDS
A2	Date: Monday, October 25, 2021		Drawn: 25 of 154

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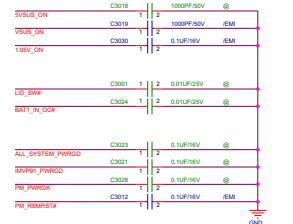
<Unlink Name>		
File		
<Title>		
File	Document Number	1.2
AD	GAD0102	
Date	Monday, October 25, 2021	Print 20 of 104





德國專利配置	WW	GE
R3023 Pull up	@ (不上件)	Mount
R3026 Pull down	Mount	@ (不上件)

@0817\_Note: PD\_GE for 德國使用  
For EMI RSVD





# Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

## 6.6.2 Power button behavior

If the Power button is implemented, it must meet the following requirements:

When the device is off, pressing the power button must turn on the device. In addition, the device must show activity when it is turned on (such as vibrating or turning on the display).

The device must implement a hardware timer to allow for either turning off the device or power cycling the device (turning off the device and then turning it on again) regardless of the current state of the device. This must be implemented by using at least one of the following options:

Press and hold the Power button.

Press and hold the Power button and the Volume Down button at the same time.

Either of these button options must start the hardware timer. The duration of the timer must be as follows:

For devices that run Windows 10 for desktop editions and support low power idle states, the timer must be 10 seconds.

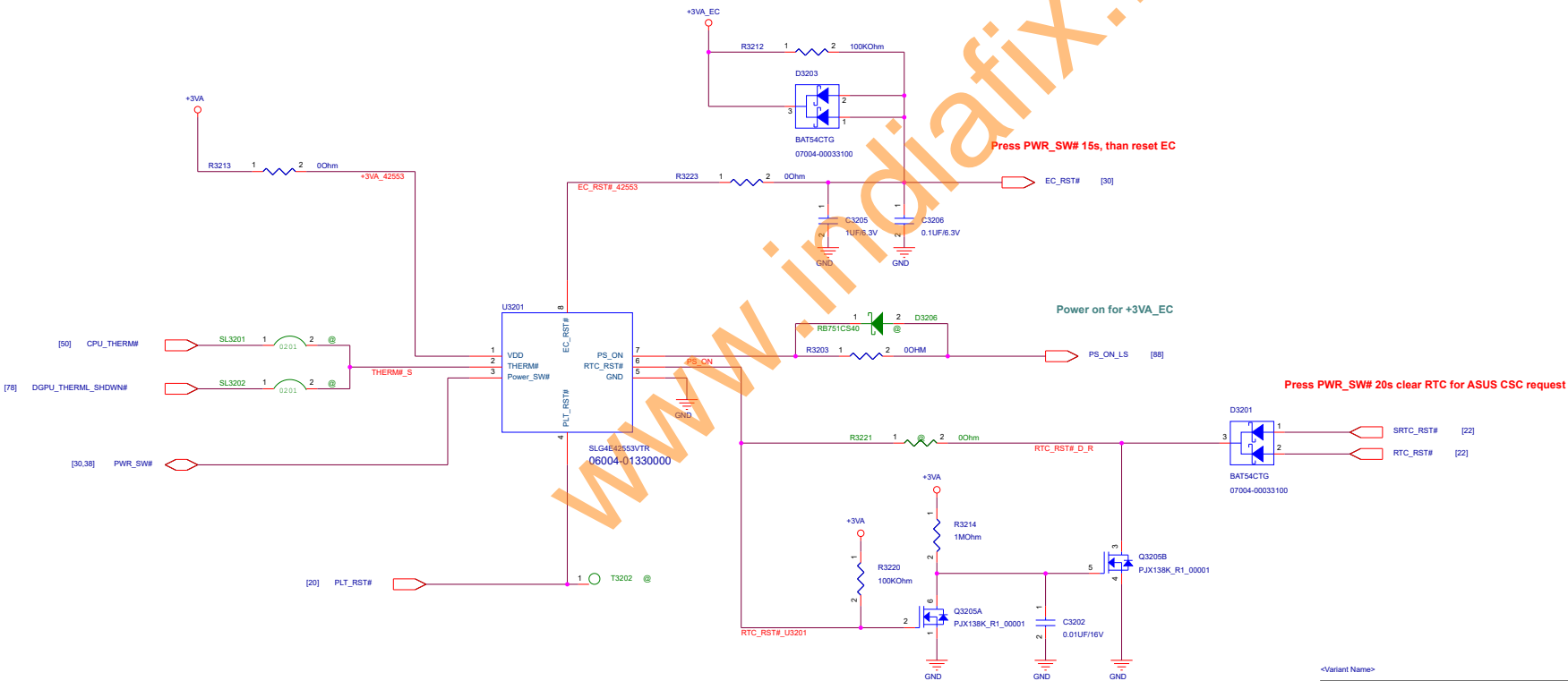
For devices that run Windows 10 for desktop editions but do not support low power idle states, or for devices that run Windows Server 2016, the timer must be 4 seconds.

For devices that run Windows 10 Mobile, the timer must be 10 seconds.

For a definition of a device that supports low power idle states, see 6.6.1.


Releasing any of the buttons used to start the timer must stop the timer. Upon expiration of the timer, the device must either power cycle or turn off the device.

Note We recommend that the Power and Volume Down combination be used to start a power cycle on devices where the display is the only sign of life (for example, devices with no fan or LED).



ASUS		Title : Reset Circuit	
ASUSTeK COMPUTER INC. NB4		Engineer: EE	
Size	Project Name	Rev	
A3	GX501IP2	1.0	
Date	Monday, October 25, 2021	Sheet	32 of 104

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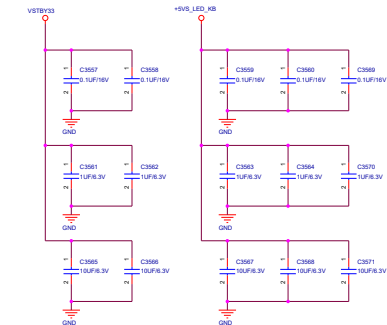
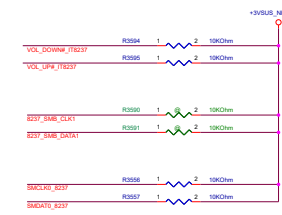
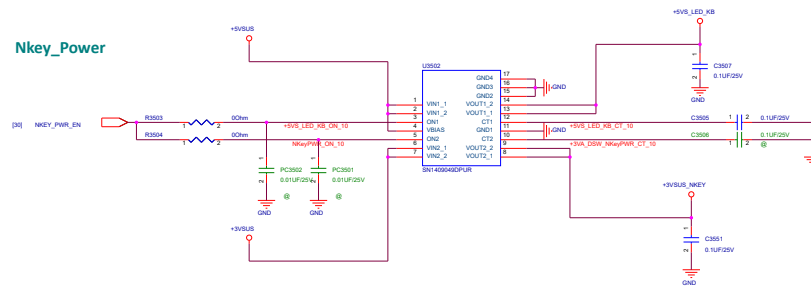
		Project Name	Rev
		GX501IP2	1.0
Title : LAN, CHP			
Size	Dept.: ASUS&A COMPUTER INC. Engineer: NR EE RD3		
A3			
Date: Monday October 25, 2021	Sheet	33	of 104

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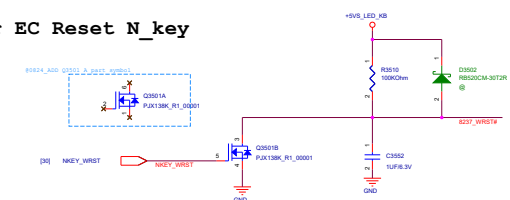
		Project Name	Rev
Title :		GX501IP2	1.0
LAN RJ45 CON			
Bin	Dept.:	ASUSTek COMPUTER	Engineer: NR EE RD3
A3			
Date: Monday, October 25, 2021	Sheet	34	of 104

## IT8237

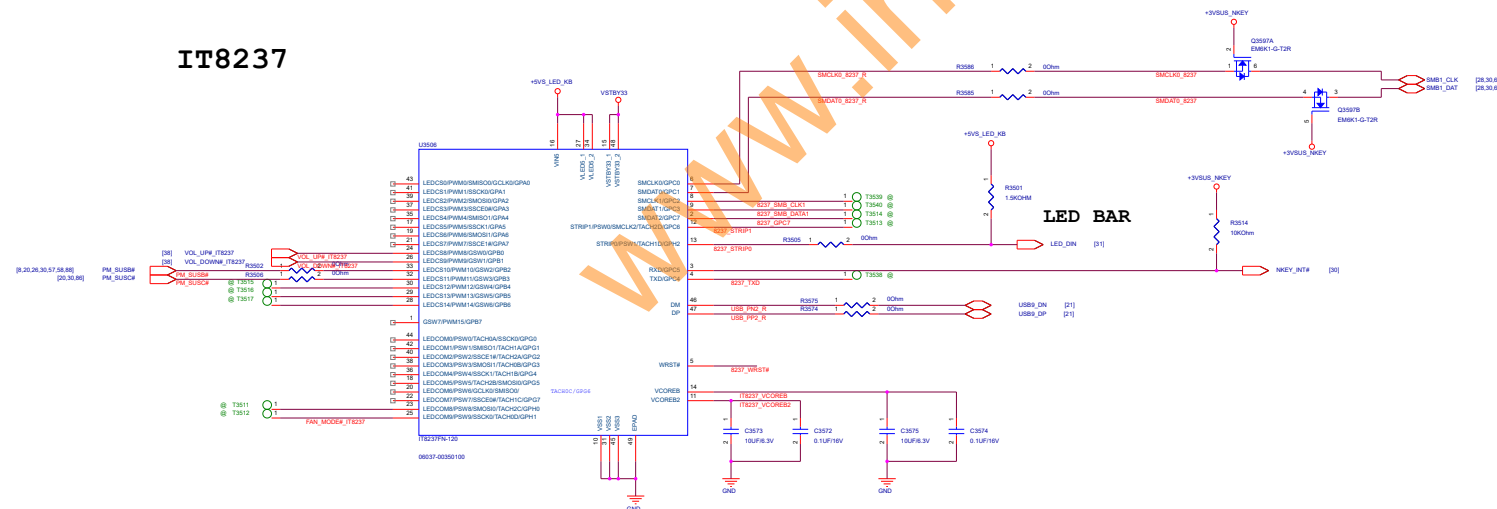
## Nkey\_Power



For EC Reset N\_key



## IT8237



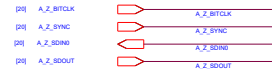
		<b>Title :</b> IT8237	
<b>ASUSTek COMPUTER</b>		<b>Engineer:</b> Gaming RD	
<b>Size</b>	<b>Project Name</b>		<b>Rev</b>
A2	<b>GX501P2</b>		1.0
<b>Date:</b>	<b>Monday, October 25, 2021</b>	<b>Printed:</b>	35 of 104

### \*\*\* POWER



### \*\*\* SINGAL

#### \*\* PCH Control



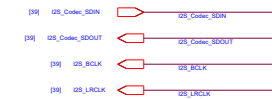
#### \*\* EC Control



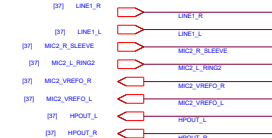
#### \*\* Jack Control



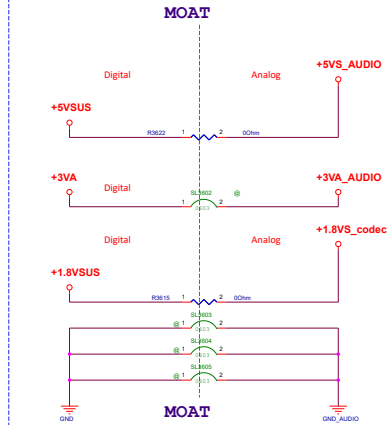
#### \*\*\* To EXT. Amp.



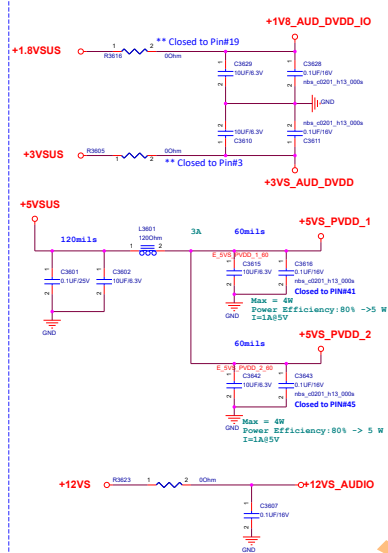
#### \*\*\* Headset Connection



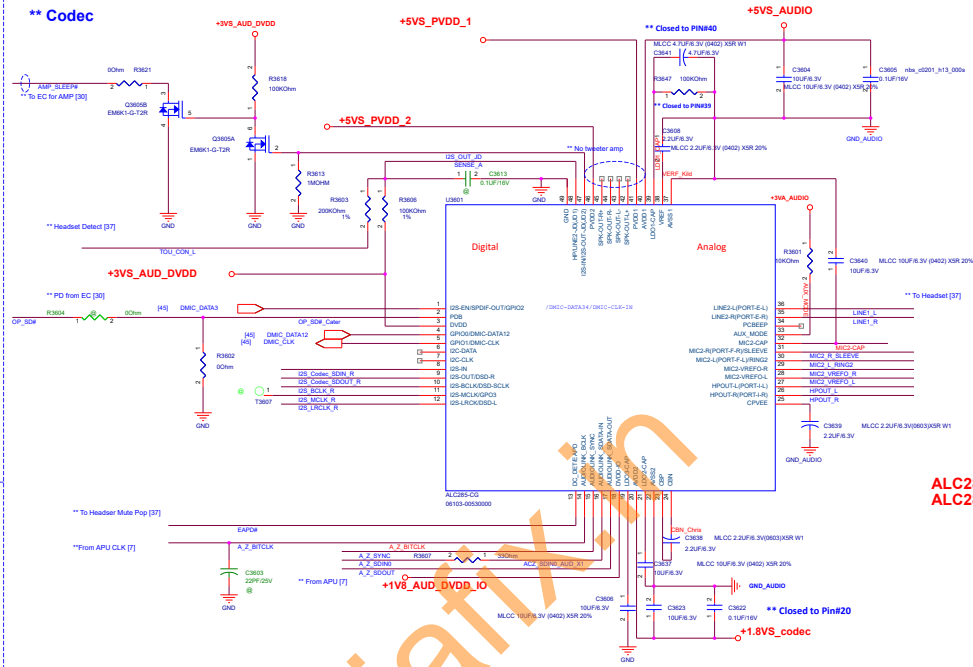
### \*\* PWR DISTRIBUTION (ANALOG)



### \*\* PWR DISTRIBUTION (DIGITAL)

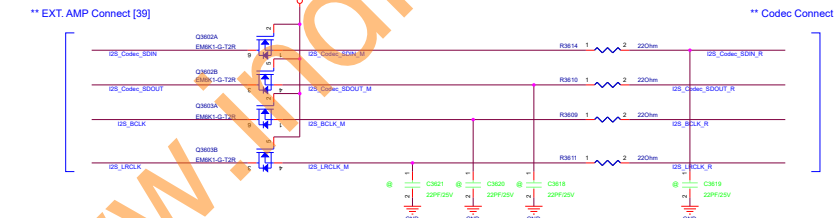


### \*\* Codec



ALC285: 06103-00530000<==  
ALC289: 06103-00510000

### \*\* EXT. AMP Connection

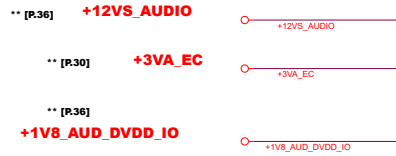


\*\*No Tweeter AMP CONN.

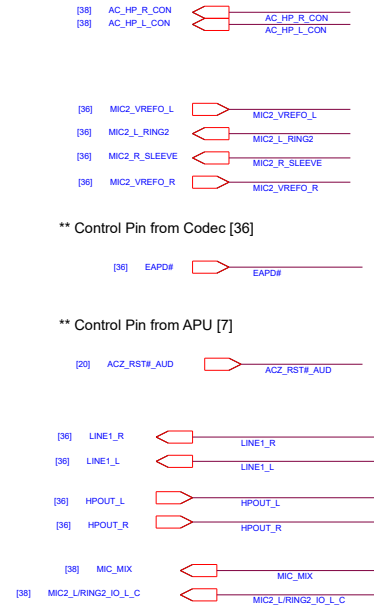
<Core Design>

Project Name		Rev
ASUS GX501IP2		1.0
Title : AUD-ALC285		
Rev	Dept.:	Engineer:
A2	ASUSTEK COMPUTER INC.	NB1 RD2.EE1
Date: Monday, October 25, 2021		Drawn: 30 of 100

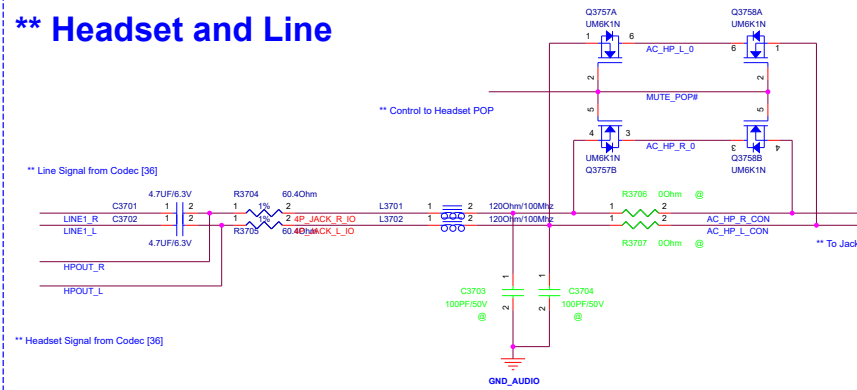
### \*\*\* POWER



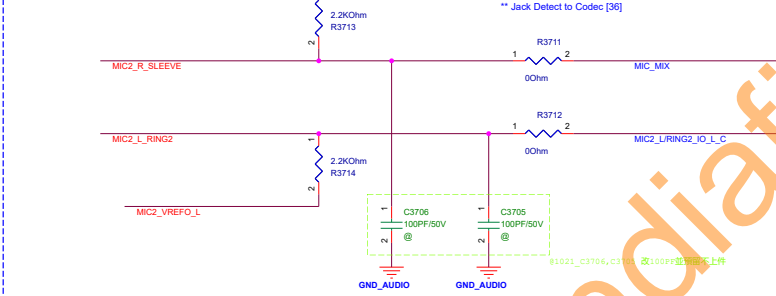
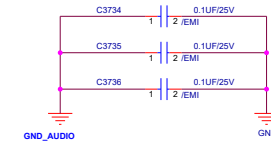
### \*\*\* SINGAL



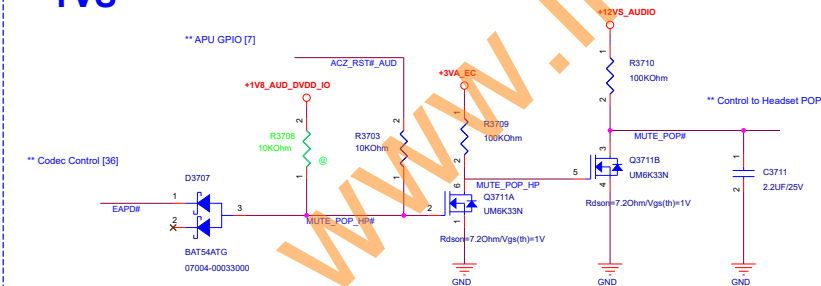
### \*\* Headset and Line



### \*\* A\_GND / GND

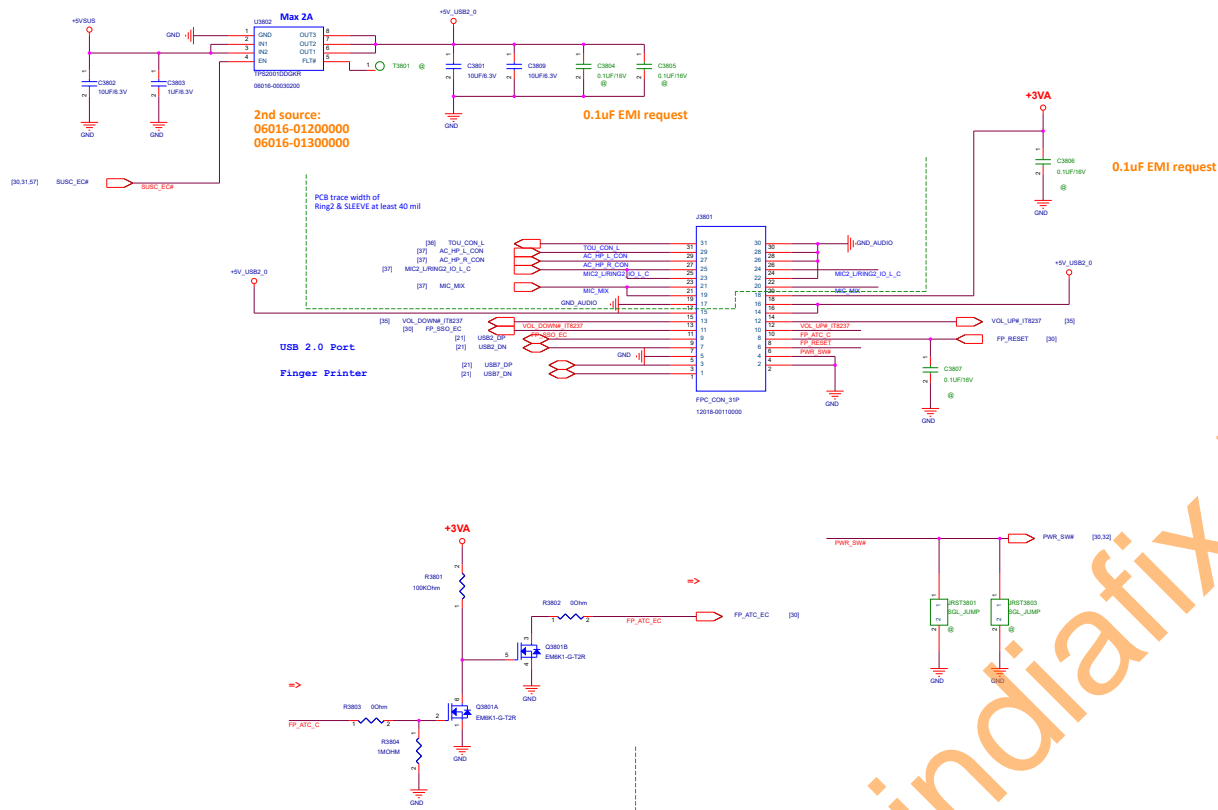


### \*\* TVS



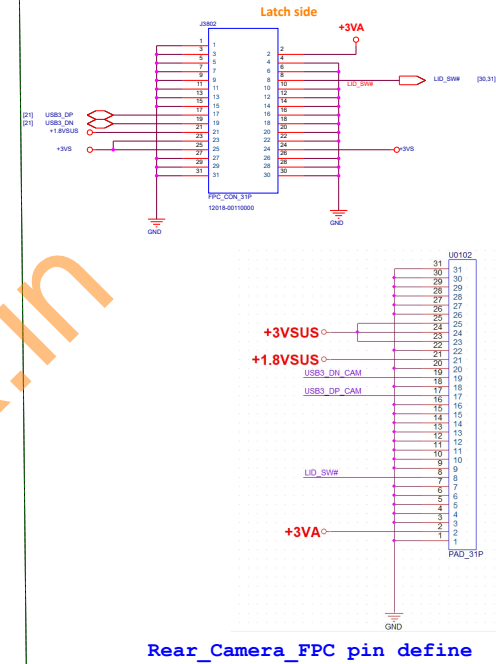
ASUS		Project Name	Rev
GX5011P2			1.0
Title : AUD_EXT Jack			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
A3			
Date: Monday, October 25, 2021	Sheet	37	of 104





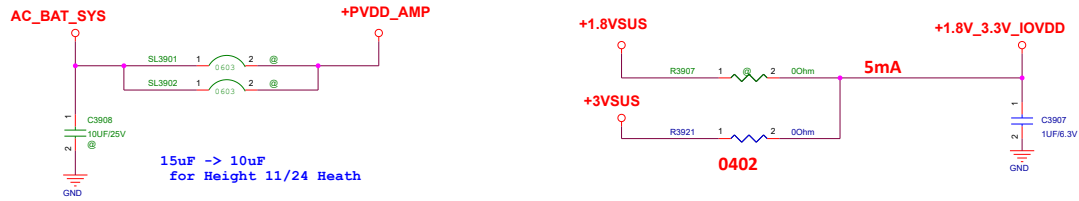
## Rear Camera Connector

REAR Camera



<b>ASUS</b>		Title : USB BOARD CONN	
ASUS/SAK COMPUTER INC. N61		Engineer: NR EE RD3	
Size	Project Name	Rev	
A2	GX5011P2	1.0	
Date: Monday, October 25, 2021		Printed	35 of 104

### \*\*\* POWER



### \*\*\* SINGAL

\*\* from EC [36]

[30] REST\_AMP#

\*\* from Codec [36]

[36] I2S\_Codec\_SDIN

[36] I2S\_LRCLK

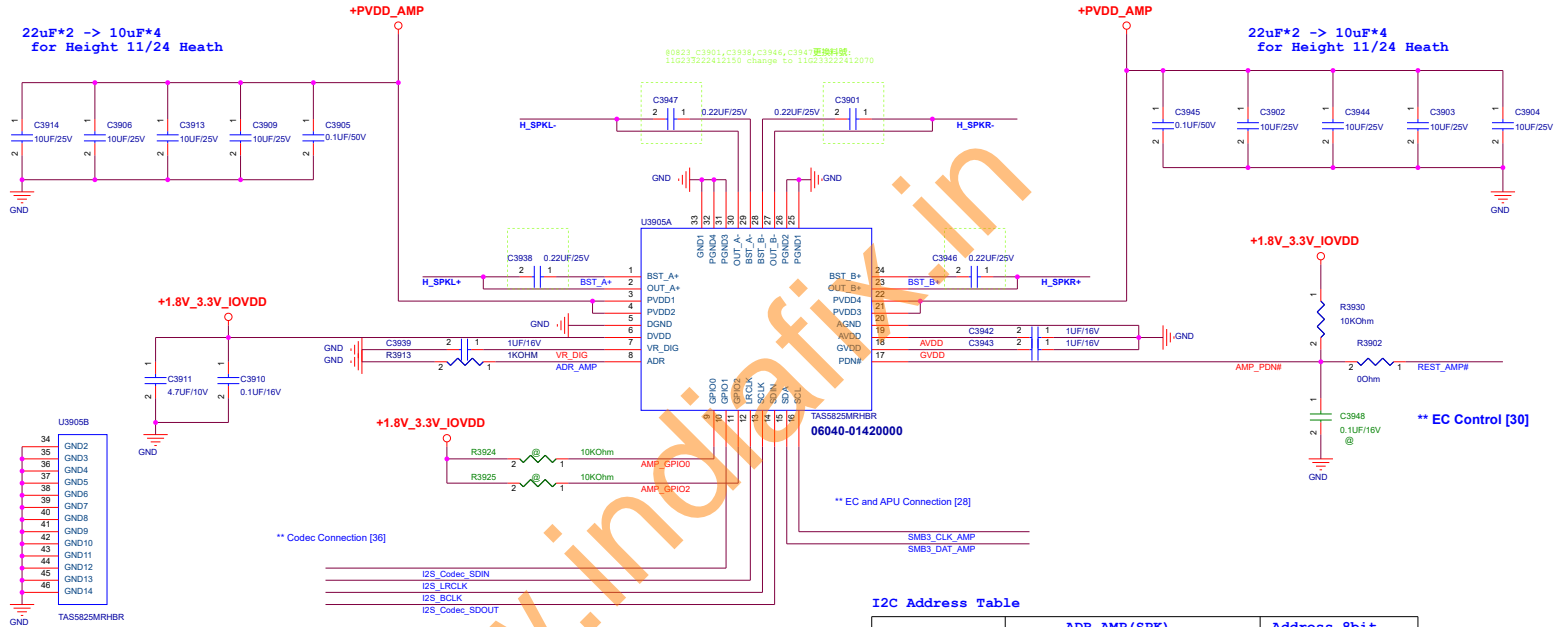
[36] I2S\_BCLK

[36] I2S\_Codec\_SDOOUT

\*\* from EC and APU [28]

[28] SMB3\_CLK\_AMP

[28] SMB3\_DAT\_AMP



I2C Address Table

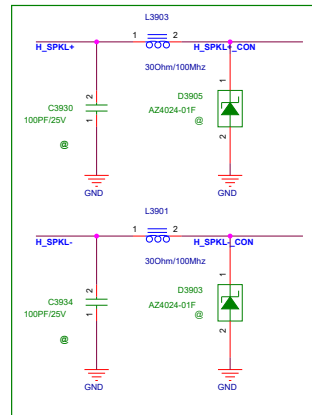
	ADR_AMP (SPK)	Address 8bit
Main (N.C.)	Open R3913 (1k ohm)	0x9A
Second	Short R3913 (0 ohm)	0x98

### Internal SPK Conn.

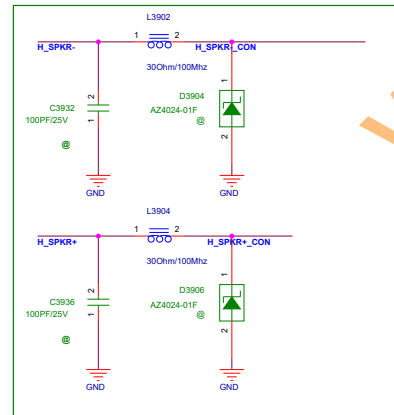
SPK L+ L- R+ R- trace width  
Speaker 8 ohm  
Max = 1.5W / Channel  
I = 0.43 A



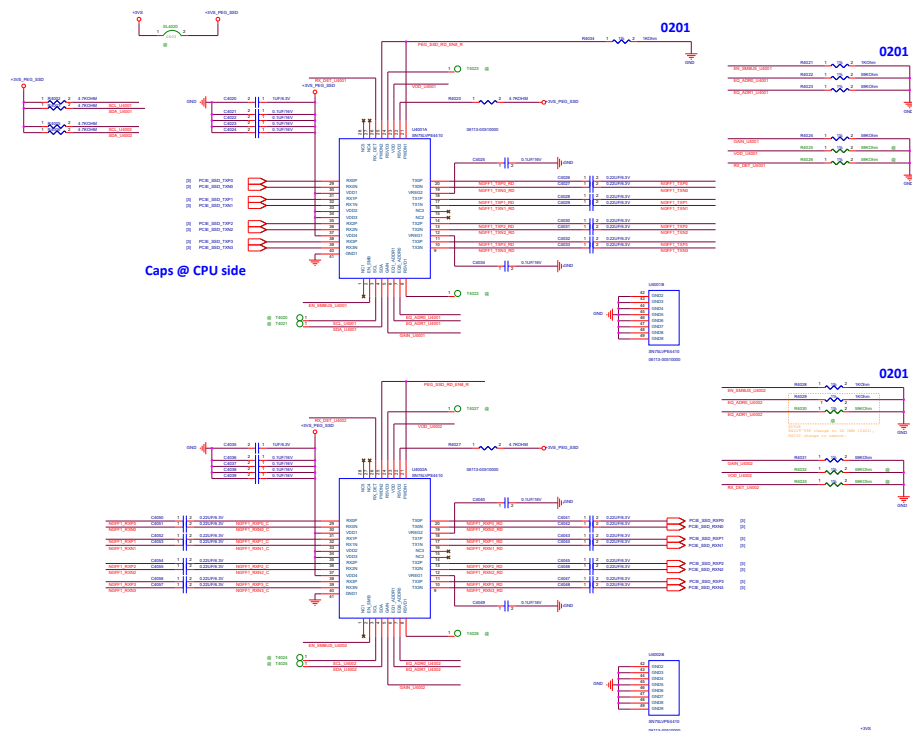
### Left



### Right



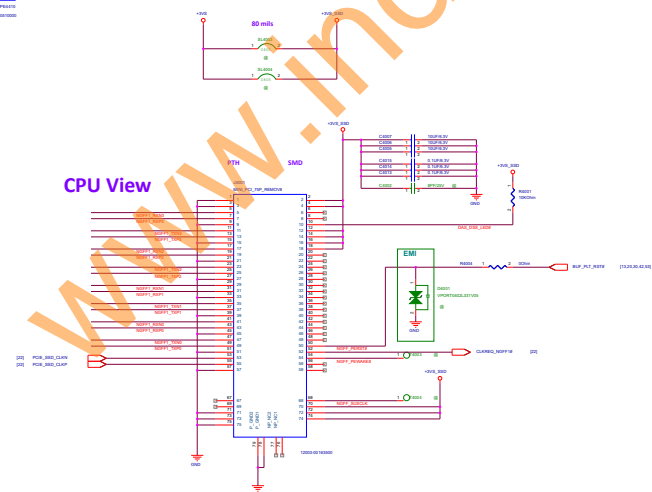
Project Name		Rev
ASUS GX501IP2		1.0
Title : AUD_INT SPK		
Size	Dept.:	ASUSTek COMPUTER INC. Engineer: EE
A3	Date: Monday, October 25, 2021	Sheet 39 of 104



Device View

Pin	Assignment	Description
1	GRND	Return current path
2	GRND	Return current path
3	PR/TX2	PCW Tx
4	PR/TX2	PCW Tx
5	GRND	Return current path
6	PR/TX2	PCW Tx
7	PR/TX2	PCW Tx
8	GRND	Return current path
9	PR/TX2	PCW Tx
10	PR/TX2	PCW Tx
11	PR/TX2	PCW Tx
12	GRND	Return current path
13	PR/TX2	PCW Tx
14	PR/TX2	PCW Tx
15	GRND	Return current path
16	PR/TX2	PCW Tx
17	PR/TX2	PCW Tx
18	GRND	Return current path
19	PR/TX2	PCW Tx
20	PR/TX2	PCW Tx
21	GRND	Return current path
22	PR/TX2	PCW Tx
23	PR/TX2	PCW Tx
24	GRND	Return current path
25	PR/TX2	PCW Tx
26	PR/TX2	PCW Tx
27	GRND	Return current path
28	PR/TX2	PCW Tx
29	PR/TX2	PCW Tx
30	GRND	Return current path
31	PR/TX2	PCW Tx
32	PR/TX2	PCW Tx
33	GRND	Return current path
34	PR/TX2	PCW Tx
35	PR/TX2	PCW Tx
36	GRND	Return current path
37	PR/TX2	PCW Tx
38	PR/TX2	PCW Tx
39	GRND	Return current path
40	PR/TX2	PCW Tx
41	PR/TX2	PCW Tx
42	GRND	Return current path
43	PR/TX2	PCW Tx
44	PR/TX2	PCW Tx
45	GRND	Return current path
46	PR/TX2	PCW Tx
47	PR/TX2	PCW Tx
48	GRND	Return current path
49	PR/TX2	PCW Tx
50	PR/TX2	PCW Tx
51	GRND	Return current path
52	PR/TX2	PCW Tx
53	PR/TX2	PCW Tx
54	GRND	Return current path
55	PR/TX2	PCW Tx
56	PR/TX2	PCW Tx
57	GRND	Return current path
58	PR/TX2	PCW Tx
59	PR/TX2	PCW Tx
60	GRND	Return current path
61	PR/TX2	PCW Tx
62	PR/TX2	PCW Tx
63	GRND	Return current path
64	PR/TX2	PCW Tx
65	PR/TX2	PCW Tx
66	GRND	Return current path
67	PR/TX2	PCW Tx
68	PR/TX2	PCW Tx
69	GRND	Return current path
70	PR/TX2	PCW Tx
71	PR/TX2	PCW Tx
72	GRND	Return current path
73	PR/TX2	PCW Tx
74	PR/TX2	PCW Tx
75	GRND	Return current path

CPU View



Pin	Assignment	Description
2	3.3V	3.3V source
4	3.3V	3.3V source
6	N/C	N/C
8	N/C	N/C
10	LED1	Device Active signal (Refer to Table 11)
12	3.3V	3.3V source
14	3.3V	3.3V source
16	3.3V	3.3V source
18	3.3V	3.3V source
20	N/C	N/C
22	N/C	N/C
24	N/C	N/C
26	N/C	N/C
28	N/C	N/C
30	N/C	N/C
32	N/C	N/C
34	N/C	N/C
36	N/C	N/C
38	N/C	N/C
40	N/C	N/C
42	N/C	N/C
44	N/C	N/C
46	N/C	N/C
48	N/C	N/C
50	PERST#	PCW Reset
52	GLXSRQ#	PCW Device Clock Request
54	PERST#	N/C
56	Reserved for WPS_DIO	N/C
58	Reserved for WPS_DIO	N/C
60	Reserved for WPS_DIO	N/C
62	Reserved for WPS_DIO	N/C
64	Reserved for WPS_DIO	N/C
66	Reserved for WPS_DIO	N/C
68	Reserved for WPS_DIO	N/C
70	3.3V	3.3V source
72	3.3V	3.3V source
74	3.3V	3.3V source

ES (M0010)  
L2/Fix mode (R01/1, A000/1) are decoded at power up to control the CPU Reset setting according to Table 3.1.1.  
L2/Fix mode (R01/1, A000/1) are used to set the L2/Fix mode address of the device.  
The L2/Fix mode address is read on power up and decoded according to Table 4.


Table 3.1.1. L2/Fix mode Address Settings			
Address	Value	Value	Value
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

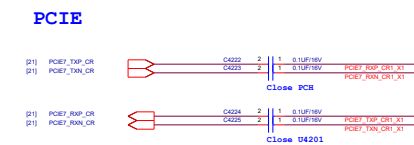
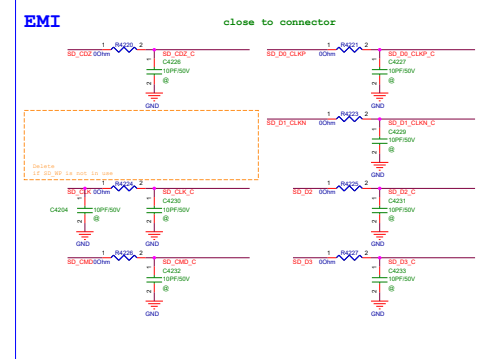
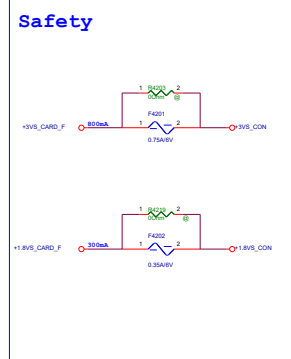
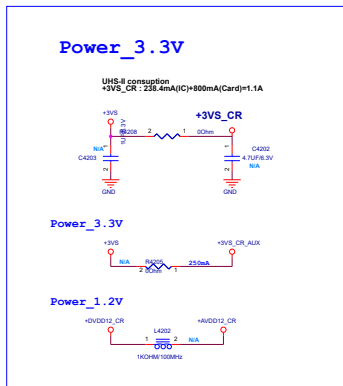
Table 4. L2/Fix mode Address Settings			
Address	Value	Value	Value
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

GA28: sets DC gain of CTR (continuous-time linear equalizer) at power up.  
L2: 0.5 dB  
L3: 0.5 dB  
L4: 0.5 dB

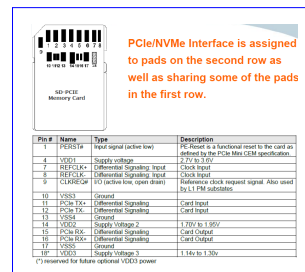
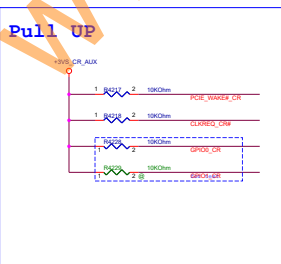
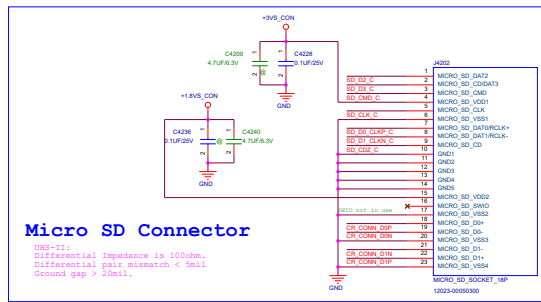
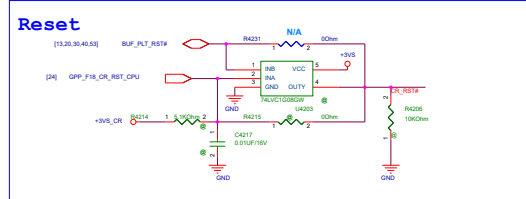
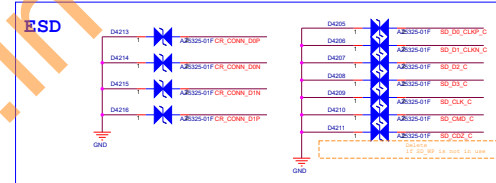
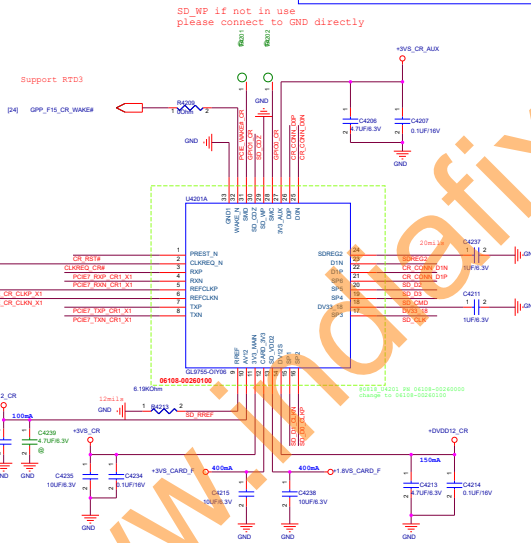
VDD: sets TR VDD setting at power up.  
L2: 0.5 dB  
L3: 0.5 dB  
L4: 0.5 dB

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<Core Design>			
		Title : M2 SSD CPU	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Drawn	Project Name		Rev
AS	GX5011P2		1.0
Date	Monday, October 25, 2021	Sheet	01 of 005



## UHS-II

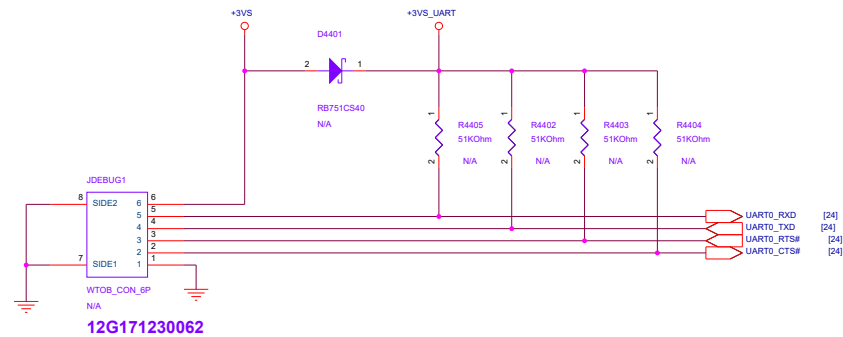


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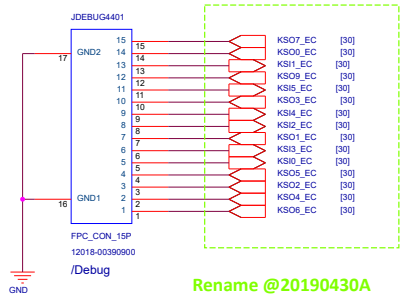
		Project Name	Rev
		GX5011P2	1.0
Title : CB_CON			
Size	Dept.: ASUS/SA COMPUTER		Engineer: NR EE RD3
A3			
Date: Monday October 25, 2021	Sheet	43	of 104

UART Debug Port

Follow GU603  
Not sure pull high needed for Tiger lake, need to be tested.

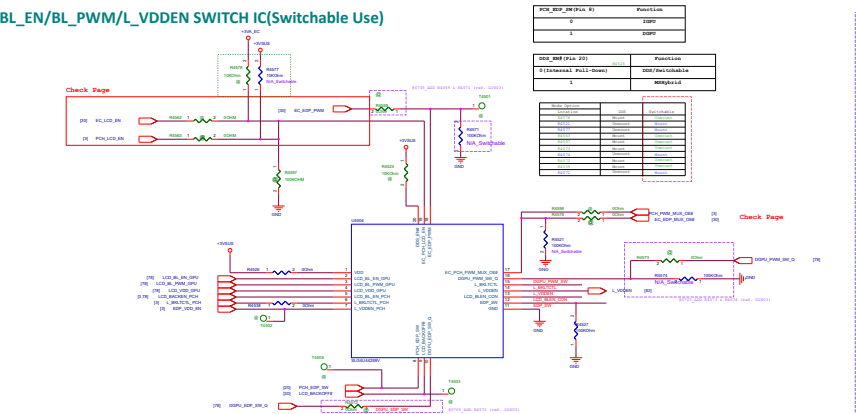


Flash BIOS

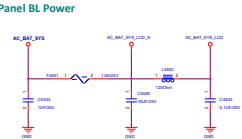


<Core Design>		Title : DEBUG_CONN	
ASUS		Engineer: NR EE RD3	
Size	Project Name	GX501IP2	Rev
A3			1.0
Date	Monday, October 25, 2021	Sheet	44 of 104

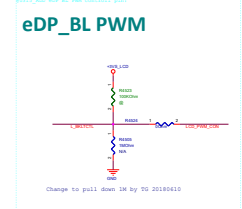
BL\_EN/BL\_PWM/L\_VDDEN SWITCH IC(Switchable Use)



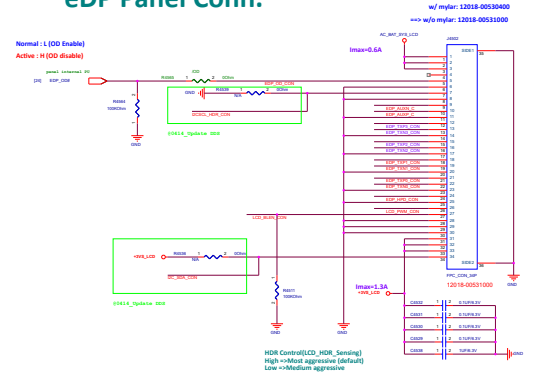
Panel BL Power



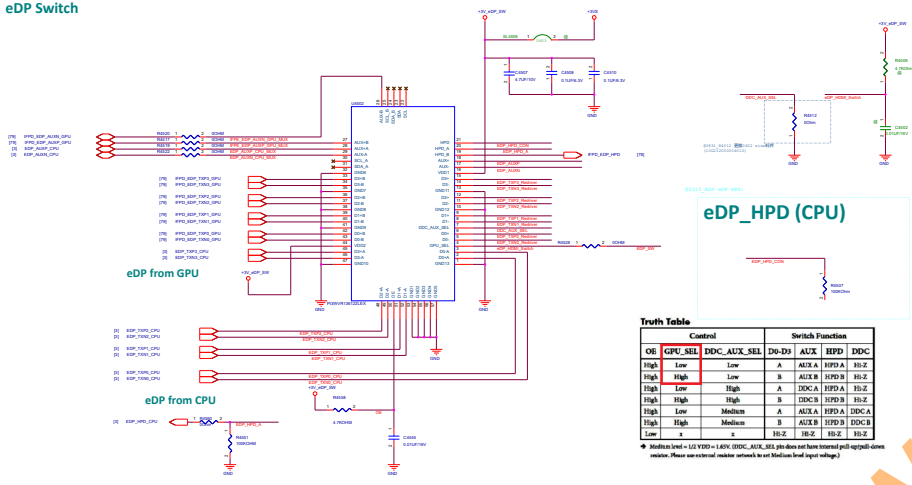
eDP\_BL PWM



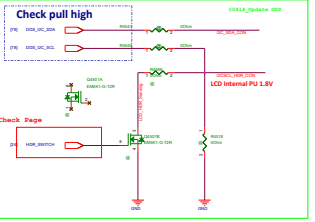
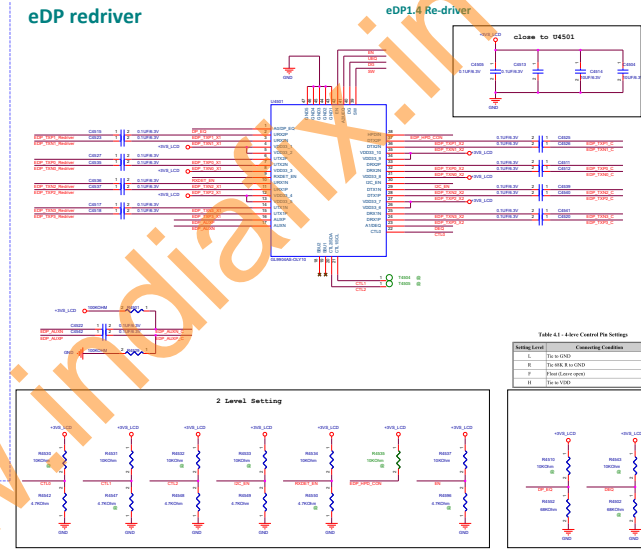
eDP Panel Conn.



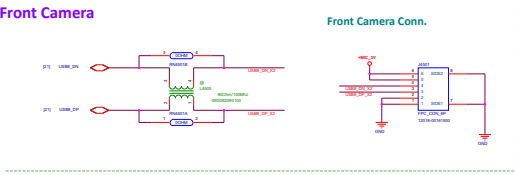
eDP Switch



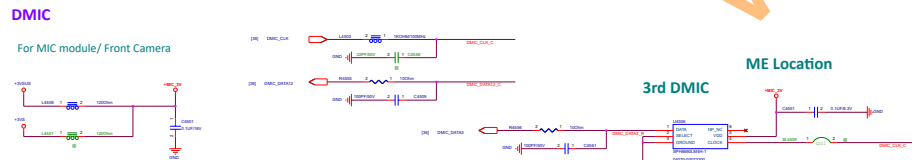
eDP redriver



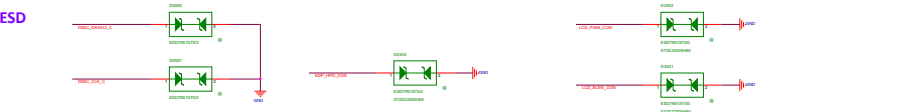
Front Camera



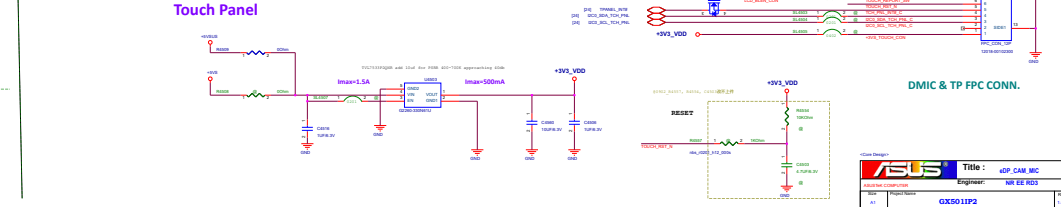
DMIC



ESD

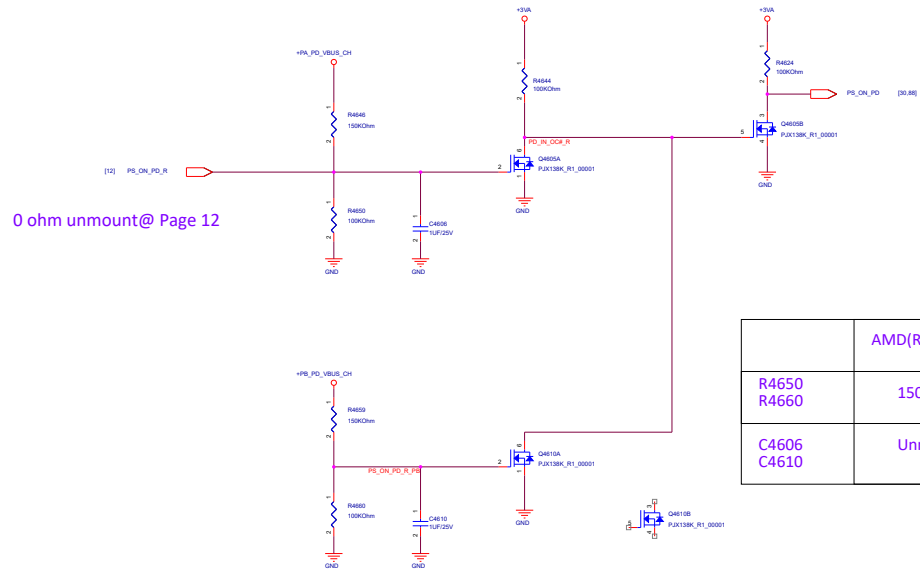


Touch Panel





## PD SINK connect



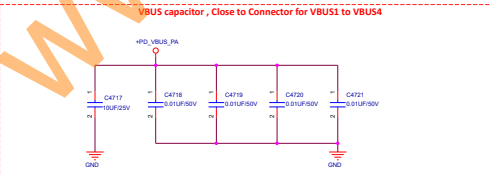
ASUS		Project Name	Rev
Title : PD_IC		G4601/PD	1.0
Rev	AS	Dept.: ASUS/SA COMPUTER INC. Engineer: NR EE RDS	
Date: Monday October 25, 2021		Sheet 48	of 104

**A**

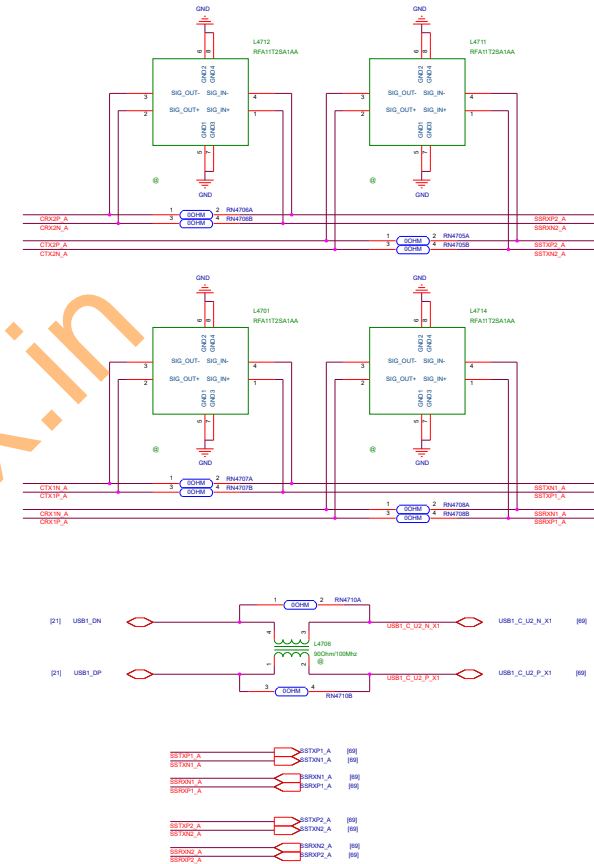
**dGPU**



A1 caps value



## USB3.0 ESD-Protection



**TYPE-C USB3.2**

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«Core Design»		Project Name		Rev.
		GX501IP2		1.0
Title : ANT				
Size	Dept.: ASUS&A COMPUTER		Engineer: NR EE RD3	
43	Date: Monday, October 25, 2021		Sheet	49 of 104

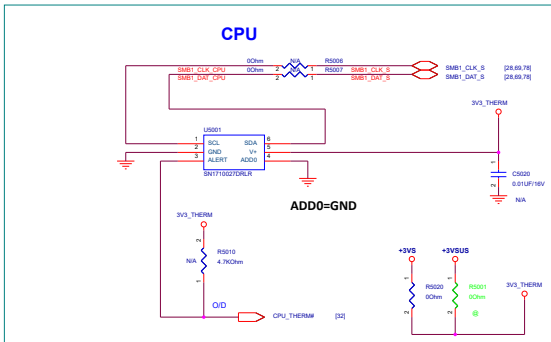
**Thermal Sensor : SN170027**

power rail : 3.3V

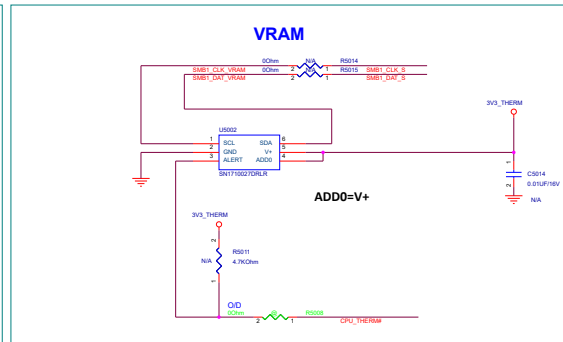
**ALERT/SDA/SCL:** Open-drain output; pullup resistor 5Kohm

## SMBUS1 to EC

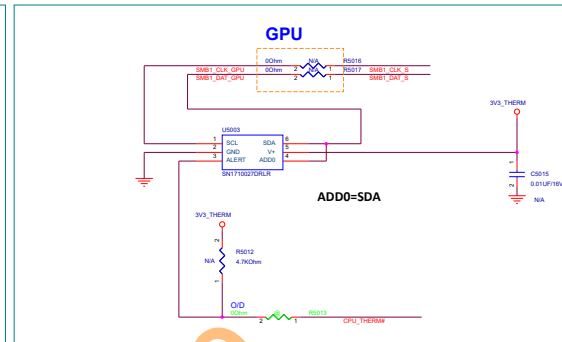
Pin function Supply voltage.: 1.62 V to 3.6 V



Near CPU  
SMBUS addr=10010000 (90)



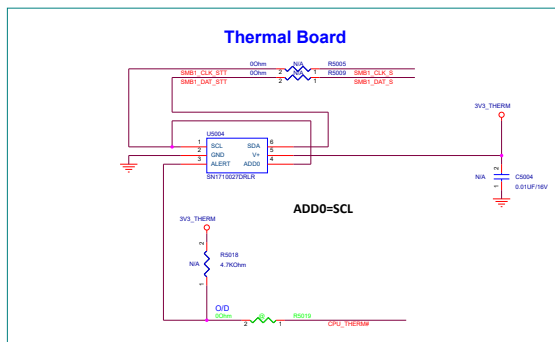
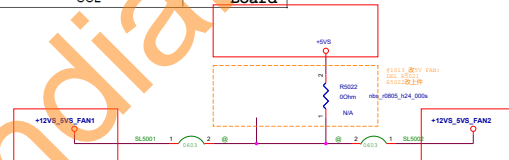
Near VRAM  
SMBUS addr=10010010(92)



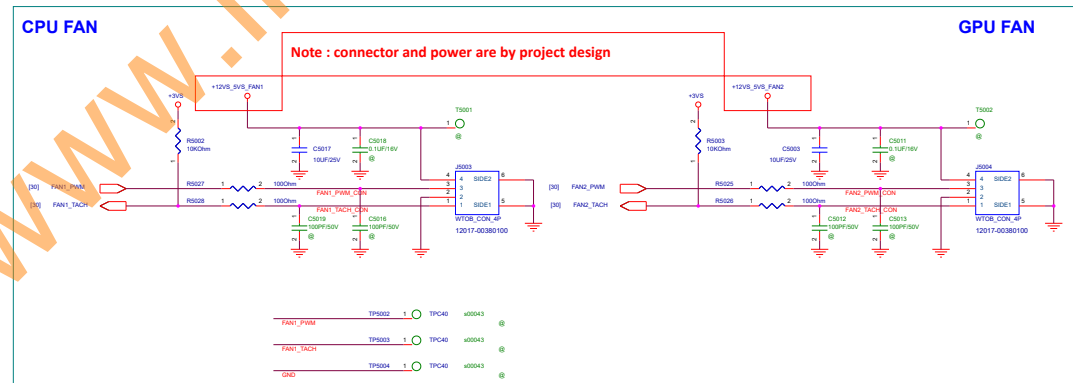
**Near GPU**  
SMBUS addr=11001010(94)

**ADD0:** Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 <b>90</b>	Ground	CPU
1001001 <b>91</b>	V+	VRAM
1001010 <b>92</b>	SDA	GPU
1001011 <b>93</b>	SCL	Board



**Near Board**  
SMBUS addr=10010110(96)



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<Close Design>

		<b>Title :</b> TYPE-C USB3.1, R1.0.4	
ASUSTeK COMPUTER		<b>Engineer:</b>	
Size	Project Name	Rev	
A3	GX501IP2	1.0	
Date: Monday, October 25, 2021		Printed	01 of 100

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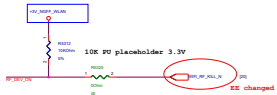
<Close Design>

		<b>Title :</b> TYPE-C USB3.1, R1.0.4	
ASUSTeK COMPUTER		<b>Engineer:</b>	
Size	Project Name	Rev.	
A3	GX501IP2	1.0	
Date: Monday, October 25, 2021		Printed	02 of 100

Control

WLAN and Vendor recommendation (prioritizable)  
1. Remove unused pins  
2. Placeholder for pinout unexpected issue

WLAN Ext\_HW\_Kill



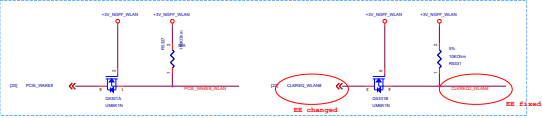
BT Ext\_HW\_Kill



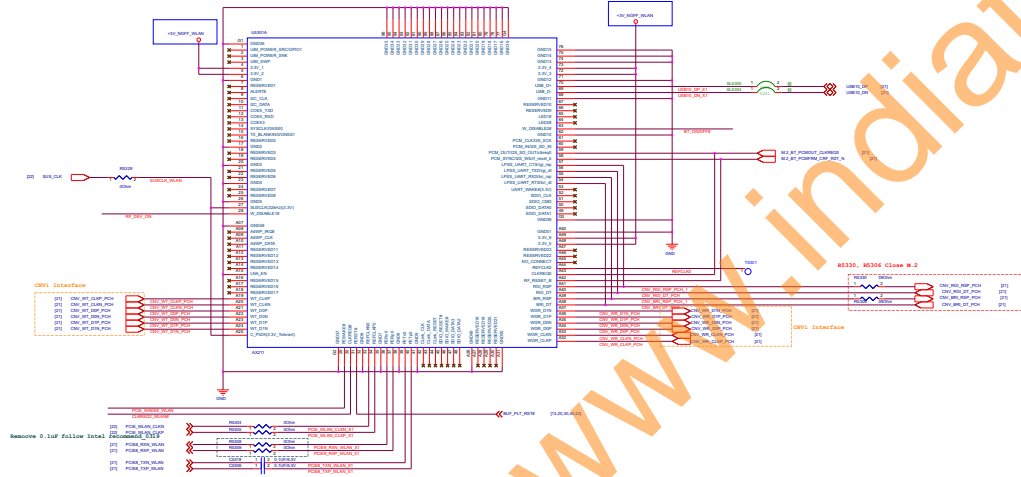
WLAN\_Wake# Control

20210219\_Admw\_add

CLKREQ\_WLAN

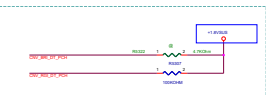


WLAN\_Intel\_GfP2\_AX211

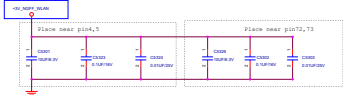


PU&PD

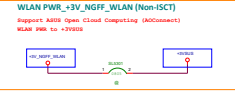
Checklist show close to DCDC  
Power for ES members, and add a PCB page



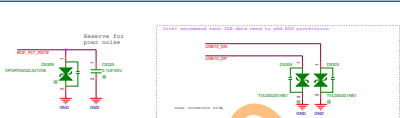
Bypass capacitor



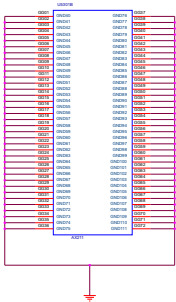
Power



For EMI



GND



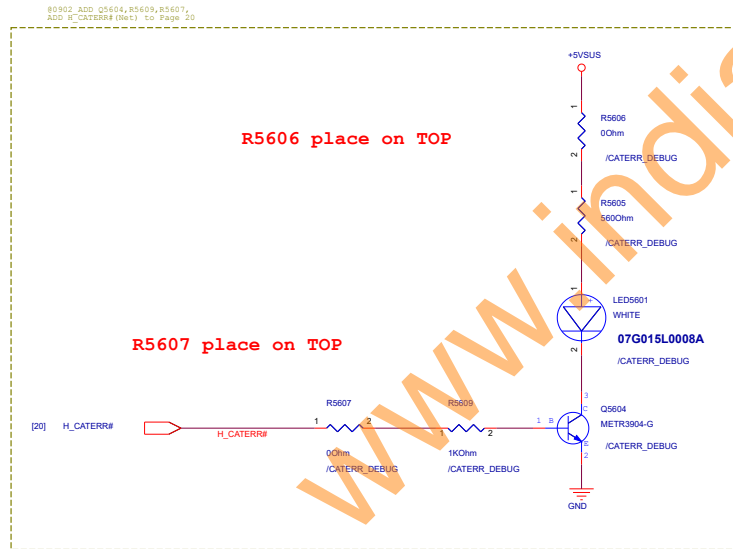
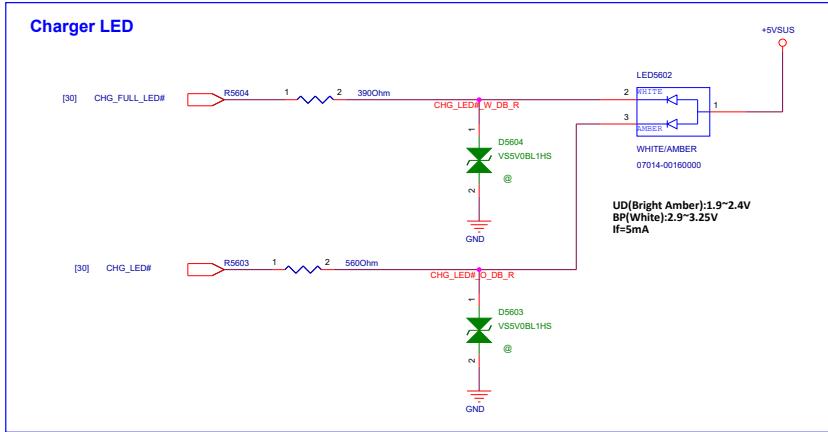
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		Project Name	Rev
		GX501IP2	1.0
Title : 5G_mmWave			
Size	Dept.: ASUS&A COMPUTER INC. Engineer: NR EE RD3		
A3			
Date	Monday October 25, 2021	Sheet	54 of 104



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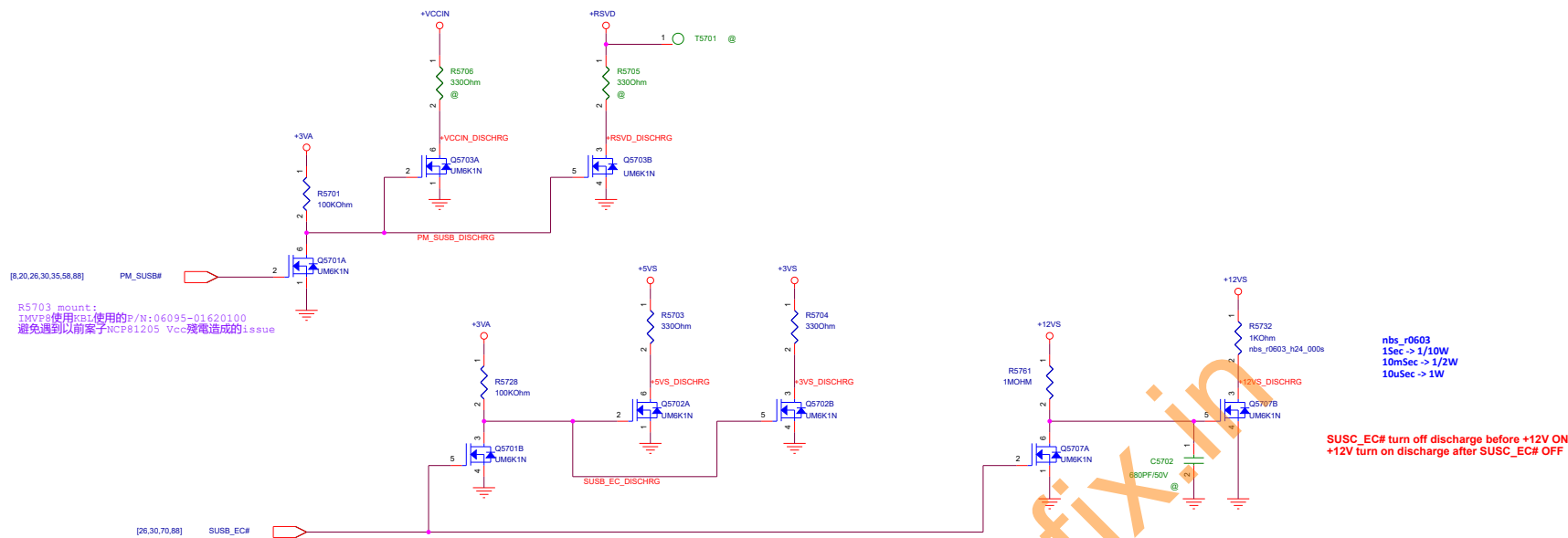
<b>ASUS</b>		Project Name	Rev
		<b>GX501IP2</b>	1.0
<b>Title :</b> 5G SUB			
Size	Dept.: ASUS&A COMPUTER INC. Engineer: NR EE RD3		
A3			
Date	Monday October 25, 2021	Sheet	55 of 104



~~HALL SENSOR  
06033-00219000 (OLD)  
06033-00210100 (NEW)~~

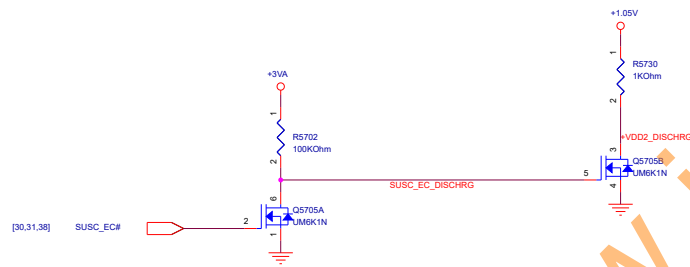
<Core Design>

<b>ASUS</b>		<b>Title :</b> LED & LID	
ASUSTek COMPUTER INC. NB3		<b>Engineer:</b> EE	
Size	Project Name	Rev	
A3	GX501IP2	1.0	
Date	Monday, October 25, 2021	Sheet	56 of 104

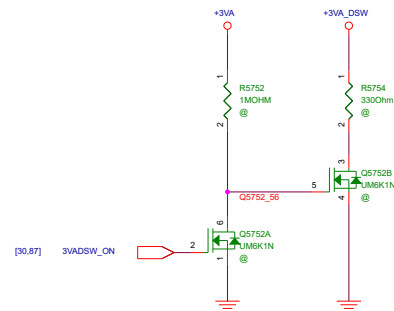
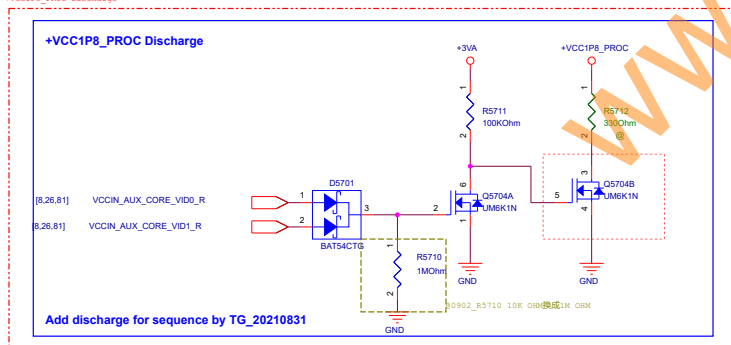


nbs\_r0603  
15sec -> 1/10W  
10mSec -> 1/2W  
10uSec -> 1W

SUSC\_EC# turn off discharge before +12V ON  
+12V turn on discharge after SUSC\_EC# OFF



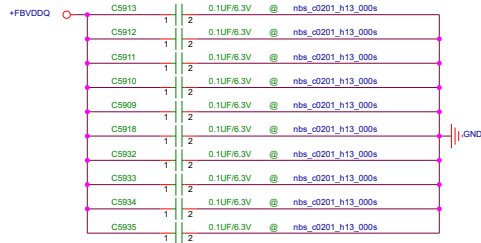
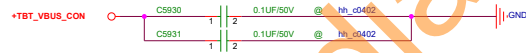
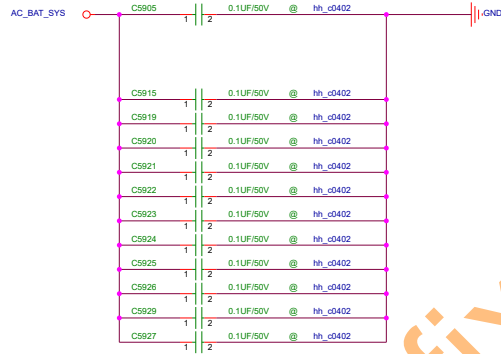
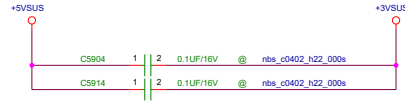
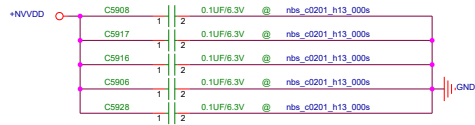
00901 Follow 00603 0811 (0811)  
ADD +VCC1P8\_PROC Discharge



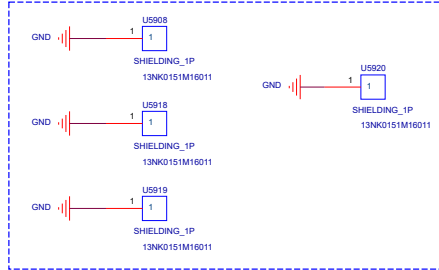
<Core Design>

<b>ASUS</b>		Title : DSG_Discharge	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Size A3	Project Name GX501IP2	Rev 1.0	
Date Monday, October 25, 2021	Sheet 57	of 104	

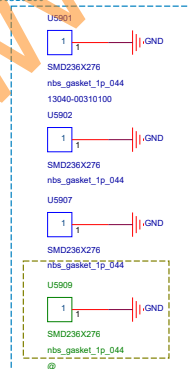




@1015 U5908, U5918, U5920:  
13NP0250M11011 change to 13NK0151M16011.  
DEL U5921.



@1014 U5901, U5902, U5907, U5909  
13NK07X0109011 change to 13040-90310100

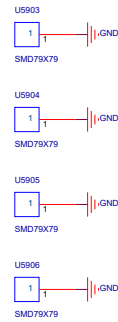


90902\_U5909 改不上件 (HIS與EHS)請認修改)

EMI GASKET

TOP

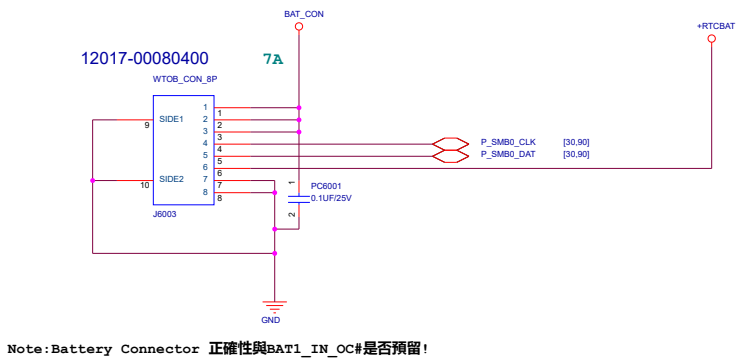
BOTTOM



<Core Design>

<b>ASUS</b>		Title : OTH_EMI	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Size A3	Project Name GX501IP2	Rev 1.0	
Date Monday, October 25, 2021	Sheet 59	of 104	

Battery Connector



Note: Battery Connector 正確性與BAT1\_IN\_OC#是否預留!

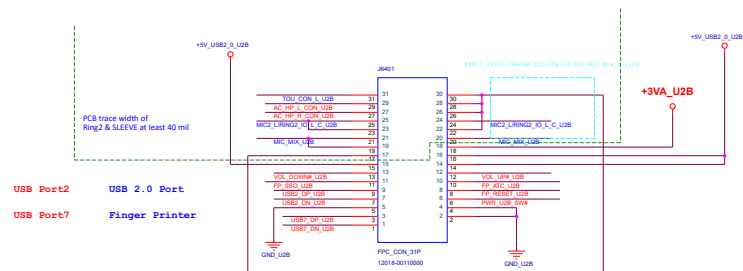
www.indiafix.in

ASUS		Project Name	Rev
GA503QS			1.0
Title : DC & BAT IN			
Size	Dept.:	Engineer:	
A3	NB_Power team	Benson	
Date:	Monday, October 25, 2021	Sheet	60 of 104



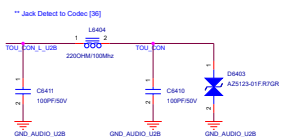
www.indiafix.in



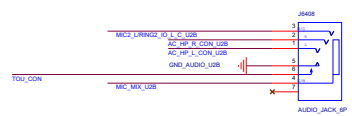


## Audio Jack

## \*\* TVS



## \*\* HP and MIC Jack



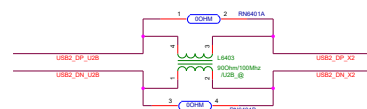
20210409 NEW PN

## \*\* A\_GND / GND



## USB2.0

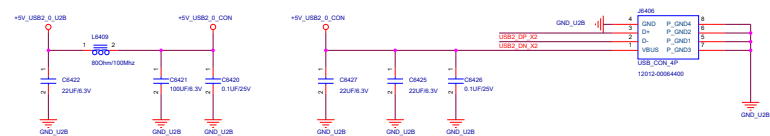
## USB2.0 EMI-Protection



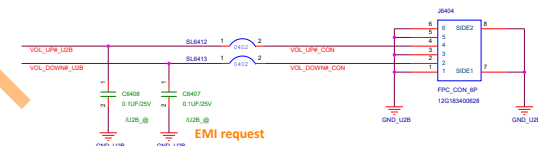
## ESD-Protection



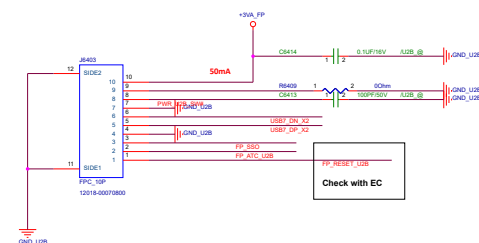
## USB2.0 Conn



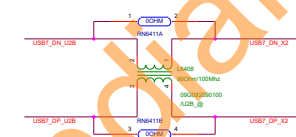
## VOL KEY FPC CONN



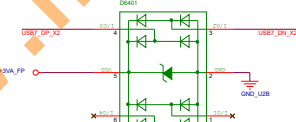
## Power Key with Finger Printer CONN



## USB2.0 EMI

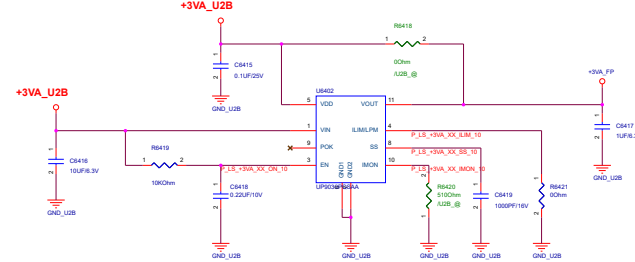


## USB2.0 ESD-Protection



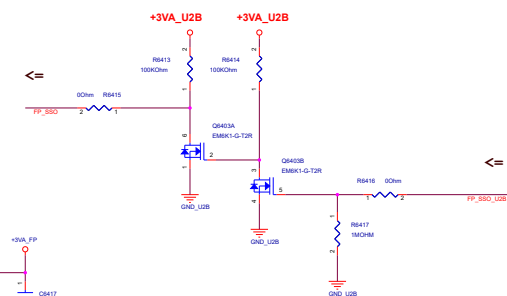
+3VA\_U2B

0402



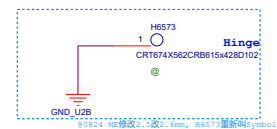
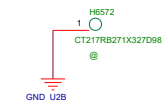
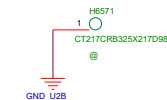
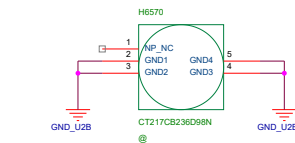
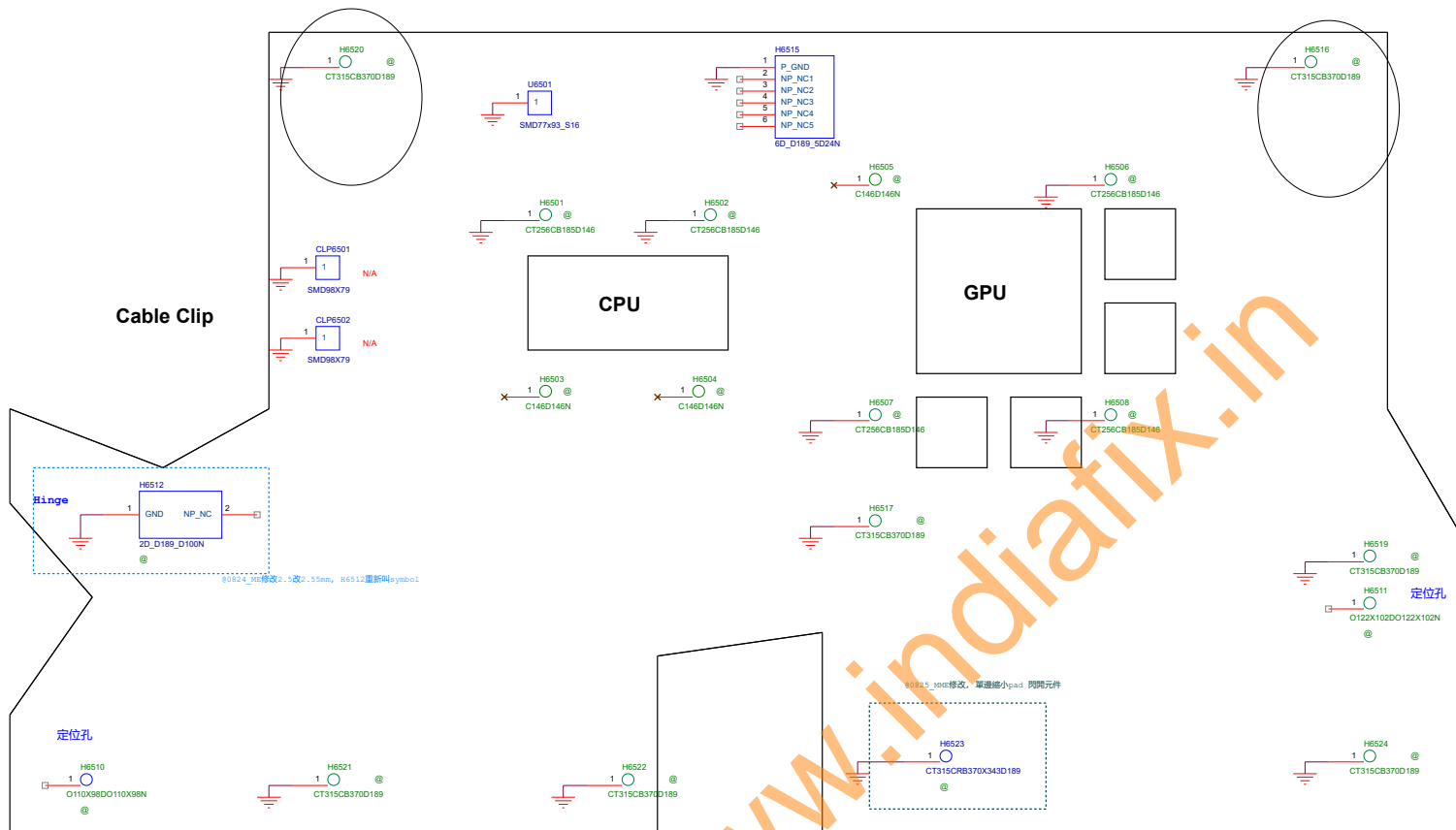
+3VA\_U2B

+3VA\_U2B

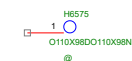


## Main Board

## USB Board



定位孔

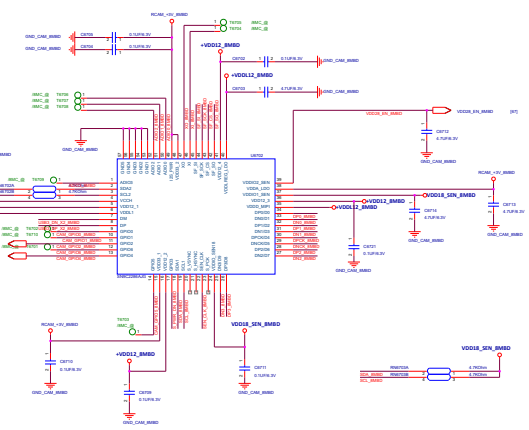
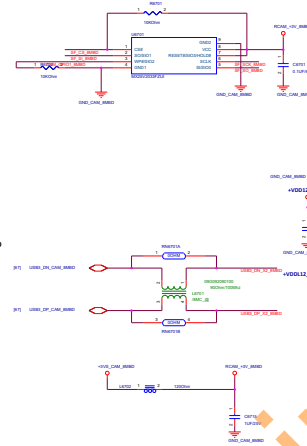
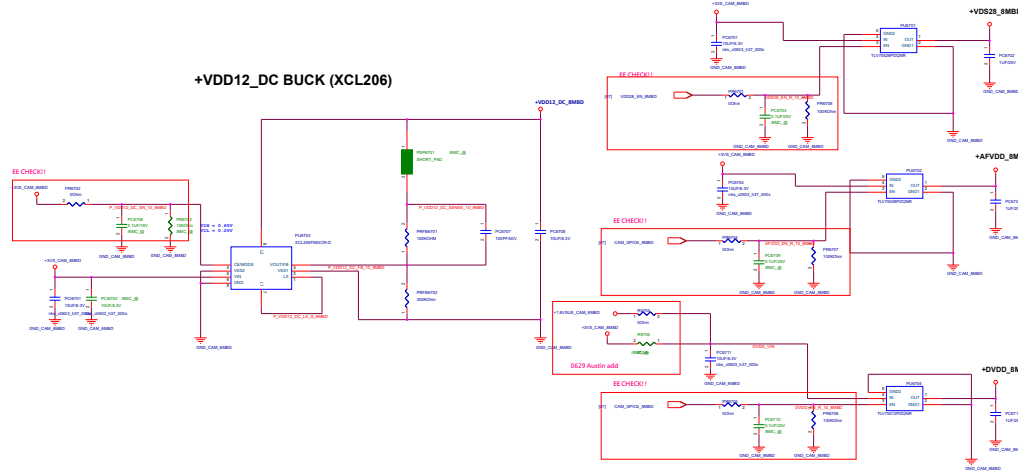


<b>ASUS</b>		Title : Screw holes	
ASUSTeK COMPUTER		Engineer: NR EE RD5	
Size	Project Name		Rev
A3	GX501IP2		1.0
Date: Monday, October 25, 2021		Sheet	65 of 104

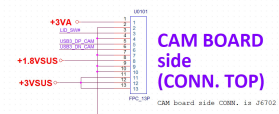
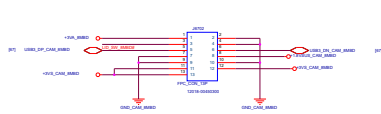
[www.indiafix.in](http://www.indiafix.in)

## 8M Rear Carmea

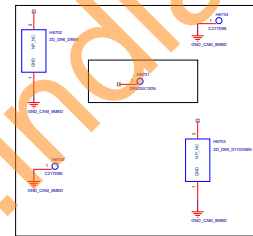
### +VDD12\_DC BUCK (XCL206)



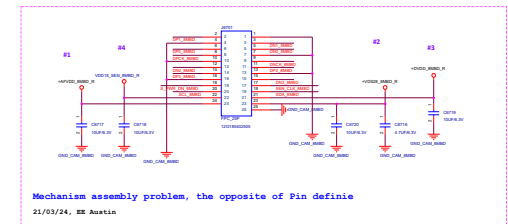
### 8M Rear Camera Board



### Hole

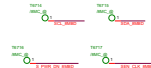


### 8M Rear Camera Conn.



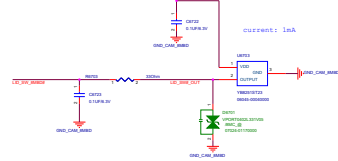
### For IEC Debug

### TOP SIDE




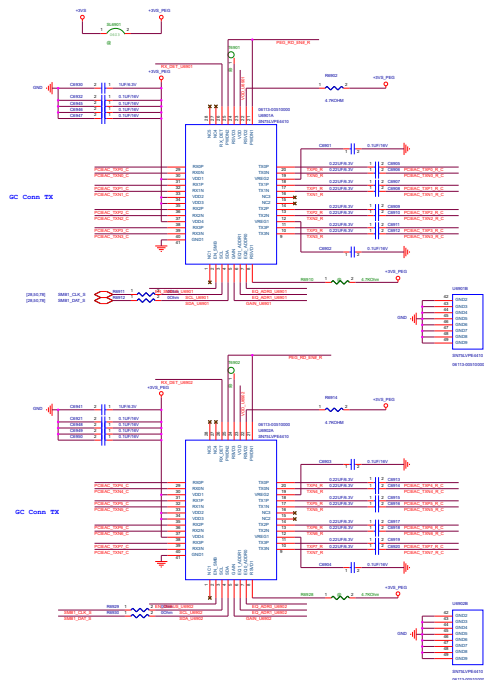
2021/10/18 add by Austin

### HALI SENSOR 06045-0040000Cmm



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«Core Design»			
		Title : OTH for test only	
ASUSTeK COMPUTER		Engineer: NR EE RD3	
Drawn	Project Name		Rev
AS	GX5011P2		1.0
Date: Monday, October 25, 2021		Print	88 12 105



SR: 000000  
SR: 000000 (SR: 000000) are decoded at power up to control the CPU boot (allowing according to Table 1).  
SR: 000000 (SR: 000000) are used to set the SR: 000000 address of the CPU boot. The SR: 000000 is read at power up and decoded according to Table 4.

Table 1: Regulation Control Settings

SR	SR: 000000	SR: 000000	SR: 000000	SR: 000000
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0
10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0

Table 2: SR: 000000 (SR: 000000) Settings

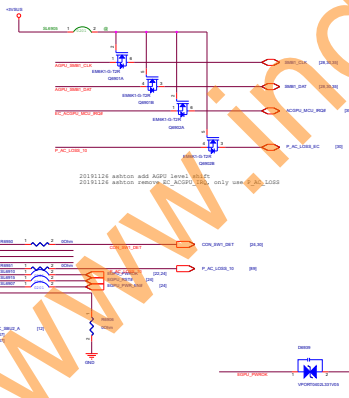
SR: 000000	SR: 000000	SR: 000000	SR: 000000
0	0	0	0
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	0	0	0
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0
14	0	0	0
15	0	0	0

SR: 000000: Data SR: 000000 (SR: 000000) linear equalizer at SR: 000000.  
SR: 000000: SR: 000000 (SR: 000000) linear equalizer at SR: 000000.

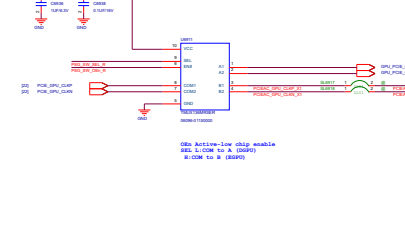
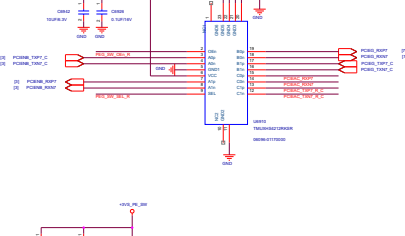
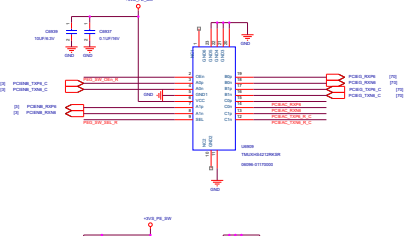
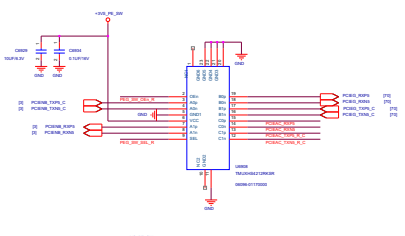
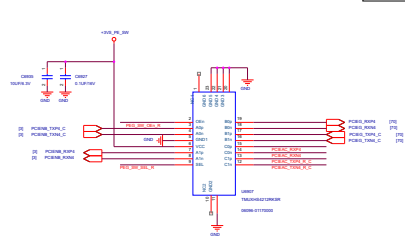
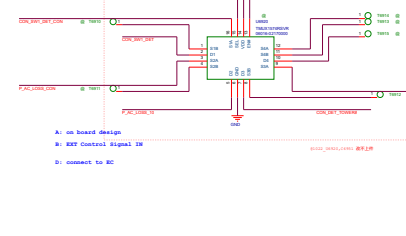
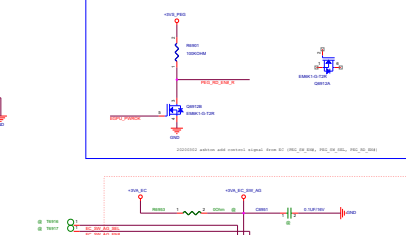
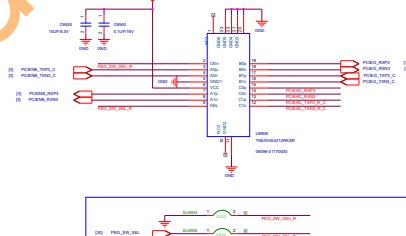
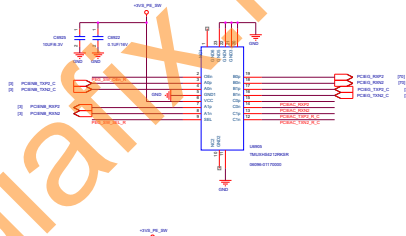
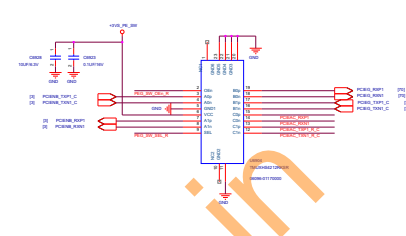
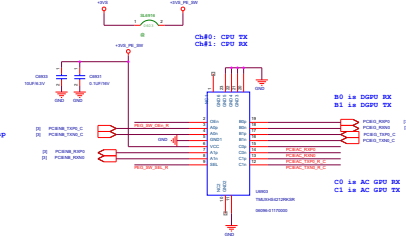
VDD: Data SR: 000000 (SR: 000000) linear equalizer at SR: 000000.  
SR: 000000: SR: 000000 (SR: 000000) linear equalizer at SR: 000000.

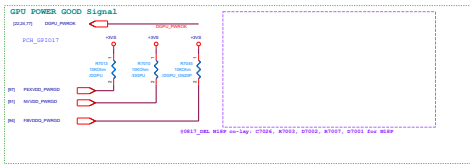
Table 3: SR: 000000 (SR: 000000) Settings

SR: 000000	SR: 000000	SR: 000000	SR: 000000
0	0	0	0
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	0	0	0
9	0	0	0
10	0	0	0
11	0	0	0
12	0	0	0
13	0	0	0
14	0	0	0
15	0	0	0



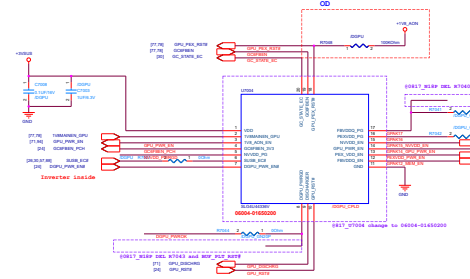
SR: 000000 (SR: 000000) are decoded at power up to control the CPU boot (allowing according to Table 1).  
SR: 000000 (SR: 000000) are used to set the SR: 000000 address of the CPU boot. The SR: 000000 is read at power up and decoded according to Table 4.





GPU POWER\_GOOD Signal

GPU POWER SEQUENCE CONTROL



U7004  
for N18 : 06004-01490100  
for GN20: 06004-01650200

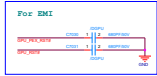
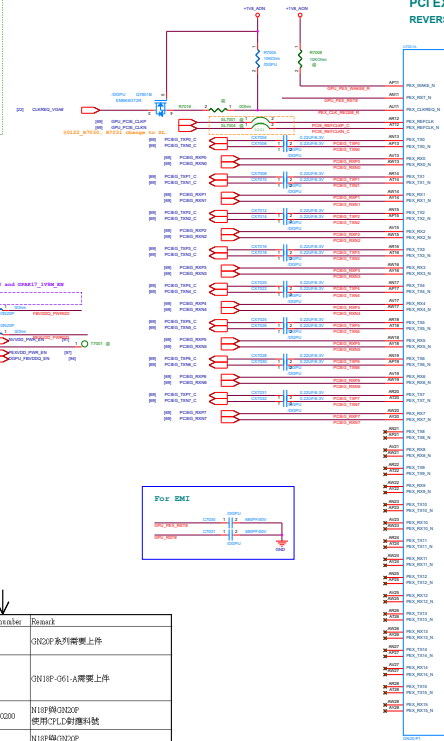
Optional	Part Reference	N18 Part number	GN20 Part number	Remark
IOGPU_GNDX2	R7045, R7041, R7042, R7044, R7103, R7106, R7006, R7009, R7914			GN20 系列需要上件
IOGPU_N18P	R7000, R7001, R7003, R7007, C7005, R7046, R7049, U7102, C7113, C7101, C7109, R7101, R7149, R7124, R7802, R7913, R7864, R7915			GN18P-G61-A需要上件
IOGPU_CPLD	U7004	06004-01490100	06004-01650200	N18 系列 CN20P 使用 CPLD 封装器件
IOGPU_ROM	U7002	05006-00041000	05006-00072000	N18 系列 CN20P 使用 ROM 封装器件
IOGPU_VREF	R7205	105212406914010	105212249114030	N18 系列 CN20P VREF 封装器件不同
IOGPU_WGA				GV301 用 OMA 301, for APU only use
VRAM				FOR GPU VRAM 的 BOM

Sample build #1  
02004-00451100  
C.S. 0202-01-A1 PC30A1358  
NVIDIA GB58-128 GA107-775-A1



料號	品名	規格
02004-00451100 (目前沒有出貨)	C.S. 0202-01-A1 PC30A1358 (10/17 update) 此為目前唯一使用料號	NVIDIA GB58-128 GA107-775-A1
02004-00451100	C.S. 0202-01-A1 PC30A1358 (10/17 update) 此為目前唯一使用料號	NVIDIA GB58-128 GA107-775-A1
02004-00574000	C.S. 0202-01-A1 PC30A1358	NVIDIA GB58-128 GA107-775-A1

## PCI EXPRESS\_Graphics REVERSED Type PCIe X16



## Main Board

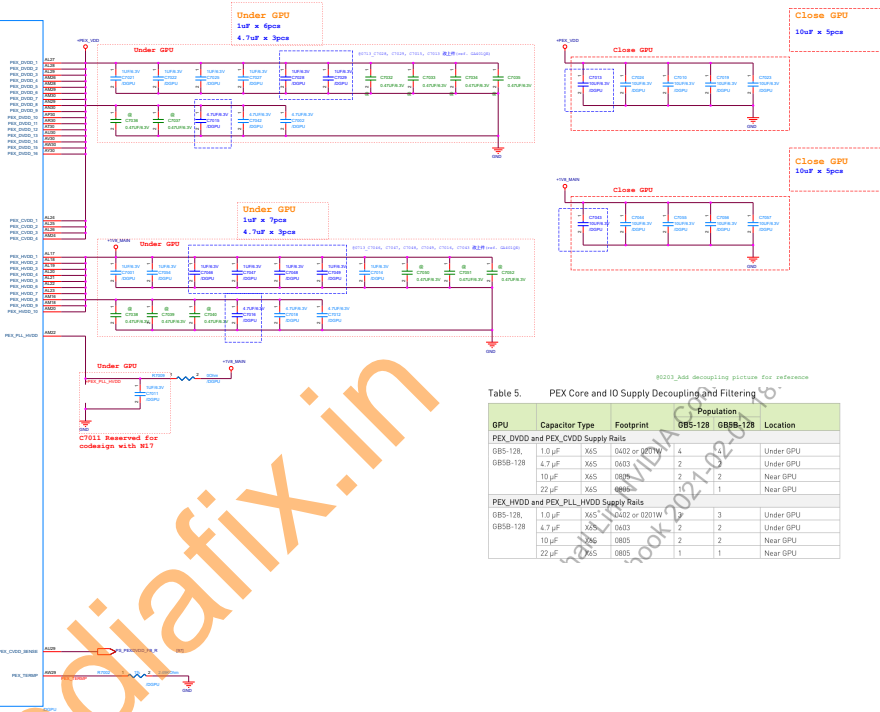
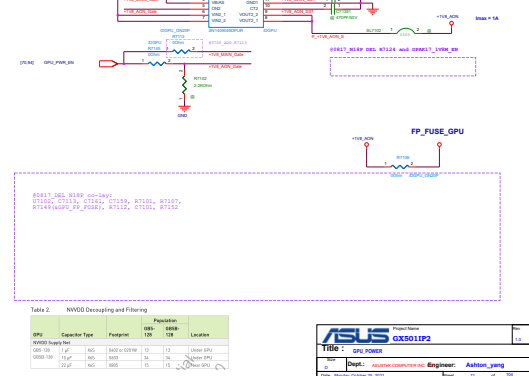
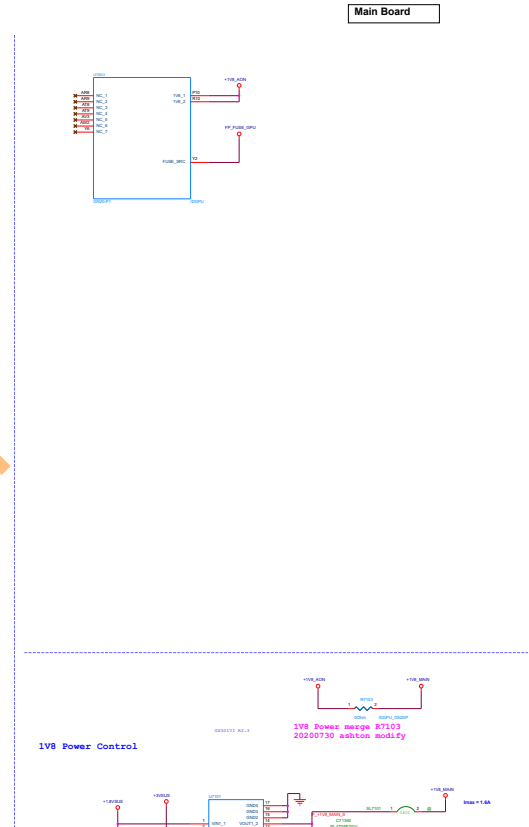


Table 5. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
PEX_DVDD and PEX_CVDD Supply Rails				
GB5-128	1.0 $\mu$ F	X65	0402 or 0603W	Under GPU
GB58-128	4.7 $\mu$ F	X65	0805	Under GPU
	10 $\mu$ F	X65	0805	Near GPU
	22 $\mu$ F	X65	0805	Near GPU
PEX_HVDD and PEX_PLL_HVDD Supply Rails				
GB5-128	1.0 $\mu$ F	X65	0402 or 0603W	Under GPU
GB58-128	4.7 $\mu$ F	X65	0805	Under GPU
	10 $\mu$ F	X65	0805	Near GPU
	22 $\mu$ F	X65	0805	Near GPU





**MEMORY: GPU FB Partition A**

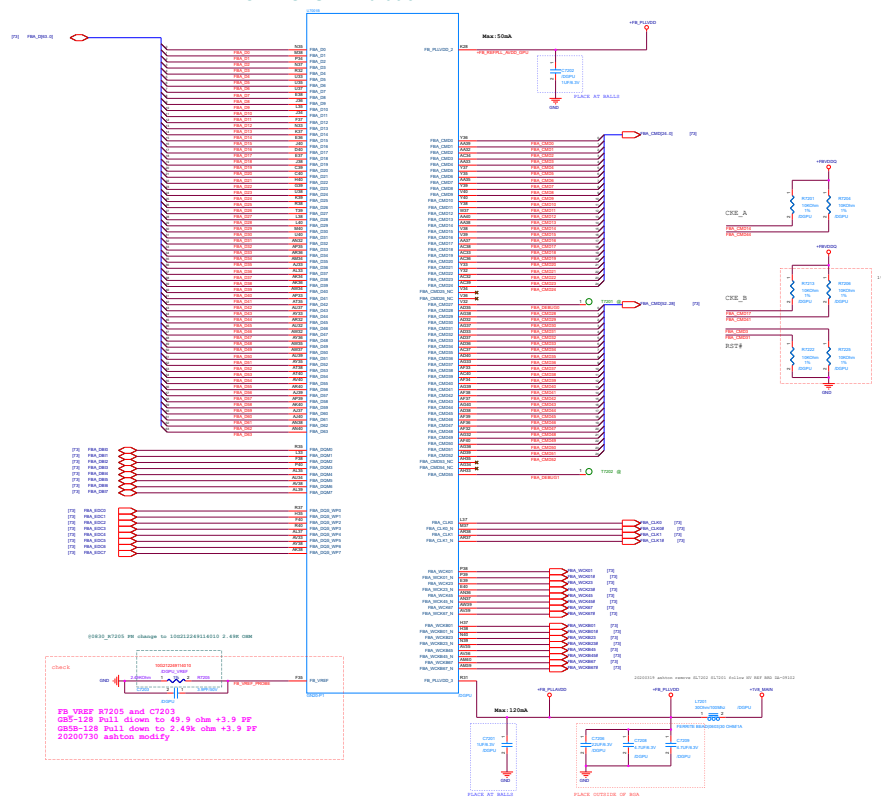
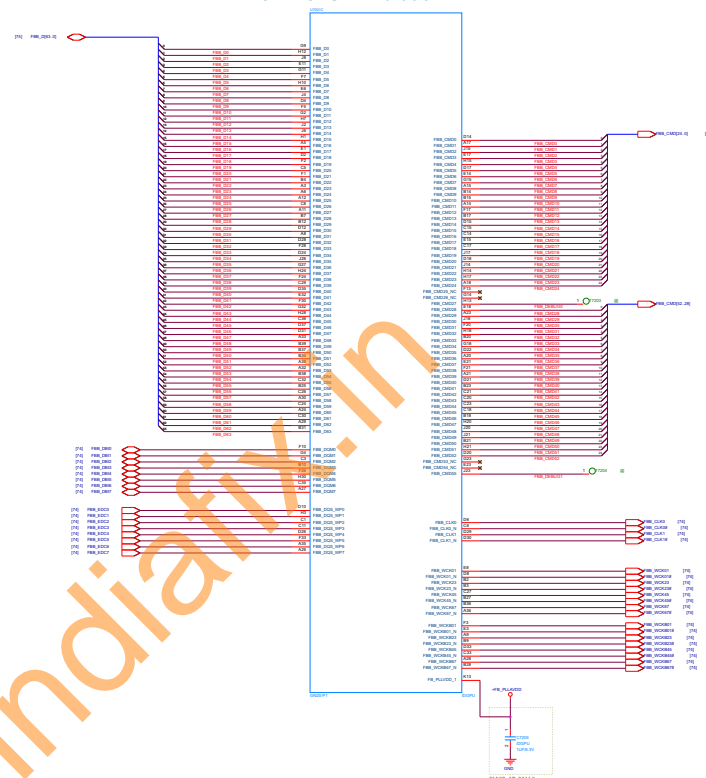


Table 4. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB5B-128		
FB PLL Supply Rail						
GB5-128	1 $\mu$ F	X6S	0402 or 0201W	3	3	Under GPU
GB5B-128	4.7 $\mu$ F	X6S	0603	2	2	Near GPU
	22 $\mu$ F	X6S	0805	1	1	Near GPU
Bead Type						
	30.0 (FSG-B-010.0)	0403	1	1	1	Near GPU

MEMORY: GPU FB Partition B



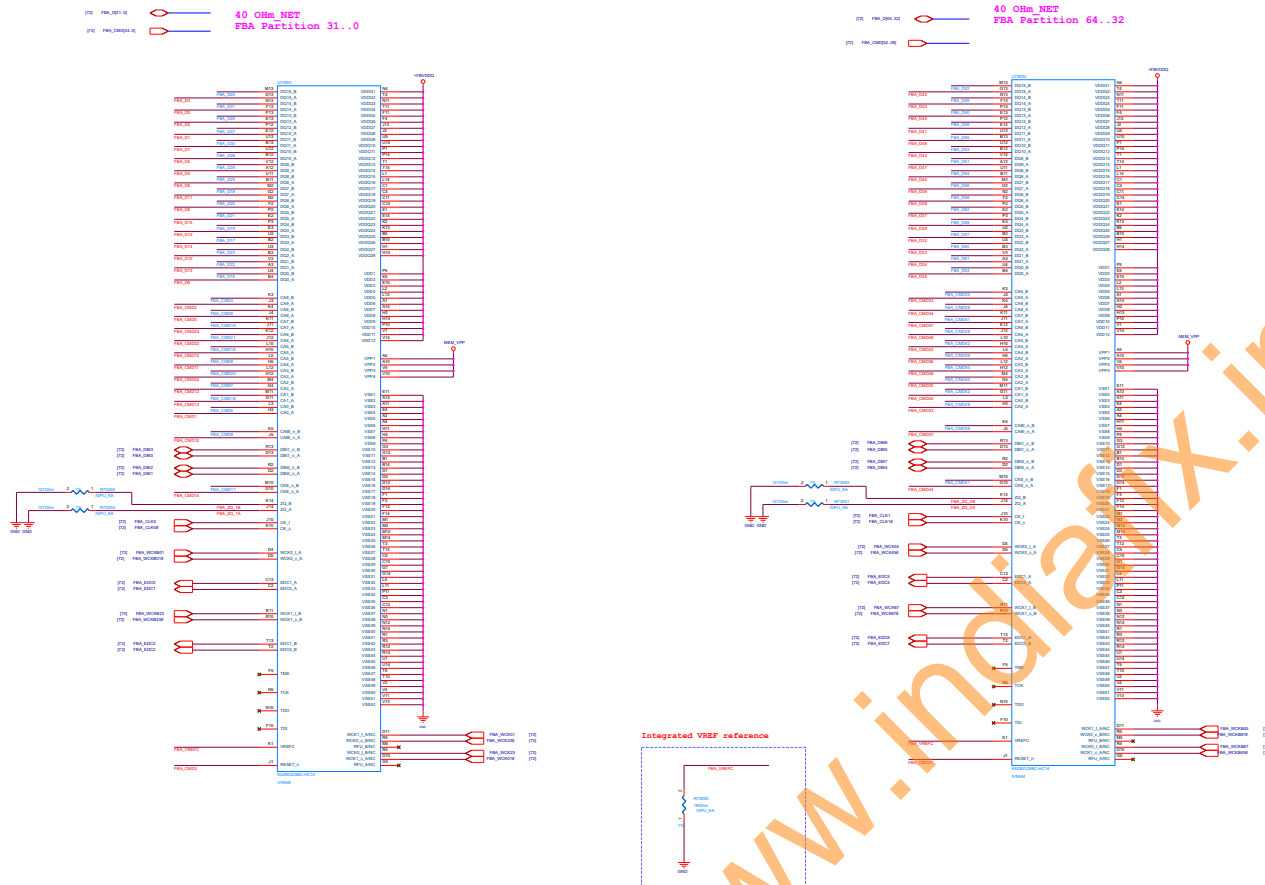
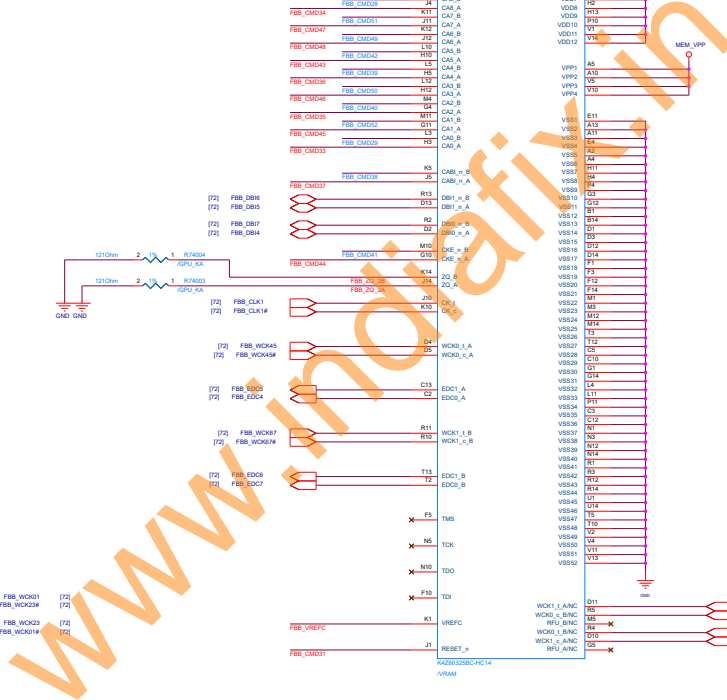
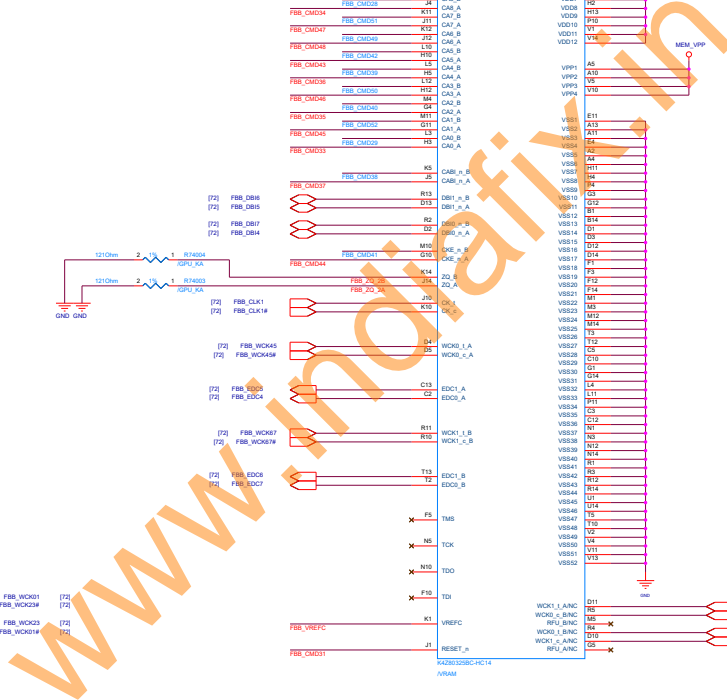
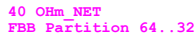
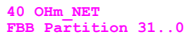


Table 4. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBV/DD/Q	Vendor	Manufacturer Part Number	Die Revision	Storage	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256tx16	1.2V	Micron	MT61K256M32JE-14J-A	A-dio	0x1	14 Gbps	Yes, TBD <sup>1</sup>	Full	Production candidate
				K4Z803258C-HC14	C-dio	0x0	14 Gbps	Yes, TBD <sup>2</sup>	Full	Production candidate

Notes:

- For H18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.



<div>&lt;Variant Name&gt;</div>			
<div>Title</div> <div>&lt;Title&gt;</div>			
<div>Doc C</div>	<div>Document Number</div> <div>GX501P2</div>		
<div>Date</div>	<div>Monday, October 25, 2021</div>	<div>Sheet</div>	<div>74 of 104</div>

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<Print Name>			
File			
<Title>			
Doc	Document Number		Rev
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FBVDDQ/VPP (VRAM)  
Channel A

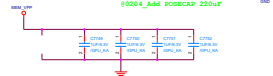
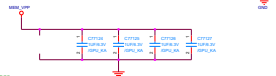
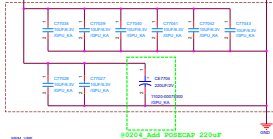
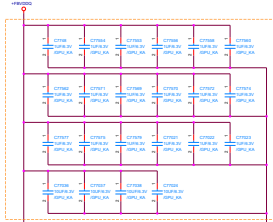
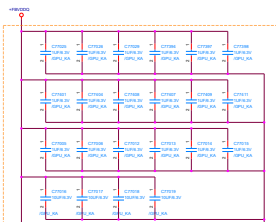


Table 3. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB9-128		
FBVDD/G Supply Rail						
GB5-128	1 $\mu$ F	X6S	0202W	12	12	Under GPU
	10 $\mu$ F	X6S	0603	5	4	Under GPU
	10 $\mu$ F	X6S	0603	2	2	Near GPU
	22 $\mu$ F	X6S	0603W	5	5	Near GPU

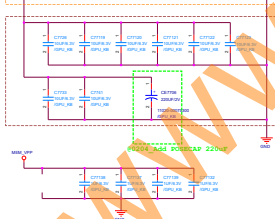
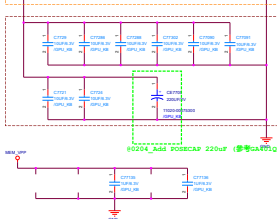
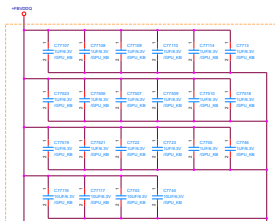
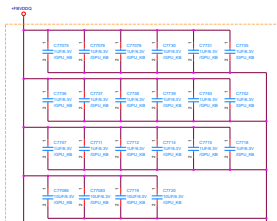
Table 3.12 DRAM Decoupling for x16<sup>1</sup>

Size	Value	Location	Quantity	Notes
0201/0402	10K, X5	Closed	18	Can use 0402 X55 or 0201 X55
0603	10K, X5	Under DRAM	4	
0603	10K, X5	Under DRAM	2	MILCC parts should be implemented first, and add POSCAP as optional
0603	22uF, X5	Under DRAM	6	
POSCAP	220uF/10V -55°C to +105°C	Under or under DRAM	1	Recommended for spare area linear or under DRAM after fulfilling all of MILCC caps. Especially for DRAMs from FMDRO Regulator output caps

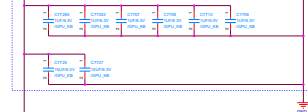
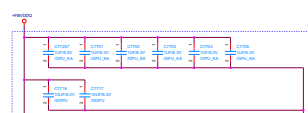
**Note:** Add 4x 10201/0402, X551 for 1.8V VPP rail (Close or Under memory).

Note: <sup>1</sup> Add 4x 1uF(0201/0402, X6S) for 1.8V YPP rail (Close or under memory)

## Channel B

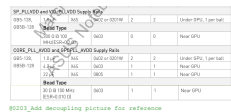
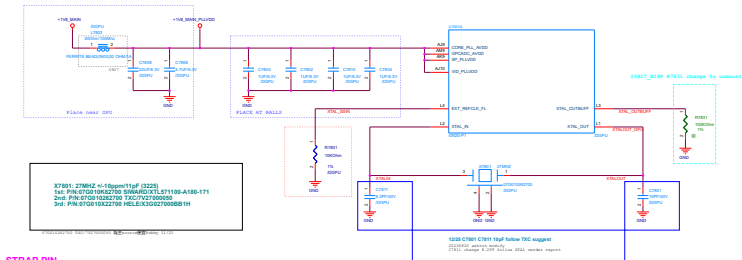


## FBVDDQ (GPU)



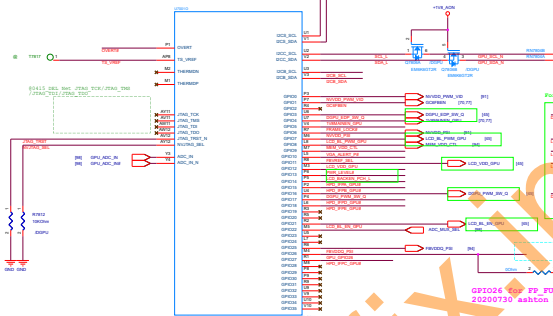
For power sequence measurement



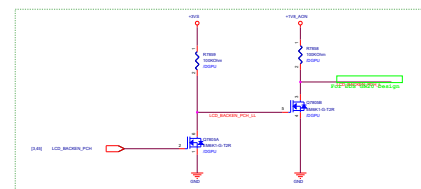
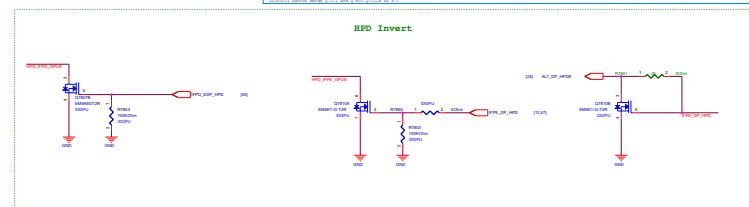
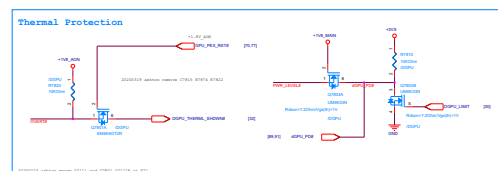


Strip Pass <sup>Row 1</sup>			Functions Selected by This Striping			
STRAPS	STRAP1	STRAP2	SWR_RLT_ADDR	DWID_SEL	POS_OGS	VGA_SERVICE
L	L	L	0	0	0	0
L	L	L	0	0	0	0
L	M	L	0	0	0	0
L	M	0	0	0	0	0
M	L	L	0	1	1	1
M	L	M	0	1	0	0
M	M	L	0	1	1	0
M	M	L	0	1	1	1
L	L	M	1	1	1	1
L	L	L	1	1	1	1
L	M	M	1	0	0	0
L	M	M	1	0	1	1
M	L	L	1	0	0	0
M	L	M	1	0	0	1
M	M	L	1	1	0	0
M	M	L	1	1	1	1

DEFAULT : L L H



Strap Pins (see Note 1)	ROM_SI (see Note 2)	ROM_SCLK	FS_0VERT* Funktion
1	0	0	FS_0VERT* Funktion DISABLED
1	0	1	FS_0VERT* Funktion CHIPSELECT 0
1	1	0	FS_0VERT* Funktion CHIPSELECT 1
1	1	1	ENABLED, do not configure

[illegible]

<b>ASUS</b>		Project Name	
		<b>GX501IP2</b>	
<b>Title :</b>		<b>GPU_CLOCK/STRAP/IGPIO</b>	
<b>Dept:</b>	<b>ASUSTK COMPUTER</b>	<b>Engineer:</b>	<b>Gaming RD</b>

Memory Density	Allowed Memory Configuration	FBDVD I/O	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual. Plan	Status	Supported CPU Milestones
8 Gb	2Chx256Mx16	12x1 and 2V	Samsung	K4B78025BC-HC14	C-die	0x0	14 Gbpps	2001F	Full	Production candidate	Q5 or later
			Hynix	H5G6KH42HJR-S2C	A-die	0x2	14 Gbpps	N/A	Full	Production candidate	Q51 or later
			Micron	M716125M32JE-16A	A-die	0x1	14 Gbpps	1940F	Full	Production candidate	Q52 or later

Notes:

<sup>1</sup> DVS is required to run WCLK - 5500 MHz.

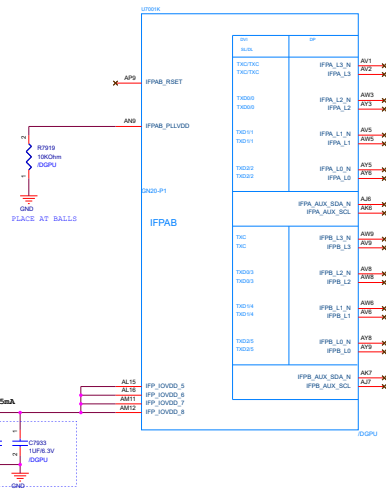
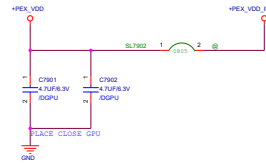
<sup>2</sup> Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "S8" letters inserted before the seven digits in its lot ID.

<sup>3</sup> Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.

For G2D2-P1/P0, the maximum allowable memory case temperature is 55°C.

4.7uF: 0603 SIZE  
1uF: 0402 SIZE

power: ABCDE



4.7uF x 1pcs  
0603 SIZE  
1uF x 2pcs  
0402 SIZE  
1uF x 1pcs  
0402 SIZE

Table 7.1 Display Link Summary (GB5-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort
IFPA (Link A)	✓Dual Link with IFPB			✓
IFPB (Link B)	✓Dual Link with IFPA			✓
IFPC (Link C)		✓		
IFPD (Link D)			✓	
IFPE (Link E)		✓		
IFPF (Link F)				✓

## 7.2 Unused pins

If an IFP Link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPx\_RESET (by = AB, CD, EF) can be left unconnected and IFPx\_PLLVDD should be 10K PD to GND if neither of IFPA/IFPB is in use. For example, if neither Link A nor Link B of the IFPA/IFPB macro is to be used, then IFPAB\_PLLVDD must be 10K PD to GND. IFPAB\_RESET should be left unconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

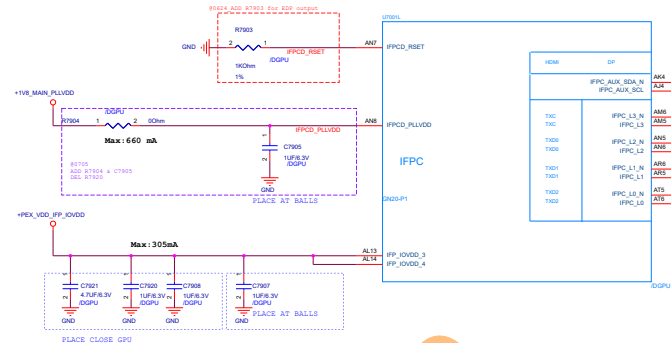
IFP\_IOVDD rail can be left unconnected if the IFP link is used. If any IFP is used, all IFP\_IOVDD balls must be connected to power rail.

Table 7.2 Display Link Power Rail Applicability

Display Link Rail	DISPLAY LINKS THAT RECEIVE POWER FROM THIS RAIL					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	✓	✓	✓	✓	✓	✓
IFPAB_PLLVDD	✓	✓				
IFPCD_PLLVDD			✓	✓		
IFPEF_PLLVDD					✓	✓

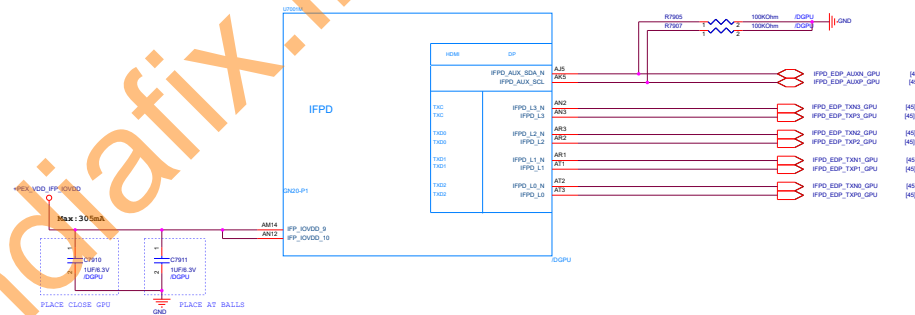
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HDMI



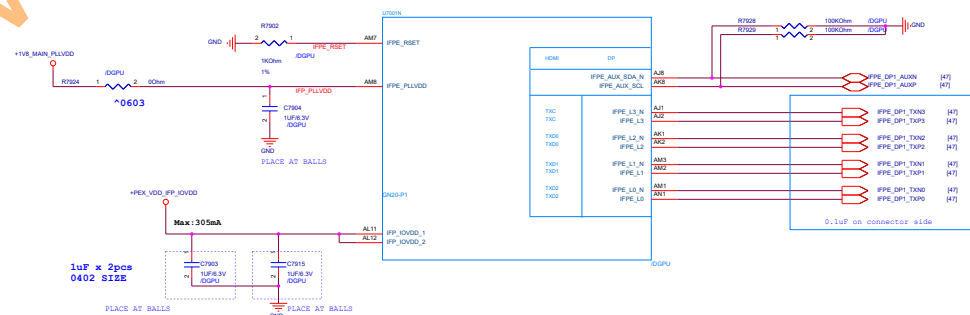
D

EDP (4Lane Panel)



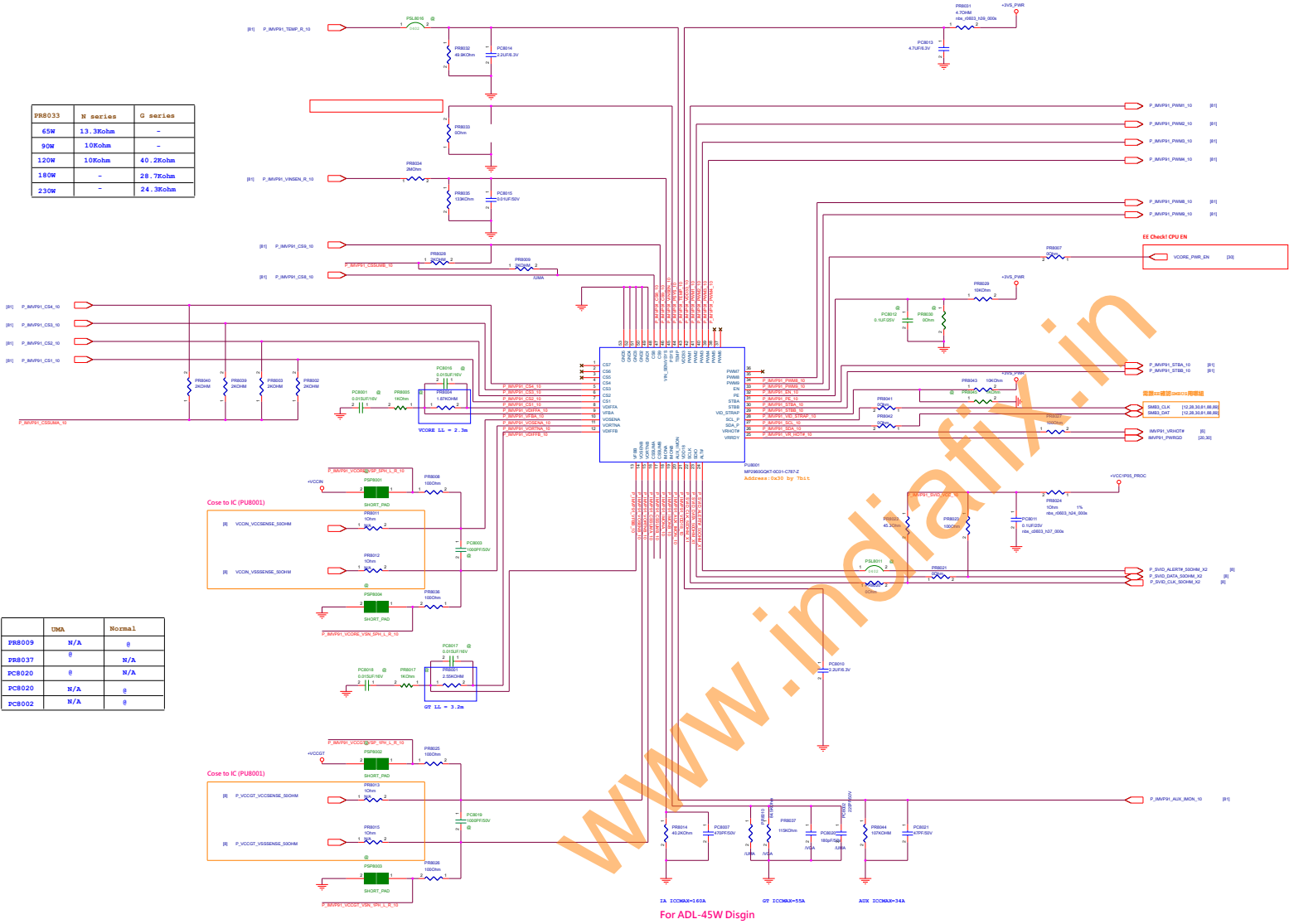
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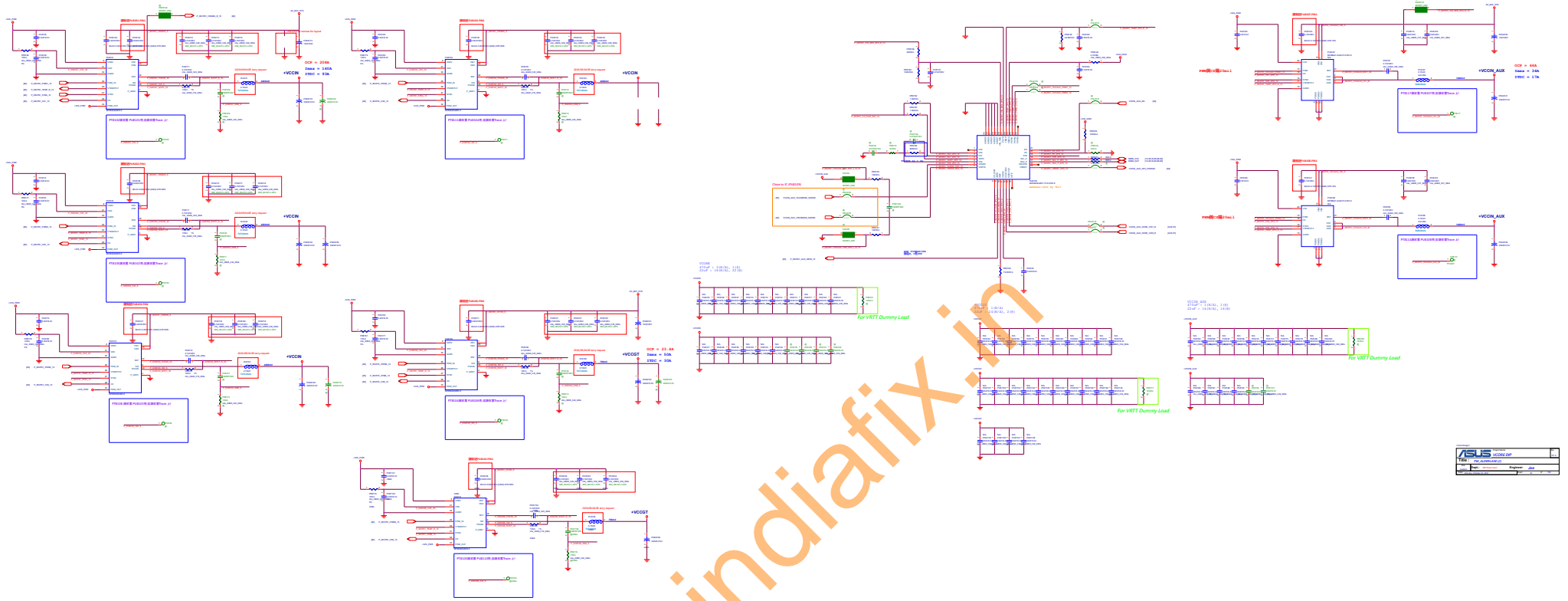
DP



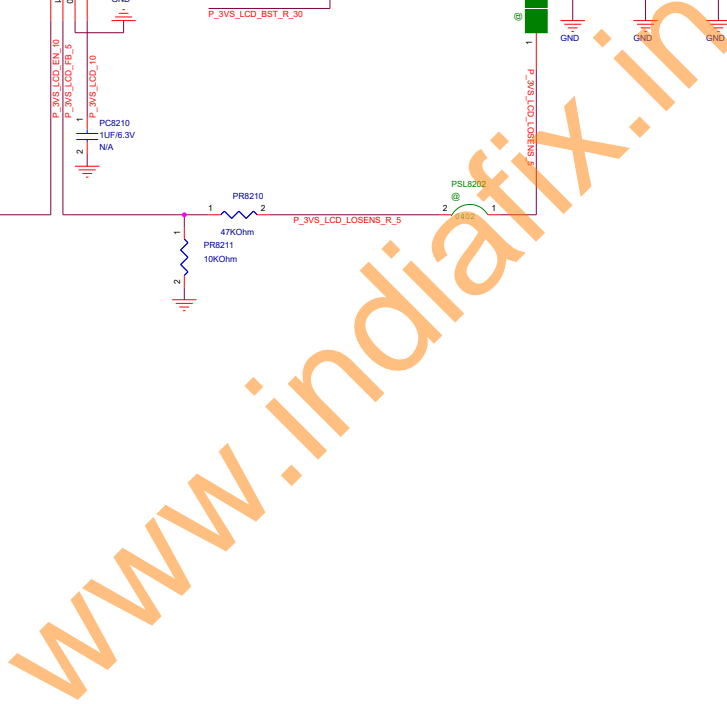


Alder Lake-P IMVP9.1 Power (1) [For CPU]






ASUS	
Model	IMVP9.1
Version	1.0
Author	ASUS
Copyright	2021

[illegible]


File <span style="color: blue;">&lt;Title&gt;</span>			
Size A3	Document Number <span style="color: blue;">&lt;Doc&gt;</span>	Rev <span style="color: blue;">&lt;RevCode&gt;</span>	
Date: <span style="color: blue;">Monday, October 25, 2021</span>		Sheet	82 of 104

+1.05VSUS [For PCH]

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		Project Name		Rev
Title :		Tiger Lake-H		R1.0
Size	Title :		PW: +1.05VSUS	
A2	Dept.:	MD Power Team	Engineer:	Power RD
Date: Monday, October 25, 2021		Sheet	81	of 104

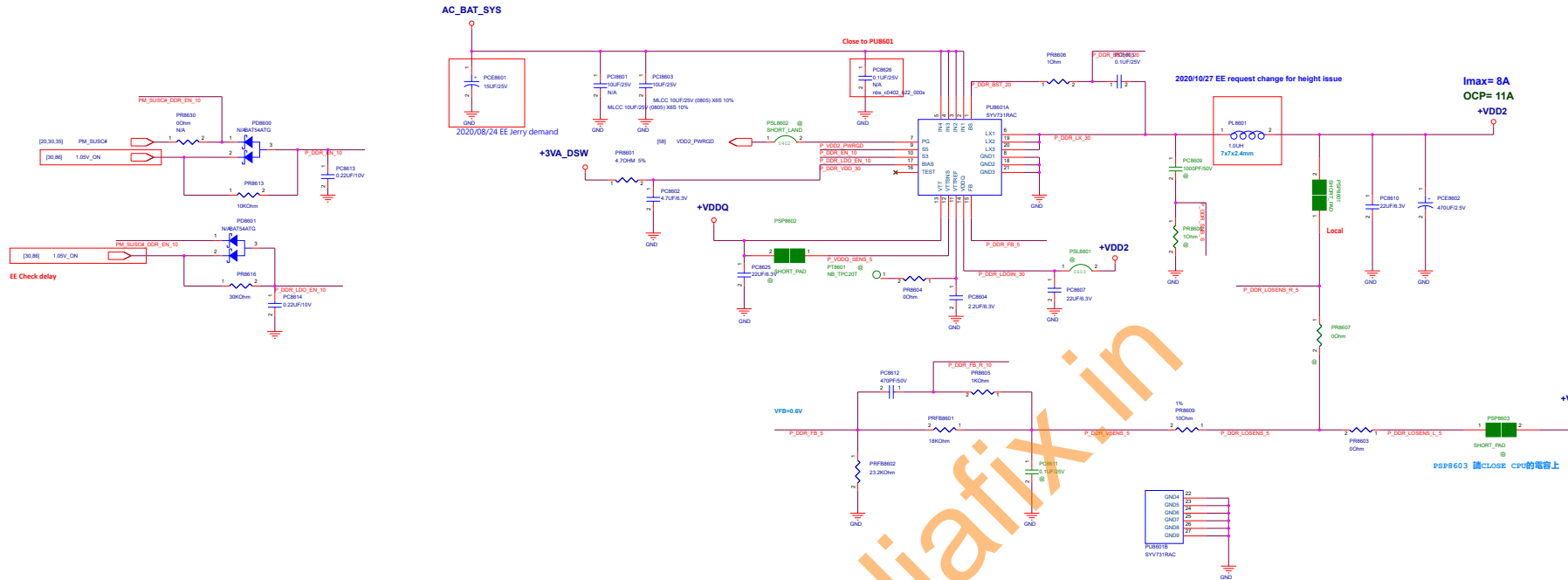


		Project Name <b>DESIGN_IP</b>		Rev <b>R1.0</b>		
<b>Title :</b> <b>PW_+1.8VSUS</b>						
Size <b>A4</b>	<b>Dept.:</b> <b>NB Power team</b>		<b>Engineer:</b> <b>Power</b>			
Date: <b>Monday, October 25, 2021</b>			Sheet	<b>84</b>	of <b>104</b>	

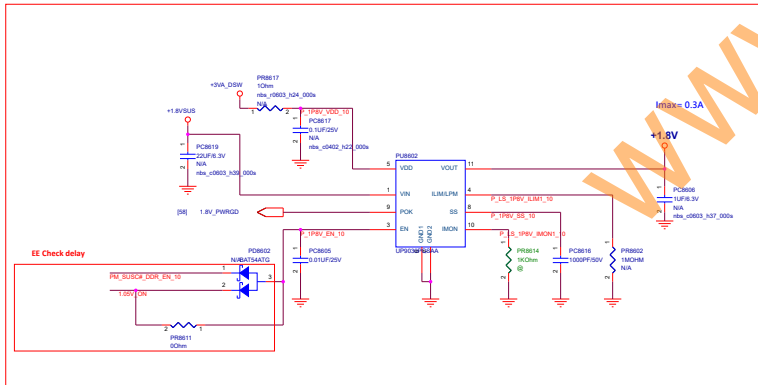
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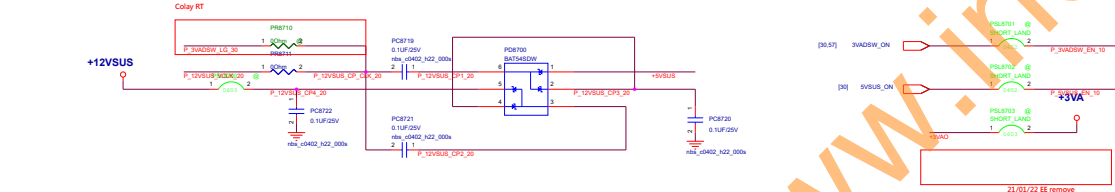
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Title : PW +1.8VSUS			
Size	Dept.:	MD Power team	Engineer: Power RD
A2			
Date: Monday, October 25, 2021	Drawn	DS	of 100

+1.05V / +VTT / +1.8V[For Memory]



DDR Type	Vout	PU8601	PRFB8601	PRFB8602	PC8604	PR8604	PIN14 NET Name
DDR4	+1.2V	Silergy / SYV731RAC 06018-02990000	20K ohm 10G212200214030	19.6K ohm 10G2122196214010	2.2UF/6.3V 11G232222525360	@	+1.2V
LPDDR4x	+1.1V	Silergy / SYV731DRAC 06018-02990100	20K ohm 10G212200214030	23.2K ohm 10G212232214030	@	0ohm 10G212000004030	+1.1V
LPDDR5	+1.05V	Silergy / SYV731RAC 06018-02990000	20K ohm 10G212200214030	26.1K ohm 10G212261214010	2.2UF/6.3V 11G232222525360	@	+1.05V



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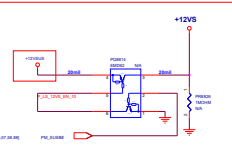
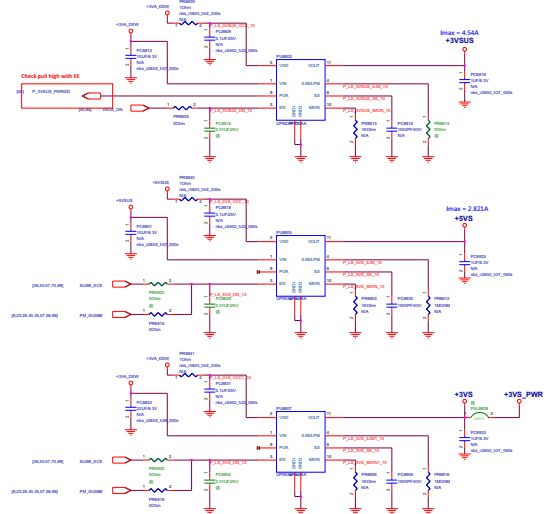
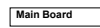
21/01/22 EE remove

Adaptor Mode (MVPS)								Battery Mode (MVPS)							
	S0	C0	S3	D03	S4	S5	S5 with USB Charger+		S0	C0	S3	D03	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	-	1	-	1	PS_ON	1	-	-	-	1	0	1
3VAD0W_ON	1	-	1	-	1	-	1	3VAD0W_ON	1	-	-	-	1	0	0
3VSD0W_ON	1	-	1	-	1	-	1	3VSD0W_ON	1	-	-	0	0	0	0
5VSD0W_ON	1	-	1	-	1	-	1	5VSD0W_ON	1	-	-	-	1	0	1
1.35V_ON	1	-	1	-	0	-	0	1.35V_ON	1	-	-	-	1	0	0
BUSC_ECF	1	-	1	-	0	-	0	BUSC_ECF	1	-	-	0	0	0	0
SUSB_ECF	1	-	0	-	0	-	0	SUSB_ECF	1	-	-	0	0	0	0





### Load Switch

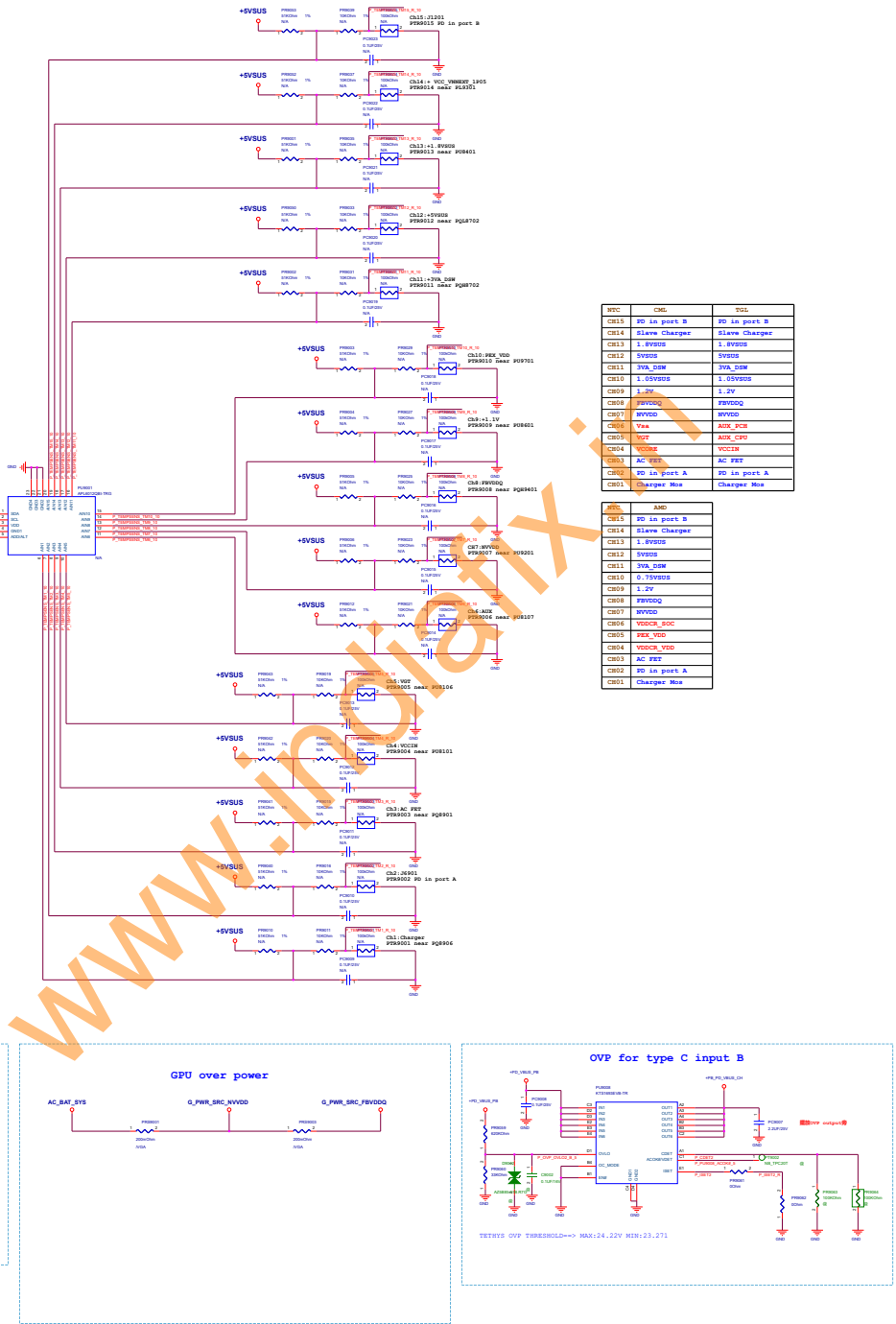
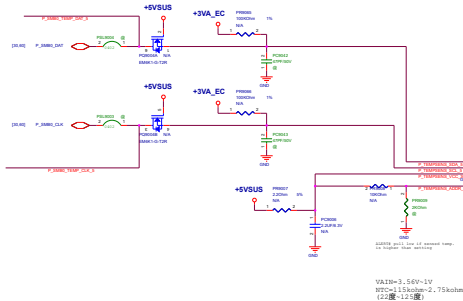




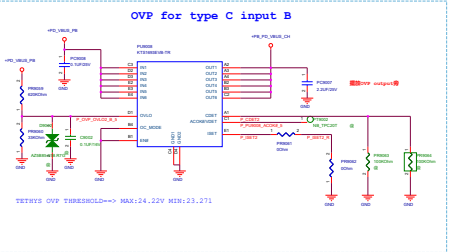
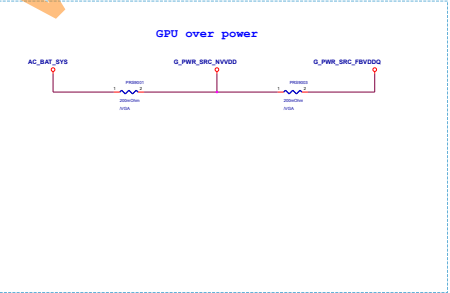
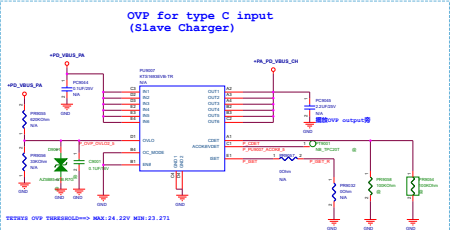
P90\_PROTECTION

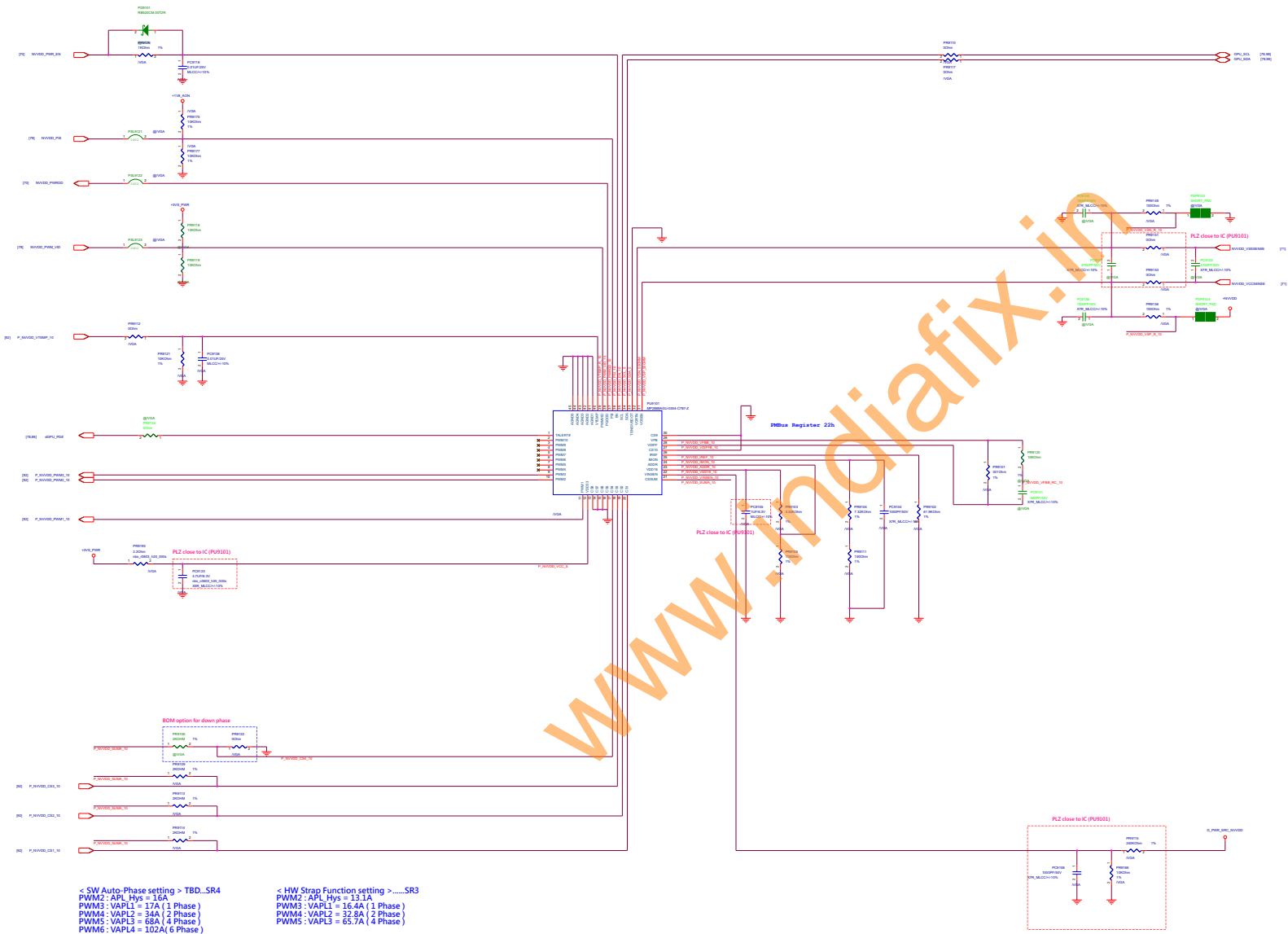
Address Selection Table											
Address	CS0	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10
00000000	0	0	0	0	0	0	0	0	0	0	0
00000001	0	0	0	0	0	0	0	0	0	0	0
00000002	0	0	0	0	0	0	0	0	0	0	0
00000003	0	0	0	0	0	0	0	0	0	0	0
00000004	0	0	0	0	0	0	0	0	0	0	0
00000005	0	0	0	0	0	0	0	0	0	0	0
00000006	0	0	0	0	0	0	0	0	0	0	0
00000007	0	0	0	0	0	0	0	0	0	0	0
00000008	0	0	0	0	0	0	0	0	0	0	0
00000009	0	0	0	0	0	0	0	0	0	0	0
0000000A	0	0	0	0	0	0	0	0	0	0	0
0000000B	0	0	0	0	0	0	0	0	0	0	0
0000000C	0	0	0	0	0	0	0	0	0	0	0
0000000D	0	0	0	0	0	0	0	0	0	0	0
0000000E	0	0	0	0	0	0	0	0	0	0	0
0000000F	0	0	0	0	0	0	0	0	0	0	0

Register Address											
Address	CS0	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10
0000	0	0	0	0	0	0	0	0	0	0	0
0001	0	0	0	0	0	0	0	0	0	0	0
0002	0	0	0	0	0	0	0	0	0	0	0
0003	0	0	0	0	0	0	0	0	0	0	0
0004	0	0	0	0	0	0	0	0	0	0	0
0005	0	0	0	0	0	0	0	0	0	0	0
0006	0	0	0	0	0	0	0	0	0	0	0
0007	0	0	0	0	0	0	0	0	0	0	0
0008	0	0	0	0	0	0	0	0	0	0	0
0009	0	0	0	0	0	0	0	0	0	0	0
000A	0	0	0	0	0	0	0	0	0	0	0
000B	0	0	0	0	0	0	0	0	0	0	0
000C	0	0	0	0	0	0	0	0	0	0	0
000D	0	0	0	0	0	0	0	0	0	0	0
000E	0	0	0	0	0	0	0	0	0	0	0
000F	0	0	0	0	0	0	0	0	0	0	0

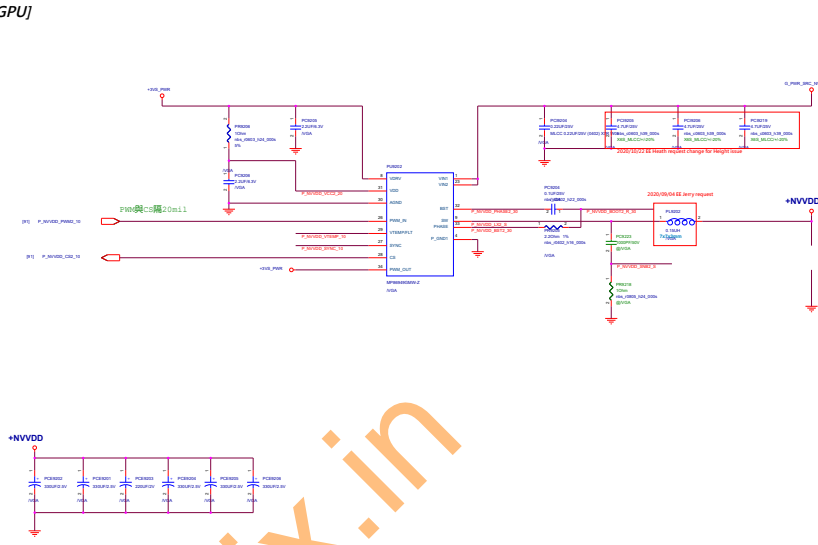
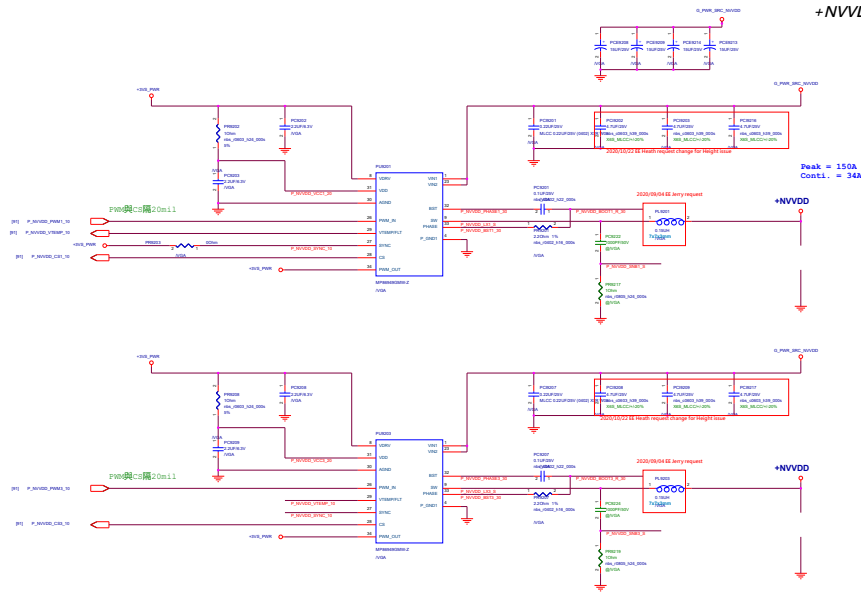


WPC	CHG	Vol
CH15	PD in port B	PD in port B
CH14	Slave Charger	Slave Charger
CH13	1.8VSDR	1.8VSDR
CH12	SVSDR	SVSDR
CH11	SVR_10M	SVR_10M
CH10	1.0VSDR	1.0VSDR
CH09	1.2V	1.2V
CH08	SVSDRQ	SVSDRQ
CH07	SVSDR	SVSDR
CH06	Vaa	AUX_PCB
CH05	VTP	AUX_CPU
CH04	VSDR	VSDR
CH03	AC_VSD	AC_VSD
CH02	PD in port A	PD in port A
CH01	Charger Nue	Charger Nue





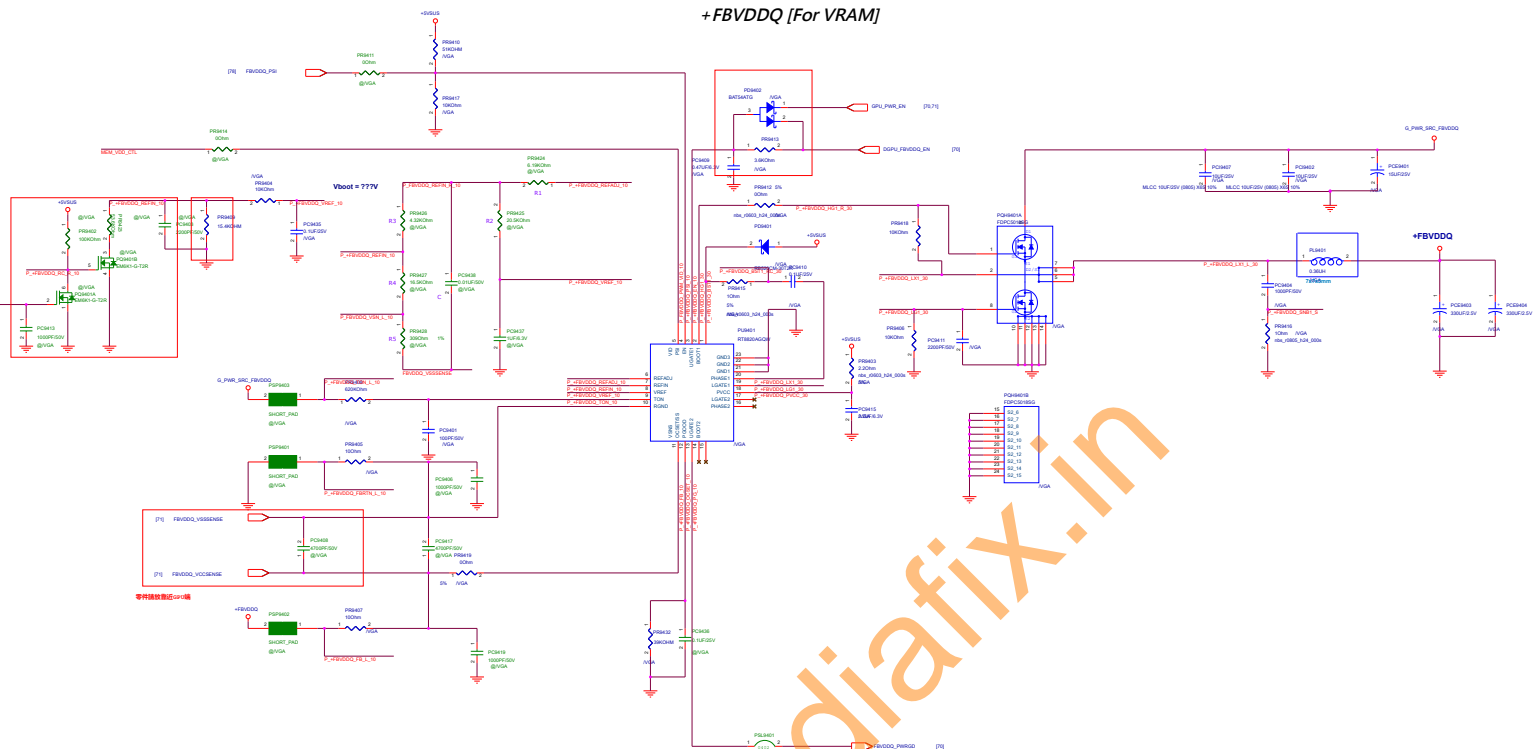
+NVVDD [For DGPU]



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<Variant Name>			
Title			
<Title>			
Size	Document Number		Size
A4	<Doc>		1.0
Date	Monday, October 26, 2021	Sheet 55 of 124	

## +FBVDDQ [For VRAM]



DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PRP404	1000ms	
PRP409	21.580ms	
PRP423	7500ms	

DVS Setting		
MEM_VID_CTL	H	L
Voltage	1.35V	1.2V
PRP404	1.080um	
PRP409	21.580um	
PRP423	53.680um	

DVS Setting		
MEM_VDD_CTL	R	L
Voltage	1.25V	1.2V
PRP404	1080m	
PRP409	16.980m	
PRP423	14080m	

Fixed Vout		
8	PC9403/999421/PQ9401 999402/999414	
Voltage	1.25V	1.2V
999404	10KOhm	
999409	16.9KOhm	15.4KOhm


PT940\* 請放置 PU9401旁;並請放置Trace 上!

PT9401  
1 1  
P\_9401001\_001\_001  
NB\_TPG001

PT9402  
1 1  
P\_9402002\_001\_001  
NB\_TPG001

PT9403  
1 1  
P\_9403003\_001\_001  
NB\_TPG001

©Core Design


		Title : OTH_for test only	
ASUS COMPUTER		Engineer: EE	
Site	Project Name		Rev
A	GA401		R1.0
Date	Monday, October 25, 2021		Print 05 of 106

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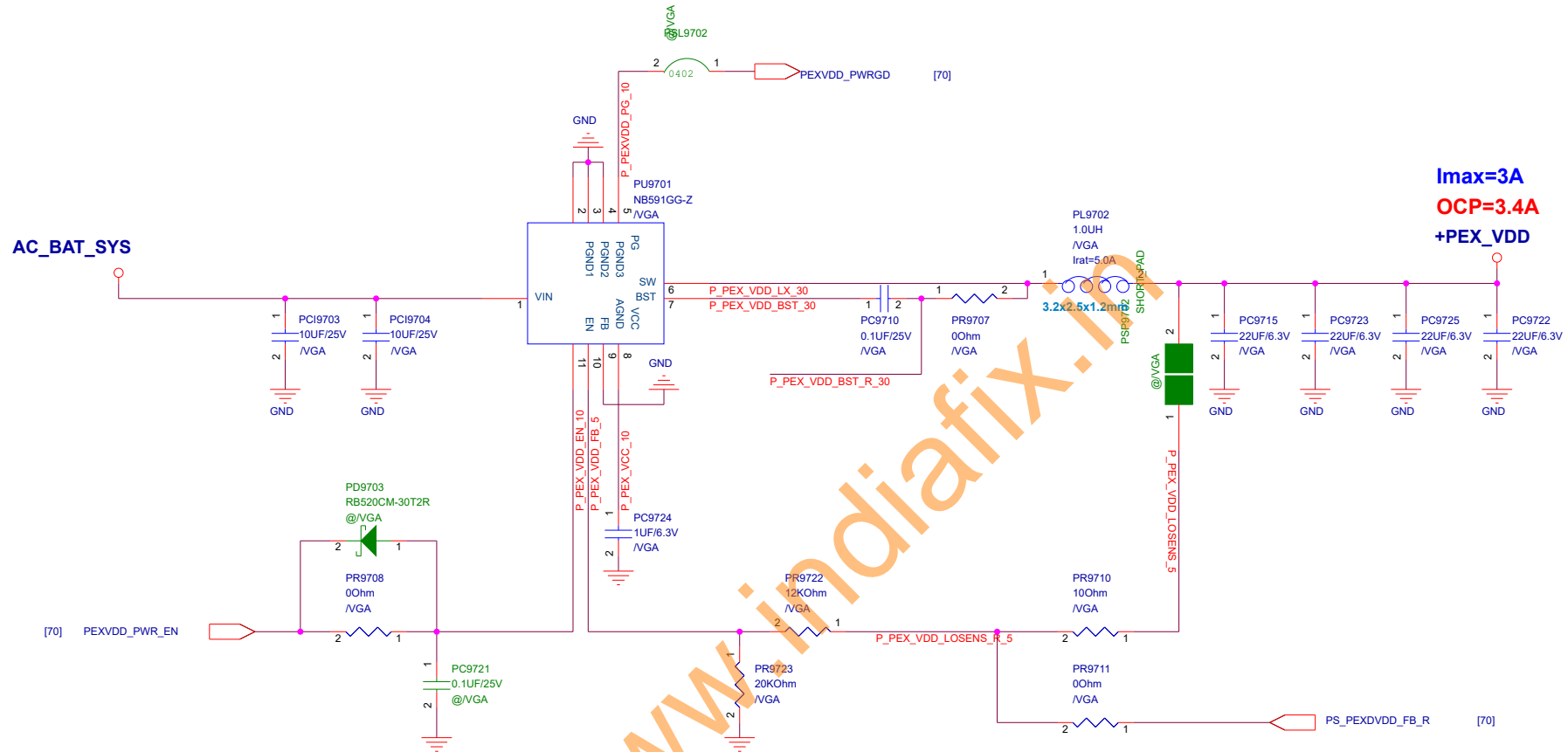


+12VS\_FAN [For FAN]

<Variant Name>

		Project Name	Rev
		GA503QS	R1.0
Title : PW_+12VS_FAN			
Size	Dept.: NB Power team		Engineer: Power RD
A4			
Date: Monday, October 25, 2021	Sheet	96	of 104

# PEX\_VDD [For GPU]



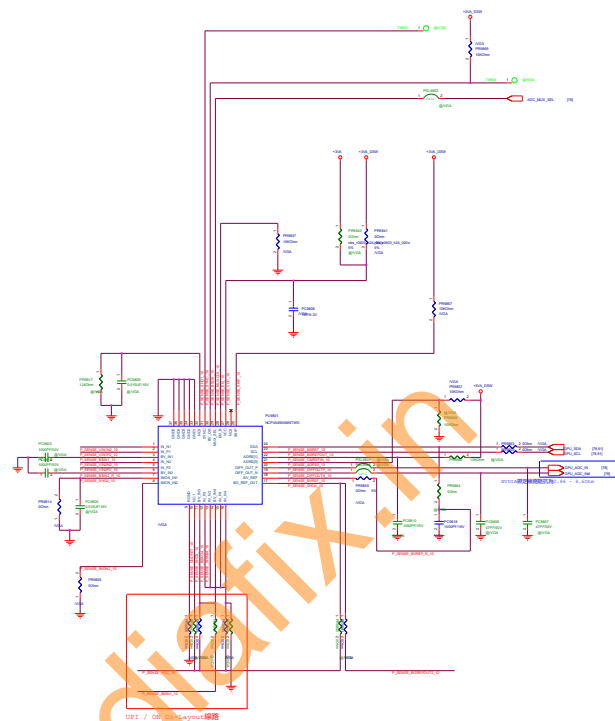
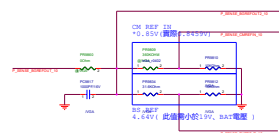
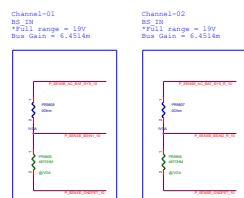
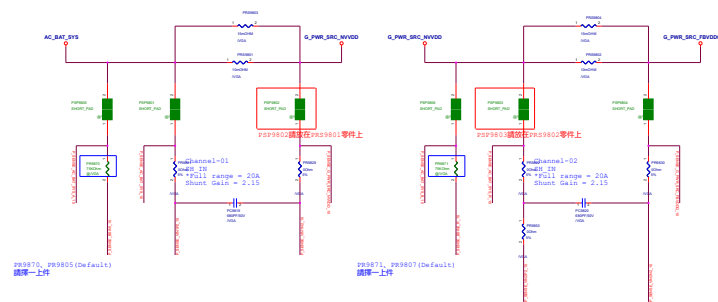
PT840\* 請放置 PU8401旁;並請放置Trace 上!

P\_PEX\_VDD\_LX\_30

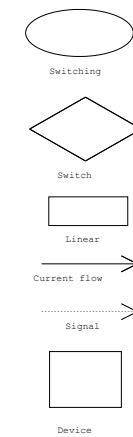
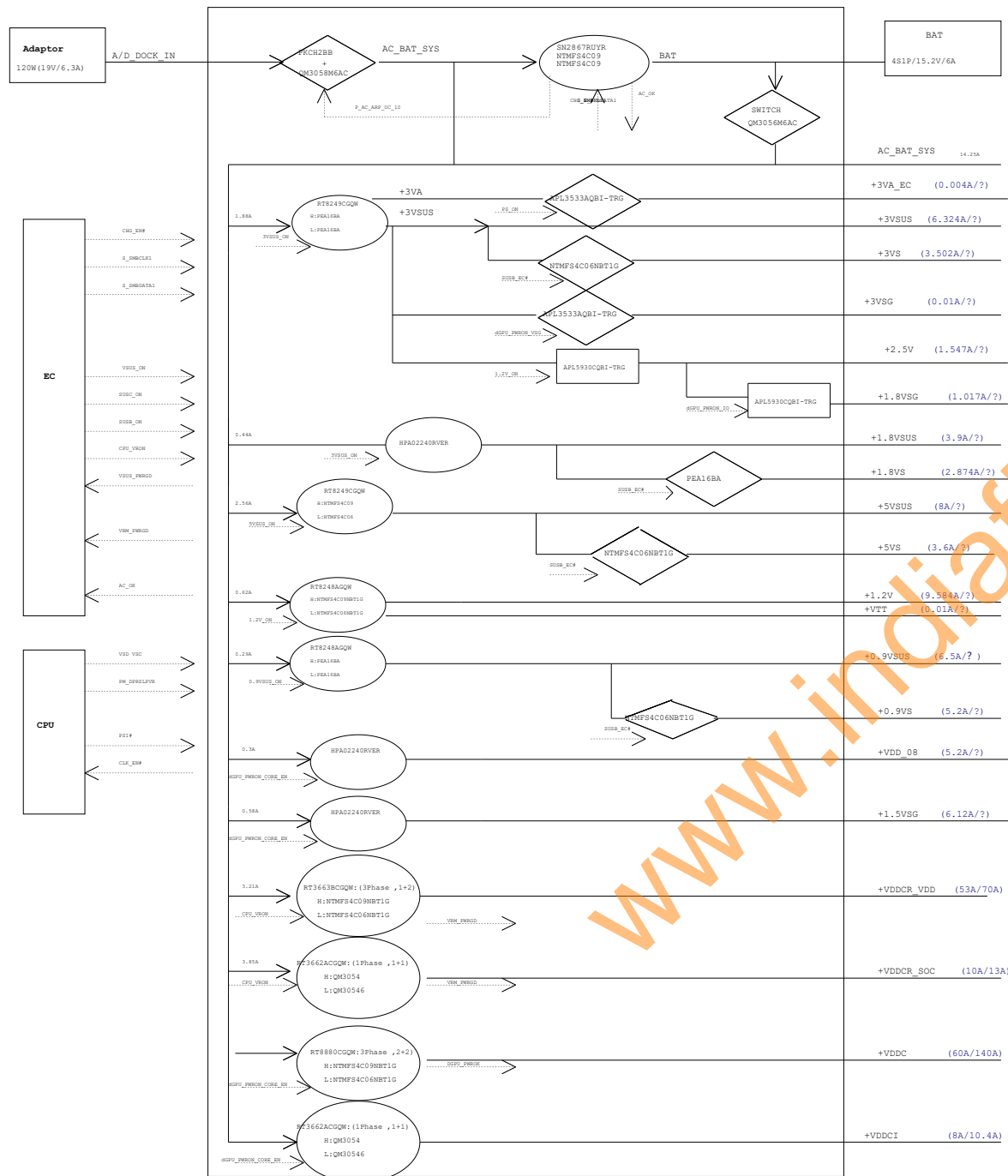
PT9701

TPC20T

Project Name		Rev
ASUS Project Name		R1.0
Title : PEX_VDD		
Size A4	Dept.: ASUSTeK COMPUTER INC.	Engineer: Power_RD
Date: Monday, October 25, 2021	Sheet	97 of 104



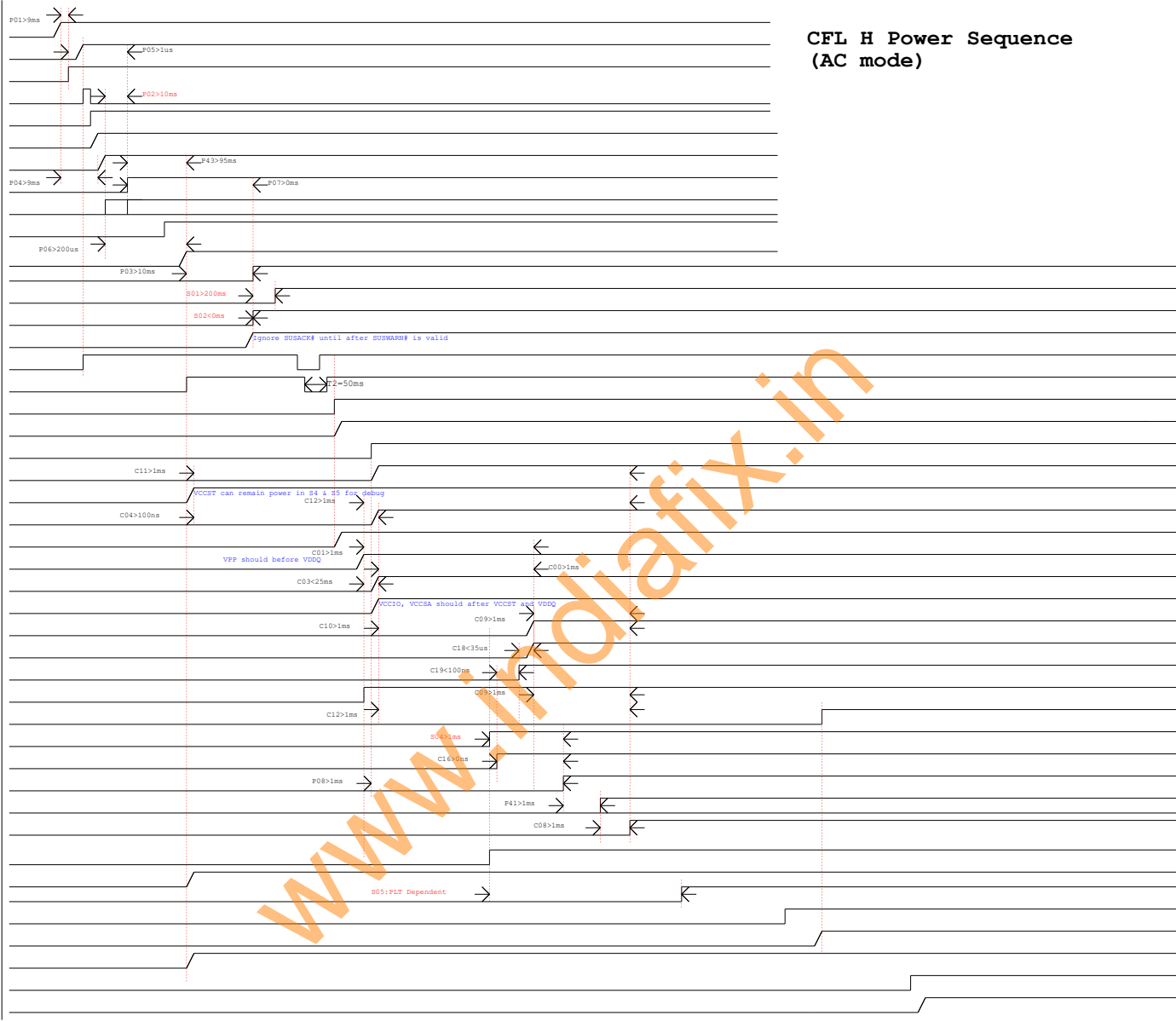
	PR9801	PR9805	PR9807	PR9803	PR9804	PR9805	PR9814	PR9855	PR9822
GN20	NC94549500W7W0 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0	0	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP950260QGT 06129-00110100	75K0hm 10G212750214010	75K0hm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.0150UF/16V 11G232115311360	3570hm 10G212357014010	0	49.90hm 10G212499914010
	PR9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PR9809	PR9808
GN20	0	0	0	10K0hm 10G212100214010	01.4314hm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0
N18P-G1	1000PF/10V 11G232110211030	0 Ohm 10G212000004030	360K0hm 10G212364004010	480K0hm 10G21480314010	360K0hm 10G213624314010	0	0.0150UF/16V 11G232115311360	4870hm 10G212487014010	0
	PR9806	PR9861	PR9864	PR9857	PR9801	PR9863	PR9817	PR9844/PR9845/PR9856	PR9846/PR9847
GN20	0	0 Ohm 10G212000004030	0	10K0hm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0	0 Ohm 10G212000004030	0
N18P-G1	4870hm 10G212487014010	0	0 Ohm 10G212000004030	0	1000hm 10G212100014010	49.90hm 10G212499914010	3570hm 10G212357014010	0	0 Ohm 10G212000004030



AC-IN Mode

C:CPU  
P:PCH  
S:FLT  
Power  
Signal

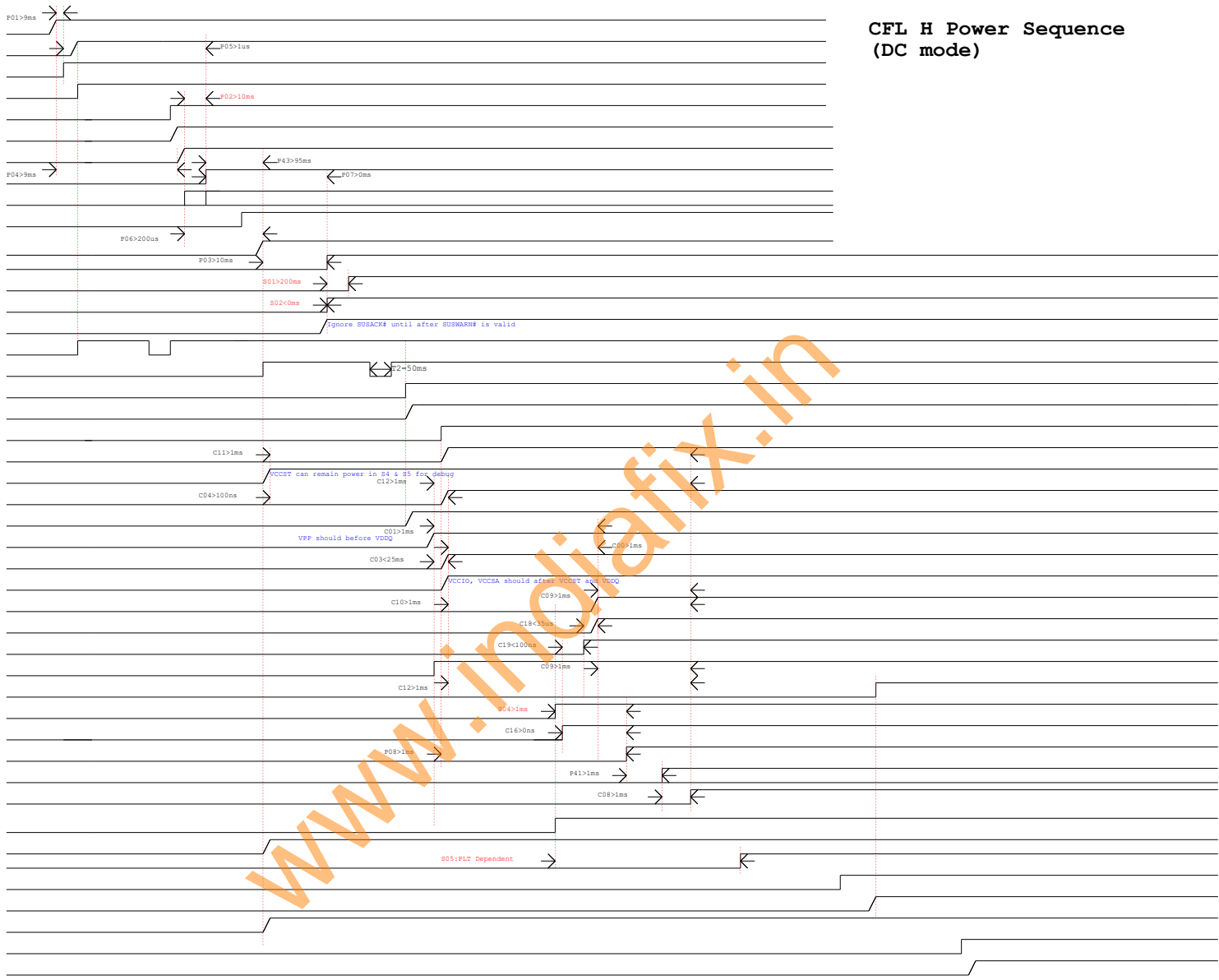
(+RTCBAT)+3VA\_RTC  
(AC\_BAT\_SYS)+3VA/+5VA  
(+3VA\_RTC)RTCRST#(PCH)  
(Power)AC\_IN\_OC#(EC)  
(EC)PS\_ON(+3VA\_EC)  
(PS\_ON)+3VA\_EC(EC)  
(3VADSW\_ON)+3VA\_DSW(3VA\_DSW\_PWRGD)  
(EC)DPWROK\_EC(PCH)  
(+3VA\_DSW)PM\_BATLOW#(PCH)  
(PCH)PM\_SLP\_SUS#(EC)  
(VSUS\_ON)+1.0VSUS\_VCCPRIM(1.0VSUS\_PWRGD)  
(EC)PM\_RSMRST#\_PCH(PCH)  
(PCH)SUSWARN#(EC)  
(EC)ME\_AC\_PRESENT\_PCH(PCH)  
(EC)PCH\_SUSACK#(PCH)  
(PWR Switch)PWR\_SW#(EC)  
(EC)PM\_PWRBTN#(PCH)  
(EC)SUSC\_EC#(Power)  
(SUSC\_EC#)+12V/+5V/+3V  
(EC)SUSB\_EC#(Power)  
(SUSB\_EC#)+12VS/+5VS/+3VS  
(SUSB\_EC#)+1.0V\_VCCST,VCCPLL  
(SUSB\_EC#)+VCCIO,(+12VS)+VCCSTG  
(1.2V\_ON)+2.5V(2.5V\_PWRGD)  
(1.2V\_ON)+VDDQ\_CPU(1.2V\_PWRGD)  
(+12VS)+VCCPLL\_OC  
(SUSB\_EC#)+VCCIO(VCCIO\_PWRGD)  
(ALL\_SYSTEM\_PWRGD)+VCCSA(IMVP8\_PWRGD)  
(DDR\_VTT\_CTRL)+0.6V  
(CPU)DDR\_VTT\_CTRL(Power)  
(Power)1.2V\_PWRGD(AND)  
(Power)IMVP8\_PWRGD  
(AND)ALL\_SYSTEM\_PWRGD(CPU/PCH/EC/Power)  
(ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU(CPU)  
(EC)PM\_PWROK\_PCH(PCH)  
(PCH)CLK\_PCH\_BCLK(CPU)  
(PCH)H\_CPUPWRGD(CPU)  
(CPU)P\_SVID\_DATA\_X2(Power)  
(EC)PM\_SYSPWROK\_PCH(PCH)  
(PCH)PLT\_RST#(CPU/EC/Device)  
(P\_IMVP8\_DRVON)+VCCCORE(IMVP8\_PWRGD)  
(CPU)H\_THERMTRIP#(PCH)  
(PCH)DDR4\_DRAMRST#(Memory)  
+VCCGT



CFL H Power Sequence  
(AC mode)

DC-IN Mode


C:CPU (+RTCBAT)+3VA\_RTC  
P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
S:PLT (+3VA\_RTC)RTCRST# (PCH)  
Power (Power)AC\_IN\_OC# (EC)  
Signal (EC)PS\_ON(+3VA\_EC)  
(PS\_ON)+3VA\_EC (EC)  
(3VADSW\_ON)+3VA\_DSW (3VA\_DSW\_PWRGD)  
(EC)DPWROK\_EC (PCH)  
(+3VA\_DSW)PM\_BATLOW# (PCH)  
(PCH)PM\_SLP\_SUS# (EC)  
(VSUS\_ON)+1.0VSUS\_VCCPRIM(1.0VSUS\_PWRGD)  
(EC)PM\_RSMRST#\_PCH (PCH)  
(PCH)SUSWARN# (EC)  
(EC)ME\_AC\_PRESENT\_PCH (PCH)  
(EC)PCH\_SUSACK# (PCH)  
(PWR Switch)PWR\_SW# (EC)  
(EC)PM\_PWRBTN# (PCH)  
(EC)SUSC\_EC# (Power)  
(SUSC\_EC#)+12V/+5V/+3V  
(EC)SUSB\_EC# (Power)  
(SUSB\_EC#)+12VS/+5VS/+3VS  
(VSUS\_ON)+1.0V\_VCCST,VCCPLL(VCCST\_PWRGD)  
(+VCCIO)+VCCSTG  
(1.2V\_ON)+2.5V (2.5V\_PWRGD)  
(1.2V\_ON)+VDDQ\_CPU (1.2V\_PWRGD)  
(+12VS)+VCCPLL\_OC  
(SUSB\_EC#)+VCCIO(VCCIO\_PWRGD)  
(ALL\_SYSTEM\_PWRGD)+VCCSA(IMVP8\_PWRGD)  
(DDR\_VTT\_CTRL)+0.6V  
(CPU)DDR\_VTT\_CTRL (Power)  
(Power)1.2V\_PWRGD (AND)  
(Power)IMVP8\_PWRGD  
(AND)ALL\_SYSTEM\_PWRGD (CPU/PCH/EC/Power)  
(ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU (CPU)  
(EC)PM\_PWROK\_PCH (PCH)  
(PCH)CLK\_PCH\_BCLK (CPU)  
(PCH)H\_CPU\_PWRGD (CPU)  
(ALL\_SYSTEM\_PWRGD)P\_IMVP8\_EN\_I0 (Power)  
(CPU)P\_SVID\_DATA\_X2 (Power)  
(EC)PM\_SYSPWROK\_PCH (PCH)  
(PCH)PLT\_RST# (CPU/EC/Device)  
(P\_IMVP8\_DRVON)+VCCCORE(IMVP8\_PWRGD)  
(CPU)H\_THERMTRIP# (PCH)  
(PCH)DDR4\_DRAMRST# (Memory)  
+VCCGT



CFL H Power Sequence  
(DC mode)

Rev	Date	Description
1.0		

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		<b>Title :</b> Revision	
<small>ASUSTeK COMPUTER</small>		<b>Engineer:</b> ROG EE	
Size A3	Project Name GX501IP2	Rev 1.0	
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60 PN	LOCATION		PART NUMBER


CPU SKU	LOCATION	PART NUMBER
	U301	
	U301	
	U301	
	U301	

60 PN	PART NUMBER	LOCATION

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		Title : HISTORY	
ASUSTeK COMPUTER		Engineer: ROG EE	
Size	Project Name		Rev
A3	GX501IP2		1.0
Date	Monday, October 25, 2021		Sheet 104 of 104