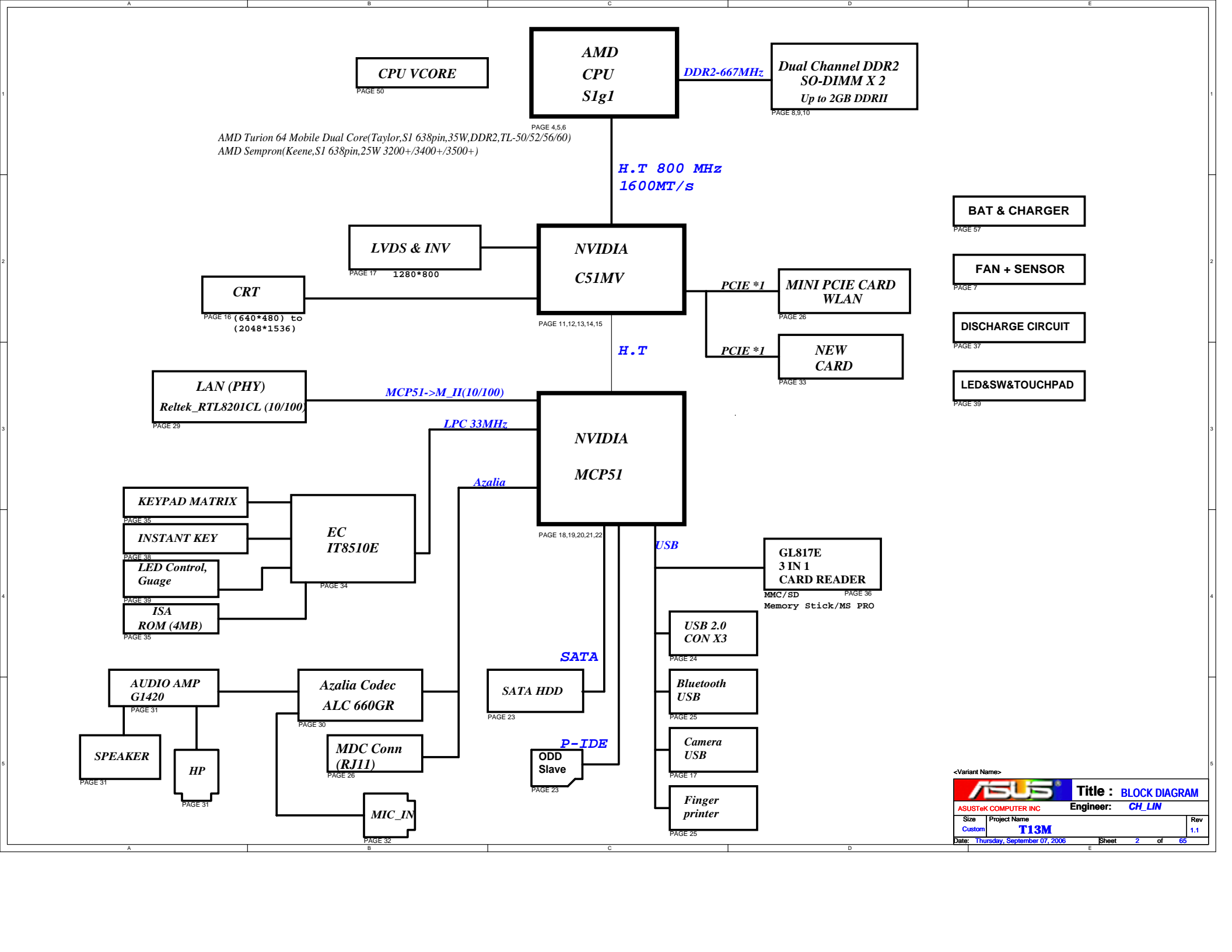


T13M SCHEMATIC Revision 1.1


PAGE	Content	PAGE	Content
	SYSTEM PAGE REF.		POWER PAGE REF.
4	AMD S1 CPU(1)-HT&MISC	50	_POWER_VCORE
5	AMD S1 CPU(2)-DDR11	51	_POWER_SYSTEM
6	AMD S1 CPU(3)-POWER&GND	52	_POWER_I/O_1.8V & 1.05VS
7	Fan CTRL/THERMAL SENSOR	53	_POWER_I/O_DDR & VTT
8	DDR2 SO-DIMM_0	54	_POWER_I/O_VTT & +2.5VS
9	DDR2 SO-DIMM_1	55	_POWER_VGA_CORE(Empty)
10	DDR2 ADDRESS TERMINATION	56	_POWER_VGA_RAM(Empty)
11	C51MV HT TO CPU	57	_POWER_CHARGER
12	C51MV HT TO MCP	58	_POWER_PIC(Empty)
13	C51MV PCIEx16	59	_POWER_DETECT
14	C51MV VGA&LVDS	60	_POWER_PROTECT
15	C51MV POWER&GND	61	_POWER_LOAD SWITCH
16	CRT CONN	62	_POWER_FLOWCHART
17	LVDS & INVERTER CONN	63	_POWER_SIGNAL
18	MCP51_HT TO C51MV		
19	MCP51_PCI I/F		
20	MCP51_SATA&IDE&LAN		
21	MCP51_USB&GPIO&MISC		
22	MCP51_POWER&GND		
23	HDD & CD-ROM CONN		
24	USB PORTS		
25	B/T & F/P		
26	B To B CONN(M)		
27	EMPTY		
28	EMPTY		
29	LAN PHY RTL8201CL(10/100)		
30	AZALIA - ALC660-GR		
31	AUDIO_AMPLIFIER		
32	MICROPHONE		
33	NEW CARD		
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36	Card Reader GL817E		
37	DISCHARGE		
38	Instant Key & FFC CONN		
39	LEDs		
40	EMPTY		
41	EMPTY		
42	EMPTY		
43	EMPTY		
44	EMPTY		
45	DC & BAT IN		
46	SREW HOLE		
47	SCH Information		
48	History(1)		
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<Variant Name>			
		Title : PAGE REF.	
ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size	Project Name		Rev
Custom	T13M		1.1
Date: Thursday, September 07, 2006		Sheet	1 of 65



	5	4	3	2	1
D					
C					
B					
A					

<Variant Name>



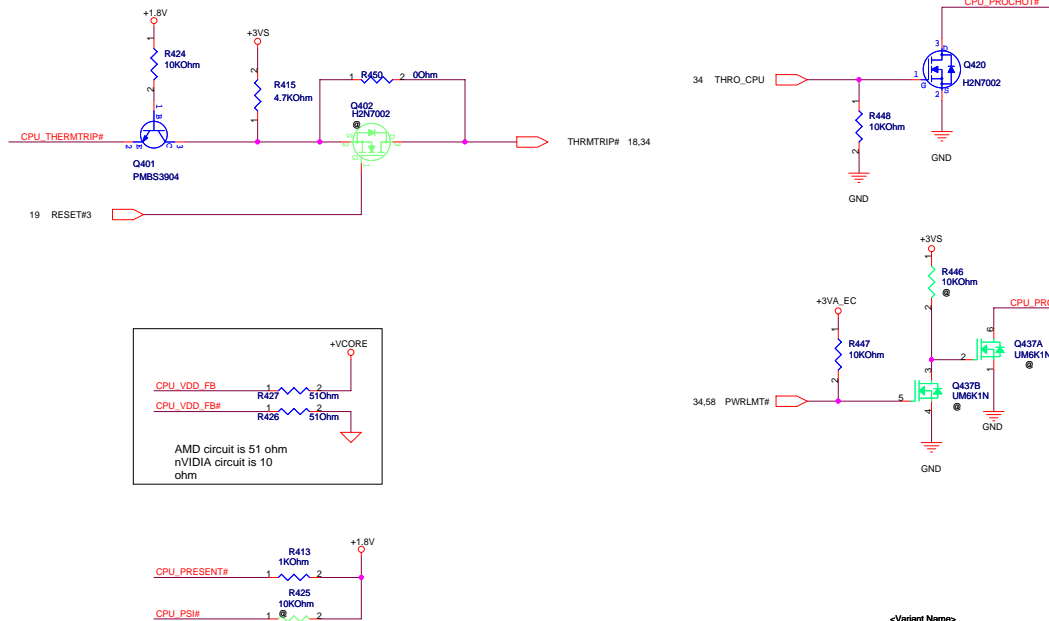
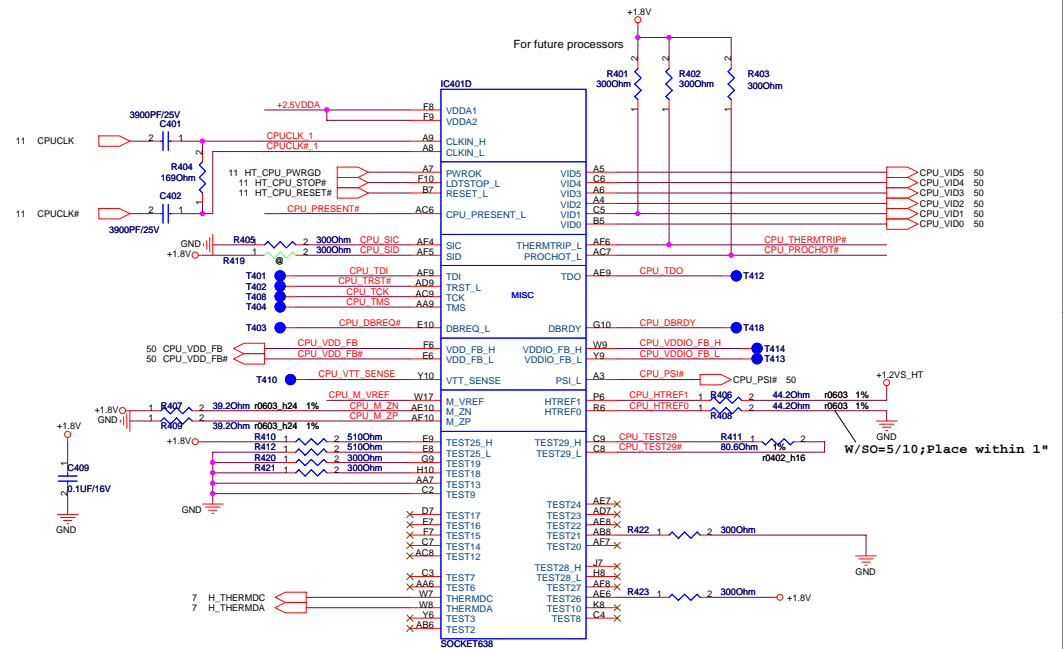
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ASUSTeK COMPUTER INC

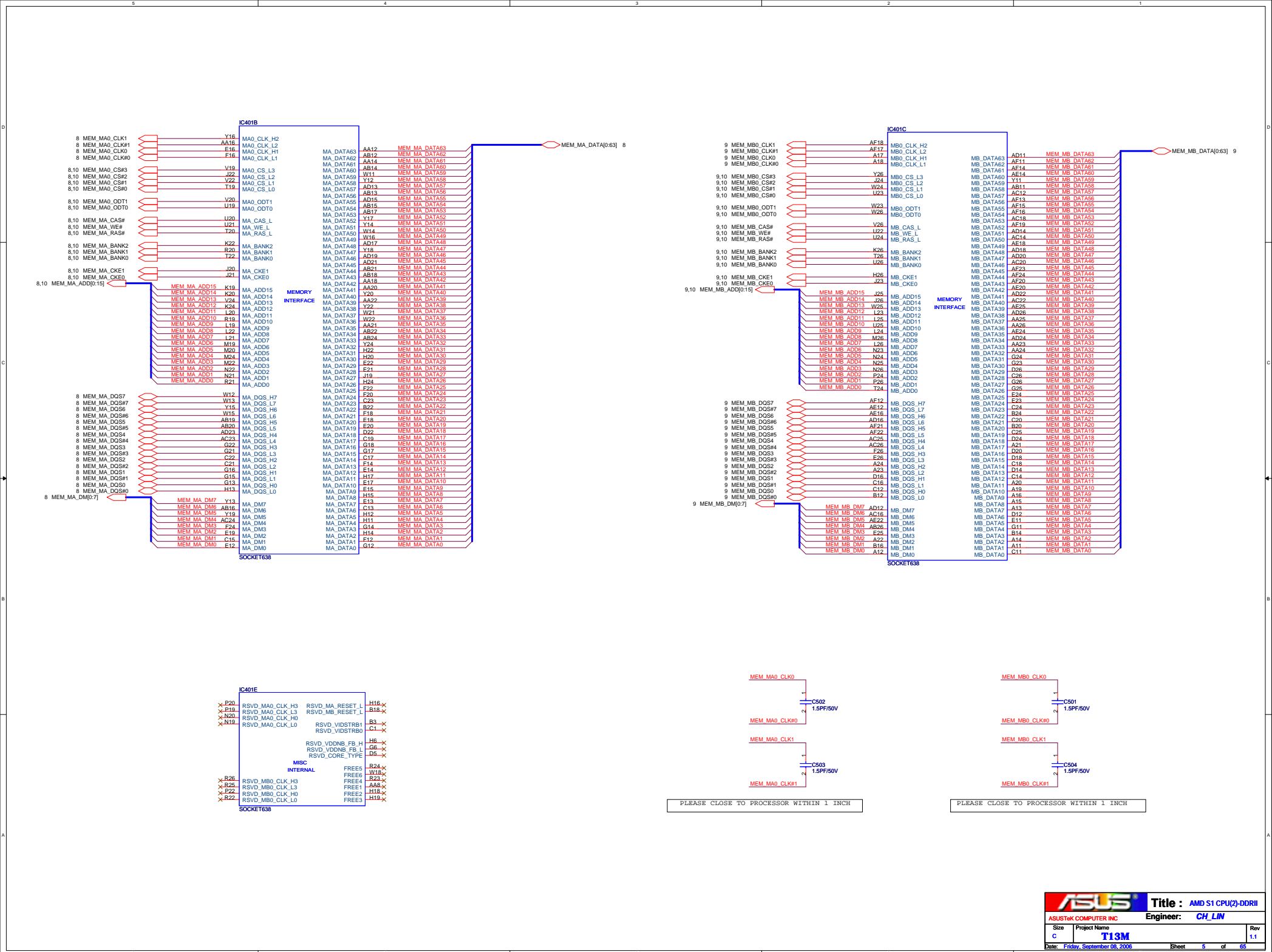
Engineer: **CH LIN**

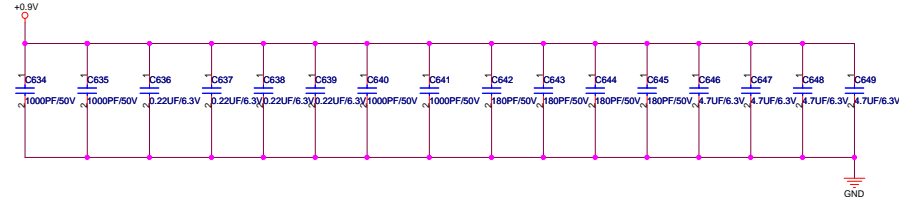
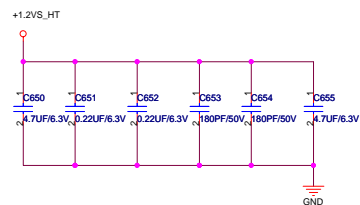
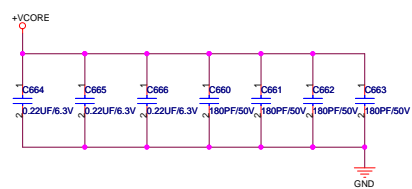
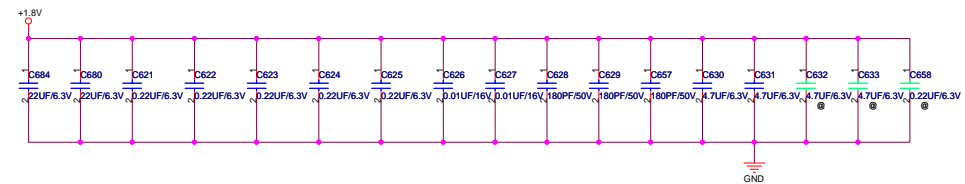
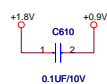
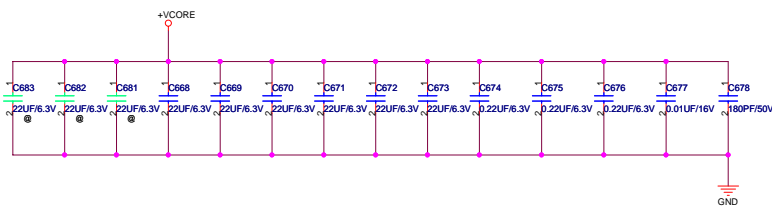
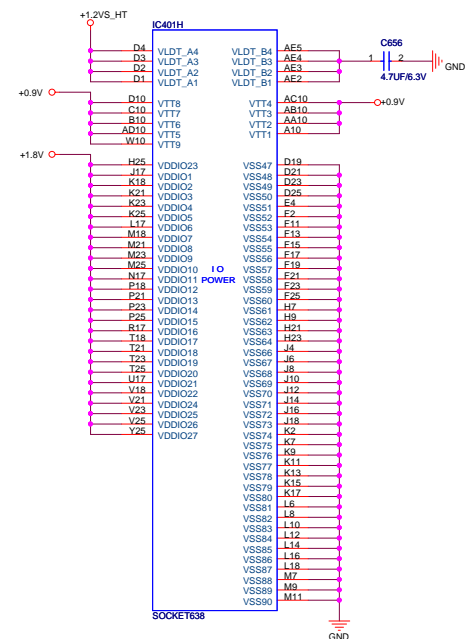
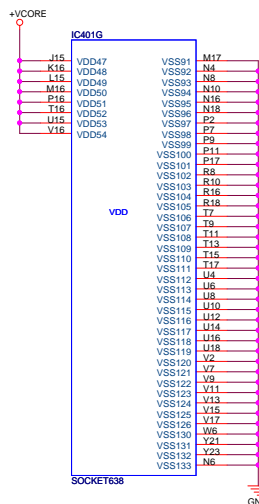
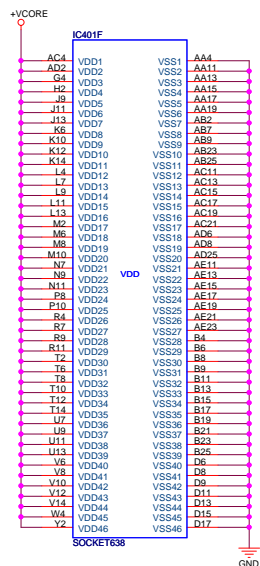
Size	Project Name	Rev
Custom	T13M	1.1

Date: **Thursday, September 07, 2006** Sheet **3** of **65**

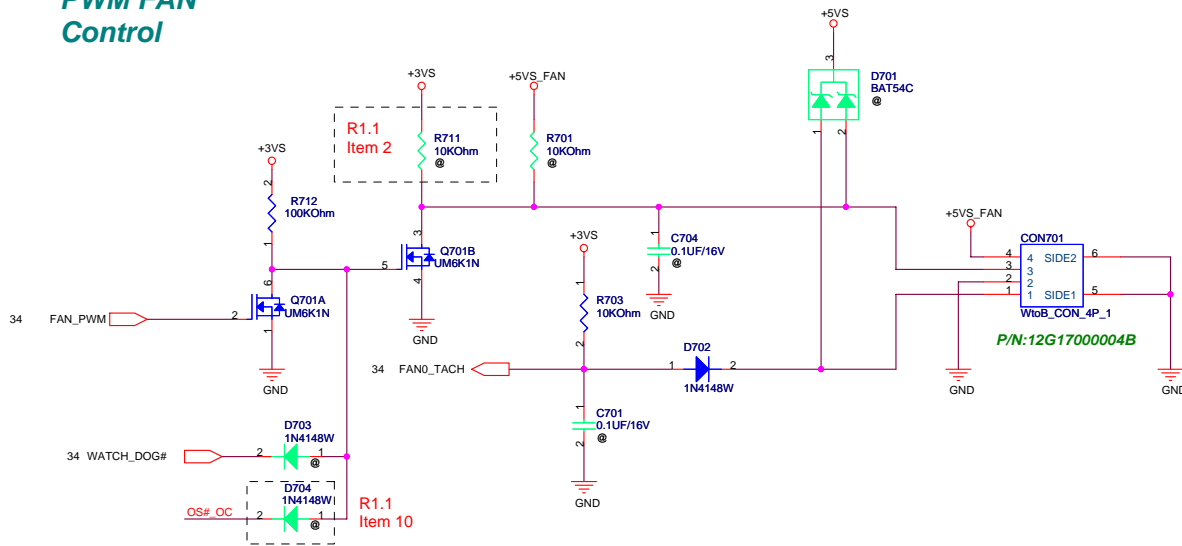


AMD circuit is 51 ohm
nVIDIA circuit is 10 ohm

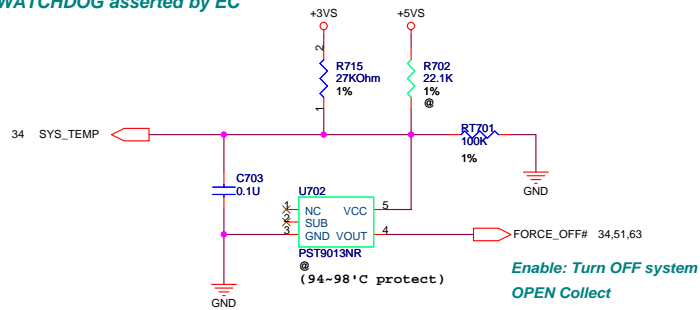




PWM FAN Control

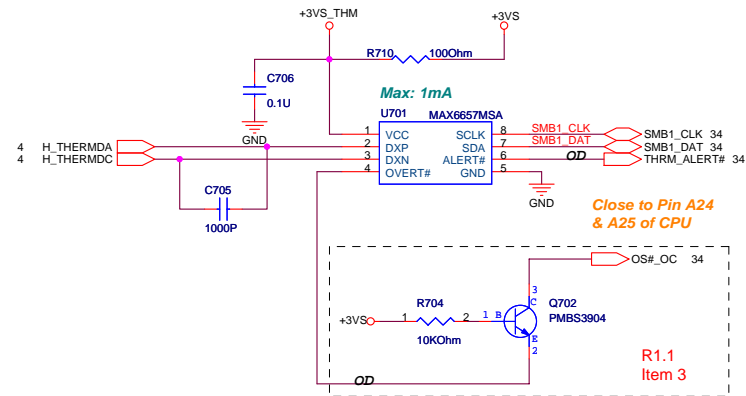


CPU FAN will be forced on:
1) Thermal Sensor Over-temperature
2) WATCHDOG asserted by EC



Enable: Turn OFF system
OPEN Collect

Thermal Sensor

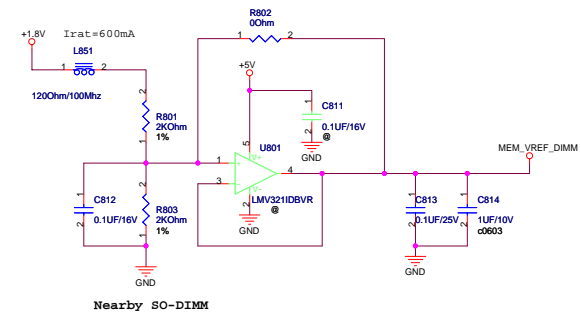
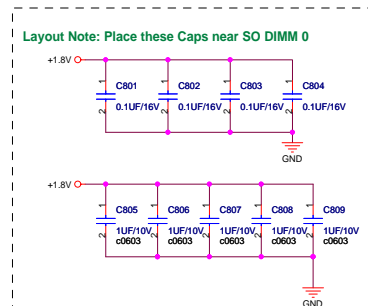
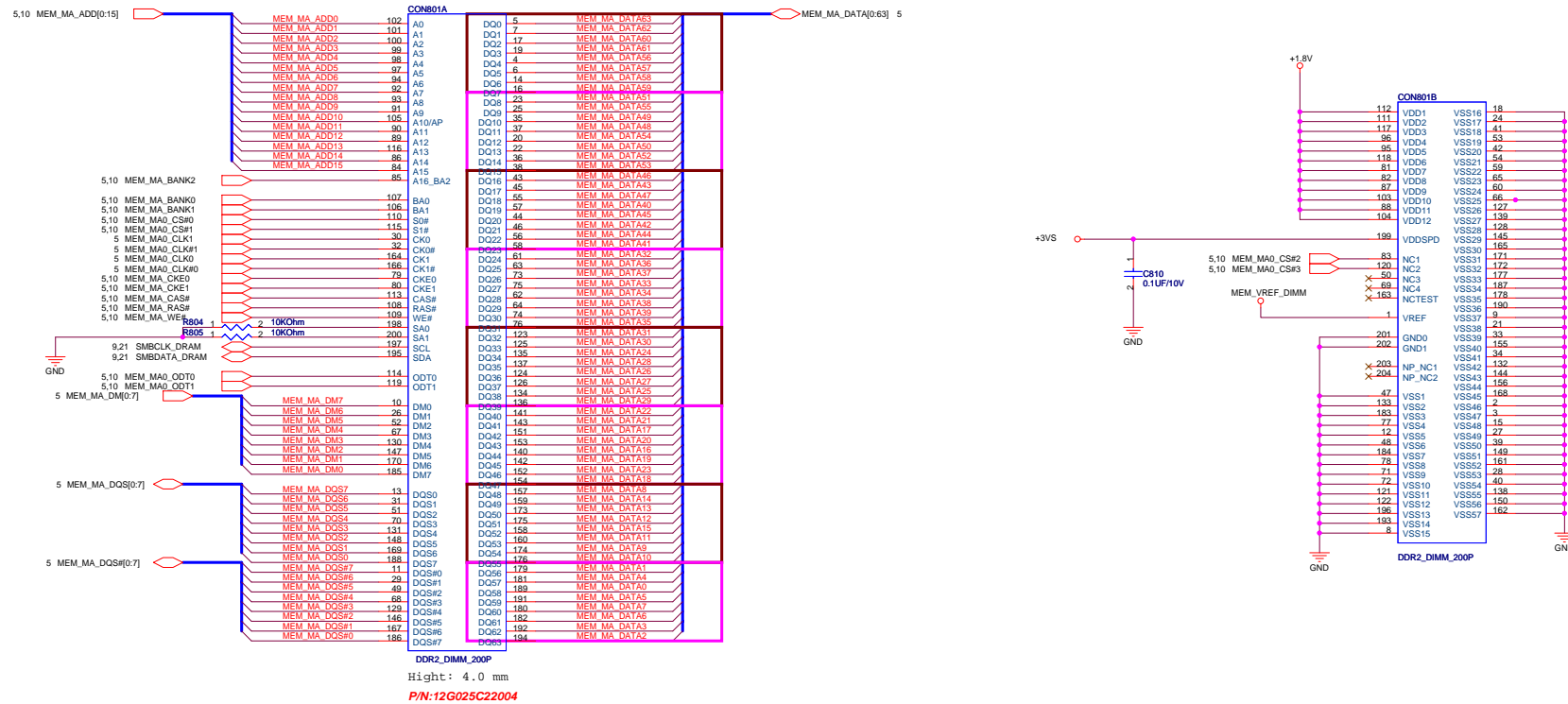


Enable: Turn OFF system
Slave address: 98h

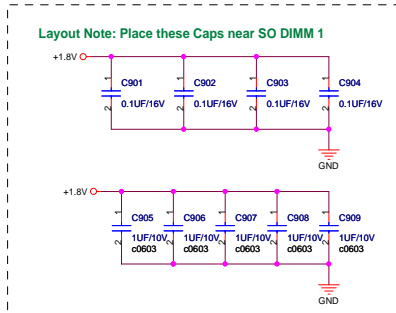
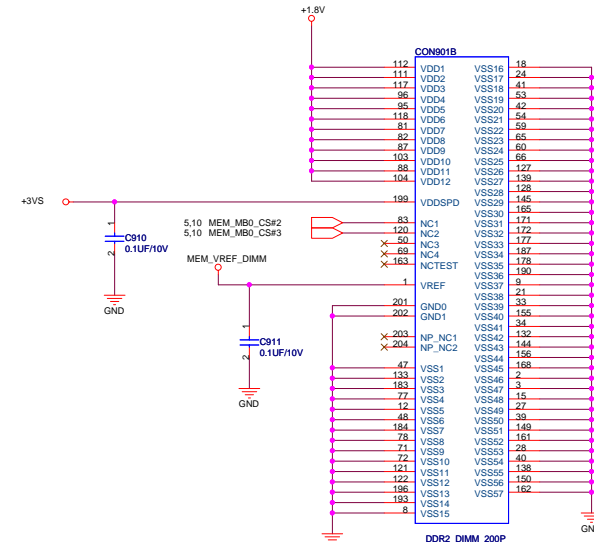
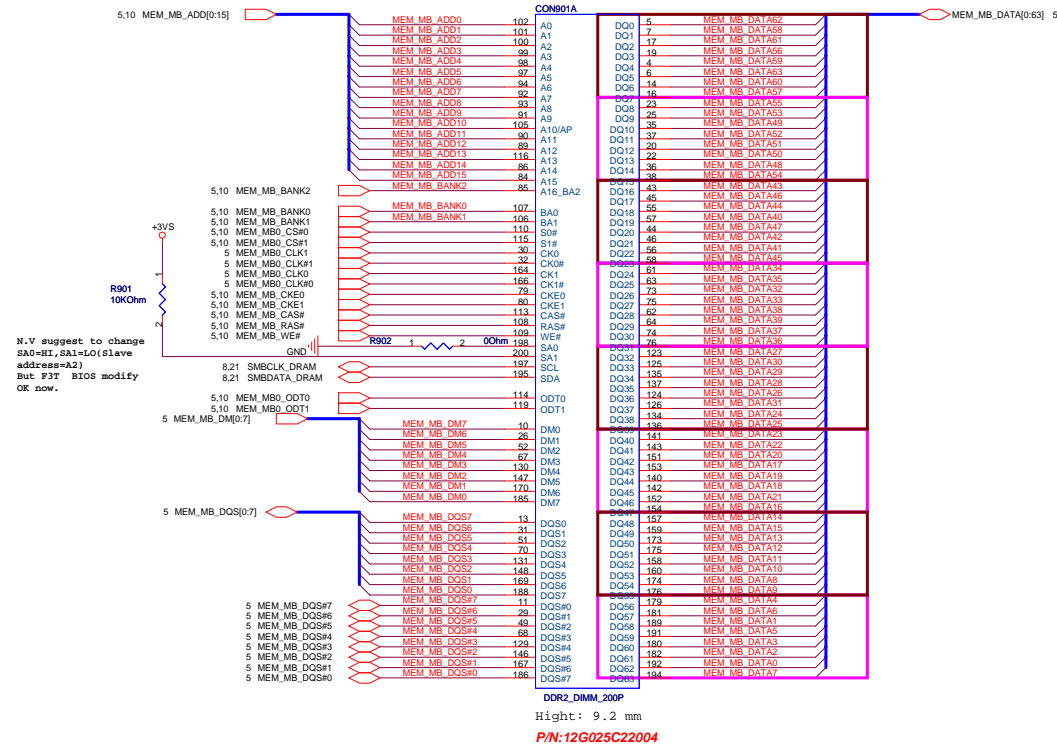
<Variant Name>

ASUS		Title : FAN_CTRL&Thermal	
ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size	Project Name		Rev
Custom	T13M		1.1
Date: Friday, September 08, 2006		Sheet	7 of 65

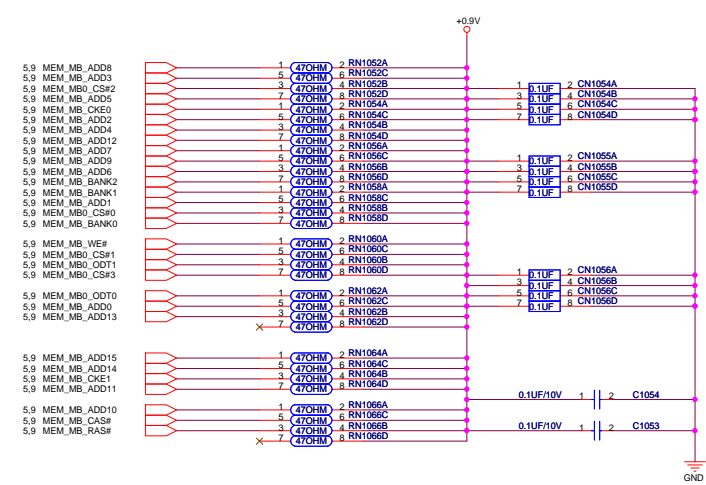
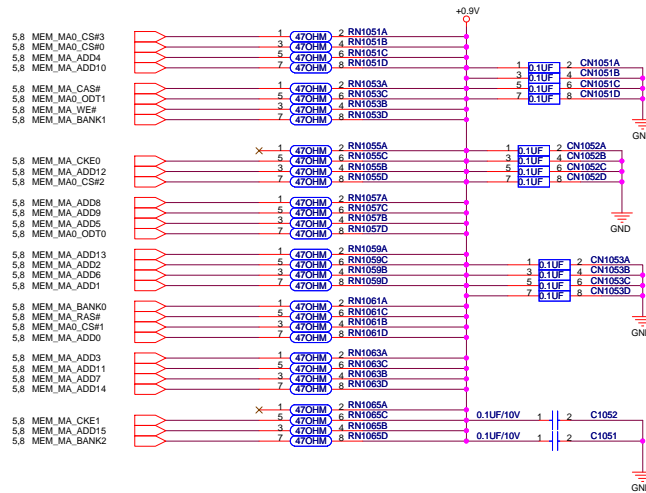
DDR2 DIMM 0

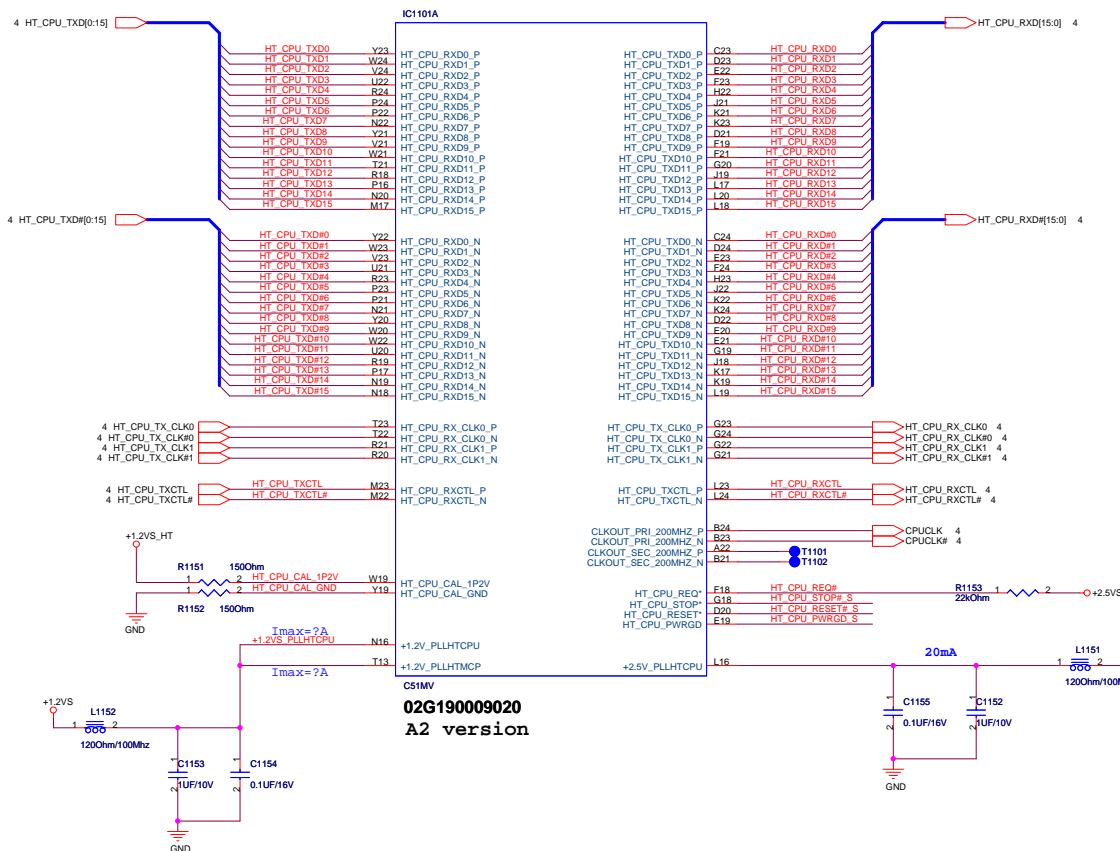


DDR2 DIMM 1

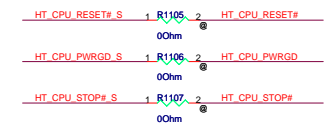
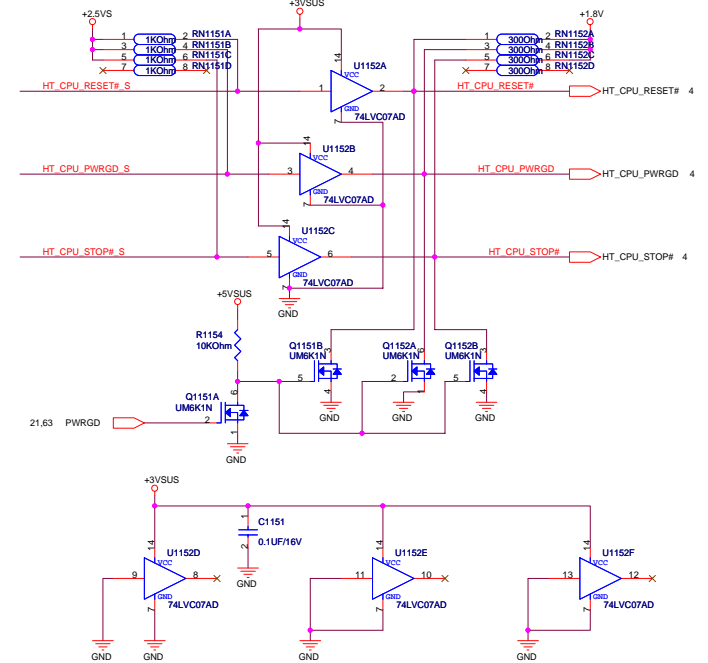


DIMM TERMINATION





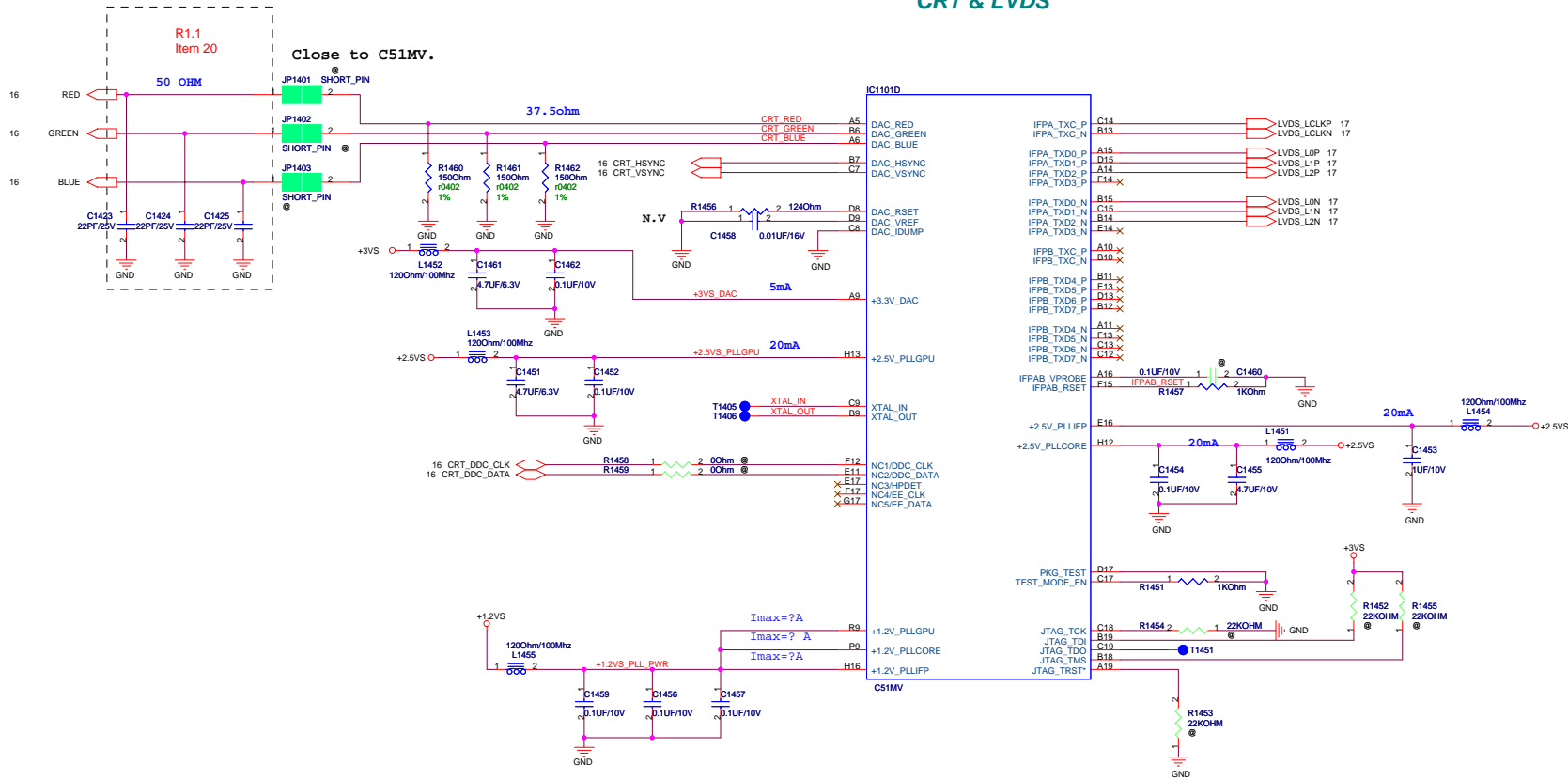
nVidia C51 Chipset side-band signal
glitch issue solution.

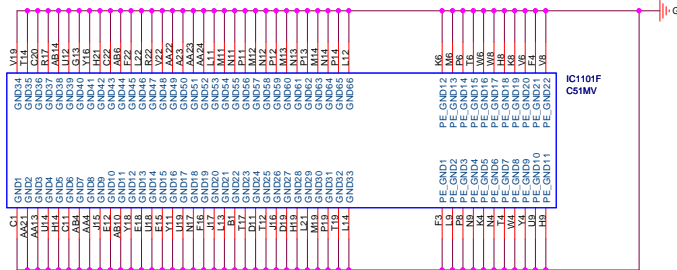
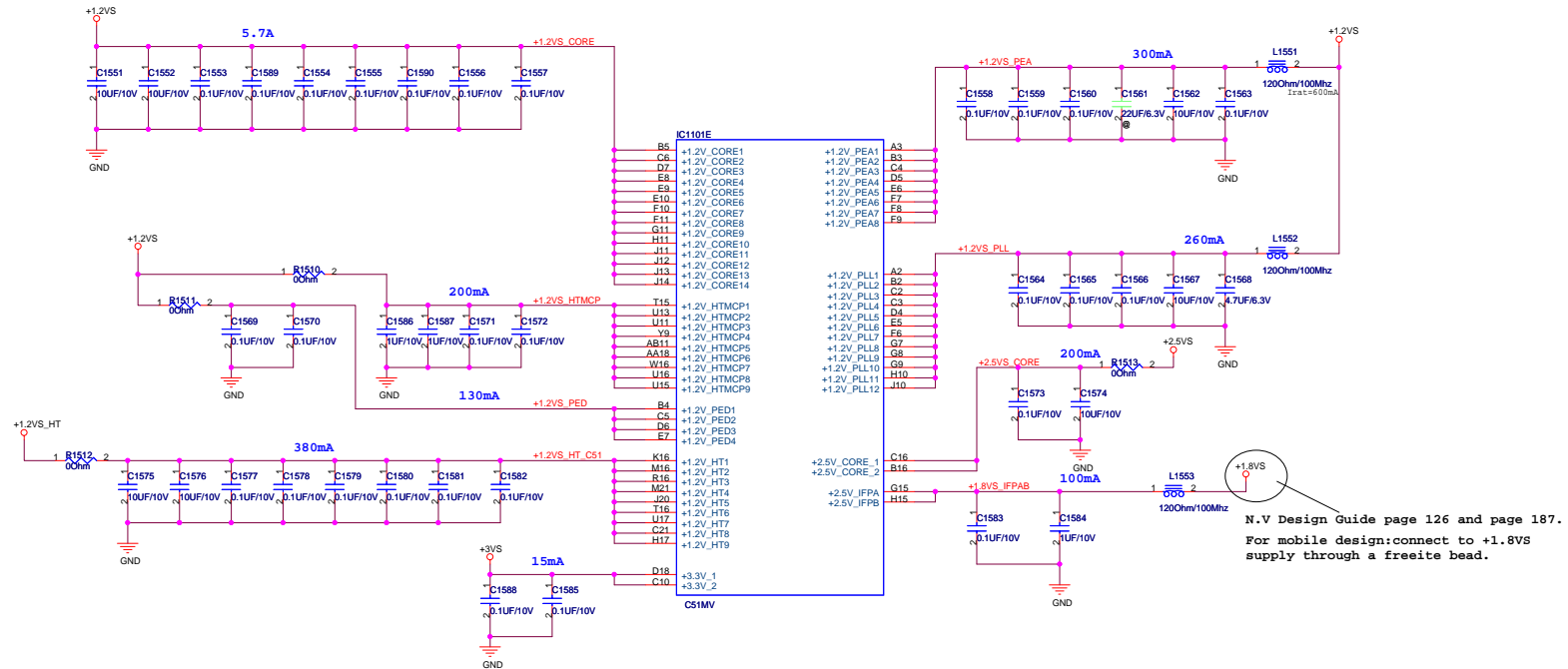


IC101C			
16	PE0_RX0_N, P	PE0_TX0, P	L1
18	PE0_RX1_N, P	PE0_TX1, P	L3
19	PE0_RX2_N, P	PE0_TX2, P	M
20	PE0_RX3_N, P	PE0_TX3, P	M
21	PE0_RX4_N, P	PE0_TX4, P	R1
22	PE0_RX5_N, P	PE0_TX5, P	R4
23	PE0_RX6_N, P	PE0_TX6, P	R4
24	PE0_RX7_N, P	PE0_TX7, P	R4
25	PE0_RX8_N, P	PE0_TX8, P	U1
26	PE0_RX9_N, P	PE0_TX9, P	V1
27	PE0_RX10_N, P	PE0_TX10, P	W3
28	PE0_RX11_N, P	PE0_TX11, P	AA1
29	PE0_RX12_N, P	PE0_TX12, P	AA1
30	PE0_RX13_N, P	PE0_TX13, P	AC1
31	PE0_RX14_N, P	PE0_TX14, P	AD2
32	PE0_RX15_N, P	PE0_TX15, N	
33			
34			
35			
36			
37	PE0_RX0_N, N	PE0_TX0, N	L2
38	PE0_RX1_N, N	PE0_TX1, N	M2
39	PE0_RX2_N, N	PE0_TX2, N	N2
40	PE0_RX3_N, N	PE0_TX3, N	R2
41	PE0_RX4_N, N	PE0_TX4, N	R3
42	PE0_RX5_N, N	PE0_TX5, N	T2
43	PE0_RX6_N, N	PE0_TX6, N	T2
44	PE0_RX7_N, N	PE0_TX7, N	U3
45	PE0_RX8_N, N	PE0_TX8, N	V2
46	PE0_RX9_N, N	PE0_TX9, N	V2
47	PE0_RX10_N, N	PE0_TX10, N	W2
48	PE0_RX11_N, N	PE0_TX11, N	X2
49	PE0_RX12_N, N	PE0_TX12, N	AA2
50	PE0_RX13_N, N	PE0_TX13, N	AB2
51	PE0_RX14_N, N	PE0_TX14, N	AC2
52	PE0_RX15_N, N	PE0_TX15, N	AD1
53			
54			
55			
56			
57	PE1_PRSNT*	PE0_REFCLK_P	K1
58		PE0_REFCLK_N	K2
59			
60	PE1_RX_P, P	PE1_T, P	G5
61	PE1_RX_N, N	PE1_TX_N, P	G6
62	PE1_PRSNT*	PE1_REFCLK_P	G3
63		PE1_REFCLK_N	G4
64			
65	PE2_RX_P, P	PE2_T, P	H3
66	PE2_RX_N, N	PE2_TX_N, P	H4
67	PE2_PRSNT*	PE2_REFCLK_P	H3
68		PE2_REFCLK_N	
69			
70			
71	PE1_CLKREQ*/CLK	PE_TSTCLK_P	F1
72	PE2_CLKREQ*/DATA	PE_TSTCLK_N	F2
73			
74			
75	PE_REFCLKIN_P	PE_RESET*	G1
76	PE_REFCLKIN_N		
77			
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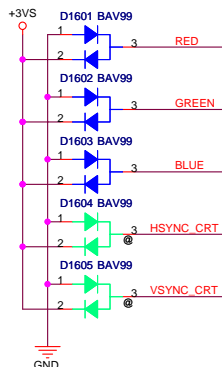
CRT & LVDS



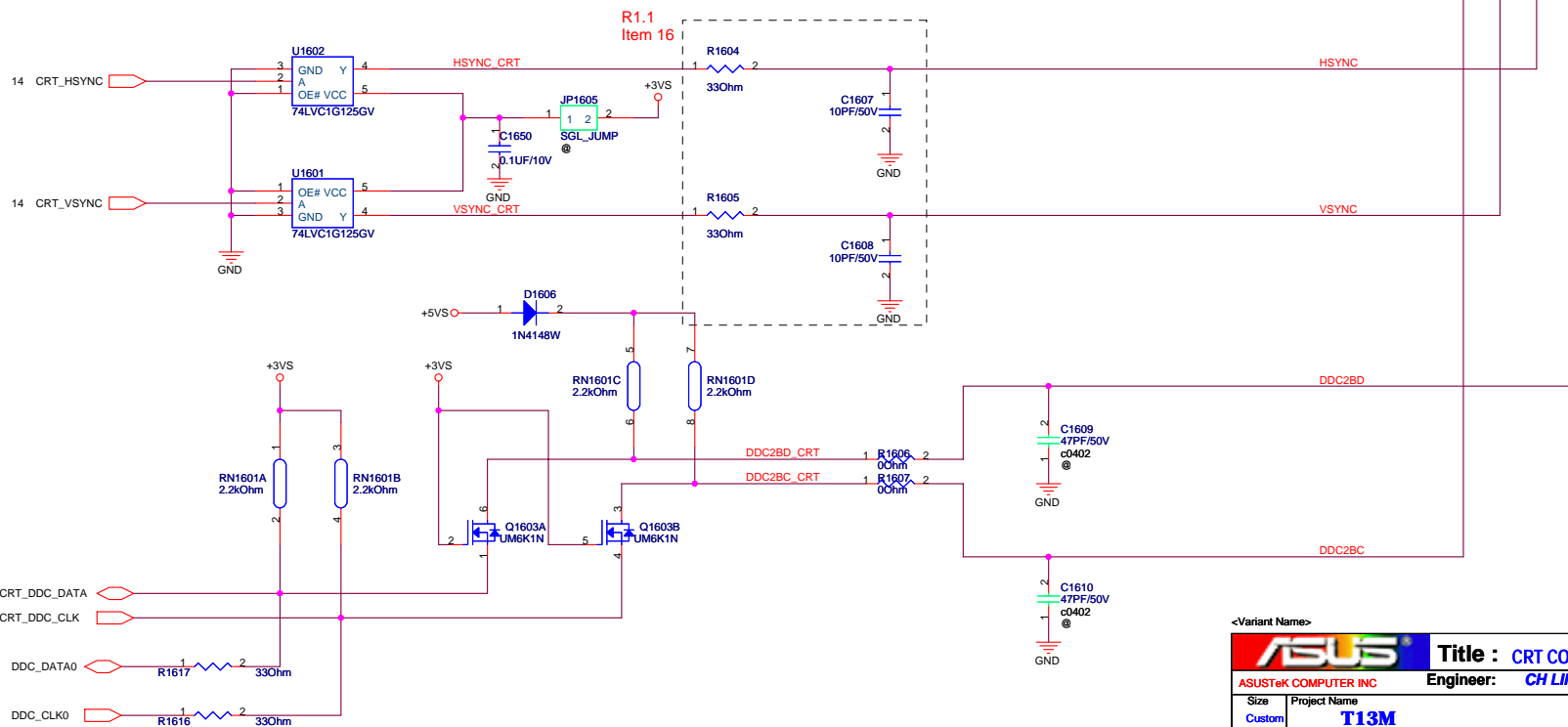
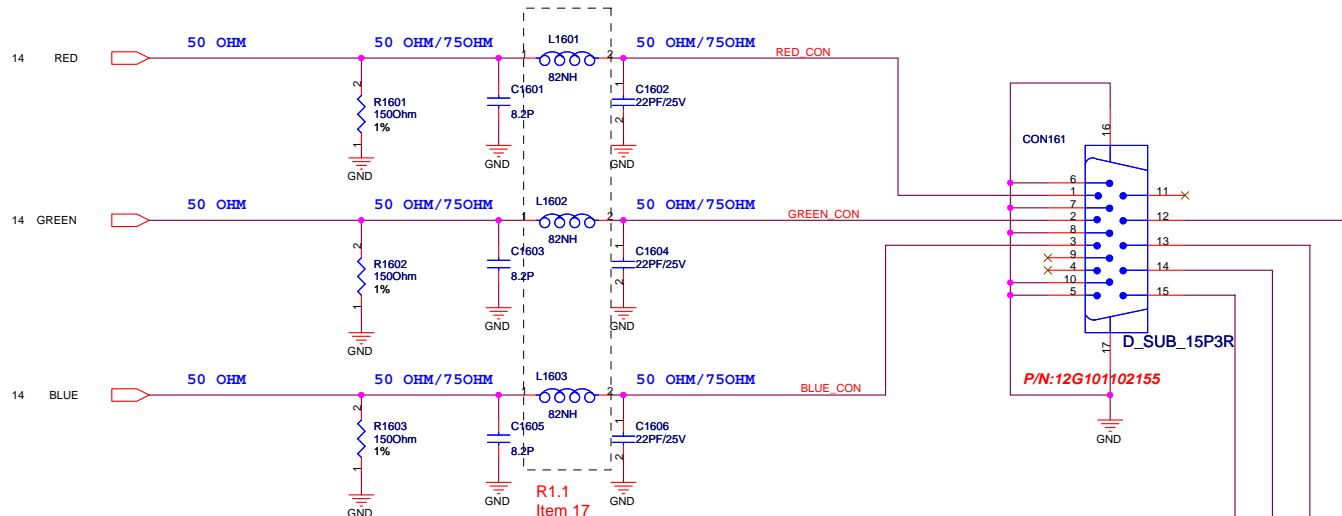


CRT

PLACE NEAR CON161.

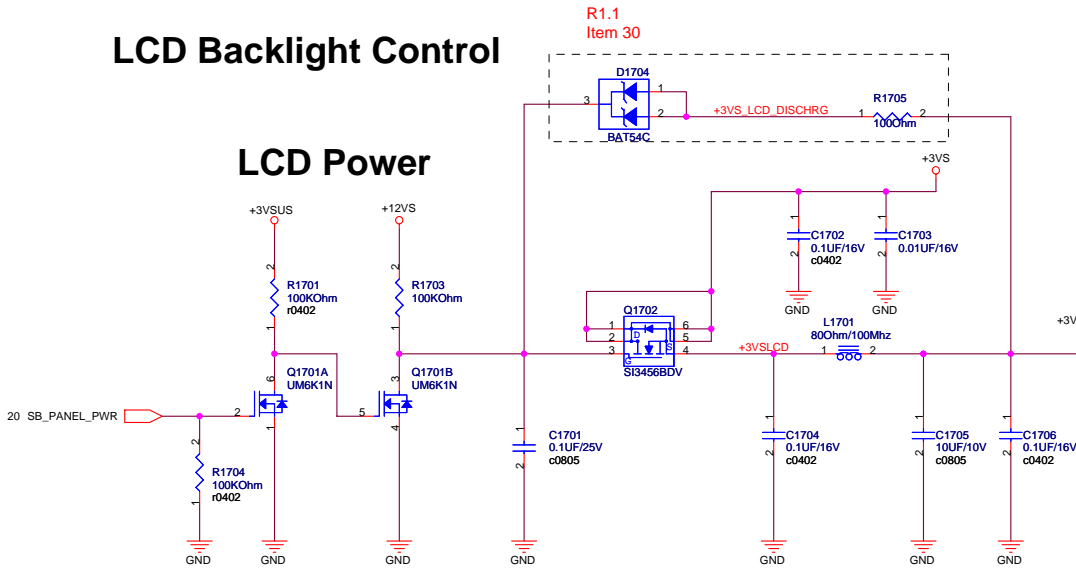


Close to CON161



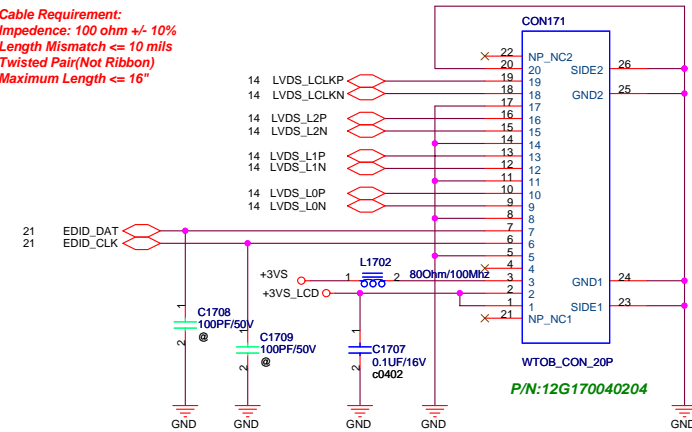
LCD Backlight Control

LCD Power

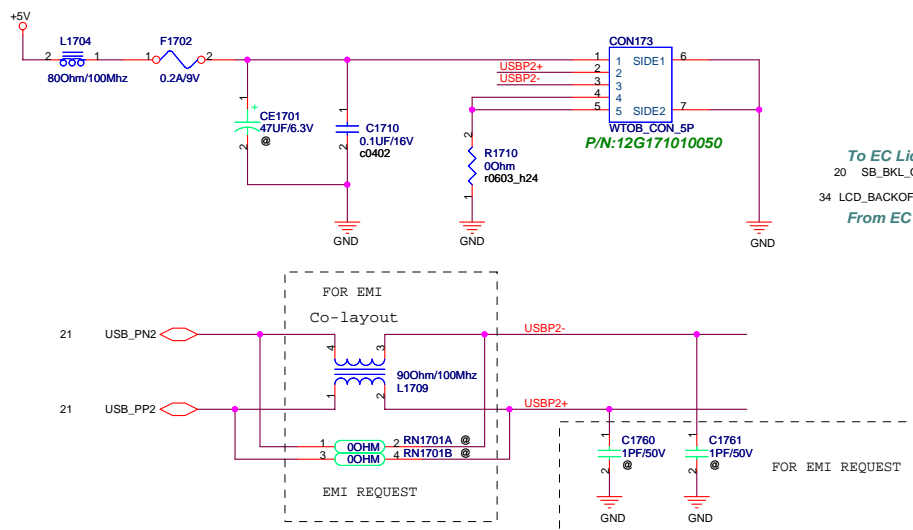


LCD LVDS Interface

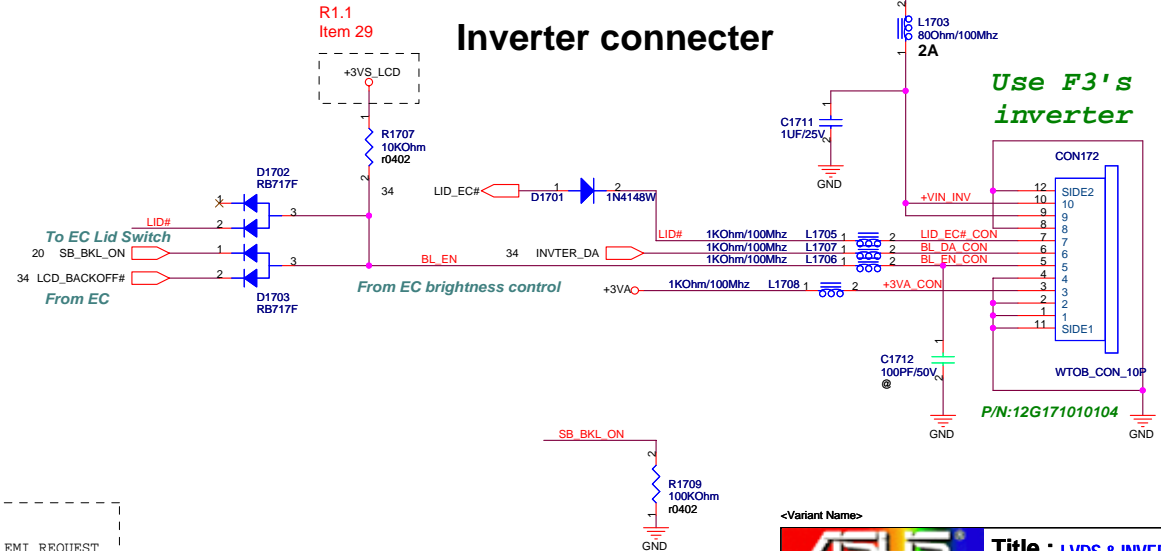
Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"



CCD connector

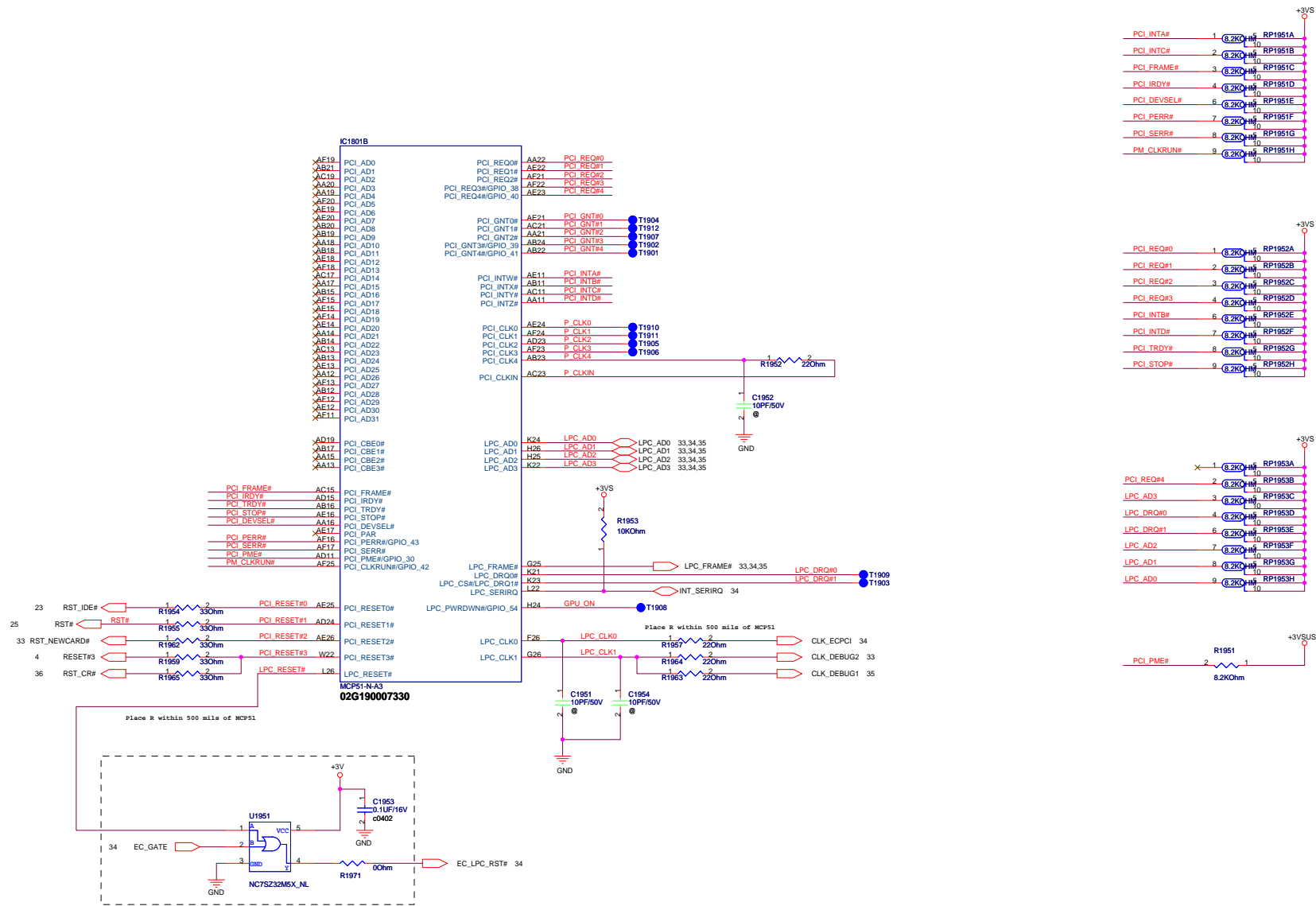


Inverter connector



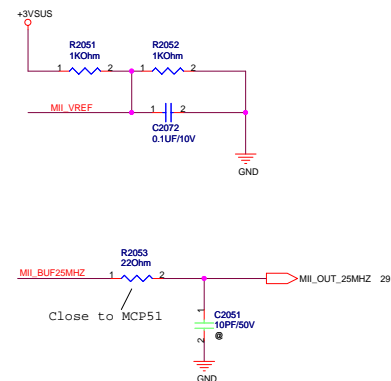
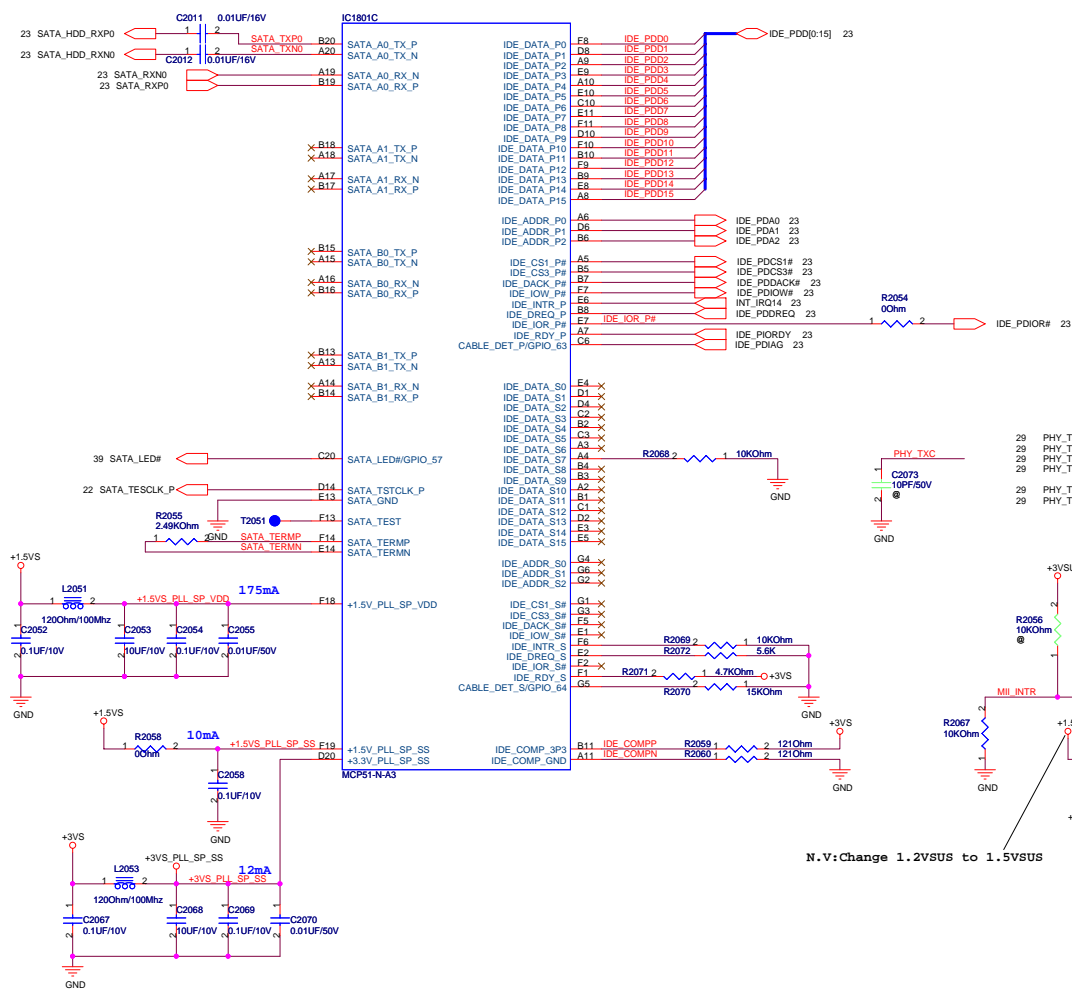
<Variant Name>

ASUS		Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size	Project Name	Rev	
Custom	T13M	1.1	
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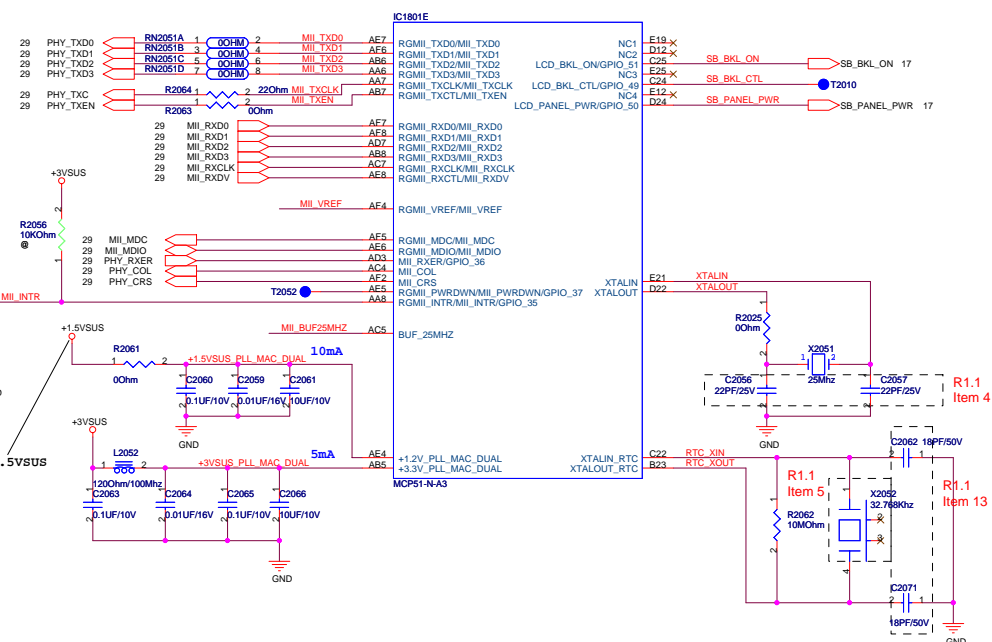


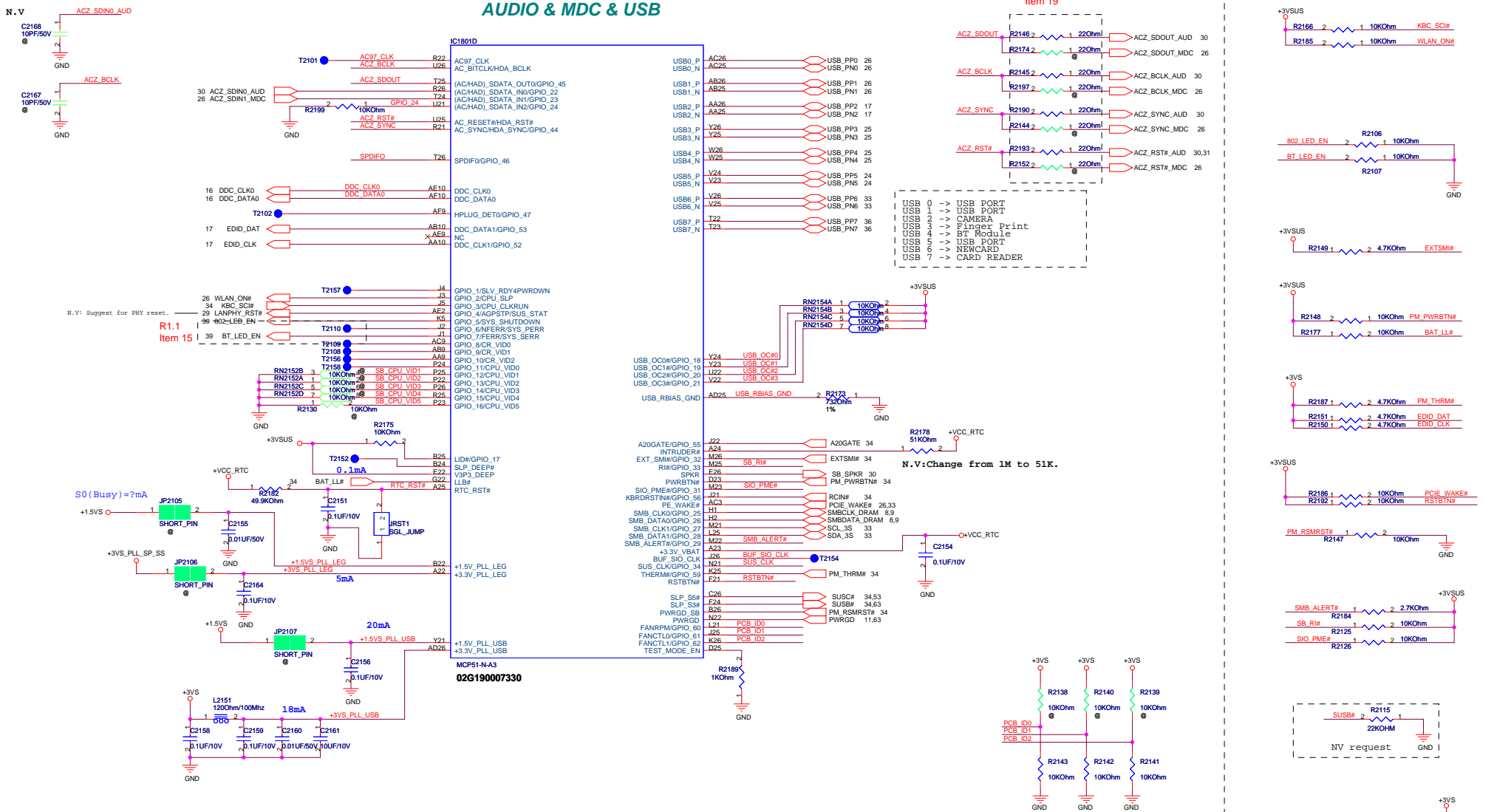
R1.1
Item 18

SATA & ODD



PHY



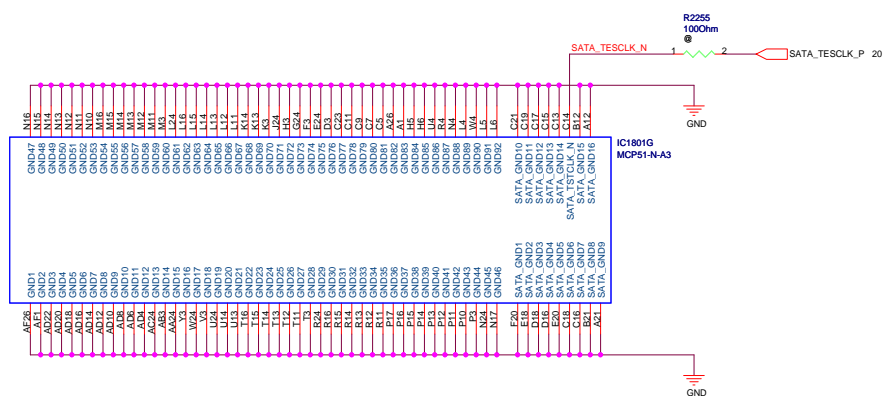


ACZ_RST# select	
0	MII(10/100M) *
1	RGMII(1000/100/10M)

BUFSIO_CLK select	
0	14.31818 MHz *
1	24 MHz

MCP51 master/slave mode	
0	normal *
1	slave mode

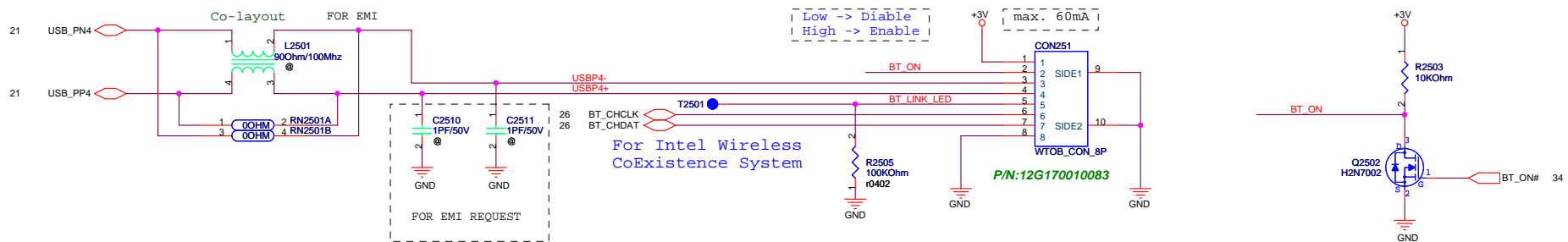
Boot mode select	
0	User Mode *
1	Safe Mode



The schematic diagram illustrates the PATA ODD CON connector and its associated components. It includes the following details:

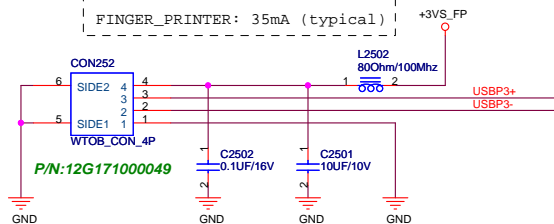
- Top Left:** A circuit involving a +3VS supply, a 330 Ohm resistor (R2302), a 10K Ohm resistor (R2305), a 0 Ohm resistor (R2301), and a component labeled Q2301 PMBS3904. It also shows a 0 Ohm resistor (R1.1 Item 7) and a connection to RST_IDE#.
- Bottom Left:** A circuit with a +3VS supply, a 4.7K Ohm resistor (R2304), a 5.6K resistor (R2373), and 10K Ohm resistors (R2308, R2302, R2314) connected to IDE_PIORDY, IDE_PDDREQ, IDE_PDD7, INT_IRQ14, and IDE_PDIAF.
- Center:** A detailed view of the CON232 connector. It shows connections for IDE_PDIOW#, IDE_PDIORDY, IDE_PDIOR#, IDE_PDIACK#, IDE_PDIAF, IDE_PDA2, IDE_PDCS3#, IDE_PDD1, IDE_PDD2, IDE_PDD3, IDE_PDD4, IDE_PDD5, IDE_PDD6, IDE_PDD7, IDE_PDD8, IDE_PDD9, IDE_PDD10, IDE_PDD11, IDE_PDD12, IDE_PDD13, IDE_PDD14, and IDE_PDD15. It also shows a connection to IDE_PDD[15:0] and IDE_PDD[15:0].
- Bottom Center:** A circuit with a +5VS supply, a 1.5A current source, and capacitors C2308 (0.1UF/16V), C2309 (0.1UF/16V), C2312 (10UF/10V), and C2314 (22UF/10V). It also shows a connection to IDE_PDDREQ and IDE_PDIOR#.
- Right Side:** A circuit with a +5VS supply, a 1.5A current source, and capacitors C2308 (0.1UF/16V), C2309 (0.1UF/16V), C2312 (10UF/10V), and C2314 (22UF/10V). It also shows a connection to IDE_PDDREQ and IDE_PDIOR#.
- Bottom Right:** A circuit with a +5VS supply, a 1.5A current source, and capacitors C2308 (0.1UF/16V), C2309 (0.1UF/16V), C2312 (10UF/10V), and C2314 (22UF/10V). It also shows a connection to IDE_PDDREQ and IDE_PDIOR#.

		Title : HDD & ODD	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size Custom	Project Name T13M		Rev 1.1
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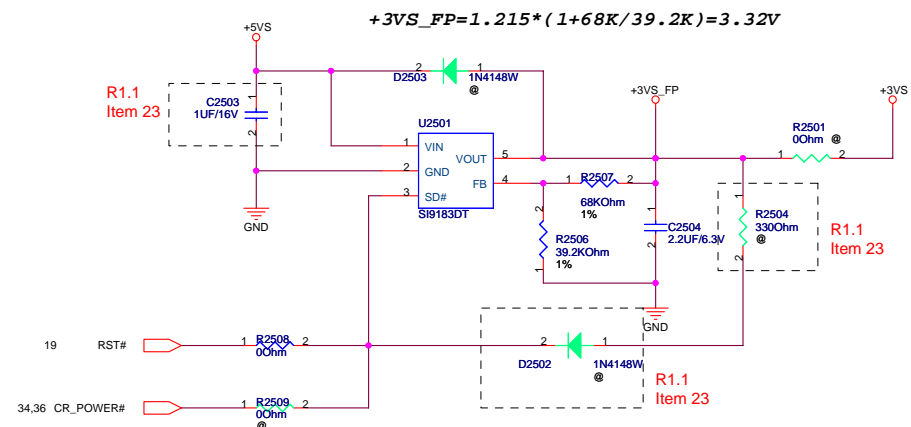
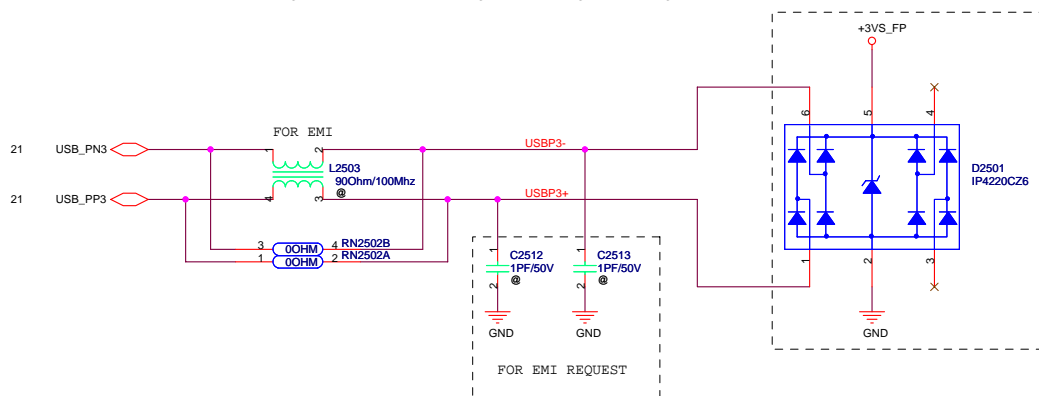


Finger Printer

FINGER_PRINTER: 35mA (typical)



R1.1
Item 28



<Variant Name>

ASUS		Title : BT & FP	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size Custom	Project Name T13M	Rev 1.1	
Date: Friday, September 08, 2006		Sheet 25 of 65	

POWER CONSUMPTION:

+3VS: +3.003V~+3.597V

Max= 750 mA

+1.5VS:+1.425V~+1.575V

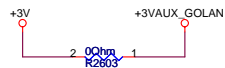
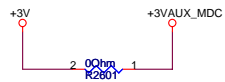
Max= 375 mA

+3VAUX_GOLAN:+3.003V~+3.597V

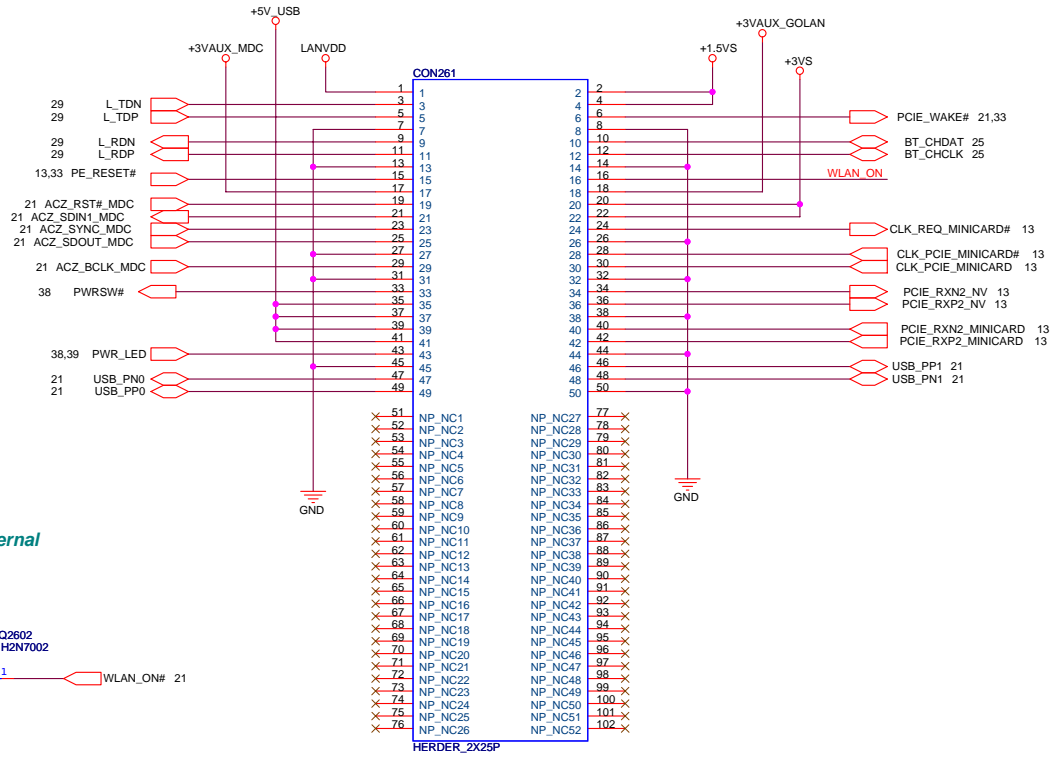
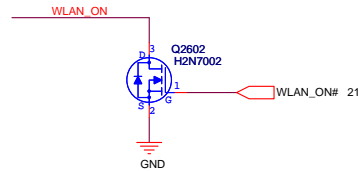
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V

Max= 300 mA



**Intel SPEC(18780):Internal
Pull UP 110Kohm**

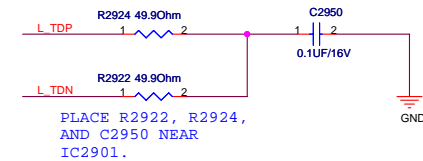
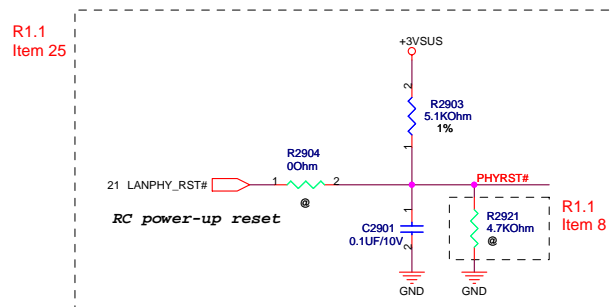
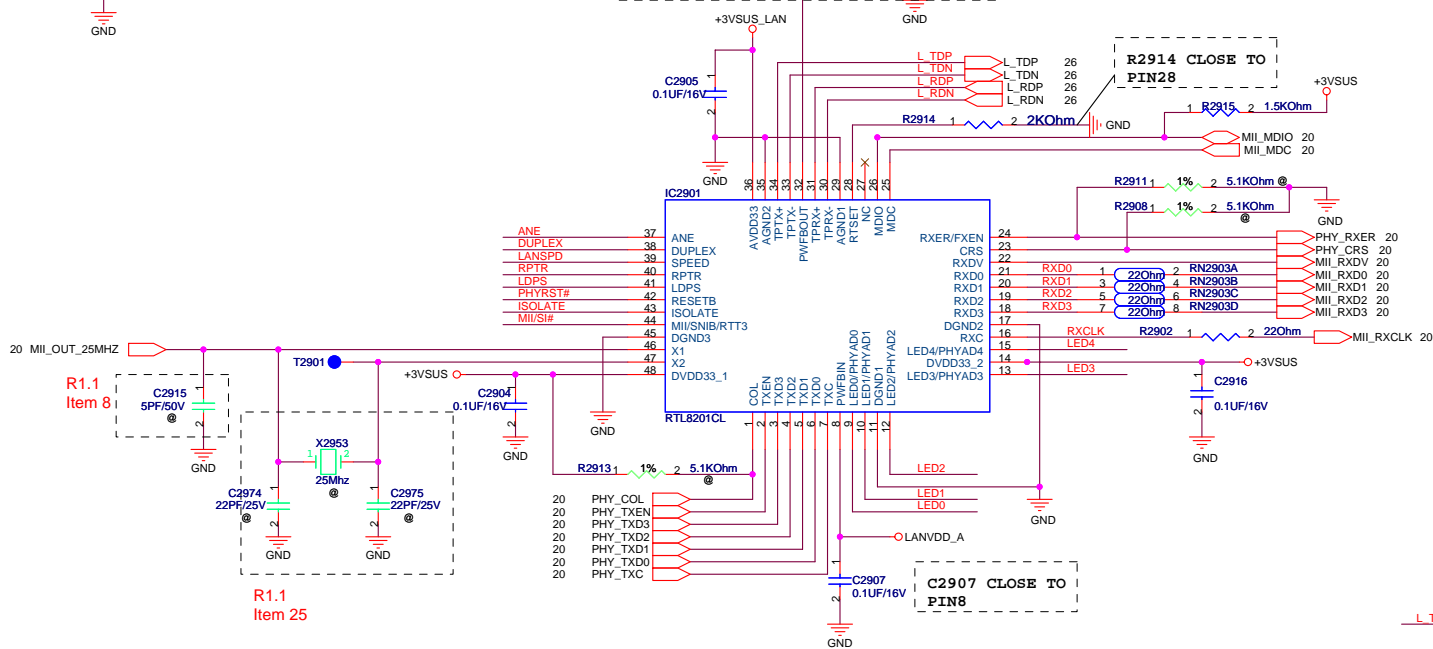
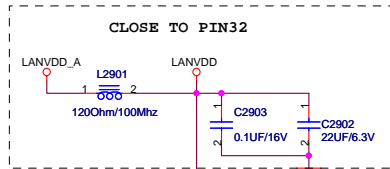
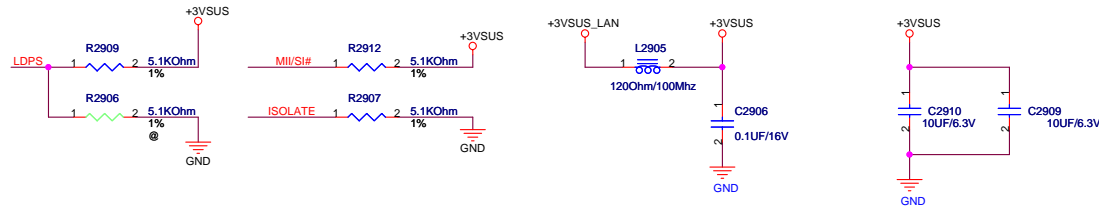
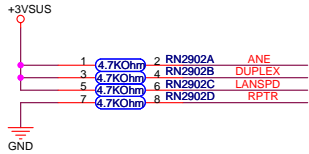
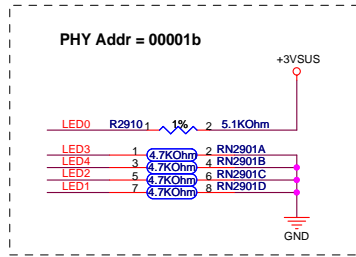


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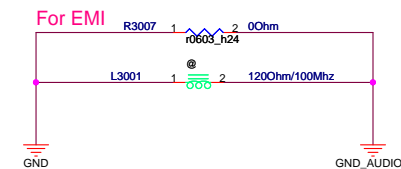
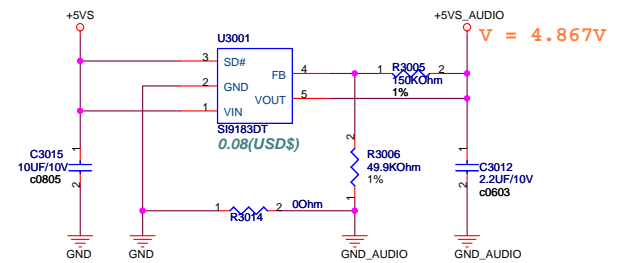
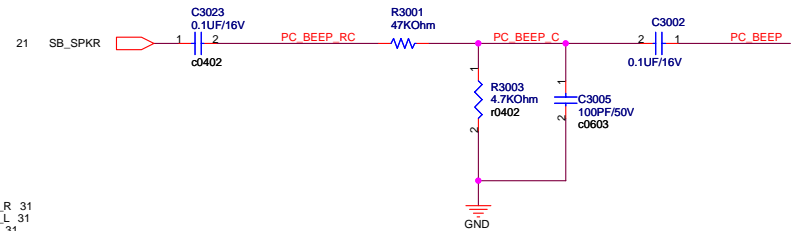
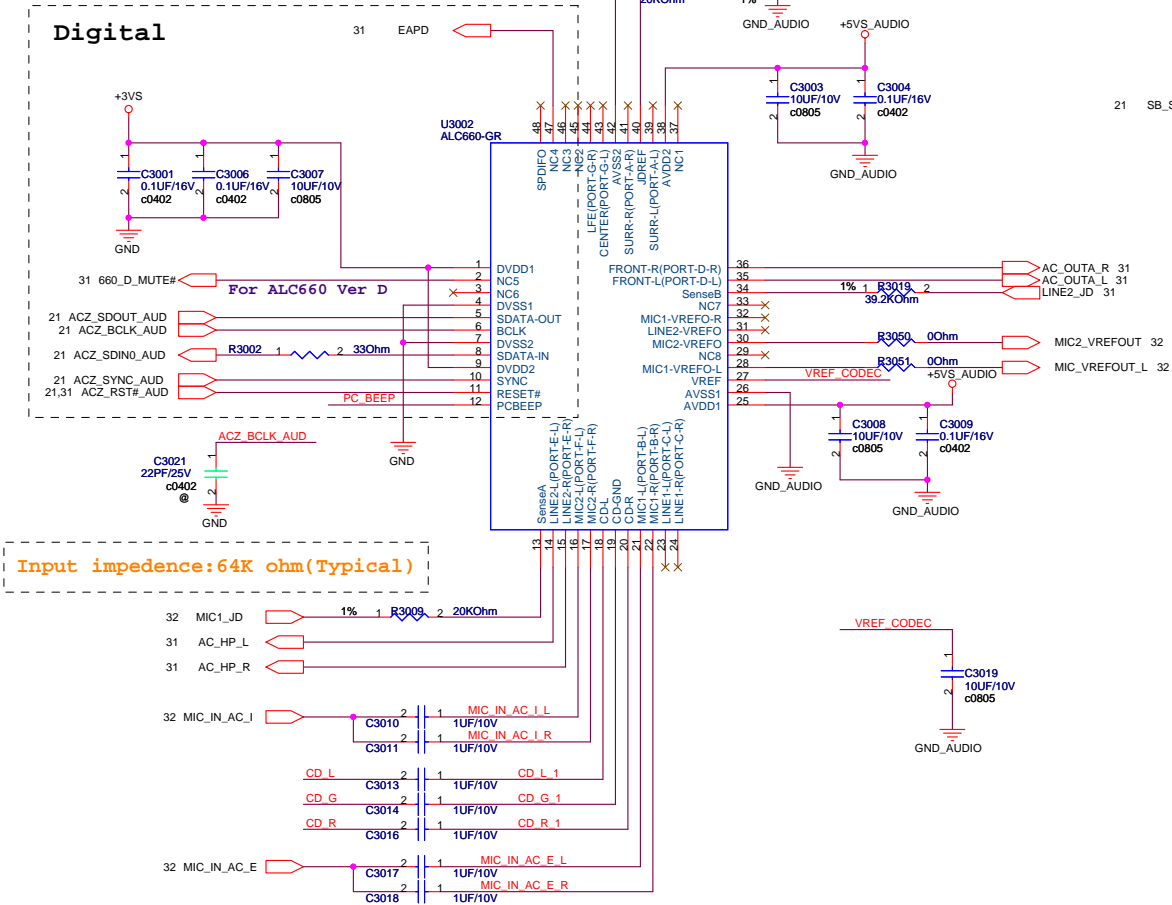
ASUS		Title : B TO B CONN(M)	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size	Project Name	Rev	
Custom	T13M	1.1	
Date: Friday, September 08, 2006		Sheet	26 of 65

PHY



CODEC

Digital

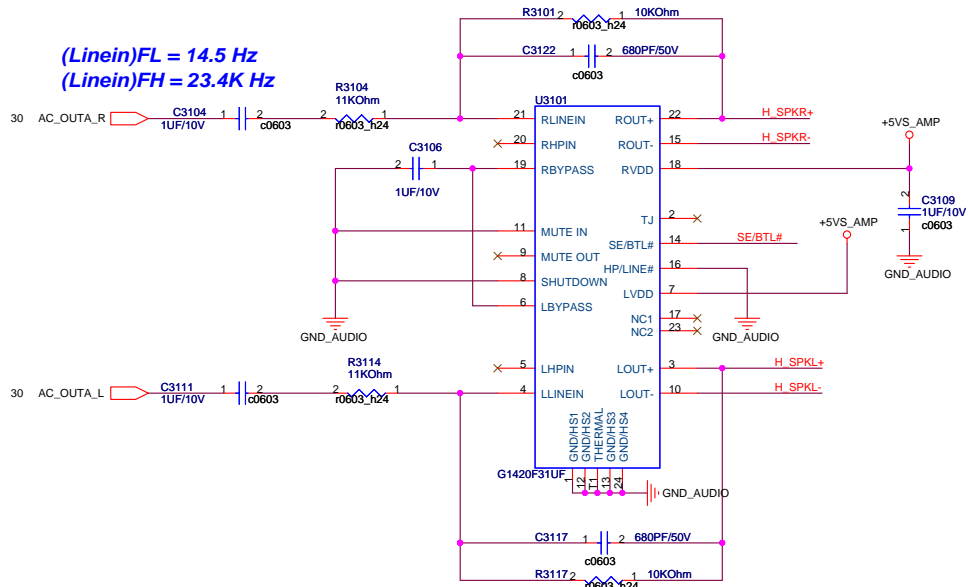


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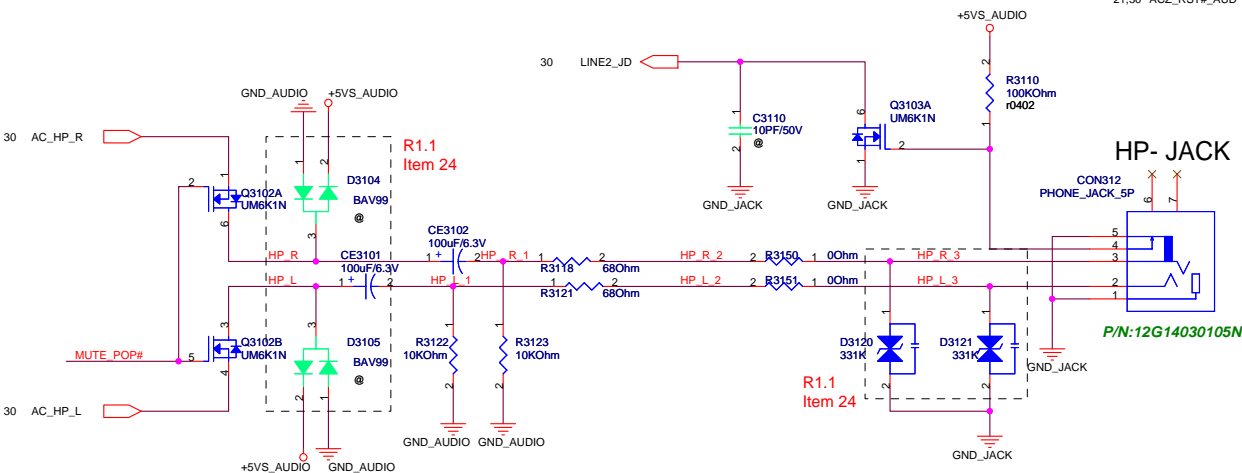
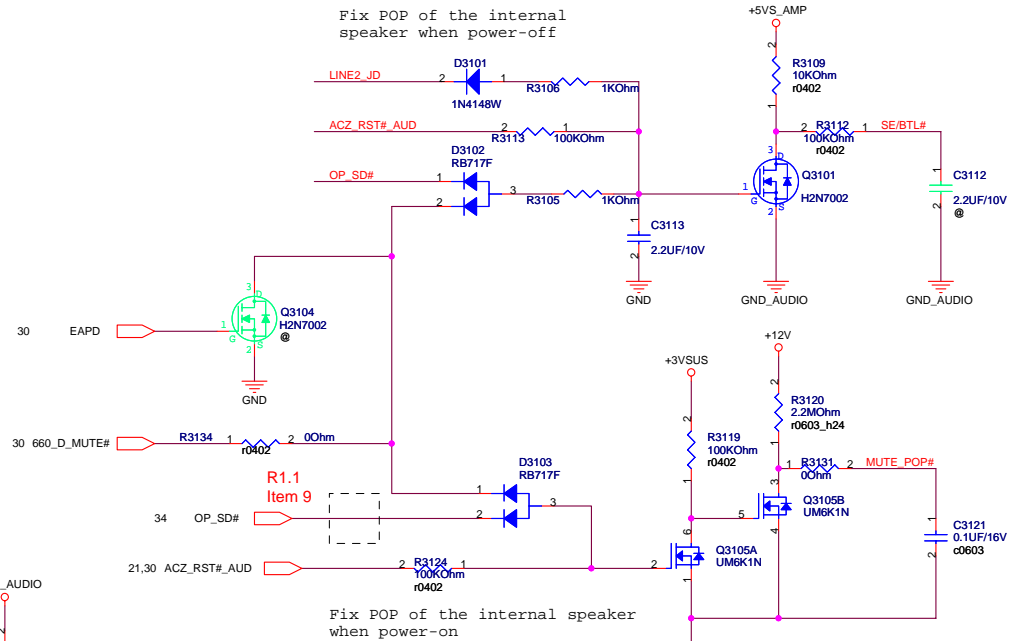
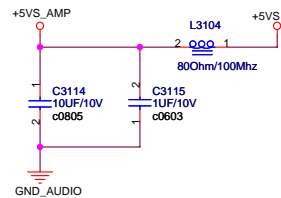
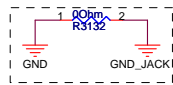
ASUS		Title : ALC660-GR	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size	Project Name	Rev	
Custom	T13M	1.1	
Date: Friday, September 08, 2006		Sheet	30 of 65

SPEAKER AMP

(Linein)FL = 14.5 Hz
(Linein)FH = 23.4K Hz



EMI Request



HP- JACK

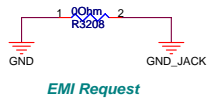
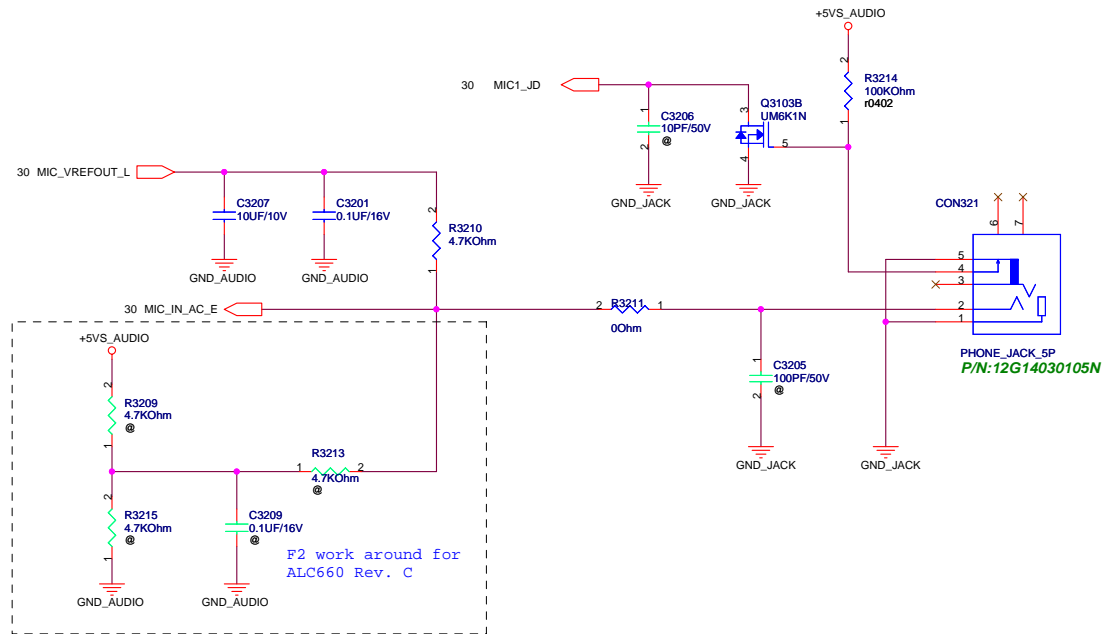
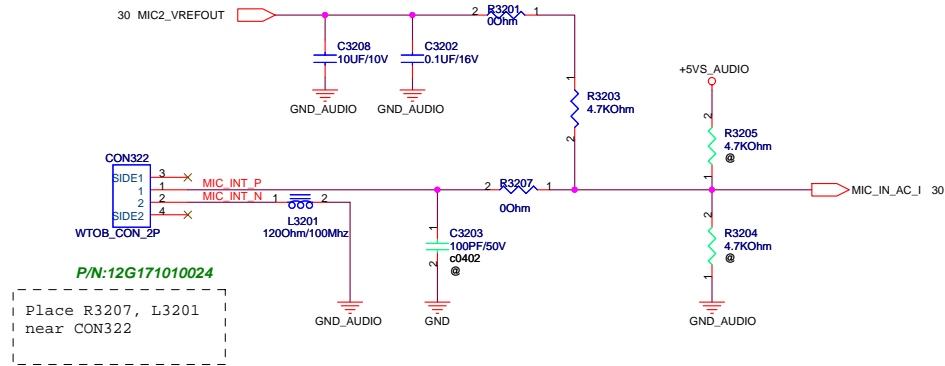
ON312
JACK_5P

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<Variant Name>

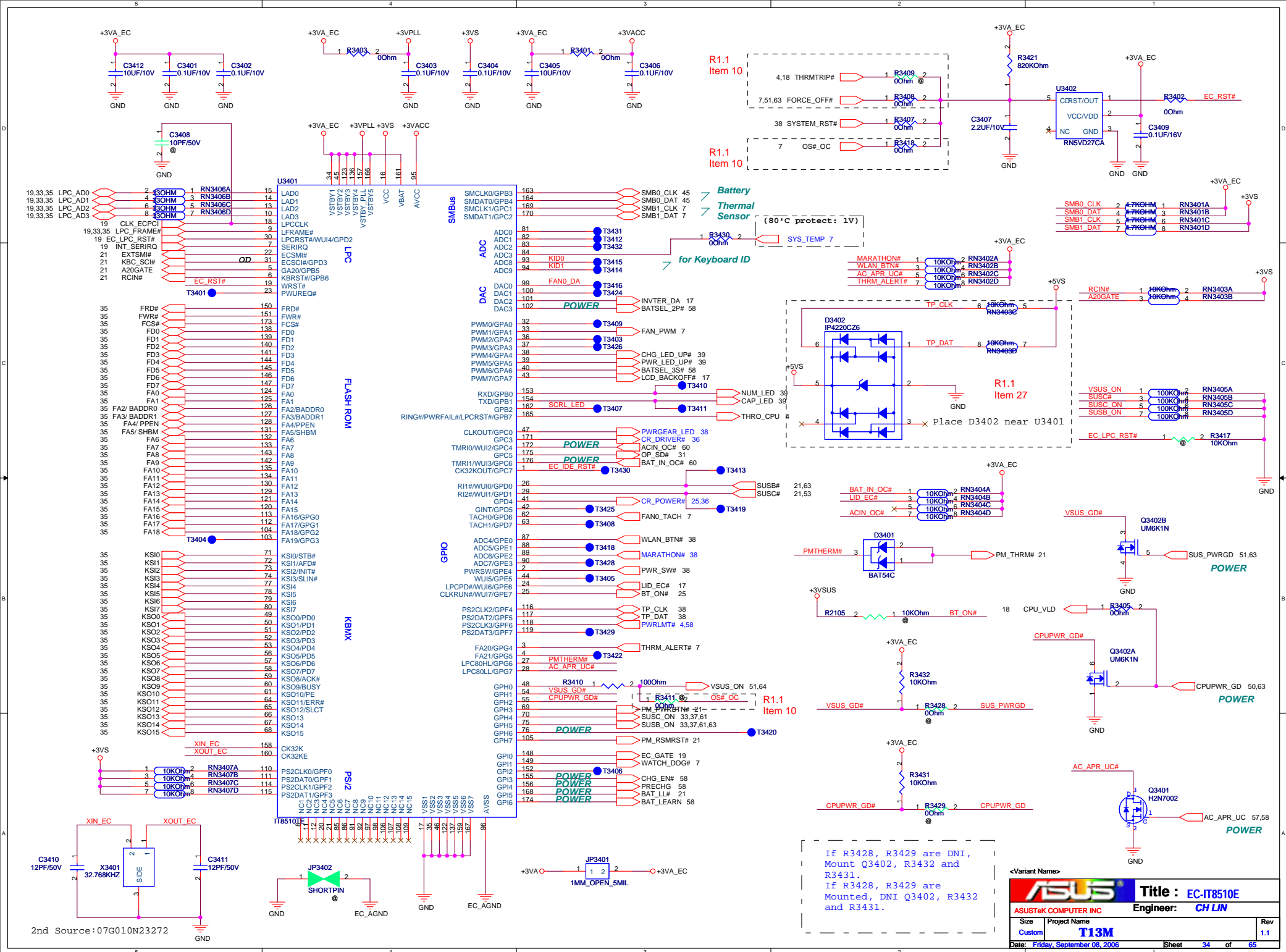


MIC



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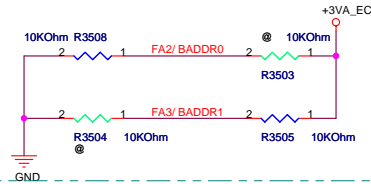
ASUS		Title : MICROPHONE	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size	Project Name	Rev	
Custom	T13M	1.1	
Date: Friday, September 08, 2006		Sheet	32 of 65



EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

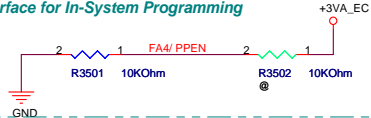
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved



Note: Sampled at VSTBY Power Up Reset

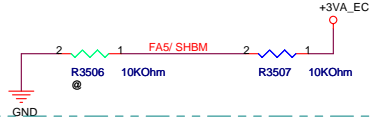
FA4/ PPEN

- 0: Normal
 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

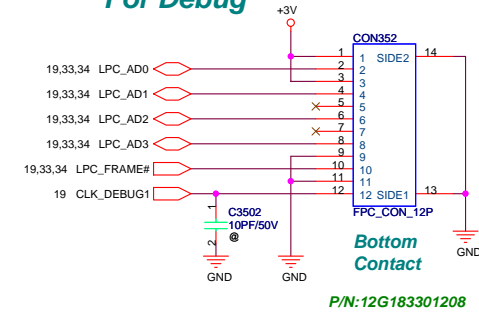


FA5/ SHBM

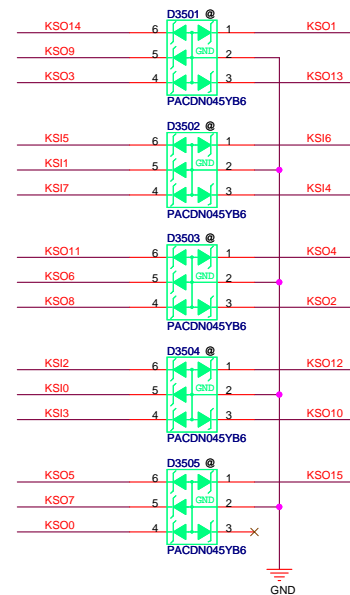
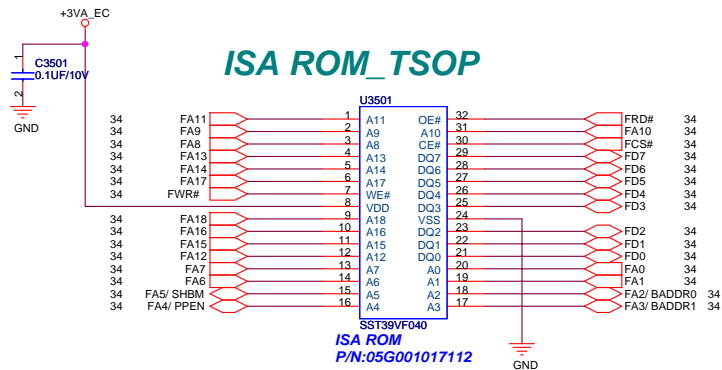
- 0: Disable Shared Memory with Host BIOS
 1: Enable Shared Memory with Host BIOS



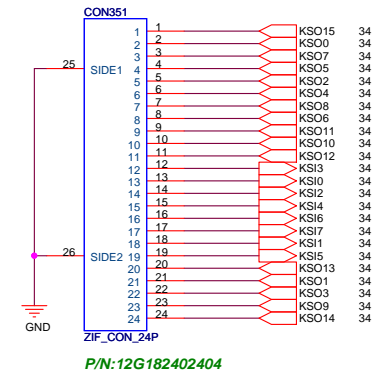
For Debug



ISA ROM_TSOP



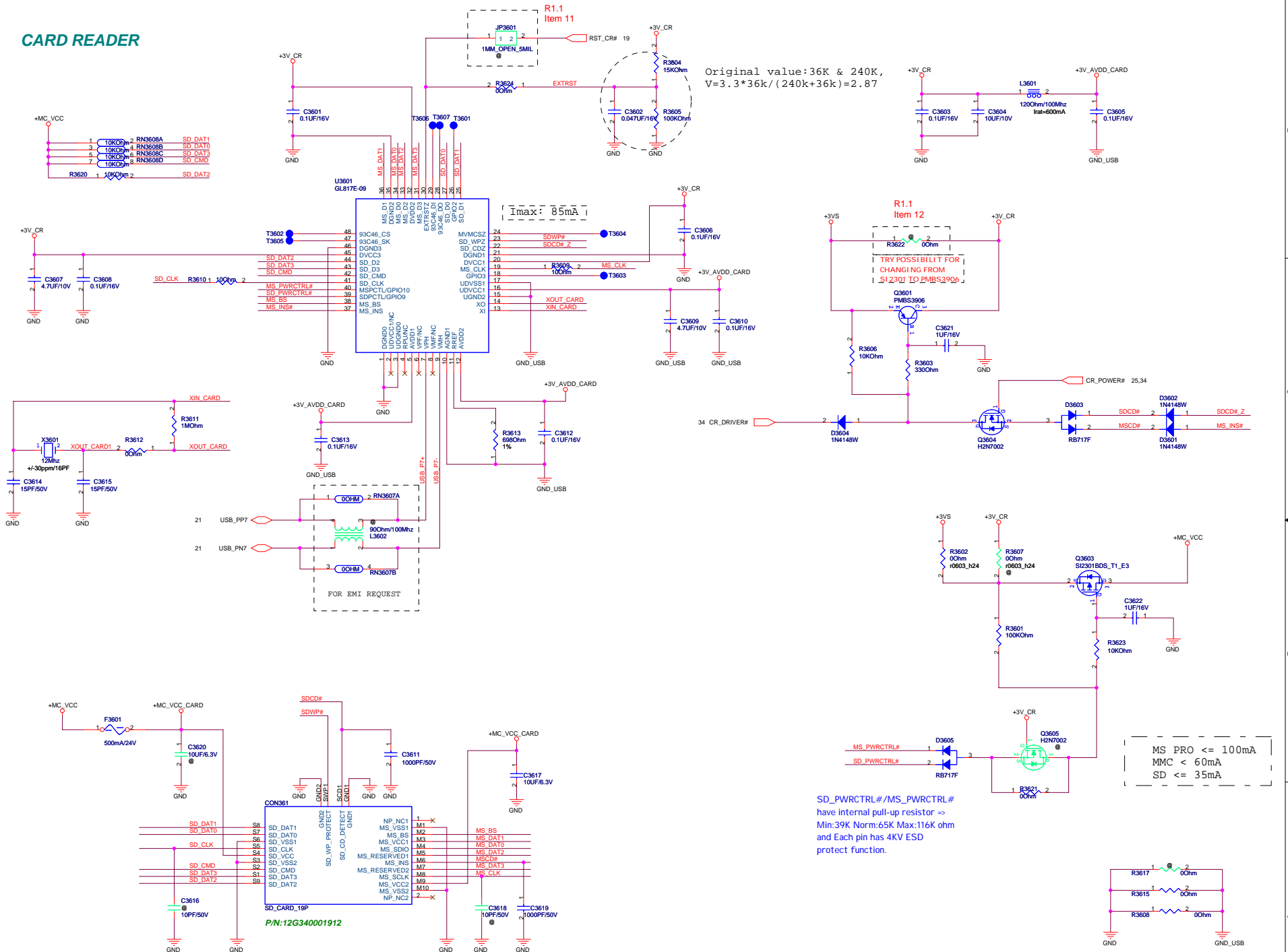
For Keyboard

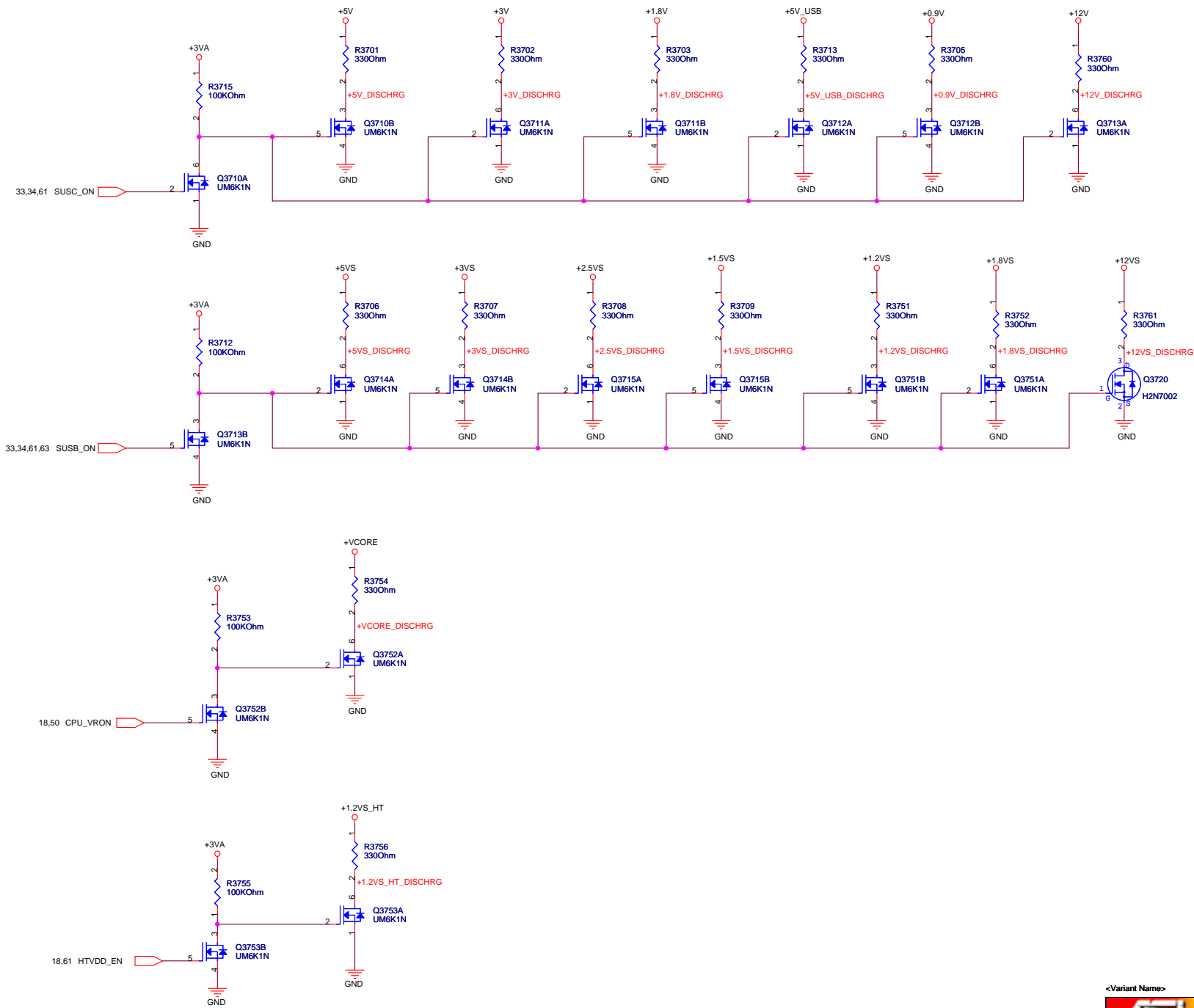


<Variant Name>

ASUS		Title : ISA_ROM&KB conn	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size	Project Name	Rev	
Custom	T13M	1.1	
Date: Friday, September 08, 2006	Sheet 35 of 65		

CARD READER

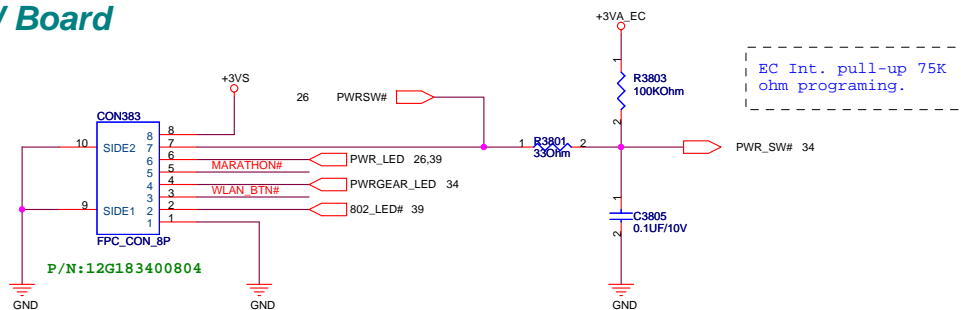
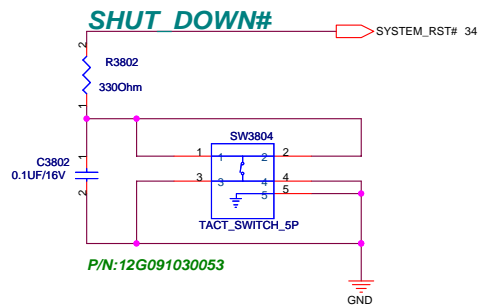




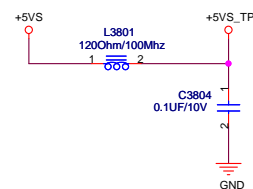
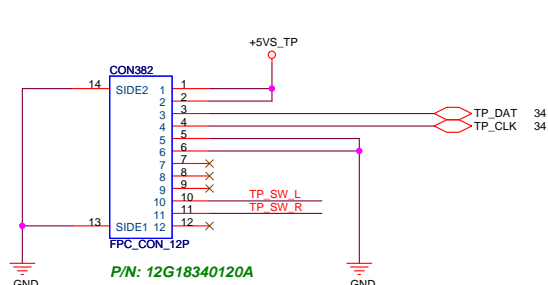
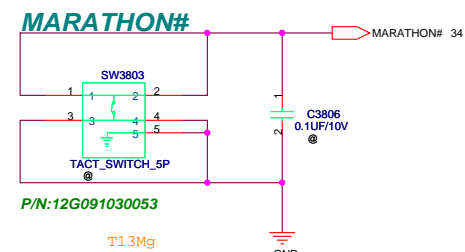
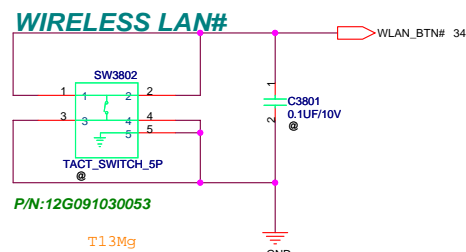
<Variant Name>

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: CH_LIN	
Size	Project Name	T13M	Rev 1.1
Custom			
Date: Friday, September 08, 2006		Sheet	37 of 65

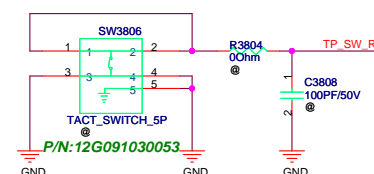
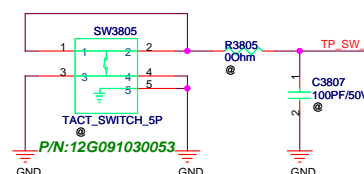
FFC CONNECTER for T13Mv SW Board



INSTANT KEY



Select Button for T13Mg

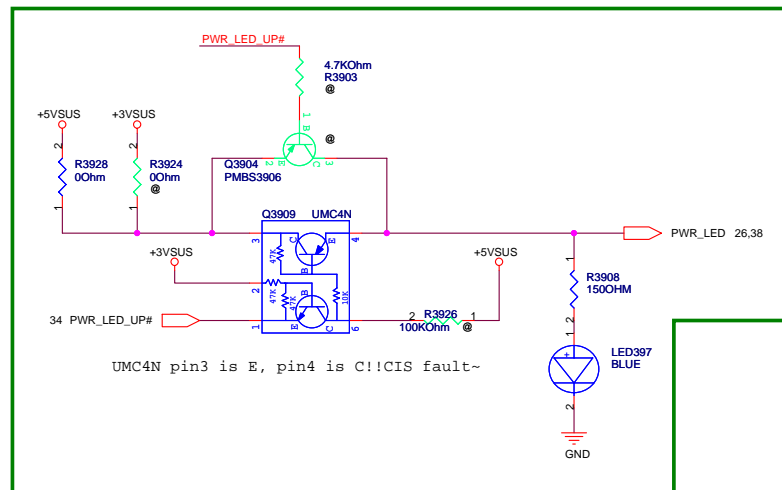


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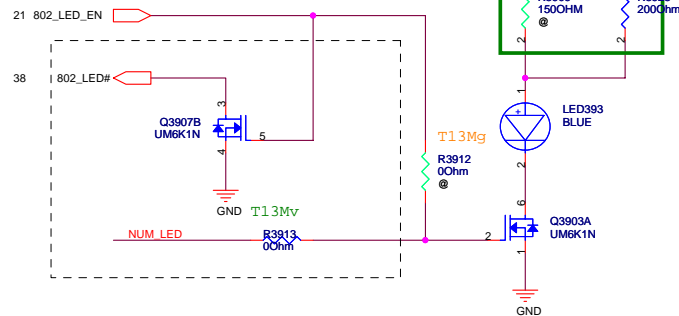
ASUS		Title : Key & FFC CONN	
ASUSTek COMPUTER INC		Engineer: CH LIN	
Size Custom	Project Name T13M	Rev 1.1	
Date: Friday, September 08, 2006	Sheet	38	of 65

For T13Fg: Change LED397, LED393, LED394, LED391, LED395, LED396 to 07G015700771 *Green
,change R3908 to 10G213101003010 *100 ohm, and change LED392 to 07G015700294* Orange.
Mount R3924, R3903, Q3904, Q3902, R3902, R3905, R3906, R3912, R3909, R3918, R3907, R3915,
R3910
DNI R3928, Q3909, R3923, R3913, Q3908, R3919, R3921, R3917, R3922, R3920, R3916

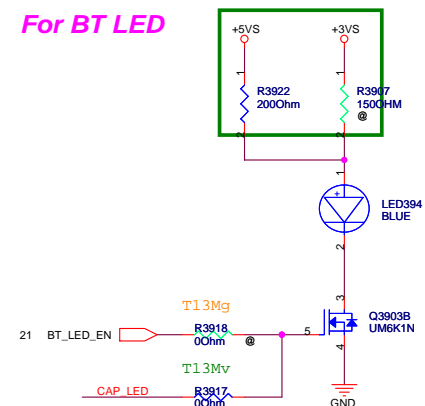
For POWER LED



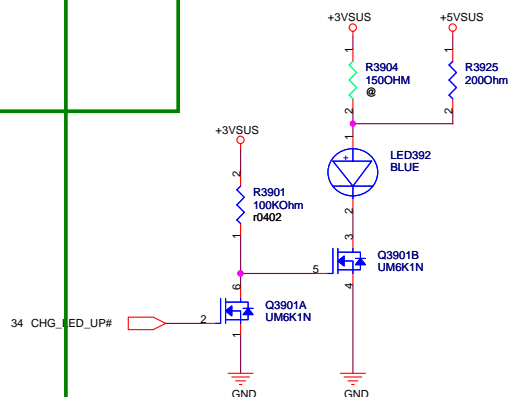
For WireLess LED



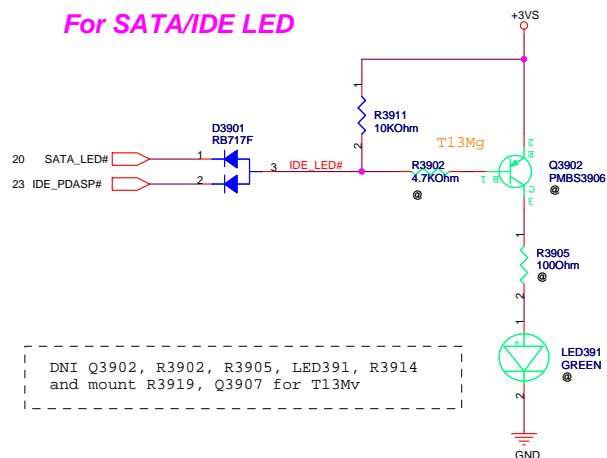
For BT LED



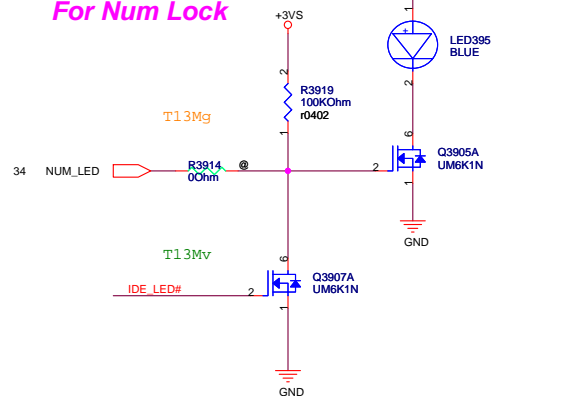
For BATTERY LED



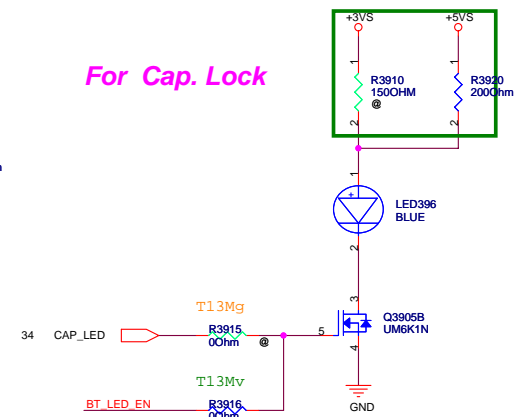
For SATA/IDE LED



For Num Lock



For Cap. Lock



<Variant Name>


ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CH_LIN	
Size	Project Name		
Custom	T13M		
Date: Friday, September 08, 2006	Sheet	39	of 65
	Rev	1.1	

	5	4	3	2	1
D					
C					
B					
A					

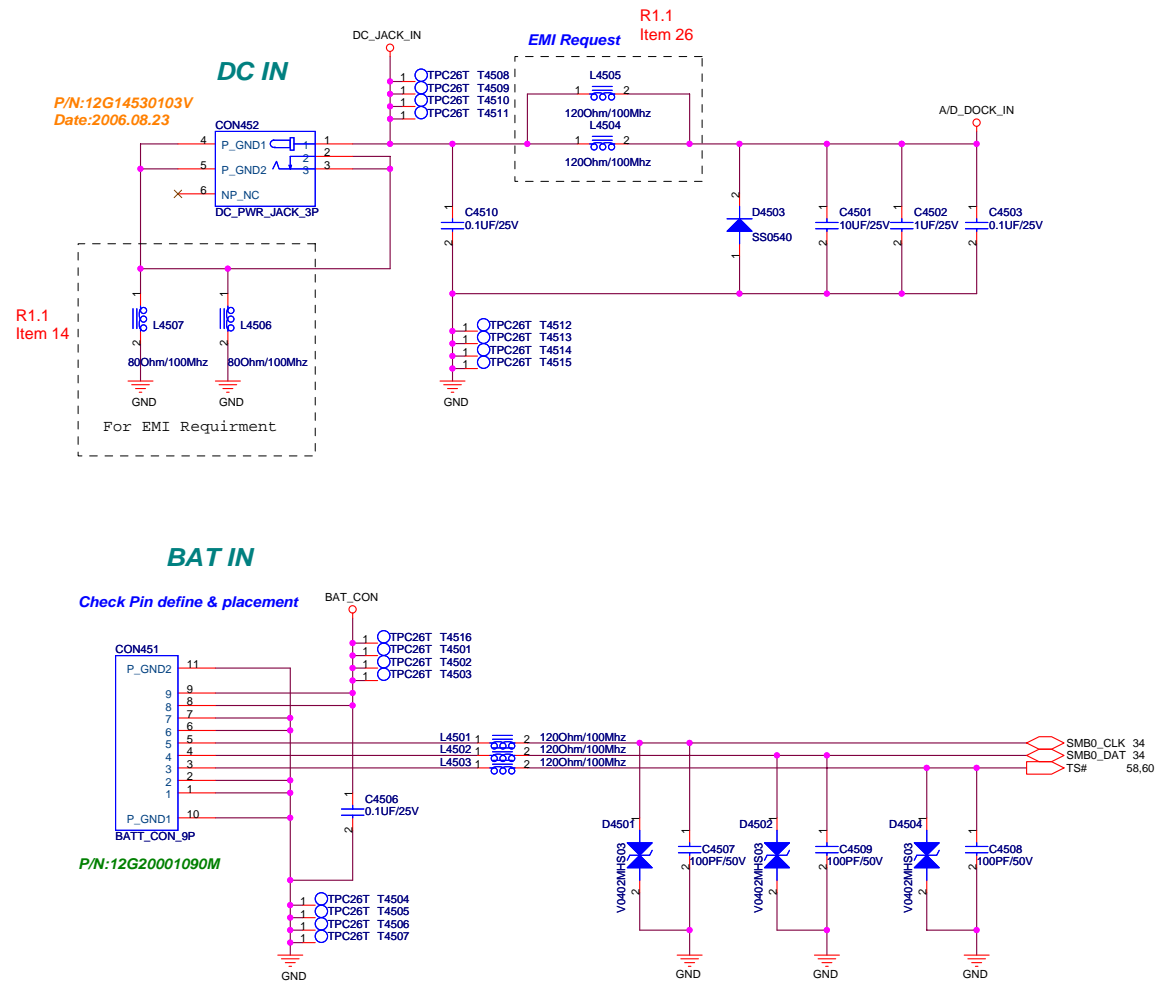
<Variant Name>

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size	Project Name		Rev
Custom	T13M		1.1
Date: Thursday, September 07, 2006		Sheet	41 of 65

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

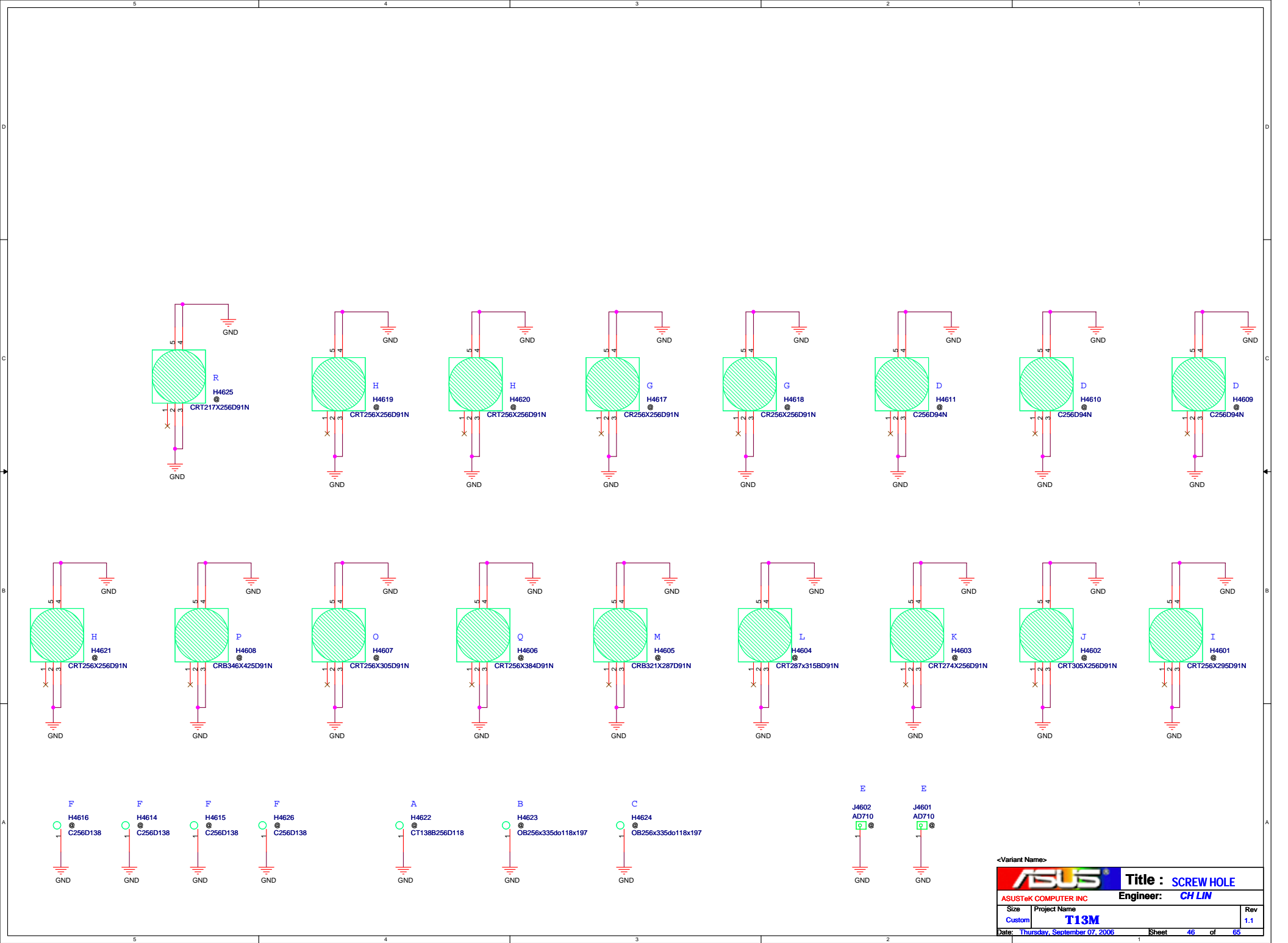
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ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size	Project Name		Rev
Custom	T13M		1.1
Date: Thursday, September 07, 2006		Sheet	43 of 65





<Variant Name>

ASUS		Title : BAT&Adapter conn	
ASUSTeK COMPUTER INC		Engineer: CH LIN	
Size Custom	Project Name T13M		Rev 1.1
Date: Friday, September 08, 2006		Sheet 45 of 65	



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	I
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	CR_DRIVER#	
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	LPC_RST#	I
31	ECSC#GPD3	EXT_SC#	O
41	GPD4	CR_POWER#	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	
88	ADC5/GPE1	N/A	
89	ADC6/GPE2	MARATHON#	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	
25	CLKRUN#/WUI7/GPE7	BT_ON#	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/O
115	PS2DAT1/GPF3	/	I/O
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	
28	LPC80LL/GPG7	AC_APR_UC#	

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	N/A	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

NV MCP51

Pin	Use As	Signal Name	Power
GPIO 1	i	GPO	+3VS
GPIO 2	i	GPO	+3VSUS
GPIO 3	i	GPI	+3VSUS
GPIO 4	i	GPO	+3VSUS
GPIO 5	i	GPO	+3VSUS
GPIO 6	i	GPO	+3VSUS
GPIO 7	i	GPO	+3VSUS
GPIO 8	i	GPO	+3VSUS
GPIO 9	i	GPO	+3VSUS
GPIO 10	i	GPO	+3VSUS
GPIO 11	i	GPO	+3VSUS
GPIO 12	i	GPO	+3VSUS
GPIO 13	i	GPO	+3VSUS
GPIO 14	i	GPO	+3VSUS
GPIO 15	i	GPO	+3VSUS
GPIO 16	i	GPO	+3VSUS
GPIO 17	N	Native	LID#
GPIO 18	N	Native	USB_OC#0
GPIO 19	N	Native	USB_OC#1
GPIO 20	N	Native	USB_OC#2
GPIO 21	N	Native	USB_OC#3
GPIO 22	N	Native	ACZ_SDIN0_AUD
GPIO 23	N	Native	ACZ_SDIN1_MDC
GPIO 24	N	Native	+3VSUS
GPIO 25	N	Native	SMB_CLK0
GPIO 26	N	Native	SMB_DATA0
GPIO 27	N	Native	SMB_CLK1
GPIO 28	N	Native	SMB_DATA1
GPIO 29	N	Native	SMB_ALERT#
GPIO 30	N	Native	PCI_PME#
GPIO 31	N	Native	SIO_PME#
GPIO 32	N	GPI	EXTSM#
GPIO 33	N	Native	SB_R#
GPIO 34	N	Native	SUS_CLK
GPIO 35	N	Native	MII_INTR
GPIO 36	N	Native	PHY_RXER

PCI Device	IDSEL#	REQ/GNT#	Interrupts

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

Pin	Use As	Signal Name	Power
GPIO 37	N	Native	+3VSUS
GPIO 38	N	Native	+3VS
GPIO 39	N	Native	+3VS
GPIO 40	N	Native	+3VS
GPIO 41	N	Native	+3VS
GPIO 42	N	Native	PM_CLKRUN#
GPIO 43	N	Native	PCI_PERR#
GPIO 44	N	Native	ACZ_SYNC
GPIO 45	N	Native	ACZ_SDOUT
GPIO 46	i	GPO	+3VS
GPIO 47	i	GPO	+3VS
GPIO 48	N/A	N/A	N/A
GPIO 49	N	Native	+3VS
GPIO 50	N	Native	SB_PANEL_PWR
GPIO 51	N	Native	SB_BKL_ON
GPIO 52	N	Native	EDID_CLK
GPIO 53	N	Native	EDID_DAT
GPIO 54	i	GPO	+3VS
GPIO 55	N	Native	A20GATE
GPIO 56	N	Native	RCIN#
GPIO 57	N	Native	SATA_LED#
GPIO 58	N	Native	THRMTRIP#
GPIO 59	N	Native	PM_THRM#
GPIO 60	N	GPI	PCB_ID0
GPIO 61	N	GPI	PCB_ID1
GPIO 62	N	GPI	PCB_ID2
GPIO 63	N	Native	IDE_PDIAG
GPIO 64	N	Native	+3VS

<Variant Name>

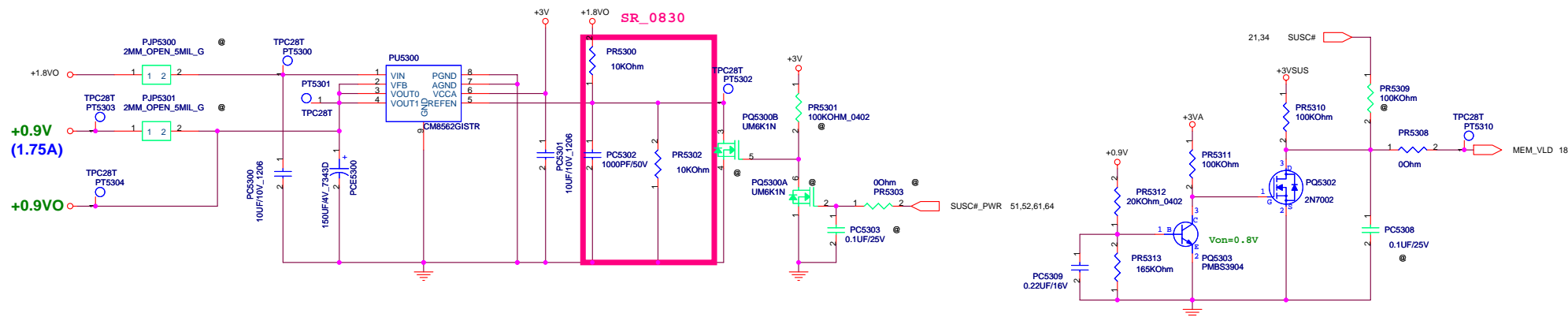
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ASUSTek COMPUTER INC		Engineer: CH LIN	
Size	Project Name		
Custom	T13M		
Date: Thursday, September 07, 2006	Sheet	47	of 65
			Rev 1.1

- R1.0 (Release on 2006/07/26)
- R1.10 (Release on 2006/09/07)
- 1.)Page 4: Change reference name from L1 to L401.
 - 2.)Page 6: DNI R711 because Int. pull-up resister exists in FAN module.
 - 3.)Page 7: Add R704, Q702 prevent leakage current.
 - 4.)Page 20: Change C2056 and C2057 form 27pF to 22pF for ITTI recommendation.
 - 5.)Page 20: Change reference name from X1901 to X2052.
 - 6.)Page 23: Change reference name C4511 -> C2315, C4513 -> C2313, C4512 -> C2312, C4514 -> C2314.
 - 7.)Page 23: Change R2301 size from 0603 to 0402.
 - 8.)Page 29: Change reference name from R3921 to R2921, C4515 to 2915.
 - 9.)Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.
 - 10.)Page 34: DNI D704, R3409, R3411 and mount R3408, R3418 for thermal protection.
 - 11.)Page 36: Change reference name from JP3403 to JP3601
 - 12.)Page 36: Change R3622 size from 0402 to 0603.
 - 13.)Page 20: Change C2062 and C2071 form 15pF to 18pF for ITTI recommendation.
 - 14.)Page 45:Add L4506 and L4507 for EMI requirement.
 - 15.)Page 21: Change BT_LED_EN from GPIO6 to GPIO7, GPIO6 is reserve for VBIOS.
 - 16.)Page 16: Change R1604, R1605 from 0ohm to 33ohm ,C1607, C1608 from 47PF to 10PF ,prevent large overshoot and undershoot.
 - 17.)Page 16: Change L1601, L1602, and L1603 from bead to inductor for tune VGA signal.
 - 18.)Page 19: Add U1951, C1953 to prevent EC second reset from S3.
 - 19.)Page 21: Delete R2174, R2197, R2144, R2152 for no MDC function.
 - 20.)Page 14: Reserve C1423, C1424, C1425 for tune VGA signal and EMI .
 - 21.)Page 13: Mount R1356 for meet NV spec.
 - 22.)Page 23: Change JP2302 footprint .
 - 23.)Page 25: Change C2503 from 0.1uF to 1uF for meet chip spec. Unmount R2504, D2502 for chip can self discharge .
 - 24.)Page 31: Unmount D3104, D3105 ,Add D3120, D3121 for depop (+5VS_AUDIO).
 - 25.)Page 29: Reserve X2953,C2974,C2975,Del R2904,R2921,Add R2903,C2901 for NV AP NOTE .
 - 26.)Page 45: Change L4504, L4505 from 80ohm/100MHz to 120ohm/100MHz for EMI request.
 - 27.)Page 34: Add ESD Protection*D3402 for Touch Pad.
 - 28.)Page 25: Mount D2501 for EMI request.
 - 29.)Page 17: Change +3VS to +3VS_LCD for prevent resume from S3 pannel white noise .
 - 30.)Page 17: Change D1704, R1705 value to meet LCD power discharge sequence.
 - 31.)Page 13&17 : Unmount parts about NEWCARD for no NEWCARD spec.

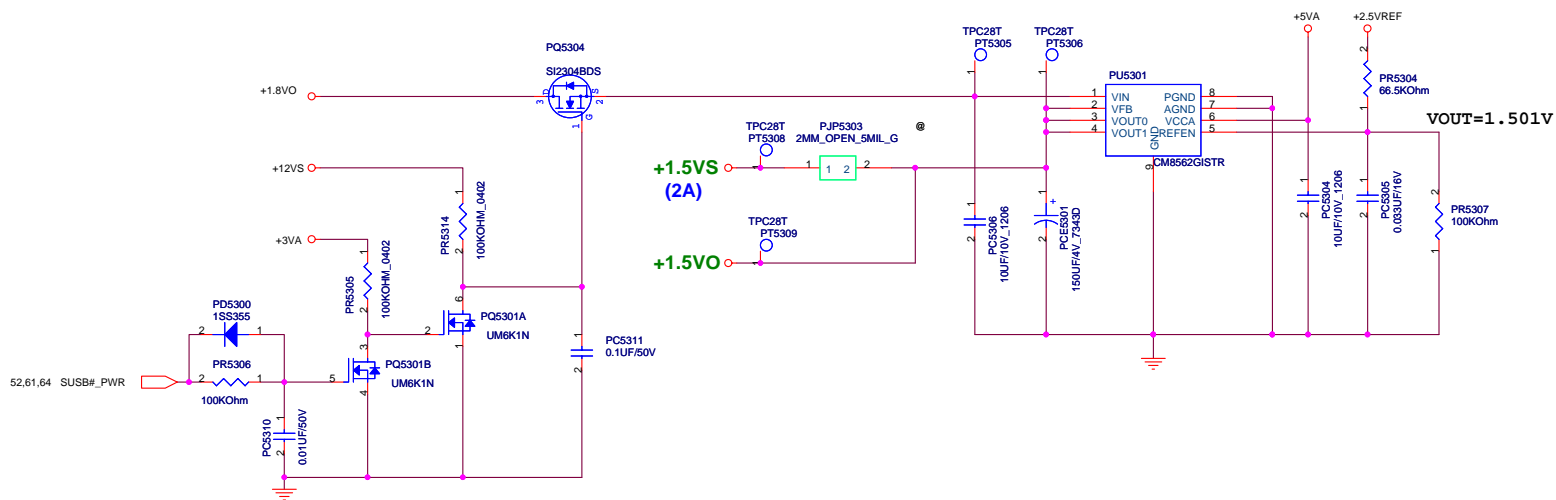
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		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer: CH_Lin	
Size	Project Name		Rev
Custom	T13M		1.1
Date: Thursday, September 07, 2006		Sheet	48 of 65

VTT



1.5Vs



	5	4	3	2	1
D					
C					
B					
A					



Title : POWER_VGA_CORE & RAM

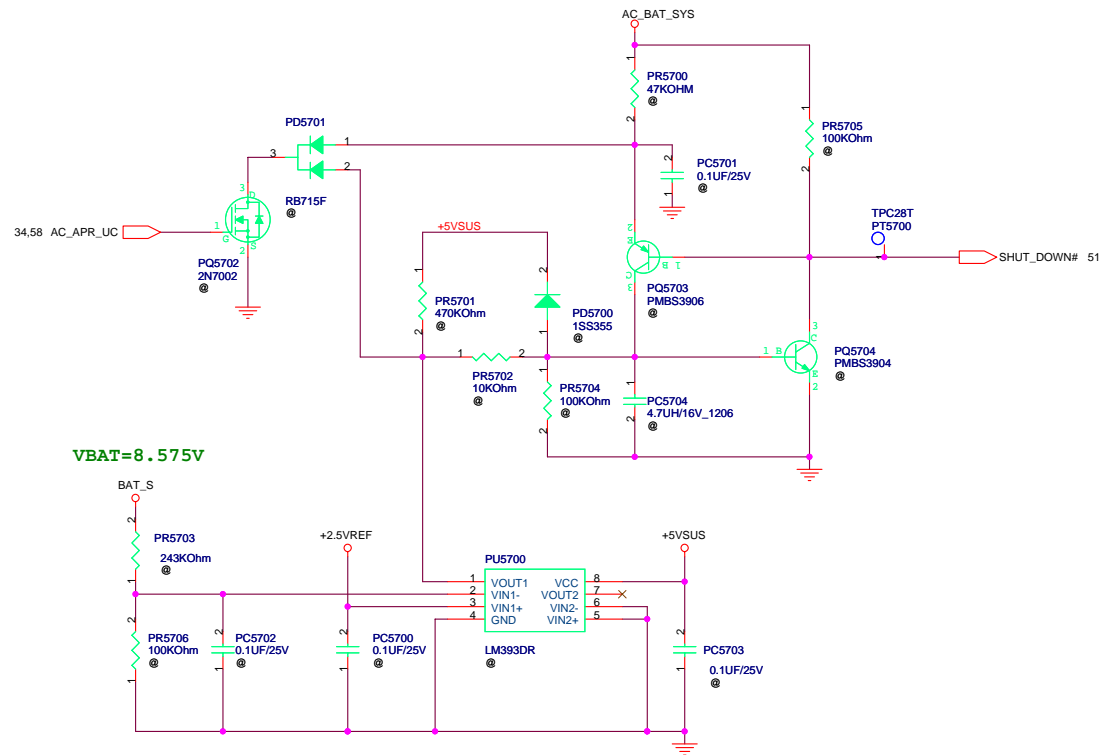
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Engineer:

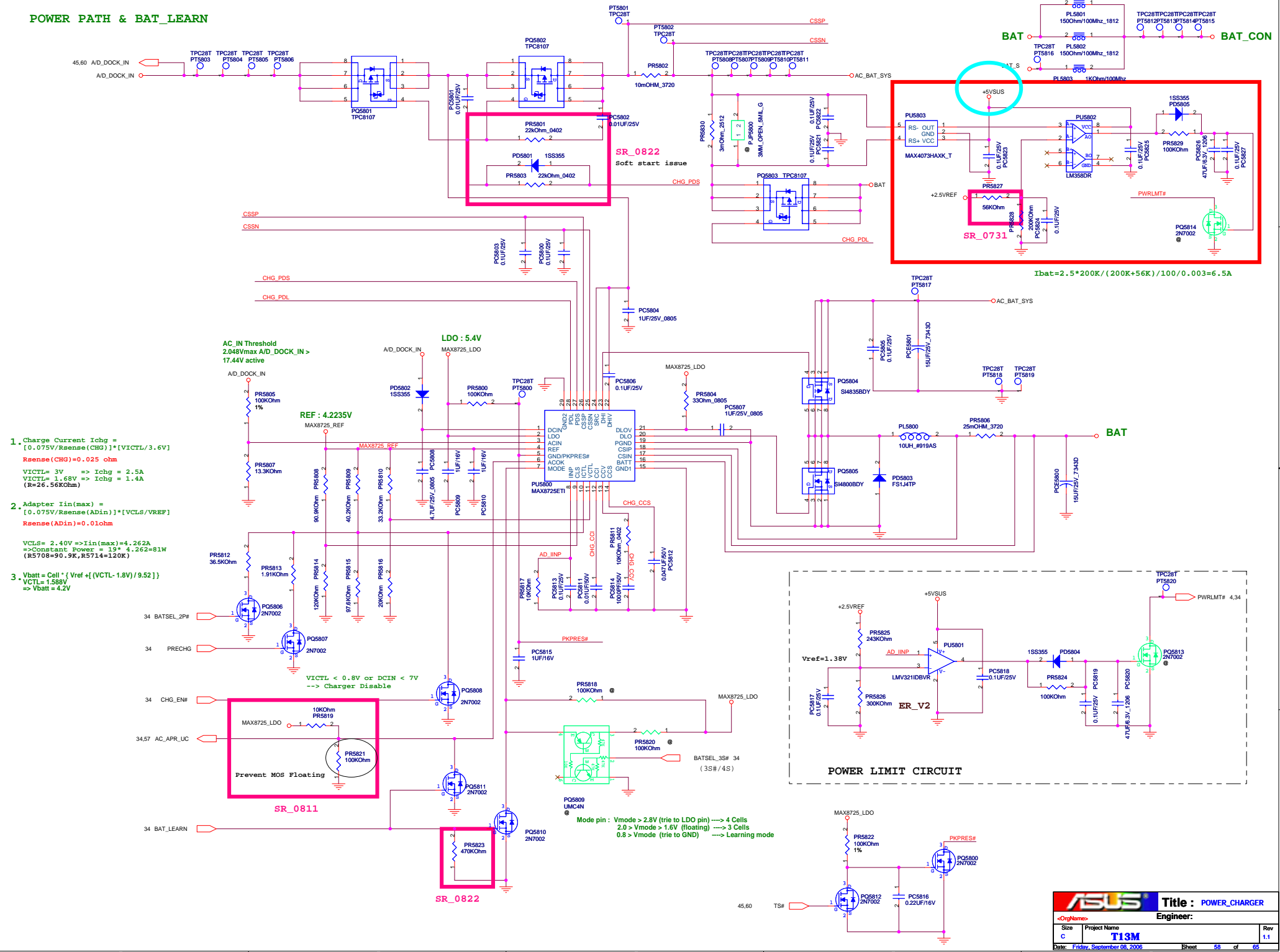
Size	Project Name	Rev
C	T13M	1.1

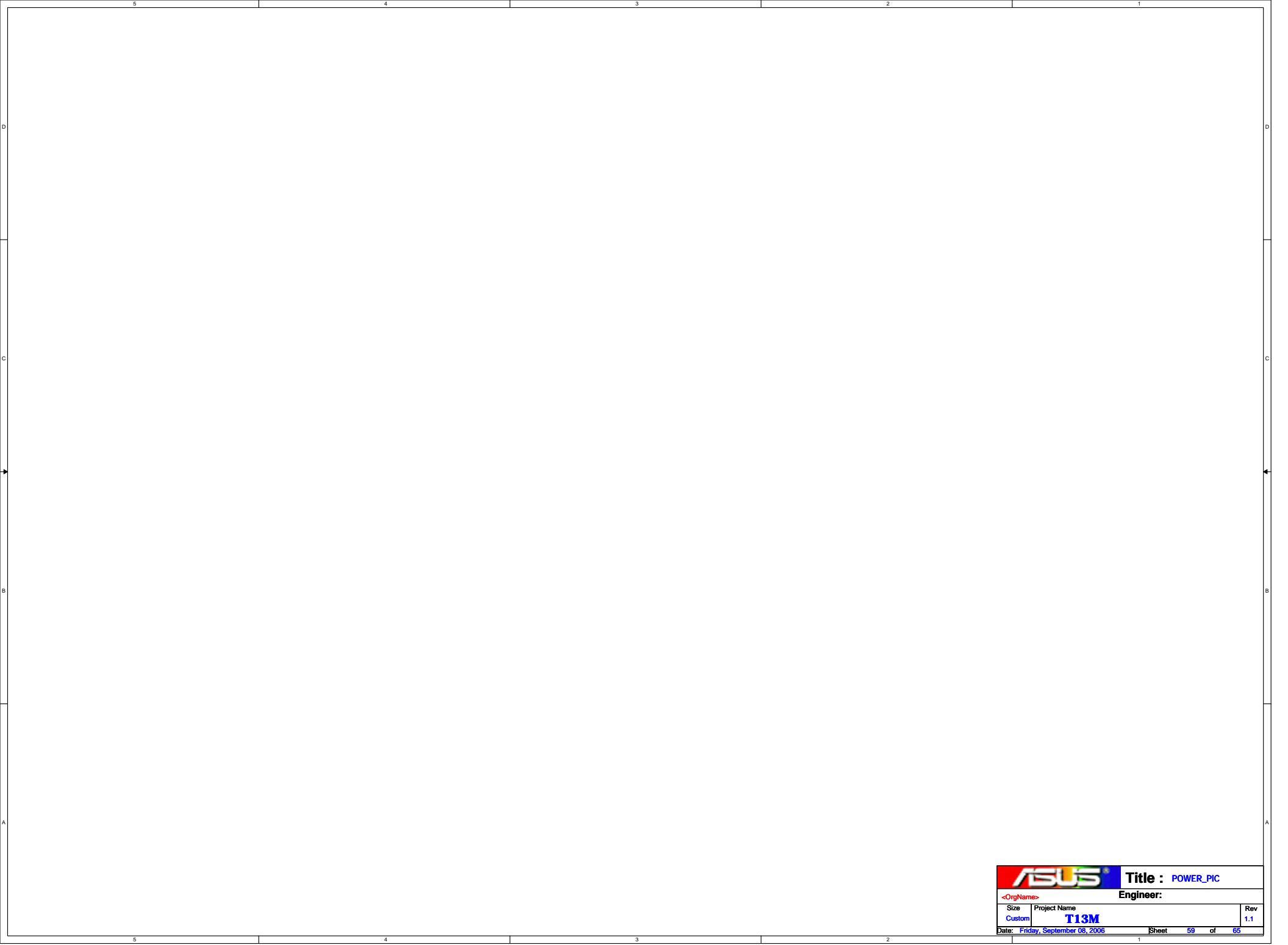
Date: Friday, September 06, 2006Sheet 55 of 65

BATTERY UVP CIRCUIT



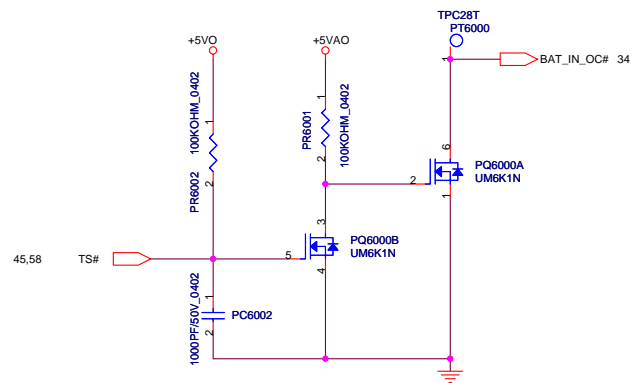
POWER PATH & BAT_LEARN



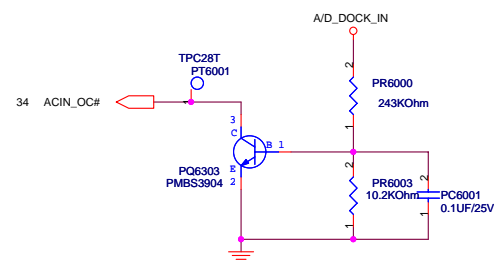


		Title : POWER_PIC	
Engineer:			
Size	Project Name		Rev
Custom	T13M		1.1
Date: Friday, September 08, 2006		Sheet	59 of 65

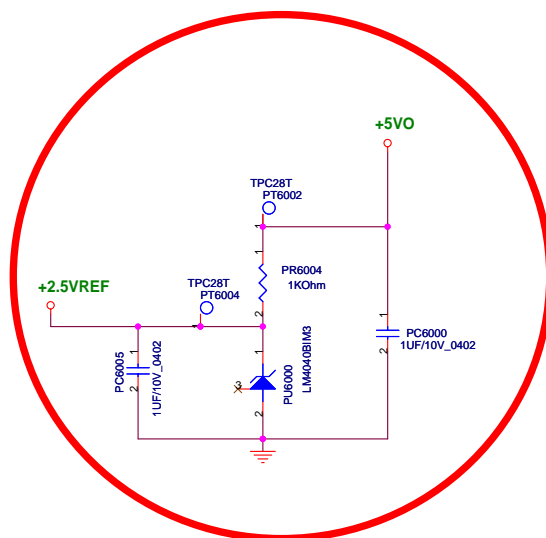
BATTERY IN DETECT



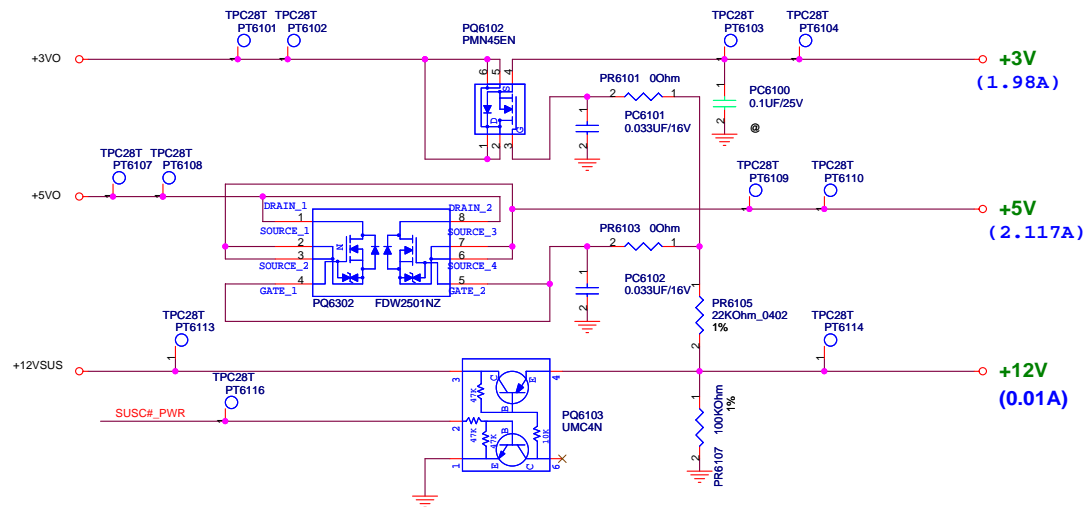
ADAPTER IN DETECT



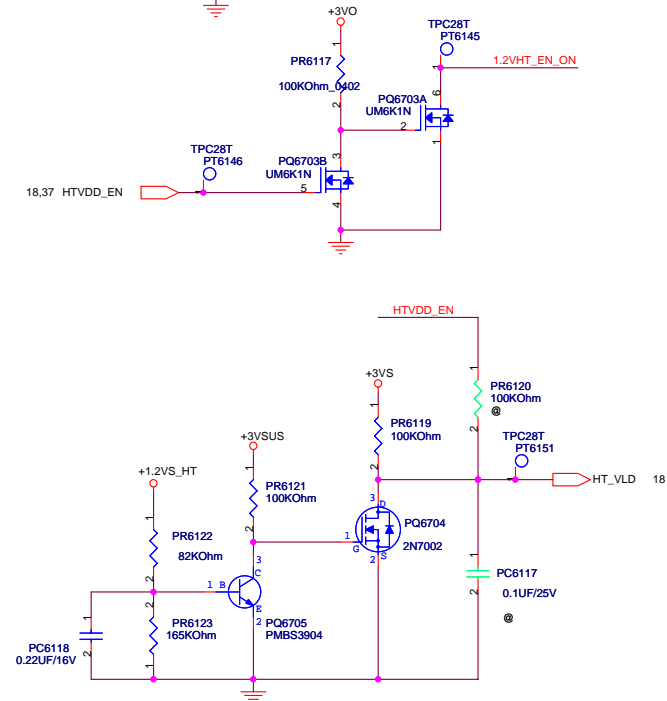
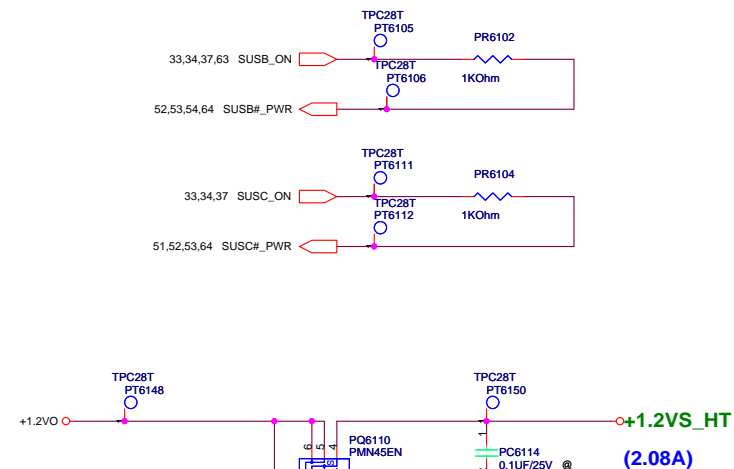
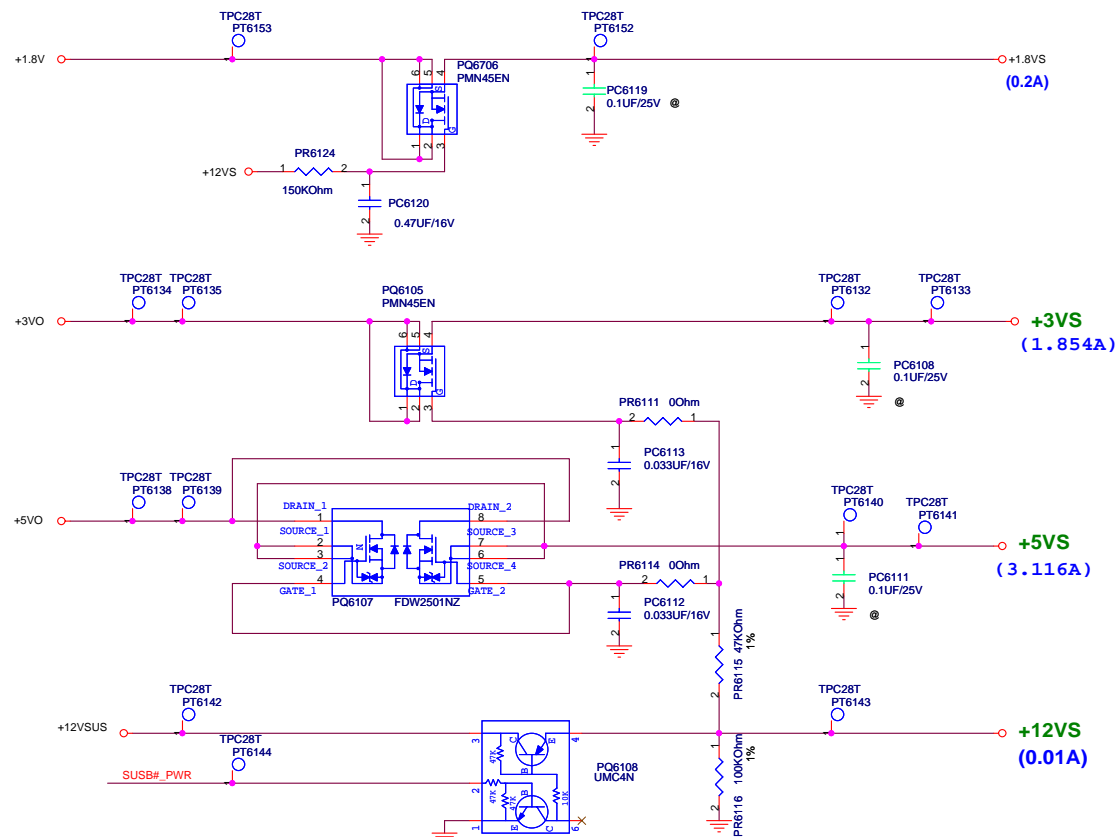
+2.5VREF

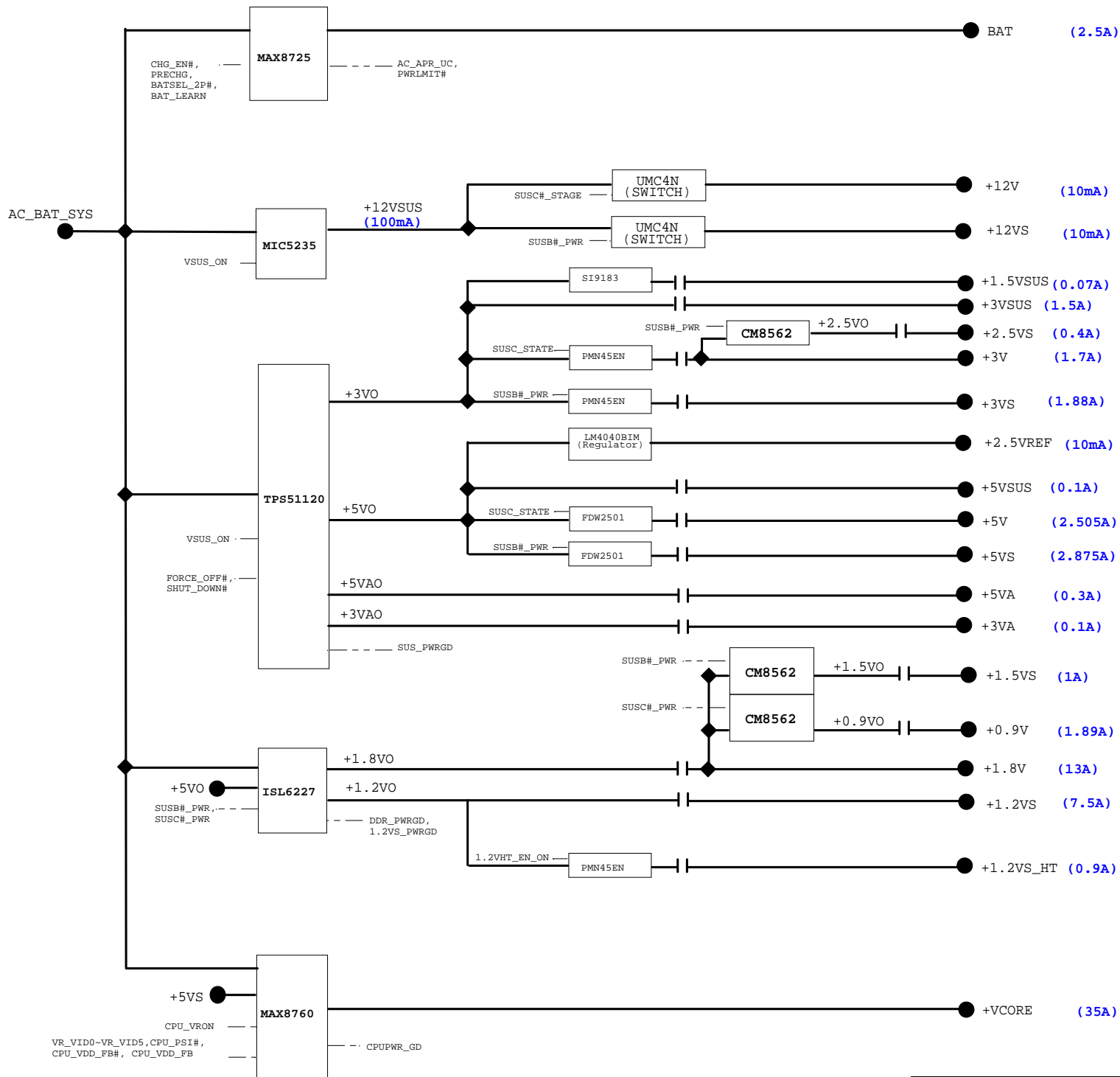


SUSC#_STAGE POWER

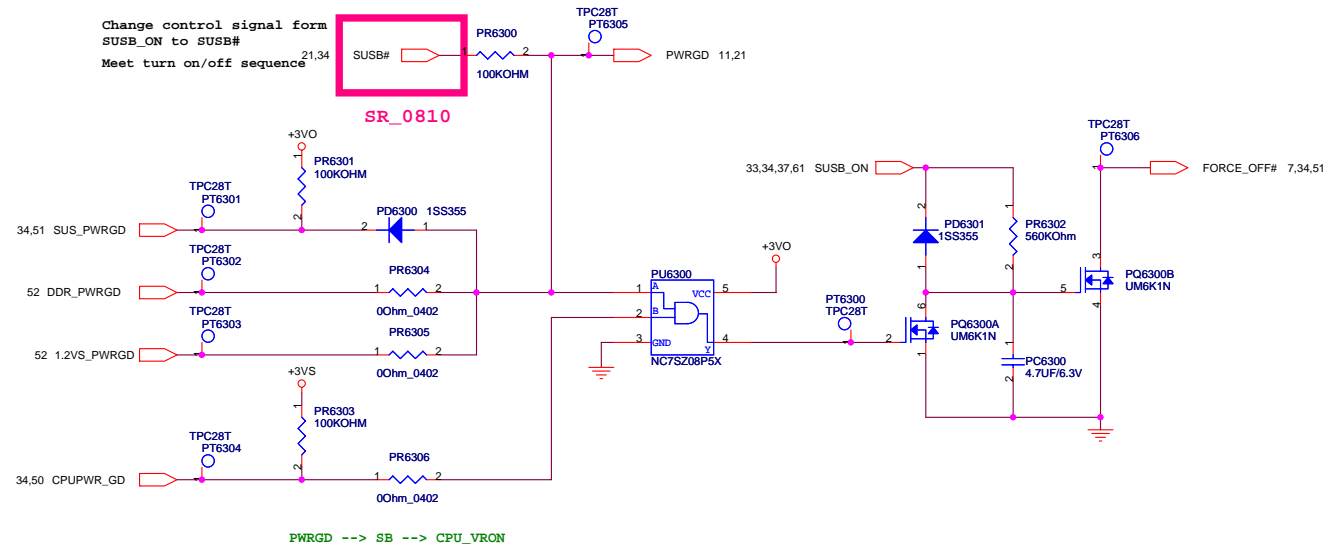


SUSB#_PWR POWER





POWER GOOD DETECTOR





FOR POWER TEST

