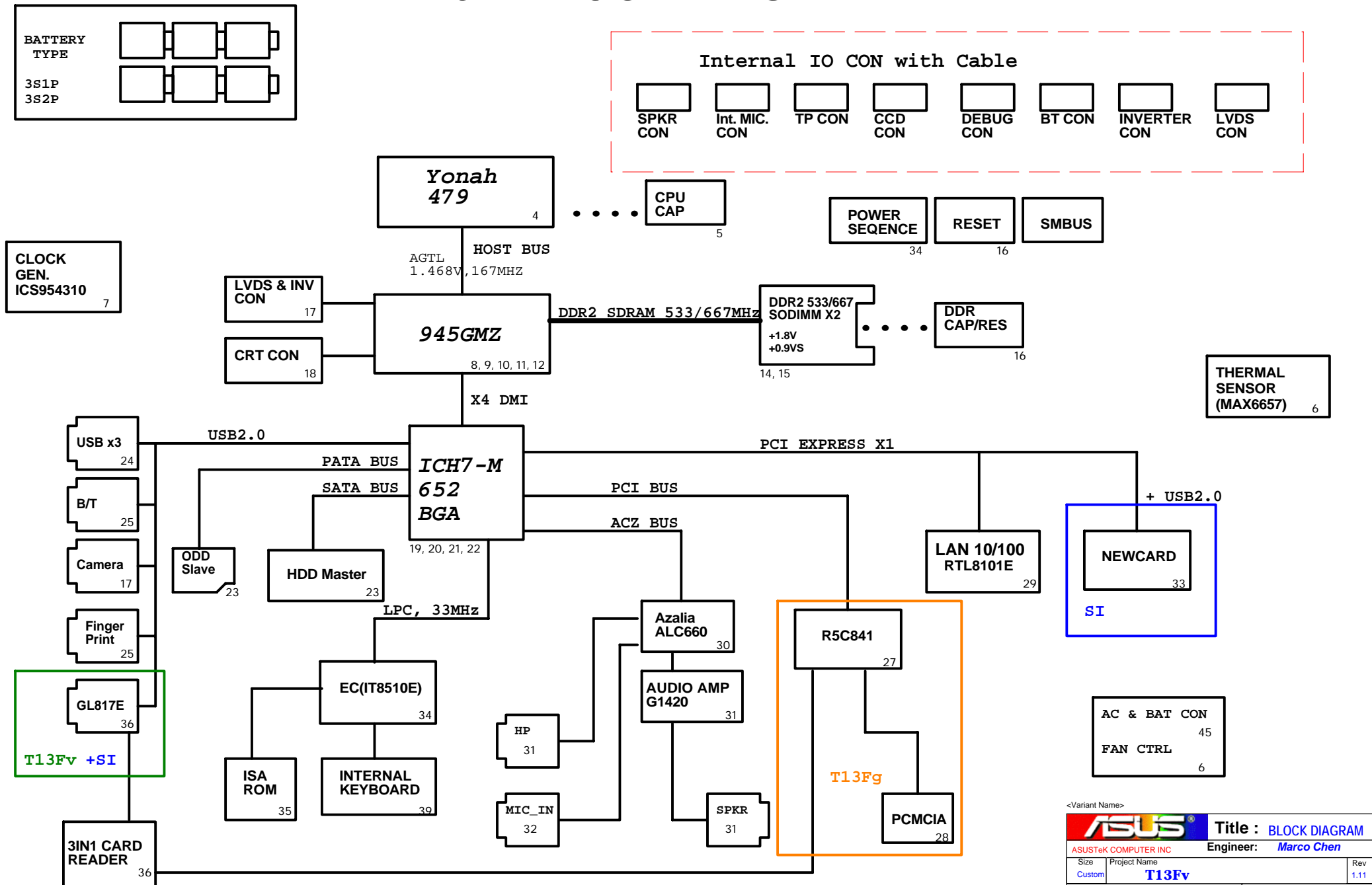


T13Fv SCHEMATIC R1.11

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5	YONAH CPU (2)	49	History(2)
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7	CLK GEN-ICS954310	POWER PAGE REF.	
8	Calistoga--CPU	50	POWER_VCORE
9	Calistoga--PCIE	51	POWER_SYSTEM
10	Calistoga--DDR2	52	POWER_I/O_1.8V & 1.05VS
11	Calistoga--POWER	53	POWER_I/O_DDR & VTT
12	Calistoga--GND	54	POWER_I/O_VTT & +2.5VS
13	Calistoga--Strap	55	POWER_VGA_CORE(Empty)
14	DDR2 SO-DIMM_0	56	POWER_VGA_RAM(Empty)
15	DDR2 SO-DIMM_1	57	POWER_CHARGER
16	DDR2 ADDRESS TERMINATION	58	POWER_PIC(Empty)
17	LVDS & INVERTER CONN	59	POWER_DETECT
18	VGA CONN	60	POWER_PROTECT
19	ICH7M--CPU,IDE,AUDIO	61	POWER_LOAD SWITCH
20	ICH7M--GPIO	62	POWER_FLOWCHART
21	ICH7M--PCI,PCI-E,USB	63	POWER_SIGNAL
22	ICH7M--VCC,GND		
23	HDD & CD-ROM CONN		
24	USB PORT		
25	B/T & F/P		
26	B TO B CONN(M)		
27	CARDBUS R5C841		
28	PCMCIA SOCKET		
29	PCI-E--LAN_RTL8101E		
30	AZALIA - ALC660-GR		
31	AUDIO_AMPLIFIER		
32	MICROPHONE		
33	NEWCARD		
34	EC-IT8510E		
35	ISA ROM & Touch Pad & KB& FP		
36	Card Reader GL817E		
37	DISCHARGE		
38	Instant Key & FFC CONN		
39	LEDs		
40	EMPTY		
41	EMPTY		
42	EMPTY		
43	EMPTY		
44	EMPTY		
45	SREW HOLE		
46	DC & BAT IN		

# T13F BLOCK DIAGRAM



## EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	KCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	CR_DRIVER#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PCI_RST#	I
31	ECSC#GPD3	EXT_SC#	O
41	GPD4	CR_POWER#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	PWR_LMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTERR_DA	O
102	DAC3	BATSEL_2P#	O

## ICH7M\_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

## ICH7M\_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A4 )
Thermal Sensor( MAX6657)	1001100x ( 98 )

## ICH7M\_PCI\_DEVICE:

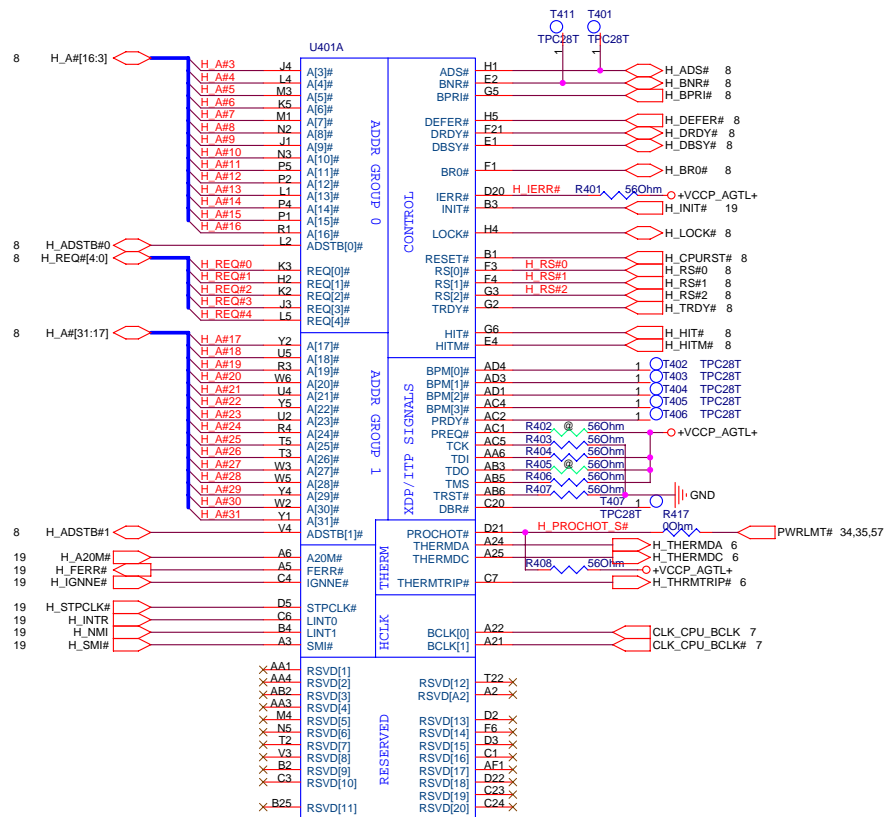
PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

## ICH7M\_GPIO

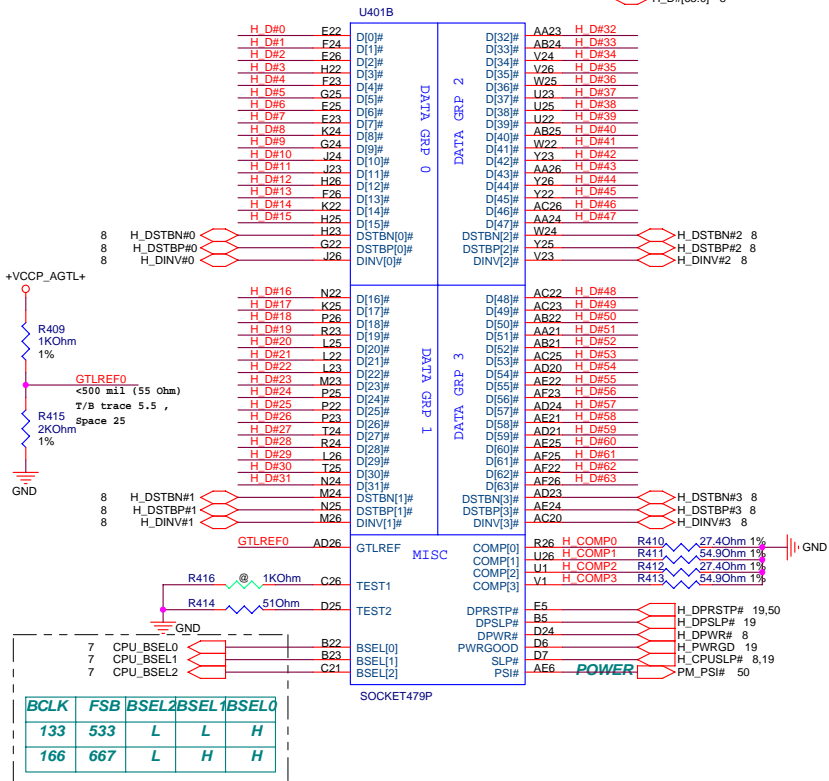
Pin	Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#
GPIO 01	i	GPI	PCI_REQ#5
GPIO [5:2]	i	GPI	PCI_INT[E:H]#
GPIO 06	i	GPO	BT_LED_EN
GPIO 07	i	GPI	N/A
GPIO 08	i	GPI	EXTSM#
GPIO 09	i	GPI	N/A
GPIO 10	i	GPI	N/A
GPIO 11	i	Native	SMB_ALERT#
GPIO 12	i	GPI	KBC_SC#
GPIO 13	i	GPI	N/A
GPIO 14	i	GPI	N/A
GPIO 15	i	GPO	802_LED_EN
GPIO 16	O 0	GPO	PM DPRSLPVR
GPIO 17	O 1	GPO	PCI_GNT#5
GPIO 18	O 1	GPO	STP_PCI#
GPIO 19	i 1	GPI	N/A
GPIO 20	O 1	GPO	STP_CPU#
GPIO 21	i 1	GPO	N/A
GPIO 22	i 1	Native	PCI_REQ#4
GPIO 23	i 1	Native	N/A
GPIO 24	O 0	GPO	MSK_PCIRST
GPIO 25	O 1	GPO	CB_SD#
GPIO 26	O 0	GPO	BT_ON#
GPIO 27	O 0	GPO	WLAN_ON#
GPIO 28	O 0	GPO	MEMROM/YONAH#
GPIO 29	i 0	Native	USB_OC#5
GPIO 30	i 0	Native	USB_OC#6
GPIO 31	i 0	Native	USB_OC#7
GPIO 32	O 1	GPO	PM_CLKRUN#
GPIO 33	O 1	GPO	N/A
GPIO 34	O 0	GPO	CPU_Select
GPIO 35	O 0	GPO	N/A
GPIO 36	i 0	GPO	N/A
GPIO 37	i 0	GPI	PCB_ID0
GPIO 38	i 0	GPI	PCB_ID1
GPIO 39	i 0	GPI	PCB_ID2
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

<Variant Name>

		Title :	Schematic data
ASUSTek COMPUTER INC		Engineer:	Marco Chen
Size	Project Name	Rev	
Custom	T13Fv	1.11	
Date: Monday, August 28, 2006		Sheet	3 of 63



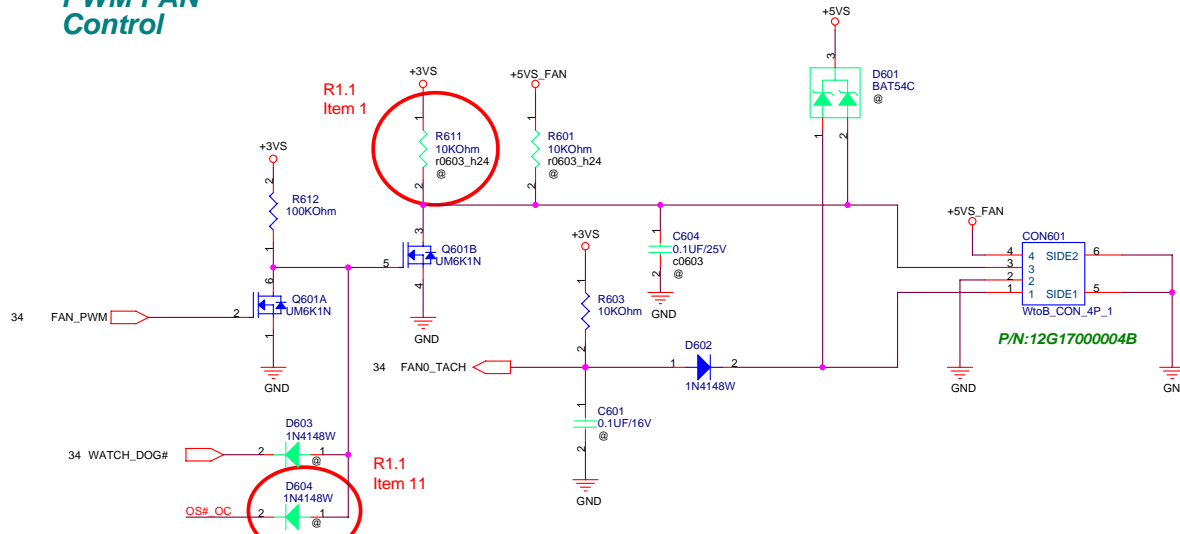
P/N: 12G04600479A



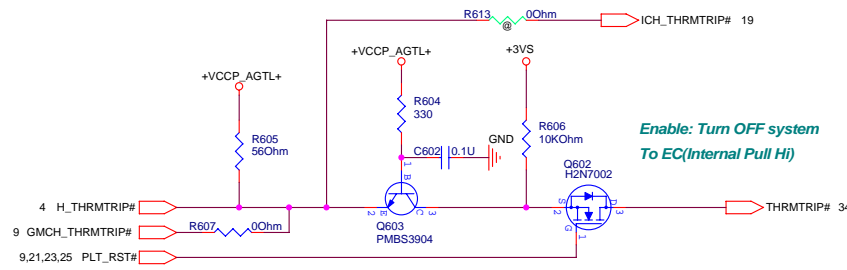
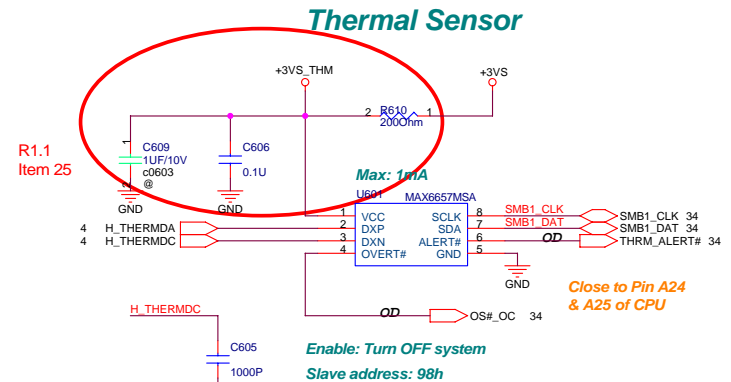
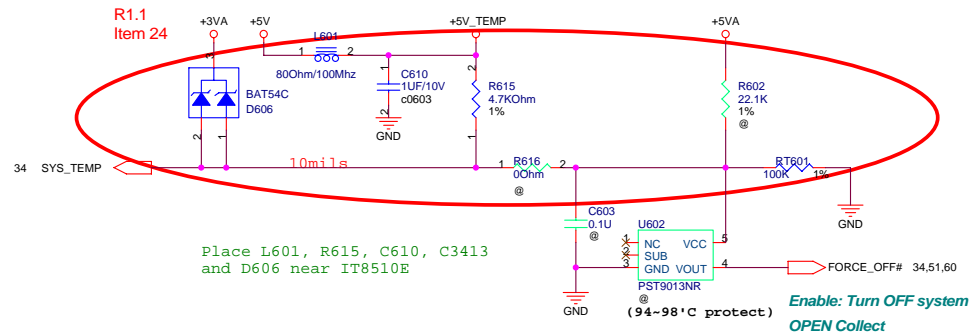
<Variant Name>



## PWM FAN Control



CPU FAN will be forced on:  
1) Thermal Sensor Over-temperature  
2) WATCHDOG asserted by EC



<Variant Name>

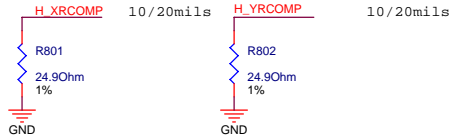
<b>ASUS</b>		Title :FAN_CTRL&Thermal	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13Fv	1.11	
Date: Monday, August 28, 2006		Sheet	6 of 63





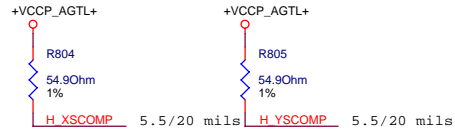
## RCOMP

For Calibrating FSB I/O Buffer



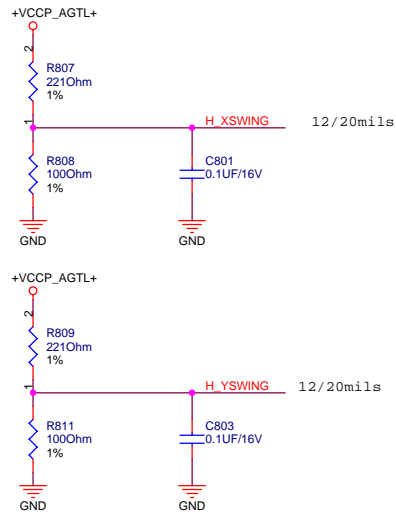
## SCOMP

For Slew Rate Compensation on the FSB

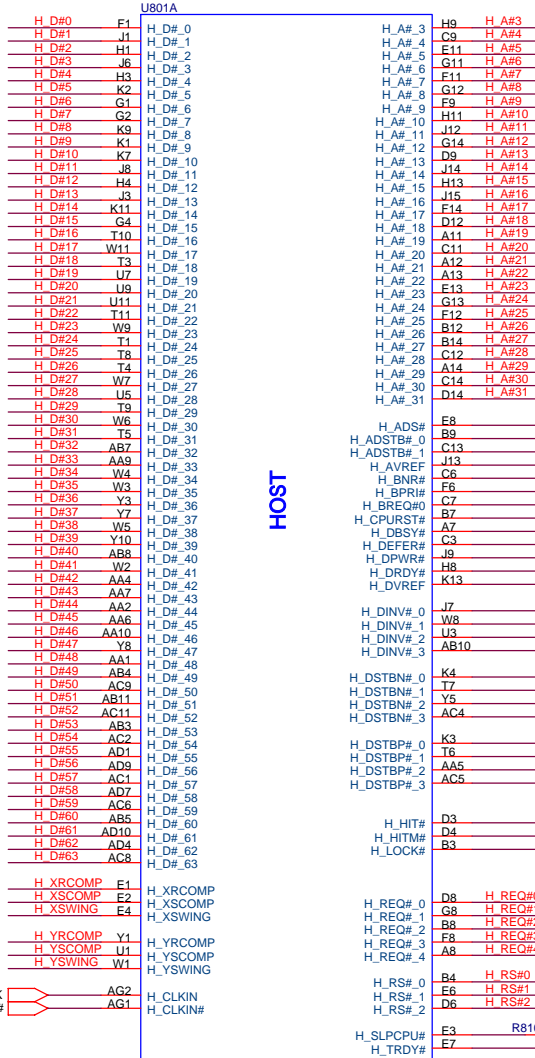


## Voltage Swing

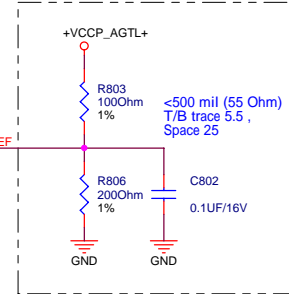
For Providing a Reference Voltage to The FSB RCOMP Circuit



4 H\_D#[0..63] H\_D#[0..63] H\_A#[3..31] H\_A#[3..31] 4



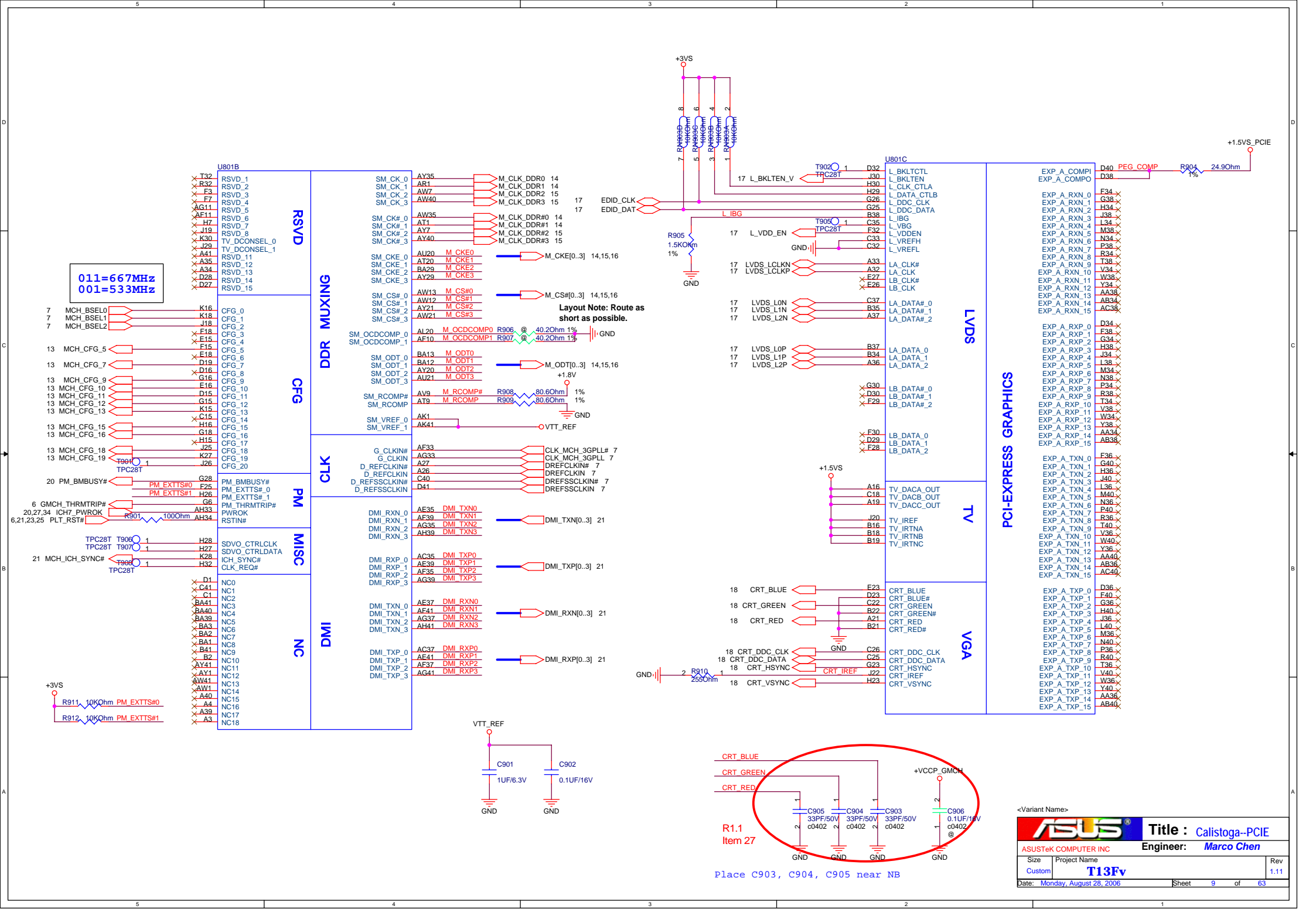
## AGTL+ I/O Voltage Reference



H\_VREF T801 TPC28T

<Variant Name>





14 M\_A\_DQ[0..63]

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M\_A\_DQ0 AJ35 SA\_DQ0  
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M\_A\_DQ4 AK35 SA\_DQ4  
M\_A\_DQ5 AJ36 SA\_DQ5  
M\_A\_DQ6 AJ32 SA\_DQ6  
M\_A\_DQ7 AH31 SA\_DQ7  
M\_A\_DQ8 AN35 SA\_DQ8  
M\_A\_DQ9 AP33 SA\_DQ9  
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M\_A\_DQ11 AP31 SA\_DQ11  
M\_A\_DQ12 AN38 SA\_DQ12  
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M\_A\_DQ16 AK26 SA\_DQ16  
M\_A\_DQ17 AL27 SA\_DQ17  
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M\_A\_DQ47 AL5 SA\_DQ47  
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M\_A\_DQ60 AH6 SA\_DQ60  
M\_A\_DQ61 AF4 SA\_DQ61  
M\_A\_DQ62 AF4 SA\_DQ62  
M\_A\_DQ63 AFB SA\_DQ63

## DDR SYSTEM MEMORY A

SA\_BS\_0 AU12 M\_A\_BS#0 14,16  
SA\_BS\_1 AV14 M\_A\_BS#1 14,16  
SA\_BS\_2 BA20 M\_A\_BS#2 14,16  
SA\_CAS# AY13 M\_A\_CAS# 14,16  
SA\_DM\_0 AJ33 M\_A\_DM0  
SA\_DM\_1 AM35 M\_A\_DM1  
SA\_DM\_2 AL26 M\_A\_DM2  
SA\_DM\_3 AN22 M\_A\_DM3  
SA\_DM\_4 AM14 M\_A\_DM4  
SA\_DM\_5 AL9 M\_A\_DM5  
SA\_DM\_6 AR3 M\_A\_DM6  
SA\_DM\_7 AH4 M\_A\_DM7  
SA\_DQS\_0 AK33 M\_A\_DQS0  
SA\_DQS\_1 AT33 M\_A\_DQS1  
SA\_DQS\_2 AN28 M\_A\_DQS2  
SA\_DQS\_3 AM22 M\_A\_DQS3  
SA\_DQS\_4 AN12 M\_A\_DQS4  
SA\_DQS\_5 AN8 M\_A\_DQS5  
SA\_DQS\_6 AP3 M\_A\_DQS6  
SA\_DQS\_7 AG5 M\_A\_DQS7  
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SA\_DQS#\_6 AN3 M\_A\_DQS#6  
SA\_DQS#\_7 AH5 M\_A\_DQS#7  
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SA\_MA\_1 AU14 M\_A\_A1  
SA\_MA\_2 AW16 M\_A\_A2  
SA\_MA\_3 BA16 M\_A\_A3  
SA\_MA\_4 BA17 M\_A\_A4  
SA\_MA\_5 AU16 M\_A\_A5  
SA\_MA\_6 AV17 M\_A\_A6  
SA\_MA\_7 AU17 M\_A\_A7  
SA\_MA\_8 AW17 M\_A\_A8  
SA\_MA\_9 AT16 M\_A\_A9  
SA\_MA\_10 AU13 M\_A\_A10  
SA\_MA\_11 AT17 M\_A\_A11  
SA\_MA\_12 AV20 M\_A\_A12  
SA\_MA\_13 AV12 M\_A\_A13  
SA\_RAS# AW14 M\_A\_RAS# 14,16  
SA\_RCVENIN# AK23  
SA\_RCVENOUT# AK24  
SA\_WE# AY14 M\_A\_WE# 14,16

M\_A\_BS#0 14,16  
M\_A\_BS#1 14,16  
M\_A\_BS#2 14,16  
M\_A\_CAS# 14,16  
M\_A\_DM[0..7] 14  
M\_A\_DQS[0..7] 14  
M\_A\_DQS#[0..7] 14  
M\_A\_A[0..13] 14,16  
M\_A\_RAS# 14,16  
M\_A\_WE# 14,16

15 M\_B\_DQ[0..63]

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M\_B\_DQ31 AW29 SB\_DQ31  
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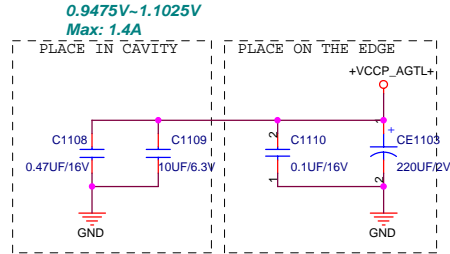
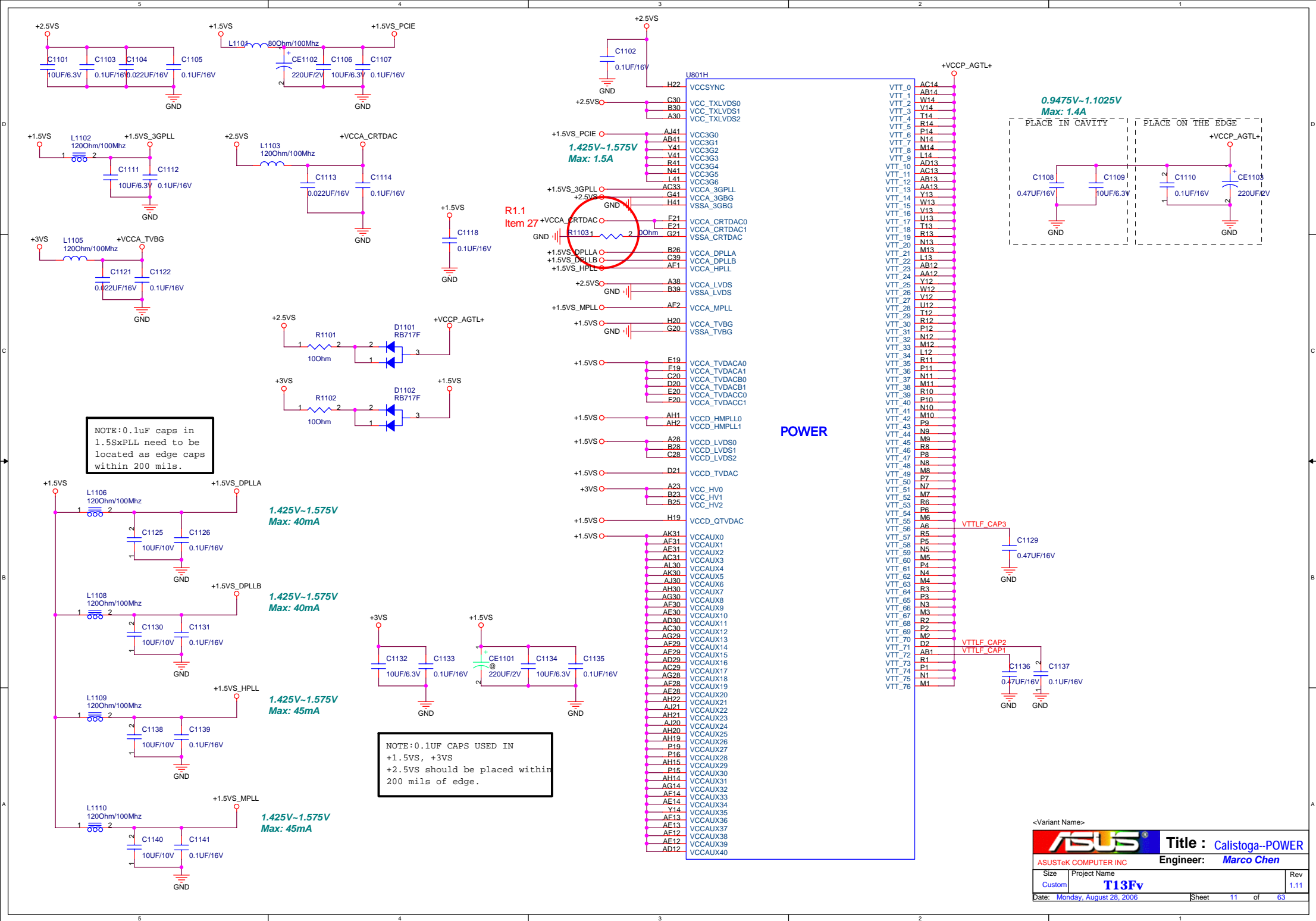
## DDR SYSTEM MEMORY B

SB\_BS\_0 AT24 M\_B\_BS#0 15,16  
SB\_BS\_1 AV23 M\_B\_BS#1 15,16  
SB\_BS\_2 AY28 M\_B\_BS#2 15,16  
SB\_CAS# AR24 M\_B\_CAS# 15,16  
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SB\_DM\_1 AR38 M\_B\_DM1  
SB\_DM\_2 AT36 M\_B\_DM2  
SB\_DM\_3 BA31 M\_B\_DM3  
SB\_DM\_4 AL17 M\_B\_DM4  
SB\_DM\_5 AH8 M\_B\_DM5  
SB\_DM\_6 BA5 M\_B\_DM6  
SB\_DM\_7 AN4 M\_B\_DM7  
SB\_DQS\_0 AM39 M\_B\_DQS0  
SB\_DQS\_1 AT39 M\_B\_DQS1  
SB\_DQS\_2 AU35 M\_B\_DQS2  
SB\_DQS\_3 AR29 M\_B\_DQS3  
SB\_DQS\_4 AR16 M\_B\_DQS4  
SB\_DQS\_5 AR10 M\_B\_DQS5  
SB\_DQS\_6 AR7 M\_B\_DQS6  
SB\_DQS\_7 AN5 M\_B\_DQS7  
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SB\_DQS#\_6 AT7 M\_B\_DQS#6  
SB\_DQS#\_7 AP5 M\_B\_DQS#7  
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SB\_MA\_1 AW24 M\_B\_A1  
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SB\_MA\_3 AR28 M\_B\_A3  
SB\_MA\_4 AT27 M\_B\_A4  
SB\_MA\_5 AT28 M\_B\_A5  
SB\_MA\_6 AU27 M\_B\_A6  
SB\_MA\_7 AV28 M\_B\_A7  
SB\_MA\_8 AV27 M\_B\_A8  
SB\_MA\_9 AW27 M\_B\_A9  
SB\_MA\_10 AY24 M\_B\_A10  
SB\_MA\_11 BA27 M\_B\_A11  
SB\_MA\_12 AY27 M\_B\_A12  
SB\_MA\_13 AR23 M\_B\_A13  
SB\_RAS# AU23 M\_B\_RAS# 15,16  
SB\_RCVENIN# AK18  
SB\_RCVENOUT# AK18  
SB\_WE# AR27 M\_B\_WE# 15,16

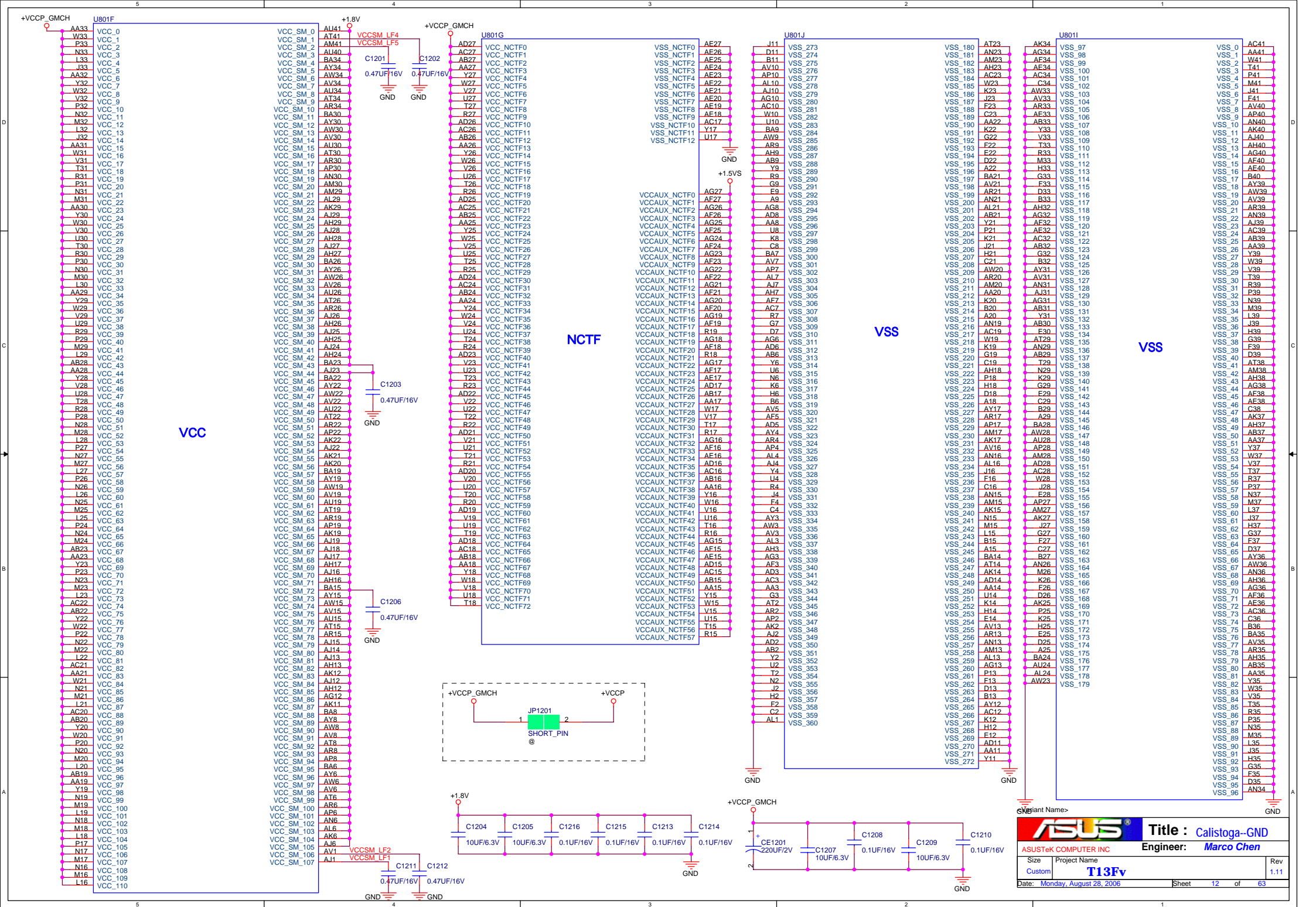
&lt;Variant Name&gt;

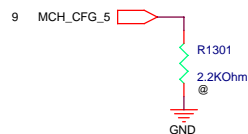
Title : Calistoga--DDR2  
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11
Date: Monday, August 28, 2006	Sheet 10 of 63	



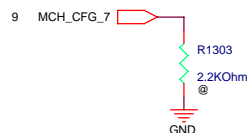
POWER





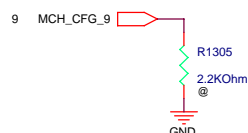
#### CFG5 : DMI STRAP

LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**



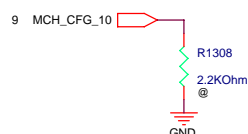
#### CFG7 : CPU STRAP

LOW = RESERVED  
**HIGH = Mobile Yonah CPU (Default)**



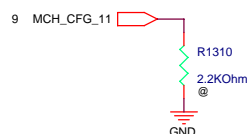
#### CFG9 : PCIE GRAPHIC LANE

**LOW = REVERSE LANE**  
 HIGH = NORMAL OPERATION (Default)



#### CFG10 : HOST PLL VCO SELECT

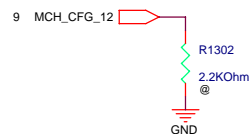
LOW = RESERVED  
**HIGH = MOBILITY (Default)**



#### CFG11 : PSB 4x CLK ENABLE

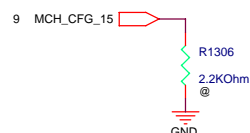
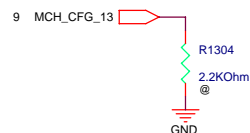
LOW = 4X ENABLED  
**HIGH = 8X ENABLED (Default)**

CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.



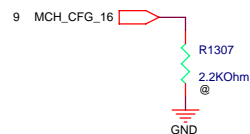
#### CFG[13:12] : GMCH TEST MODE SELECT

00 = Partial CLK gating disable  
 01 = XOR Mode Enable  
 10 = ALL Z Mode Enable  
**11 = NORMAL OPERATION (Default)**



#### CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled  
**HIGH = Normal Operation (Default)**



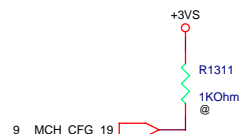
#### CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**



#### CFG18 : GMCH Core Voltage Level

**LOW = 1.05V (Default)**  
 HIGH = 1.5V



#### CFG19 : DMI LANE REVERSAL

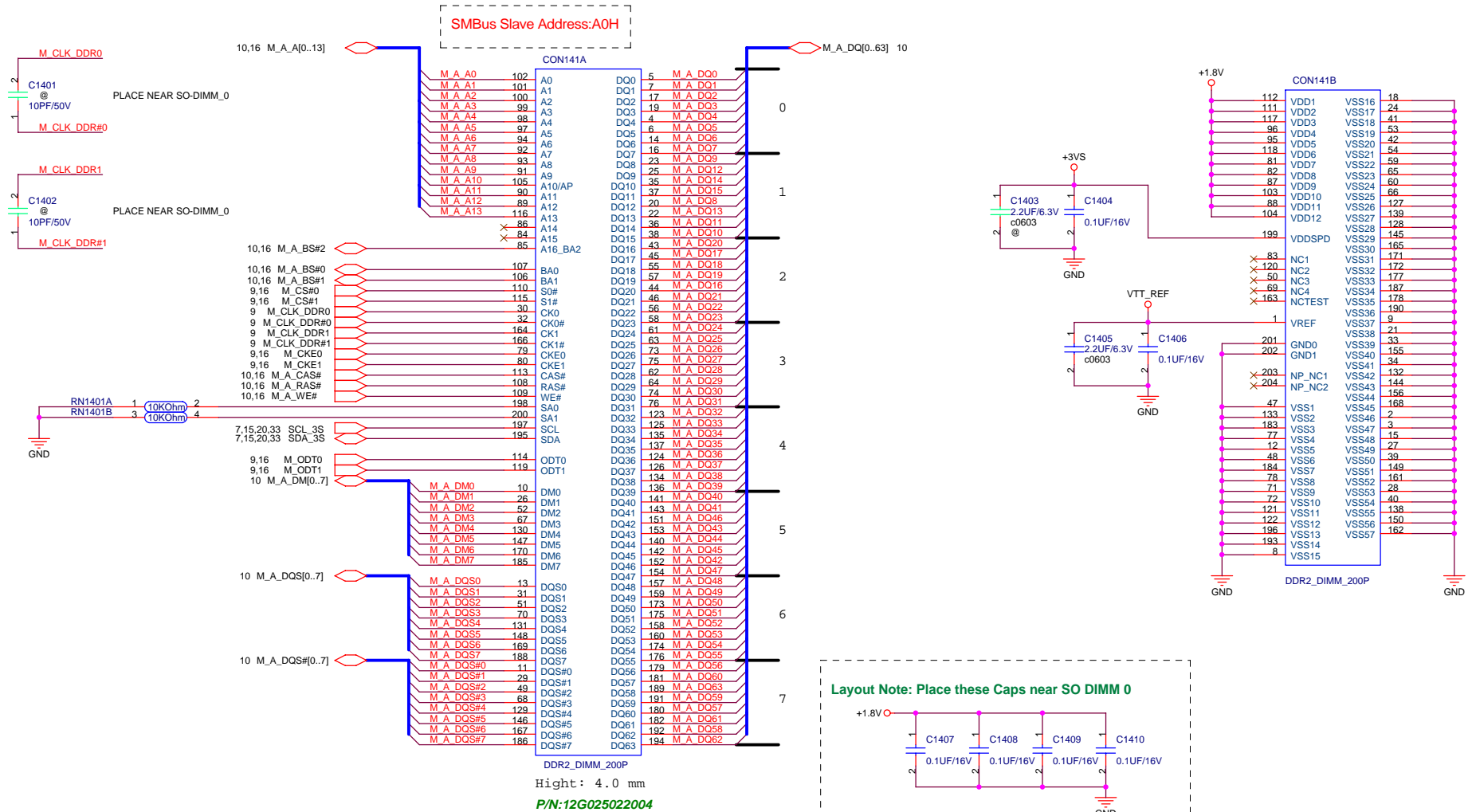
**LOW = NORMAL (Default)**  
 HIGH = LANES REVERSED

<Variant Name>

		Title : Calistoga--Strap	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13Fv	1.11	
Date: Monday, August 28, 2006	Sheet 13	of 63	

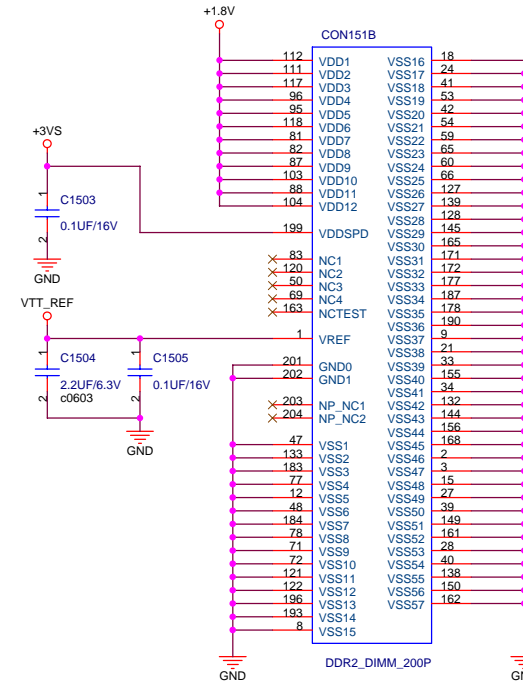
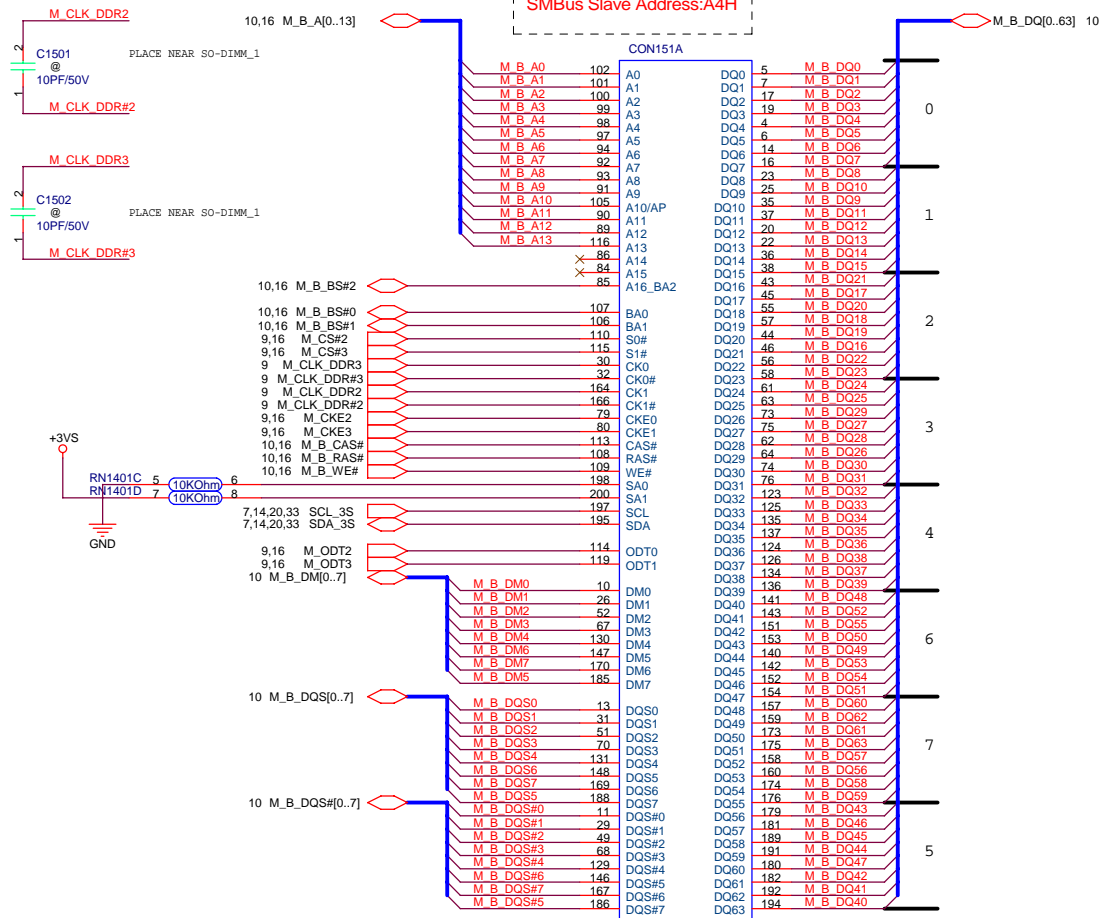


DDR2 HAD SWAPED.

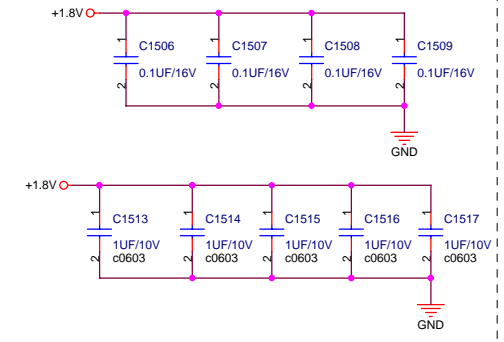


<Variant Name>

DDR2 HAD SWAPED.



Layout Note: Place these Caps near SO DIMM 1

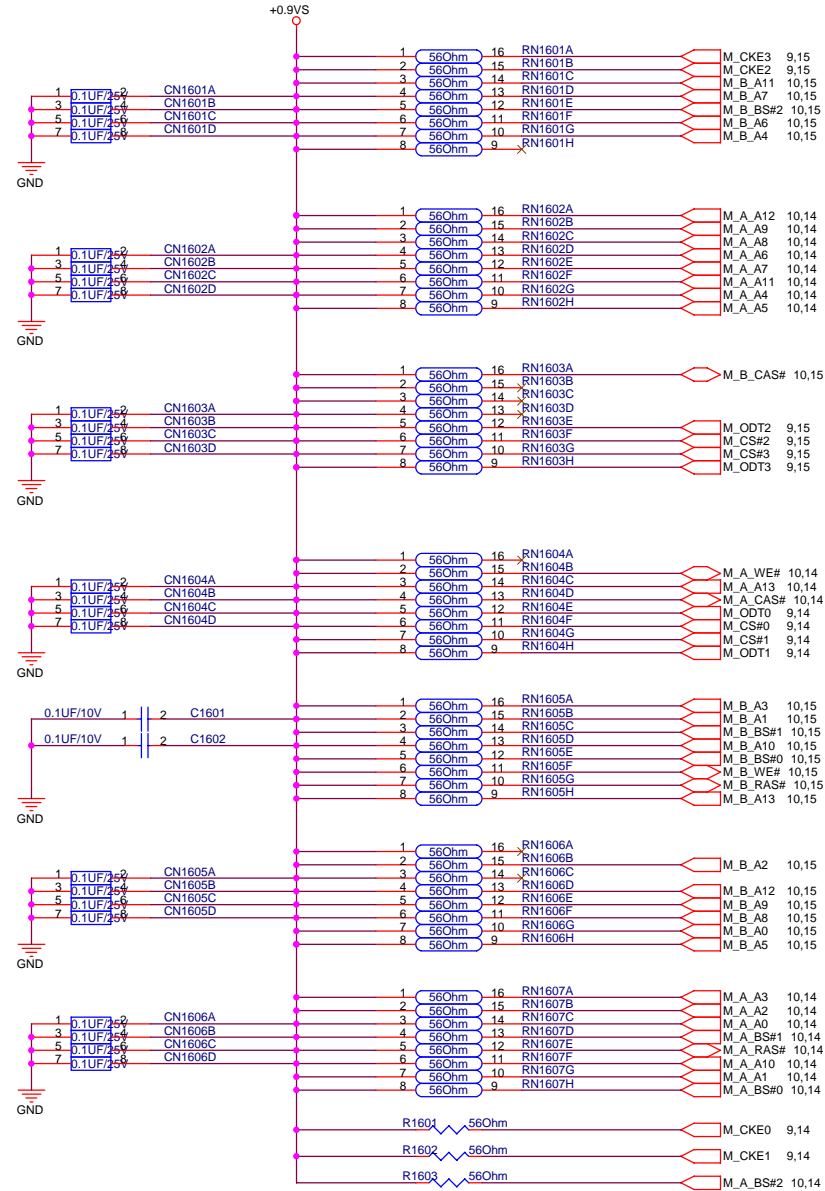


<Var Name>

<b>ASUS</b>		Title : <b>DDR2 SO-DIMM_1</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size	Project Name	Rev	
Custom	<b>T13Fv</b>	1.11	
Date: Monday, August 28, 2006		Sheet 15 of 63	



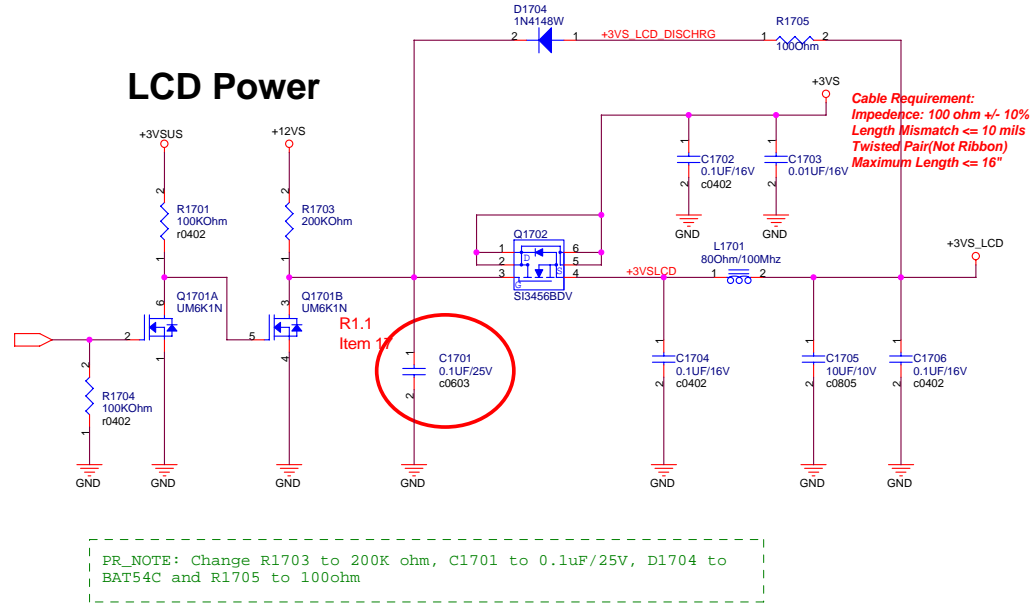
DDR2 HAD SWAPED.



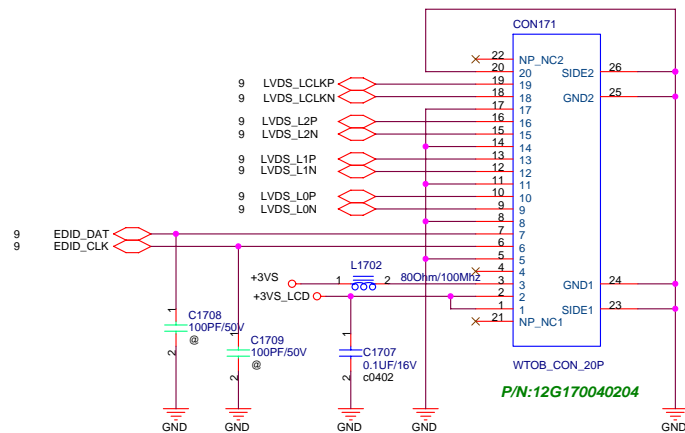
Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

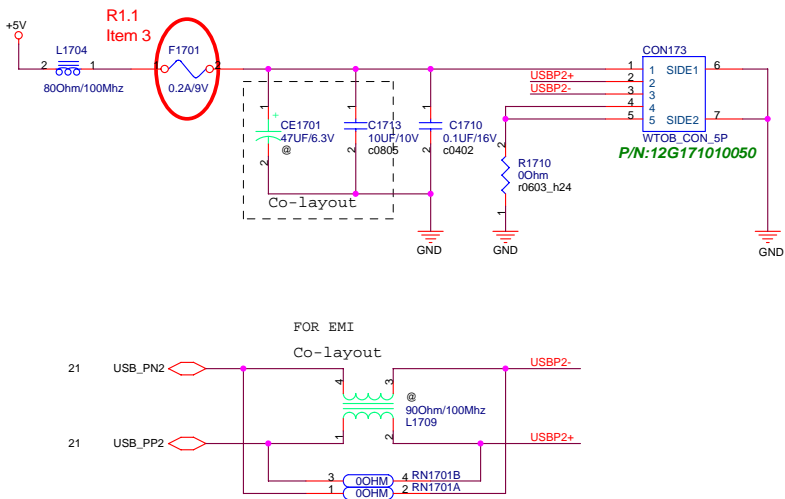
LCD Backlight Control



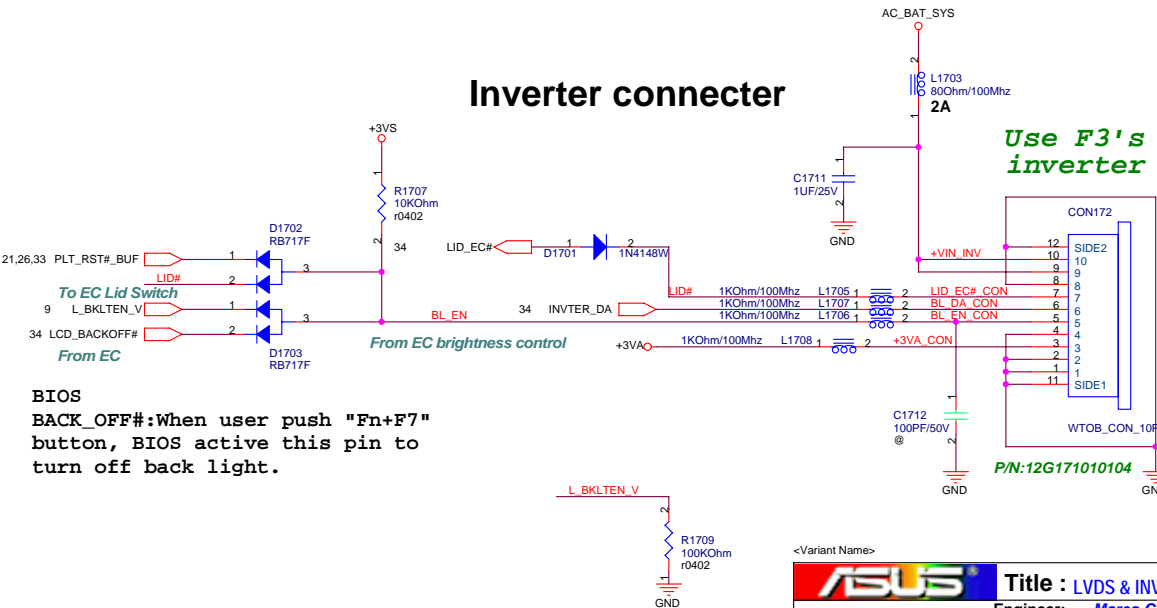
LCD LVDS Interface



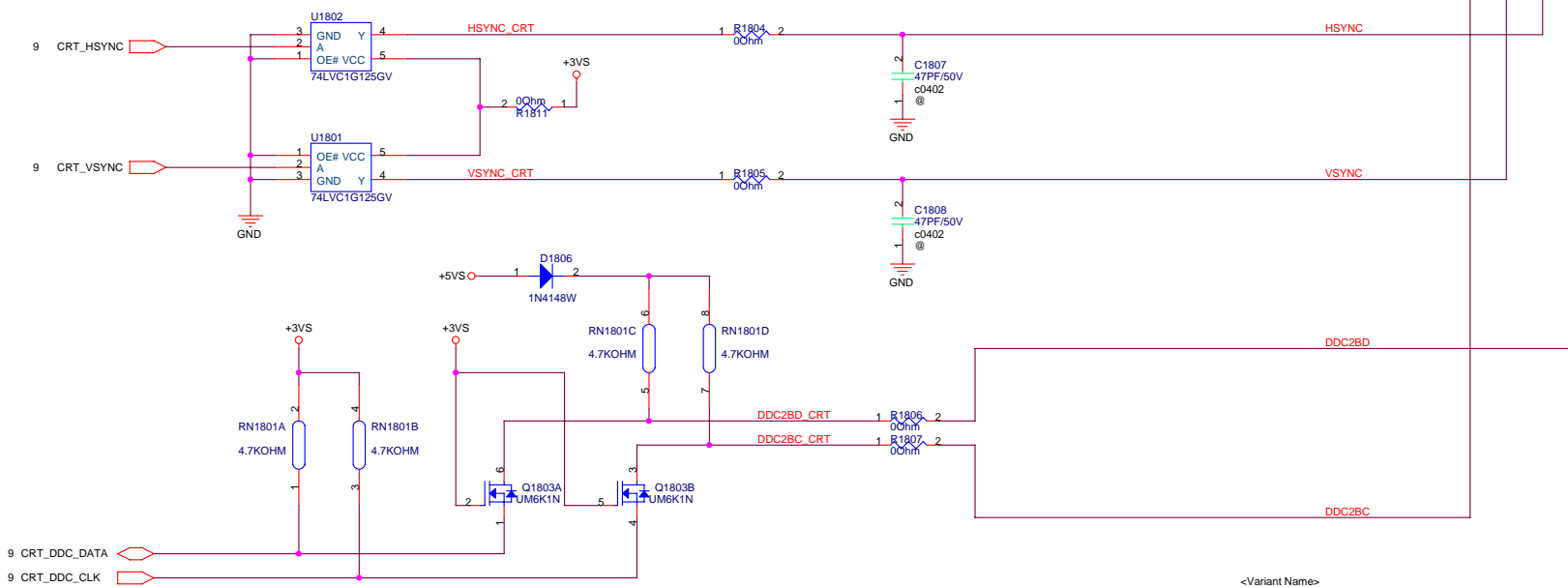
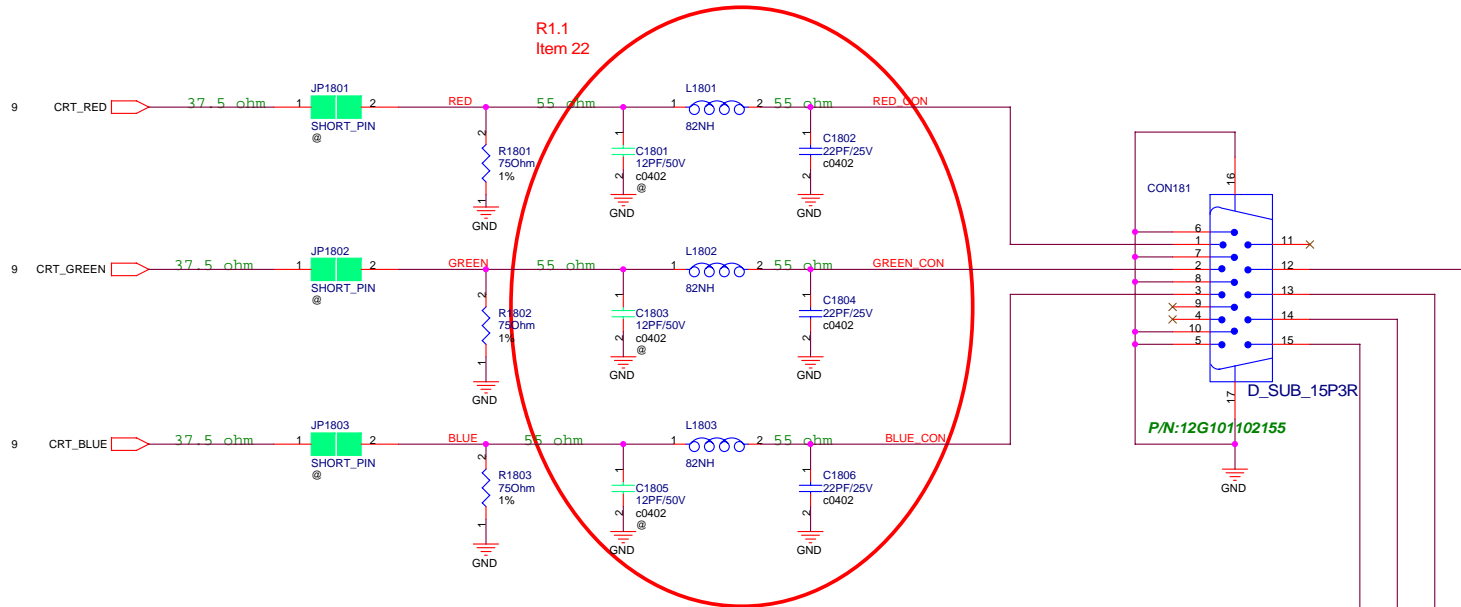
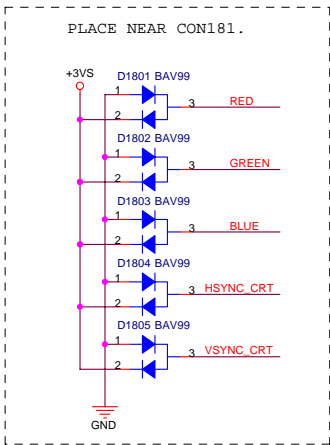
CCD connector



Inverter connector

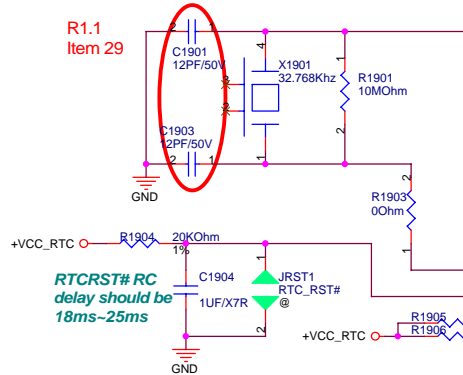


***CRT***



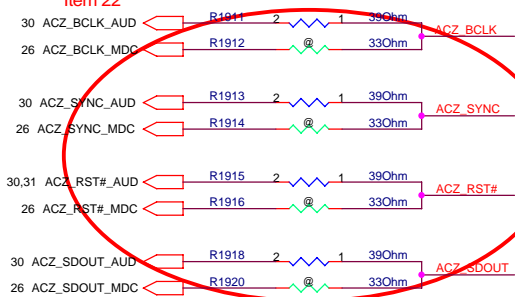
Request of CSC for CMOS clear function

R1.1  
Item 29



RTC\_RST# RC delay should be 18ms-25ms

R1.1  
Item 22



ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

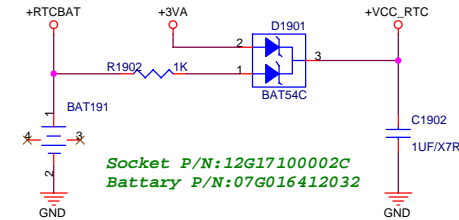
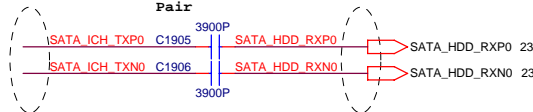
ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

ACZ\_RST#

Differential Pair



Socket P/N:12G17100002C  
Battery P/N:07G016412032

U1901A

RTC X1

RTC X2

AA3

Y5

W4

Int.PD W1

Int.PD Y1

Int.PD Y2

Int.PD W3

Int.PD V3

Int.PD U3

Int.PD U5

Int.PD V4

Int.PD T5

Int.PD U7

Int.PD V6

Int.PD V7

Int.PD U1

Int.PD R6

Int.PD T2

Int.PD T3

Int.PD T1

Int.PD T4

Int.PD AF18

Int.PD AF3

Int.PD AF3

Int.PD AG2

Int.PD AH2

Int.PD AE7

Int.PD AE6

Int.PD AH6

Int.PD AF1

Int.PD AE1

Int.PD AH10

Int.PD AG10

Int.PD AF15

Int.PD AH15

Int.PD AE16

Int.PD AH16

Int.PD AG16

Int.PD IE15

Int.PD IE15

Int.PD IE15

Int.PD IE15

Int.PD IE15

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Int.PD IE15

Int.PD IE15

Int.PD IE15

ICH7M

LAD0

LAD1

LAD2

LAD3

LDRQ0#

LDRQ1#/GPIO23

LFRAME#

A20GATE

A20M#

CPUSLP#

TP1/DPRSTP#

TP2/DPSLP#

FERR#

GPIO49/CPUPWRGD

IGNNE#

INIT3\_3V#

INIT#

INTR#

RCIN#

NMI

SMI#

STPCLK#

THERMTRIP#

DD0

DD1

DD2

DD3

DD4

DD5

DD6

DD7

DD8

DD9

DD10

DD11

DD12

DD13

DD14

DD15

DA0

DA1

DA2

DCS1#

DCS3#

DCS1#

DCS3#

DCS1#

DCS3#

DCS1#

DCS3#

DCS1#

DCS3#

DCS1#

DCS3#

DCS1#

DCS3#

AA6

AB5

AC4

Y6

AC3

AA5

AB3

AE22

AH28

AG27

AF24

AH25

AG26

AG24

AG22

AG21

AE22

AF25

AG23

AH24

AF23

AH22

AF26

AB15

AE14

AG13

AF13

AD14

AC13

AD12

AC12

AE12

AF12

AB13

AC14

AF14

AH13

AH14

AC15

AH17

AE17

AF17

AE16

AD16

AE16

AD16

AE16

AD16

AE16

AD16

AE16

AD16

AE16

AD16

AE16

AD16

AE16

LPC

LPC\_AD0

LPC\_AD1

LPC\_AD2

LPC\_AD3

LPC\_FRAME#

A20GATE

H\_A20M#

H\_CPUSLP#

H\_DPRSTP#

H\_DPSLP#

H\_FERR#

H\_PWRGD

H\_IGNNE#

H\_INIT#

H\_INTR#

H\_RCIN#

H\_NMI

H\_SMI#

H\_STPCLK#

H\_THRMTRIP#

IDE\_PDD0

IDE\_PDD1

IDE\_PDD2

IDE\_PDD3

IDE\_PDD4

IDE\_PDD5

IDE\_PDD6

IDE\_PDD7

IDE\_PDD8

IDE\_PDD9

IDE\_PDD10

IDE\_PDD11

IDE\_PDD12

IDE\_PDD13

IDE\_PDD14

IDE\_PDD15

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

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IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

IDE\_PDD[15:0]

AA6

AB5

AC4

Y6

AC3

AA5

AB3

AE22

AH28

AG27

AF24

AH25

AG26

AG24

AG22

AG21

AE22

AF25

AG23

AH24

AF23

AH22

AF26

AB15

AE14

AG13

AF13

AD14

AC13

AD12

AC12

AE12

AF12

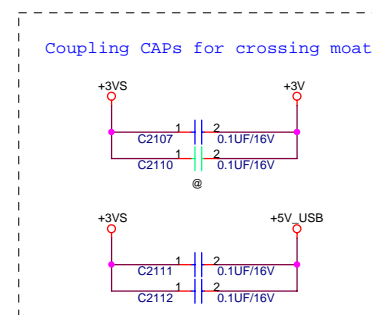
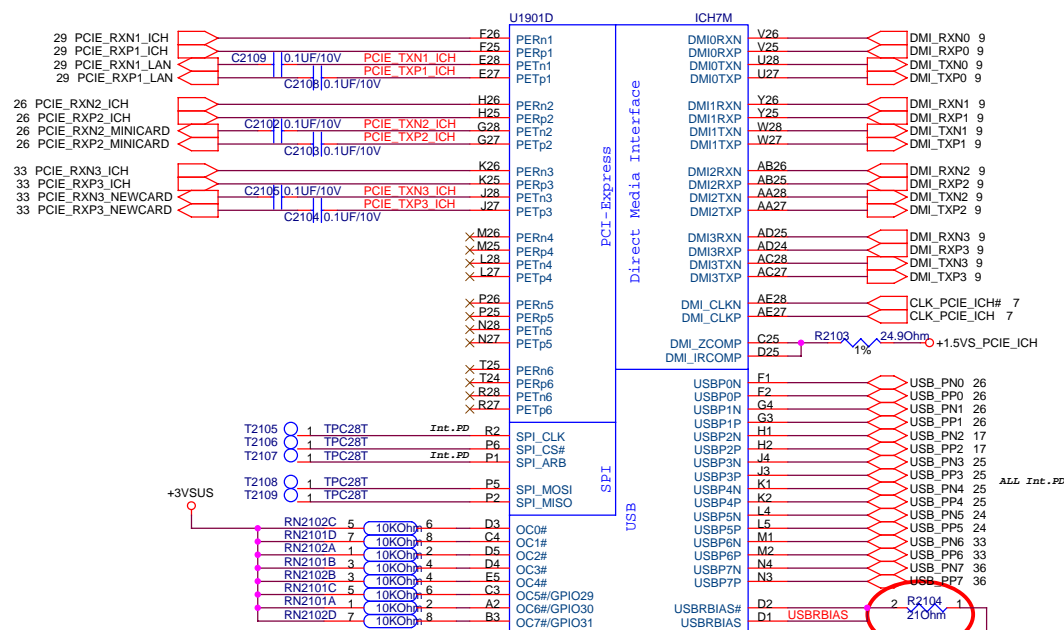
AB13

AC14

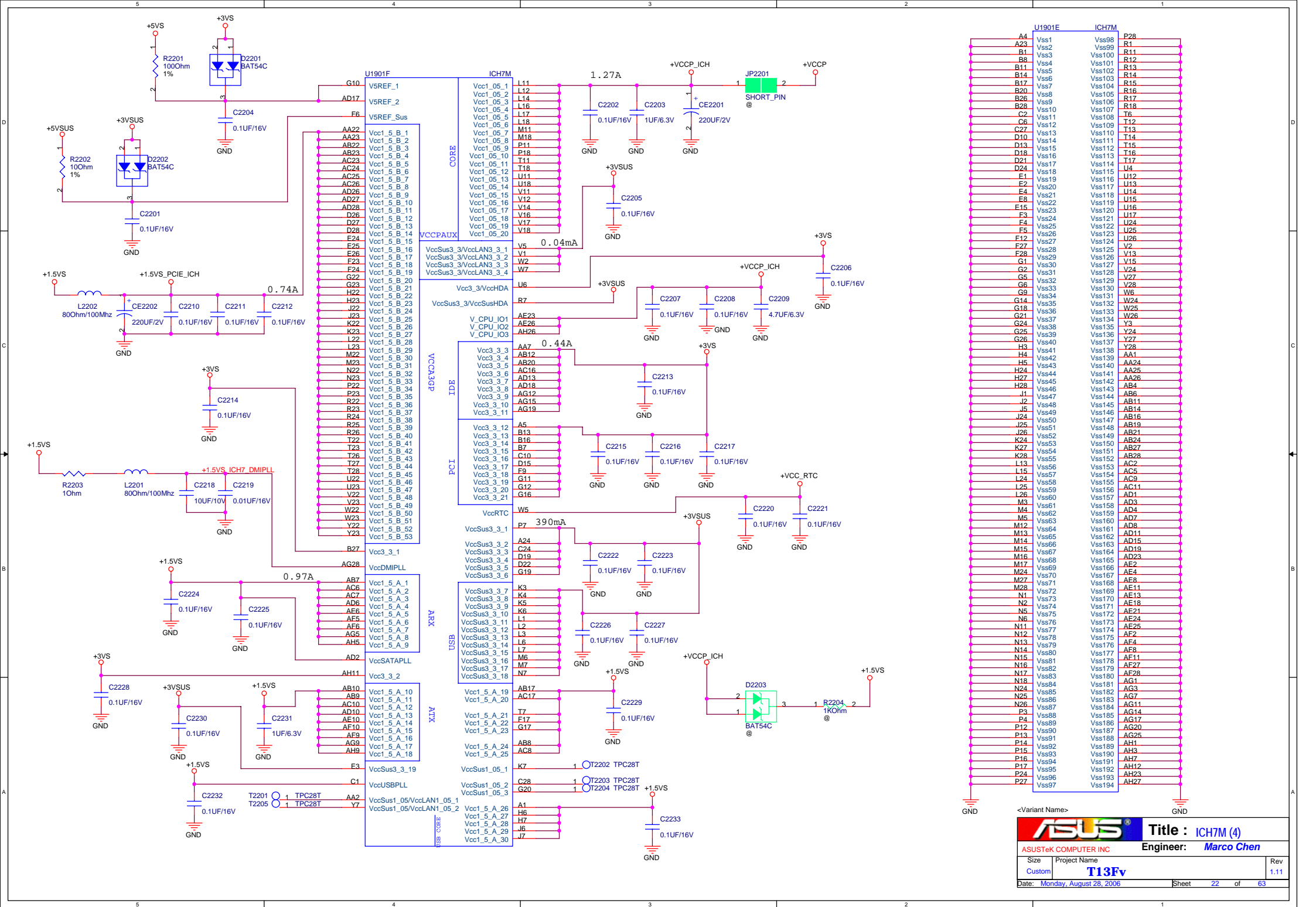
AF14

AH13</



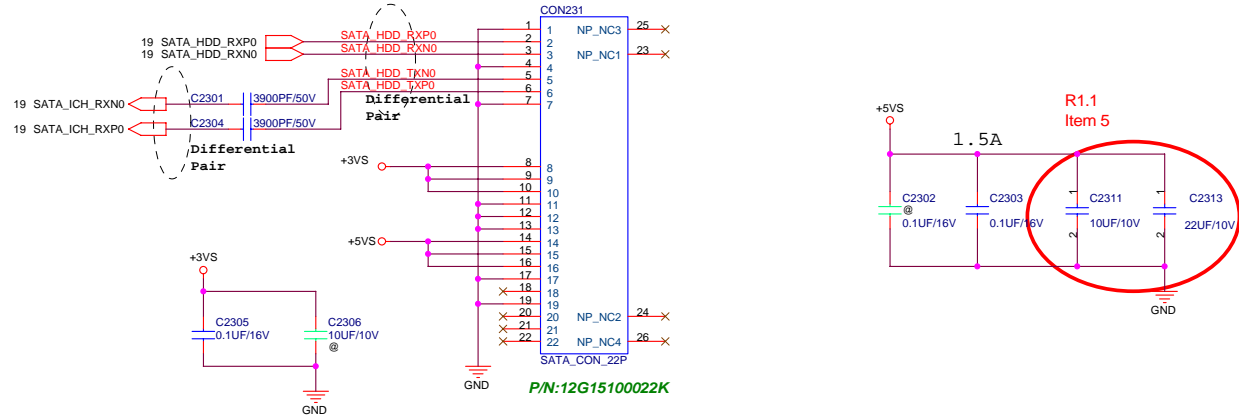


USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER

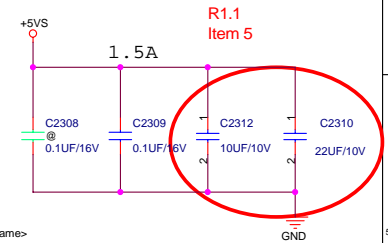
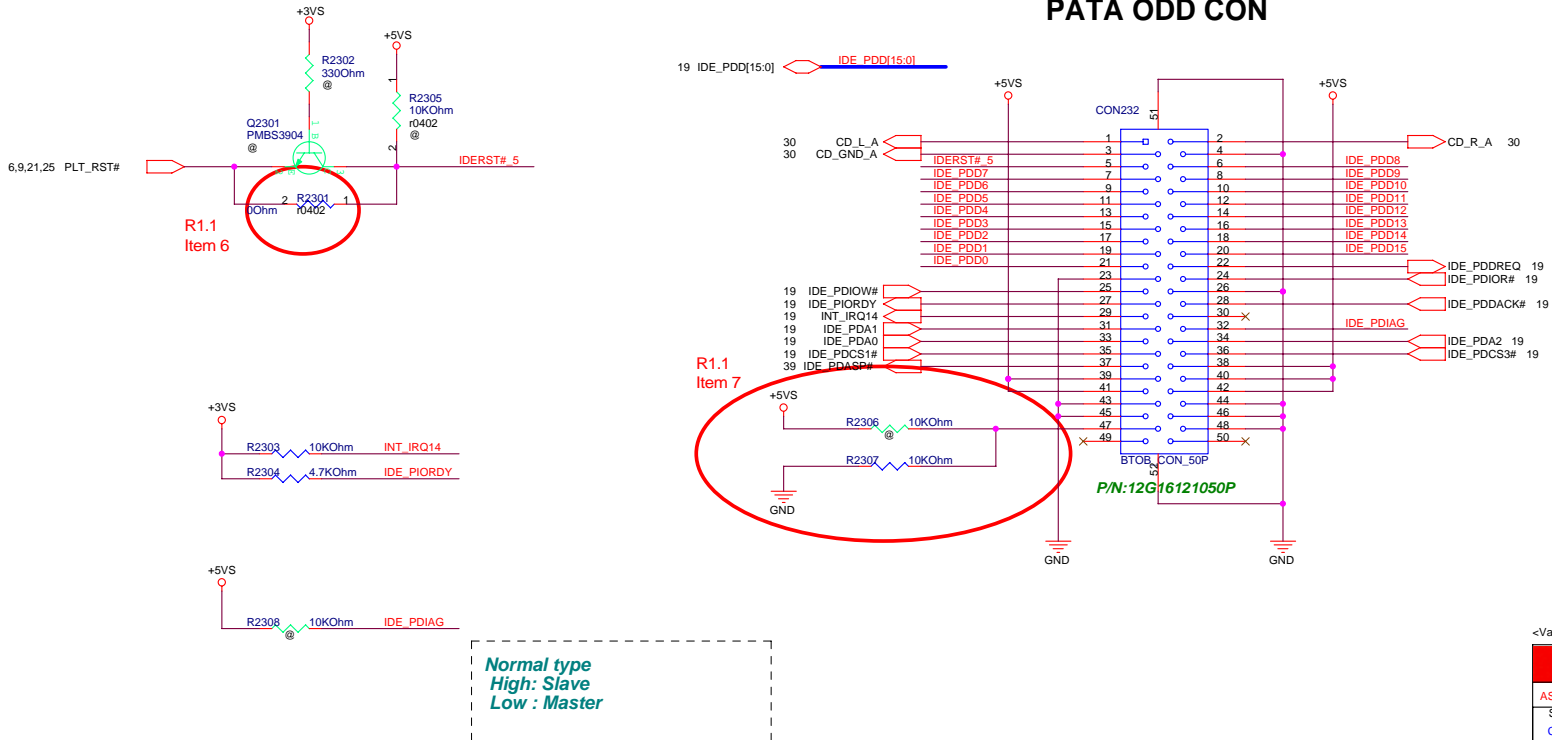


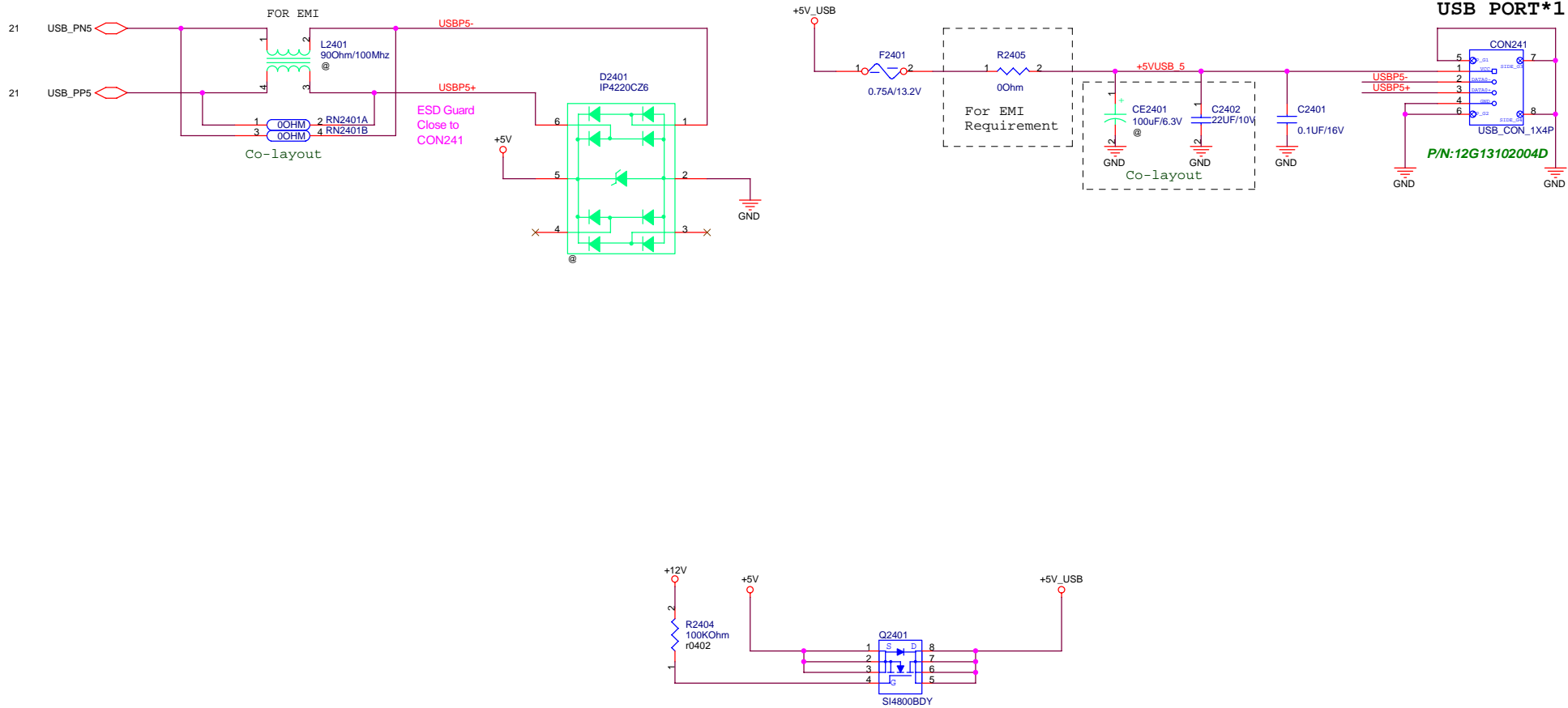


## SATA HDD CON




## PATA ODD CON





<Variant Name>

		<b>Title :</b> USB PORT	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Marco Chen	
Size Custom	Project Name <b>T13Fv</b>		Rev 1.11
Date: Monday, August 28, 2006		Sheet	24 of 63

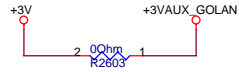
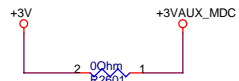


**POWER CONSUMPTION:**  
**+3VS: +3.003V~+3.597V**  
**Max= 750 mA**

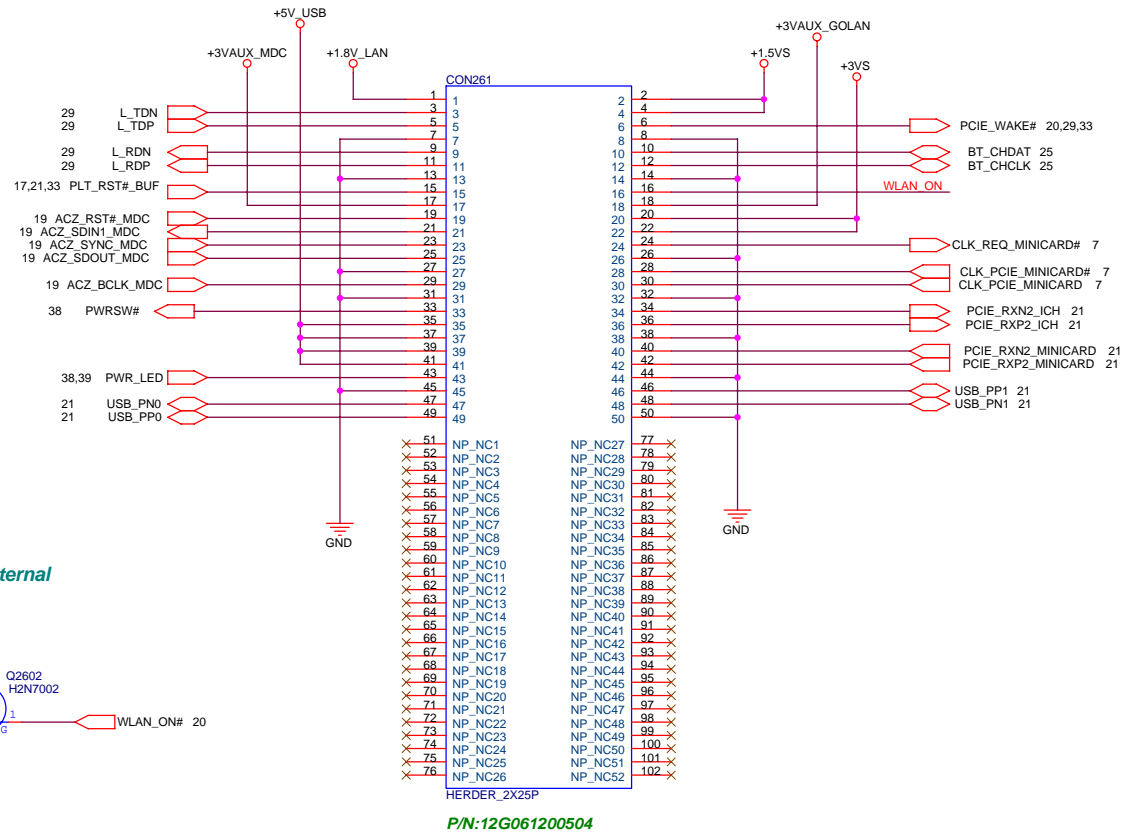
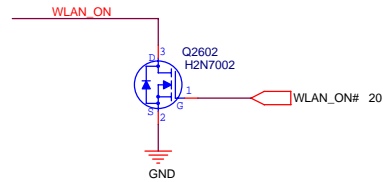
**+1.5VS: +1.425V~+1.575V**  
**Max= 375 mA**

**+3VAUX\_GOLAN: +3.003V~+3.597V**  
**Max= 250 mA**

**+3VAUX\_MDC: +3.003V~+3.597V**  
**Max= 300 mA**

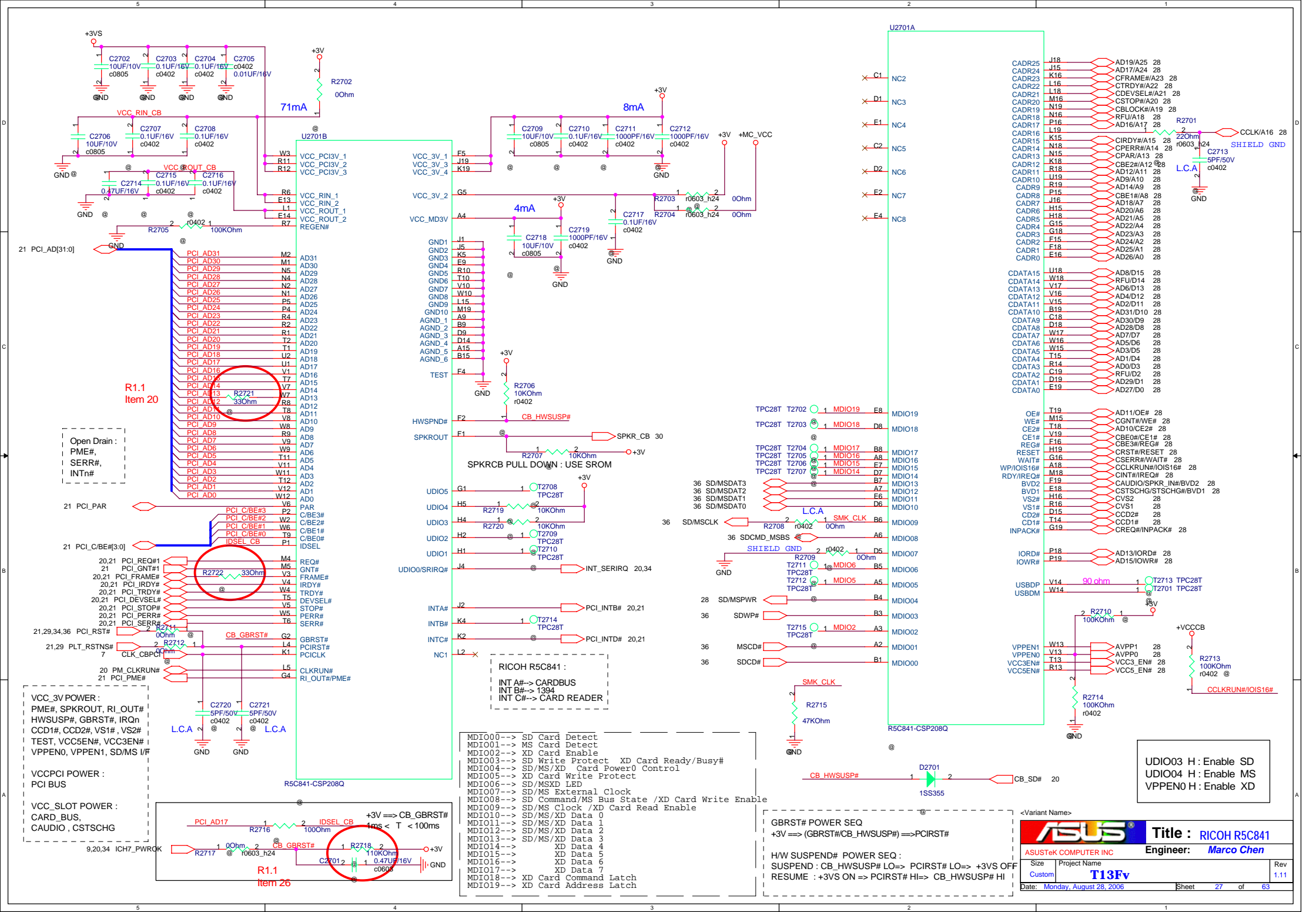


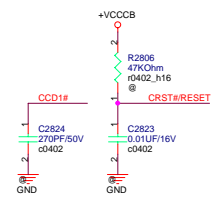
**Intel SPEC(18780):Internal  
Pull UP 110Kohm**



<Variant Name>

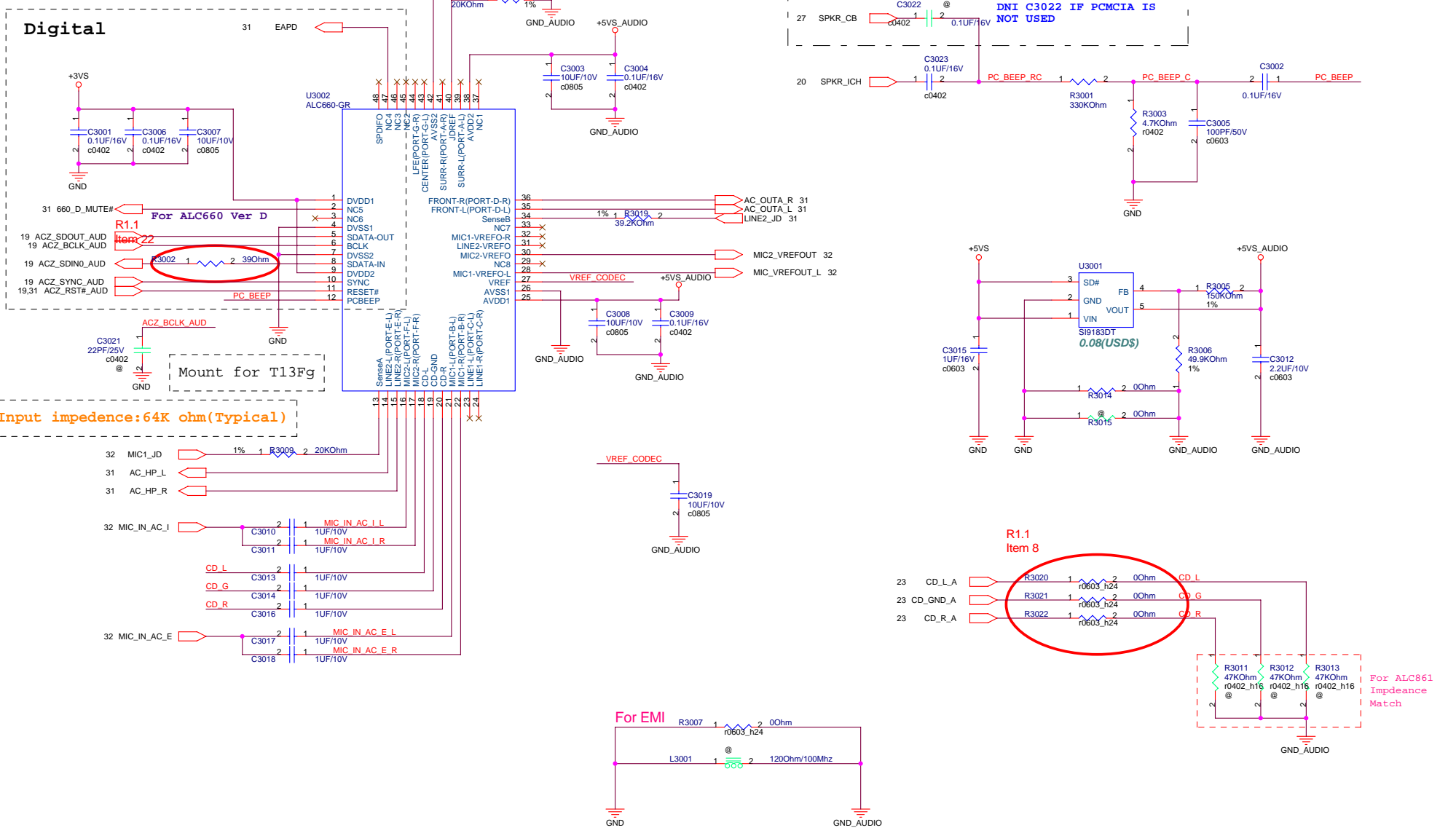
<b>ASUS</b>		<b>Title : B TO B CONN(M)</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size Custom	Project Name <b>T13Fv</b>	Rev 1.11	
Date: Monday, August 28, 2006		Sheet 26 of 63	



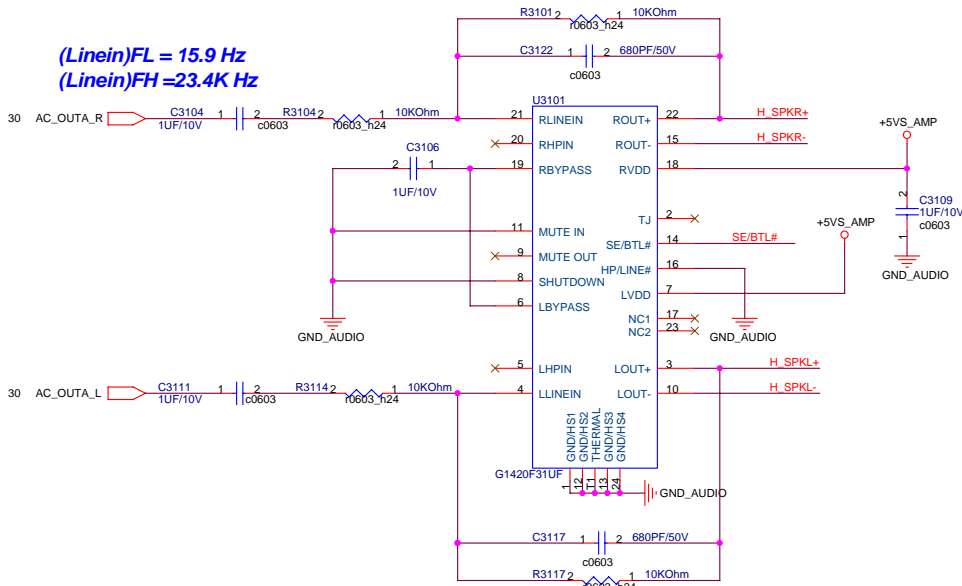




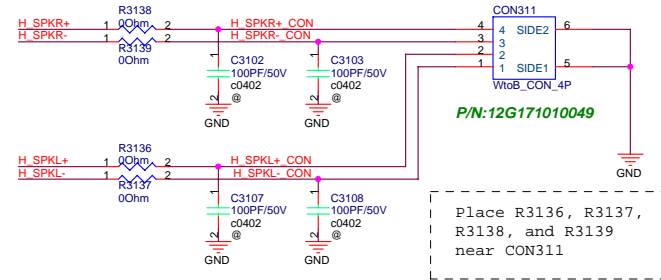
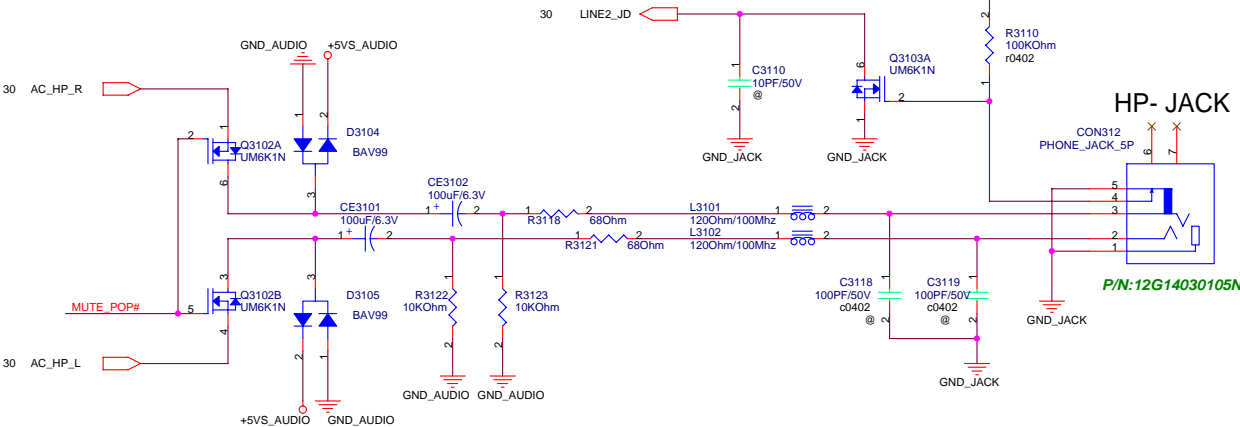
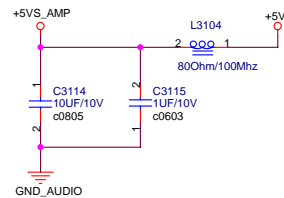
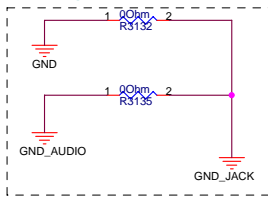




(Linein)FL = 15.9 Hz  
(Linein)FH = 23.4K Hz

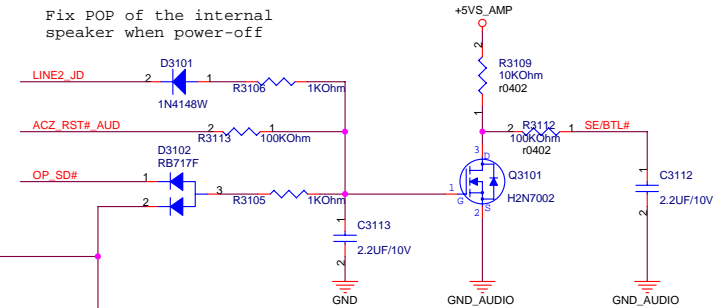


EMI Request



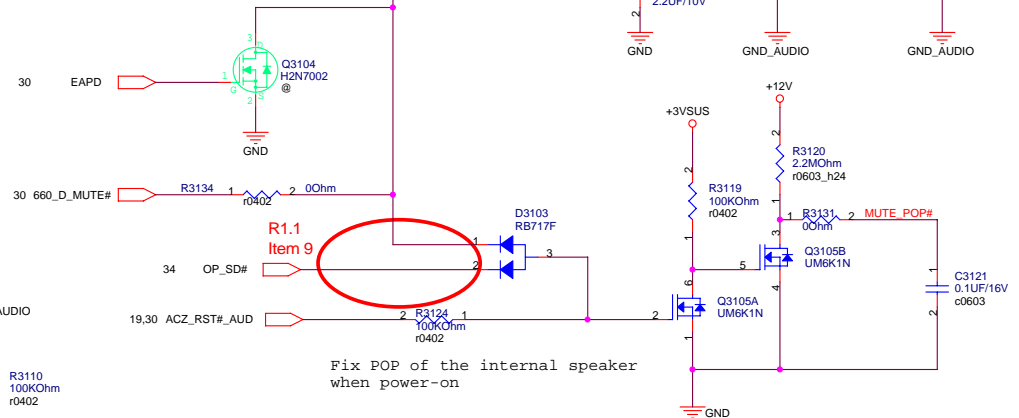
Place R3136, R3137,  
R3138, and R3139  
near CON311

Fix POP of the internal  
speaker when power-off



Fix POP of the internal  
speaker when power-on

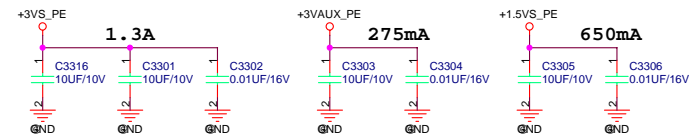
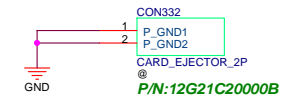
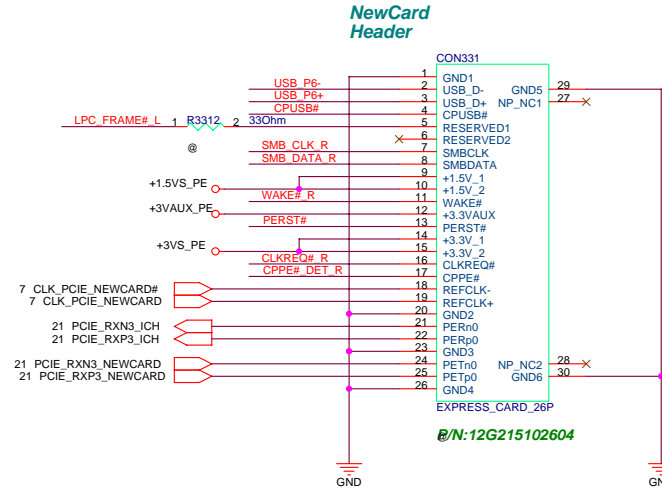
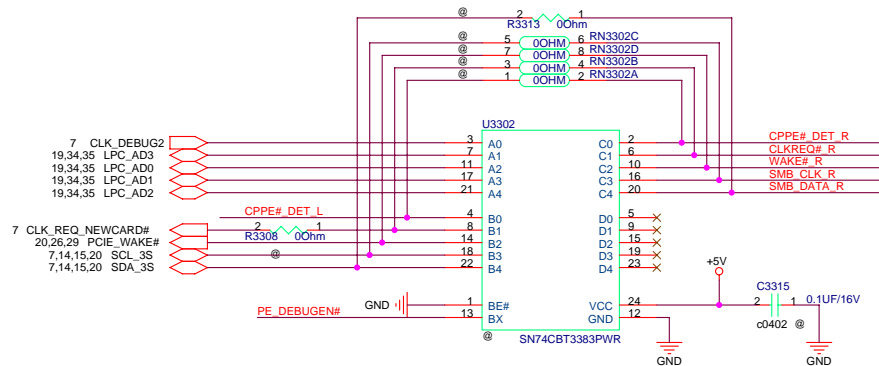
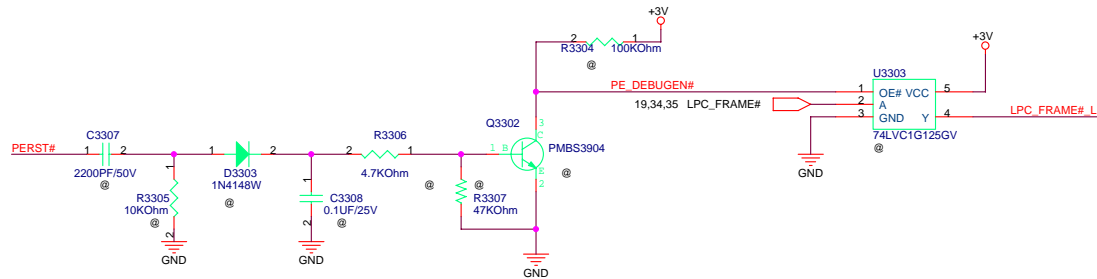
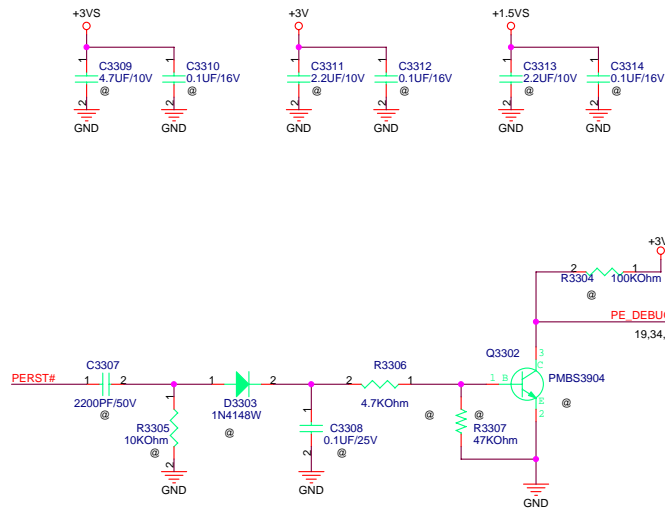
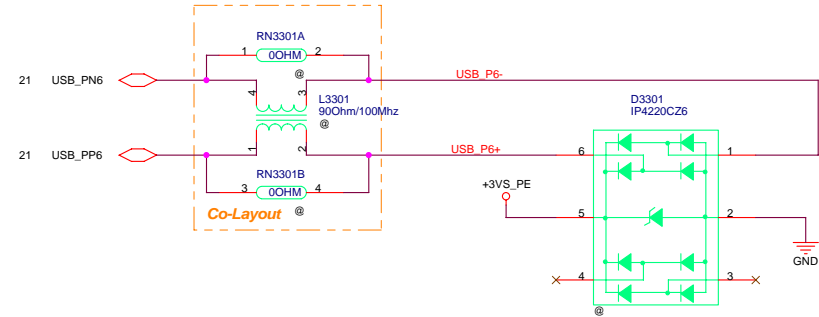
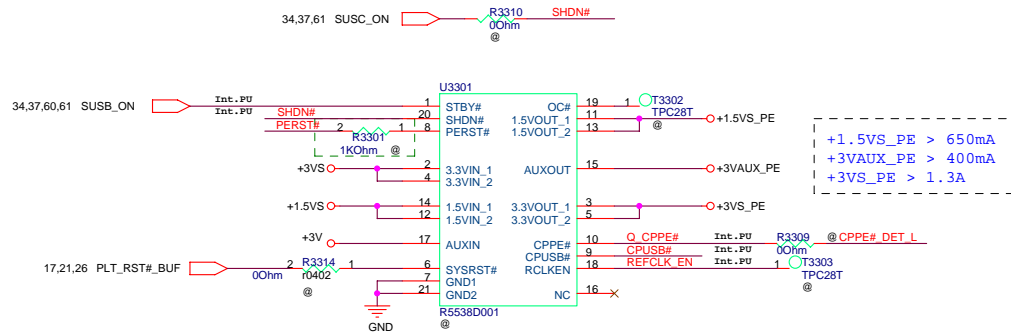
HP- JACK




<Variant Name>

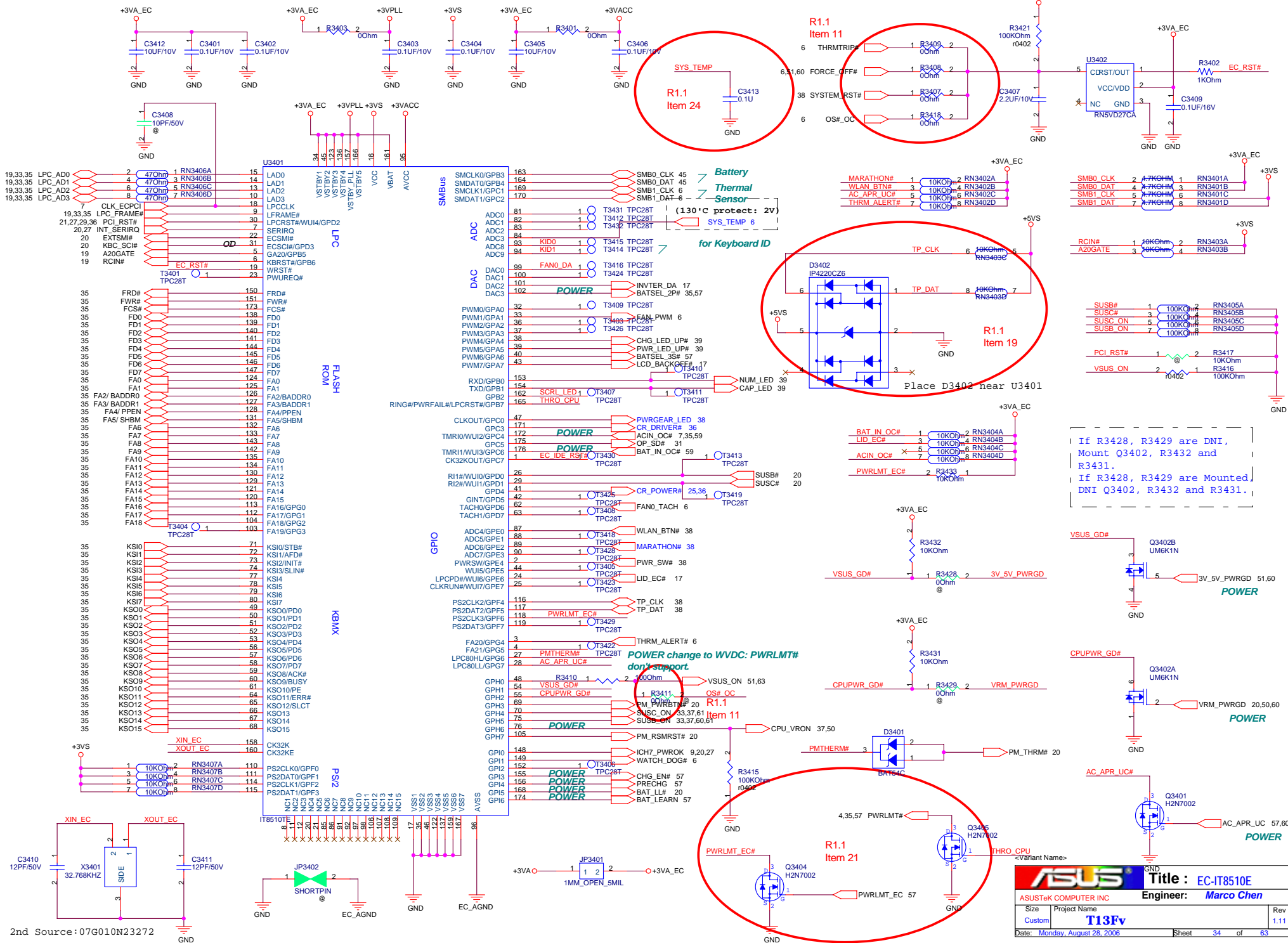
		Title : G1420	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13Fv		Rev 1.11
Date: Monday, August 28, 2006		Sheet 31	of 63





<Variant Name>

		Title : <b>NEWCARD</b>	
ASUSTek COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size	Project Name		Rev
Custom	<b>T13Fv</b>		
Date: Monday, August 28, 2006		Sheet 33 of 63	1.11

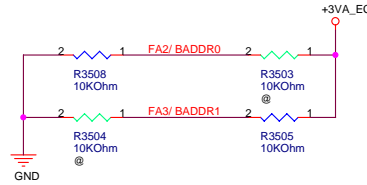


2nd Source: 07G010N23272

## EC Hardware Strapping

### FA2/ BADDR0 & FA3/ BADDR1

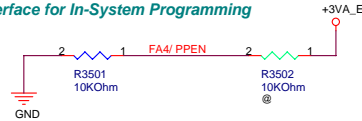
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

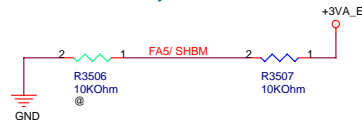
### FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

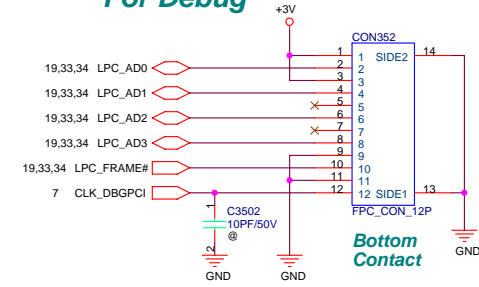


### FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

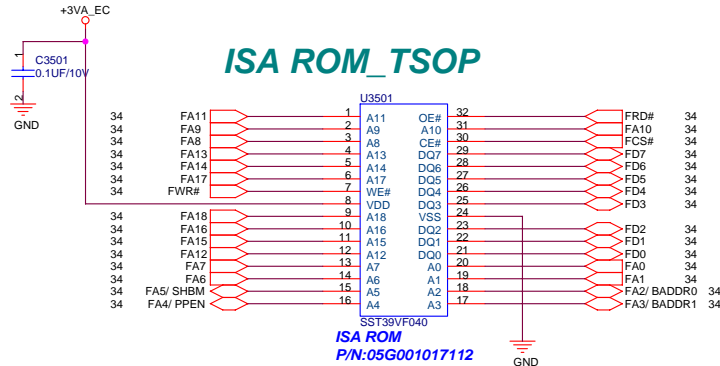


## For Debug

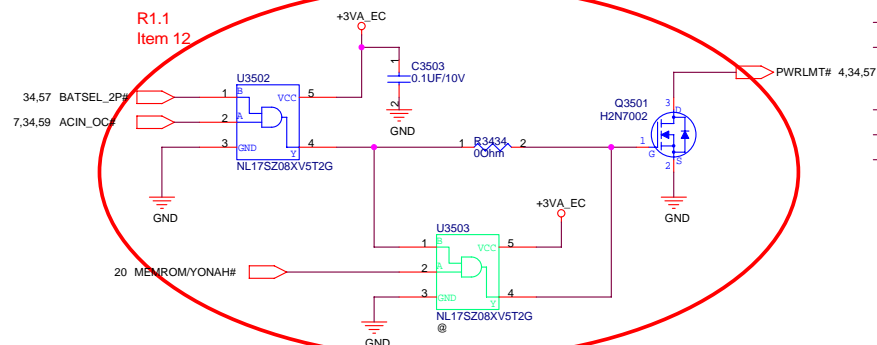


P/N:12G183301208

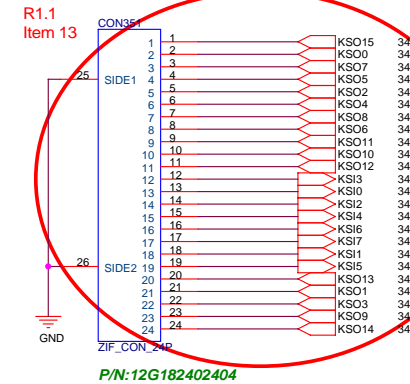
## ISA ROM\_TSOP



### R.1.1 Item 12

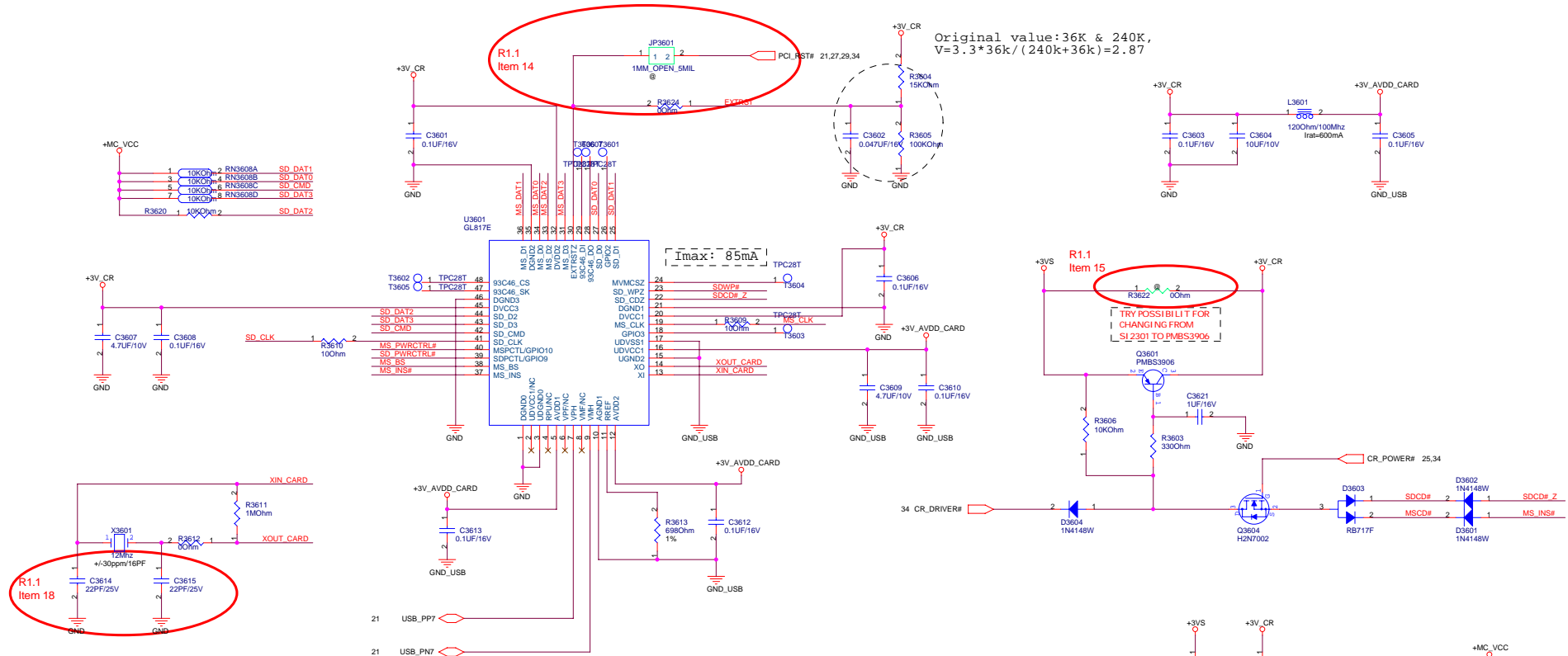


## For Keyboard

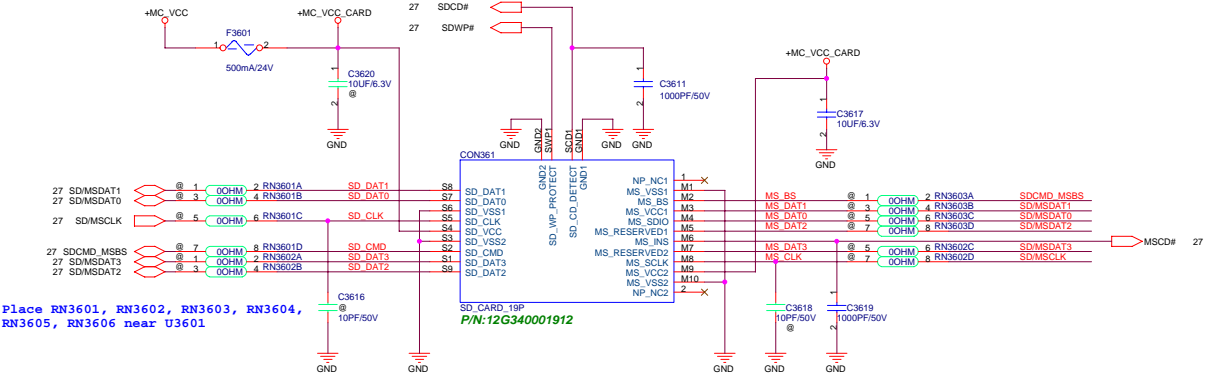


<Variant Name>

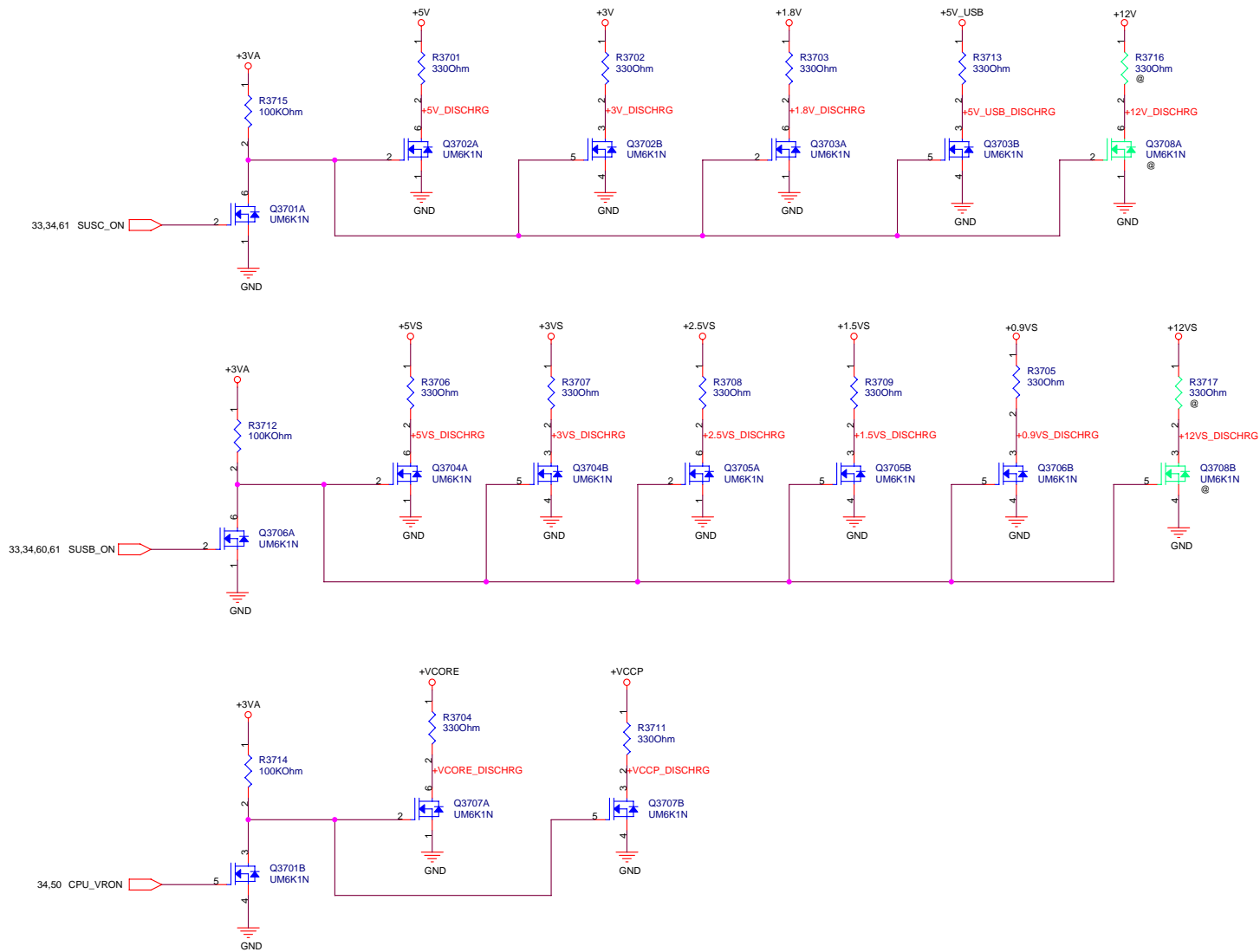
ASUS		Title :ISA_ROM&KB conn	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13Fv	1.11	
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DNI RN3601, RN3602, RN3603, RN3604, RN3605, RN3606 BY USING GL17E.



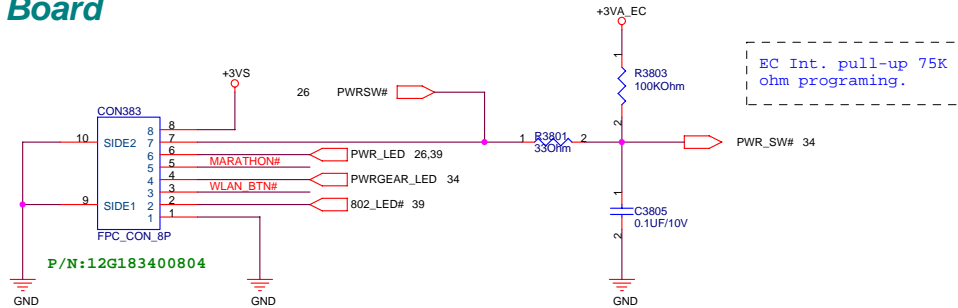
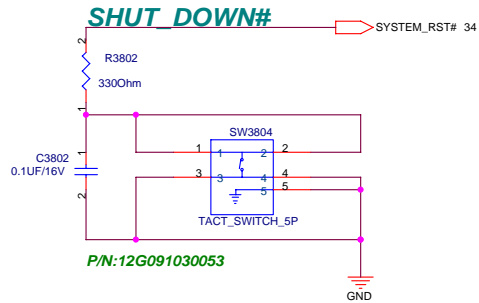




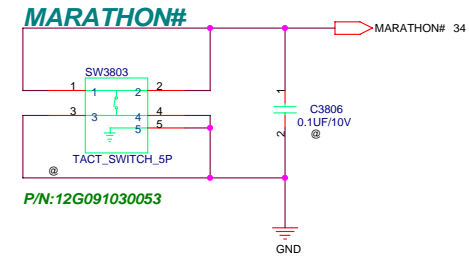
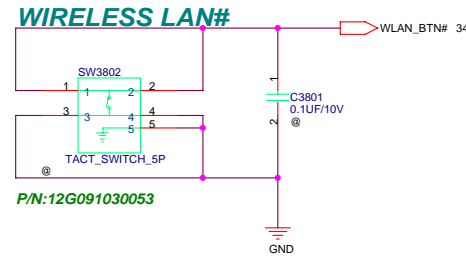
<Variant Name>

		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name <b>T13Fv</b>		Rev 1.11
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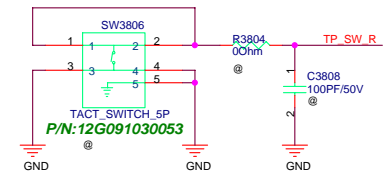
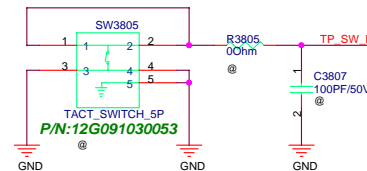
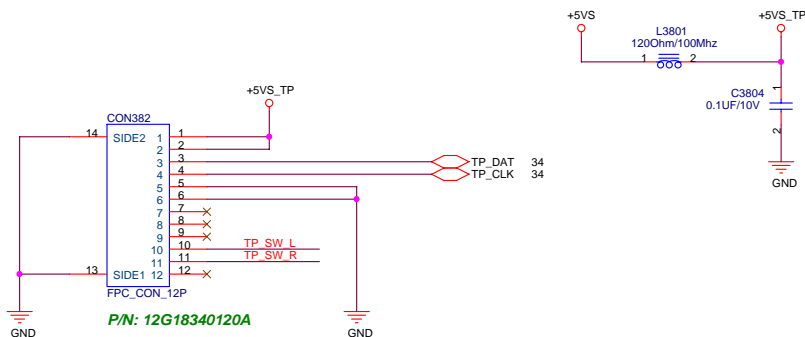
## FFC CONNECTER for T13Fv SW Board



**INSTANT KEY for T13Fg**

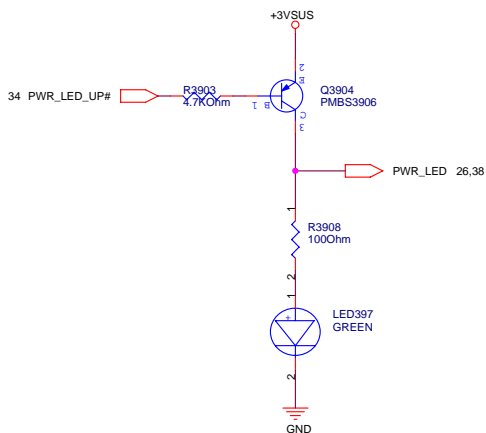


**Select Button for T13Fg**

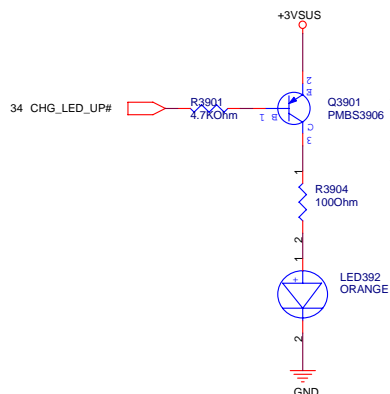


```
PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.
```

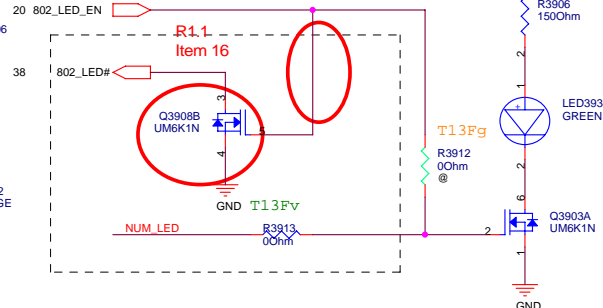
***For POWER LED***



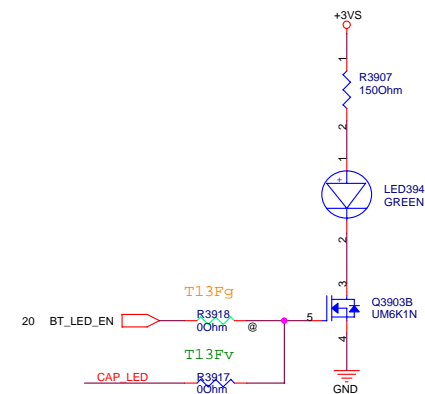
**For BATTERY LED**



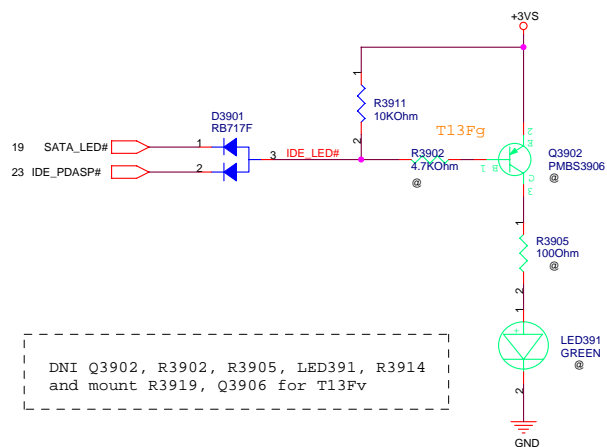
**For WireLess LED**



**For BT LED**

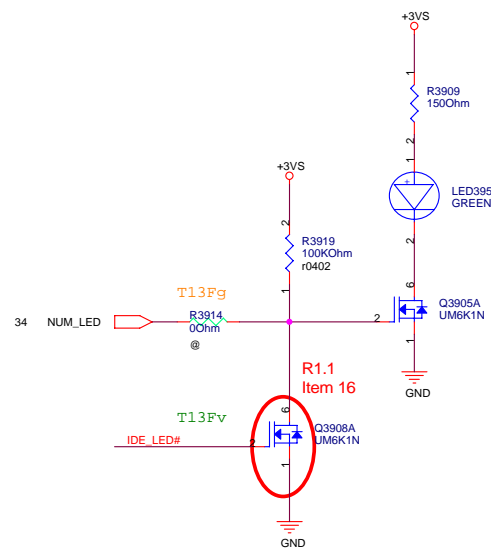


**For SATA/IDE LED**

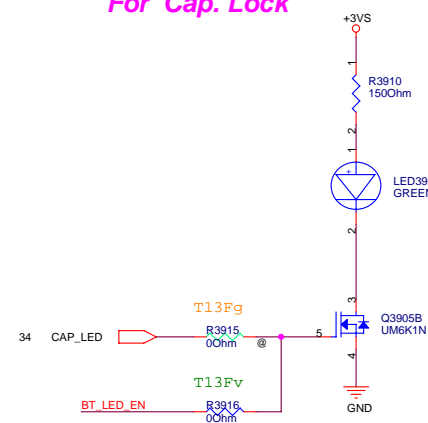


DNI Q3902, R3902, R3905, LED391, R3914  
and mount R3919, Q3906 for T13Fv

### For Num Lock



***For Cap. Lock***



3

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A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13Fv</b>
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3

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3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13Fv</b>
--------------	--------------

Rev  
1.11

Date: Monday, August 28, 2006

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3

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3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13Fv</b>
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Rev  
1.11

Date: Monday, August 28, 2006

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3

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A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13Fv</b>
--------------	--------------

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1.11

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3

(c)

3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

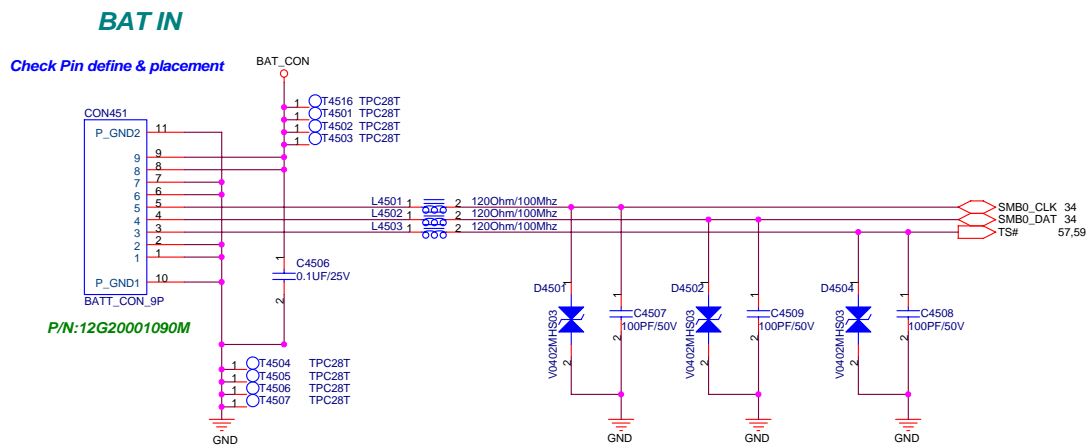
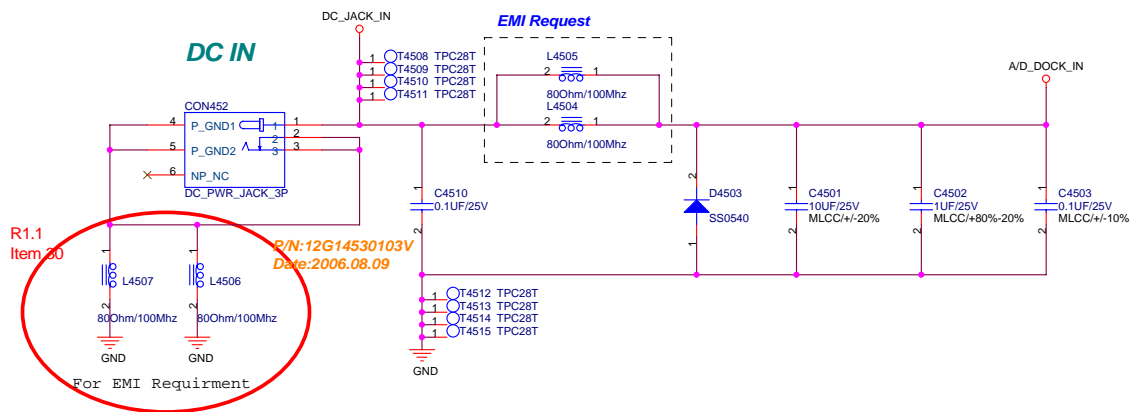
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Custom

Project Name	<b>T13Fv</b>
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Rev  
1.11

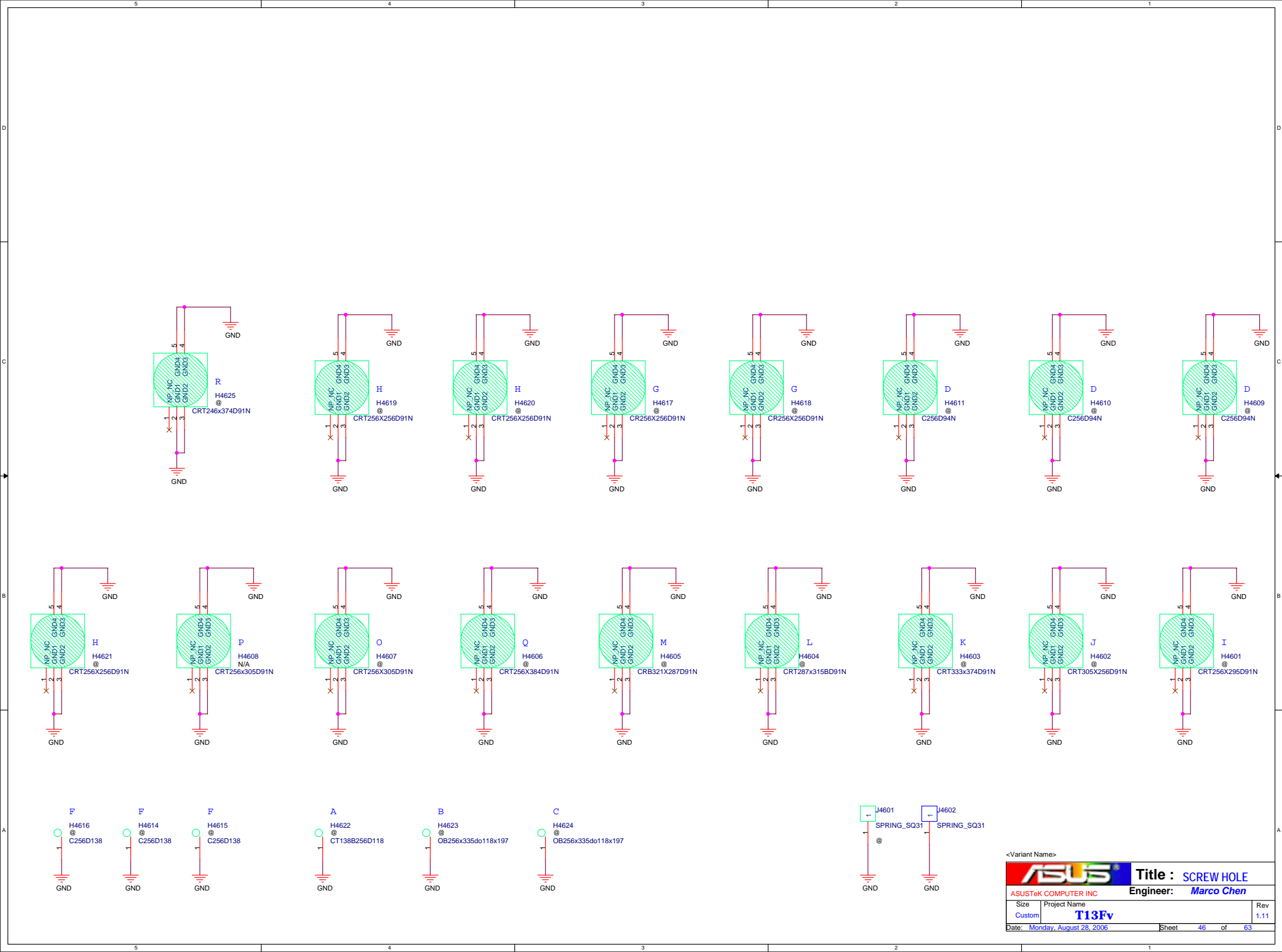
Date: Monday, August 28, 2006

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<Variant Name>

<b>ASUS</b>		<b>Title :BAT&amp;Adapter conn</b>	
ASUSTek COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size	Project Name	Rev	
Custom	<b>T13Fv</b>	1.11	
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R1.0 -> R1.1

- 1. Page 6: DNI R611 because Int. pull-up resister exists in FAN module.
- 2. Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.
- 3. Page 17: Change reference name from F3602 to F1701.
- 4. Page 21: DNI U2103.
- 5. Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.
- 6. Page 23: Change R2301 size from 0603 to 0402.
- 7. Page 23: Add pull high resister R2306\*DNI and pull down resister R2307\*Mount for ODD cable select.
- 8. Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.
- 9. Page 31: Delete R3133 and connect OP\_SD# to D3103.2 directly.
- 10. Page 32: Delete R3201 and connect MIC2\_VREFOUTto R3203.1 directly.
- 11. Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.
- 12. Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.
- 13. Page 35: Change keyboard matrix.
- 14. Page 36: Change reference name from JP3403 to JP3601
- 15. Page 36: Change R3622 size from 0402 to 0603.
- 16. Page 39: Delete R3920 and change Q3906 and Q3907\*2N7006 to Q3908\*UM6K1N.
- 17. Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.
- 18. Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.
- 19. Page 34: Add ESD Protection\*D3402 for Touch Pad.
- 20. Page 27: Add series resister 33 ohm for PCI\_FRAME# and PCI\_AD13
- 21. Page 34:Change Q3403\*\*UM6K1N to Q3404, Q3405\*2N7002.
- 22. Page 18: Change L1801, L1802, and L1803 from bead to inductor.
- 23. Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

- 24. Page 6: Change R615 pull up from +3VS to +5VS\_AUDIO.
- 25. Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.
- 26. Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.
- 27. Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.
- 28. Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.
- 29. Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.
- 30. Page 45:Add L4506 and L4507 for EMI requirement.

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A

<Variant Name>



**Title :** History(2)

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

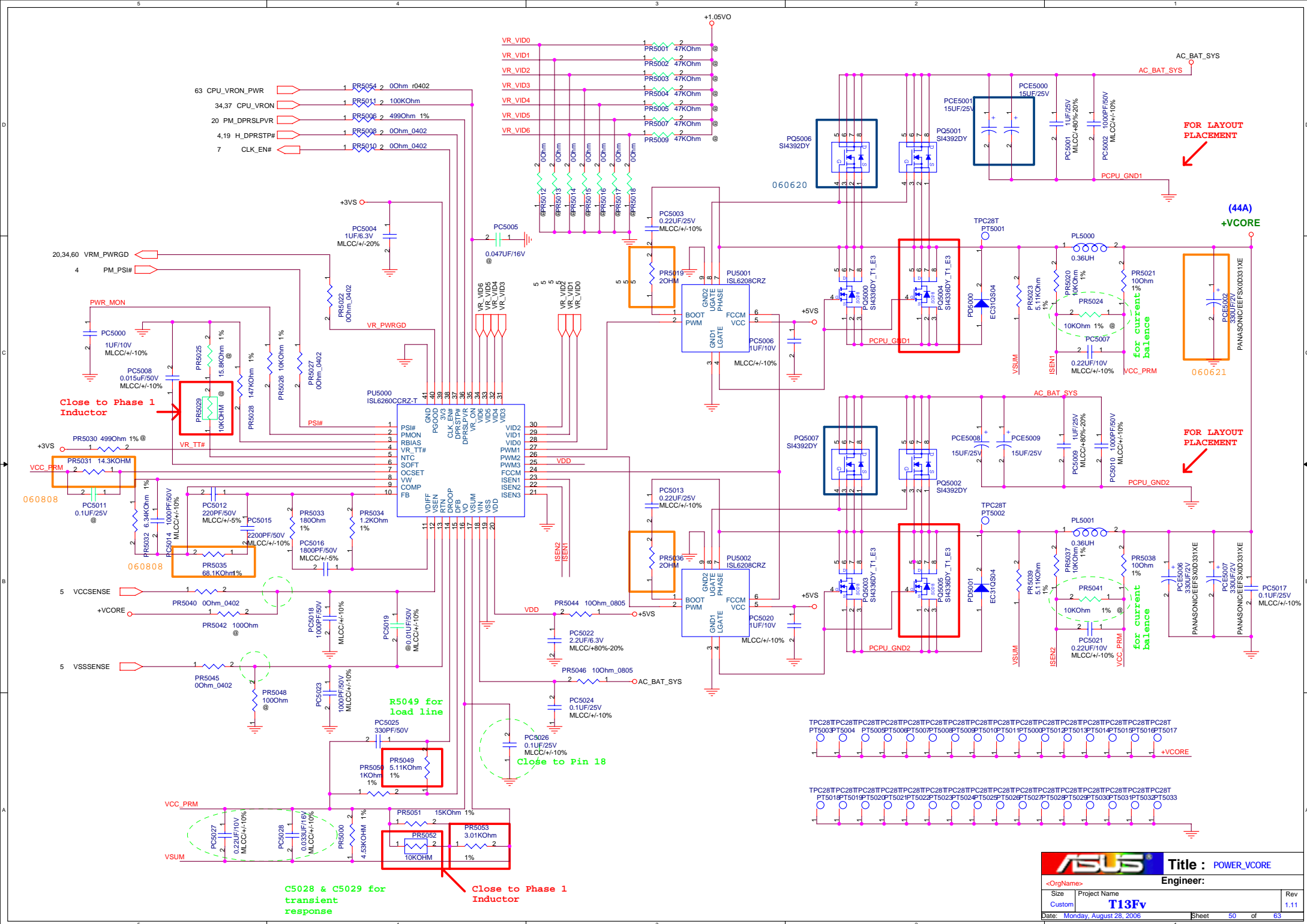
Size  
Custom

Project Name	<b>T13Fv</b>
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Rev  
1.11

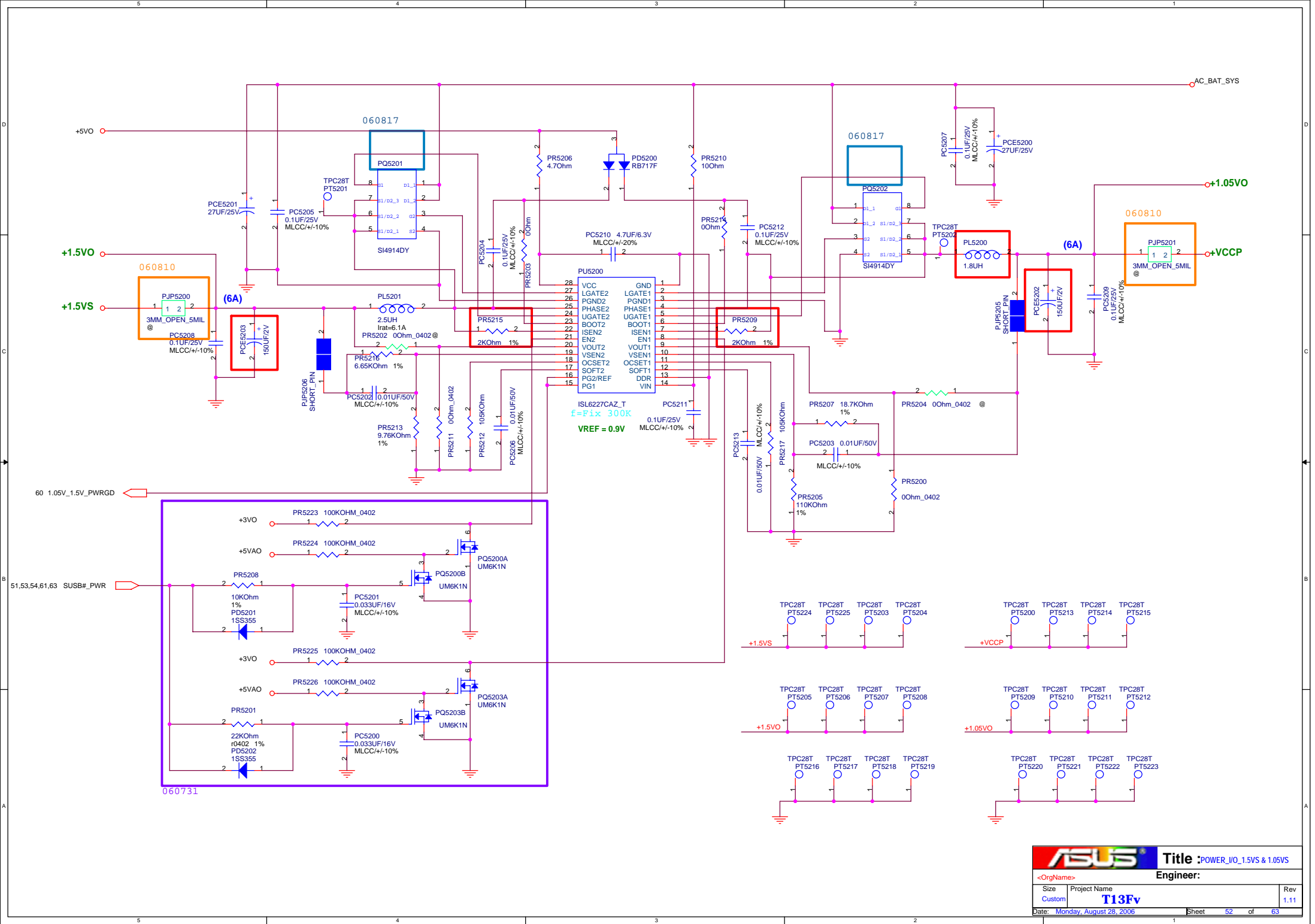
Date: Monday, August 28, 2006

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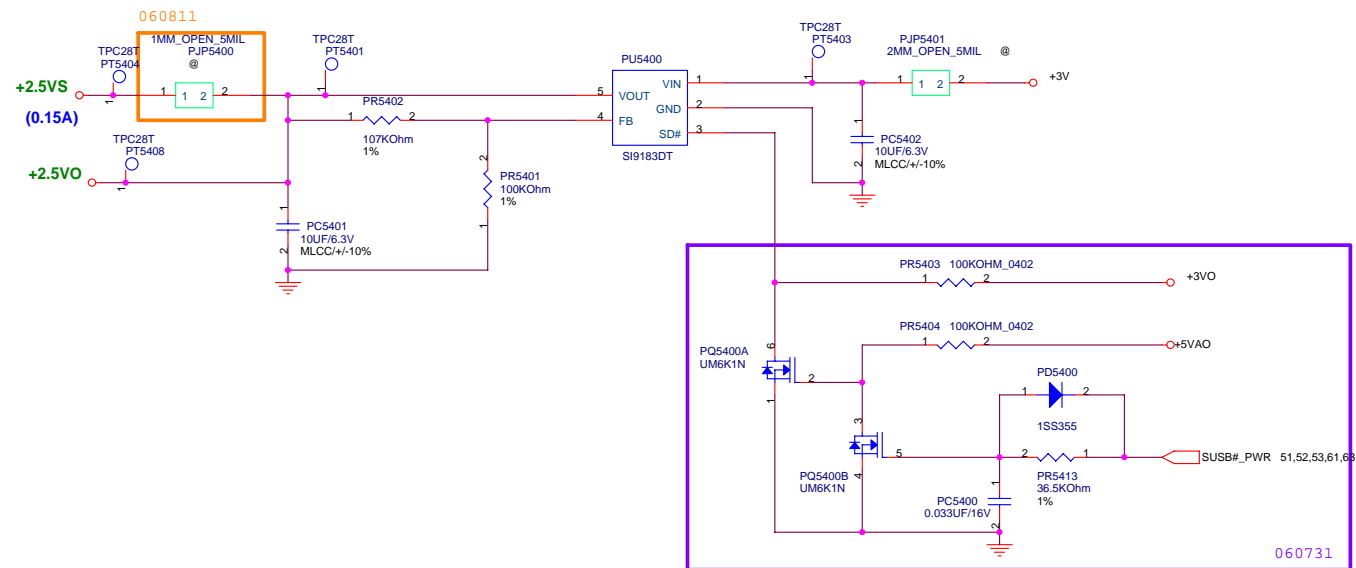






		<b>Title :</b> POWER_I/O_DDR & VTT	
<b>&lt;OrigName&gt;</b>		<b>Engineer:</b>	
Size Custom	Project Name <b>T13Fv</b>		Rev 1.11
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+2.5VS

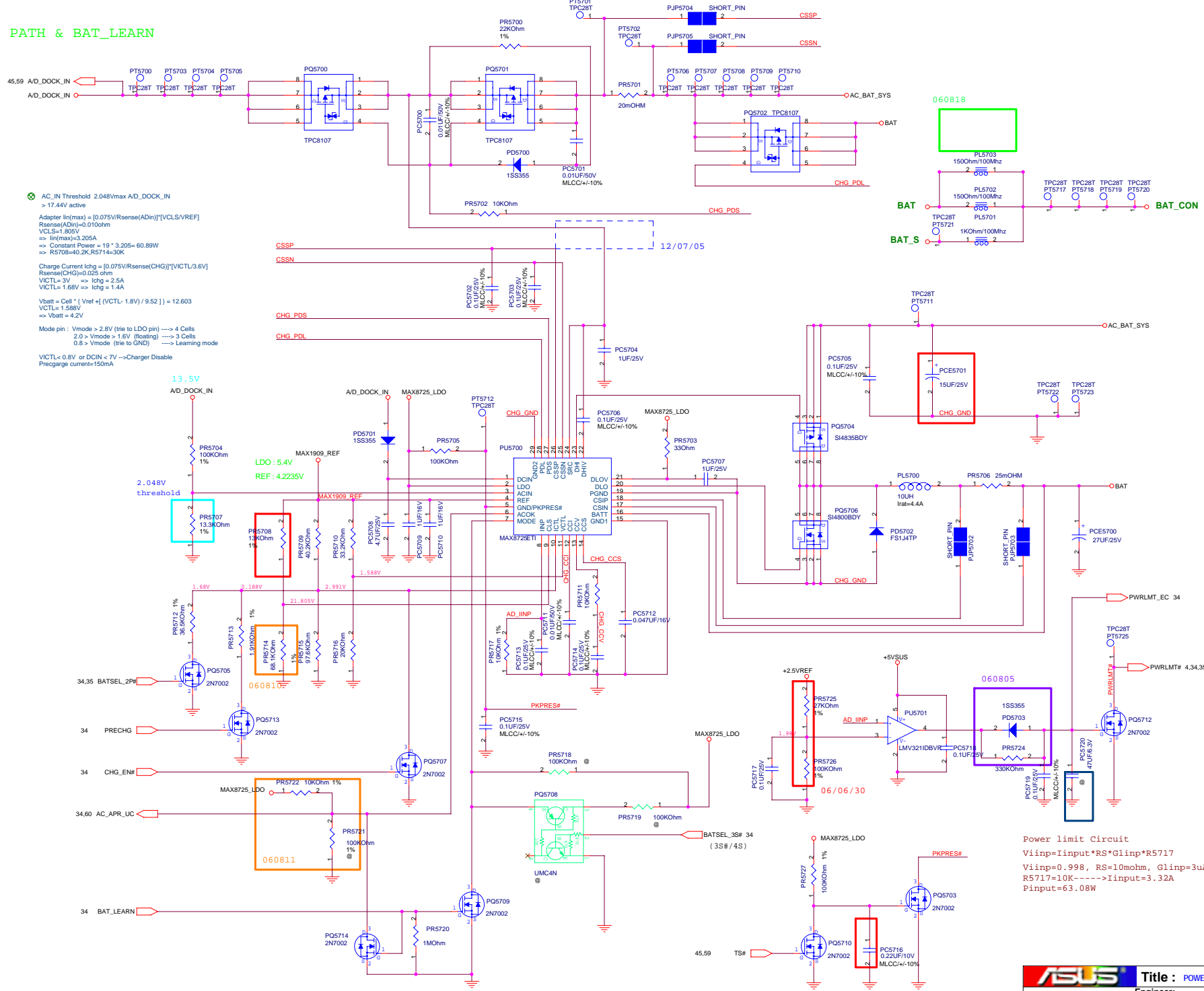






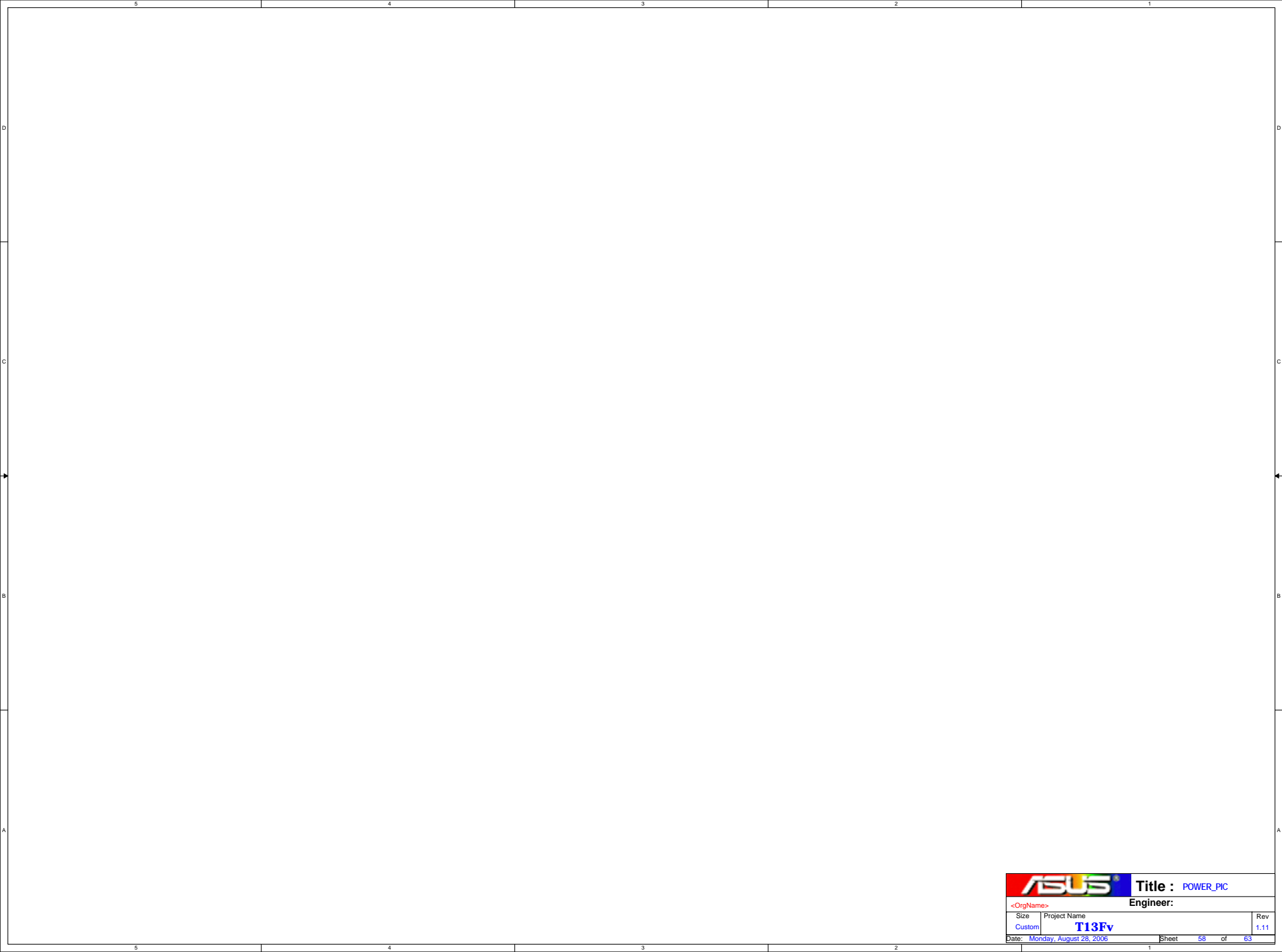
# POWER PATH & BAT\_LEARN


AC\_IN Threshold  $2.048V_{max} A/D\_DOCK\_IN$   
 $> 17.44V$  active  
 Adapter  $lin(max) = [0.075V/R_{sense}(ADIN)] * [V_{CLS}/V_{REF}]$   
 $R_{sense}(ADIN) = 0.010ohm$   
 $V_{CLS} = 1.805V$   
 $\Rightarrow lin(max) = 3.205A$   
 $\Rightarrow Constant Power = 19 * 3.205 = 60.89W$   
 $\Rightarrow R_{5708} = 40.2K, R_{5714} = 30K$   
 Charge Current  $I_{chg} = [0.075V/R_{sense}(CHG)] * [V_{ICTL}/3.6V]$   
 $R_{sense}(CHG) = 0.025ohm$   
 $V_{ICTL} = 3V \Rightarrow I_{chg} = 2.5A$   
 $V_{ICTL} = 1.88V \Rightarrow I_{chg} = 1.4A$   
 $V_{batt} = Cell * (V_{ref} - (V_{ICTL} - 1.8V) / 9.52) = 12.803$   
 $V_{ICTL} = 1.588V$   
 $\Rightarrow V_{batt} = 4.2V$   
 Mode pin :  $V_{mode} > 2.8V$  (tie to LDO pin)  $\Rightarrow$  4 Cells  
 $2.0 > V_{mode} > 1.6V$  (floating)  $\Rightarrow$  3 Cells  
 $0.8 > V_{mode}$  (tie to GND)  $\Rightarrow$  Learning mode  
 $V_{ICTL} < 0.8V$  or  $DCIN < 7V \Rightarrow$  Charger Disable  
 Precharge current=150mA



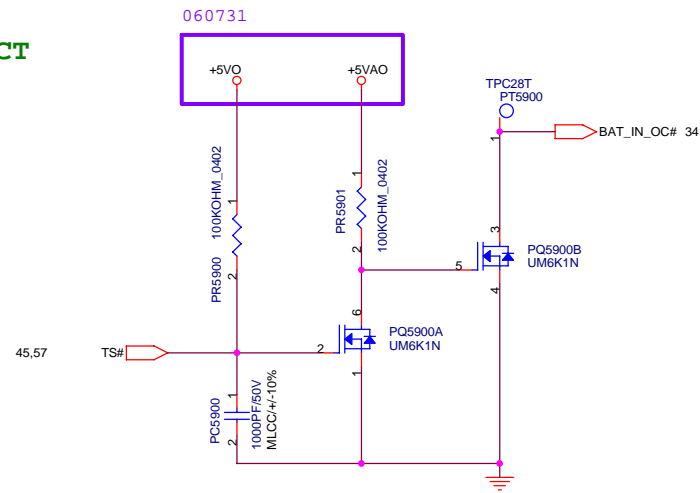
Power limit Circuit  
 $V_{iinp} = Input * RS * G_{iinp} * R_{5717}$   
 $V_{iinp} = 0.998, RS = 10mohm, G_{iinp} = 3uA/mV,$   
 $R_{5717} = 10K \Rightarrow I_{input} = 3.32A$   
 $P_{input} = 63.08W$



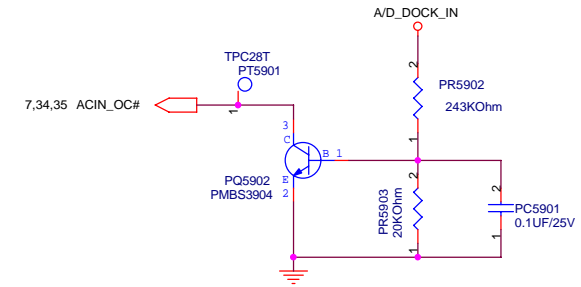


		<b>Title :</b> POWER_PIC	
<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>T13Fv</b>	1.11	
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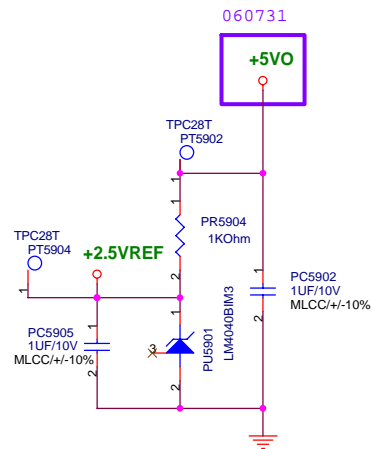
BATTERY IN DETECT

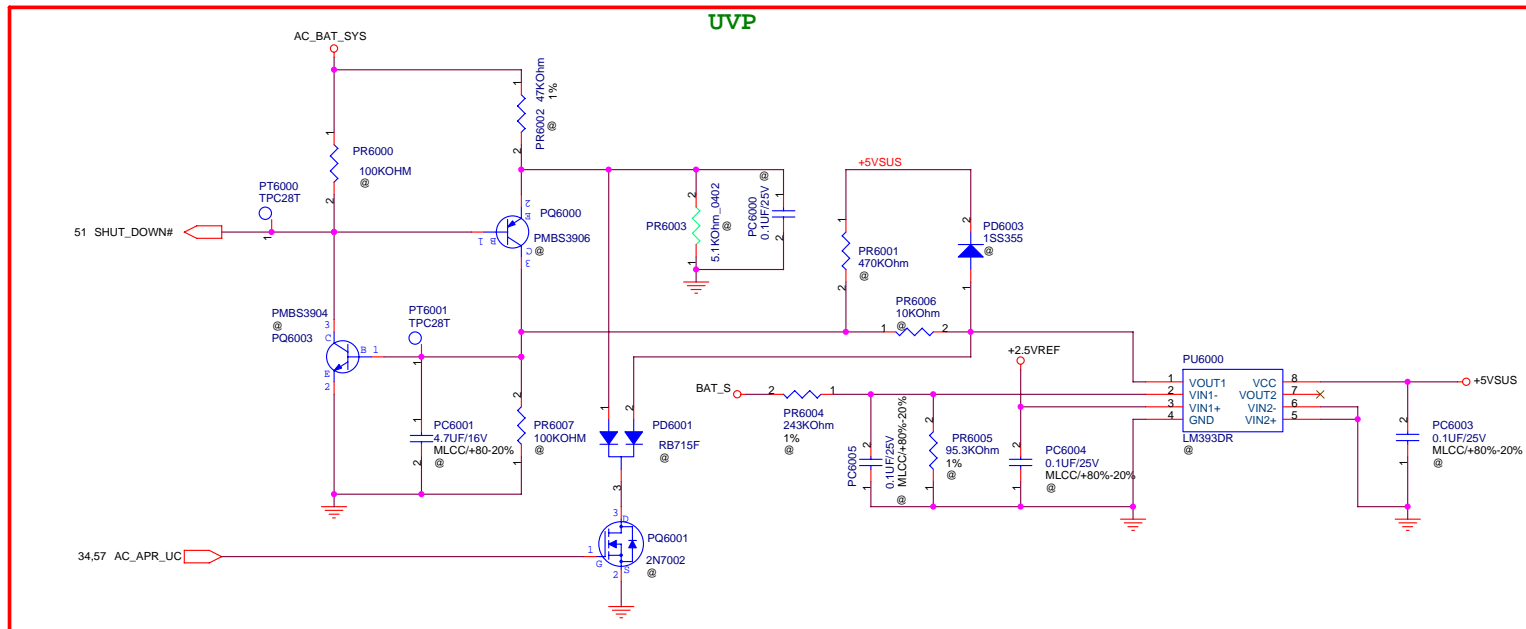


## ADAPTER IN DETECT

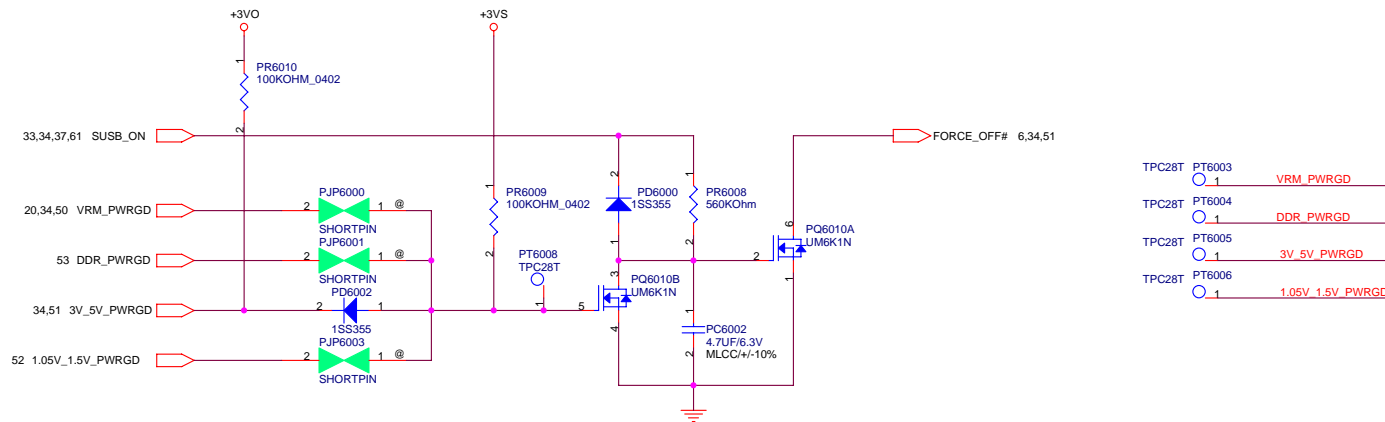


**+5VLCM, +5VCHG & +2.5VREF**

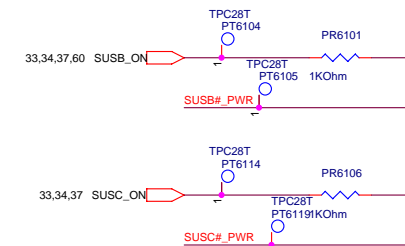




## POWER GOOD DETECTER



## SUSC# PWR POWER



SUSB#\_PWR POWER







## FOR POWER TEST

