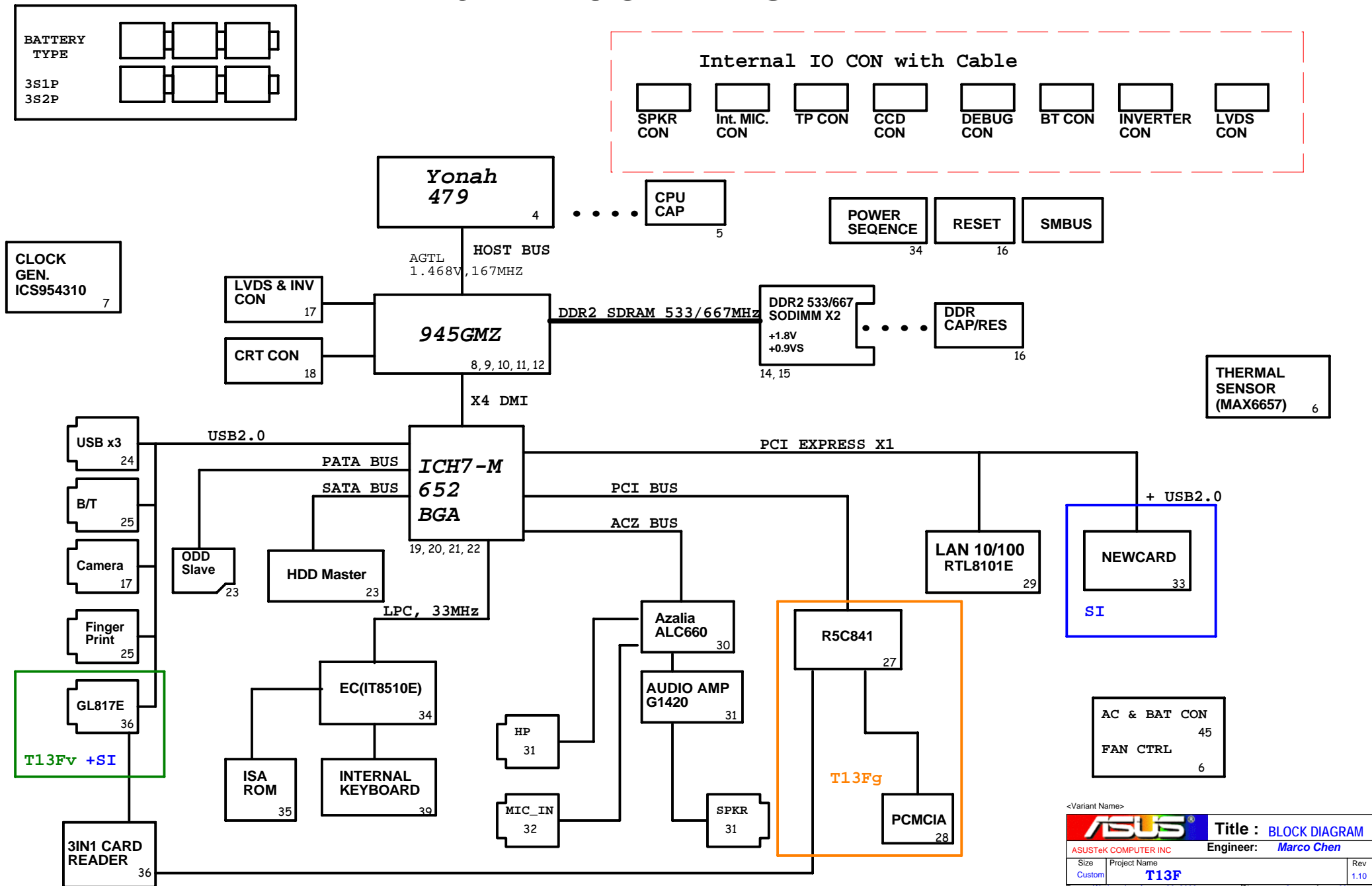


T13F SCHEMATIC R1.10

PAGE	Content	PAGE	Content
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4	YONAH CPU (1)	48	History(1)
5	YONAH CPU (2)	49	History(2)
6	FAN CTRL&Thernal protection	-----	
7	CLK GEN-ICS954310	POWER PAGE REF.	
8	Calistoga--CPU	50	POWER_VCORE
9	Calistoga--PCIE	51	POWER_SYSTEM
10	Calistoga--DDR2	52	POWER_I/O_1.8V & 1.05VS
11	Calistoga--POWER	53	POWER_I/O_DDR & VTT
12	Calistoga--GND	54	POWER_I/O_VTT & +2.5VS
13	Calistoga--Strap	55	POWER_VGA_CORE(Empty)
14	DDR2 SO-DIMM_0	56	POWER_VGA_RAM(Empty)
15	DDR2 SO-DIMM_1	57	POWER_CHARGER
16	DDR2 ADDRESS TERMINATION	58	POWER_PIC(Empty)
17	LVDS & INVERTER CONN	59	POWER_DETECT
18	VGA CONN	60	POWER_PROTECT
19	ICH7M--CPU,IDE,AUDIO	61	POWER_LOAD SWITCH
20	ICH7M--GPIO	62	POWER_FLOWCHART
21	ICH7M--PCI,PCI-E,USB	63	POWER_SIGNAL
22	ICH7M--VCC,GND		
23	HDD & CD-ROM CONN		
24	USB PORT		
25	B/T & F/P		
26	B TO B CONN(M)		
27	CARDBUS R5C841		
28	PCMCIA SOCKET		
29	PCI-E--LAN_RTL8101E		
30	AZALIA - ALC660-GR		
31	AUDIO_AMPLIFIER		
32	MICROPHONE		
33	NEWCARD		
34	EC-IT8510E		
35	ISA ROM & Touch Pad & KB& FP		
36	Card Reader GL817E		
37	DISCHARGE		
38	Instant Key & FFC CONN		
39	LEDs		
40	EMPTY		
41	EMPTY		
42	EMPTY		
43	EMPTY		
44	EMPTY		
45	SREW HOLE		
46	DC & BAT IN		

# T13F BLOCK DIAGRAM



## EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	KCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	CR_DRIVER#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PCI_RST#	I
31	ECSC#/#GPD3	EXT_SC#	O
41	GPD4	CR_POWER#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	PWRLMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTTER_DA	O
102	DAC3	BATSEL_2P#	O

## ICH7M\_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

## ICH7M\_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A4 )
Thermal Sensor( MAX6657)	1001100x ( 98 )

## ICH7M\_PCI\_DEVICE:

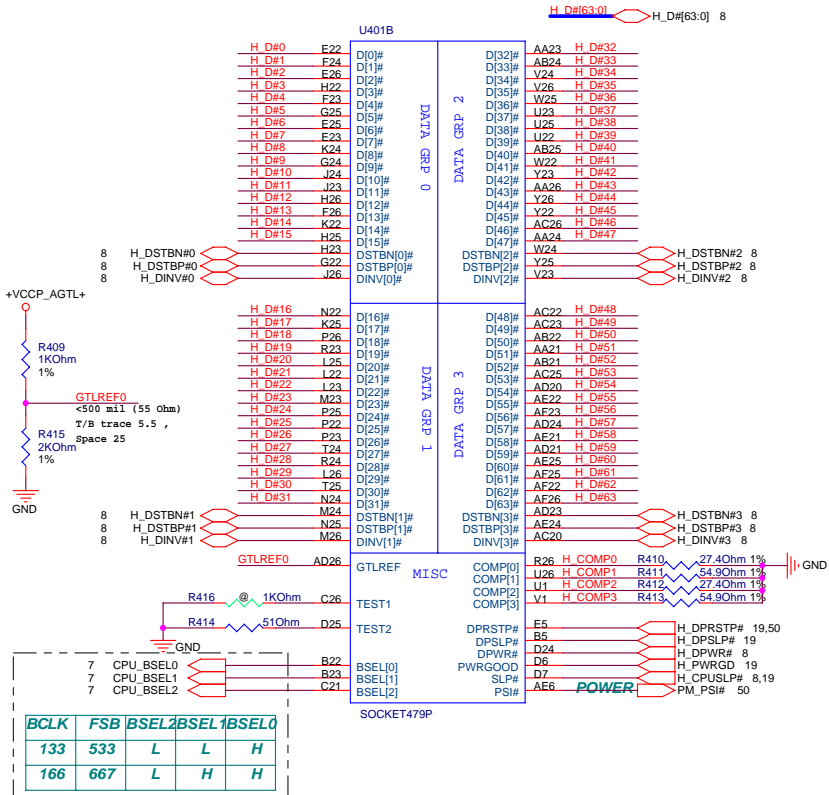
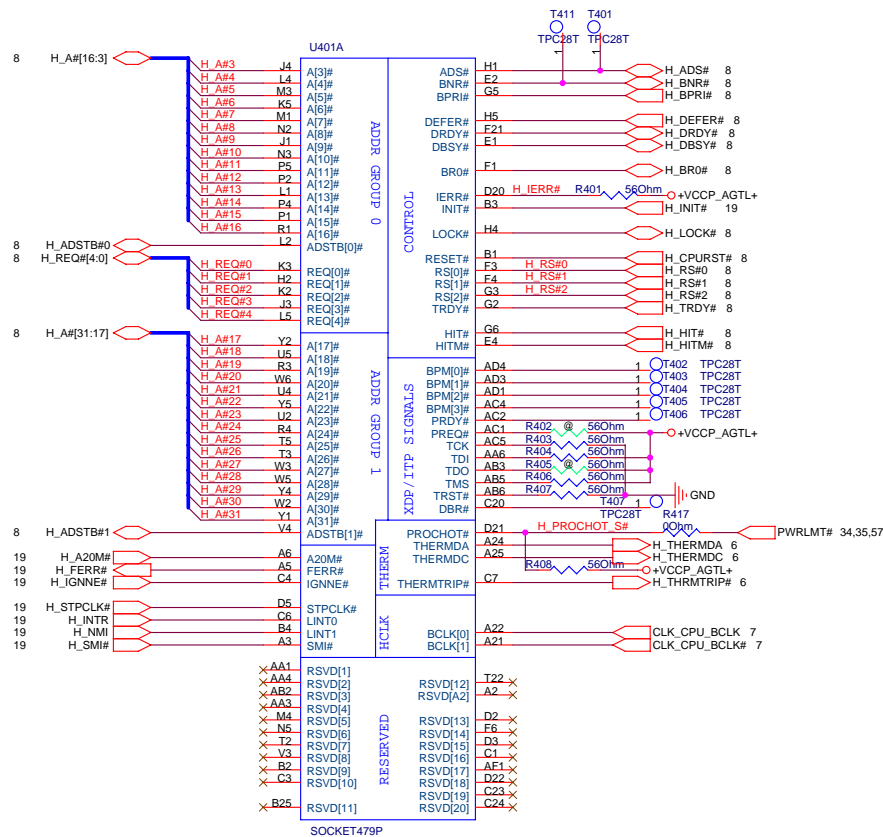
PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

## ICH7M\_GPIO

Pin	Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#
GPIO 01	i	GPI	PCI_REQ#5
GPIO [5:2]	i	GPI	PCI_INT[E:H]#
GPIO 06	i	GPO	BT_LED_EN
GPIO 07	i	GPI	N/A
GPIO 08	i	GPI	EXTSM#
GPIO 09	i	GPI	N/A
GPIO 10	i	GPI	N/A
GPIO 11	i	Native	SMB_ALERT#
GPIO 12	i	GPI	KBC_SC#
GPIO 13	i	GPI	N/A
GPIO 14	i	GPI	N/A
GPIO 15	i	GPO	802_LED_EN
GPIO 16	O 0	GPO	PM DPRSLPVR
GPIO 17	O 1	GPO	PCI_GNT#5
GPIO 18	O 1	GPO	STP_PCI#
GPIO 19	i 1	GPI	N/A
GPIO 20	O 1	GPO	STP_CPU#
GPIO 21	i 1	GPO	N/A
GPIO 22	i 1	Native	PCI_REQ#4
GPIO 23	i 1	Native	N/A
GPIO 24	O 0	GPO	MSK_PCIRST
GPIO 25	O 1	GPO	CB_SD#
GPIO 26	O 0	GPO	BT_ON#
GPIO 27	O 0	GPO	WLAN_ON#
GPIO 28	O 0	GPO	MEMROM/YONAH#
GPIO 29	i 0	Native	USB_OC#5
GPIO 30	i 0	Native	USB_OC#6
GPIO 31	i 0	Native	USB_OC#7
GPIO 32	O 1	GPO	PM_CLKRUN#
GPIO 33	O 1	GPO	N/A
GPIO 34	O 0	GPO	CPU_Select
GPIO 35	O 0	GPO	N/A
GPIO 36	i 0	GPO	N/A
GPIO 37	i 0	GPI	PCB_ID0
GPIO 38	i 0	GPI	PCB_ID1
GPIO 39	i 0	GPI	PCB_ID2
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

<Variant Name>

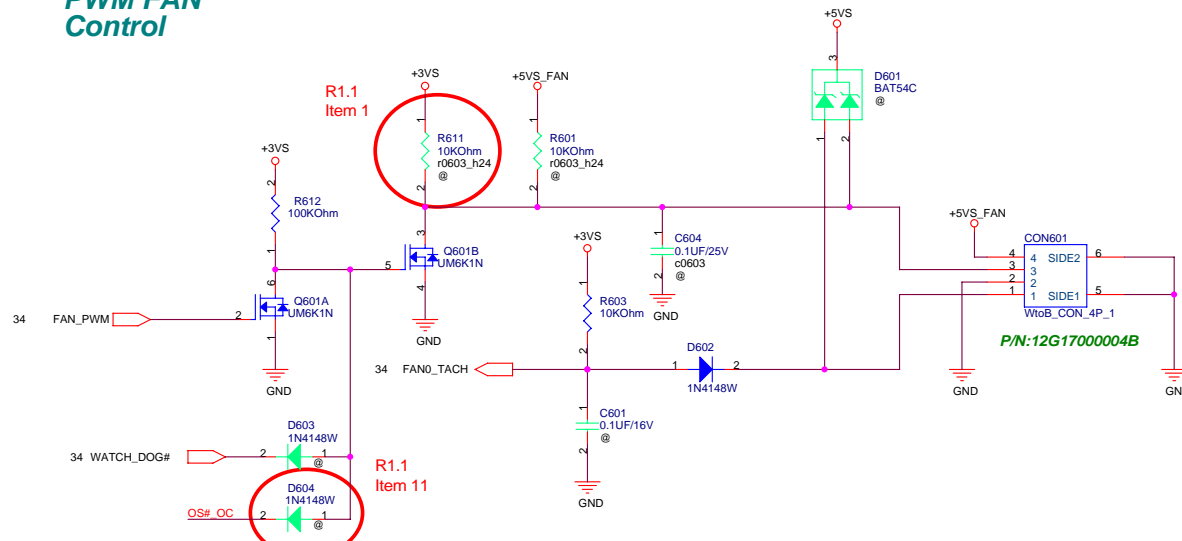
		Title :	Schematic data
ASUSTeK COMPUTER INC		Engineer:	Marco Chen
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Wednesday, August 30, 2006		Sheet	3 of 63



<Variant Name>

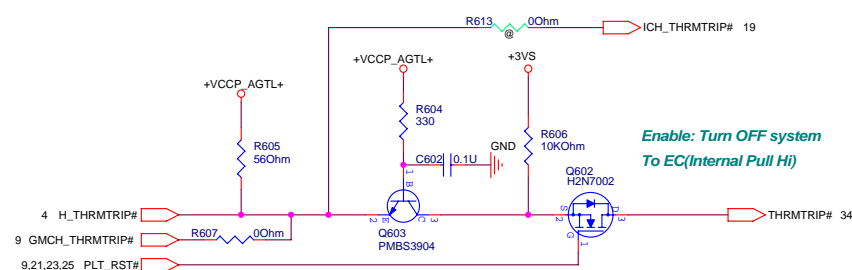
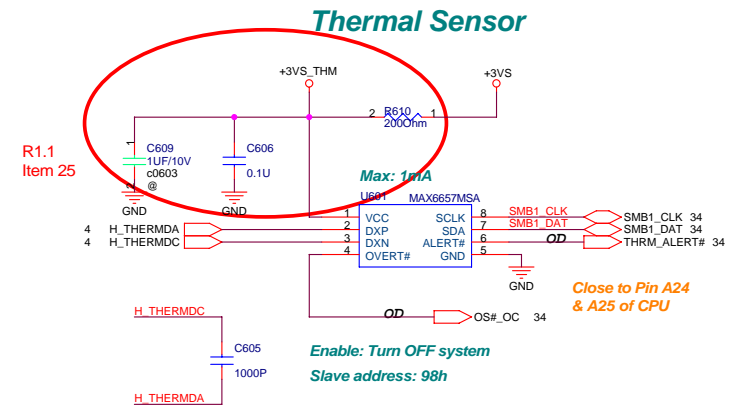
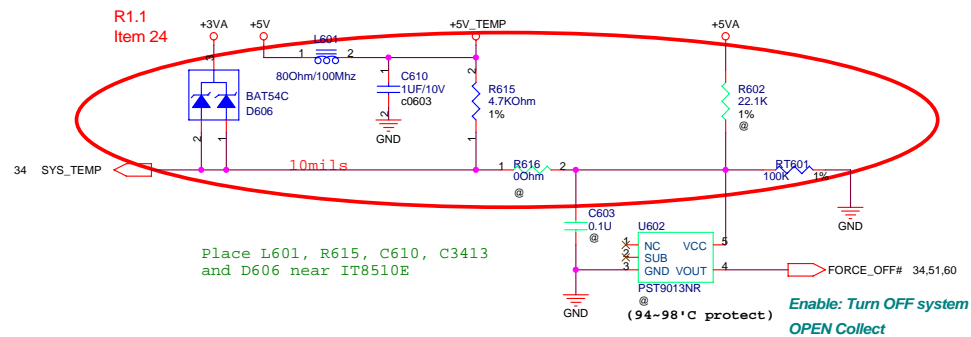


## PWM FAN Control



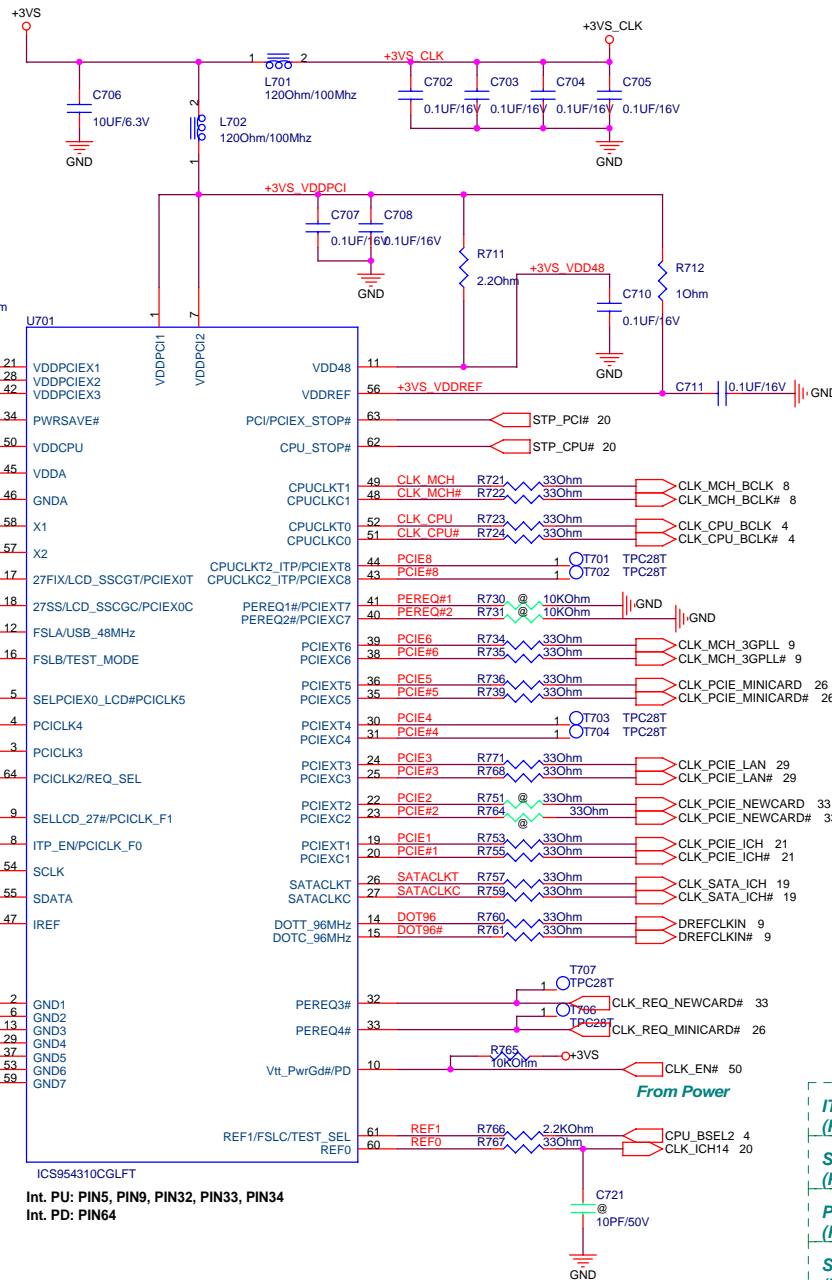
**CPU FAN will be forced on:**

- 1) Thermal Sensor Over-temperature
- 2) WATCHDOG asserted by EC



CPU\_BSEL0 R701 1KOhm MCH\_BSEL0 9  
CPU\_BSEL1 R702 1KOhm MCH\_BSEL1 9  
CPU\_BSEL2 R705 1KOhm MCH\_BSEL2 9

FSLC FSLB FSLA				
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



PLACE termination close to source IC

CLK MCH\_BCLK R703 49.9Ohm 1%  
CLK MCH\_BCLK# R704 49.9Ohm 1%  
CLK CPU\_BCLK R706 49.9Ohm 1%  
CLK CPU\_BCLK# R708 49.9Ohm 1%  
CLK PCIE\_MINICARD R709 49.9Ohm 1%  
CLK PCIE\_MINICARD# R710 49.9Ohm 1%  
CLK MCH\_3GPLL R713 49.9Ohm 1%  
CLK MCH\_3GPLL# R715 49.9Ohm 1%  
CLK PCIE\_ICH R717 49.9Ohm 1%  
CLK PCIE\_ICH# R718 49.9Ohm 1%  
CLK PCIE\_NEWCARD R763 49.9Ohm 1%  
CLK PCIE\_NEWCARD# R750 49.9Ohm 1%  
CLK PCIE\_LAN R769 49.9Ohm 1%  
CLK PCIE\_LAN# R770 49.9Ohm 1%  
CLK SATA\_ICH R726 49.9Ohm 1%  
CLK SATA\_ICH# R728 49.9Ohm 1%  
DREFCLKIN R737 49.9Ohm 1%  
DREFCLKIN# R741 49.9Ohm 1%  
DREFSSCLKIN R744 49.9Ohm 1%  
DREFSSCLKIN# R746 49.9Ohm 1%

PEREQ#1: PCIE#0, PCIE#6  
PEREQ#2: PCIE#1, PCIE#8  
PEREQ#3: PCIE#2, PCIE#4  
PEREQ#4: PCIE#3, PCIE#5, PCIE#7

### Latched Input Select

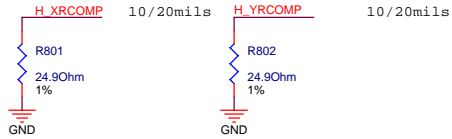
/	PIN9	PIN5	PIN17	PIN18
*	0	X	27FIX	27SS
	1	0	96MSS_T	96MSS_C
	1	1	PCIE#0_T	PCIE#0_C

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)



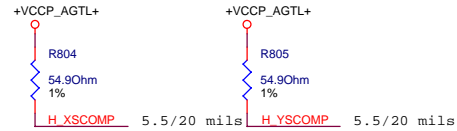
## RCOMP

For Calibrating FSB I/O Buffer



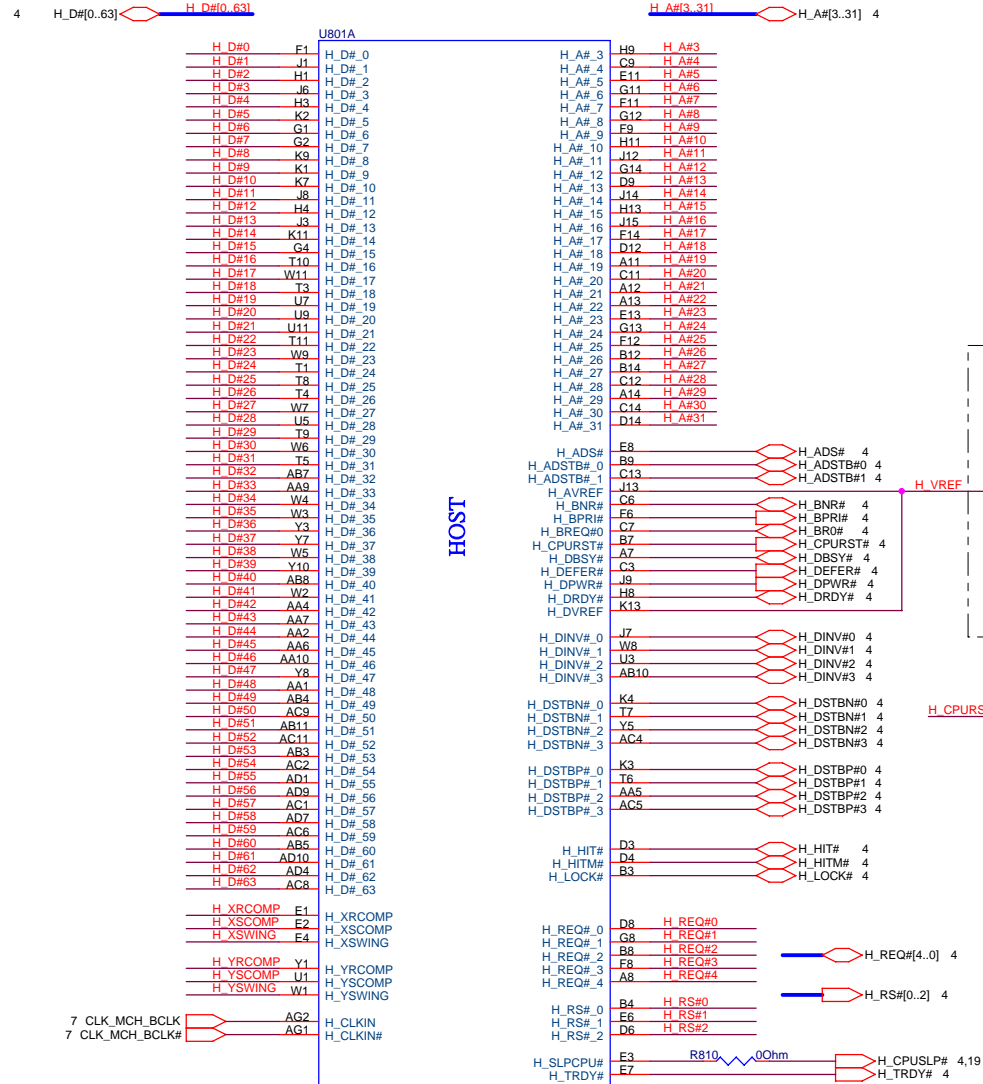
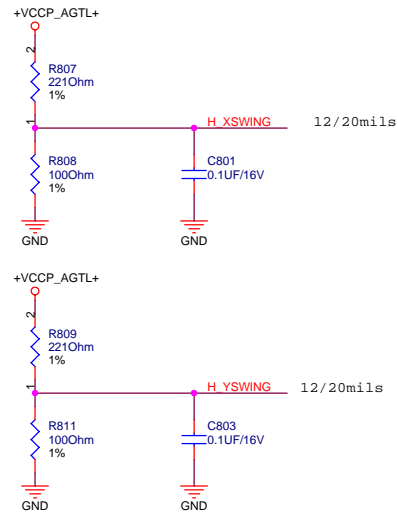
## SCOMP

For Slew Rate Compensation on the FSB

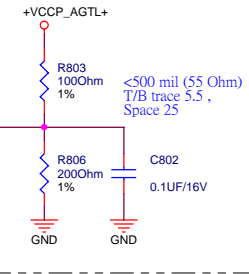


## Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit

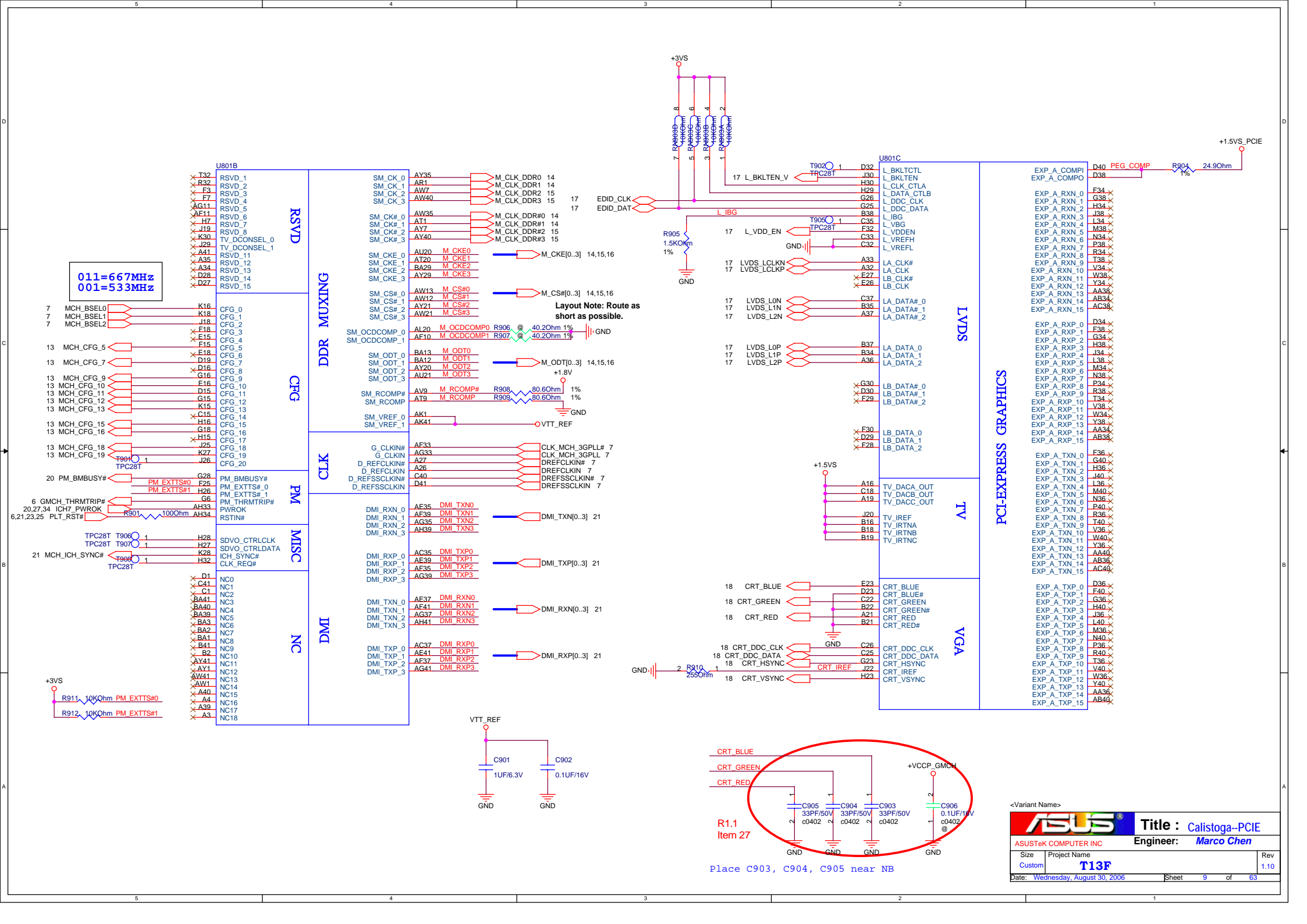


## AGTL+ I/O Voltage Reference



<Variant Name>





14 M\_A\_DQ[0..63]

U801D  
M\_A\_DQ0 AJ35 SA\_DQ0  
M\_A\_DQ1 AJ34 SA\_DQ1  
M\_A\_DQ2 AM31 SA\_DQ2  
M\_A\_DQ3 AM33 SA\_DQ3  
M\_A\_DQ4 AJ36 SA\_DQ4  
M\_A\_DQ5 AK35 SA\_DQ5  
M\_A\_DQ6 AJ32 SA\_DQ6  
M\_A\_DQ7 AH31 SA\_DQ7  
M\_A\_DQ8 AN35 SA\_DQ8  
M\_A\_DQ9 AP33 SA\_DQ9  
M\_A\_DQ10 AP31 SA\_DQ10  
M\_A\_DQ11 AP31 SA\_DQ11  
M\_A\_DQ12 AN38 SA\_DQ12  
M\_A\_DQ13 AM36 SA\_DQ13  
M\_A\_DQ14 AM34 SA\_DQ14  
M\_A\_DQ15 AN33 SA\_DQ15  
M\_A\_DQ16 AK26 SA\_DQ16  
M\_A\_DQ17 AL27 SA\_DQ17  
M\_A\_DQ18 AM26 SA\_DQ18  
M\_A\_DQ19 AN24 SA\_DQ19  
M\_A\_DQ20 AK28 SA\_DQ20  
M\_A\_DQ21 AL28 SA\_DQ21  
M\_A\_DQ22 AM24 SA\_DQ22  
M\_A\_DQ23 AP28 SA\_DQ23  
M\_A\_DQ24 AP23 SA\_DQ24  
M\_A\_DQ25 AL22 SA\_DQ25  
M\_A\_DQ26 AP21 SA\_DQ26  
M\_A\_DQ27 AN20 SA\_DQ27  
M\_A\_DQ28 AL23 SA\_DQ28  
M\_A\_DQ29 AP24 SA\_DQ29  
M\_A\_DQ30 AP20 SA\_DQ30  
M\_A\_DQ31 AT21 SA\_DQ31  
M\_A\_DQ32 AR12 SA\_DQ32  
M\_A\_DQ33 AR14 SA\_DQ33  
M\_A\_DQ34 AP13 SA\_DQ34  
M\_A\_DQ35 AP12 SA\_DQ35  
M\_A\_DQ36 AT13 SA\_DQ36  
M\_A\_DQ37 AT12 SA\_DQ37  
M\_A\_DQ38 AL14 SA\_DQ38  
M\_A\_DQ39 AL12 SA\_DQ39  
M\_A\_DQ40 AK9 SA\_DQ40  
M\_A\_DQ41 AN7 SA\_DQ41  
M\_A\_DQ42 AK8 SA\_DQ42  
M\_A\_DQ43 AK7 SA\_DQ43  
M\_A\_DQ44 AP9 SA\_DQ44  
M\_A\_DQ45 AN9 SA\_DQ45  
M\_A\_DQ46 AT5 SA\_DQ46  
M\_A\_DQ47 AL5 SA\_DQ47  
M\_A\_DQ48 AY2 SA\_DQ48  
M\_A\_DQ49 AW2 SA\_DQ49  
M\_A\_DQ50 AP1 SA\_DQ50  
M\_A\_DQ51 AN2 SA\_DQ51  
M\_A\_DQ52 AV2 SA\_DQ52  
M\_A\_DQ53 AT3 SA\_DQ53  
M\_A\_DQ54 AN1 SA\_DQ54  
M\_A\_DQ55 AL2 SA\_DQ55  
M\_A\_DQ56 AG7 SA\_DQ56  
M\_A\_DQ57 AF9 SA\_DQ57  
M\_A\_DQ58 AG4 SA\_DQ58  
M\_A\_DQ59 AF6 SA\_DQ59  
M\_A\_DQ60 AG9 SA\_DQ60  
M\_A\_DQ61 AH6 SA\_DQ61  
M\_A\_DQ62 AF4 SA\_DQ62  
M\_A\_DQ63 AF8 SA\_DQ63

## DDR SYSTEM MEMORY A

SA\_BS\_0 AU12 M\_A\_BS#0 14,16  
SA\_BS\_1 AV14 M\_A\_BS#1 14,16  
SA\_BS\_2 BA20 M\_A\_BS#2 14,16  
SA\_CAS# AY13 M\_A\_CAS# 14,16  
SA\_DM\_0 AJ33 M\_A\_DM0  
SA\_DM\_1 AM35 M\_A\_DM1  
SA\_DM\_2 AL26 M\_A\_DM2  
SA\_DM\_3 AN22 M\_A\_DM3  
SA\_DM\_4 AM14 M\_A\_DM4  
SA\_DM\_5 AL9 M\_A\_DM5  
SA\_DM\_6 AR3 M\_A\_DM6  
SA\_DM\_7 AH4 M\_A\_DM7  
SA\_DQS\_0 AK33 M\_A\_DQS0  
SA\_DQS\_1 AT33 M\_A\_DQS1  
SA\_DQS\_2 AN28 M\_A\_DQS2  
SA\_DQS\_3 AM22 M\_A\_DQS3  
SA\_DQS\_4 AN12 M\_A\_DQS4  
SA\_DQS\_5 AN8 M\_A\_DQS5  
SA\_DQS\_6 AP3 M\_A\_DQS6  
SA\_DQS\_7 AG5 M\_A\_DQS7  
SA\_DQS#\_0 AK32 M\_A\_DQS#0  
SA\_DQS#\_1 AN27 M\_A\_DQS#1  
SA\_DQS#\_2 AM21 M\_A\_DQS#2  
SA\_DQS#\_3 AM12 M\_A\_DQS#3  
SA\_DQS#\_4 AL8 M\_A\_DQS#4  
SA\_DQS#\_5 AN3 M\_A\_DQS#5  
SA\_DQS#\_6 AN3 M\_A\_DQS#6  
SA\_DQS#\_7 AH5 M\_A\_DQS#7  
SA\_MA\_0 AY16 M\_A\_A0  
SA\_MA\_1 AU14 M\_A\_A1  
SA\_MA\_2 AW16 M\_A\_A2  
SA\_MA\_3 BA16 M\_A\_A3  
SA\_MA\_4 BA17 M\_A\_A4  
SA\_MA\_5 AU16 M\_A\_A5  
SA\_MA\_6 AV17 M\_A\_A6  
SA\_MA\_7 AU17 M\_A\_A7  
SA\_MA\_8 AW17 M\_A\_A8  
SA\_MA\_9 AT16 M\_A\_A9  
SA\_MA\_10 AU13 M\_A\_A10  
SA\_MA\_11 AT17 M\_A\_A11  
SA\_MA\_12 AV20 M\_A\_A12  
SA\_MA\_13 AV12 M\_A\_A13  
SA\_RAS# AW14 M\_A\_RAS# 14,16  
SA\_RCVENIN# AK23 M\_A\_RCVENIN#  
SA\_RCVENOUT# AK24 M\_A\_RCVENOUT#  
SA\_WE# AY14 M\_A\_WE# 14,16

M\_A\_BS#0 14,16  
M\_A\_BS#1 14,16  
M\_A\_BS#2 14,16  
M\_A\_CAS# 14,16  
M\_A\_DM[0..7] 14  
M\_A\_DQS[0..7] 14  
M\_A\_DQS#[0..7] 14  
M\_A\_A[0..13] 14,16  
M\_A\_RAS# 14,16  
M\_A\_WE# 14,16

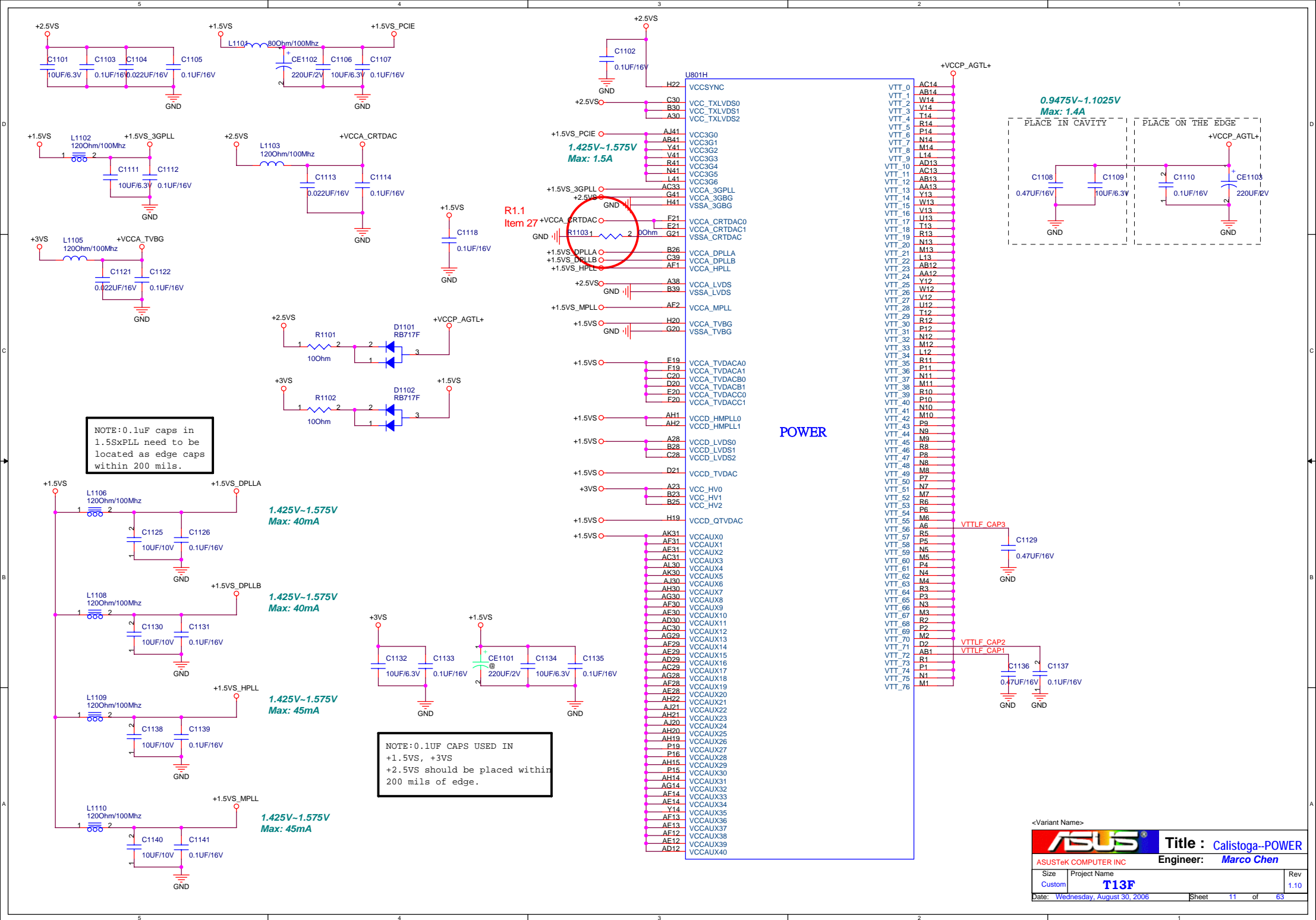
15 M\_B\_DQ[0..63]

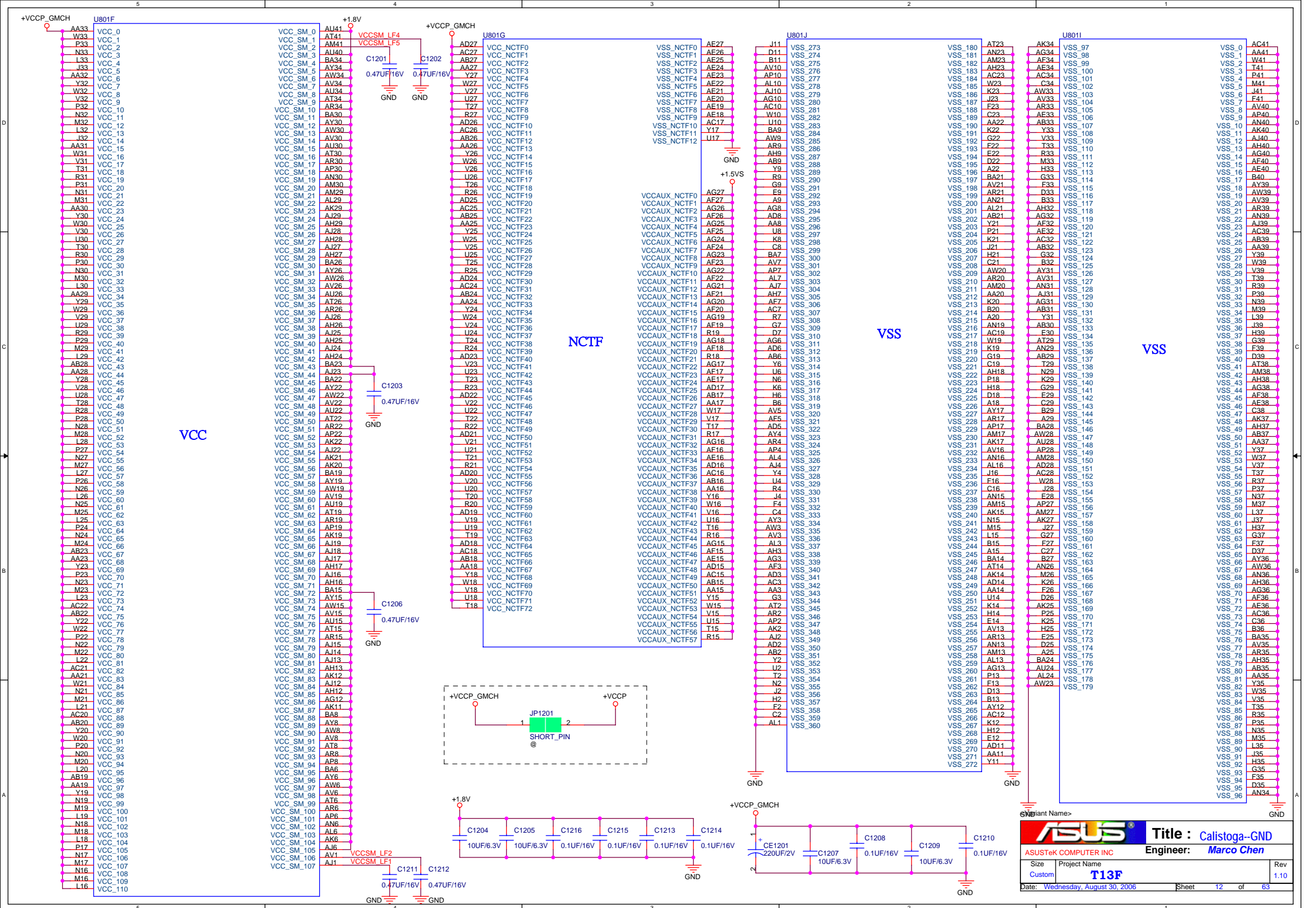
U801E  
M\_B\_DQ0 AK39 SB\_DQ0  
M\_B\_DQ1 AJ37 SB\_DQ1  
M\_B\_DQ2 AP39 SB\_DQ2  
M\_B\_DQ3 AR41 SB\_DQ3  
M\_B\_DQ4 AK38 SB\_DQ4  
M\_B\_DQ5 AJ38 SB\_DQ5  
M\_B\_DQ6 AN41 SB\_DQ6  
M\_B\_DQ7 AP41 SB\_DQ7  
M\_B\_DQ8 AT40 SB\_DQ8  
M\_B\_DQ9 AV41 SB\_DQ9  
M\_B\_DQ10 AU38 SB\_DQ10  
M\_B\_DQ11 AV38 SB\_DQ11  
M\_B\_DQ12 AP38 SB\_DQ12  
M\_B\_DQ13 AR40 SB\_DQ13  
M\_B\_DQ14 AW38 SB\_DQ14  
M\_B\_DQ15 AY38 SB\_DQ15  
M\_B\_DQ16 BA38 SB\_DQ16  
M\_B\_DQ17 AV36 SB\_DQ17  
M\_B\_DQ18 AR36 SB\_DQ18  
M\_B\_DQ19 AP36 SB\_DQ19  
M\_B\_DQ20 BA36 SB\_DQ20  
M\_B\_DQ21 AU36 SB\_DQ21  
M\_B\_DQ22 AP35 SB\_DQ22  
M\_B\_DQ23 AP34 SB\_DQ23  
M\_B\_DQ24 AY33 SB\_DQ24  
M\_B\_DQ25 BA33 SB\_DQ25  
M\_B\_DQ26 AT31 SB\_DQ26  
M\_B\_DQ27 AU29 SB\_DQ27  
M\_B\_DQ28 AU31 SB\_DQ28  
M\_B\_DQ29 AW31 SB\_DQ29  
M\_B\_DQ30 AV29 SB\_DQ30  
M\_B\_DQ31 AW29 SB\_DQ31  
M\_B\_DQ32 AM19 SB\_DQ32  
M\_B\_DQ33 AL19 SB\_DQ33  
M\_B\_DQ34 AP14 SB\_DQ34  
M\_B\_DQ35 AN14 SB\_DQ35  
M\_B\_DQ36 AM17 SB\_DQ36  
M\_B\_DQ37 AM16 SB\_DQ37  
M\_B\_DQ38 AP15 SB\_DQ38  
M\_B\_DQ39 AL15 SB\_DQ39  
M\_B\_DQ40 AH10 SB\_DQ40  
M\_B\_DQ41 AH10 SB\_DQ41  
M\_B\_DQ42 AJ8 SB\_DQ42  
M\_B\_DQ43 AN10 SB\_DQ43  
M\_B\_DQ44 AK13 SB\_DQ44  
M\_B\_DQ45 AH11 SB\_DQ45  
M\_B\_DQ46 AK10 SB\_DQ46  
M\_B\_DQ47 AJ8 SB\_DQ47  
M\_B\_DQ48 BA10 SB\_DQ48  
M\_B\_DQ49 AW10 SB\_DQ49  
M\_B\_DQ50 BA4 SB\_DQ50  
M\_B\_DQ51 AW4 SB\_DQ51  
M\_B\_DQ52 AY10 SB\_DQ52  
M\_B\_DQ53 AY9 SB\_DQ53  
M\_B\_DQ54 AW5 SB\_DQ54  
M\_B\_DQ55 AY5 SB\_DQ55  
M\_B\_DQ56 AV4 SB\_DQ56  
M\_B\_DQ57 AR5 SB\_DQ57  
M\_B\_DQ58 AK4 SB\_DQ58  
M\_B\_DQ59 AK3 SB\_DQ59  
M\_B\_DQ60 AT4 SB\_DQ60  
M\_B\_DQ61 AK5 SB\_DQ61  
M\_B\_DQ62 AJ5 SB\_DQ62  
M\_B\_DQ63 AJ3 SB\_DQ63

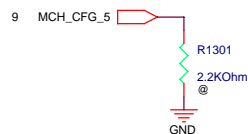
## DDR SYSTEM MEMORY B

SB\_BS\_0 AT24 M\_B\_BS#0 15,16  
SB\_BS\_1 AV23 M\_B\_BS#1 15,16  
SB\_BS\_2 AY28 M\_B\_BS#2 15,16  
SB\_CAS# AR24 M\_B\_CAS# 15,16  
SB\_DM\_0 AK36 M\_B\_DM0  
SB\_DM\_1 AR38 M\_B\_DM1  
SB\_DM\_2 AT36 M\_B\_DM2  
SB\_DM\_3 BA31 M\_B\_DM3  
SB\_DM\_4 AL17 M\_B\_DM4  
SB\_DM\_5 AH8 M\_B\_DM5  
SB\_DM\_6 BA5 M\_B\_DM6  
SB\_DM\_7 AN4 M\_B\_DM7  
SB\_DQS\_0 AM39 M\_B\_DQS0  
SB\_DQS\_1 AT39 M\_B\_DQS1  
SB\_DQS\_2 AU35 M\_B\_DQS2  
SB\_DQS\_3 AR29 M\_B\_DQS3  
SB\_DQS\_4 AR16 M\_B\_DQS4  
SB\_DQS\_5 AR10 M\_B\_DQS5  
SB\_DQS\_6 AR7 M\_B\_DQS6  
SB\_DQS\_7 AN5 M\_B\_DQS7  
SB\_DQS#\_0 AM40 M\_B\_DQS#0  
SB\_DQS#\_1 AU39 M\_B\_DQS#1  
SB\_DQS#\_2 AT35 M\_B\_DQS#2  
SB\_DQS#\_3 AP29 M\_B\_DQS#3  
SB\_DQS#\_4 AP16 M\_B\_DQS#4  
SB\_DQS#\_5 AT10 M\_B\_DQS#5  
SB\_DQS#\_6 AT7 M\_B\_DQS#6  
SB\_DQS#\_7 AP5 M\_B\_DQS#7  
SB\_MA\_0 AY23 M\_B\_A0  
SB\_MA\_1 AW24 M\_B\_A1  
SB\_MA\_2 AY24 M\_B\_A2  
SB\_MA\_3 AR28 M\_B\_A3  
SB\_MA\_4 AT27 M\_B\_A4  
SB\_MA\_5 AT28 M\_B\_A5  
SB\_MA\_6 AV27 M\_B\_A6  
SB\_MA\_7 AV28 M\_B\_A7  
SB\_MA\_8 AV27 M\_B\_A8  
SB\_MA\_9 AW27 M\_B\_A9  
SB\_MA\_10 AY24 M\_B\_A10  
SB\_MA\_11 BA27 M\_B\_A11  
SB\_MA\_12 AY27 M\_B\_A12  
SB\_MA\_13 AR23 M\_B\_A13  
SB\_RAS# AU23 M\_B\_RAS# 15,16  
SB\_RCVENIN# AK18 M\_B\_RCVENIN#  
SB\_RCVENOUT# AK18 M\_B\_RCVENOUT#  
SB\_WE# AR27 M\_B\_WE# 15,16

&lt;Variant Name&gt;

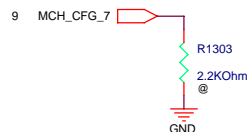






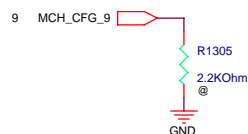
#### CFG5 : DMI STRAP

LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**



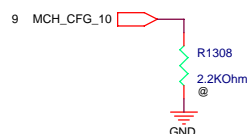
#### CFG7 : CPU STRAP

LOW = RESERVED  
**HIGH = Mobile Yonah CPU (Default)**



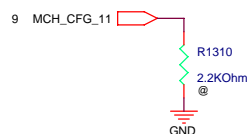
#### CFG9 : PCIE GRAPHIC LANE

**LOW = REVERSE LANE**  
 HIGH = NORMAL OPERATION (Default)



#### CFG10 : HOST PLL VCO SELECT

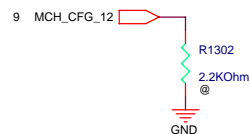
LOW = RESERVED  
**HIGH = MOBILITY (Default)**



#### CFG11 : PSB 4x CLK ENABLE

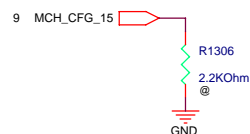
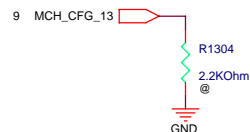
LOW = 4X ENABLED  
**HIGH = 8X ENABLED (Default)**

CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.



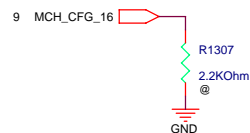
#### CFG[13:12] : GMCH TEST MODE SELECT

00 = Partial CLK gating disable  
 01 = XOR Mode Enable  
 10 = ALL Z Mode Enable  
**11 = NORMAL OPERATION (Default)**



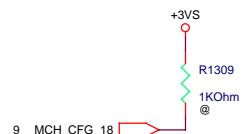
#### CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled  
**HIGH = Normal Operation (Default)**



#### CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**



#### CFG18 : GMCH Core Voltage Level


**LOW = 1.05V (Default)**  
 HIGH = 1.5V



#### CFG19 : DMI LANE REVERSAL

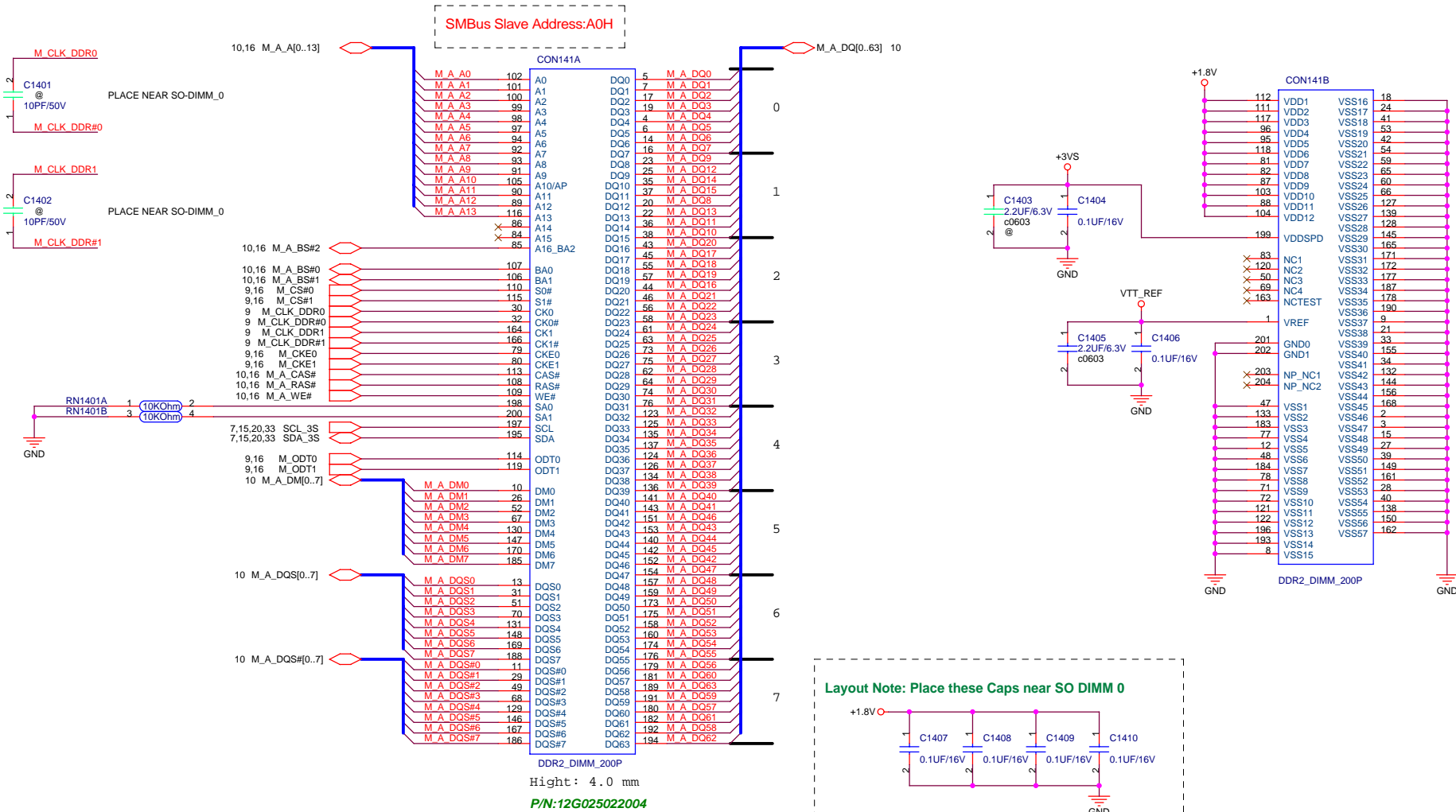
**LOW = NORMAL (Default)**  
 HIGH = LANES REVERSED

<Variant Name>

		Title : Calistoga--Strap	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name <b>T13F</b>		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet 13 of 63	

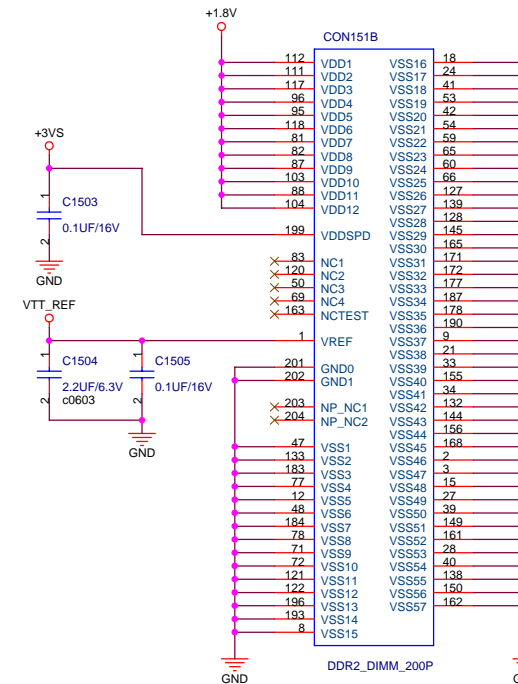


DDR2 HAD SWAPED.

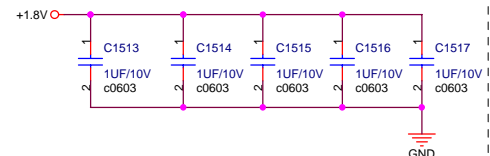



<Variant Name>

SMBus Slave Address:A4H



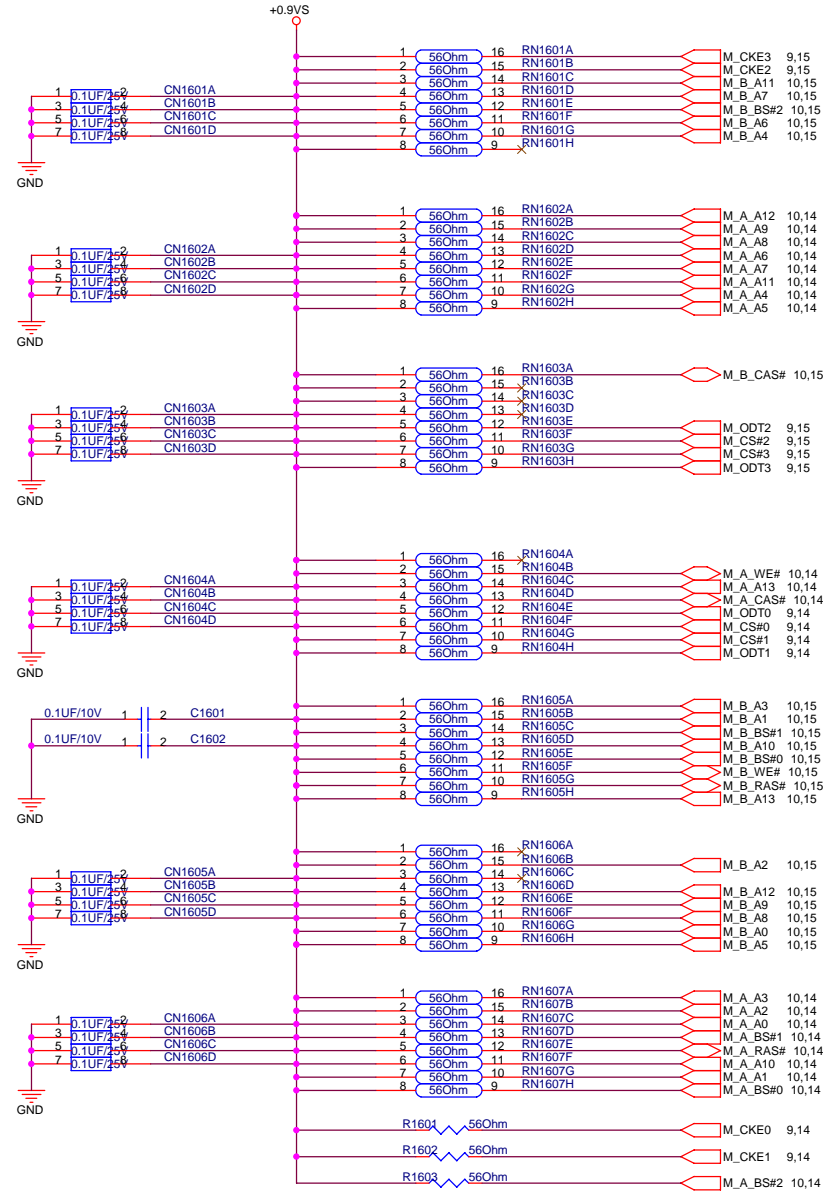
The diagram shows a parallel circuit with four capacitors, labeled C1506, C1507, C1508, and C1509. Each capacitor is rated at 0.1UF/16V. They are all connected to a +1.8V supply on one side and a common ground (GND) on the other side.



		<b>Title :</b> <u>DDR2 SO-DIMM_1</u>	
<b>ASUSTeK COMPUTER INC.</b>		<b>Engineer:</b> <u>Marco Chen</u>	
Size <u>Custom</u>	Project Name <b>T13F</b>		Rev <u>1.10</u>
Date: <u>Wednesday, August 30, 2006</u>		Sheet <u>15</u> of <u>63</u>	



DDR2 HAD SWAPED.

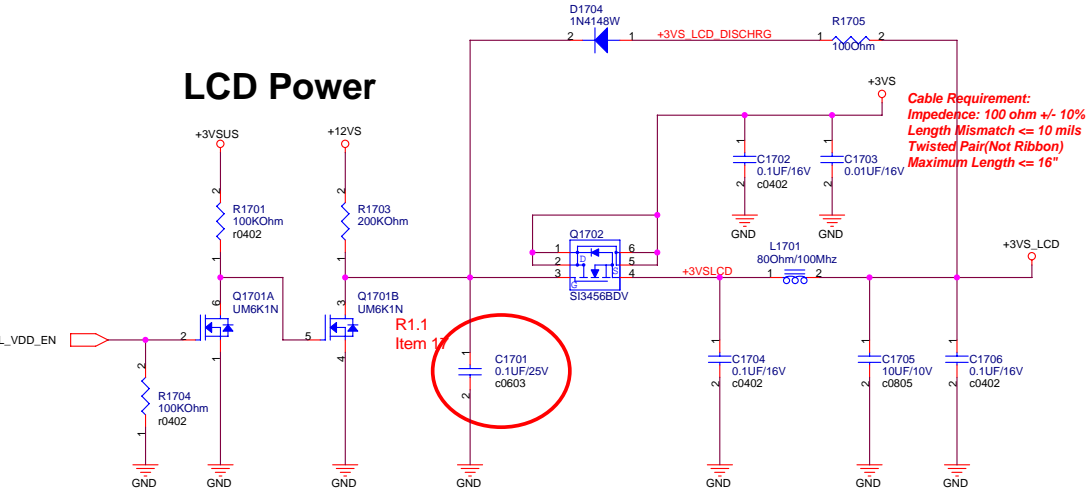


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

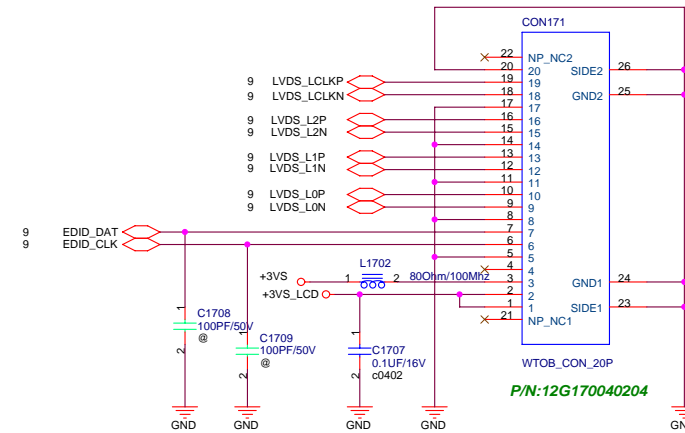
## LCD Backlight Control

### LCD Power

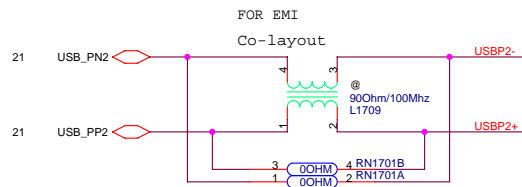
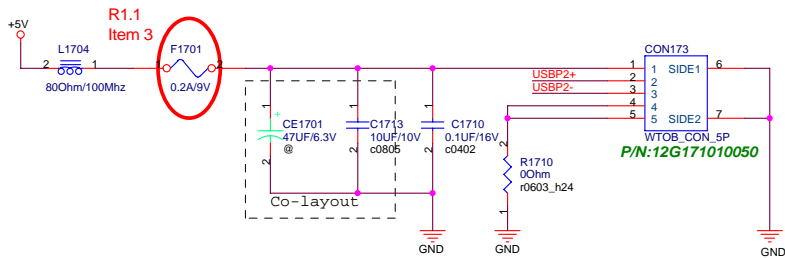


PR\_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

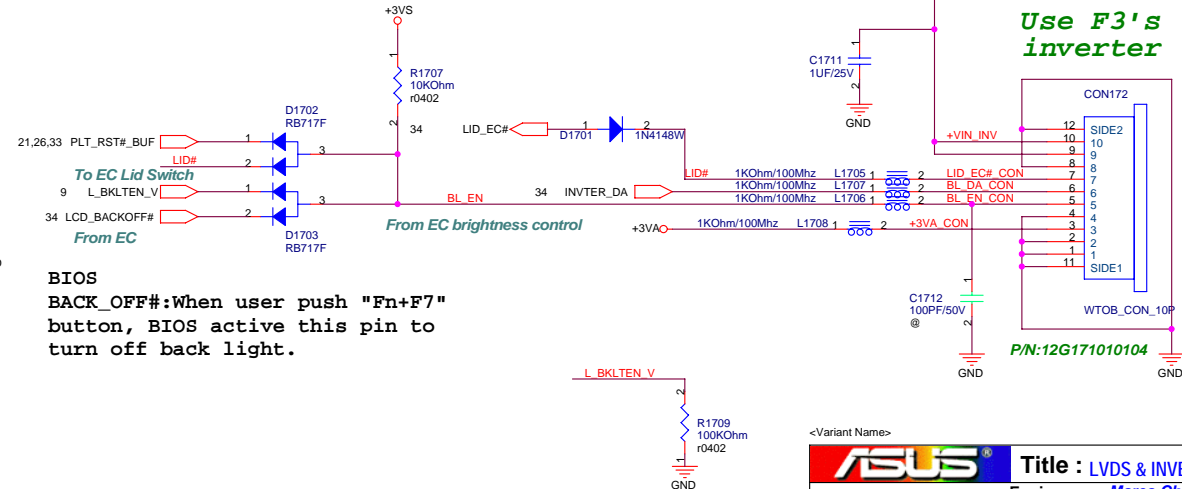
## LCD LVDS Interface



## CCD connector



## Inverter connector

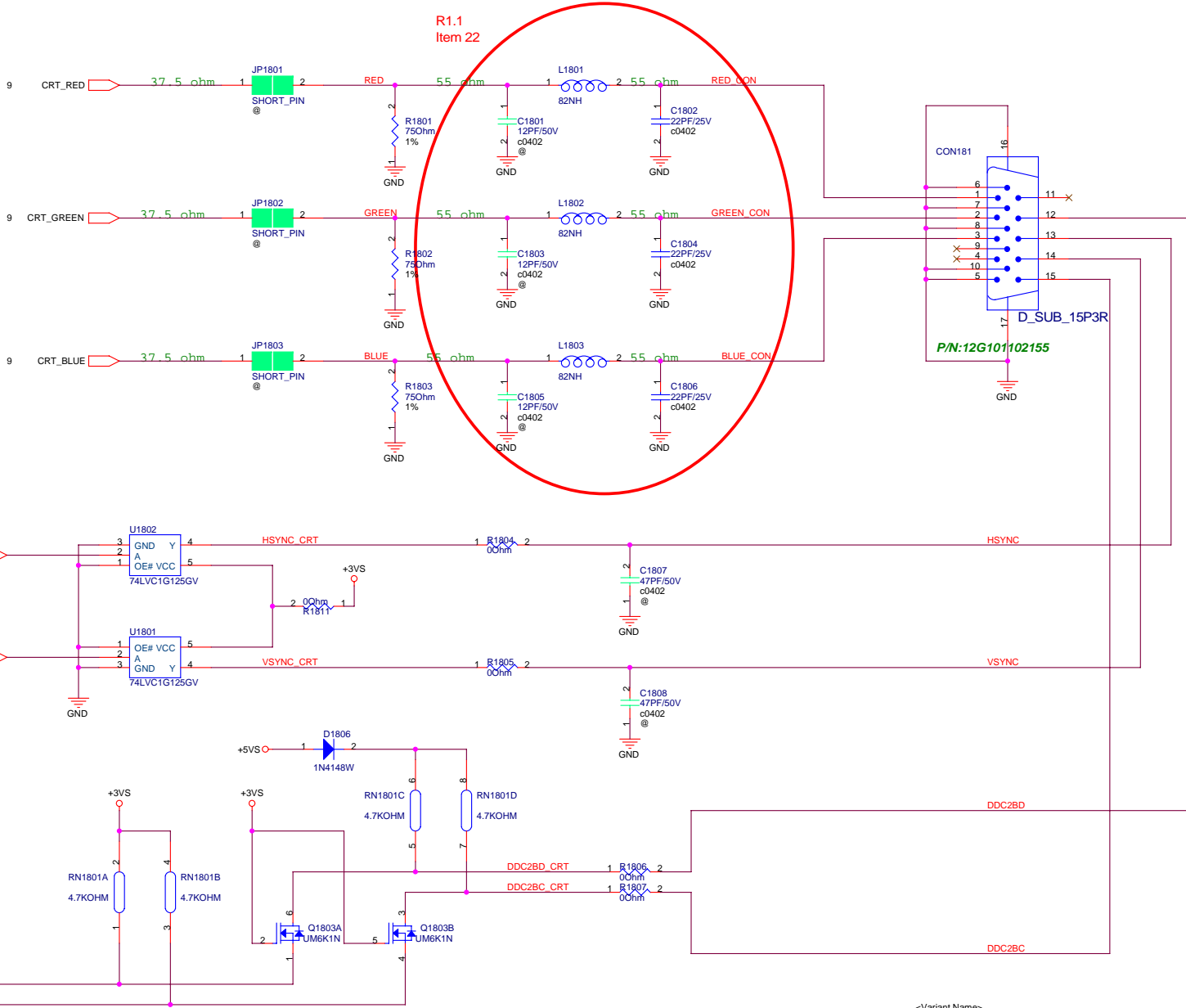
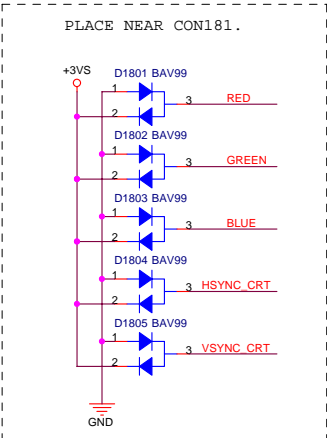


BIOS  
BACK\_OFF#: When user push "Fn+F7"  
button, BIOS active this pin to  
turn off back light.

<Variant Name>

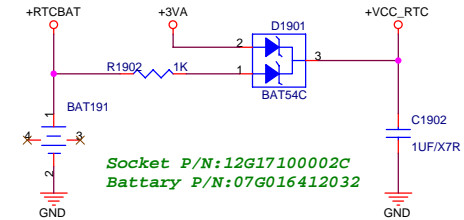
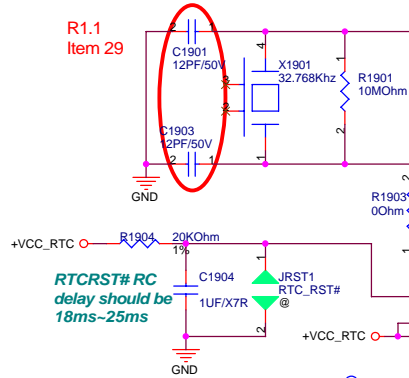
<b>ASUS</b>		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Custom	Rev
Custom	T13F		1.10
Date: Wednesday, August 30, 2006		Sheet 17 of 63	

**CRT**

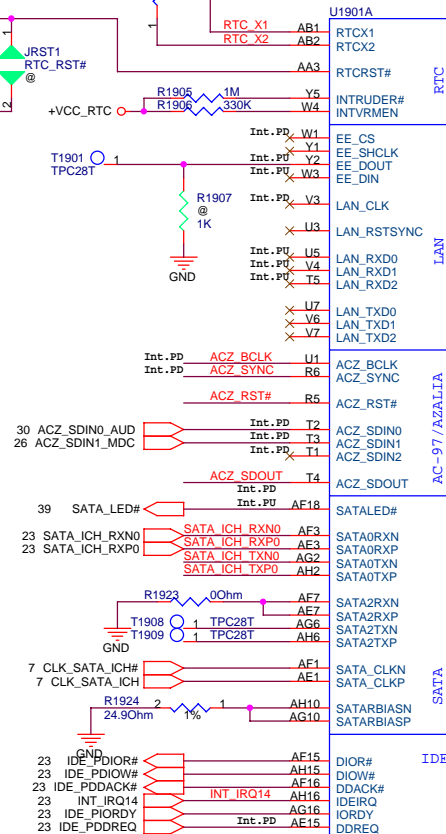
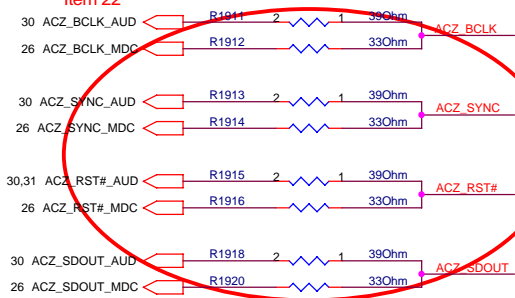


Request of CSC for CMOS clear function

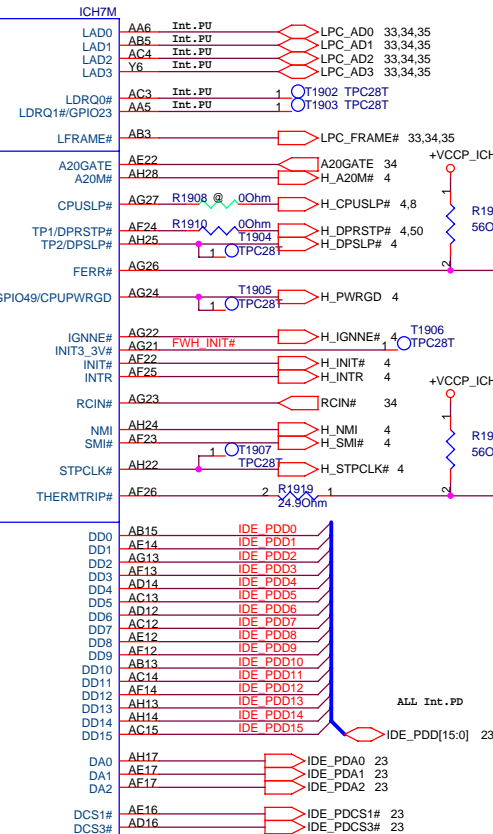
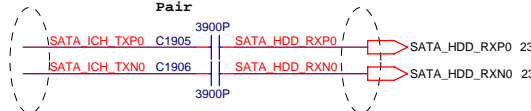
R1.1  
Item 29



R1.1  
Item 22



Differential Pair

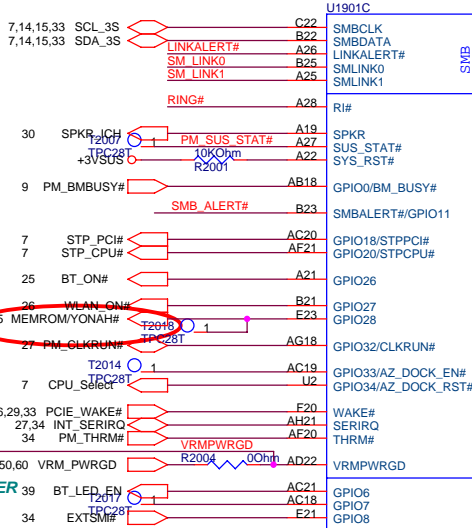


<Variant Name>

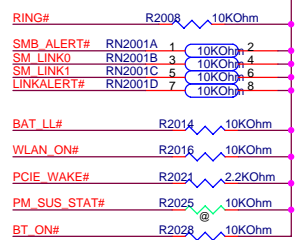
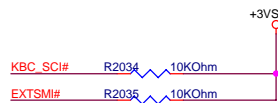
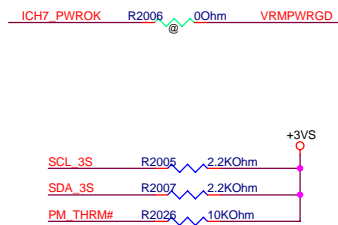
<b>ASUS</b>		Title : ICH7M (1)	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F	Rev 1.10	
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# To new card check power plane

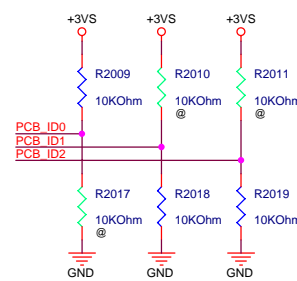
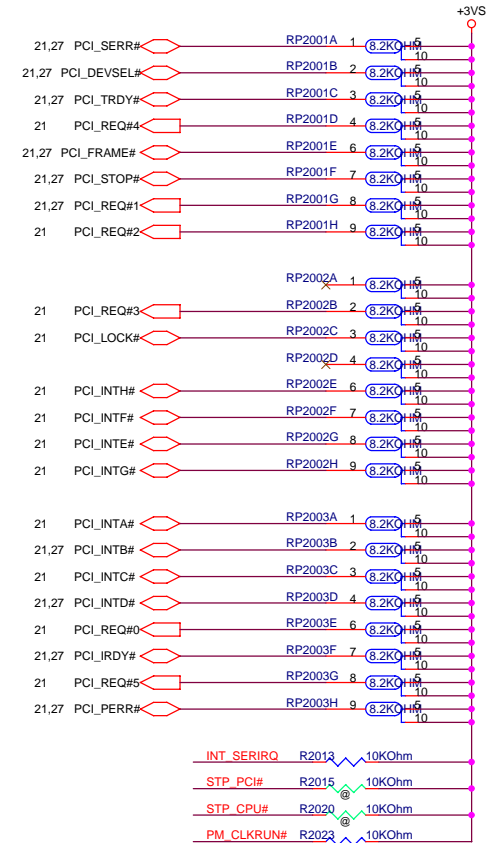
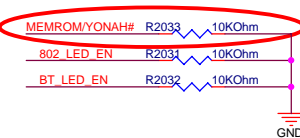
Clock Generator  
DDR2 SO-DIMM



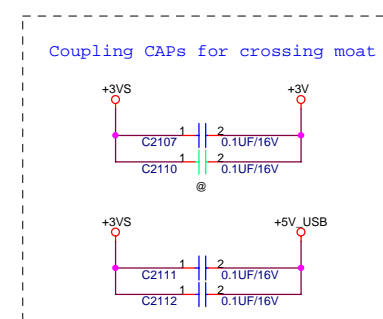
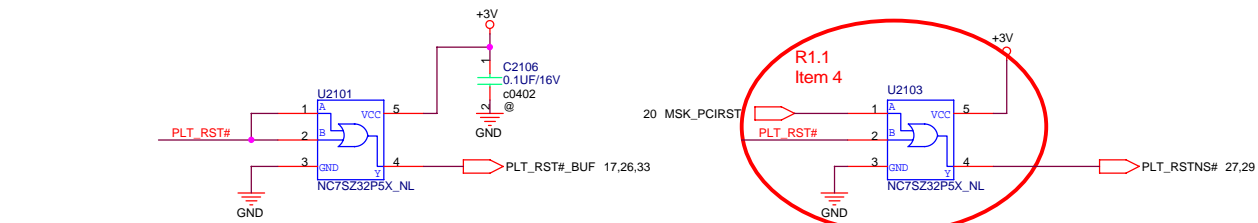
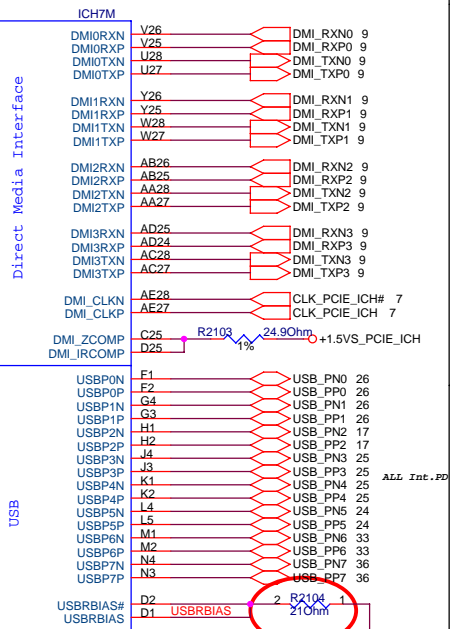
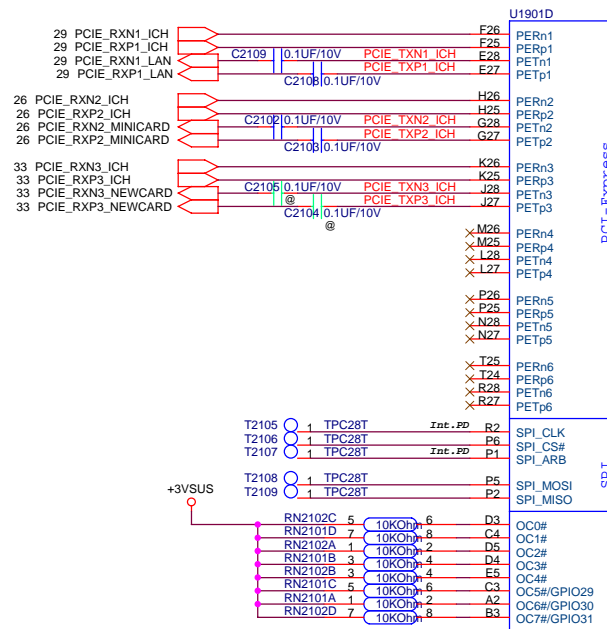
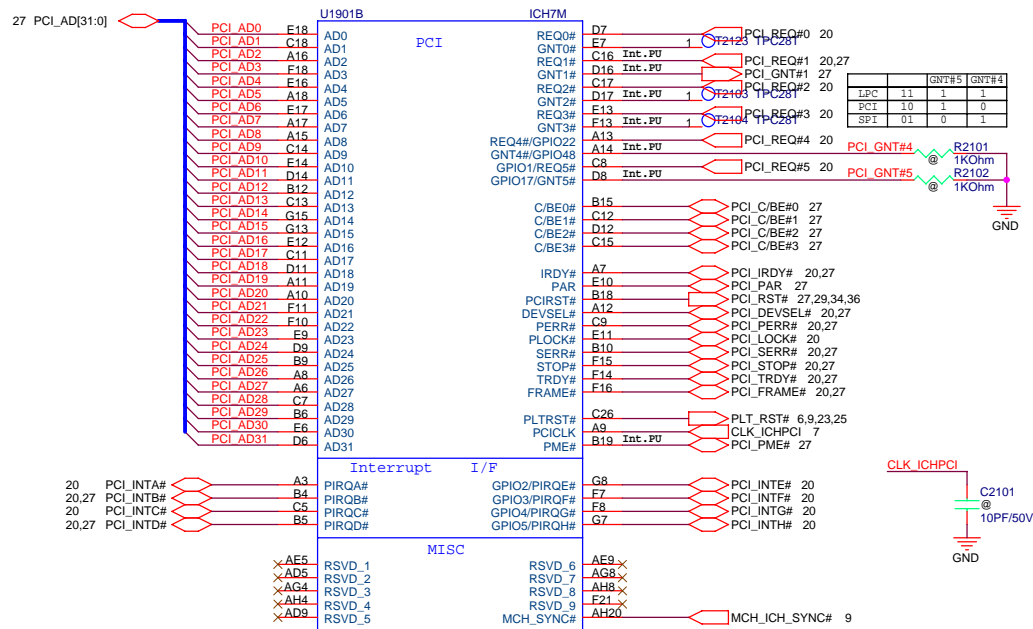
R1.1  
Item 12



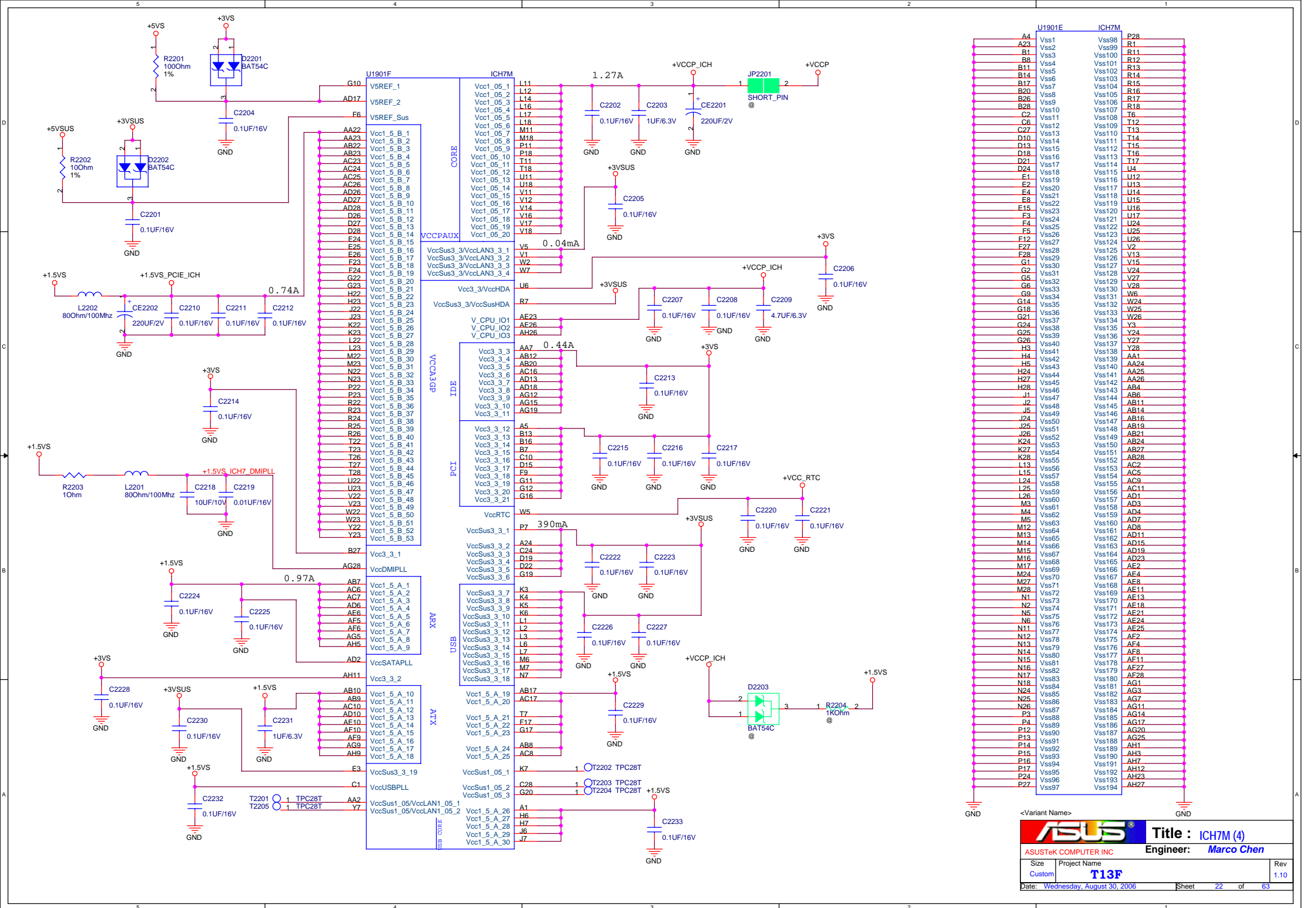
R1.1  
Item 12



<Variant Name>

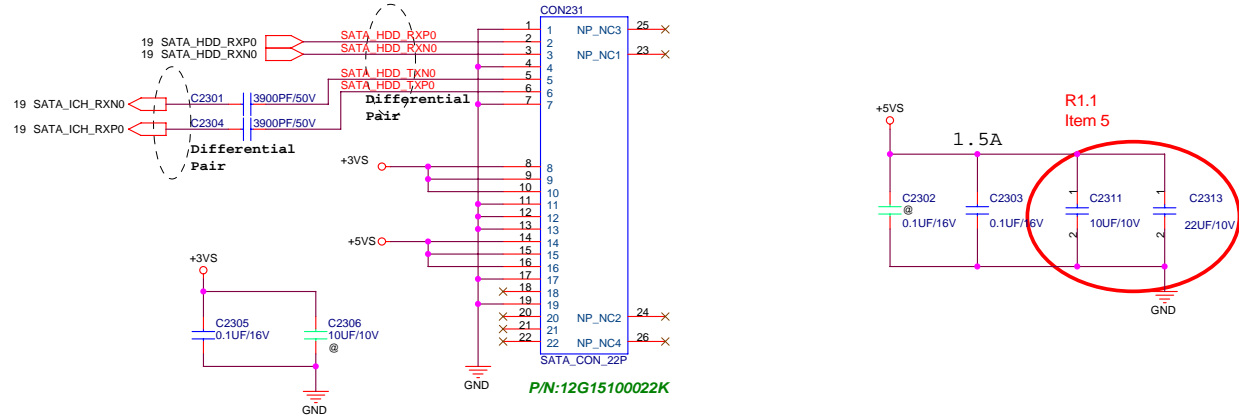


USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER

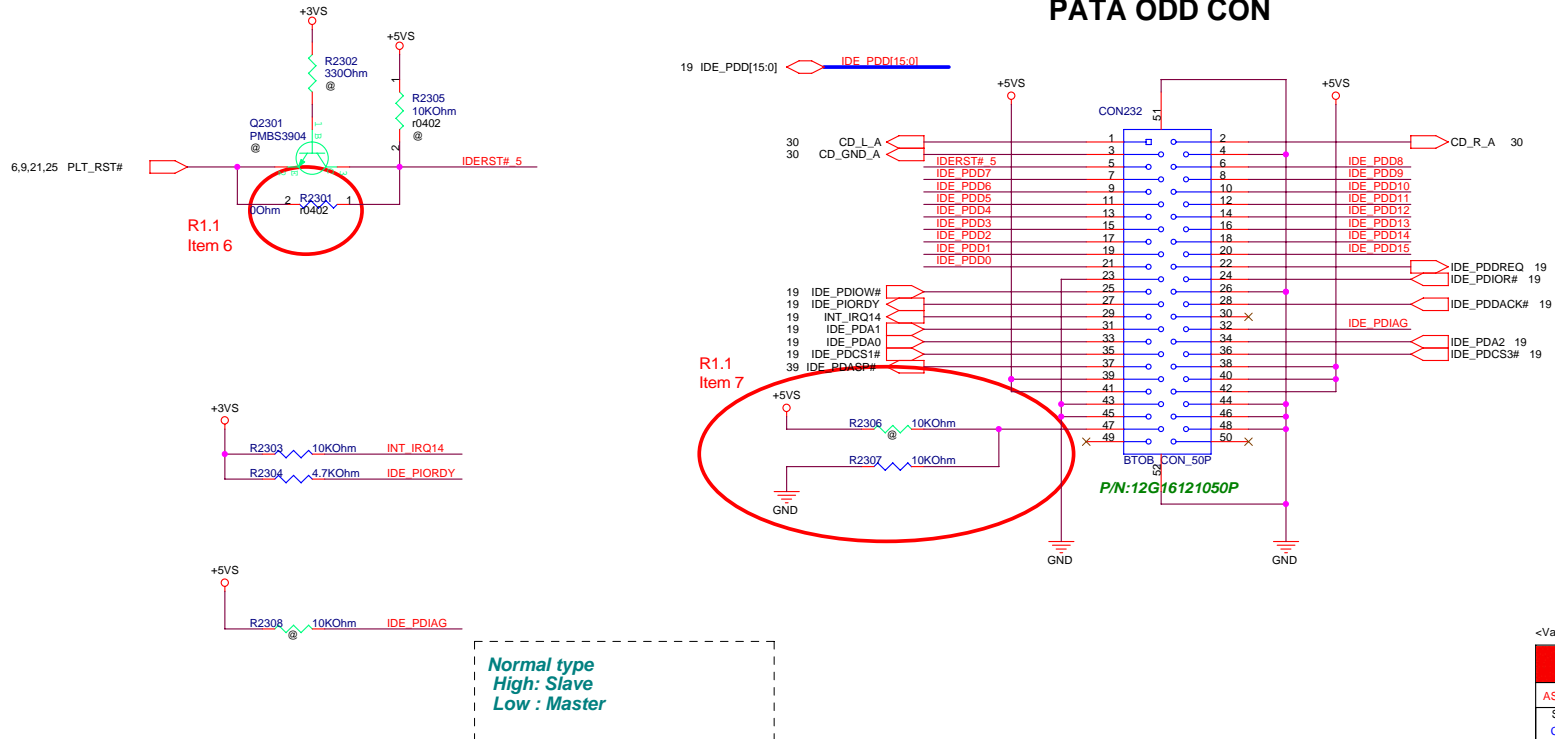




## SATA HDD CON

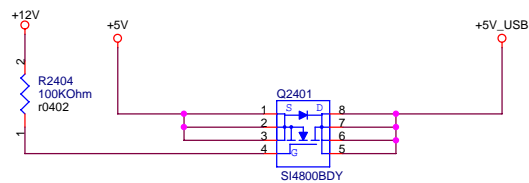
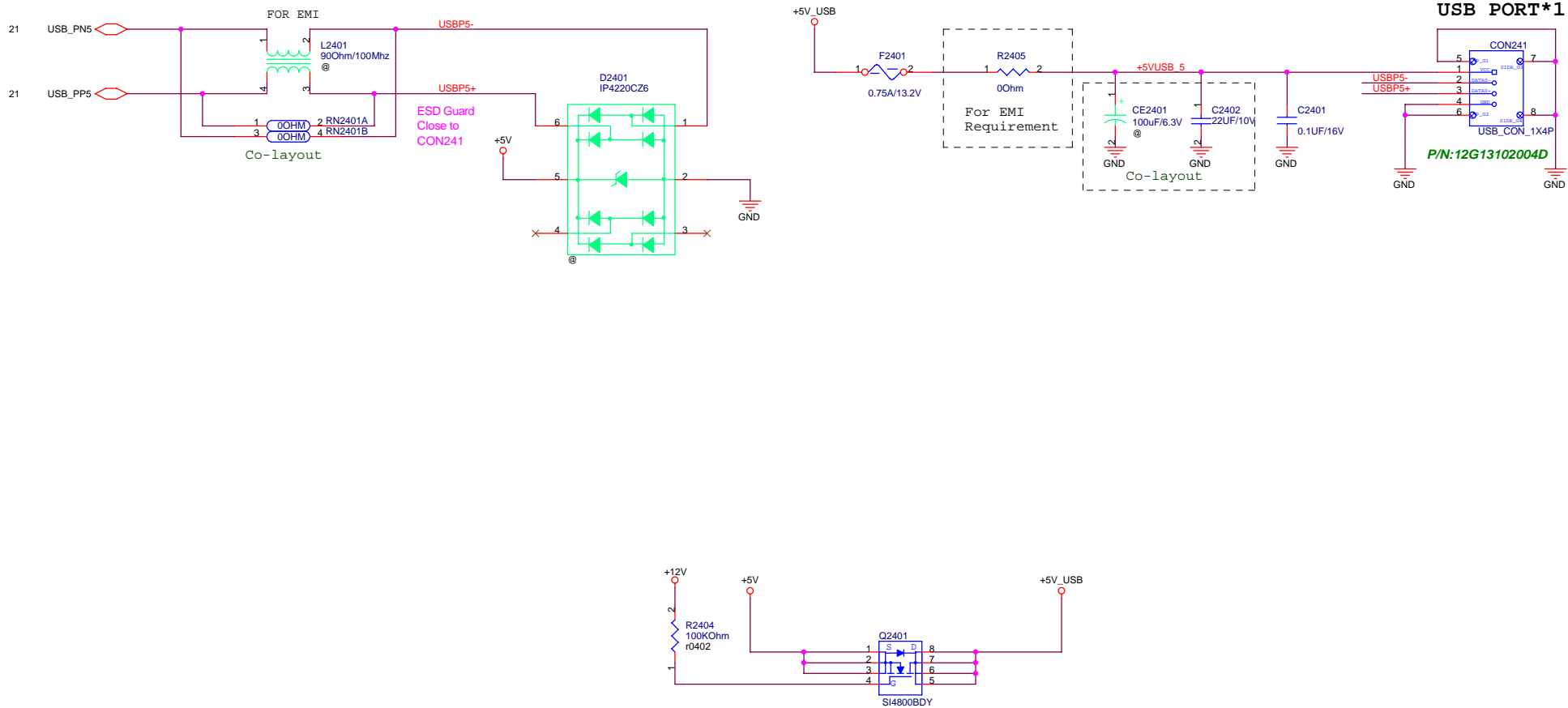


## PATA ODD CON




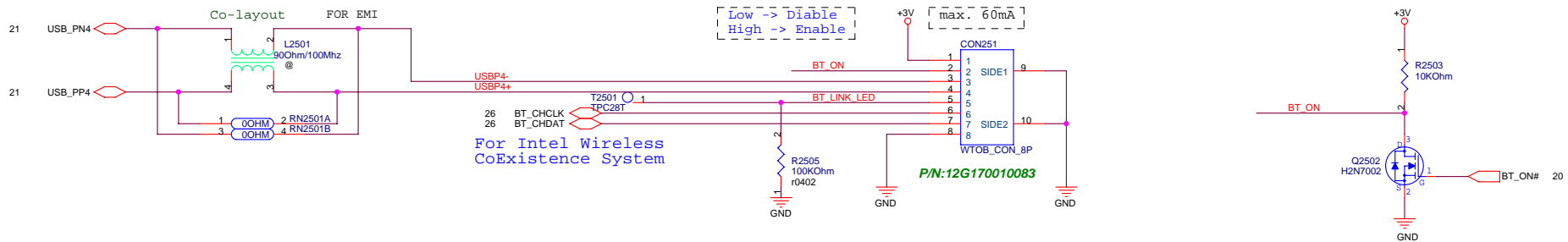
<Variant Name>

		Title : HDD & ODD	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
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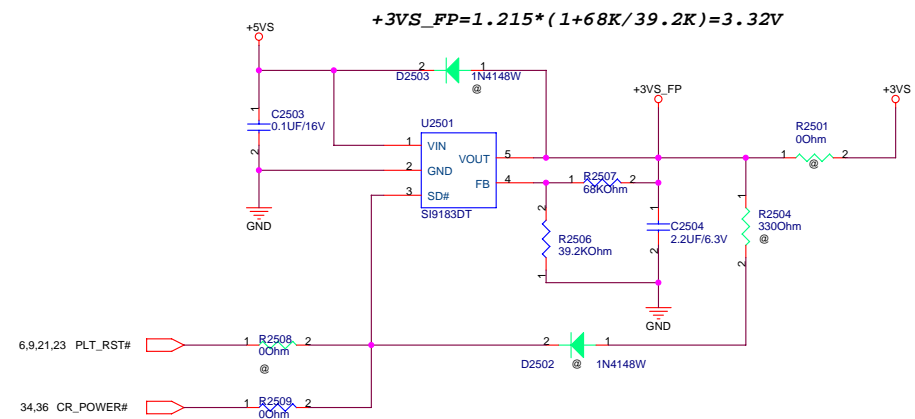
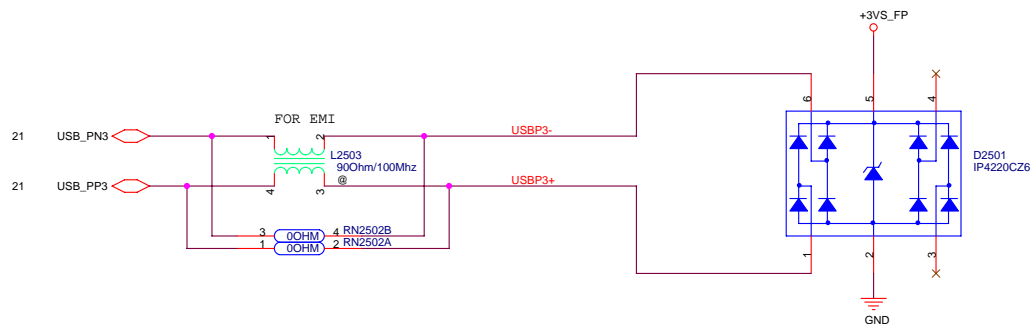
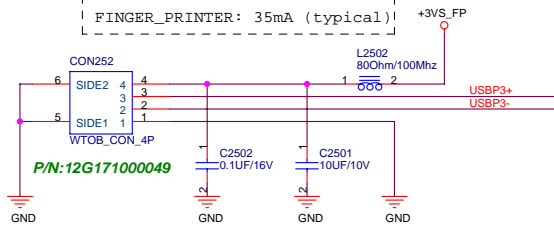
<Variant Name>

		<b>Title :</b> USB PORT	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> Marco Chen	
Size Custom	Project Name <b>T13F</b>		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet 24 of 63	



## Finger Printer

FINGER\_PRINTER: 35mA (typical)



<Variant Name>

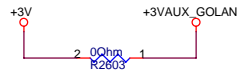
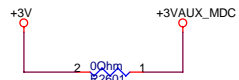
		Title : BT & FP	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet	25 of 63

**POWER CONSUMPTION:**  
**+3VS: +3.003V~+3.597V**  
**Max= 750 mA**

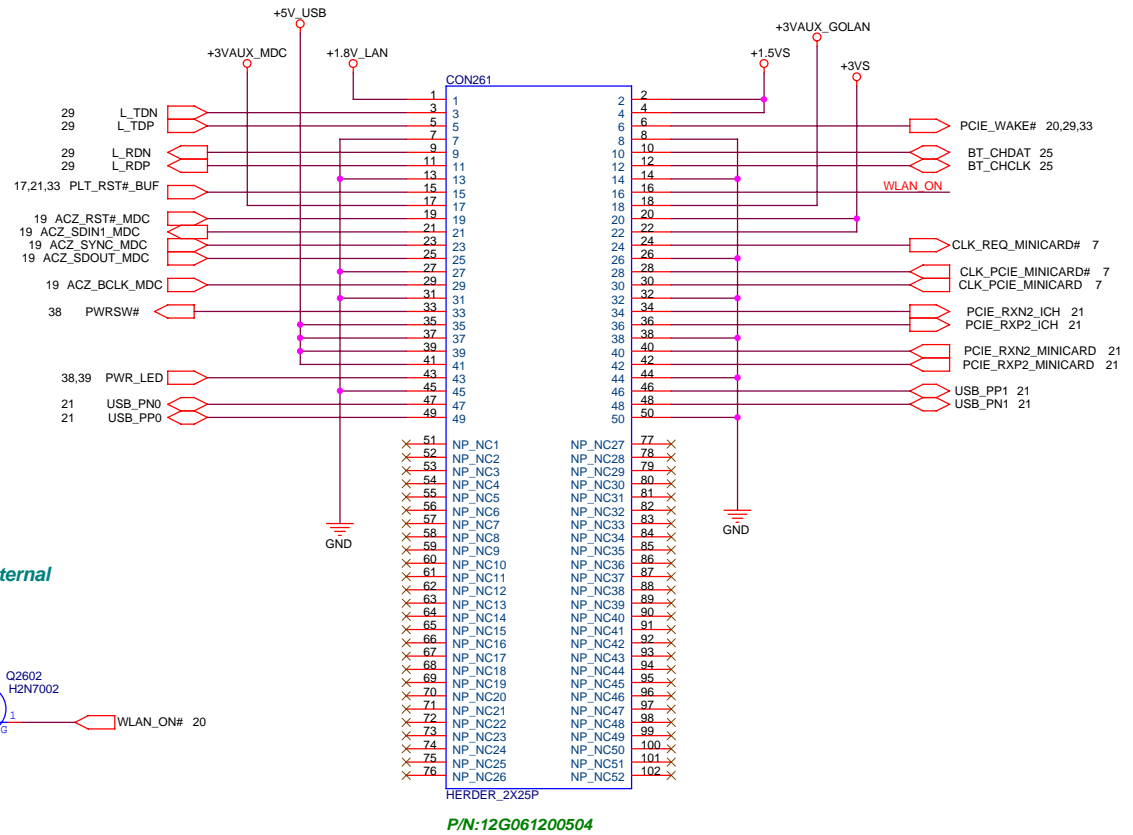
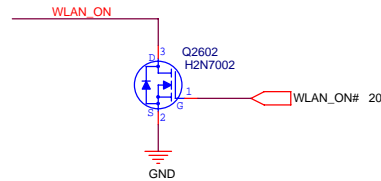
**+1.5VS: +1.425V~+1.575V**  
**Max= 375 mA**

**+3VAUX\_GOLAN: +3.003V~+3.597V**  
**Max= 250 mA**

**+3VAUX\_MDC: +3.003V~+3.597V**  
**Max= 300 mA**

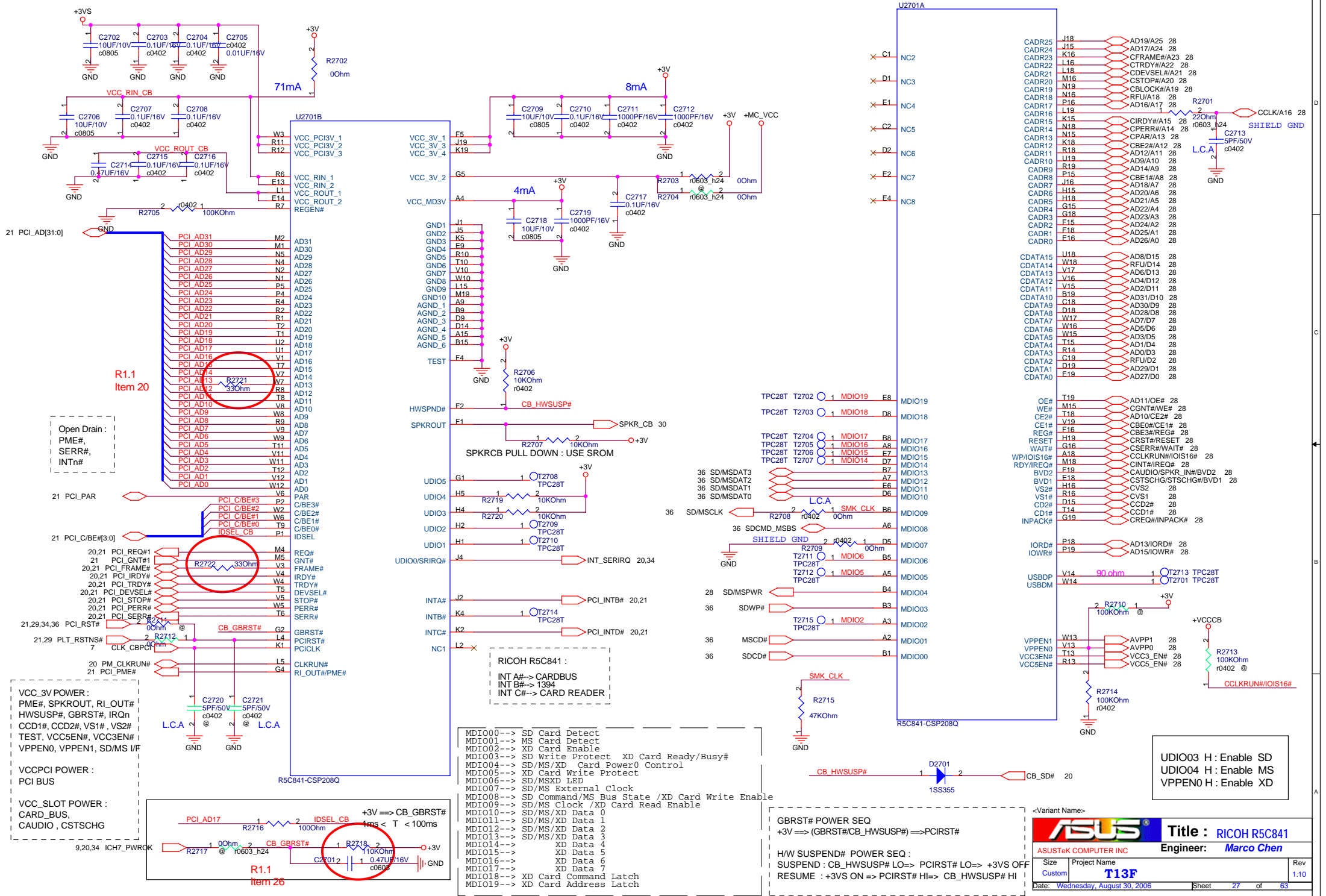


**Intel SPEC(18780):Internal**  
**Pull UP 110Kohm**



<Variant Name>

<b>ASUS</b>		<b>Title : B TO B CONN(M)</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size Custom	Project Name <b>T13F</b>	Rev 1.10	
Date: Wednesday, August 30, 2006		Sheet 26 of 63	

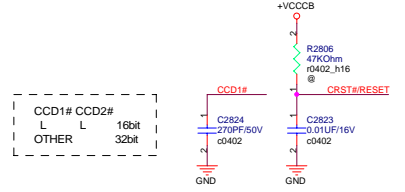
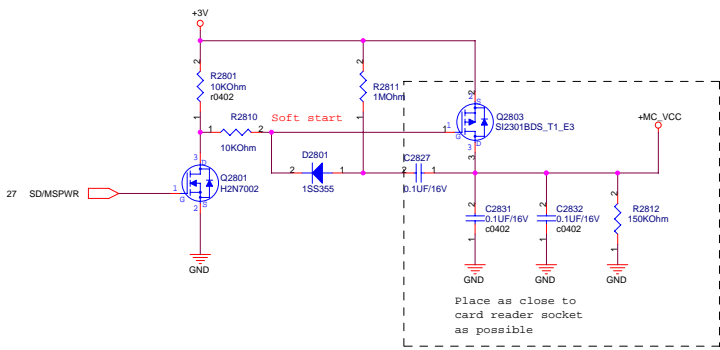
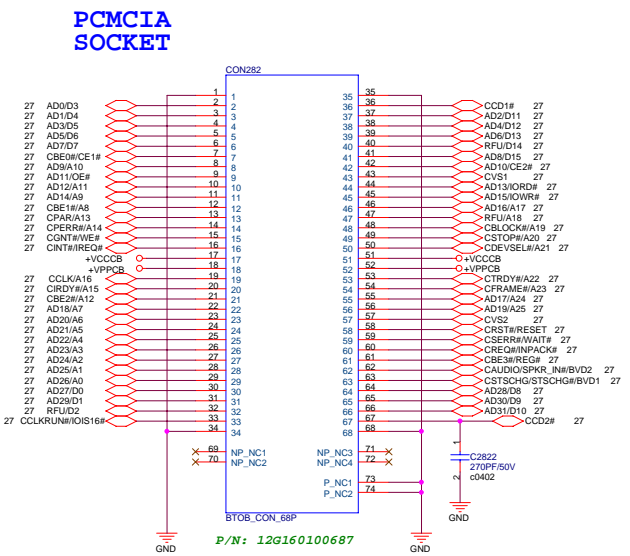
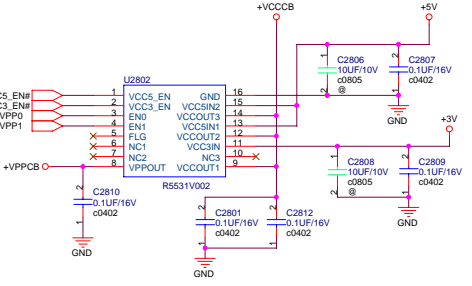
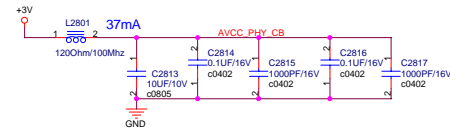
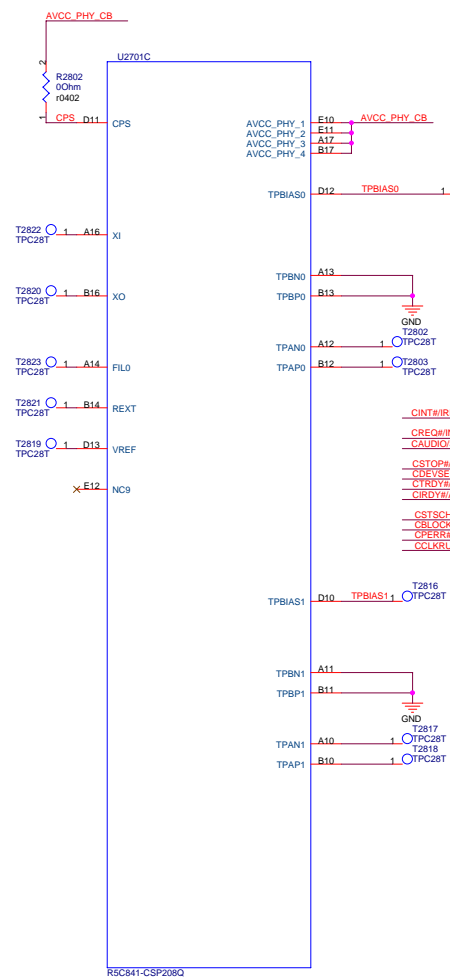


MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO02-->	XD Card Enable
MDIO03-->	SD Write Protect    XD Card Ready/Busy#
MDIO04-->	SD/MS/XD    Card Power0 Control
MDIO05-->	XD Card Write Protect
MDIO06-->	SD/MSXD LED
MDIO07-->	SD/MS External Clock
MDIO08-->	SD Command/MS Bus State /XD Card Write Enable
MDIO09-->	SD/MS Clock /XD Card Read Enable
MDIO10-->	SD/MS/XD Data 0
MDIO11-->	SD/MS/XD Data 1
MDIO12-->	SD/MS/XD Data 2
MDIO13-->	SD/MS/XD Data 3
MDIO14-->	XD Data 4
MDIO15-->	XD Data 5
MDIO16-->	XD Data 6
MDIO17-->	XD Data 7
MDIO18-->	XD Card Command Latch
MDIO19-->	XD Card Address Latch

GBRST# POWER SEQ  
+3V ==> (GBRST#/CB\_HWSUSP#) ==> PCIRST#

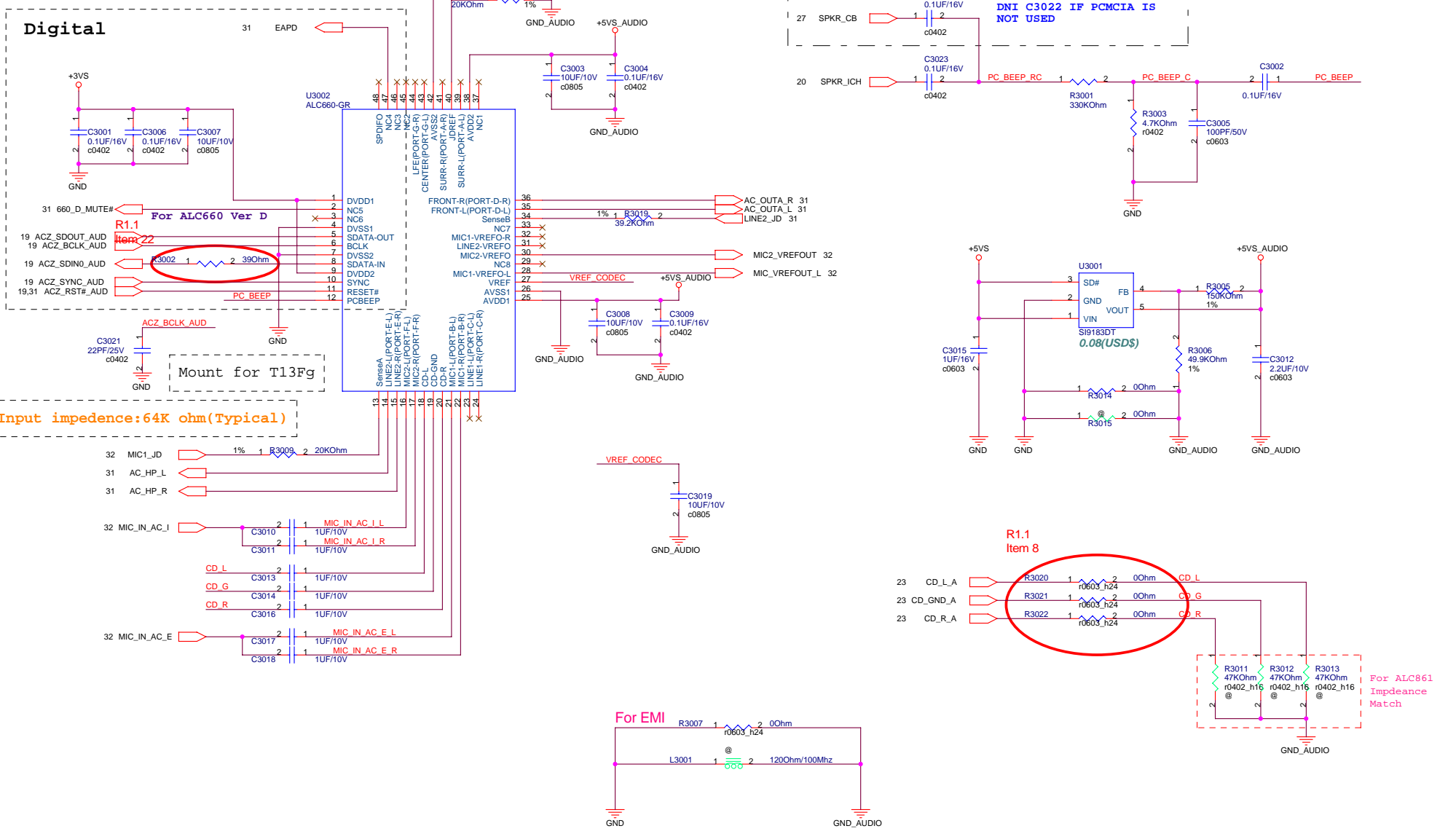
H/W SUSPEND# POWER SEQ :  
SUSPEND : CB\_HWSUSP# LO=> PCIRST# LO=> +3VS OFF  
RESUME : +3VS ON => PCIRST# HI=> CB\_HWSUSP# HI

<Variant Name>		ASUS®		Title : RICOH R5C841	
ASUSTek COMPUTER INC		Engineer: Marco Chen			
Size	Project Name	T13F		Rev	
Custom				1.10	
Date: Wednesday, August 30, 2006		Sheet		27 of 63	

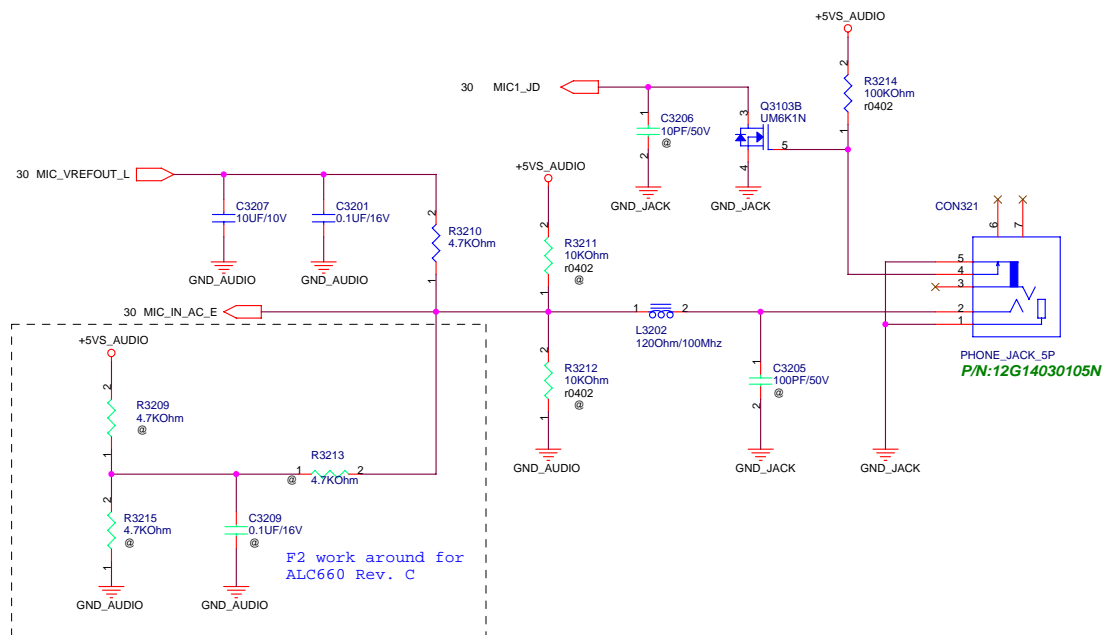
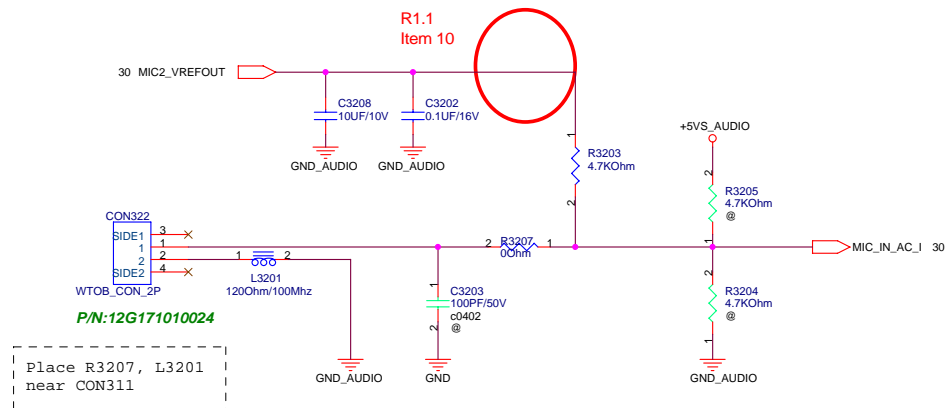






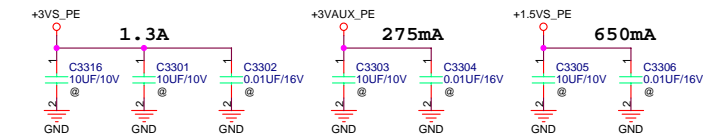
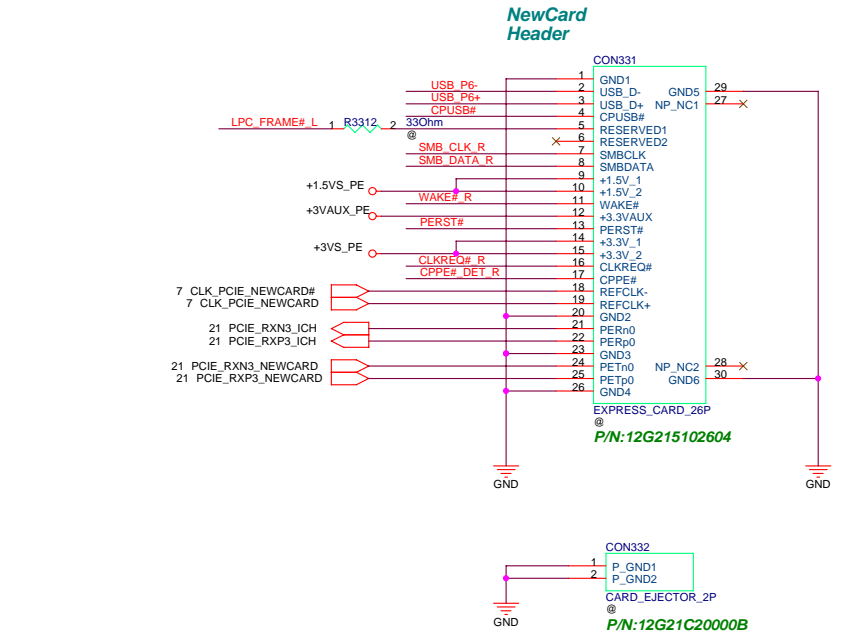
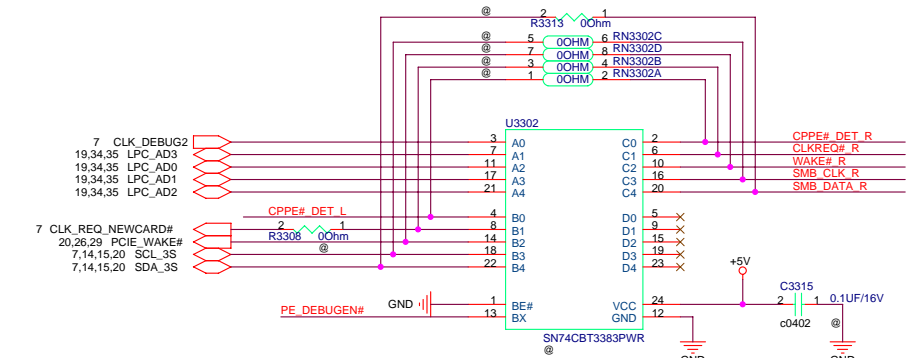
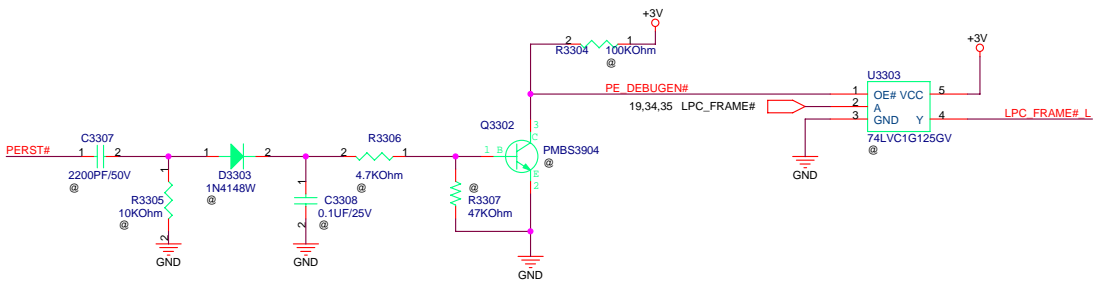
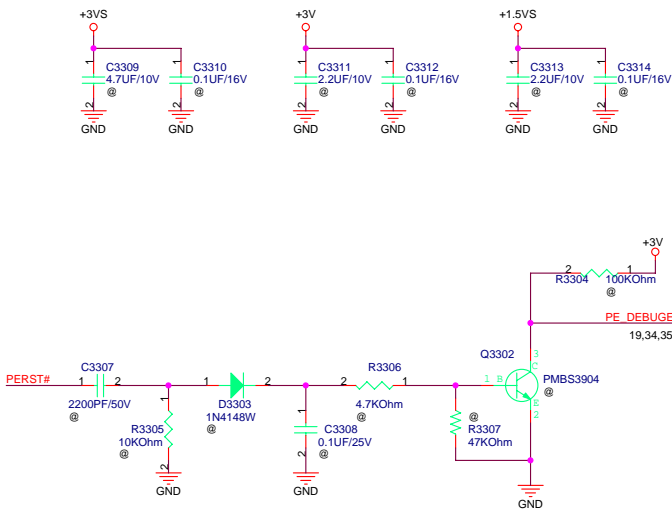
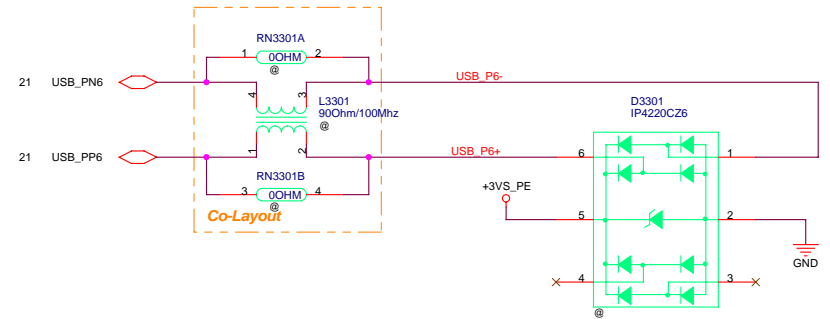
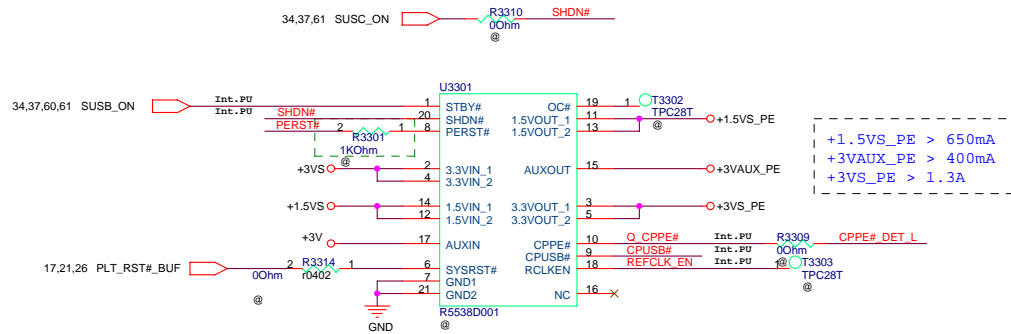






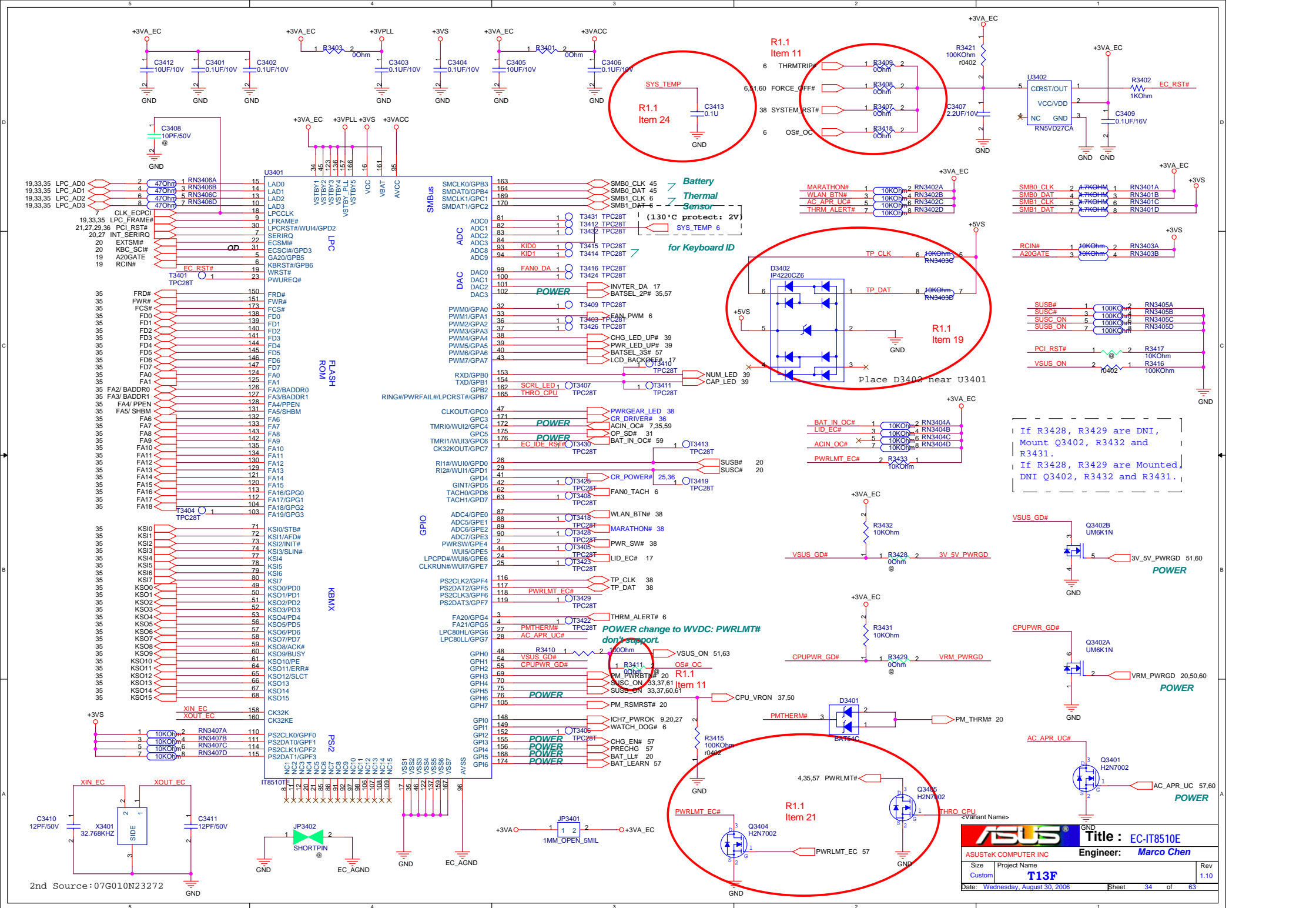
<Variant Name>

		Title : <b>MICROPHONE</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Marco Chen</b>	
Size Custom	Project Name <b>T13F</b>		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet 32 of 63	



<Variant Name>

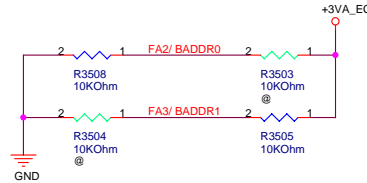
<b>ASUS</b>		Title :	NEWCARD
ASUSTek COMPUTER INC		Engineer:	Marco Chen
Size	Project Name		Rev
Custom	T13F		1.10
Date: Wednesday, August 30, 2006		Sheet	33 of 63



## EC Hardware Strapping

### FA2/ BADDR0 & FA3/ BADDR1

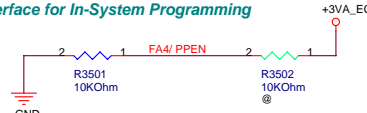
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

### FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

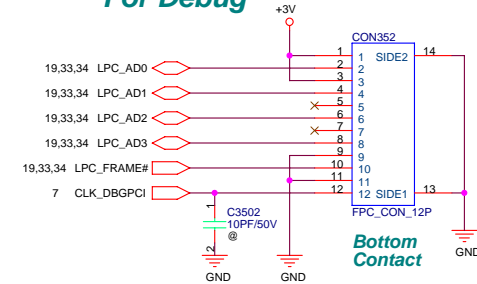


### FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

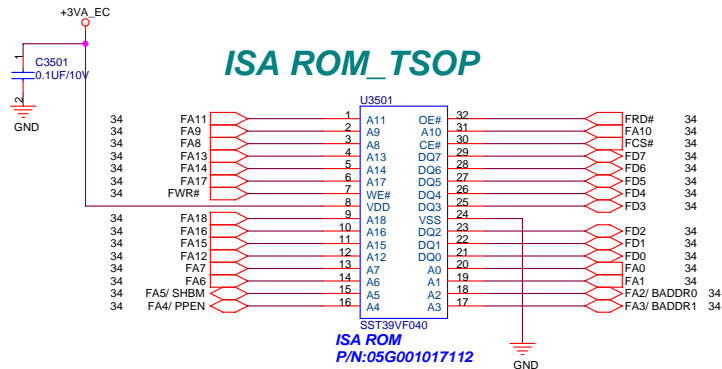


## For Debug



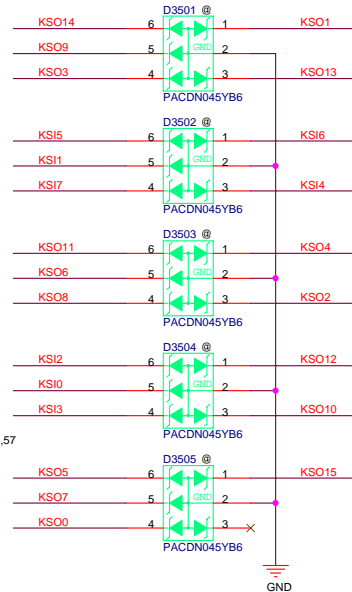
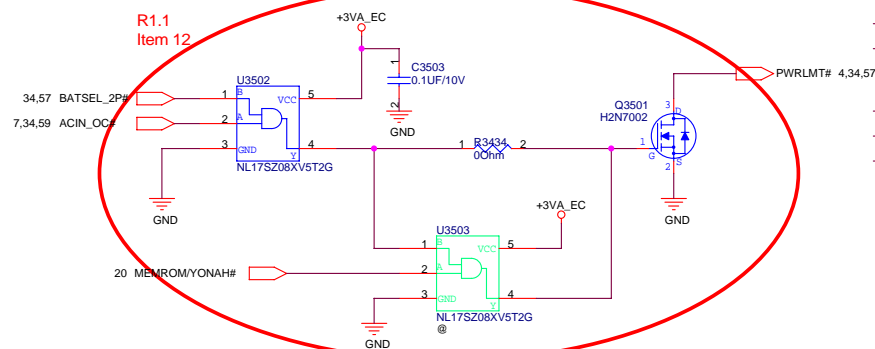
P/N:12G183301208

## ISA ROM\_TSOP

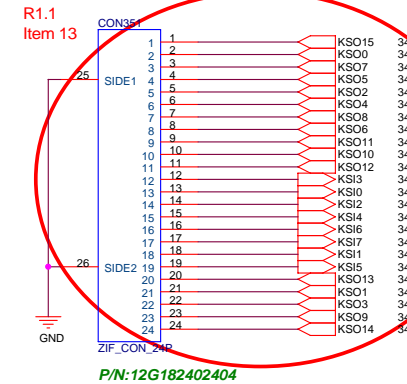


ISA ROM  
P/N:05G001017112

R1.1  
Item 12



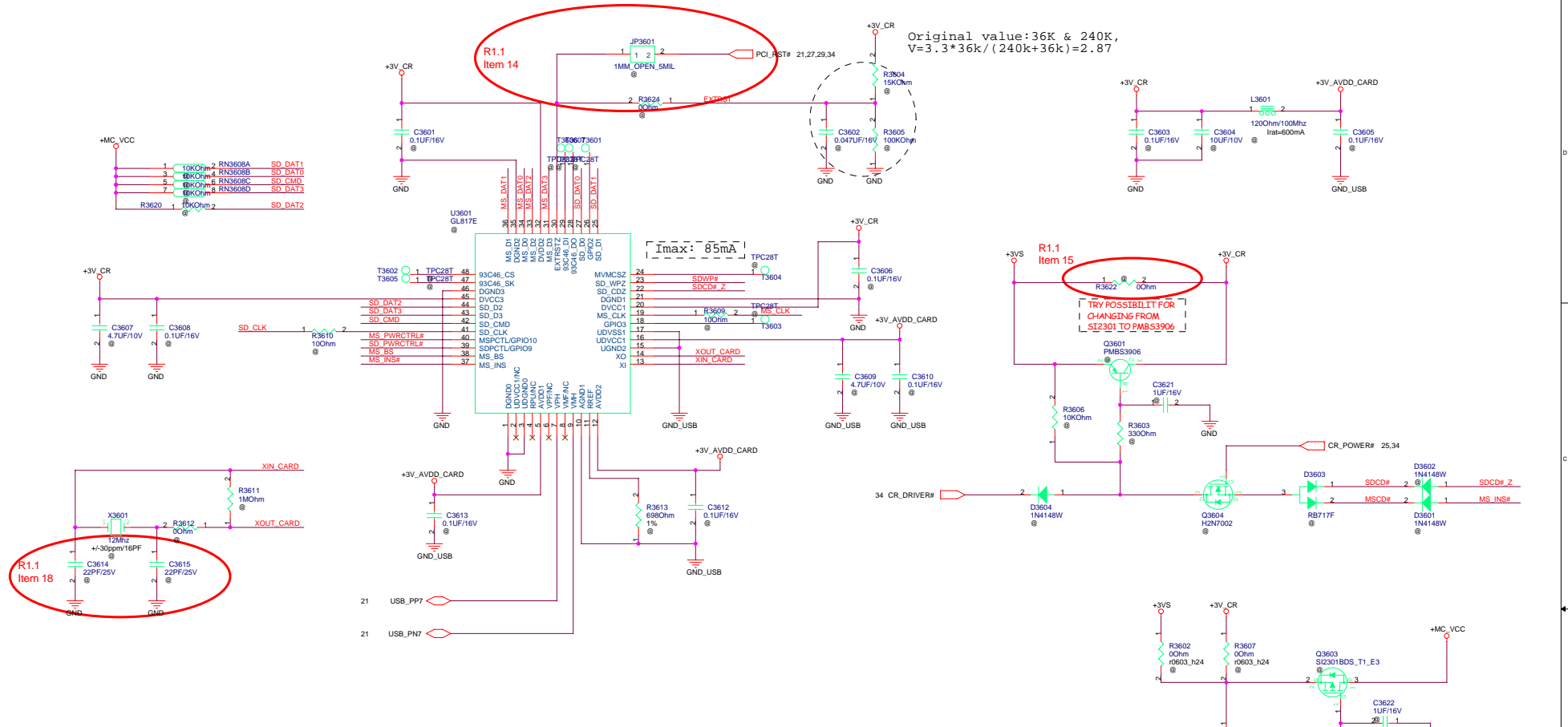
## For Keyboard



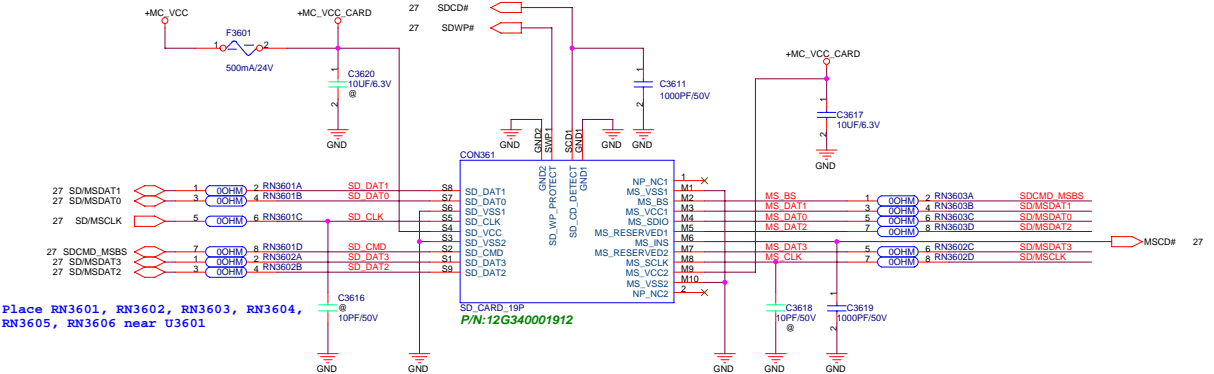
P/N:12G182402404

<Variant Name>

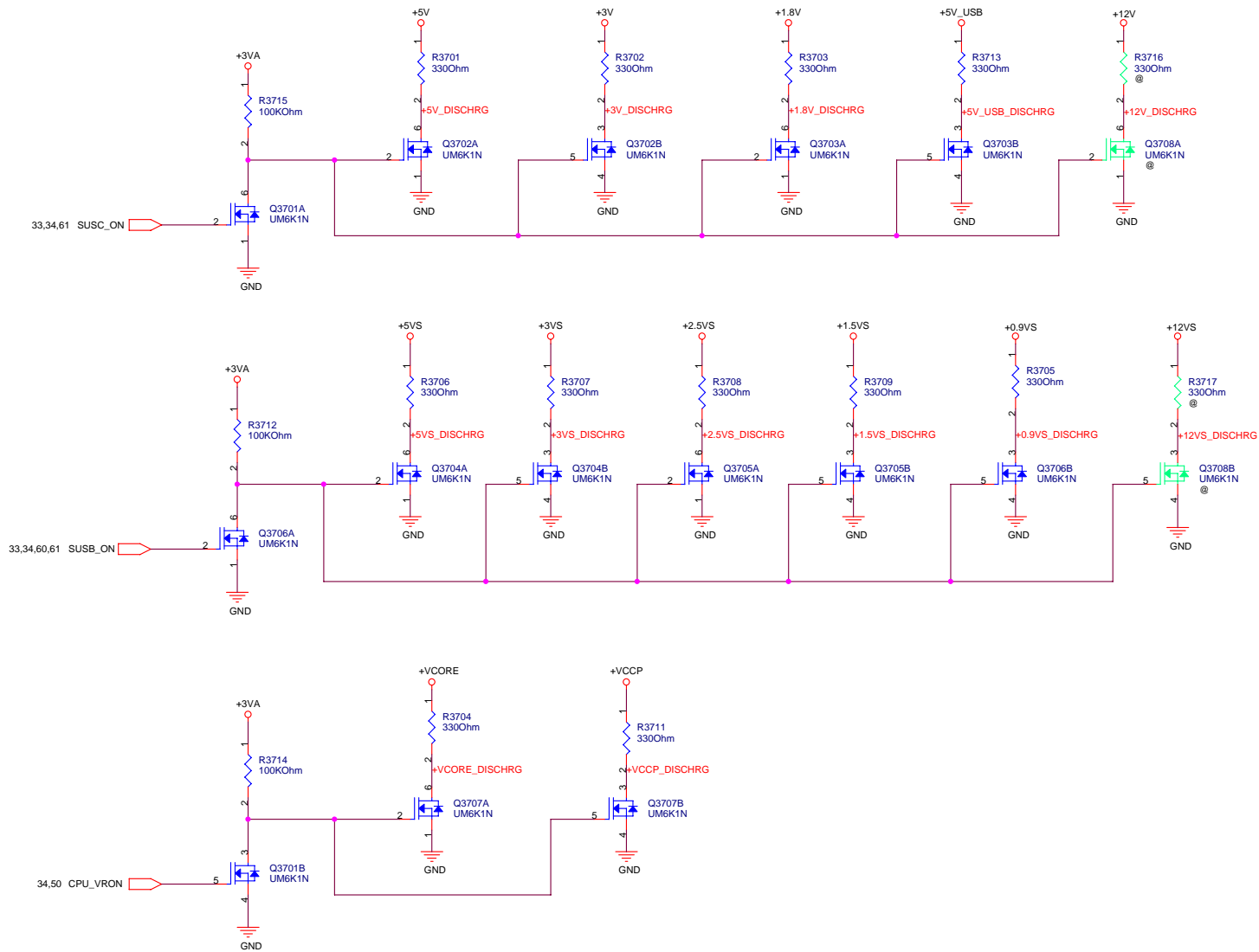
		Title :ISA_ROM&KB conn	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name <b>T13F</b>		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet 35	of 63



DNI RN3601, RN3602, RN3603, RN3604,  
 RN3605, RN3606 BY USING GL817E.



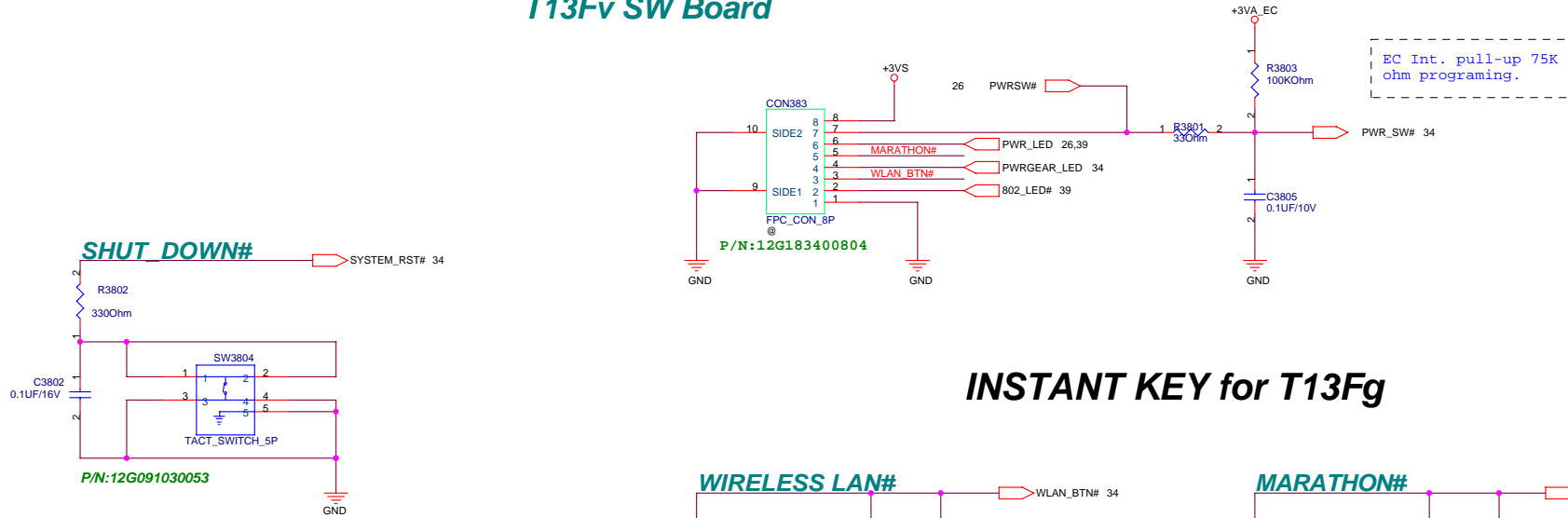




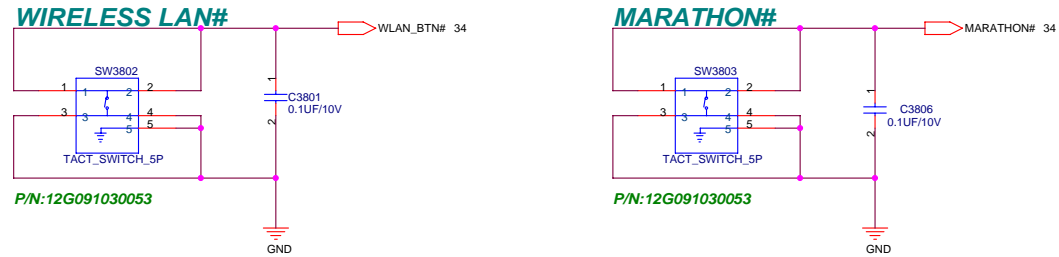
<Variant Name>

		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Wednesday, August 30, 2006		Sheet 37 of 63	

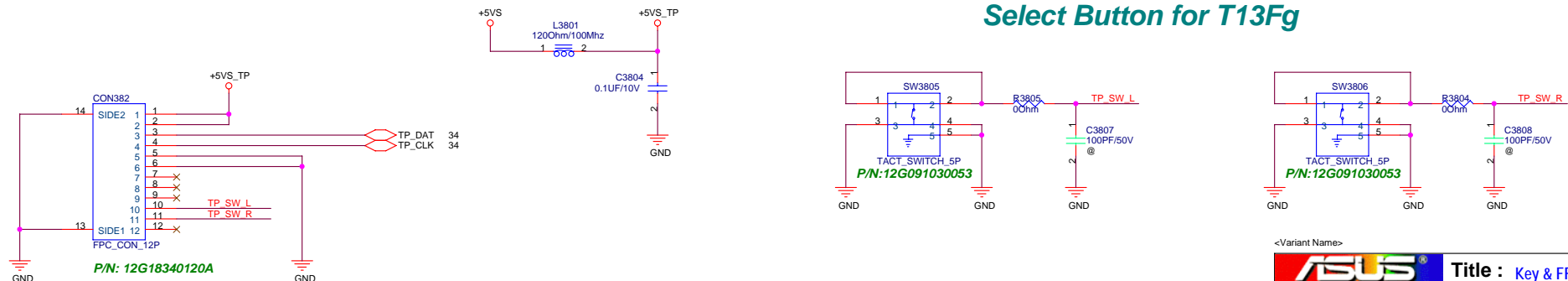
## FFC CONNECTER for T13Fv SW Board



## INSTANT KEY for T13Fg



## Select Button for T13Fg

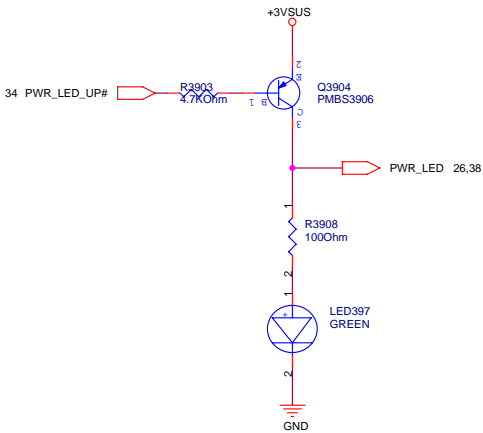


<Variant Name>

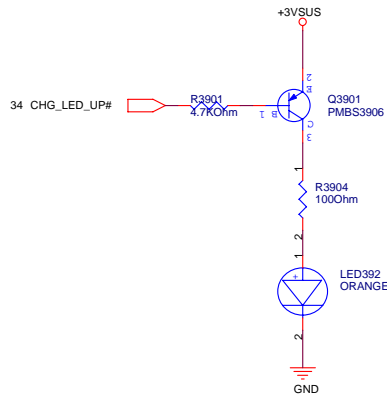
<b>ASUS</b>		Title : Key & FFC CONN	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Wednesday, August 30, 2006		Sheet 38 of 63	

PR\_NOTE: Change all LED series resistors from 0402 to 0603 type and change color from green to blue.

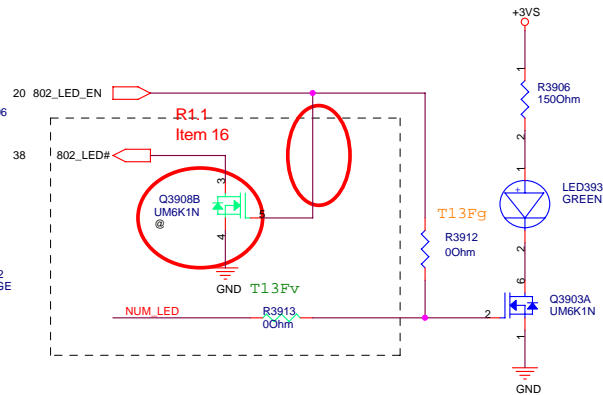
### For POWER LED



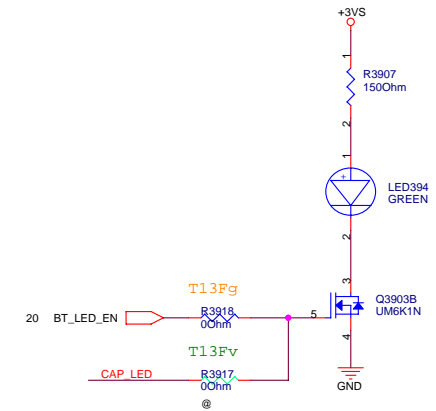
### For BATTERY LED



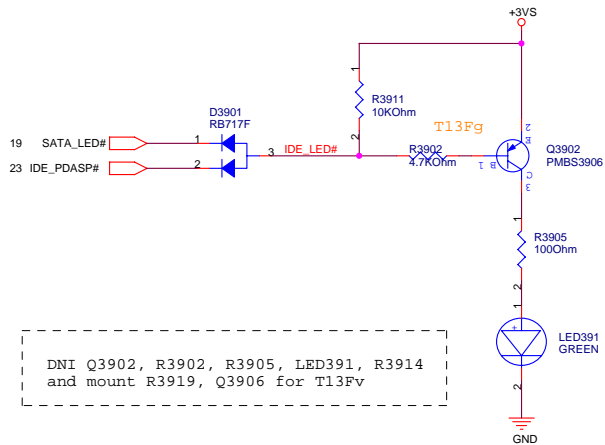
### For WireLess LED



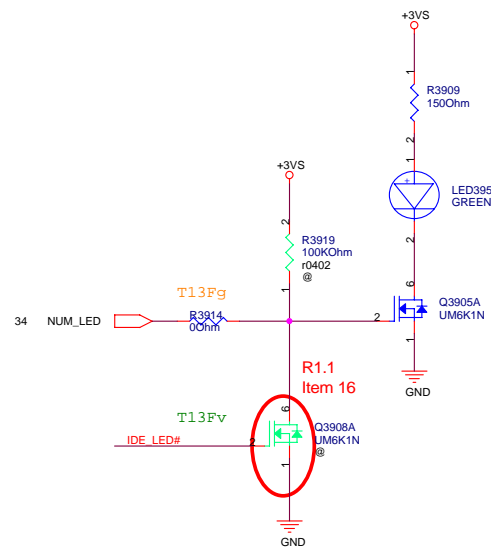
### For BT LED



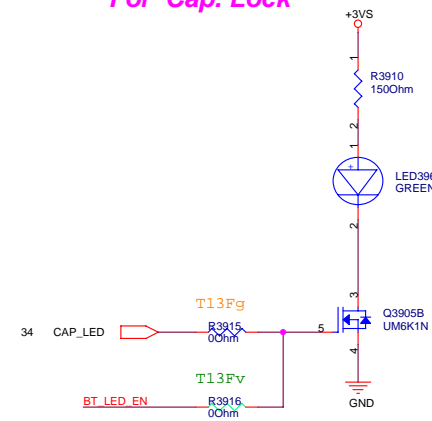
### For SATA/IDE LED



### For Num Lock



### For Cap. Lock



DNI Q3902, R3902, R3905, LED391, R3914 and mount R3919, Q3906 for T13Fv

<Variant Name>

<b>ASUS</b>		Title : LEDs	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Wednesday, August 30, 2006		Sheet 39 of 63	

3

6

3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13F</b>
--------------	-------------

Rev
1.10

Date: Wednesday, August 30, 2006

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3

6

3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

Project Name	<b>T13F</b>
--------------	-------------

Rev
1.10

Date: Wednesday, August 30, 2006

Sheet 41 of 63

3

6

3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*


Size  
Custom

Project Name	<b>T13F</b>
--------------	-------------

Rev
1.10

Date: Wednesday, August 30, 2006

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	5	4	3	2	1						
D											
C											
B											
A											
					<Variant Name>						
					<div><div><div><div>Title : EMPTY</div><div>ASUSTeK COMPUTER INC</div><div>Engineer: Marco Chen</div></div></div><table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>Custom</td><td>T13F</td><td>1.10</td></tr></table><div>Date: Wednesday, August 30, 2006Sheet 43 of 63</div></div>	Size	Project Name	Rev	Custom	T13F	1.10
Size	Project Name	Rev									
Custom	T13F	1.10									

3

6

3

A

<Variant Name>



**Title :** EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size  
Custom

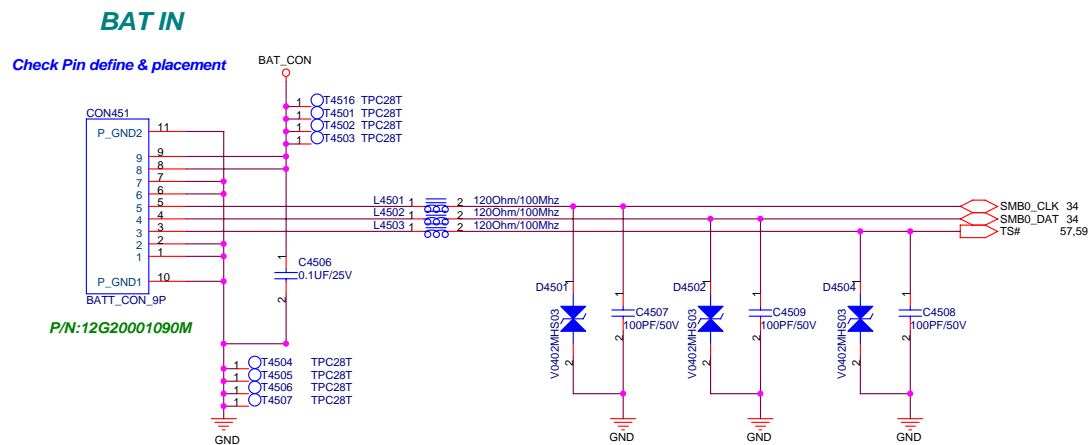
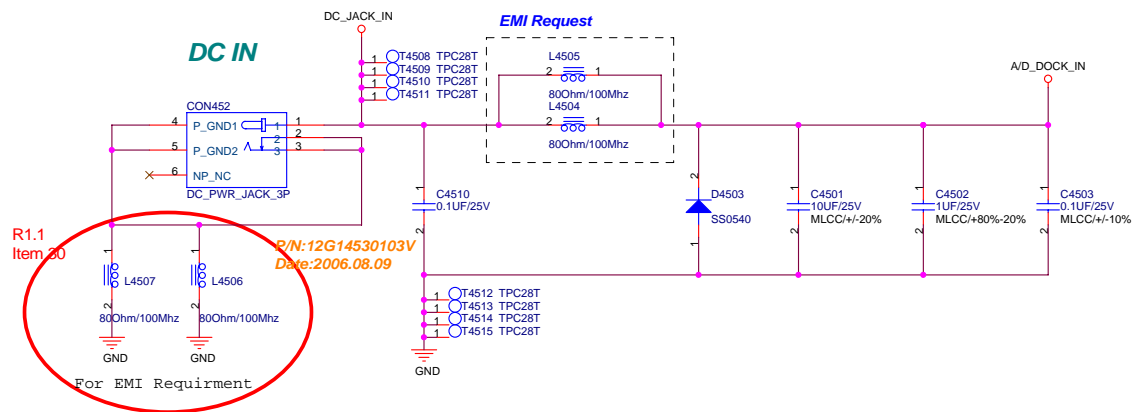
Project Name	<b>T13F</b>
--------------	-------------

Rev
1.10

Date: Wednesday, August 30, 2006

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<Variant Name>

		Title :BAT&Adapter conn	
ASUSTek COMPUTER INC		Engineer: <i>Marco Chen</i>	
Size Custom	Project Name <b>T13F</b>		Rev 1.10
Date: Wednesday, August 30, 2006			
		Sheet 45	of 63





R1.0 -> R1.1

- 1. Page 6: DNI R611 because Int. pull-up resister exists in FAN module.
- 2. Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.
- 3. Page 17: Change reference name from F3602 to F1701.
- 4. Page 21: DNI U2103.
- 5. Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.
- 6. Page 23: Change R2301 size from 0603 to 0402.
- 7. Page 23: Add pull high resister R2306\*DNI and pull down resister R2307\*Mount for ODD cable select.
- 8. Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.
- 9. Page 31: Delete R3133 and connect OP\_SD# to D3103.2 directly.
- 10. Page 32: Delete R3201 and connect MIC2\_VREFOUTto R3203.1 directly.
- 11. Page 34: DNI D604, R3411 and mount R3408, R3418 for thermal protection.
- 12. Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.
- 13. Page 35: Change keyboard matrix.
- 14. Page 36: Change reference name from JP3403 to JP3601
- 15. Page 36: Change R3622 size from 0402 to 0603.
- 16. Page 39: Delete R3920 and change Q3906 and Q3907\*2N7006 to Q3908\*UM6K1N.
- 17. Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.
- 18. Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.
- 19. Page 34: Add ESD Protection\*D3402 for Touch Pad.
- 20. Page 27: Add series resister 33 ohm for PCI\_FRAME# and PCI\_AD13
- 21. Page 34: Change Q3403\*\*UM6K1N to Q3404, Q3405\*2N7002.
- 22. Page 18: Change L1801, L1802, and L1803 from bead to inductor.
- 23. Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

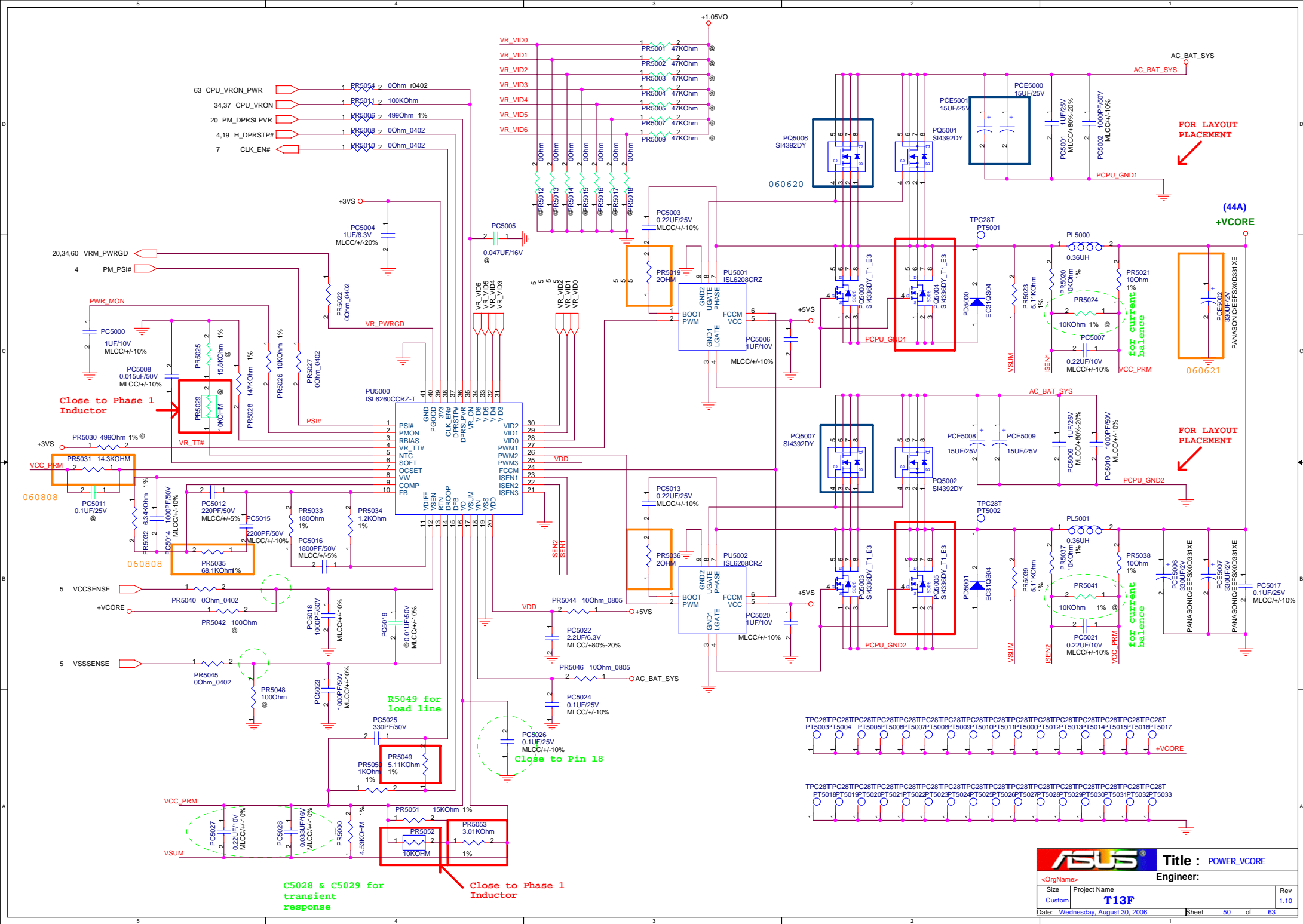
- 24. Page 6: Change R615 pull up from +3VS to +5VS\_AUDIO.
- 25. Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.
- 26. Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.
- 27. Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.
- 28. Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.
- 29. Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.
- 30. Page 45: Add L4506 and L4507 for EMI requirement.

# T13FG R11 for CardBus (Modify from T13F\_MBX\_R11\_0822)

- 1.R745, R750, R751, R763, R764 DNI for NEW card
- 2.DNI C2104, C2105
- 3.Mount D2501
- 4.Mount R2711, DNI R2712
- 5.Mount C3021
- 6.Change CE3101, CE3102 to C3123, C3124 from 100uF to 22uF
- 7.Mark page33 empty
- 8.Mount R3434, Q3501; DNI U3503
- 9.Keep CON361 and related schematic, DNI other schematic
- 10.DNI CON383
- 11.DNI Q3908

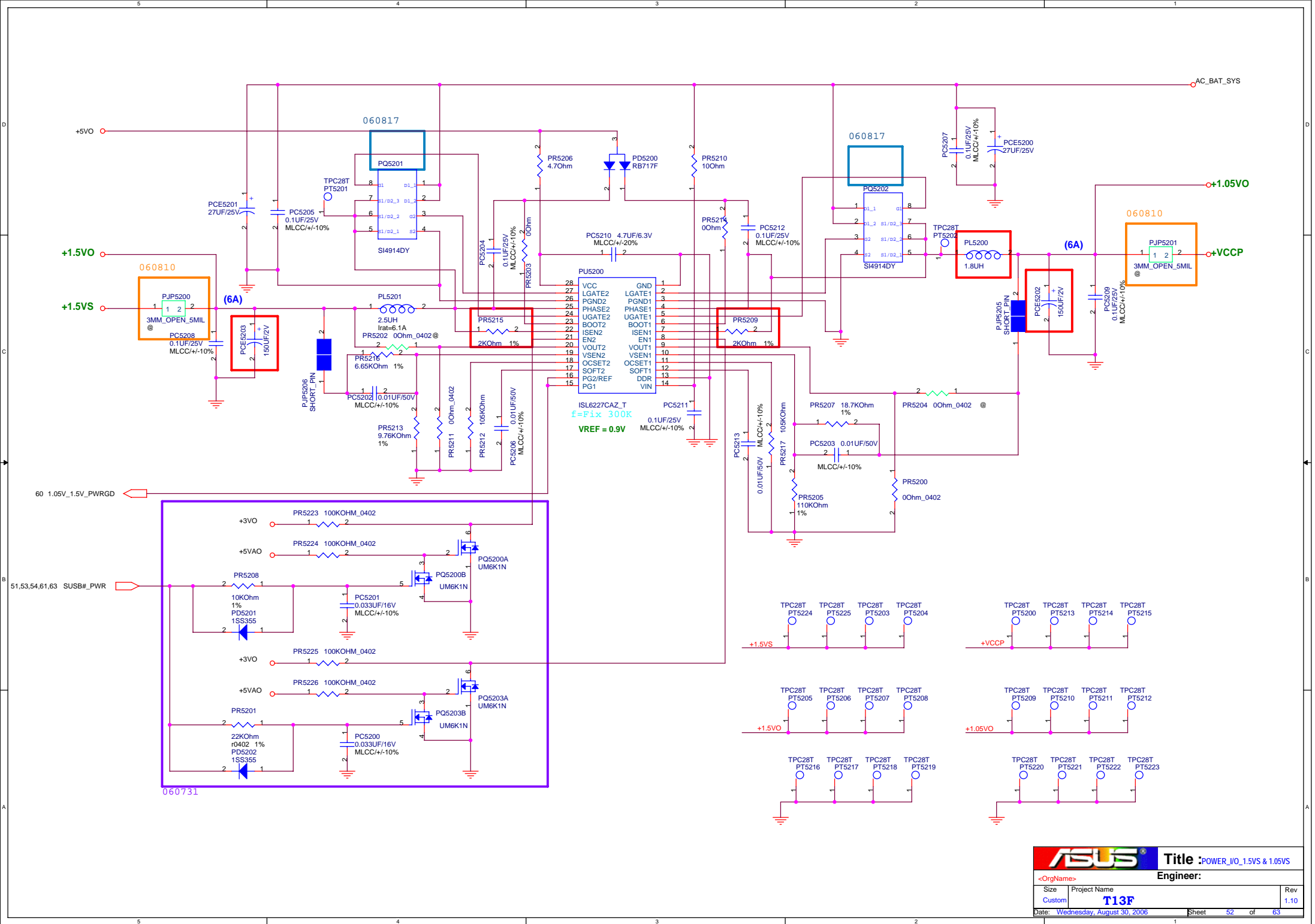
<Variant Name>

		Title : History(2)	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Wednesday, August 30, 2006		Sheet	49 of 63



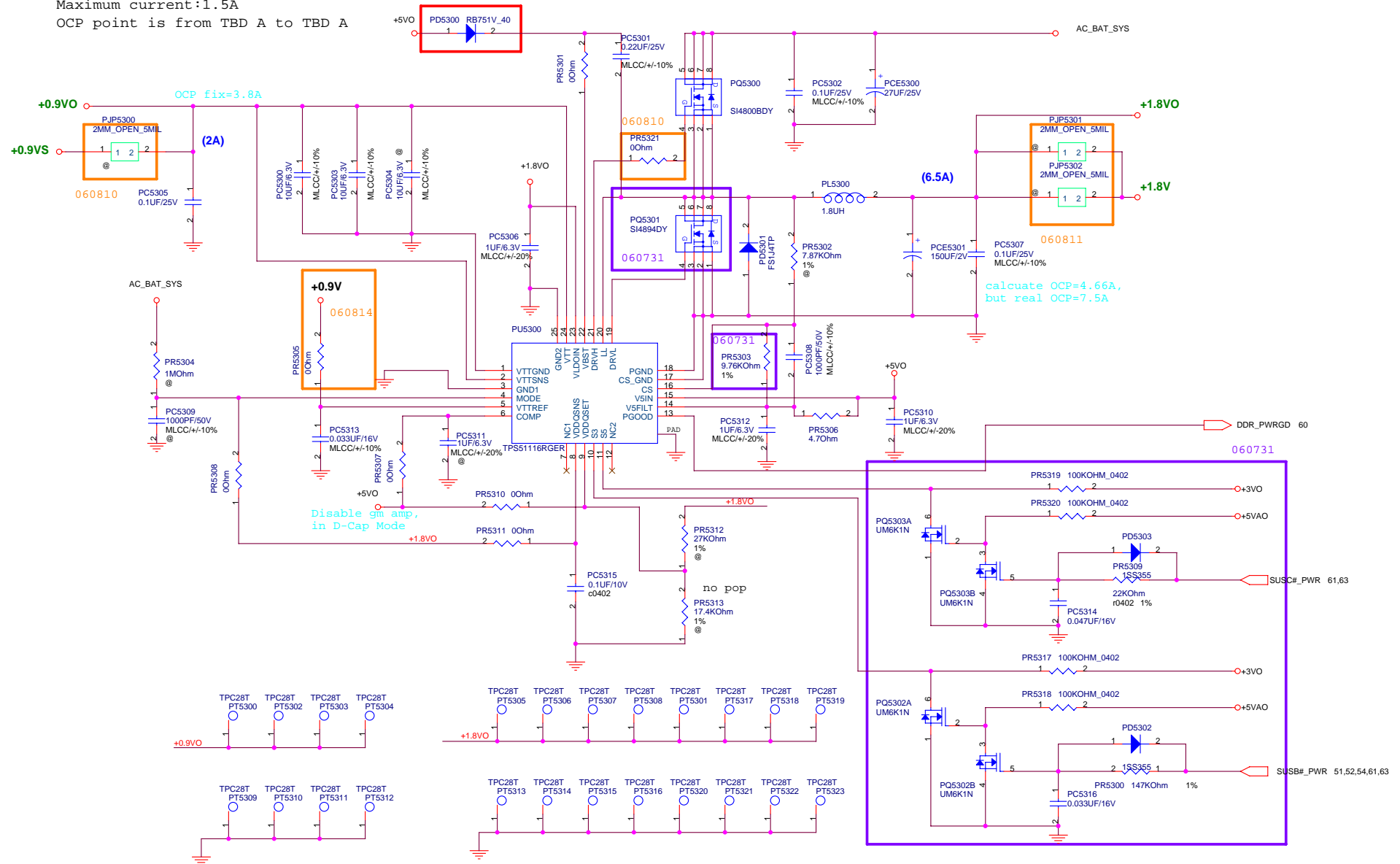









.9 Volt +/-5% .9 Volt +/-5%  
 Design Current:1.05A  
 Maximum current:1.5A  
 OCP point is from TBD A to TBD A

1.8Volt +/-5%  
 Design Current:7.3A  
 Maximum current:10.5A  
 OCP point is from TBD A to TBD A

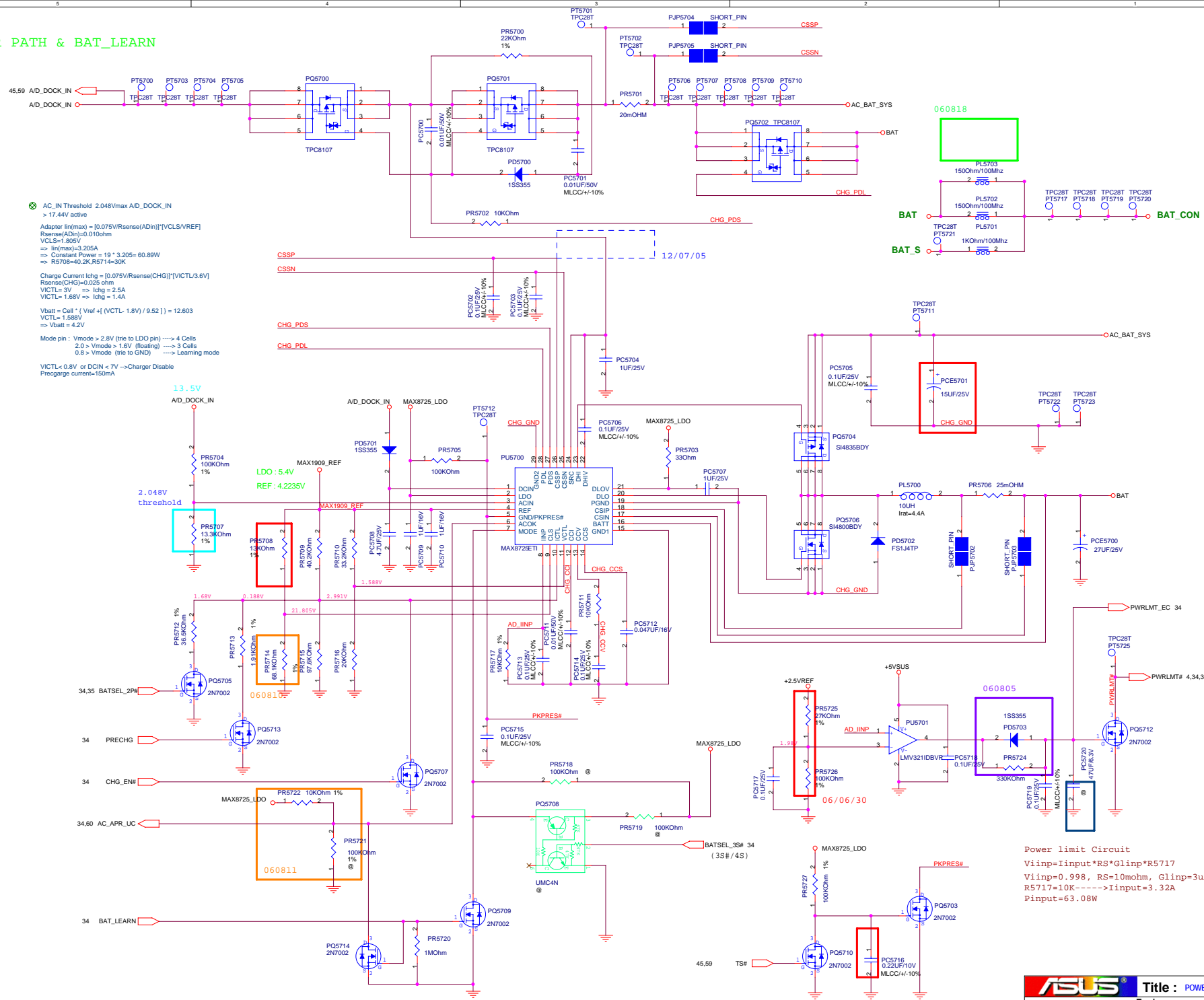




	5	4	3	2	1																				
D					D																				
C					C																				
B					B																				
A					A																				
					<table><tr><td colspan="2"></td><td colspan="2">Title :EMPTY</td></tr><tr><td colspan="2">&lt;OrgName&gt;</td><td colspan="2">Engineer:</td></tr><tr><td>Size</td><td colspan="2">Project Name</td><td>Rev</td></tr><tr><td>Custom</td><td colspan="2">T13F</td><td>1.10</td></tr><tr><td>Date: Wednesday, August 30, 2006</td><td>Sheet</td><td>55</td><td>of 63</td></tr></table>			Title :EMPTY		<OrgName>		Engineer:		Size	Project Name		Rev	Custom	T13F		1.10	Date: Wednesday, August 30, 2006	Sheet	55	of 63
		Title :EMPTY																							
<OrgName>		Engineer:																							
Size	Project Name		Rev																						
Custom	T13F		1.10																						
Date: Wednesday, August 30, 2006	Sheet	55	of 63																						
	5	4	3	2	1																				




## POWER PATH & BAT\_LEARN



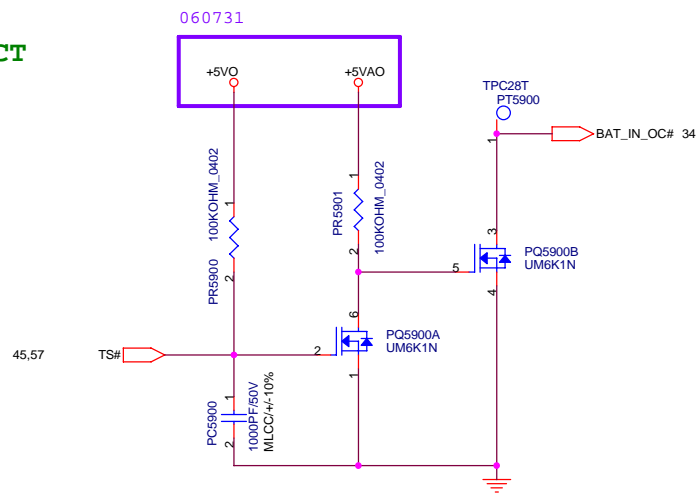
```
Power limit Circuit
Viinp=Iinput*RS*Glinp*R5717
Viinp=0.998, RS=10mohm, Glinp=3uA/mV,
R5717=10K----->Iinput=3.32A
Pinput=63.08W
```



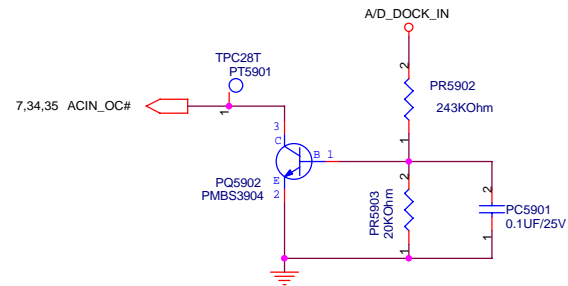
		<b>Title :</b> POWER_PIC	
<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>T13F</b>	1.10	
Date: Wednesday, August 30, 2006		Sheet	58 of 63



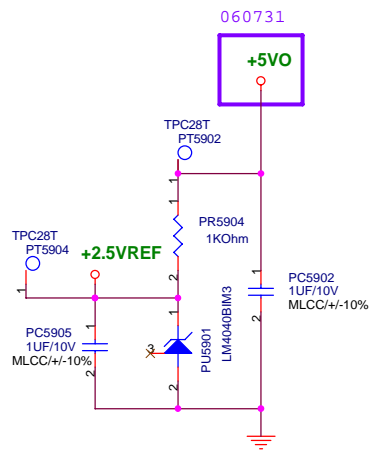
## BATTERY IN DETECT

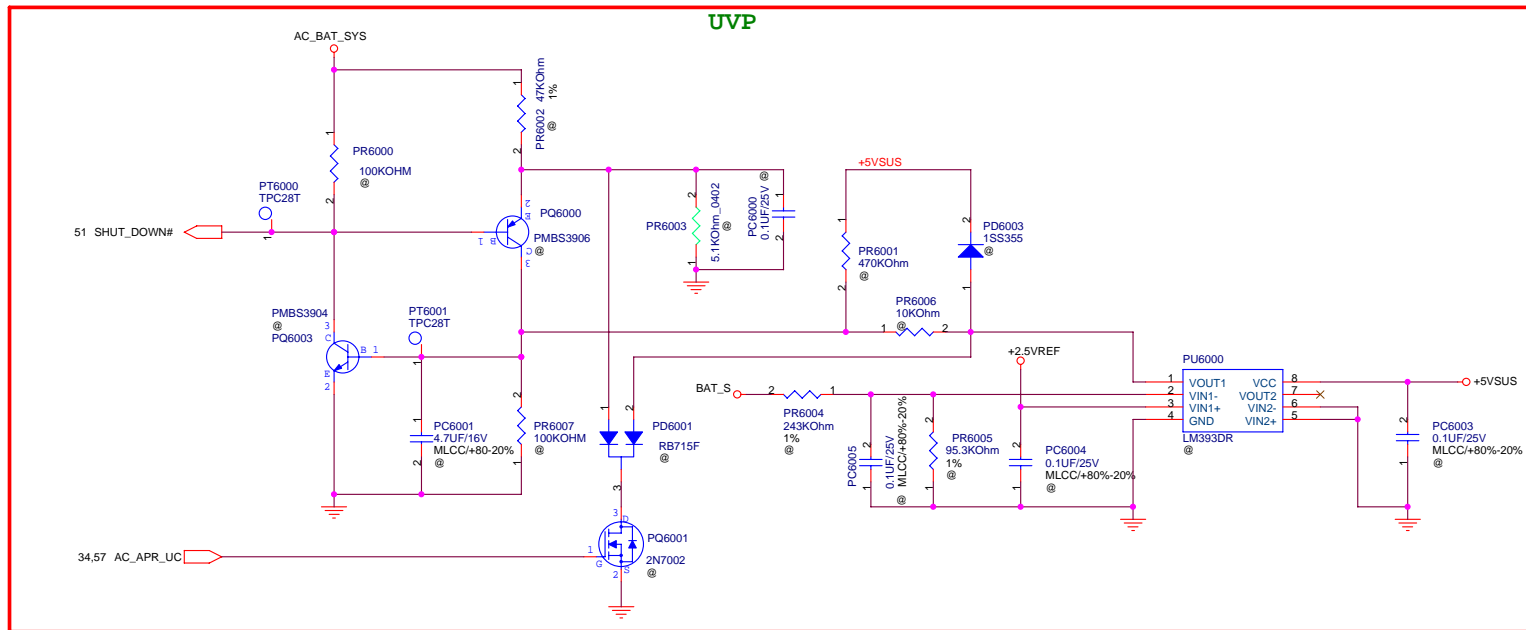


## ADAPTER IN DETECT

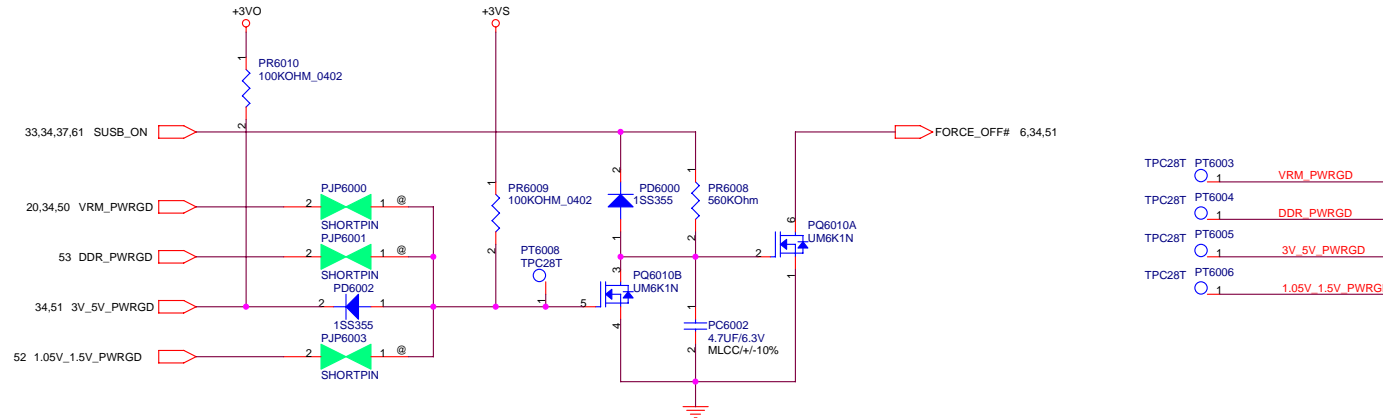


## +5VLCM, +5VCHG & +2.5VREF



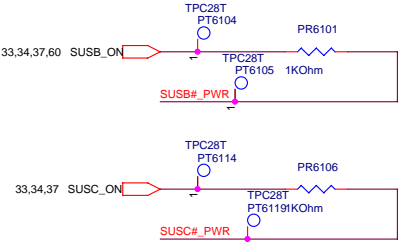
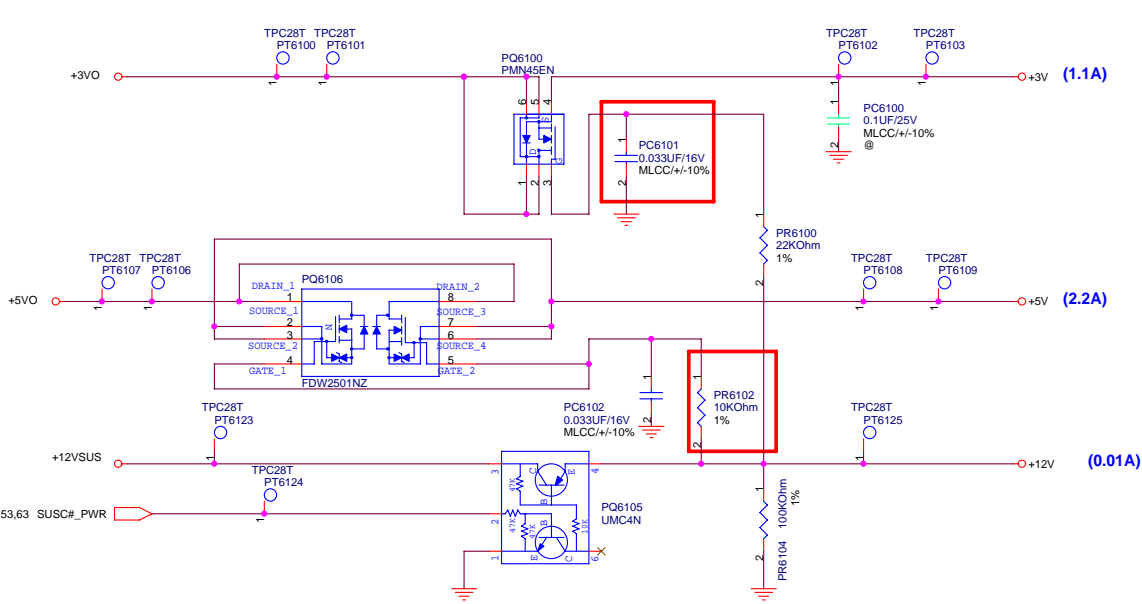


## POWER GOOD DETECTER

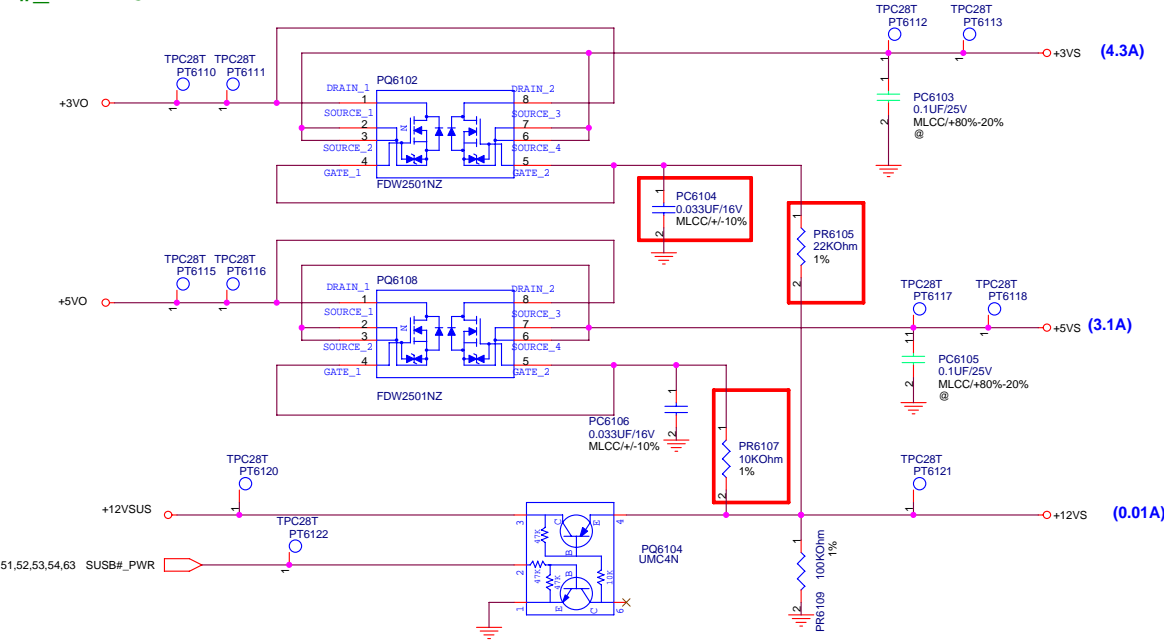


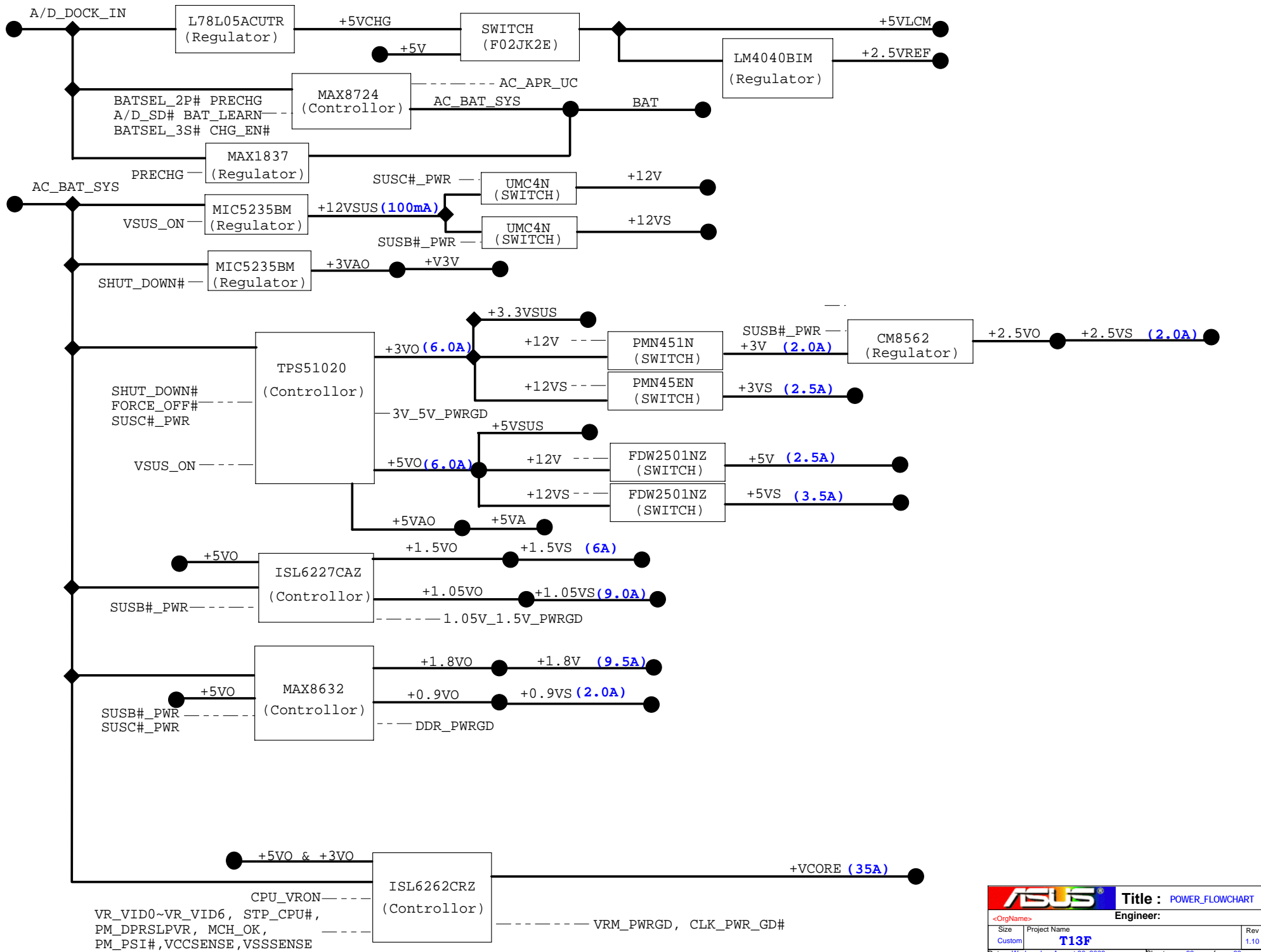
TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.5V_PWRGD

SUSC#\_PWR POWER



SUSB#\_PWR POWER







FOR POWER TEST

