

Bumblebee (LBB-2)

Cometlake-U Schematics

Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1

2020-03-03

Properties of DUMMY: (BOM Control Parts)

Value	Description
(No Value)	ASM, assemble
DY	DUMMY, NOT ASM, not assemble
ZZ (No Need to Display)	ZZ parts for testpoint / shortpad / hole
PCBID	PCB ID for SW Team (PCB number)
SKUID	SKU ID for SW Team (CPU Type: non-vPro / vPro)
MEM_IDx_0 / MEM_IDx_1 (x = 0~4)	Memory ID for SW Team (0 = Low / 1 = High Level)
DDR4_CTRL	Memory Packaging Technology setting (SDP / DDP)
SDP / DDP	Number of identical die in package (1 = SDP, 2 = DDP)
APS / ISH / LPC / XDP	Debug Connectors (Assemble in 1st build only)
EMC	Follow EMC Team requested
NON_PSL / PSL	Support / Non Support KBC Power Switched Logic
WLAN_PCIe / WLAN_CNVi	Support WLAN type (PCIe or CNVi interface)
CHARGER_HS / CHARGER_LS	Charger High / Low Side MOSFET
VCCSA_HS / VCCSA_LS	VCCSA High / Low Side MOSFET

LBB-2

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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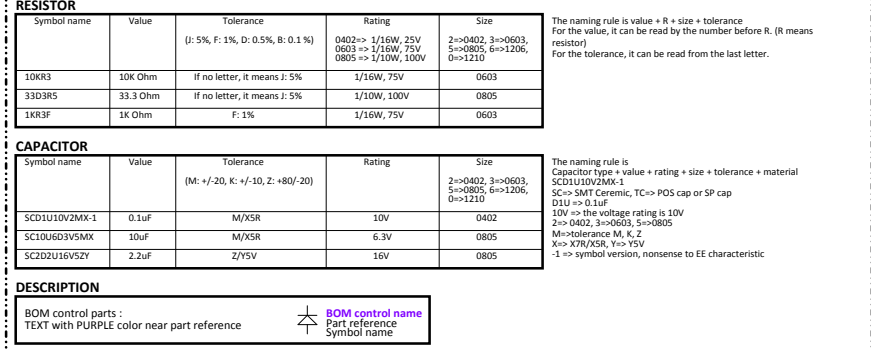
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Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1



PCB Layer Stackup		
L1:Component		
L2:GND		
L3:Signal 1		
L4:VCC		
L5:Signal 2		
L6:Signal 3		
L7:GND		
L8:Signal 4		
L9:GND		
L10:Component		
Battery Charger/Selector		
BQ25700ARSNR		44
VINT20_IN	19V_DCRATOUT BT+	
System DC/DC		
TPS51285B		45
19V_DCRATOUT	5V_S5 3D3V_S5	
DC/DC IMVP8		
NCP81218PMNTXG		46
DC/DC VCCPCPU/CORE		
NCP302045LMNTXG		47
19V_DCRATOUT	1V_CPU_CORE	
DC/DC VCCGT		
NCP302045LMNTXG		48
19V_DCRATOUT	1V_YCCGT	
DC/DC VCCSA		
NCP81253MNTBG		50
19V_DCRATOUT	1V_VCCSA	
DC/DC 1D2V_S3		
NB687GQ-C669-Z		51
19V_DCRATOUT	1D2V_S3	
DC/DC 0D6V_VREF_S0		
NB687GQ-C669-Z		51
1D2V_S3	0D6V_VREF_S0	
DC/DC 2D5V_S3		
NB687GQ-C669-Z		51
3D3V_S5	2D5V_S3	
DC/DC 1D05V_SUS		
RT8237CZQW		52
19V_DCRATOUT	1D05V_SUS	
DC/DC 1D8V_SUS		
RT5797ALGQW		53
3D3V_S5	1D8V_SUS	

Main Func = CPU

24 PECO_CPU
24,44,46 PROCHOT#_CPU

```
71 -TBT_PLUG_EVENT >>_____
```

```
61  BLUETOOTH_EN_CPU <<—
```

```

99  PROC_TCK      >>=====
99  PROC_TDI      >>=====

```

```
99 PROC_TDI //
100 PROC_TMC \>
```

```

99  PROC_TMS
99  PROC_TRST#

```

99 PCH ITAG TCK >>

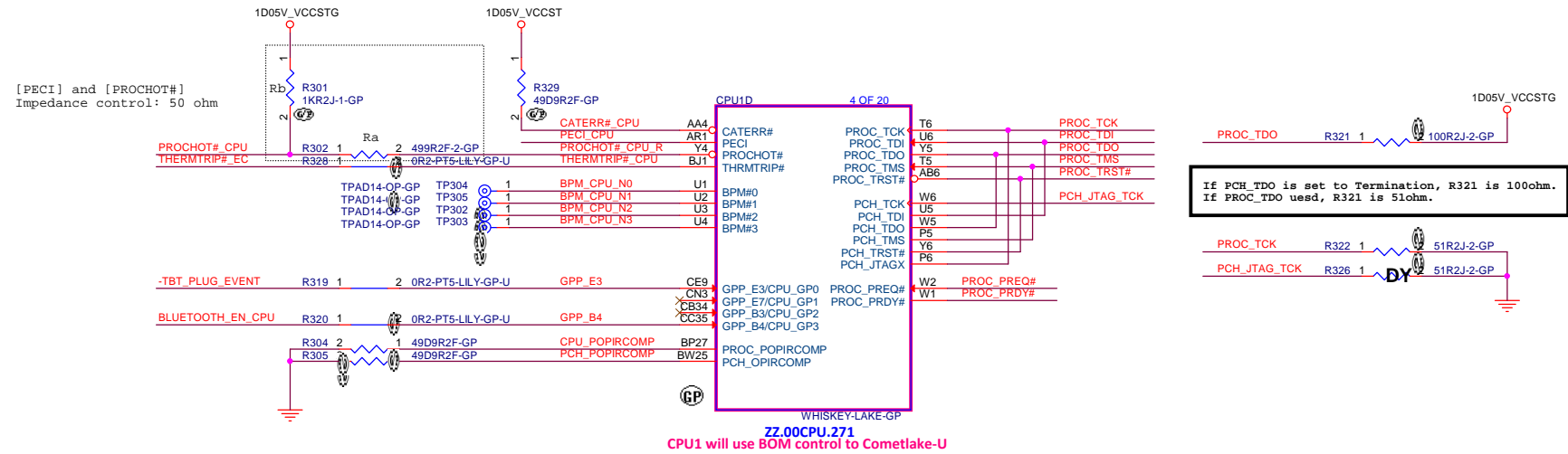
```
99      PROC: TDO      //
```

35 1855-1856 11

99 PROC_PREQ# >>—————

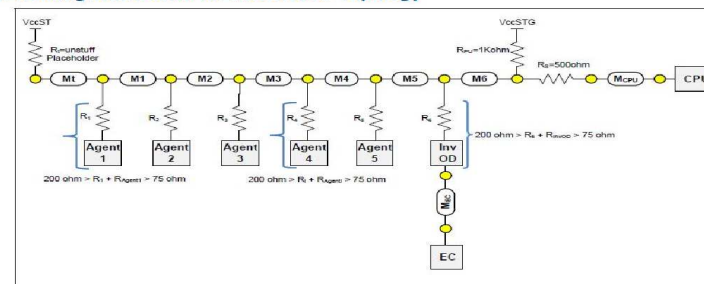
99 PROC_PRDY# <<_____

40 THERMTRIP#_EC <<—



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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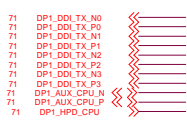
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Title	CPU (THML/JTAG)
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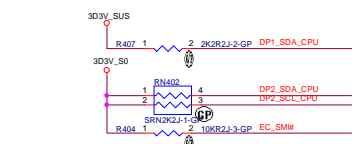
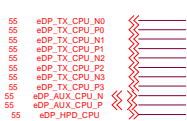
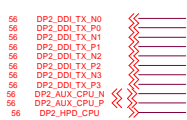
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DOCK

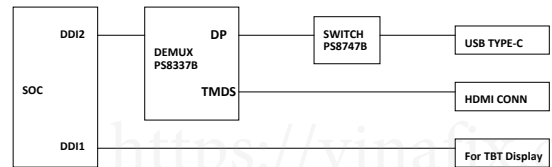


USBC

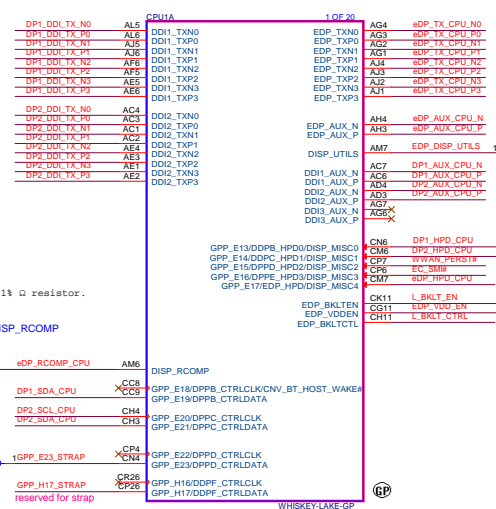
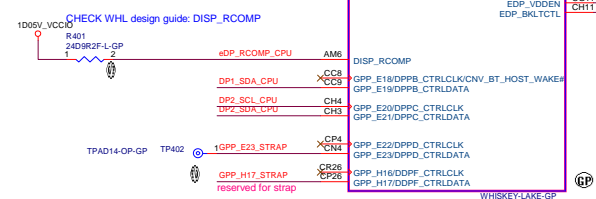


Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

TABLE: Functional Strap	
DDPB_CTRLDATA HIGH	Port B is detected.
DDPB_CTRLDATA LOW	Port B is not detected.
DDPC_CTRLDATA HIGH	Port C is detected.
DDPC_CTRLDATA LOW	Port C is not detected.

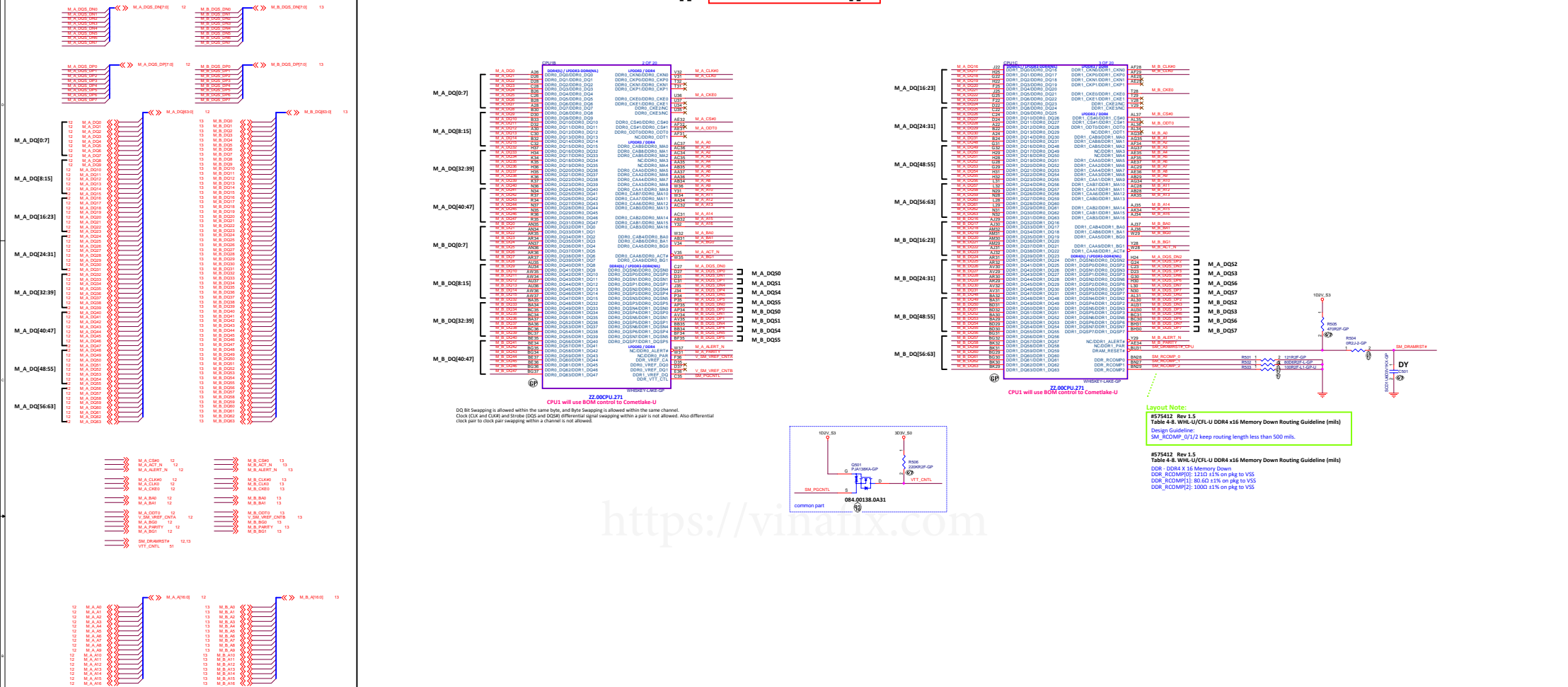


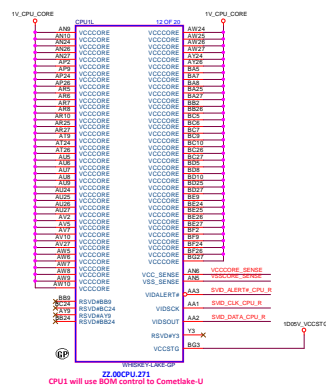
Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Q resistor.



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```
DDR4 ball type: Non-Interleaved Type
```





Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (+0.1 inch).
Route the Alert signal between the Clock and the Data signals.

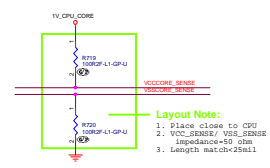
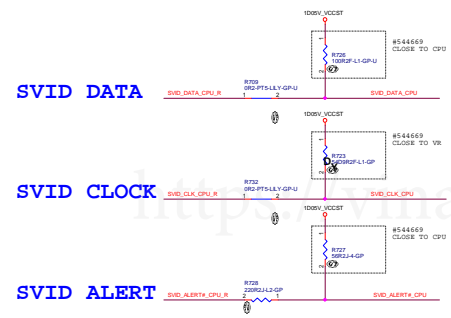


Figure 10-7. Routing Illustration for SVID Topology

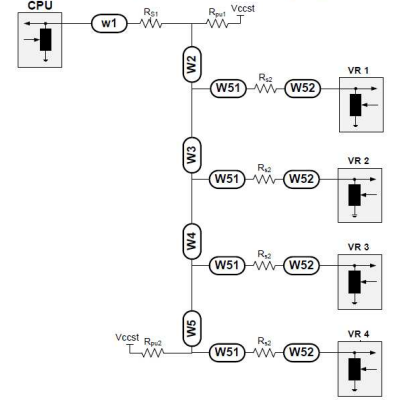
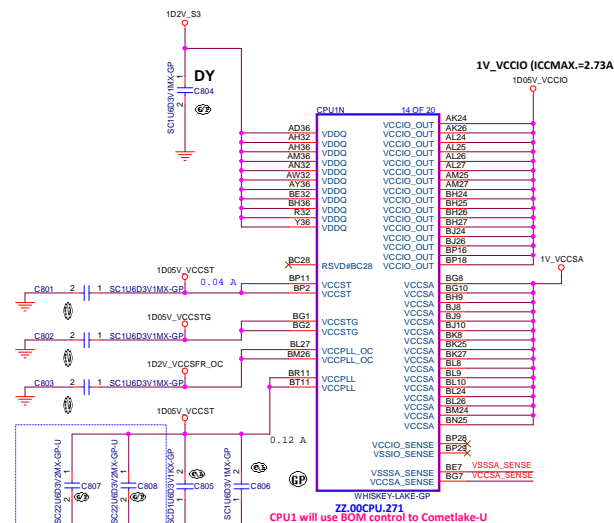


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W01 [inches]	W02 [inches]	R _{DS(on)} [mΩ]	R _{DS(on)} [mΩ]	R _{DS(on)} [mΩ]	R _{DS(on)} [mΩ]	V _{CCP} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT #							56	Empty	Y	220	0

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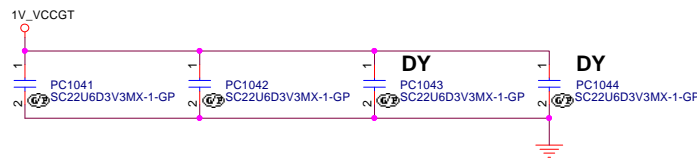
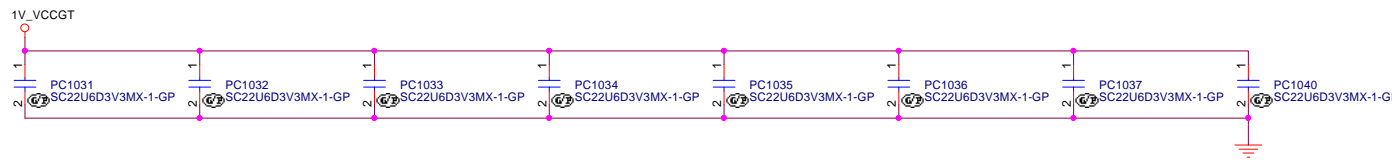
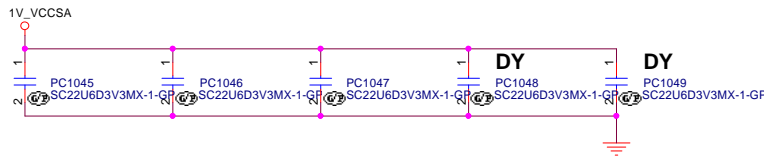
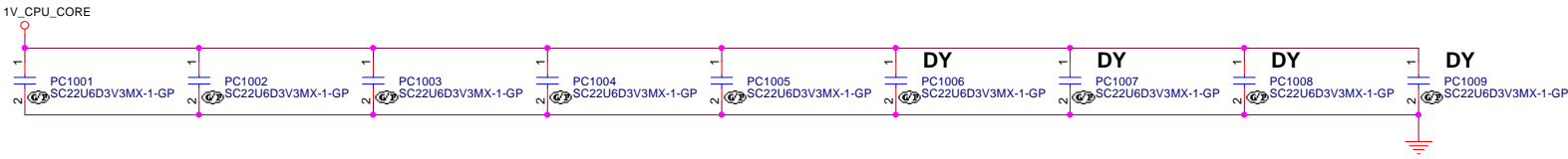
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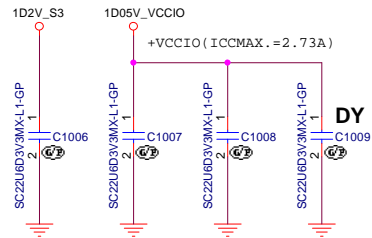
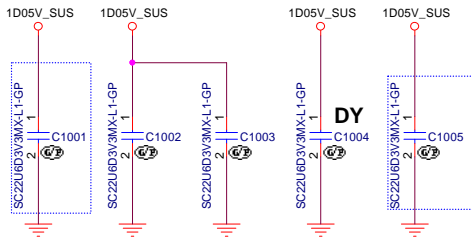
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Title CPU (RSVD)		
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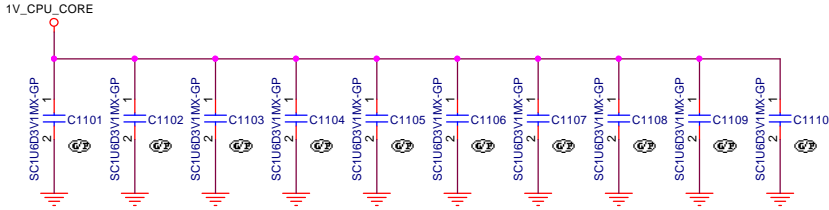
Main Func = CPU



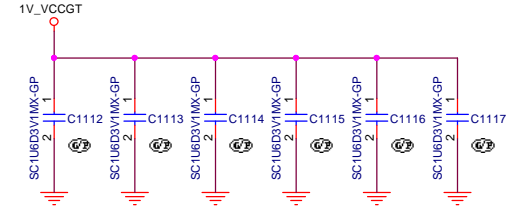
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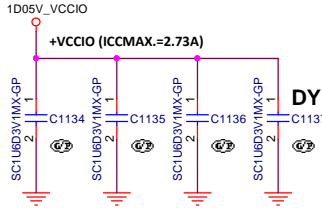
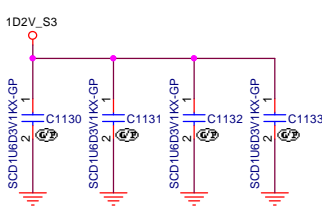
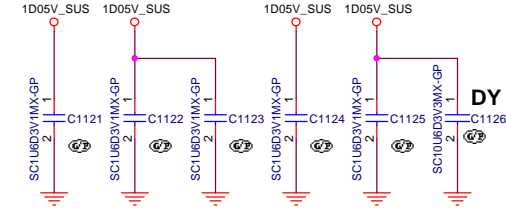
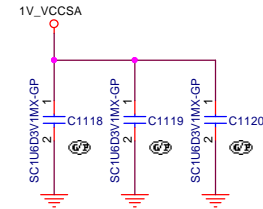
VCORE



VCCGT



VCCSA



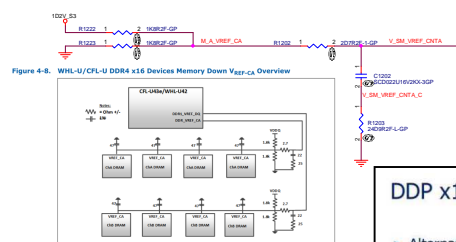
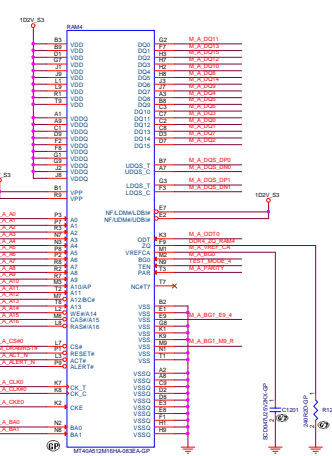
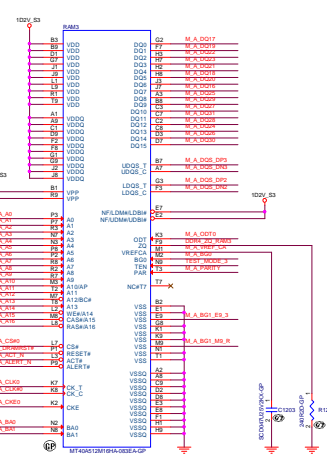
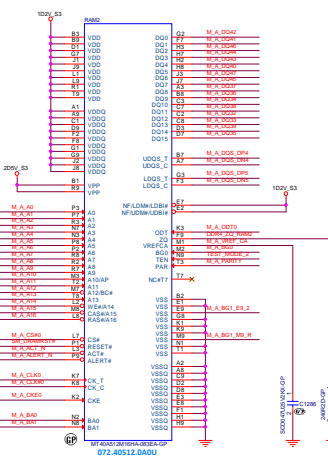
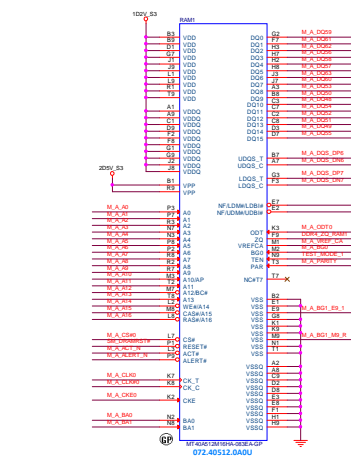


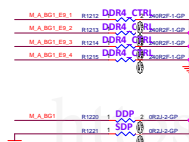
Figure 4-8. WHL-U/CFL-U DDR4 x16 Devices Memory Down V_{REF_CA} Overview

SDP & DDP SETTING

R1212~R1215:
DDR: 340 psm (64 34005 601)

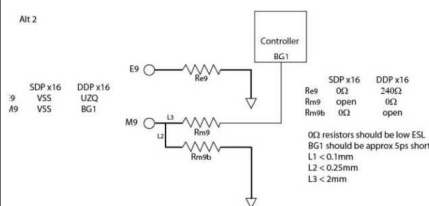
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

MABG1_E2.1 R1212 DDR



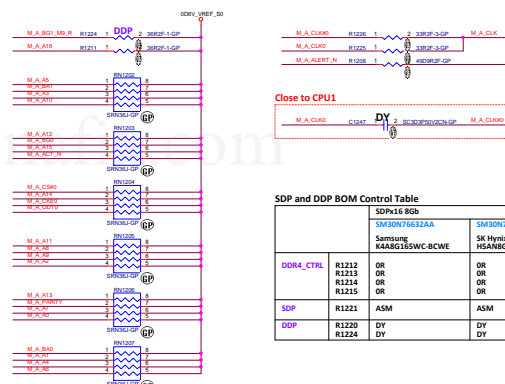
DDP x16 and SDP x16 Compatible Layout

- ▶ Alternate two layout, risk of VSS offset increases a little

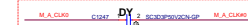


OC2 resistors should be low ESL
BG1 should be approx 5ps short
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

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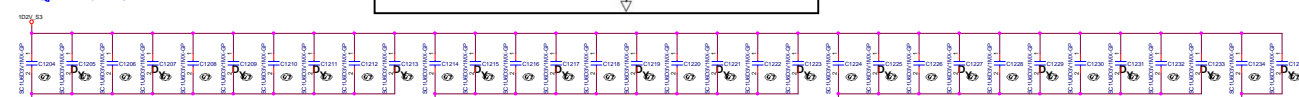
Close to CPU1



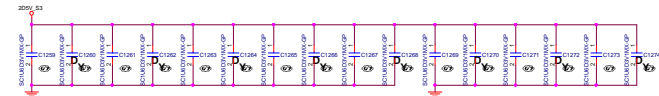
SDP and DDP BOM Control Table

[illegible]

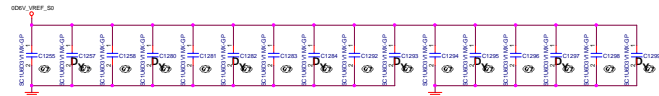
VDDQ/VDD 1uF x16



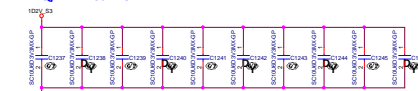
VPP 1uF x8



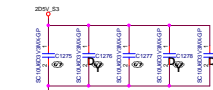
VTT 1uF x8



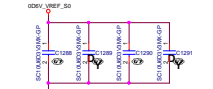
VDDQ/VDD 10uF x5

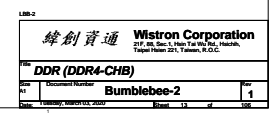


VPP 10uF x2



VTT 10uF x2





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Title
DDR (RSVD)

Size
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Document Number

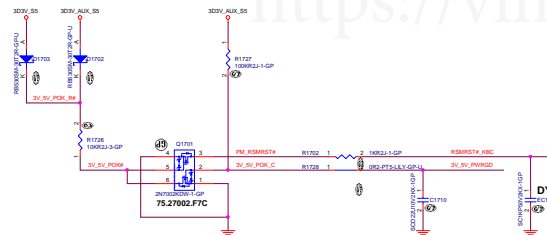
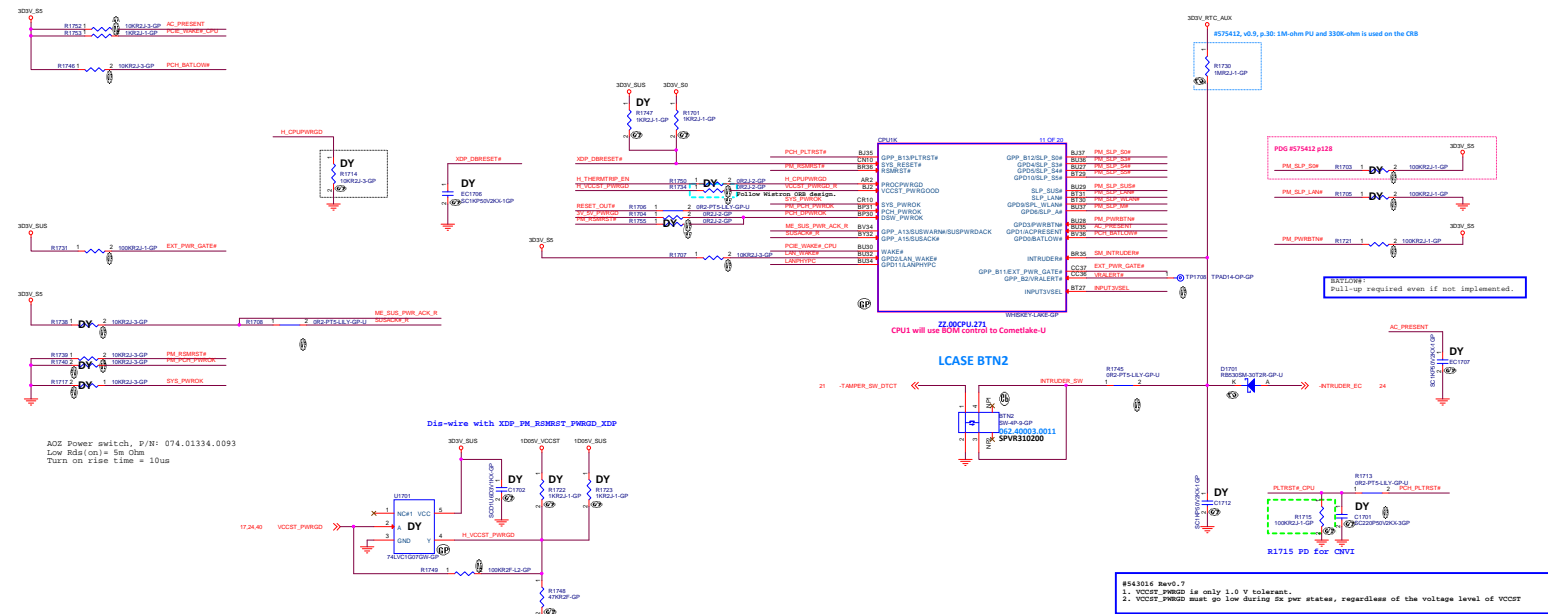
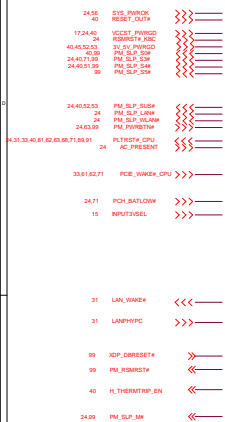
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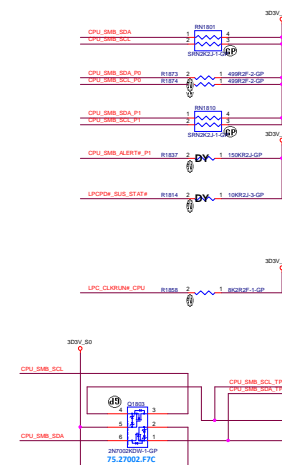
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<p>HW Strap</p>			<p>The signal has a weak internal pull-down.</p> <p>0 = Disable "No Reboot" mode. (Default)</p> <p>1 = Enable "No Reboot" mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PCH_PWROK is high. This signal is in the primary well.
<p>GPP_B14 / SPKR</p> <p>The Speaker</p> <p>Rising edge of PCH_PWROK</p>			<p>GPP_B18 / GSPID_MOSI</p> <p>No Reboot</p> <p>Rising edge of PCH_PWROK</p>
<p>GPP_C2 / SMDALERT#</p> <p>TLS Confidentiality</p> <p>Rising edge of RSMRST#</p>			<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.
<p>GPP_B14</p>			<p>GPP_B22</p>
<p>GPP_C5 / SMDALERT#</p> <p>eSPT or LPC</p> <p>Rising edge of RSMRST#</p>			<p>GPP_D12 / ISH_SPL_MOSI / GSPID_MOSI</p> <p>Reserved</p> <p>Rising edge of RSMRST#</p>
<p>GPP_C5</p>			<p>GPP_D12</p>
<p>SPID_MOSI</p> <p>Reserved</p> <p>Rising edge of RSMRST#</p>			<p>GPP_B23 / SMDALERT# / PCHHOT#</p> <p>Intel® DCI-OOB</p> <p>Rising edge of RSMRST#</p>
<p>SPID_MOSI</p>			<p>GPP_B23</p>
<p>SPID_102</p> <p>Reserved</p> <p>Rising edge of RSMRST#</p>			<p>HDA_SDO / I2SD0_TXD</p> <p>Flash Descriptor Security Override</p> <p>Rising edge of PCH_PWROK</p>
<p>SPID_102</p>			<p>GPP_E19 / DDPG_CTRLDATA / CNV_BT_IF_SELECT</p> <p>Display Port B Detected</p> <p>Rising edge of PCH_PWROK</p>
<p>SPID_103</p> <p>Reserved</p> <p>Rising edge of RSMRST#</p>			<p>GPP_H21</p> <p>XTAL Frequency Select</p> <p>Rising edge of RSMRST#</p>
<p>SPID_103</p>			<p>GPP_H21</p>
<p>GPP_E31 / DDPG_CTRLDATA</p> <p>Display Port C Detected</p> <p>Rising edge of PCH_PWROK</p>			<p>GPP_H23</p> <p>eSPT Flash Sharing Mode</p> <p>Rising edge of RSMRST#</p>
<p>GPP_E31</p>			<p>GPP_H23</p>
<p>GPP_F6 / CNV_RGL_DT</p> <p>M.2 CNV Mode Select</p> <p>Rising edge of RSMRST#</p>			<p>GPP_F6 / CNV_RGL_DT / UART0_TXD</p>
<p>GPP_F6</p>			<p>GPP_F6</p>
<p>INPUT3VSEL</p> <p>3.0V Select</p> <p>Input pin must always be driven to a valid logic level</p> <p>External pull-up or pull-down is required</p> <p>0 = 3.3V supply is 3.3V +/- 5%</p> <p>1 = 3.3V supply is 3.0V +/- 5%</p> <p>Note: This strap should only be used for specific targeted 1S battery systems.</p>			<p>GPD7</p> <p>Reserved</p> <p>Rising edge of DSW_PWROK</p>
<p>INPUT3VSEL</p>			<p>GPD7</p>
<p>GPP_F6 / CNV_RGL_DT / UART0_TXD</p>			<p>GPP_H23</p>
<p>GPP_F6</p>			<p>GPP_H23</p>





Main Func = PCH

.27 HDA_SDIN0_CPU >>>
27 HDA_SYNC_CODEEC >>>
27 HDA_BITCLK_CODEEC >>>
27 HDA_SDOOUT_CPU >>>
15 HDA_SDOOUT_CPU >>>
25 RTC_TEST >>>

24 ME_FWP_EC <<<

61 CLKREQ0_CNV1 >>>
61 RF_RESET_B_CNV1 >>>

15,27 HDA_SPKR <<<

66 DMIC_SCL_CPU <<<
66 DMIC_SDA_CPU <<<

71 TBT_RTD3_PWR_EN <<<
71 TBT_FORCE_USB_PWR <<<
71 -TBT_PERST <<<
71 -TBT_PCIE_WAKE >>>

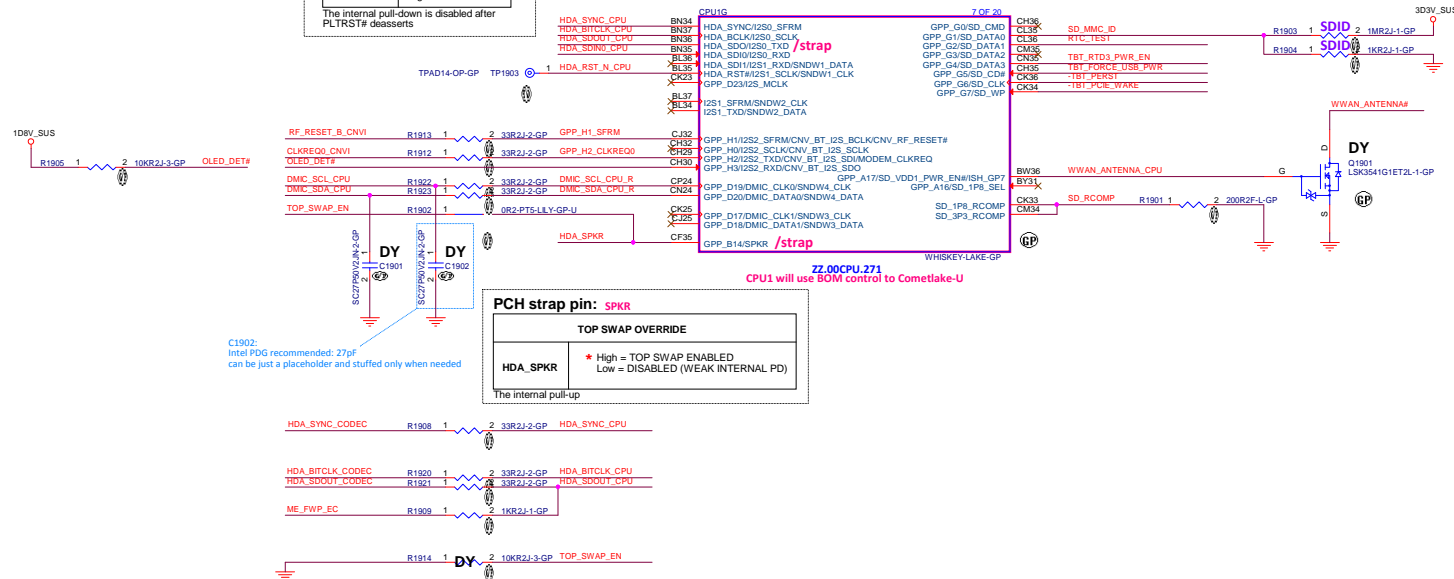
24 TOP_SWAP_EN >>>
62 WWAN_ANTENNA# >>>
55 OLED_DET# >>>

PCH strap pin: HDA_SDOOUT_CPU

Flash Descriptor Security Override/
Intel ME Debug Mode

HDA_SDOOUT Low = Default *
High = Enable

The internal pull-down is disabled after
PLTRST# deasserts



PCH strap pin: SPKR

TOP SWAP OVERRIDE

* High = TOP SWAP ENABLED
Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

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LBB-2

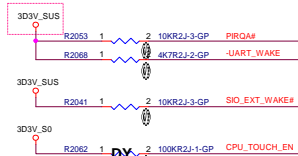
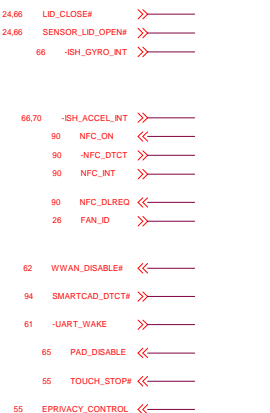
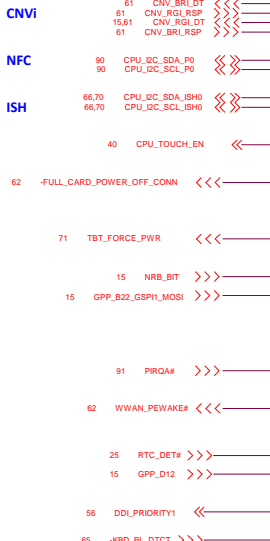
緯創資通 Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshui,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU_(HDA/I2S/SD/DMIC)

Size A2 Document Number Bumblebee-2 Rev 1

Date: Tuesday, March 03, 2020 Sheet 19 of 106

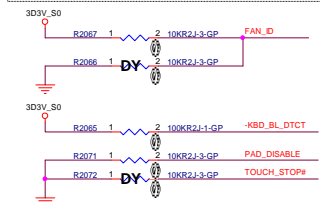
Main Func = PCH



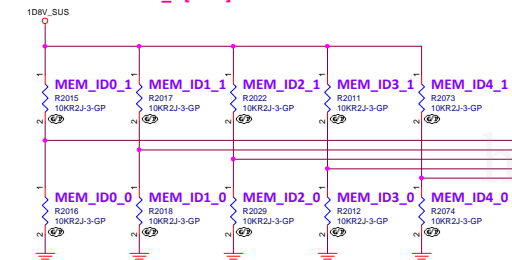
PCH strap pin: NRB_B

No Reboot	Sampled at rising edge of PCH_PWROK
GSP0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable timer system reboot feature). This function is only valid when running ITP/XDP.

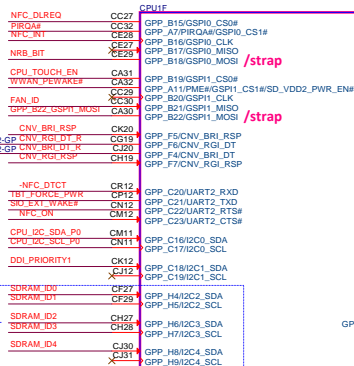
The signal has a weak internal pull-down.



Bumblebee: GPP_H[0:23] is 1.8V.

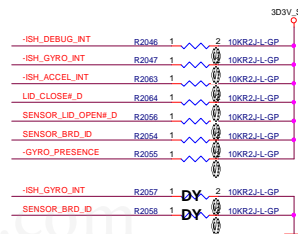


Memory Configuration		Memory Supplier		Die Revision					
00: 8Gb 01: 4Gb (Reserve) 10: 16Gb 11: 32Gb (Reserve)		00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)							
GPP_H8	GPP_H7	GPP_H6	GPP_H5	GPP_H4					
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Density	Vendor PN	
0	0	0	0	0	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCWE	
1	1	1	1	1	1	SAMSUNG	16GB (16Gb*8)	K4AAG165WA-BCWE	
2	2	2	2	2	2	MICRON	8GB (8Gb*8)	MT40AS12M16T-062E-J	
3	3	3	3	3	3	MICRON	16GB (16Gb*8)	MT40A1G16KD-062E-E	
4	4	4	4	4	4	SK HYNIX	8GB (8Gb*8)	HSAN8G6NCJR-XNC	
5	5	5	5	5	5	SK HYNIX	16GB (16Gb*8)	HSANAG6NCMR-XNC	
6	6	6	6	6	6				
7	7	7	7	7	7				
8	8	8	8	8	8				
9	9	9	9	9	9				
10	10	10	10	10	10				
11	11	11	11	11	11				
12	12	12	12	12	12				
13	13	13	13	13	13				
14	14	14	14	14	14				
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187	187	187	187	187	187				
188									



Bumblebee: GPP_H[0:23] is 1.8V.

ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

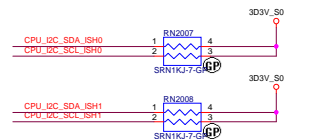
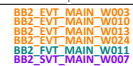
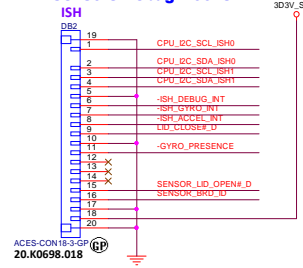


Sensors Debug Hooks_543016:

Table 31-3. 18-pin ZIF Connector Pinout

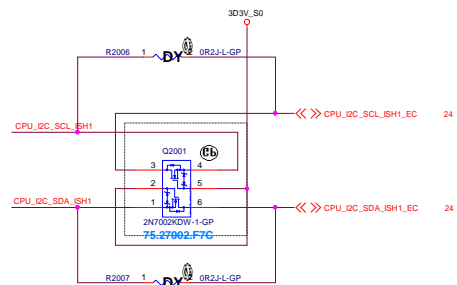
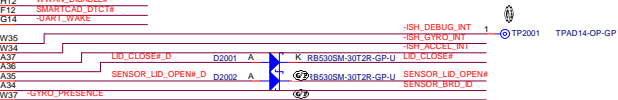
Pin	Pin Function	Description
1	SH_LD3C_SQ1	Clock line for the D20
2	SH_LD3C_SQ4	Data line for the D20
3	SH_LD3C_SQ5	Clock line for the D21
4	SH_LD3C_SQ4	Data line for the D21
5	GND	System Ground
6	GPIOC ⁽¹⁾	Connect here one of the GPIOs in use
7	GPIOC ⁽¹⁾	Connect here one of the GPIOs in use
8	GPIOC ⁽¹⁾	Connect here one of the GPIOs in use
9	GPIOC ⁽¹⁾	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	VIO	Sensors Reference Voltage

Sensors Debug Hooks



Bumblebee: GPP_H[0:23] is 1.8V.

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.



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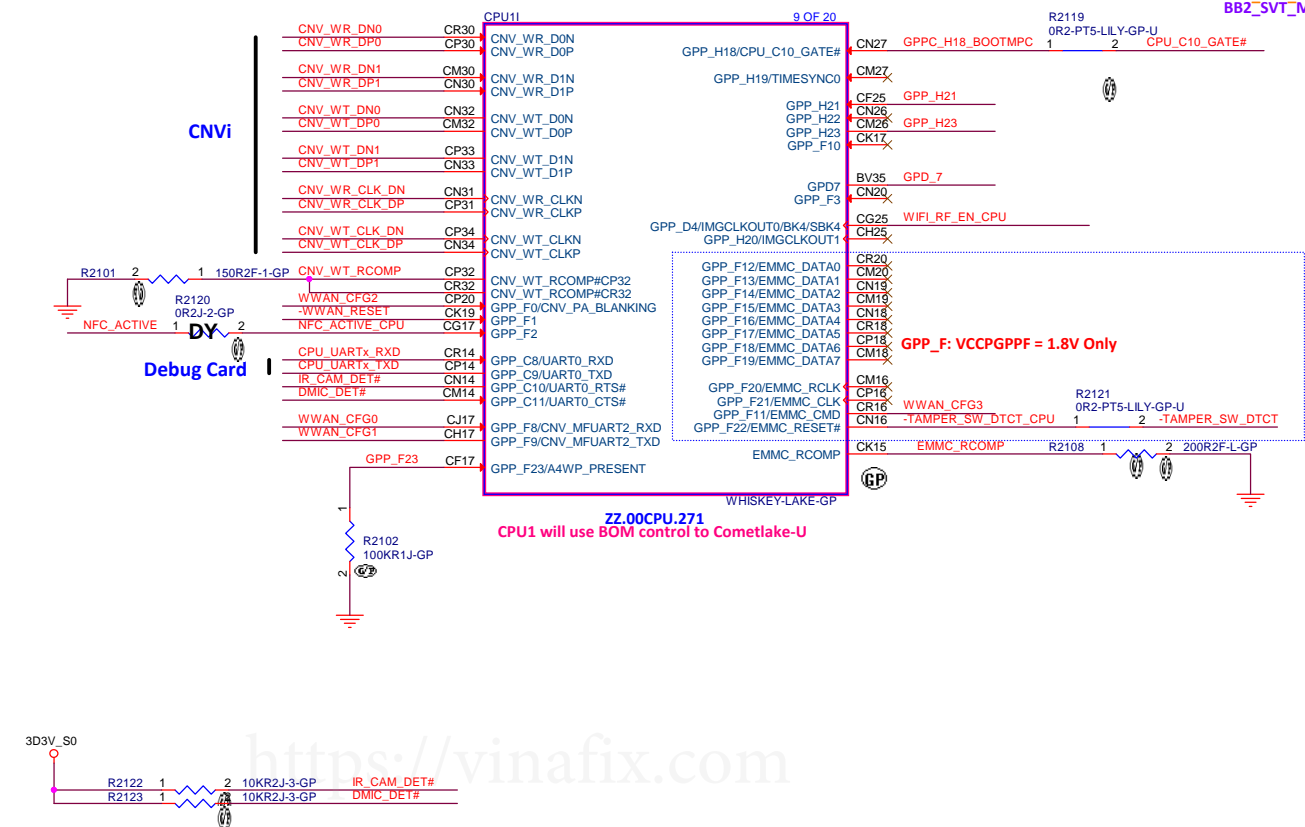
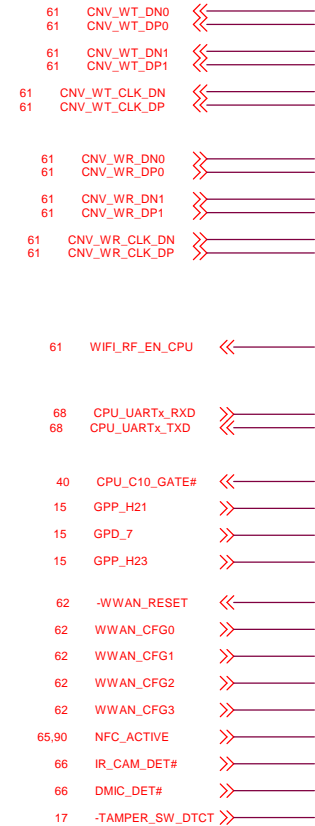
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(UART/I2C/ISH)
-------	---------------------------

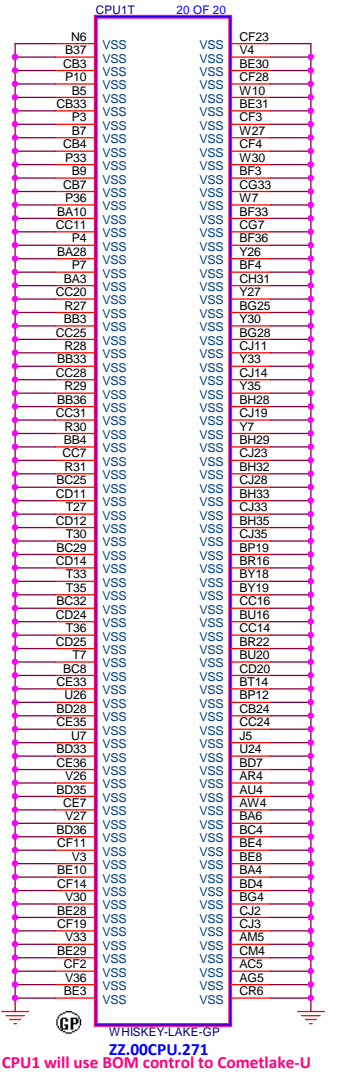
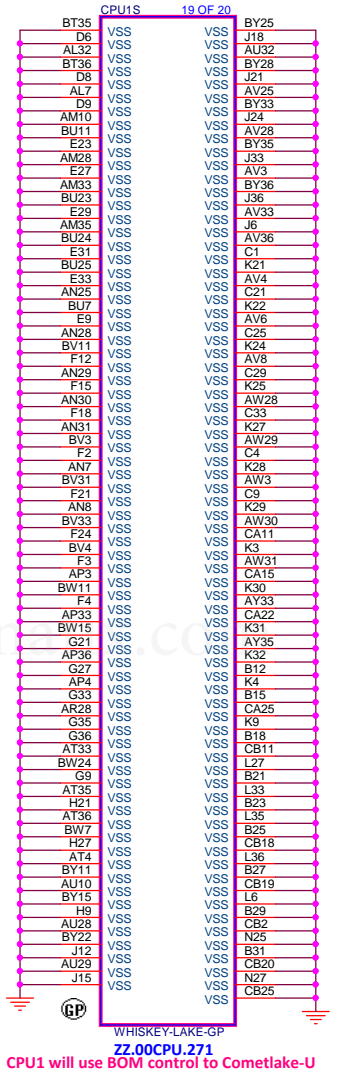
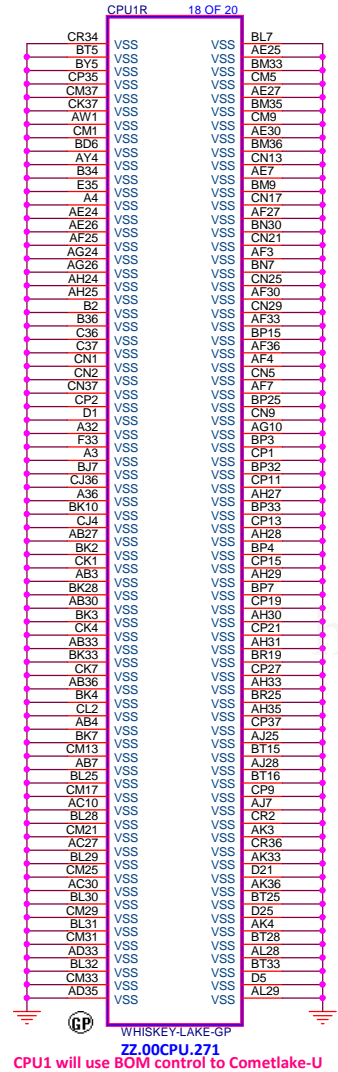
Size A2	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 20 of	106

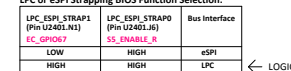
Main Func = PCH

CNVi



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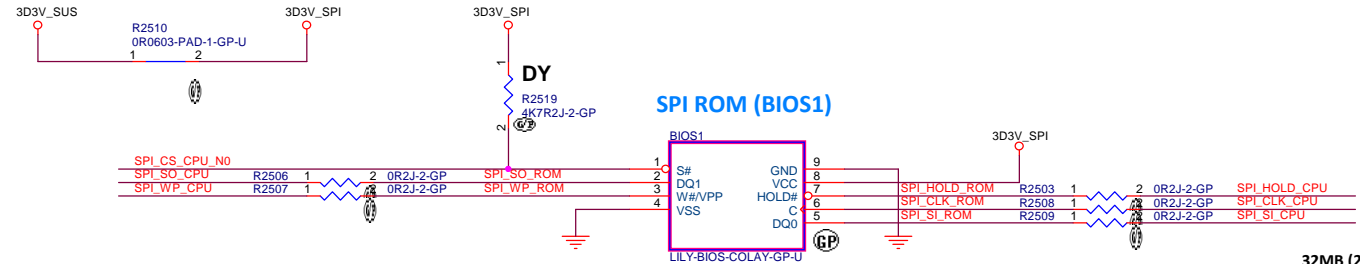




Main Func = SPI Flash

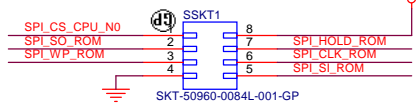
BB2_SVT_MAIN_W003

18,24 SPI_CS_CPU_N0
18,24,91 SPI_CLK_CPU
15,18,24,91 SPI_SI_CPU
18,24,91 SPI_SO_CPU
15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU



BIOS1 will use BOM control by co-lay symbol issue (WINBOND had load code issue)

SPI ROM Socket (SSKT1)

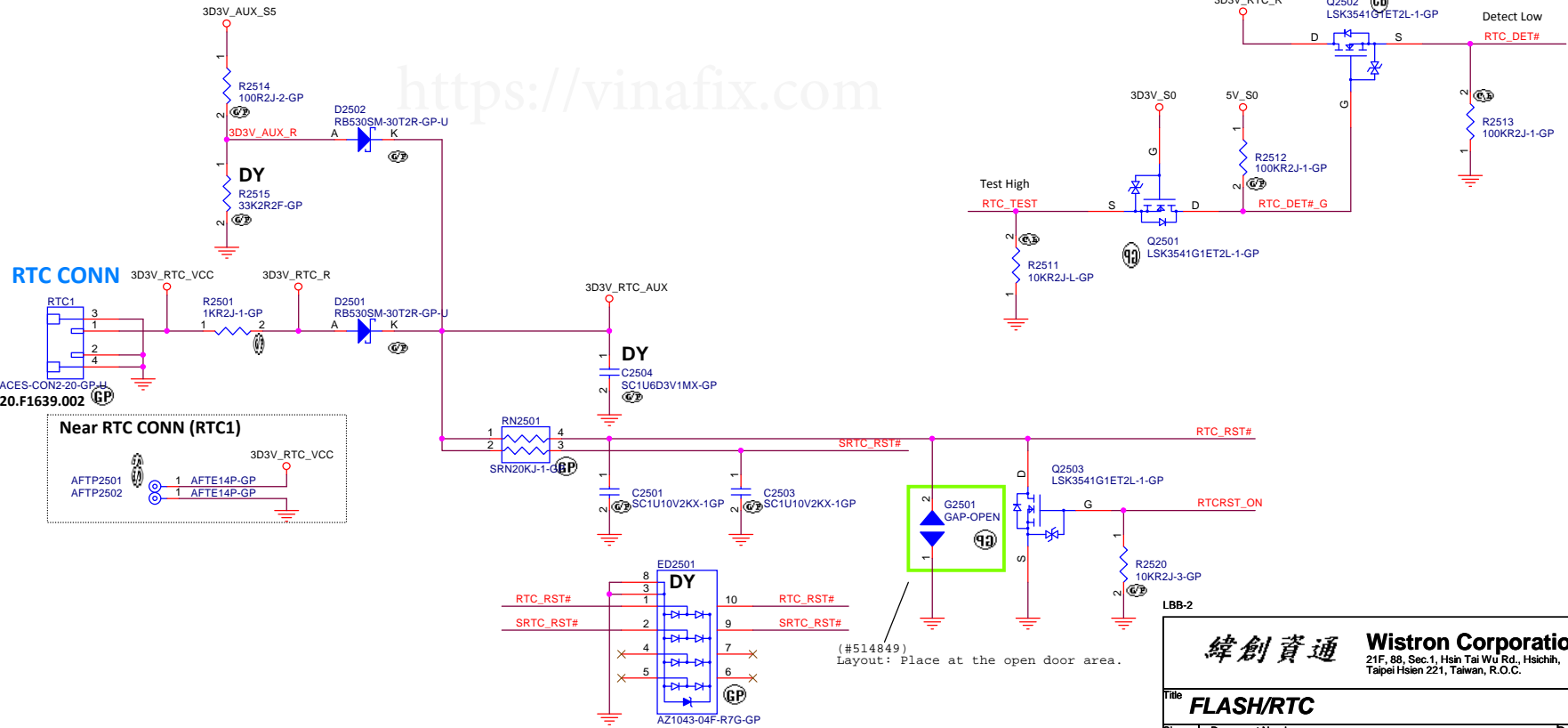


Co-Layout Design on BIOS1
SPI socket mount in SA stage
SOP 8 package only

208MIL SOIC8 (BIOS1) WSON8 / SOP8:		32MB (256Mb) non-vPro	32MB (256Mb) vPro	
MACRONIX	MX25L25673GM2I-08G	072.25256.0001	072.25256.0C01	(SOP8)
GIGADEVICE	GD25B256DYIGR	072.25256.0B03	072.25256.0C03	(WSON8)
MICRON	MT25QL256ABA1EW9-OSIT	072.25256.0E03	072.25256.0D03	(WPDFN8)

Main Func = RTC

18,99 RTC_RST#
18 SRTC_RST#
20 RTC_DET#
19 RTC_TEST
24 RTCRST_ON



(#514849)
Layout: Place at the open door area.

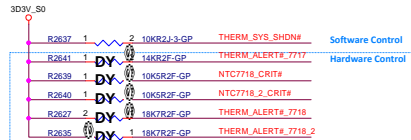
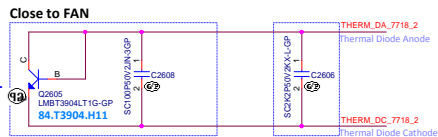
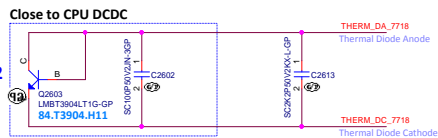
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title FLASH/RTC	
Size A3	Document Number Bumblebee-2
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Thermal Sensor

TABLE:

Sensor	Target
U2603	DIMM
U2604	Charger
U2601	SSD
Q2603	CPU DCDC
Q2605	FAN



Alert# / T_CRIT# Pull-up Resistor v.s. Alert temperature (°C)

NCT7717U Table:		R2627 \ R2639 R2635 \ R2640		2.0K	7.5K	10.5K	14.0K	18.7K
R2641								
2.0K	75	2.0K	77	87	97	107	117	
7.5K	90	7.5K	79	89	99	109	119	
10.5K	100	10.5K	81	91	101	111	121	
14.0K	105	14.0K	83	93	103	113	123	
18.7K	110	18.7K	85	95	105	115	125	

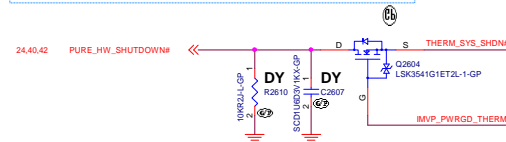
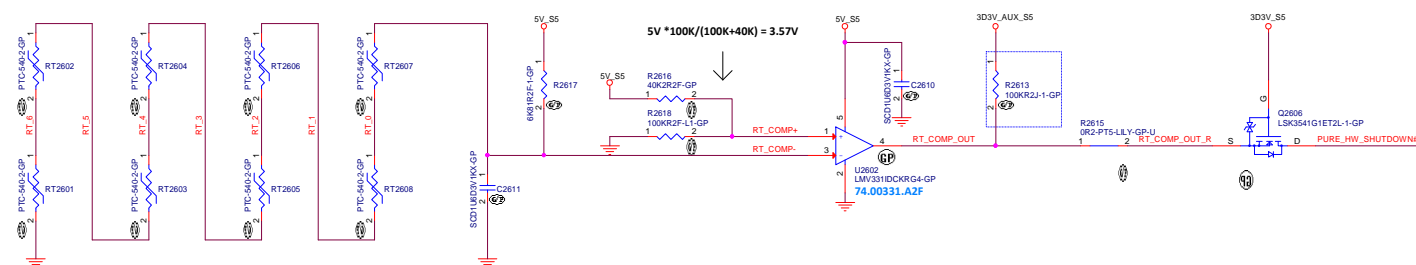


TABLE:

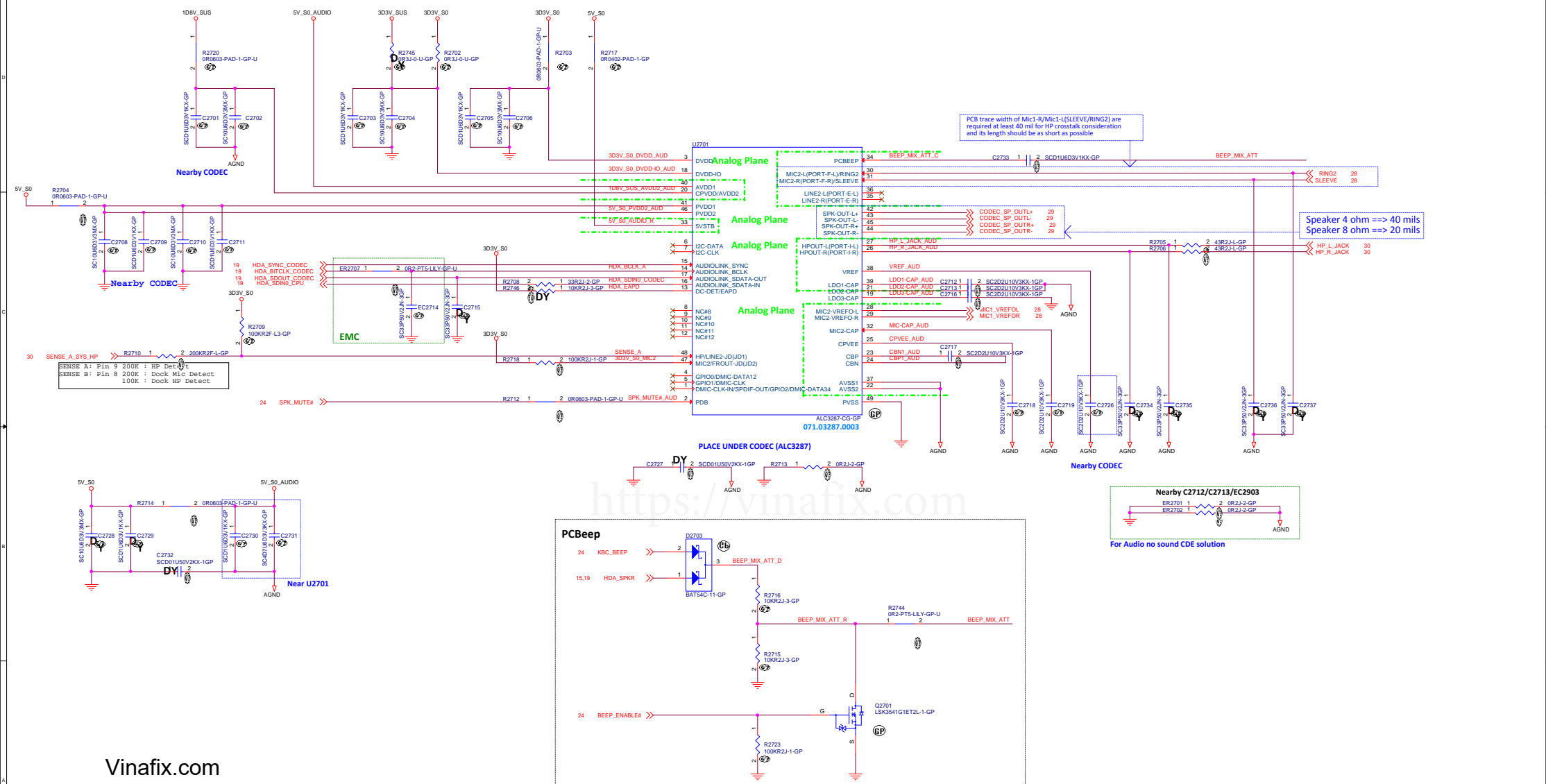
ID	Target	Function
RT2601	PUS101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PO5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PO4505	5V_S5
RT2606	PO4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost



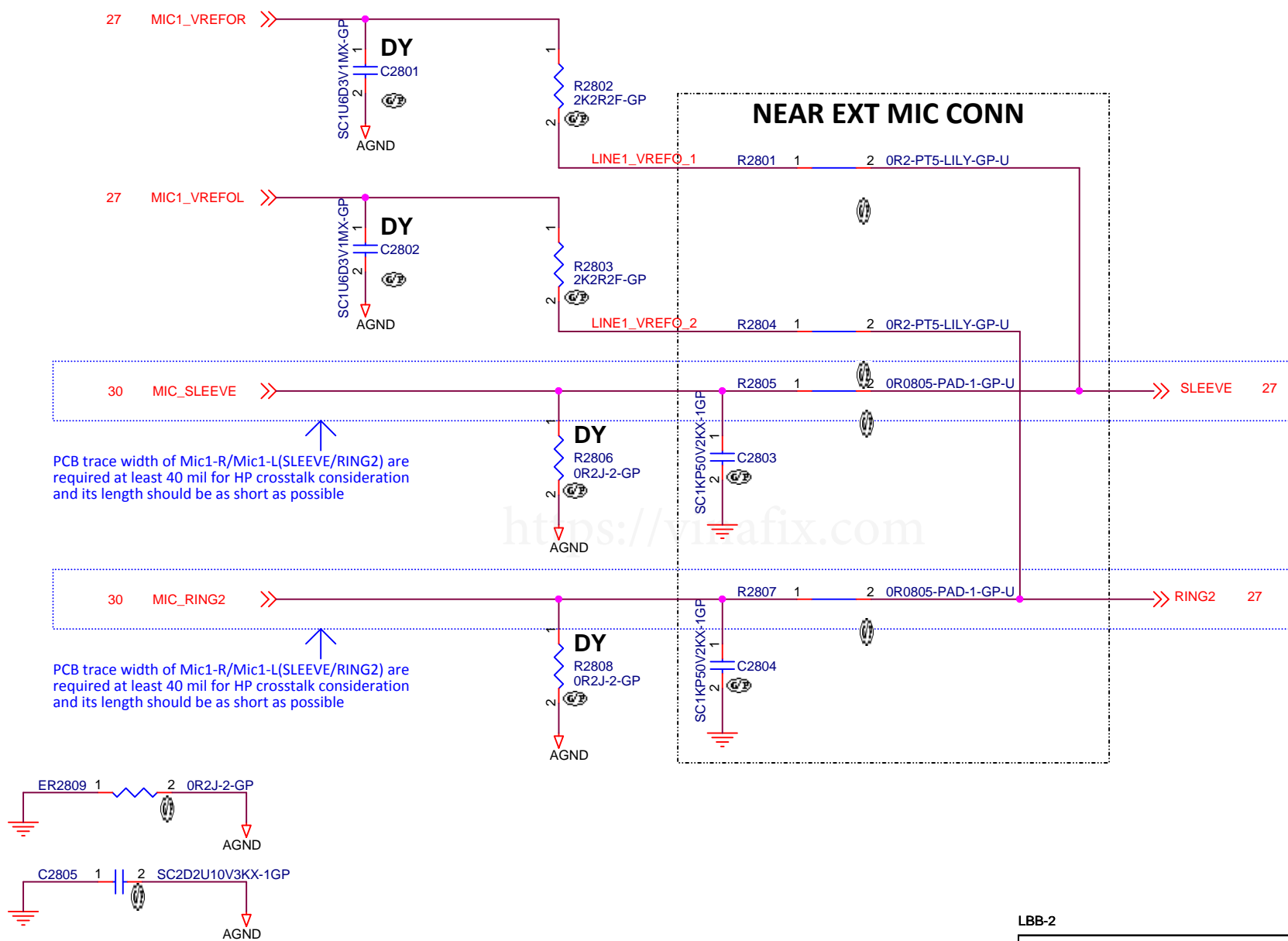
PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

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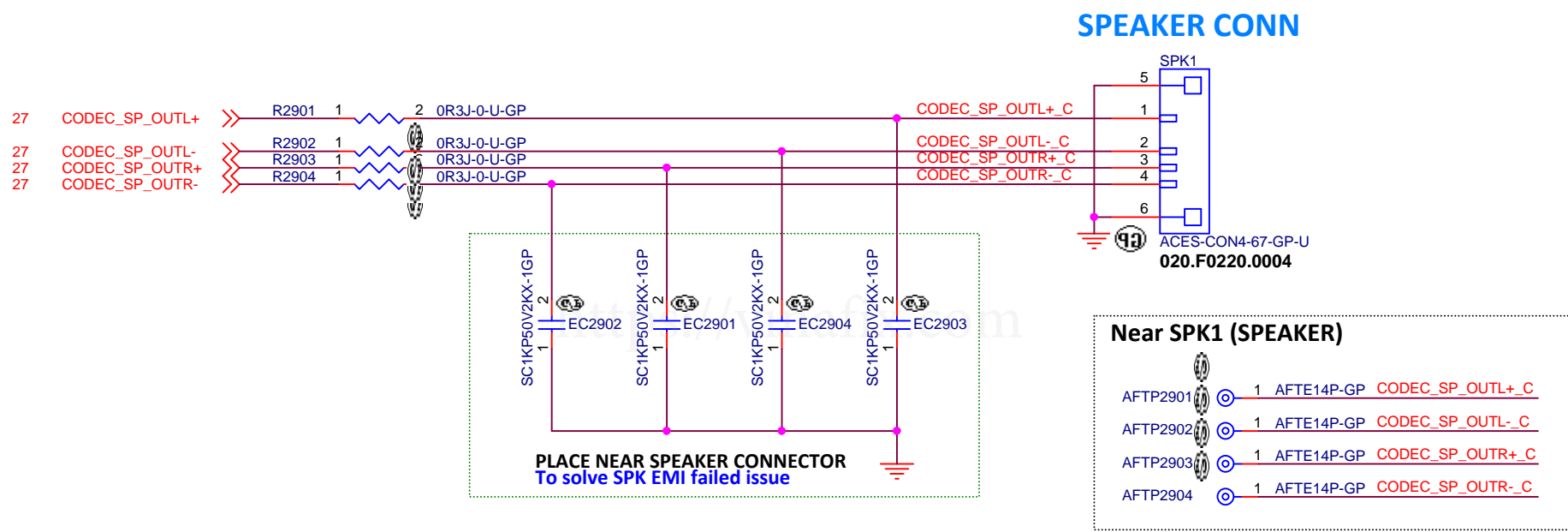


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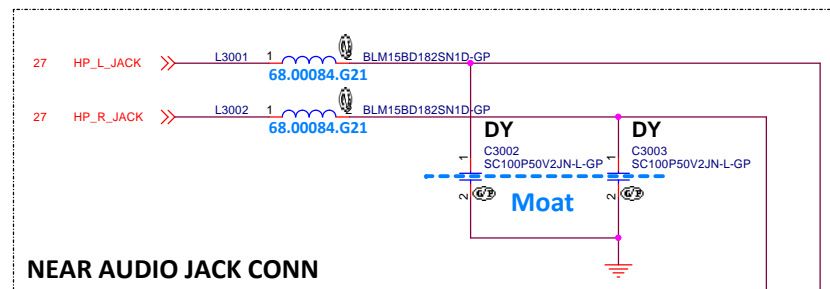
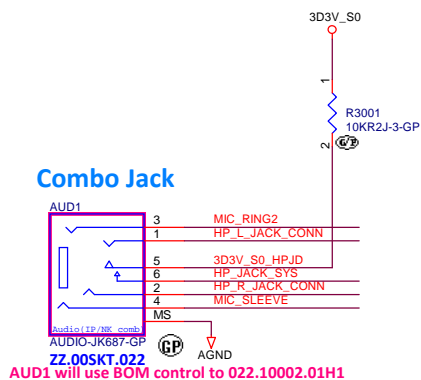
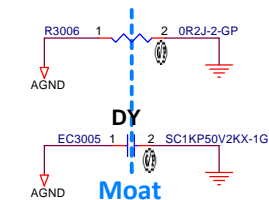
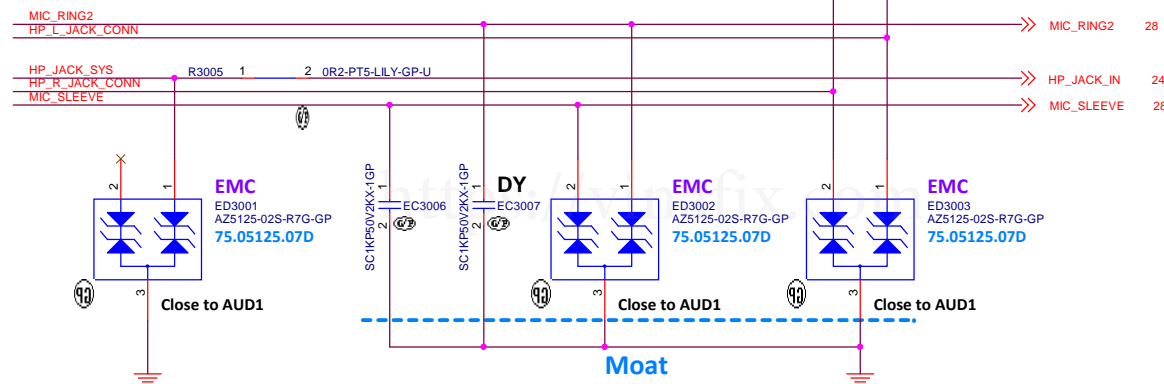
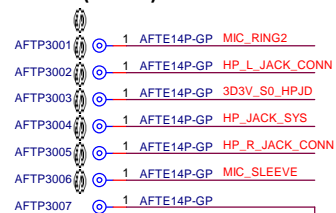
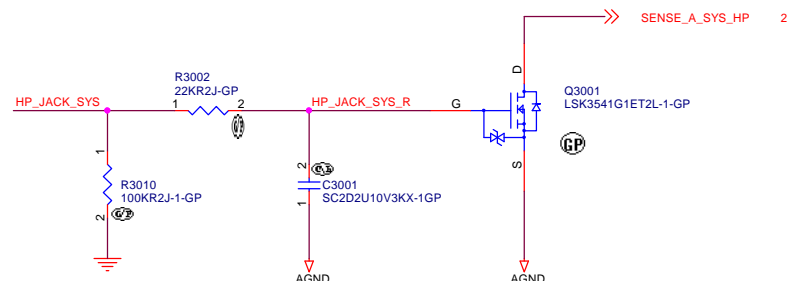


LBB-2

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO (MIC I/F)			
Size	Document Number		Rev
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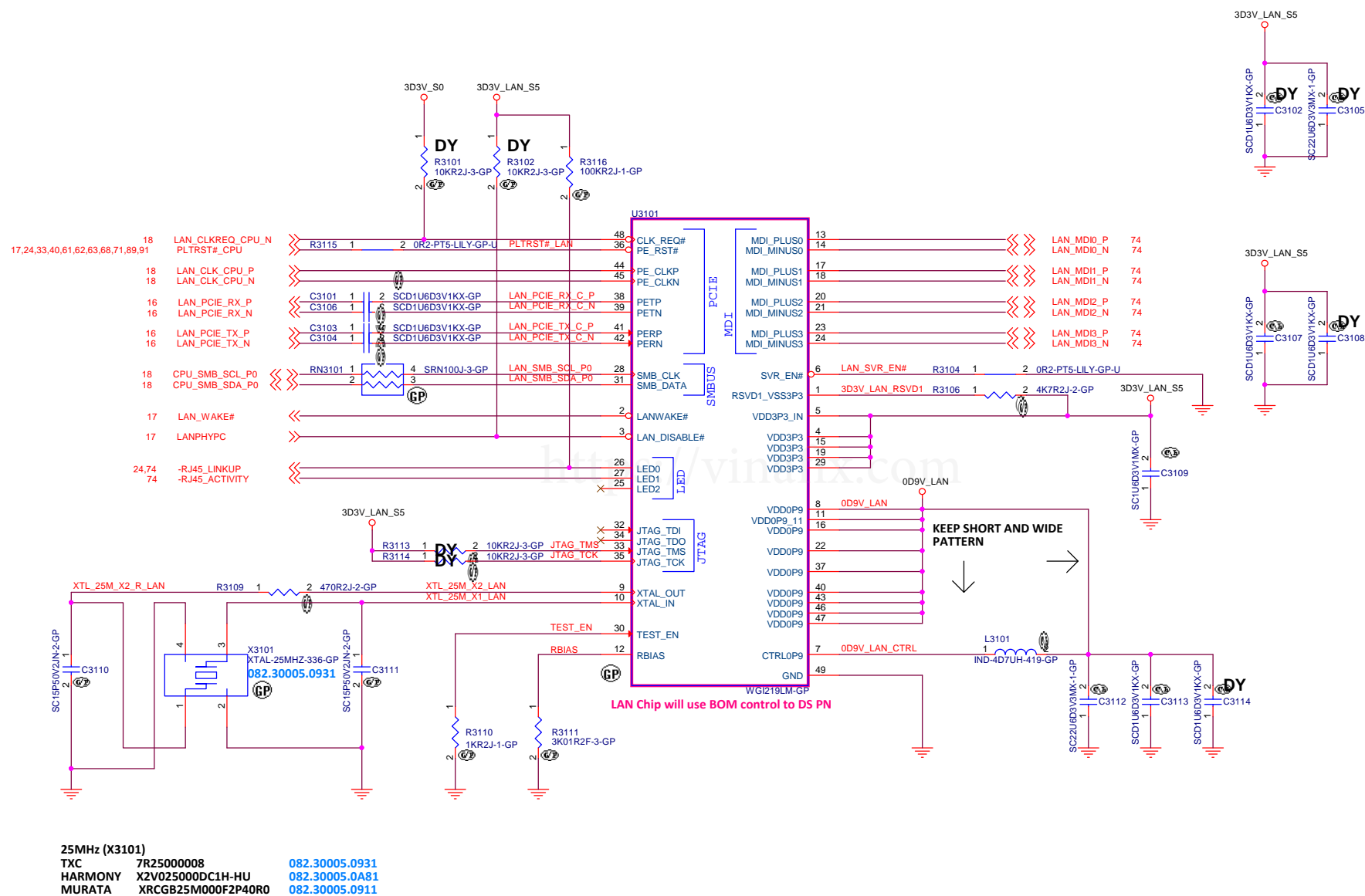
**AUDIO JACK SENSE**
CLOSE TO CODEC
6-10 mil trace recommendHGND A/HGND B trace width >70mil,
changed to sharp will be better.**Combo Jack****Near AUD1 (AUDIO)****AUDIO JACK SENSE**

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.**AUDIO (AUDIO JACK)**

Size	Document Number	Rev
A3	Bumblebee-2	1

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD)

Size
A4

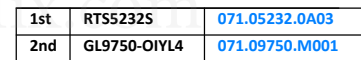
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Bumblebee-2

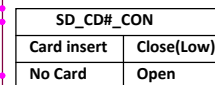
Rev
1

Date: Tuesday, March 03, 2020

Sheet 32 of 106



Layout Note:
Stub are too longer, delete test points



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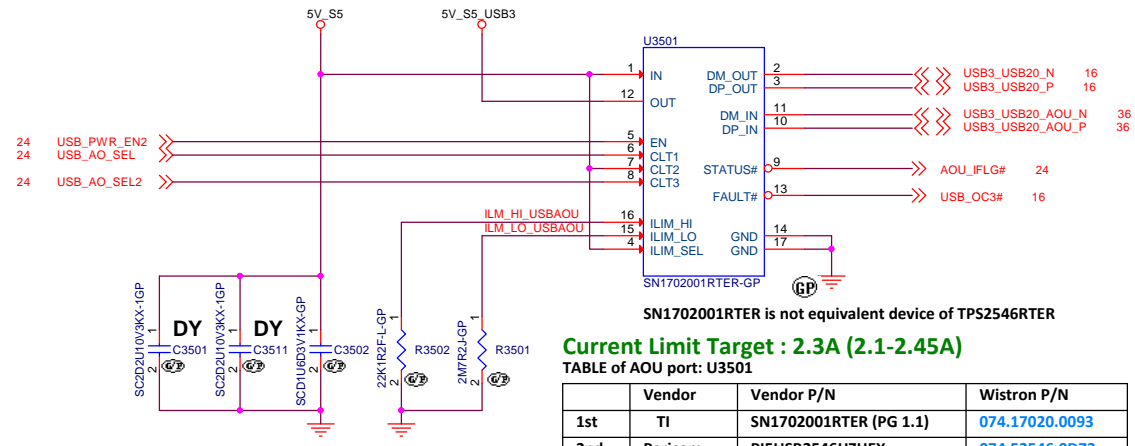
<https://vinafix.com>

LBB-2

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title USB (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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Main Func = USB Charger

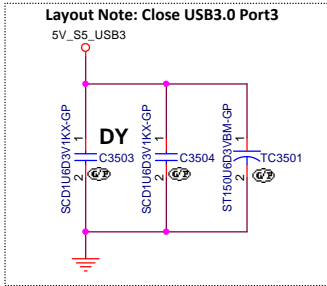
For USB3.0 System Port3 (For AOU)



Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73



For USB3.0 System Port4

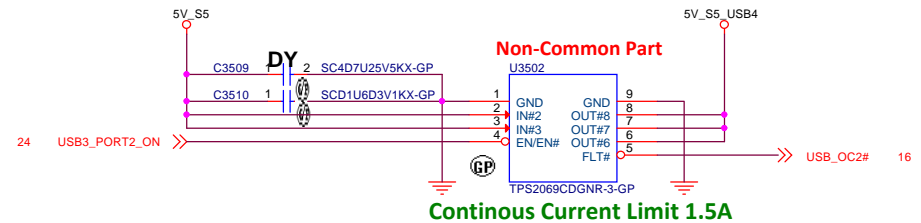
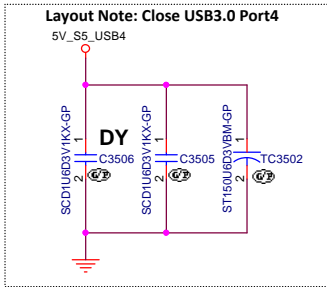
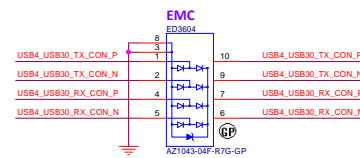
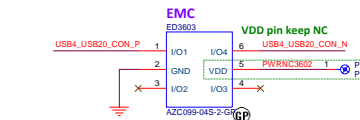
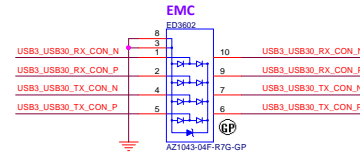
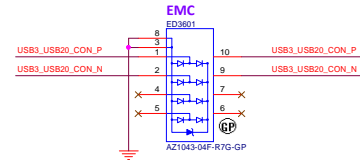
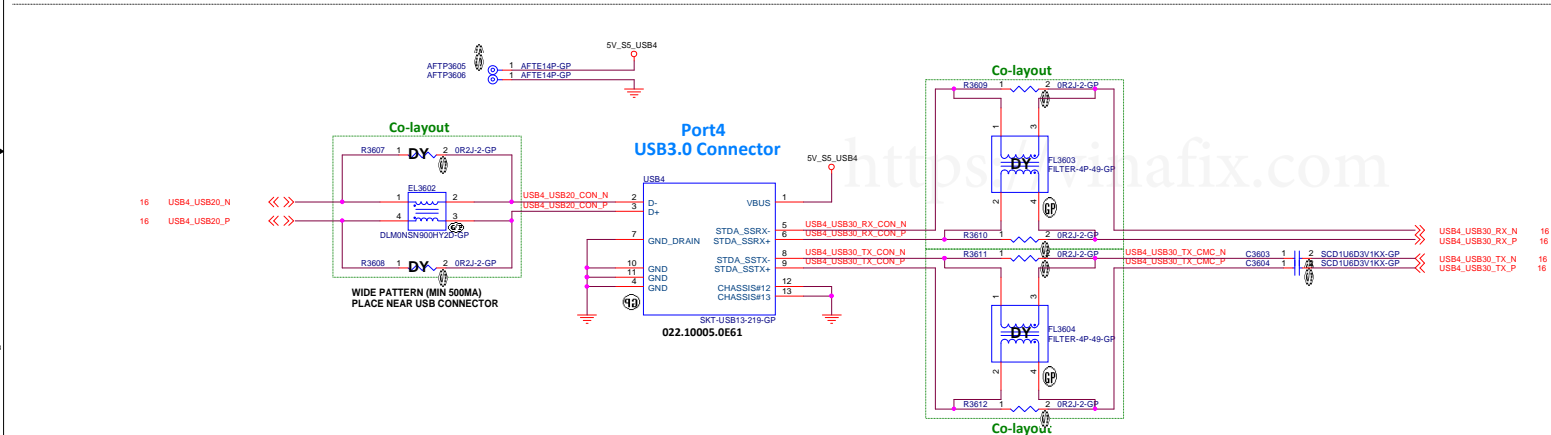


TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGMR	074.02069.M001
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G



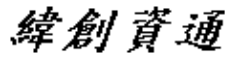
Main Func = USB3.0 Port4



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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<div>緯創資通</div> <div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title USB (RSVD)		
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緯創資通

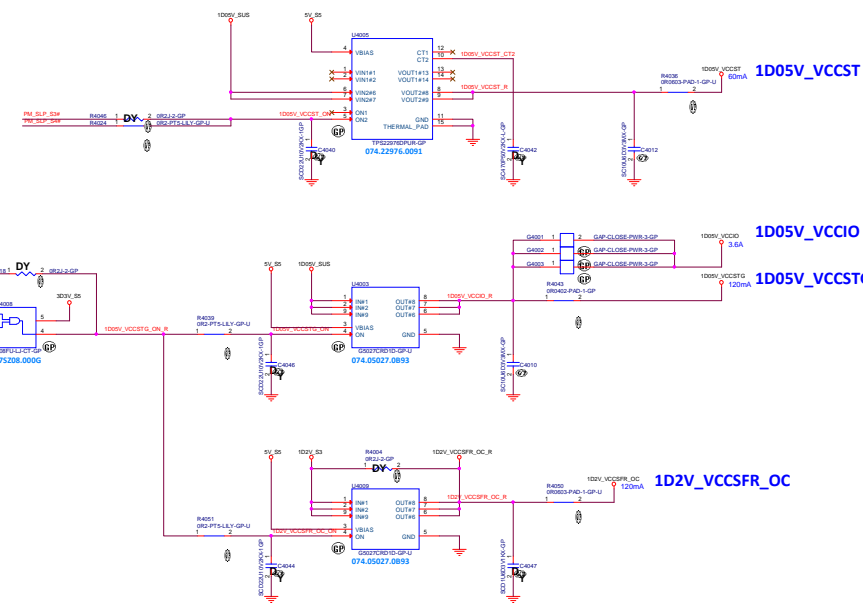
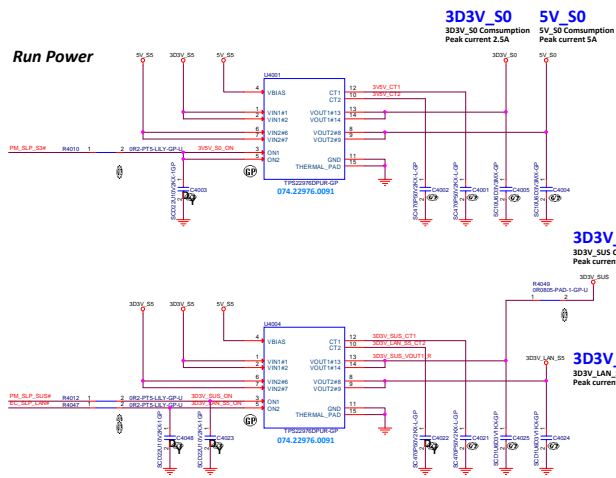
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **SEQUENCE (RSVD)**

Size A4	Document Number Bumblebee-2	Rev 1
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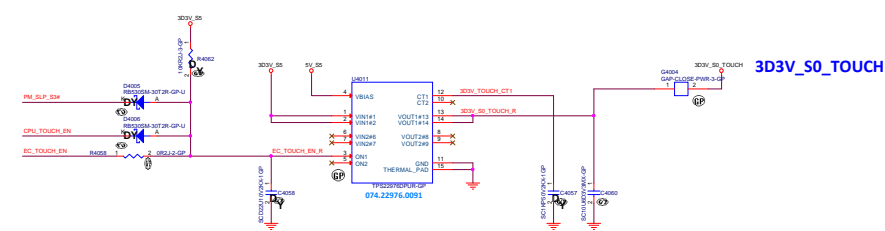
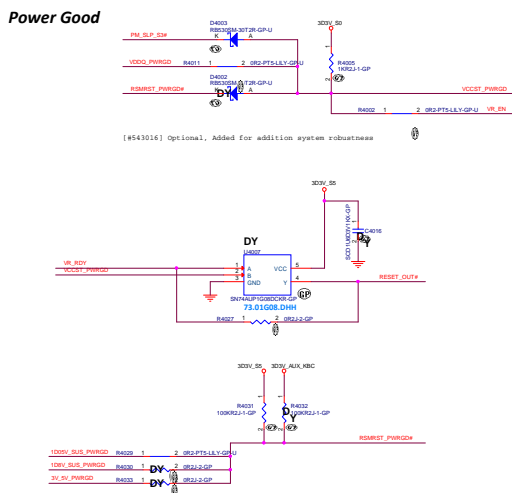
Run Power



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Power Good



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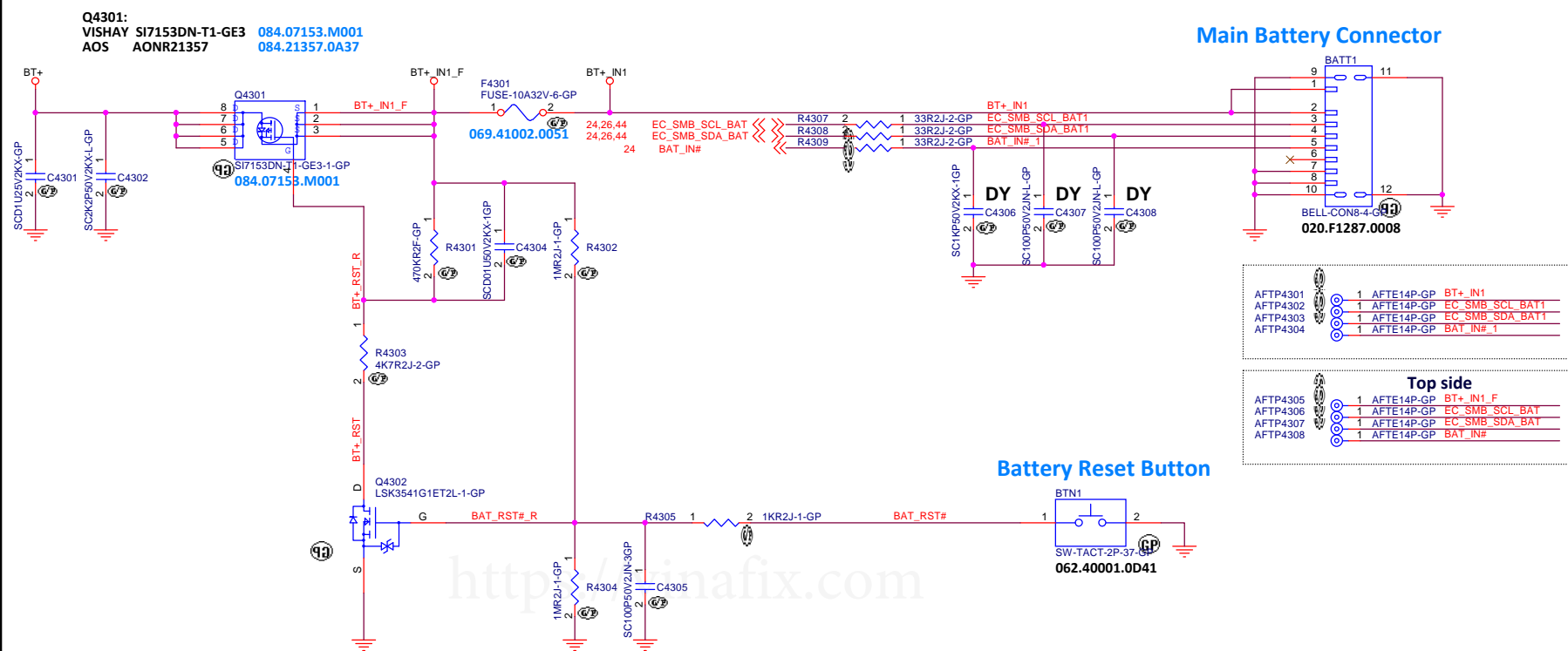
<https://vinafix.com>

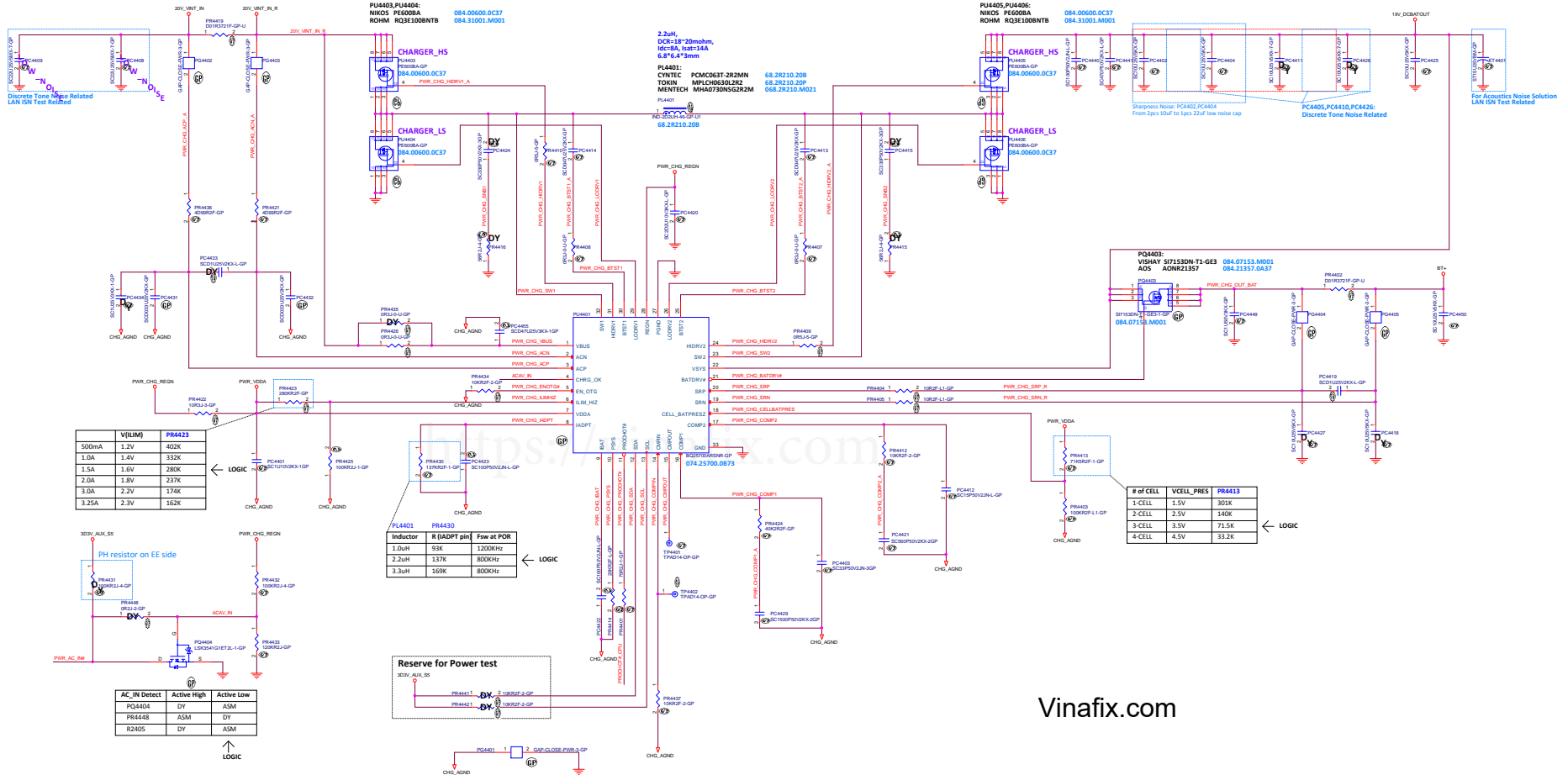
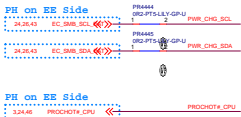
LBB-2

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title SEQUENCE (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020		Sheet 41 of 106

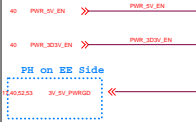
BB2_EVT_MAIN_W006
BB2_EVT_MAIN_W008
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003



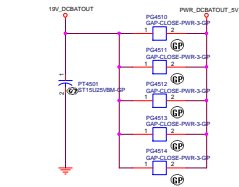
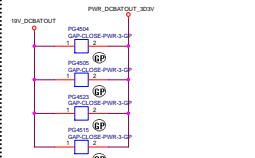




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PT4501:		
PANASONIC	25TQC15MYFB	77.21561.01L
NEC TOKIN	TEPSLB21E156M8R	77.C1561.06L

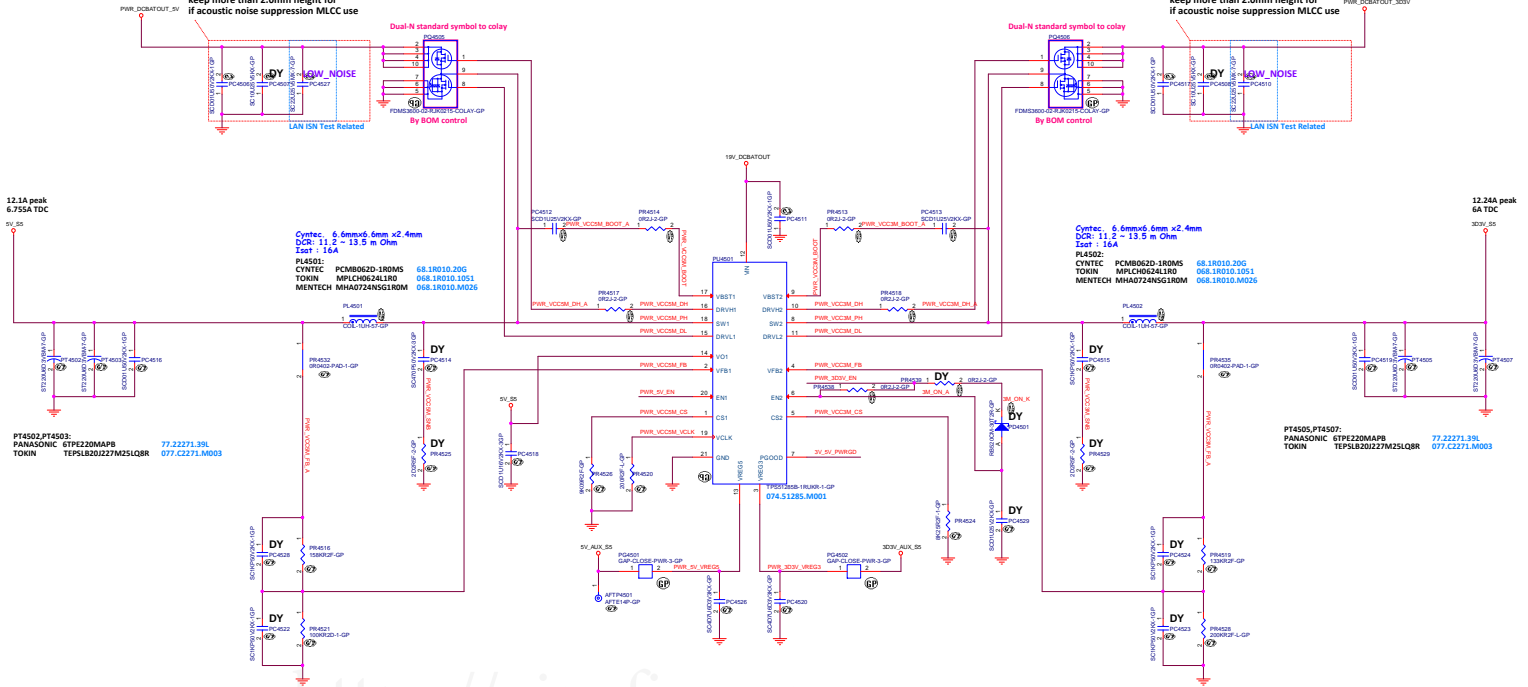
PT4502,PT4503:
PANASONIC 6TPE220MAPB 77.22271.39L
TOKIN TEPSLB20J227M25LQ8R 077.C2271.M003

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

PQ4505:
AOS AONY36354 075.36354.0073
INFINEON BSC0923NDI 075.00923.M001

PQ4506:		
AOS	AONY36354	075.36354.0073
INFINEON	BSC0923NDI	075.00923.M001

keep more than 2.0mm height for
if acoustic noise suppression MLCC use



PT4505,PT4507:
PANASONIC 6TPE220MAPB 77.22271.39L
TOKIN TEPSLB20J227M25LQ8R 077.C2271.M003



```
Main Func = CPU_CORE
```

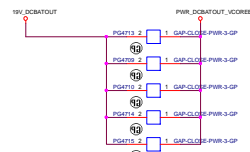
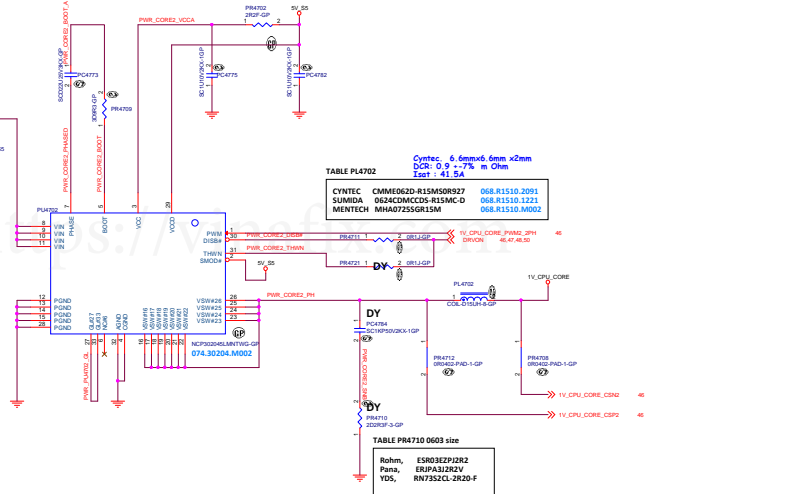
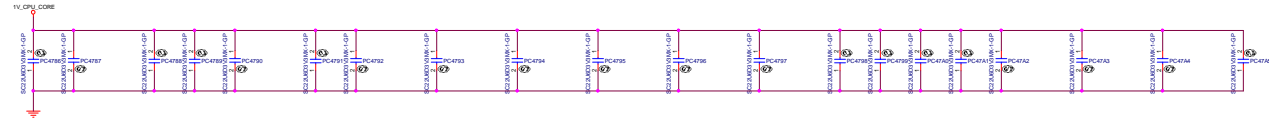
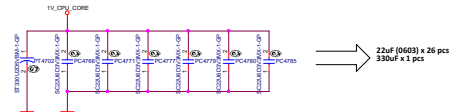


TABLE for PT4702		
NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001



	PR4704 PR4711	PR4714 PR4721
NCP302045L	0 Ohm	DY

Cyrtec, 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

2D-R15MS0R927	068.R1510.2091
MCCDS-R15MC-D	068.R1510.1221
ISSGR15M	068.R1510.M002

CMME062D-R15MSOR927	068.R1510.2091
0624CDMCCDS-R15MC-D	068.R1510.1221
MHA07255GR15M	068.R1510.M002

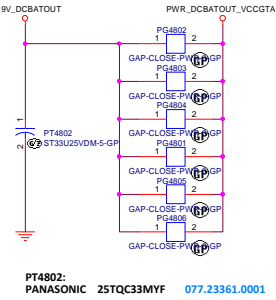
Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

OFFPAGE

Main Func = CPU_CORE

BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006



Max Current = 3.88(A)

MLCCs must be placed symmetrically on Top and Bottom.

keep more than 2.0mm height for if acoustic noise suppression MLCC use

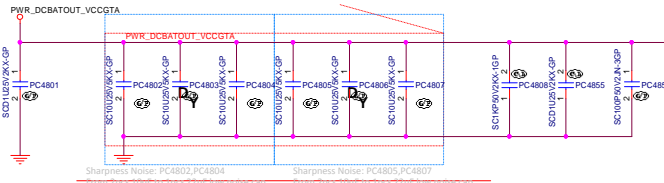


TABLE for PU4801

ON-semi NCP302045

TABLE for PT4801

NEC TOKIN PSGB20E337M9 80.3371V.A2L
PANASONIC ETPE330MA9L 077.23371.M001

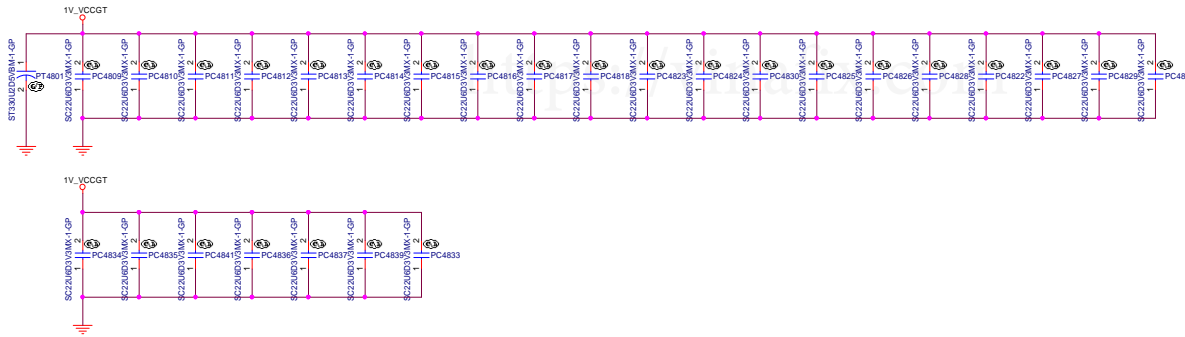


TABLE PL4802

CYNTEC CMMED62D-R15MSOR927 068.R1510.2091
SUMIDA 0624CDMCCDS-R15MC-D 068.R1510.1221
MENTECH MHA0725SGR15M 068.R1510.M002

Cynotec 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Iset : 41.5A

	PR4804	PR4814
NCP302045L	0 Ohm	DY

31A Iccmax
(TDC: 18A)

TABLE PR4803 0603 size

Rohm, ESR03EZPJ2R2
Pana, ERJPA3J2R2V
YDS, RN75S2CL-2R20-F

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Title POWER (NCP302045L_VCCGT)			
Size A2	Document Number	Bumblebee-2	Rev 1
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Main Func = CPU_CORE

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Title POWER (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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OFFPAGE

S5

7.34.40.00 PM_SLP_S4H >>>

S3

5 VTT_CNVL >>>

PH on EE Side

40 VDDQ_PHWGD <<<

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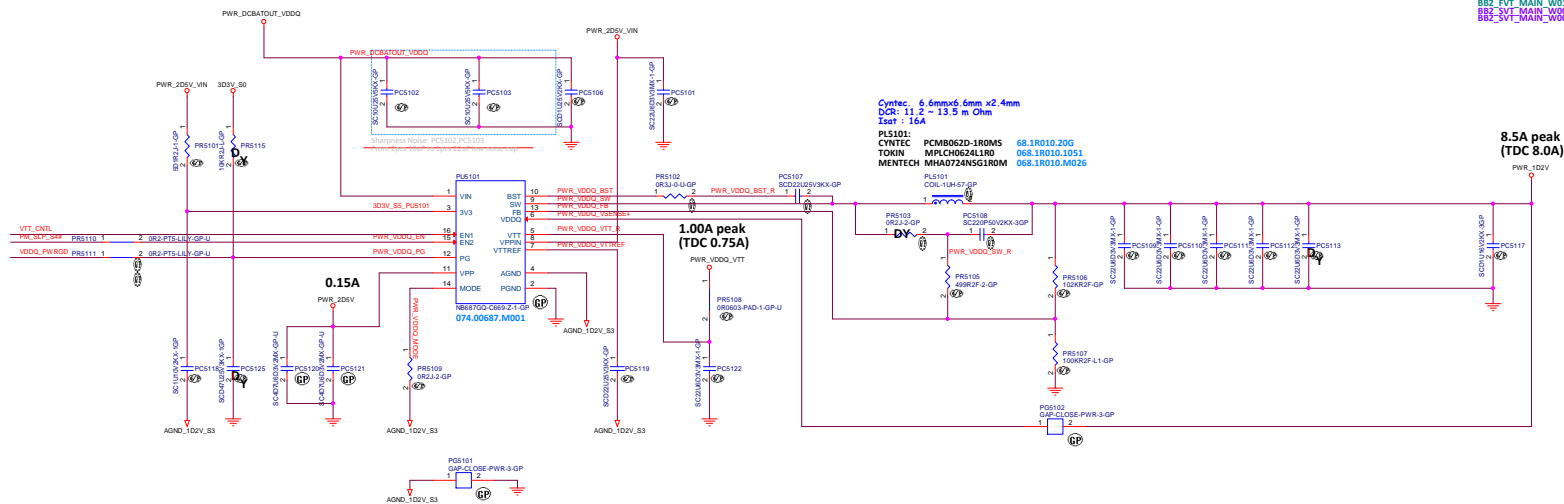
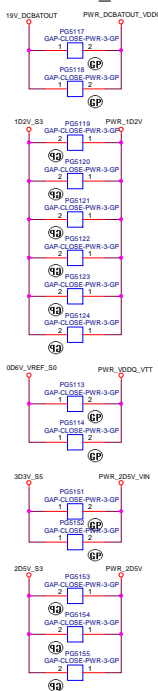


Table 1: EN1/EN2 Control

State	EN1	EN2	VDDQ	VPP	VTT	VTT
S0	High	High	On	On	On	On
S3	Low	High	On	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off	Off
Others	High	Low	Off	Off	Off	Off

Table 2: Mode Selection

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Ω
M2	Yes	700kHz	90kΩ
M3	No	500kHz	150kΩ
M4	Yes	500kHz	>230kΩ or float

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LSB-2

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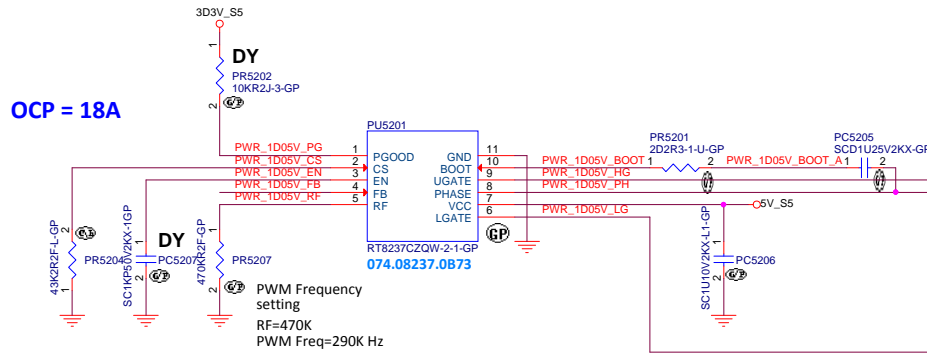
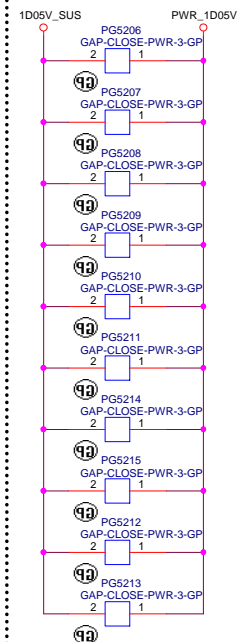
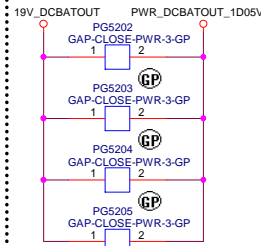
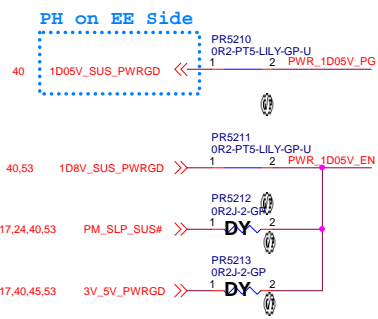


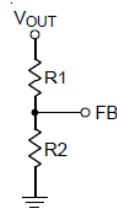
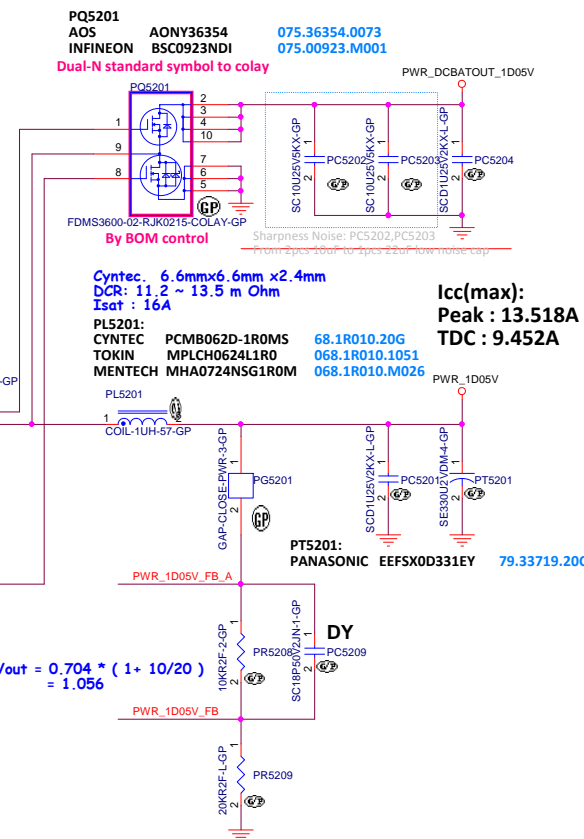
Table 1. RF Connection and Switching Frequency

R_{RF} (k Ω)	Switching Frequency (kHz)
470k Ω	290
200k Ω	340
100k Ω	380
39k Ω	430

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

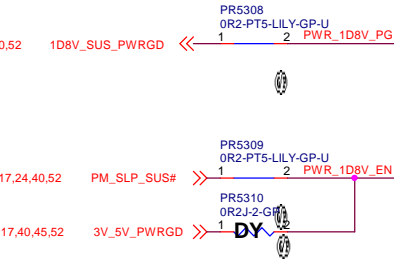
where V_{REF} is 0.704V (typ.).

Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

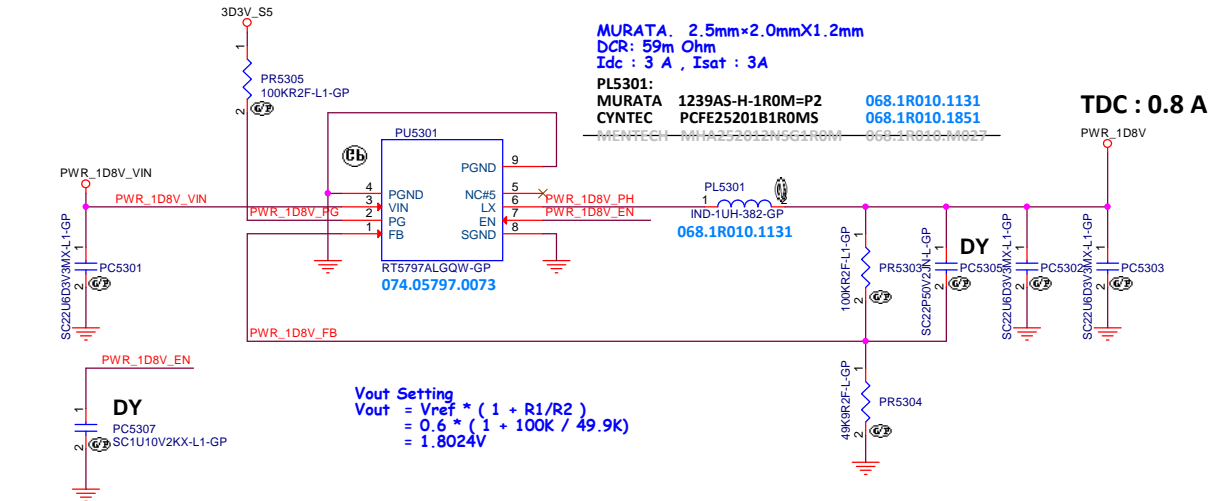
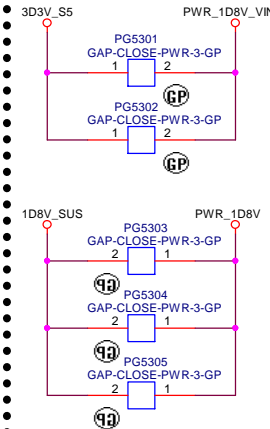
$$V_{out} = 0.704 * (1 + 10/20)$$
$$= 1.056$$

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Taipei Hsien 221, Taiwan, R.O.C.

Title **POWER (RSVD)**

Size
A4

Document Number

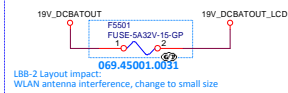
Bumblebee-2

Rev
1

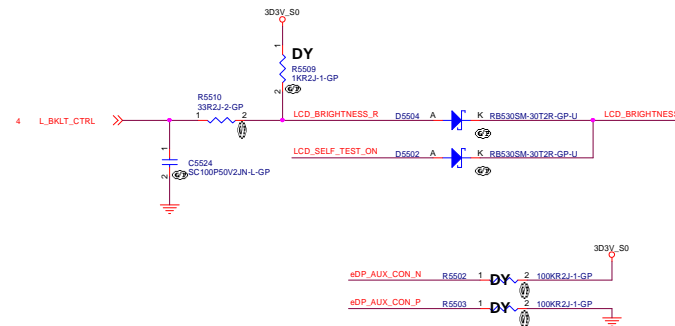
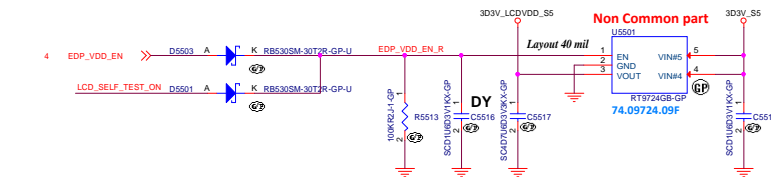
Date: Tuesday, March 03, 2020

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LCD Backlight Power



For LCD DCBATOUT inrush current



LCD Connector

Near LCD1 (LCD)

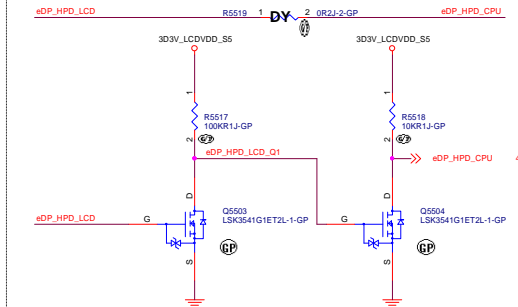
AFTP5501	1	AFTE14P-GP	TOUCH_STOP#
AFTP5501	1	AFTE14P-GP	LCD_BRIGHTNESS
AFTP5501	1	AFTE14P-GP	BLON_OUT_C
AFTP5501	1	AFTE14P-GP	EPRIVACY_CONTROL
AFTP5501	1	AFTE14P-GP	LCD_SELF_TEST_ON
AFTP5501	1	AFTE14P-GP	303V_LCDVDD_S5
AFTP5501	1	AFTE14P-GP	19V_DCBATOUT_LCD
AFTP5501	1	AFTE14P-GP	303V_S0_TOUCH
AFTP5501	1	AFTE14P-GP	
AFTP5501	1	AFTE14P-GP	

DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

For eDP VESA spec. requirement

Regarding to Intel CML/TGL platform eDP_HPD VIH cannot meet VESA Spec requirement

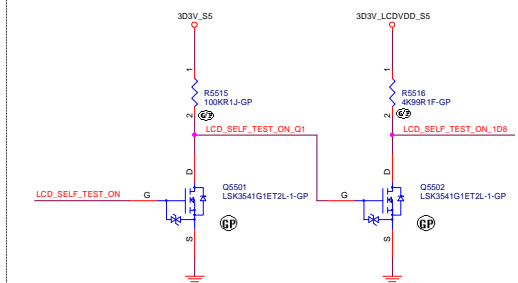
EDP_HPD	Intel CML	VIH	0.7 x VDD_3.3 = 2.31 ~ 2.59V
	VESA		2.25 ~ 3.6V



OLED Panel input voltage is 1.8V

Regarding to input voltage of BIST, please see table below: LCD_SELF_TEST_ON_1D8

Input Voltage	H-Level	VIH	0.7 x VDD_1.8	VDD_1.8	VDC
	L-Level	VIL	Vss	0.3 x VDD_1.8	VDC



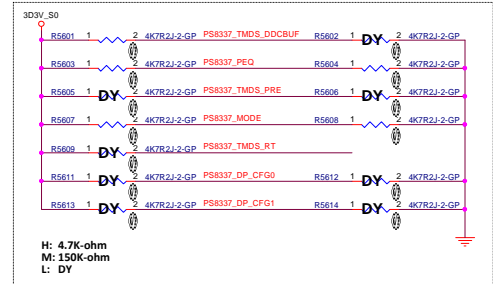
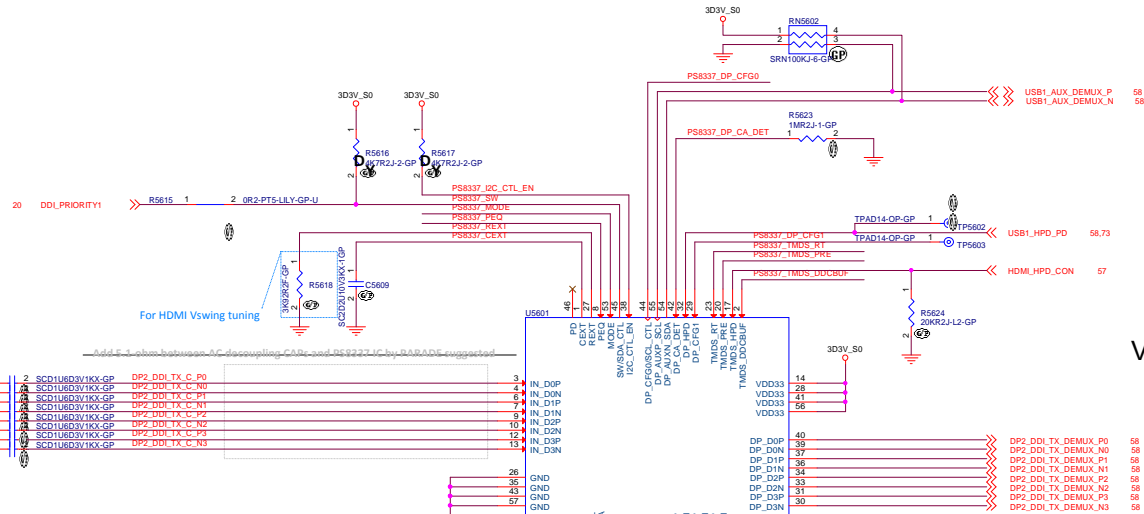
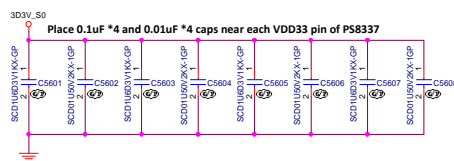
LBB-2

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY1)

L: USB Type-C has higher priority when both ports are plugged
H: HDMI Port has higher priority when both ports are plugged

Note: SW is pulled down with 150K-ohm internally

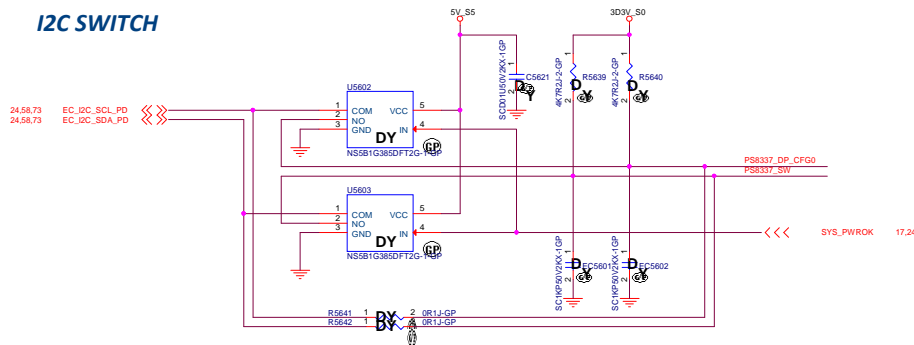


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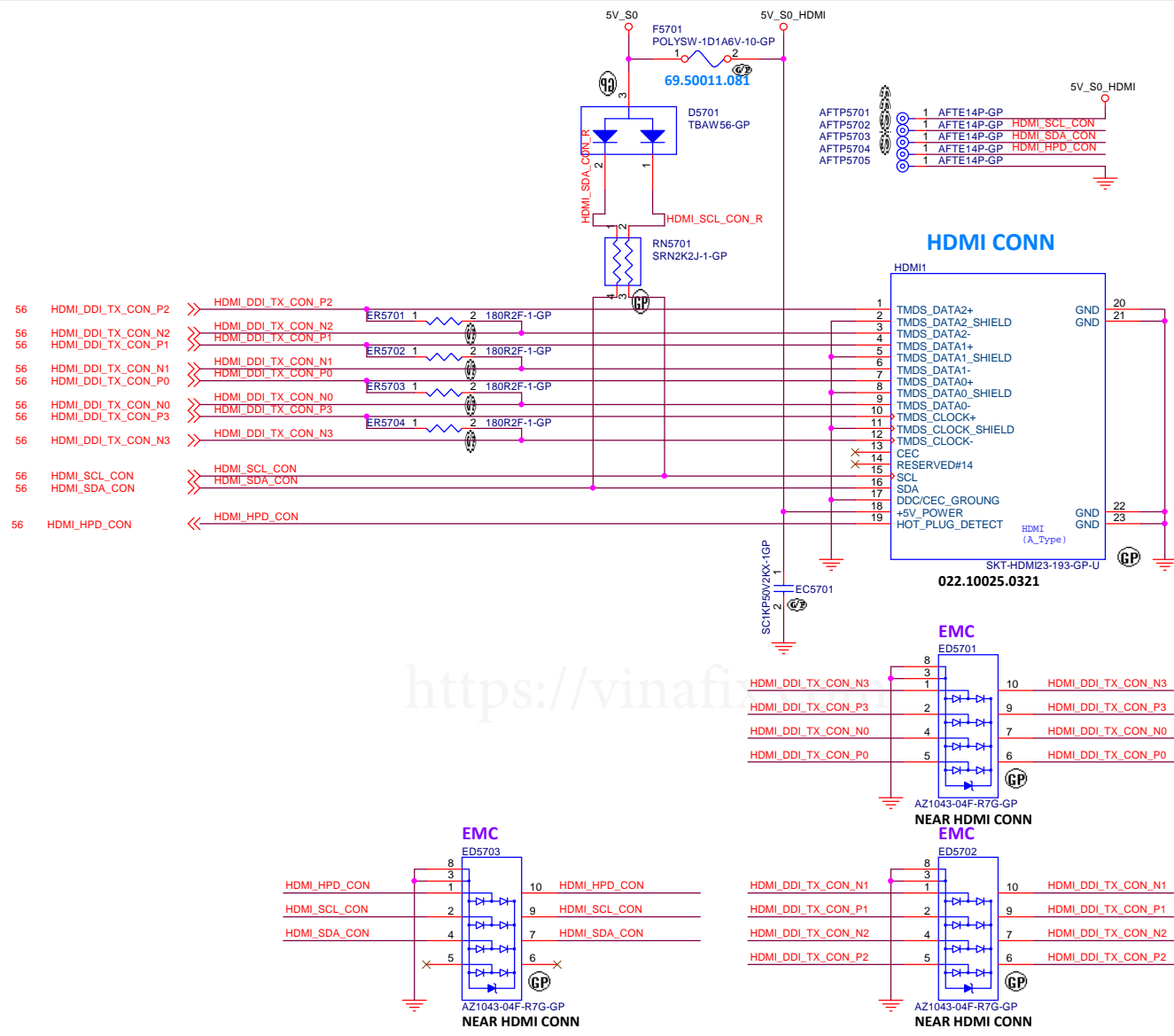
TO PS8747B

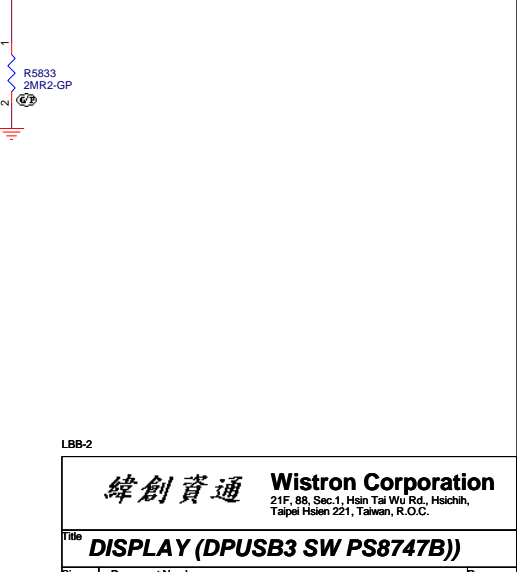
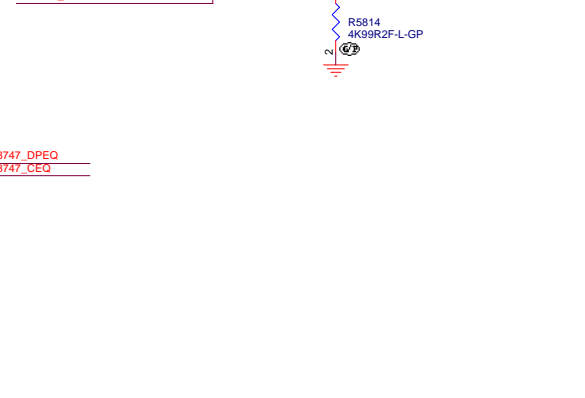
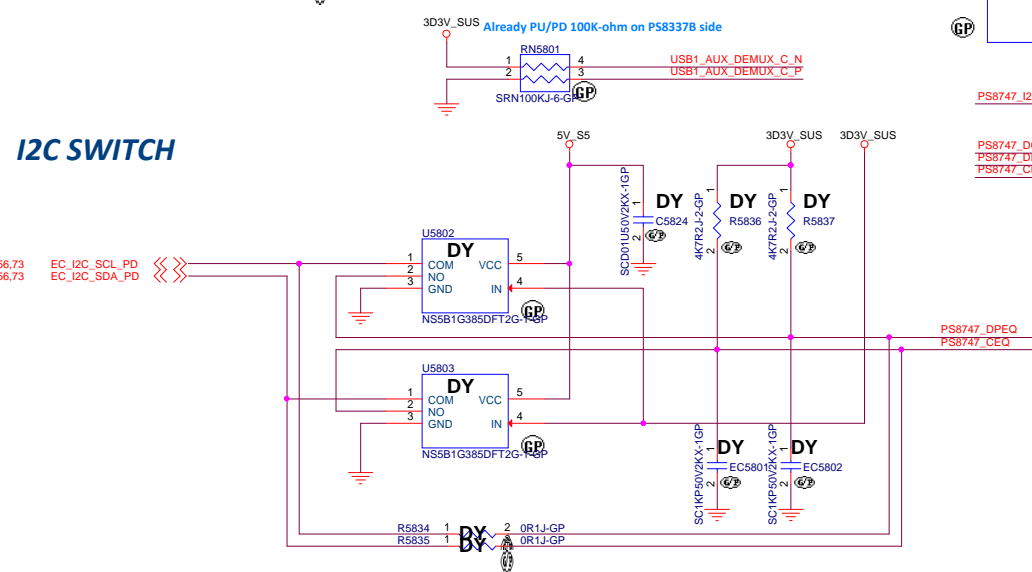
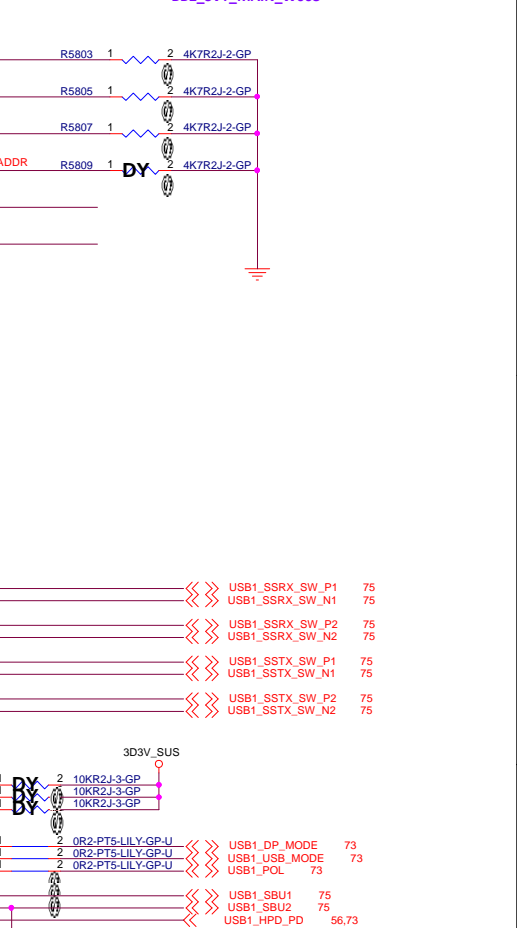
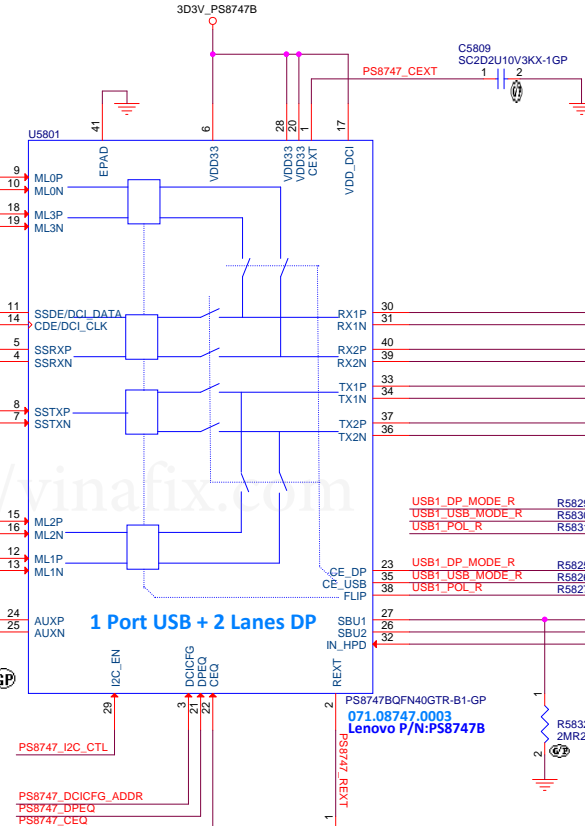
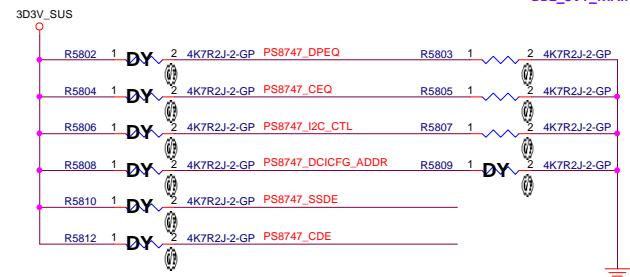
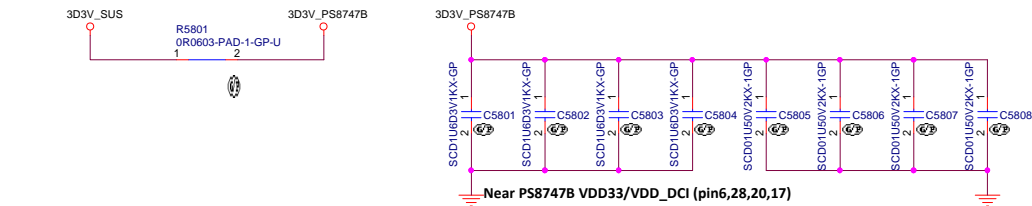
HDMI

I2C SWITCH

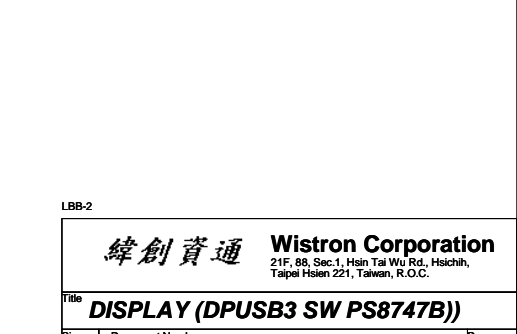
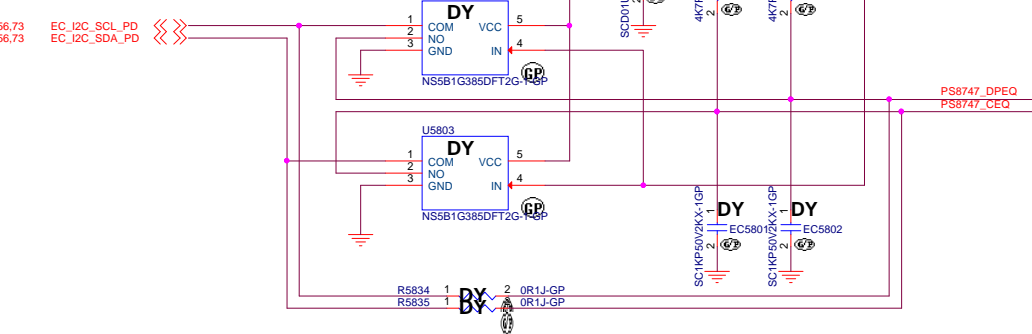


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I2C SWITCH



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Title DISPLAY (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 59 of	106

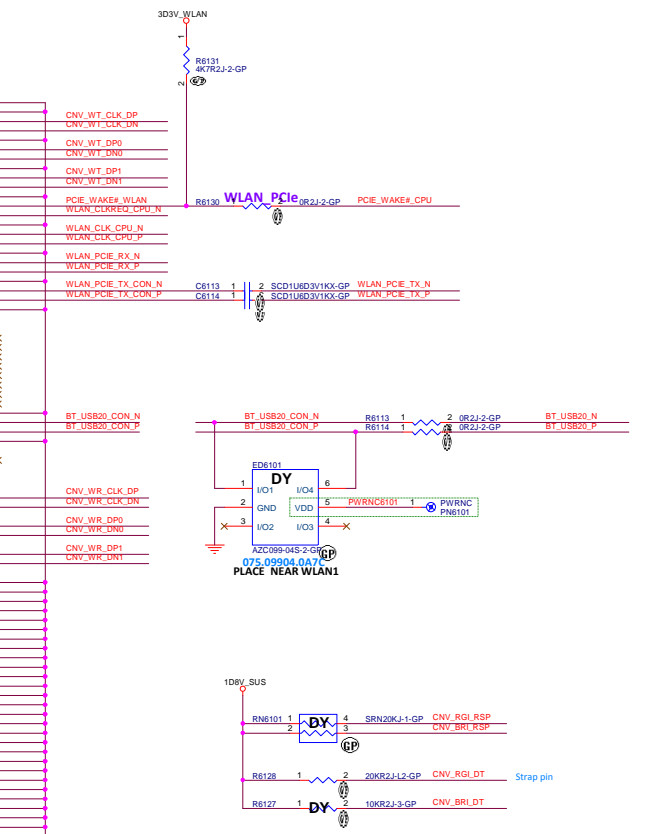
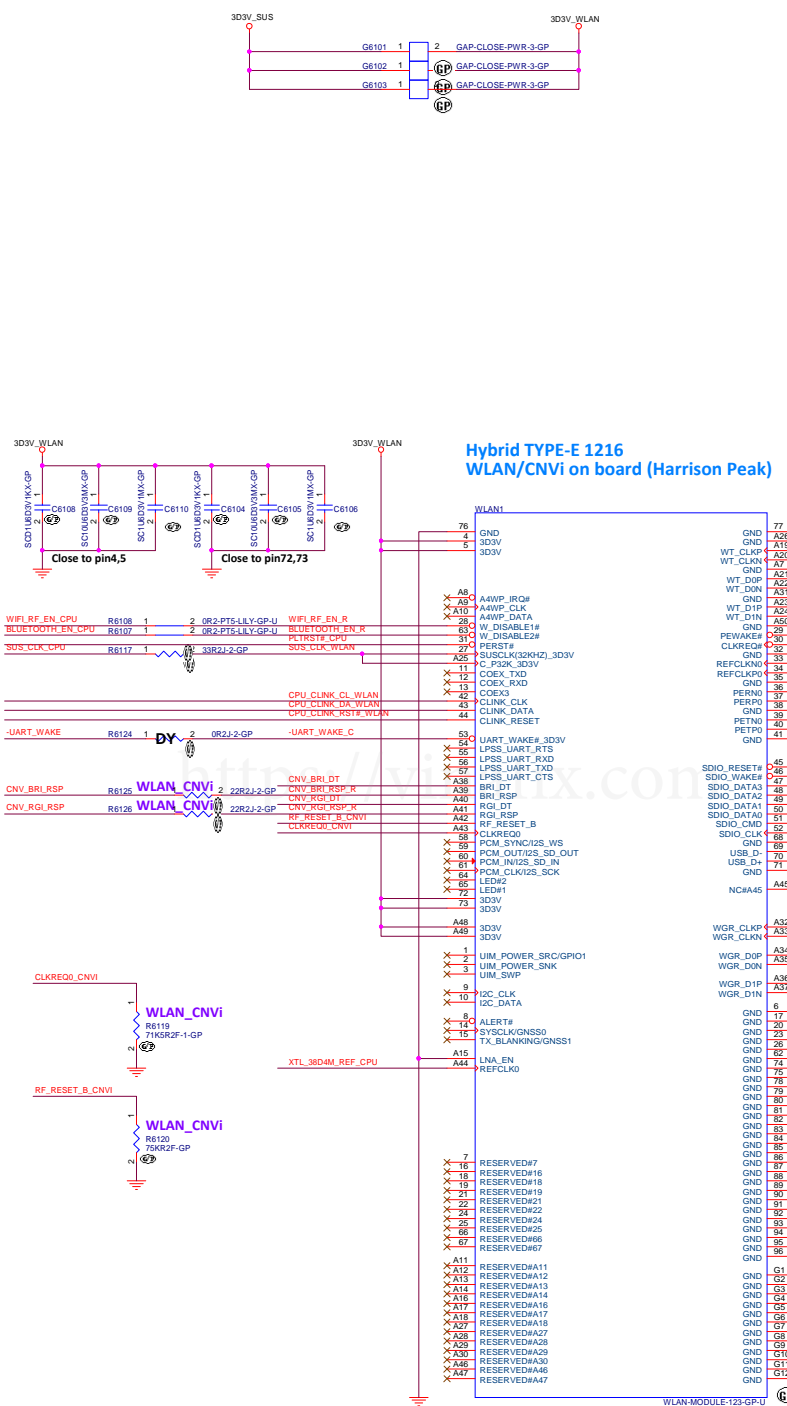
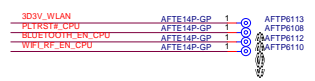
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Title INT IO (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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- 18 WLAN_CLKREQ_CPU_N <<
- 17,33,62,71 PCIE_WAKE#_CPU >>
- 18 XTL_3804M_REF_CPU <<
- 21 WIFI_RF_EN_CPU >>
- 20 CNV_RGI_DT >>
- 15,20 CNV_RGI_DT >>
- 20 CNV_BRI_RSP <<
- 19 CLKREQ0_CNVI <<
- 19 RF_RESET_B_CNVI >>
- 21 CNV_WT_CLK_DP >>
- 21 CNV_WT_CLK_DN >>
- 21 CNV_WT_DP0 >>
- 21 CNV_WT_DN0 >>
- 21 CNV_WT_DP1 >>
- 21 CNV_WT_DN1 >>
- 21 CNV_WR_CLK_DP >>
- 21 CNV_WR_CLK_DN >>
- 21 CNV_WR_DP0 >>
- 21 CNV_WR_DN0 >>
- 21 CNV_WR_DP1 >>
- 21 CNV_WR_DN1 >>
- 18 WLAN_CLK_CPU_N >>
- 18 WLAN_CLK_CPU_P >>
- 16 WLAN_PCIE_RX_N >>
- 16 WLAN_PCIE_RX_P >>
- 16 WLAN_PCIE_TX_N >>
- 16 WLAN_PCIE_TX_P >>
- 16 BT_USB20_N >>
- 16 BT_USB20_P >>
- 18 CPU_CLKIN_CL_WLAN >>
- 18 CPU_CLKIN_DA_WLAN >>
- 18 CPU_CLKIN_RSTA_WLAN >>
- 20 -UART_WAKE >>



054.03149.0021

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TYPE-M M.2 CARD FOR SSD

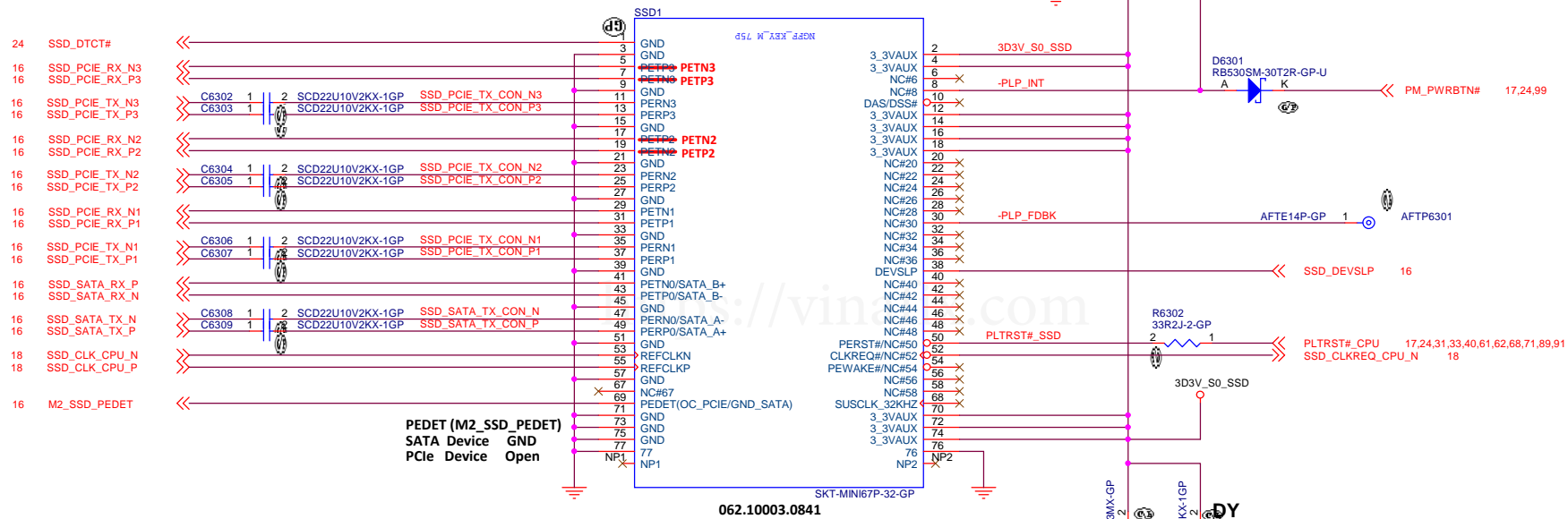


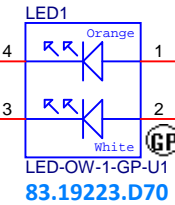
Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform

Pin	Signal	Signal	Pin
75	3.3V	GND	75
76	3.3V	GND	76
77	3.3V	GND	77
78	3.3V	PEDET (NC Pin/GND SATA)	78
79	3.3V	NC	79
80	3.3V	NC	80
81	3.3V	NC	81
82	3.3V	NC	82
83	3.3V	NC	83
84	3.3V	NC	84
85	3.3V	NC	85
86	3.3V	NC	86
87	3.3V	NC	87
88	3.3V	NC	88
89	3.3V	NC	89
90	3.3V	NC	90
91	3.3V	NC	91
92	3.3V	NC	92
93	3.3V	NC	93
94	3.3V	NC	94
95	3.3V	NC	95
96	3.3V	NC	96
97	3.3V	NC	97
98	3.3V	NC	98
99	3.3V	NC	99
100	3.3V	NC	100
101	3.3V	NC	101
102	3.3V	NC	102
103	3.3V	NC	103
104	3.3V	NC	104
105	3.3V	NC	105
106	3.3V	NC	106
107	3.3V	NC	107
108	3.3V	NC	108
109	3.3V	NC	109
110	3.3V	NC	110
111	3.3V	NC	111
112	3.3V	NC	112
113	3.3V	NC	113
114	3.3V	NC	114
115	3.3V	NC	115
116	3.3V	NC	116
117	3.3V	NC	117
118	3.3V	NC	118
119	3.3V	NC	119
120	3.3V	NC	120
121	3.3V	NC	121
122	3.3V	NC	122
123	3.3V	NC	123
124	3.3V	NC	124
125	3.3V	NC	125
126	3.3V	NC	126
127	3.3V	NC	127
128	3.3V	NC	128
129	3.3V	NC	129
130	3.3V	NC	130
131	3.3V	NC	131
132	3.3V	NC	132
133	3.3V	NC	133
134	3.3V	NC	134
135	3.3V	NC	135
136	3.3V	NC	136
137	3.3V	NC	137
138	3.3V	NC	138
139	3.3V	NC	139
140	3.3V	NC	140
141	3.3V	NC	141
142	3.3V	NC	142
143	3.3V	NC	143
144	3.3V	NC	144
145	3.3V	NC	145
146	3.3V	NC	146
147	3.3V	NC	147
148	3.3V	NC	148
149	3.3V	NC	149
150	3.3V	NC	150
151	3.3V	NC	151
152	3.3V	NC	152
153	3.3V	NC	153
154	3.3V	NC	154
155	3.3V	NC	155
156	3.3V	NC	156
157	3.3V	NC	157
158	3.3V	NC	158
159	3.3V	NC	159
160	3.3V	NC	160
161	3.3V	NC	161
162	3.3V	NC	162
163	3.3V	NC	163
164	3.3V	NC	164
165	3.3V	NC	165
166	3.3V	NC	166
167	3.3V	NC	167
168	3.3V	NC	168
169	3.3V	NC	169
170	3.3V	NC	170
171	3.3V	NC	171
172	3.3V	NC	172
173	3.3V	NC	173
174	3.3V	NC	174
175	3.3V	NC	175
176	3.3V	NC	176
177	3.3V	NC	177
178	3.3V	NC	178
179	3.3V	NC	179
180	3.3V	NC	180
181	3.3V	NC	181
182	3.3V	NC	182
183	3.3V	NC	183
184	3.3V	NC	184
185	3.3V	NC	185
186	3.3V	NC	186
187	3.3V	NC	187
188	3.3V	NC	188
189	3.3V	NC	189
190	3.3V	NC	190
191	3.3V	NC	191
192	3.3V	NC	192
193	3.3V	NC	193
194	3.3V	NC	194
195	3.3V	NC	195
196	3.3V	NC	196
197	3.3V	NC	197
198	3.3V	NC	198
199	3.3V	NC	199
200	3.3V	NC	200

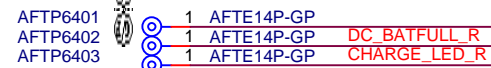
LBB-2

Layout impact:
R6410 keep 0-ohm

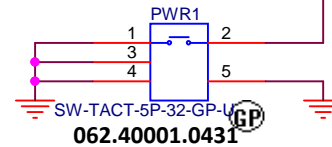
Dual LED



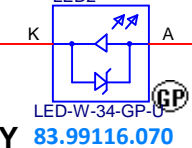
Near LED1



Power Button



Power LED



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Title

LED/BTN/POWER BTN

Size

Document Number

Bumblebee-2

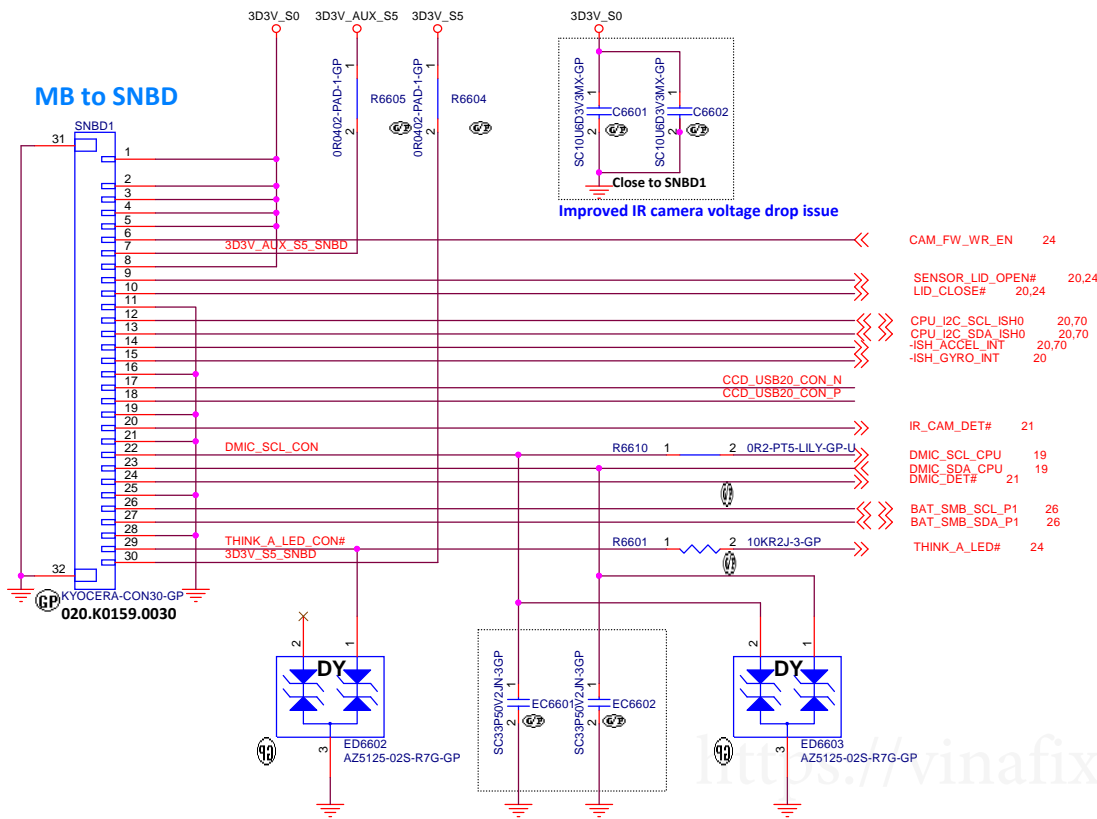
Rev

1

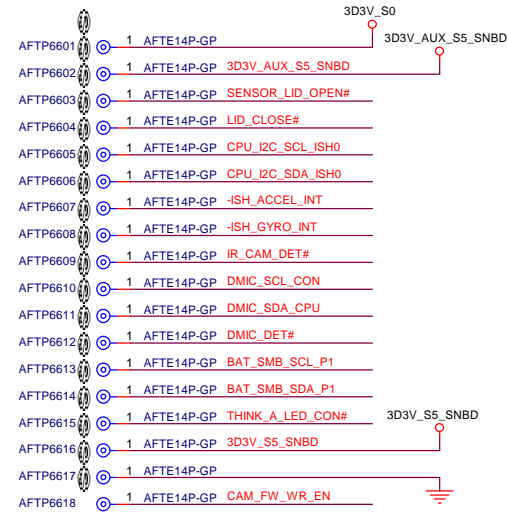
Date: Tuesday, March 03, 2020

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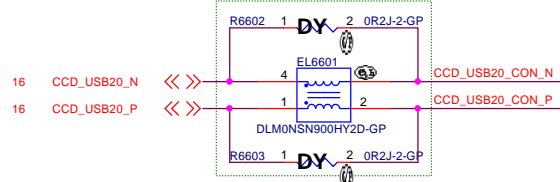
MB to SNBD



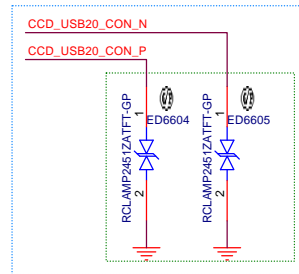
Near SNBD1 (Sensor board)



Co-Layout



LBB-2 Layout impact:
WWAN antenna interference, change to small size



For CAMERA ESD failed solution

LBB-2

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Title
IO BOARD CONN

Size A3 Document Number **Bumblebee-2** Rev **1**

Date: Tuesday, March 03, 2020 Sheet 66 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title **SENSOR (RSVD)**

Size
A4

Document Number

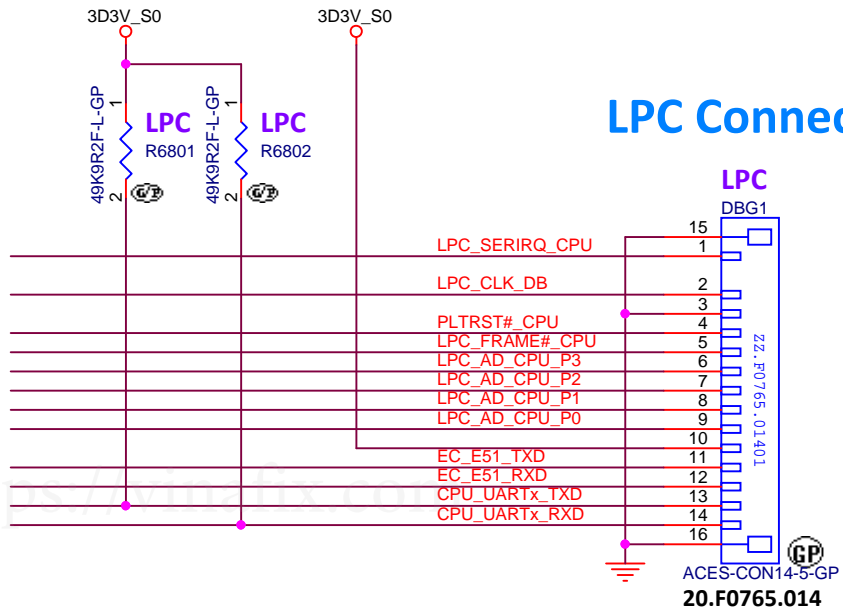
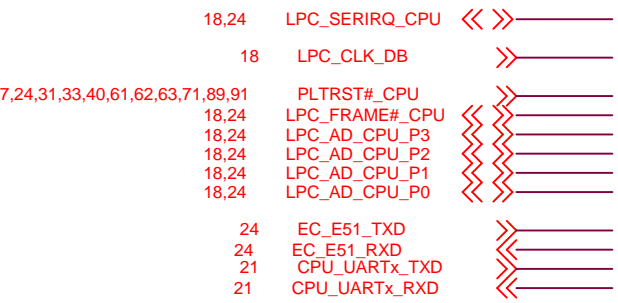
Bumblebee-2

Rev
1

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Main Func = Debug

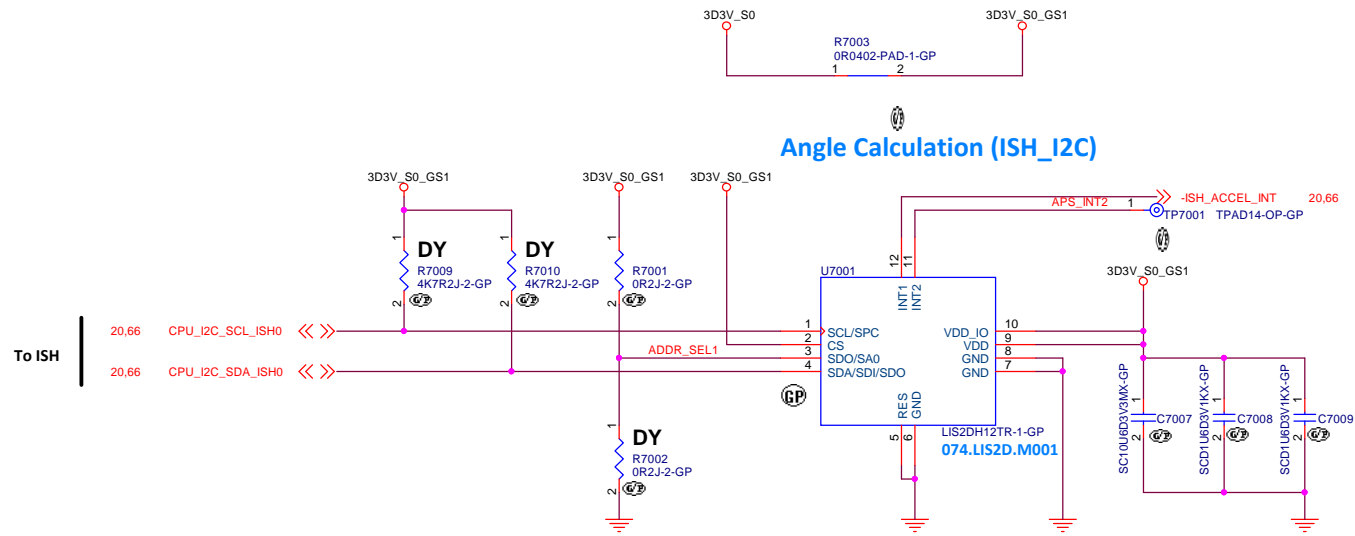


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Title <div>SENSOR (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Bumblebee-2</div>	Rev <div>1</div>
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TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address
LIS2DH12TR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7002): Tri-axis Digital Accelerometer

P/N	ADDR_SEL2	Address
BMA280	H L	32h(W) & 33h(R) 30h(W) & 31h(R)
LIS2DWLTR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor(U7002)

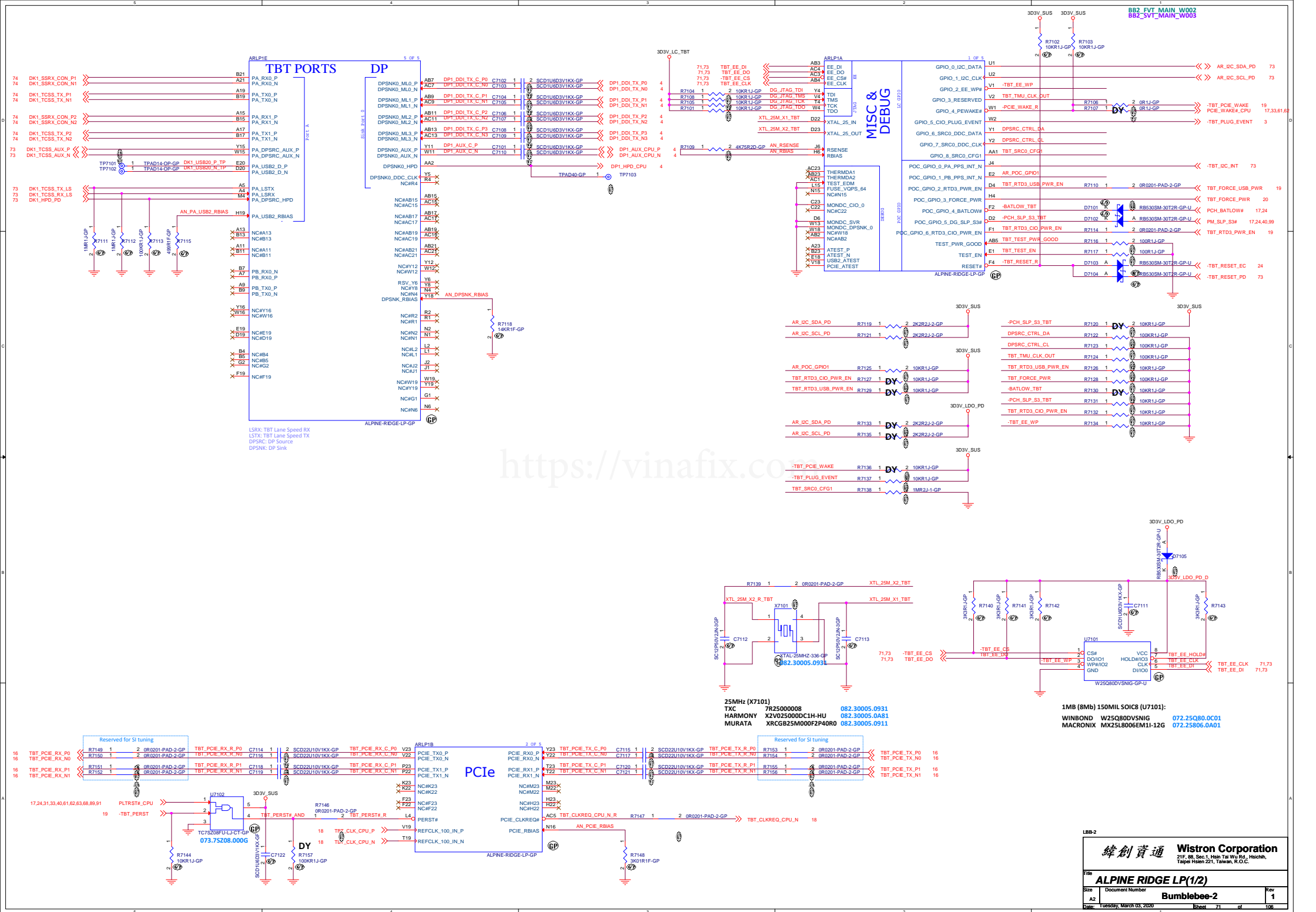
Vendor	P/N	Wistron P/N
BOSCH	BMA280	074.00280.0AB0
ST	LIS2DWLTR	074.LIS2D.00B0

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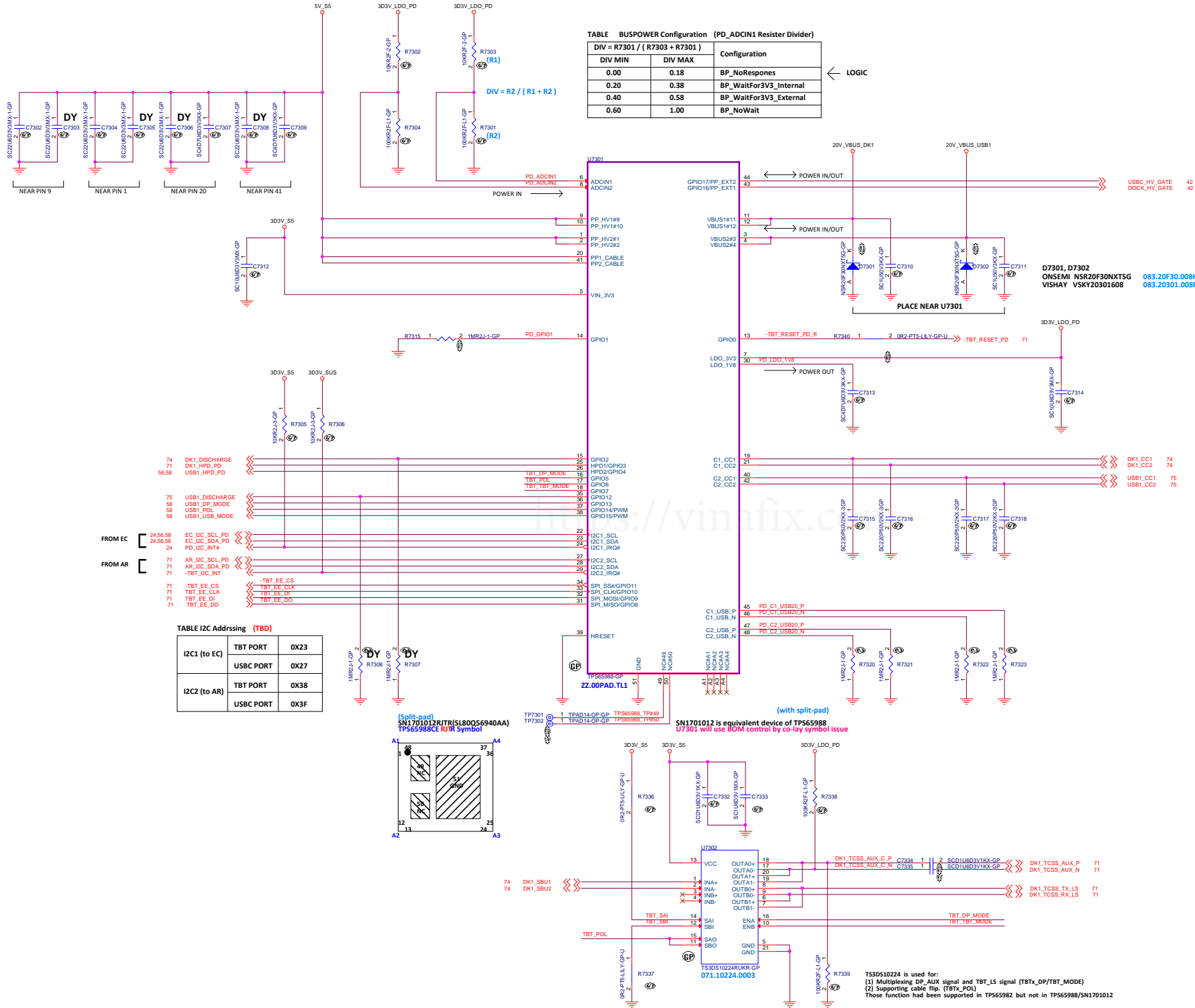
Title **SENSOR (G-SENSOR)**Size A3 Document Number **Bumblebee-2** Rev **1**

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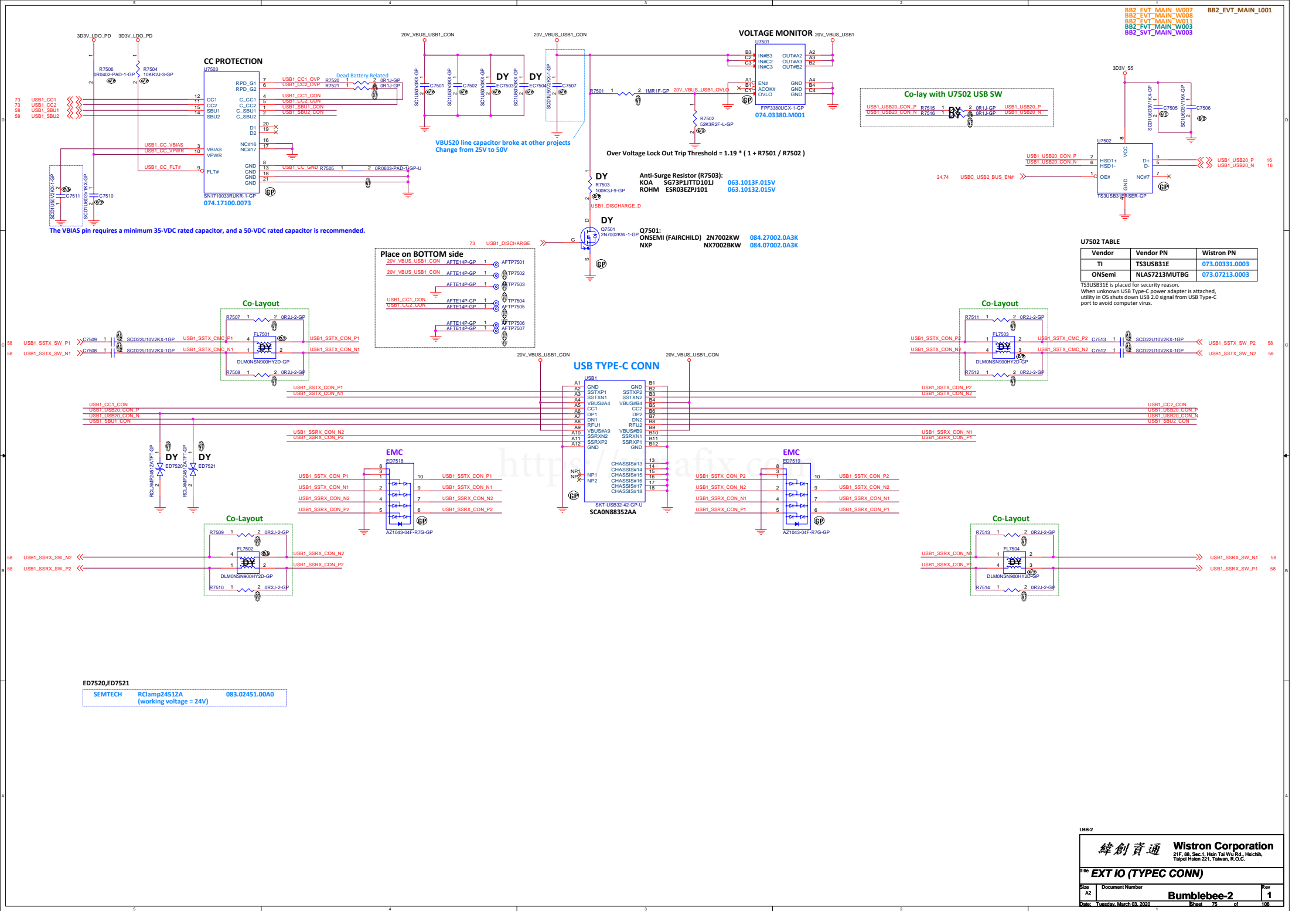


DIV = R7301 / (R7303 + R7301)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponses
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC



TS3DS10224 is used for:
 (1) Multiplexing DP_AUX signal and TBT_LS signal (TBTx_DP/TBT_MODE)
 (2) Supporting cable flip. (TBTx_POL)
 Those function had been supported in TPS65982 but not in TPS65988/SN1701012



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Title GPU (RSVD)		
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Title GPU (RSVD)		
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Title GPU (RSVD)		
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Title GPU (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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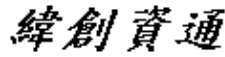
LBB-2

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title GPU (RSVD)		
Size A4	Document Number Bumblebee-2	Rev 1
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Title GPU (RSVD)		
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Title GPU (RSVD)		
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Title <div>GPU (RSVD)</div>		
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Title <div>GPU (RSVD)</div>		
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Title <div>GPU (RSVD)</div>		
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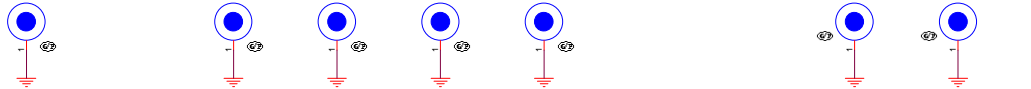
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<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>GPU (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Bumblebee-2</div>	Rev <div>1</div>
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Screw Pad

H1 HOLET237B14X240R103-S1
Special GND HOLE for Layout



H11 HOLET233B158R142-GP
ZZ.00PAD.VK1

H12 HOLET233B158R142-GP
ZZ.00PAD.VK1

Stand Off

H20 STFT7236B142R128H43-3-GP
34.4L0V1.101

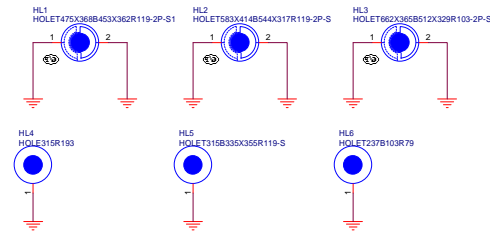


Spring Plate

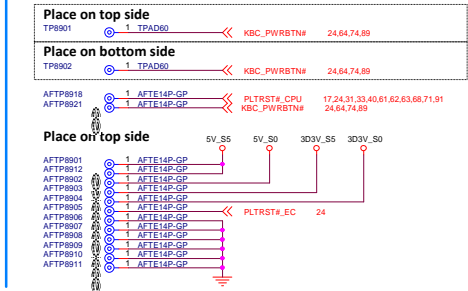
SPR1 SPRING-31-GP-U
34.49U24.001

SPR2 SPRING-64-GP
34.4H602.001

Special GND HOLE for Layout

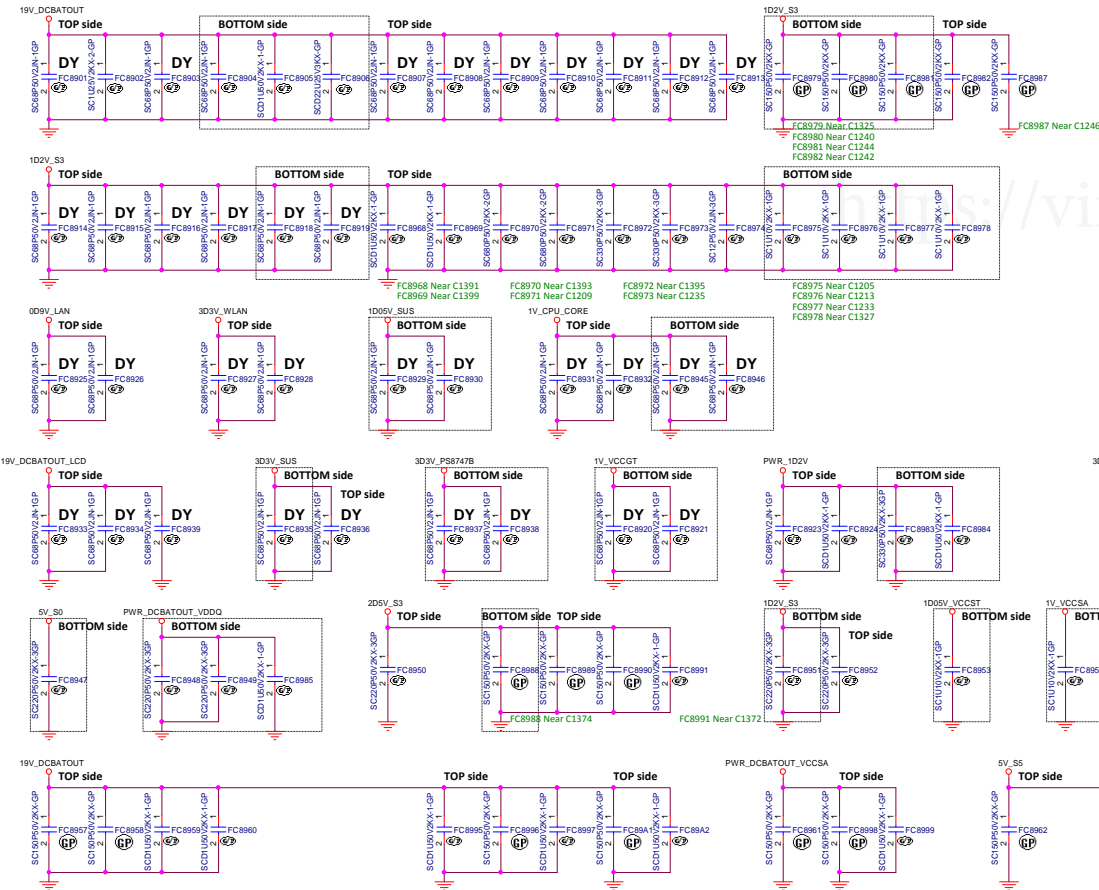


Test Point

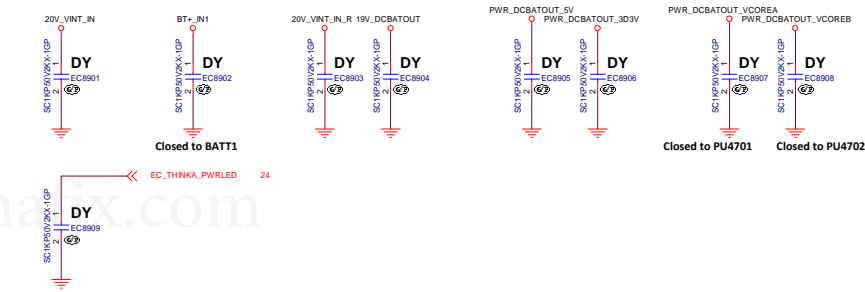


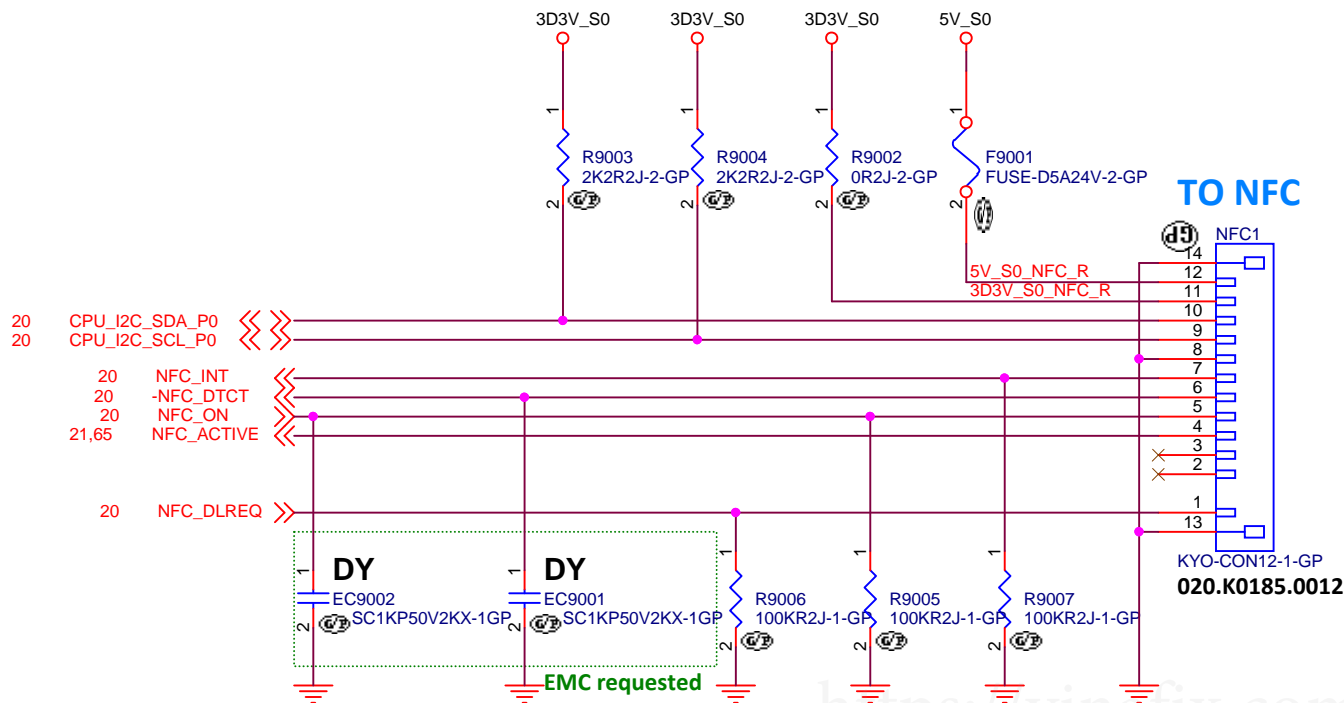
BB2 EVT_MAIN_W020
BB2_SIT_MAIN_W005
BB2_SIT_MAIN_W007V2
BB2_SIT_MAIN_W008V2
BB2_SIT_MAIN_W009
BB2_SIT_MAIN_W011
BB2_SIT_MAIN_W004

RF CAPS

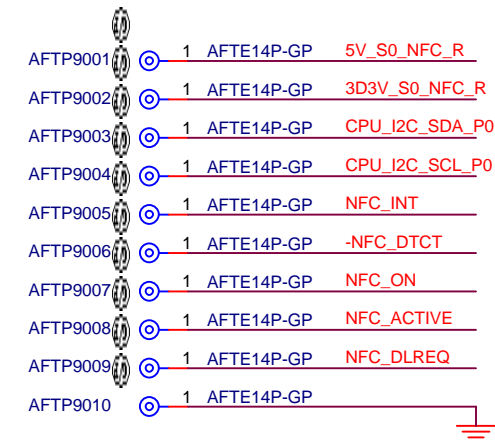


EMI CAPS





Near NFC1 (NFC)



Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V - 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P = power supply, G = ground, I = input, O = output, I/O = input/output

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INT IO (NFC)

Size
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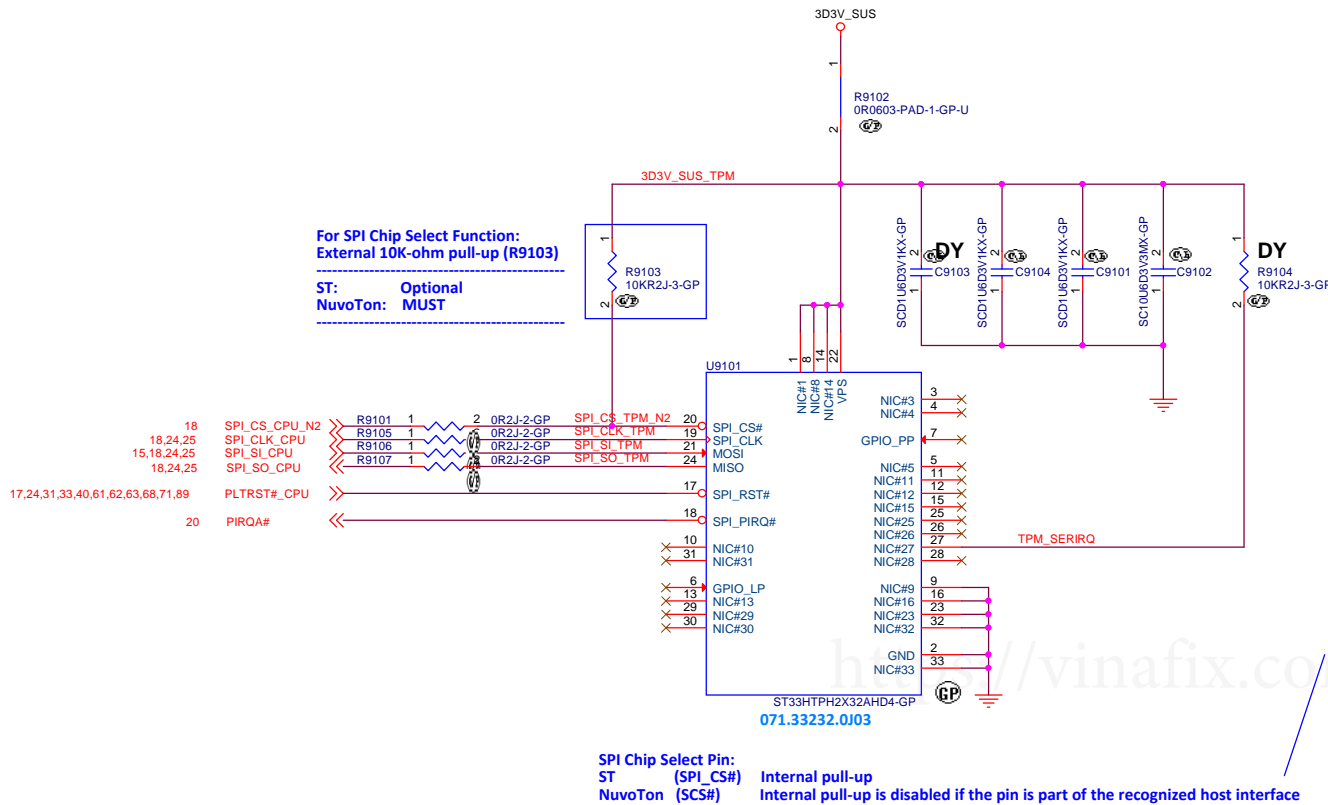
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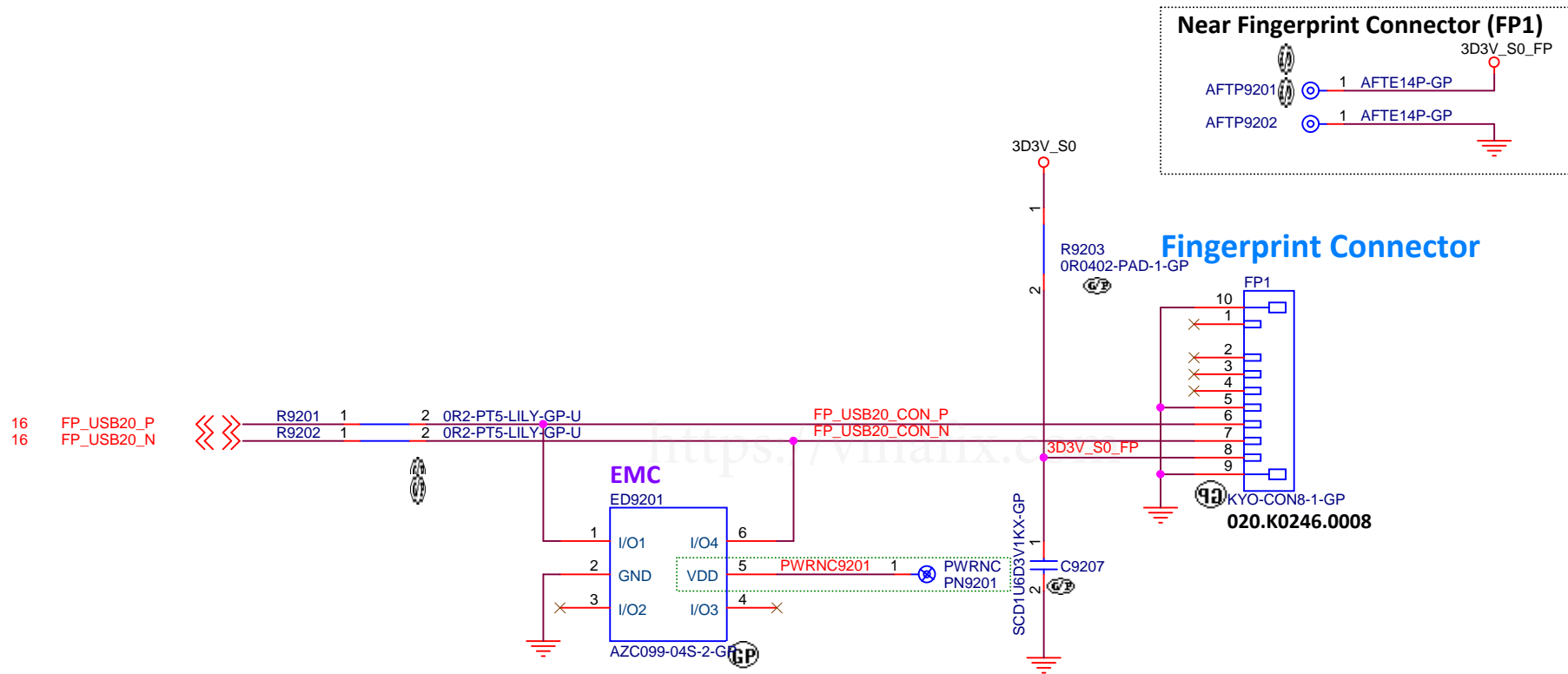


TABLE

	TPM2.0	EVT		FVT		SIT and beyond	
1st	ST	ST33HTPH2E32AHC0	071.33232.0H03	ST33HTPH2X32AHC4	071.33232.0I03	ST33HTPH2X32AHD4	071.33232.0J03
2nd	NuvoTon	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03

TABLE

TABLE		071.00750.0D03	071.33232.0J03	— 071-89670-0103 —
Pin No	TCG PTP Spec(V38)	NuvoTon NPCT750LABYX	ST Micro ST33HTPH2X32AHD4	Infineon 5189F70N Q3.0 SW7.63
1	VDD	VSB	NC	VDD
2	GND	NC	GND	GND
3	NC	NC	NC	NC
4	GPIO	GPIO/PP	PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO3	NC	GPIO
7	GPIO	NC	GPIO	PP
8	VDD	VHIO	NC	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	GPIO4	NC	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#	CS#
21	MOSI	MOSI/GPIO7	MOSI	MOSI
22	VDD	VHIO	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO0	NC	NC
30	SCL/GPIO0	SCL/GPIO1	NC	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND



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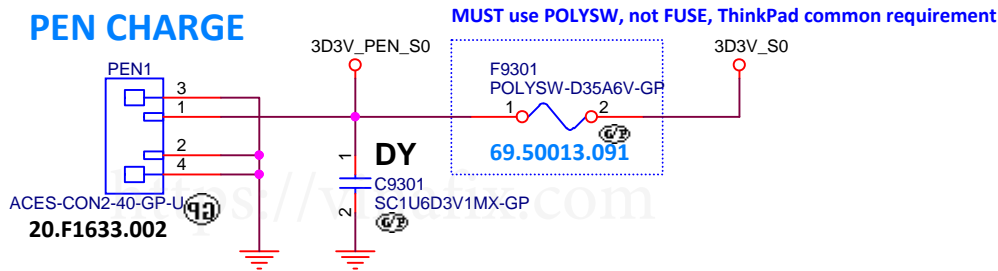
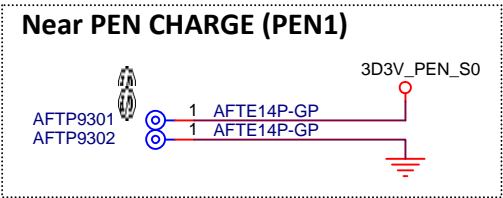
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INT IO (FINGERPRINT)

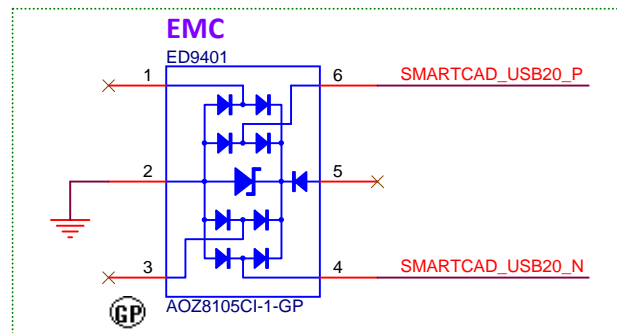
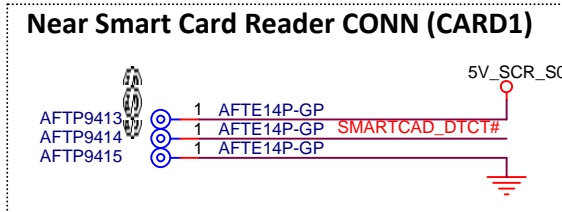
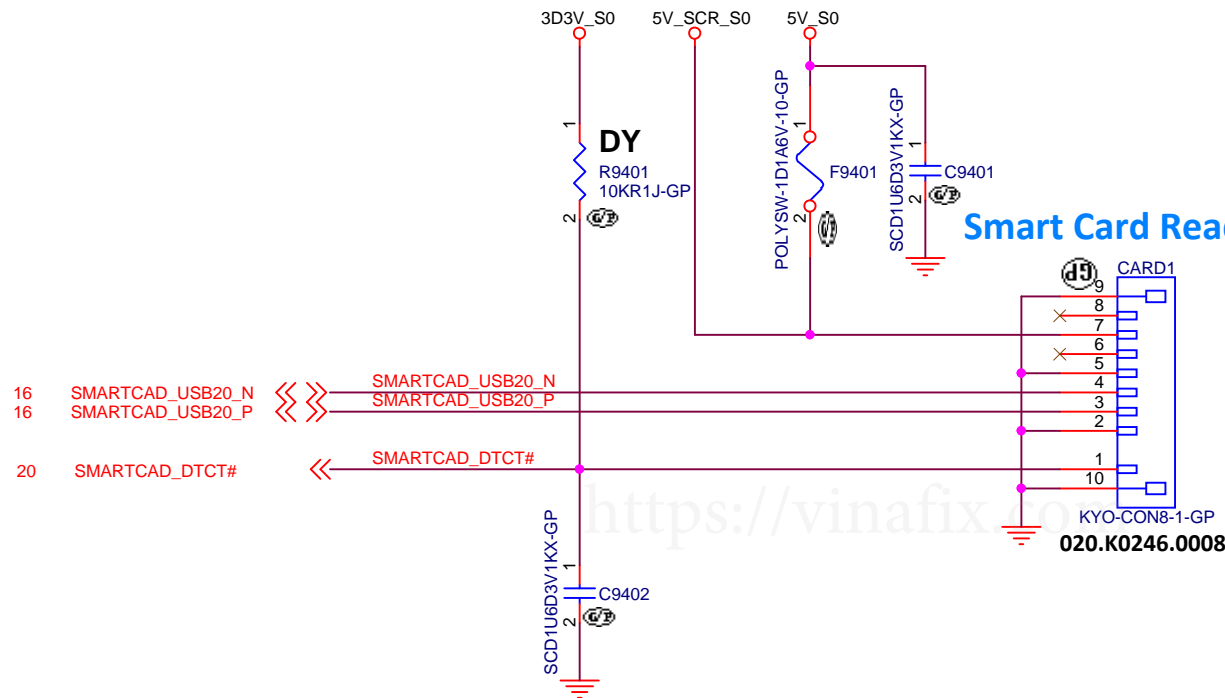
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EXT IO (ACTIVE PEN)					
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>EXT IO (SMART CARD)</p>		
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Title <div>EXT IO (RSVD)</div>		
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Title COMMERCIAL (RSVD)		
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Title COMMERCIAL (RSVD)		
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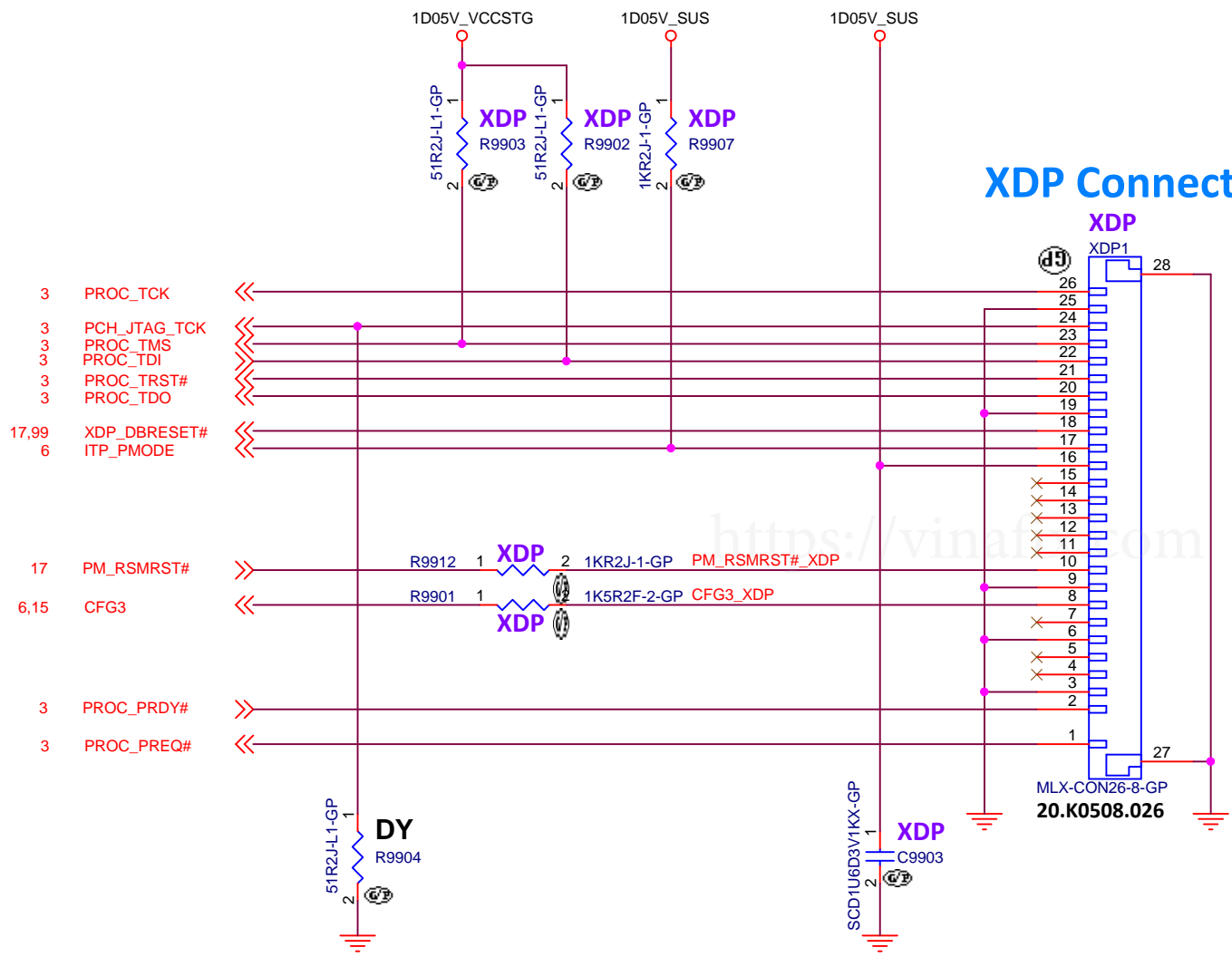
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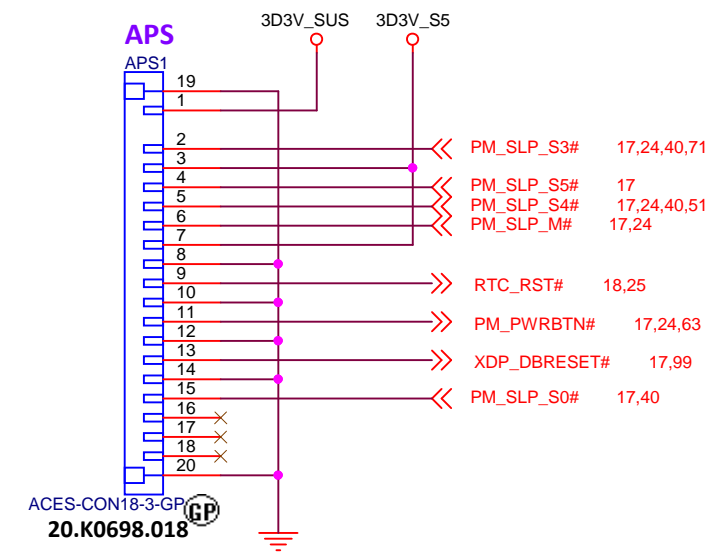
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Title		
COMMERCIAL (RSVD)		
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Main Func = Debug



XDP Connector

APS Connector



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Title DEBUG (XDP/APS)		
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Size <div>A4</div>	Document Number <div>Bumblebee-2</div>
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CHANGE HISTORY

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A4

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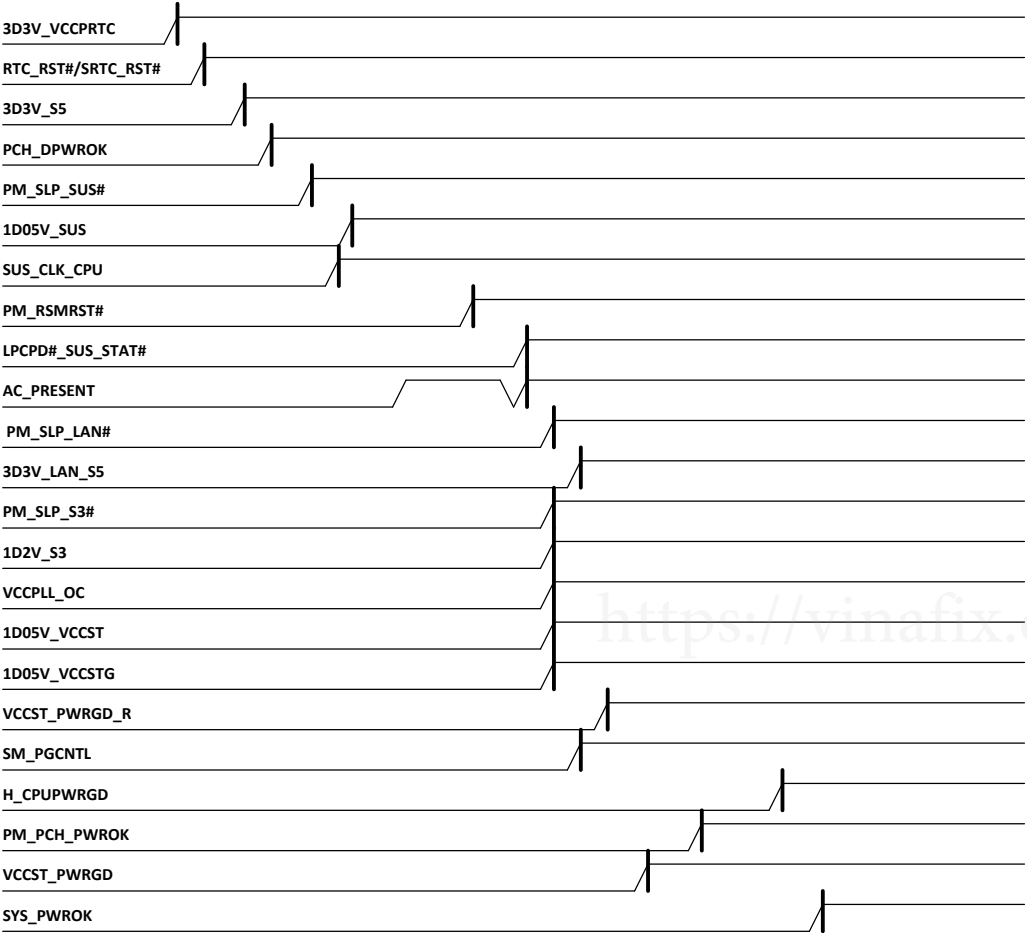
Date: Tuesday, March 03, 2020

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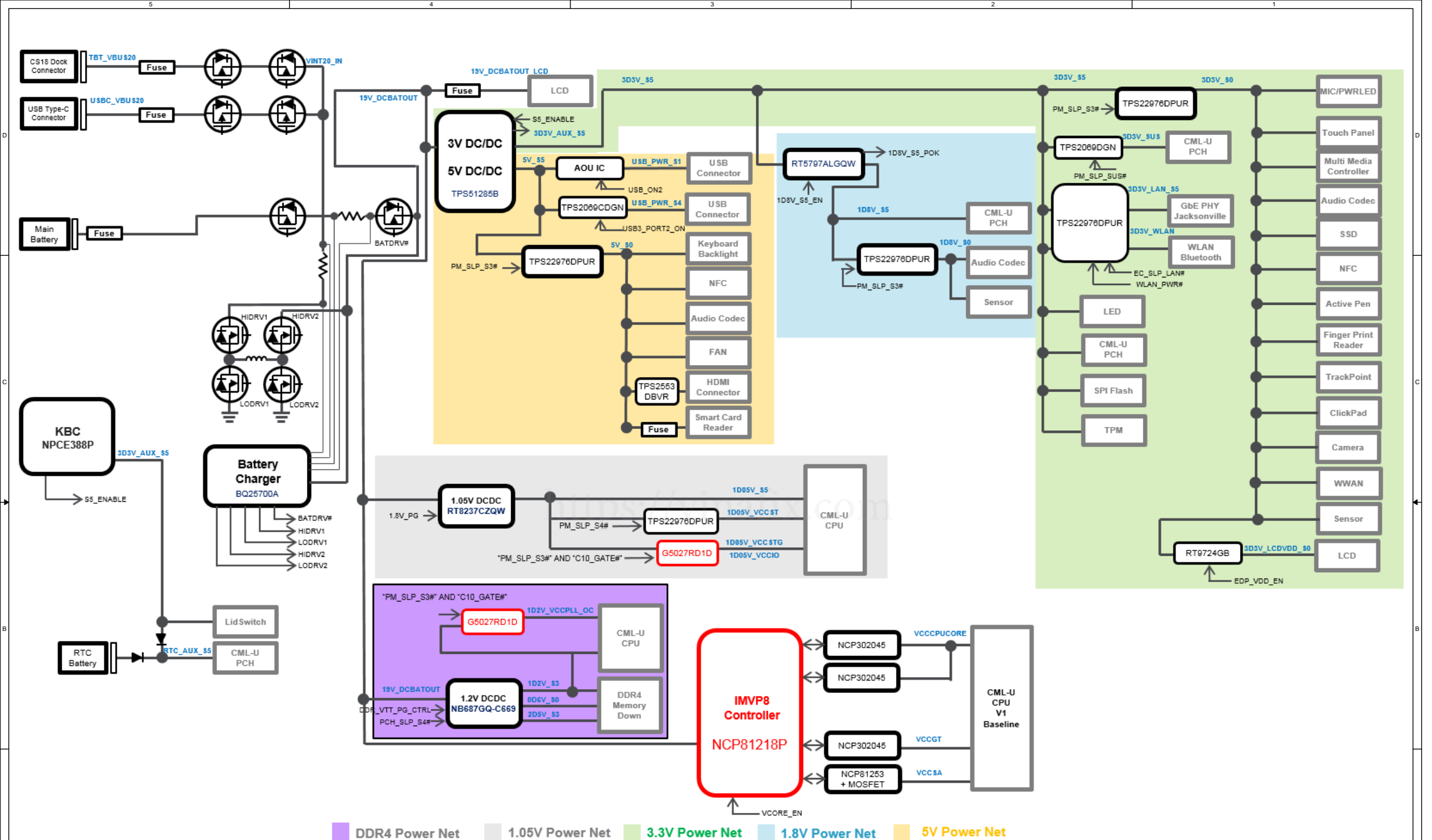
Intel-Power Up Sequence

#607109_CML_U_PDG_Rev1p2_P.629

(AC mode)



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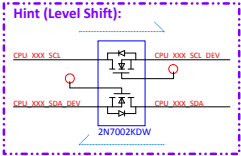
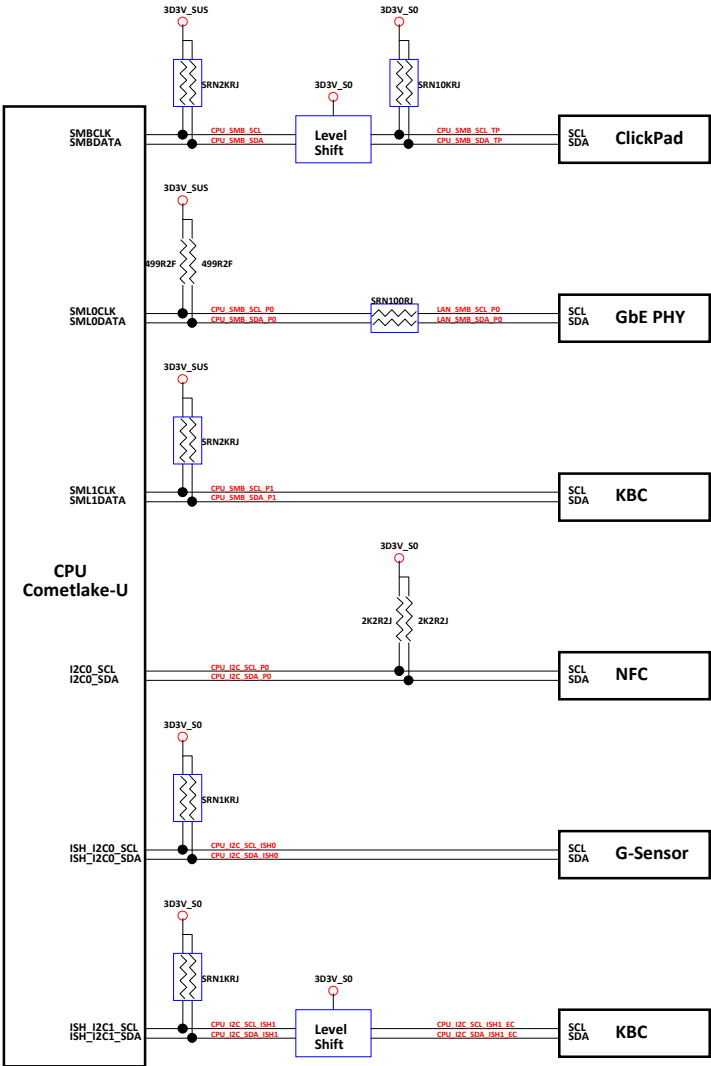
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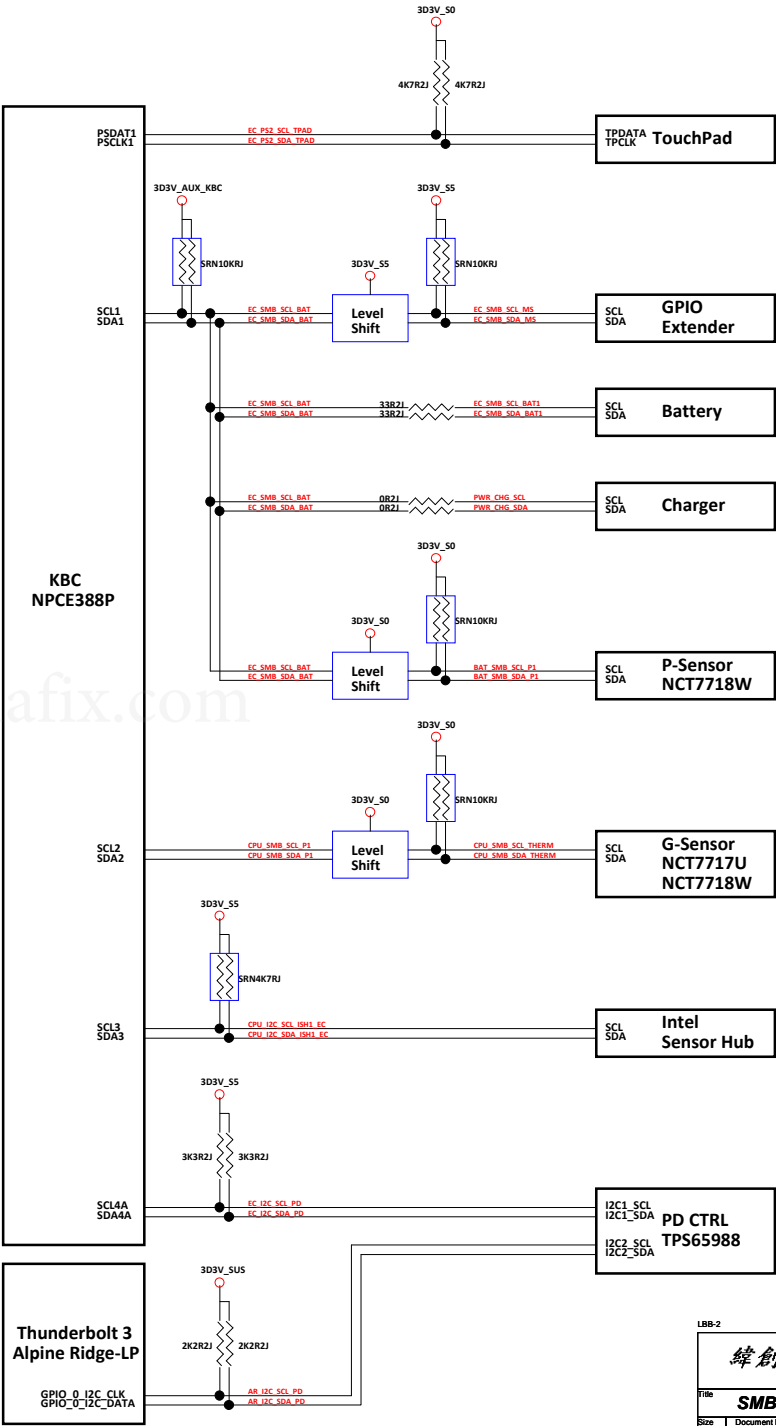
Title **POWER BLOCK DIAGRAM**

Size A3 Document Number **Bumblebee-2** Rev **1**
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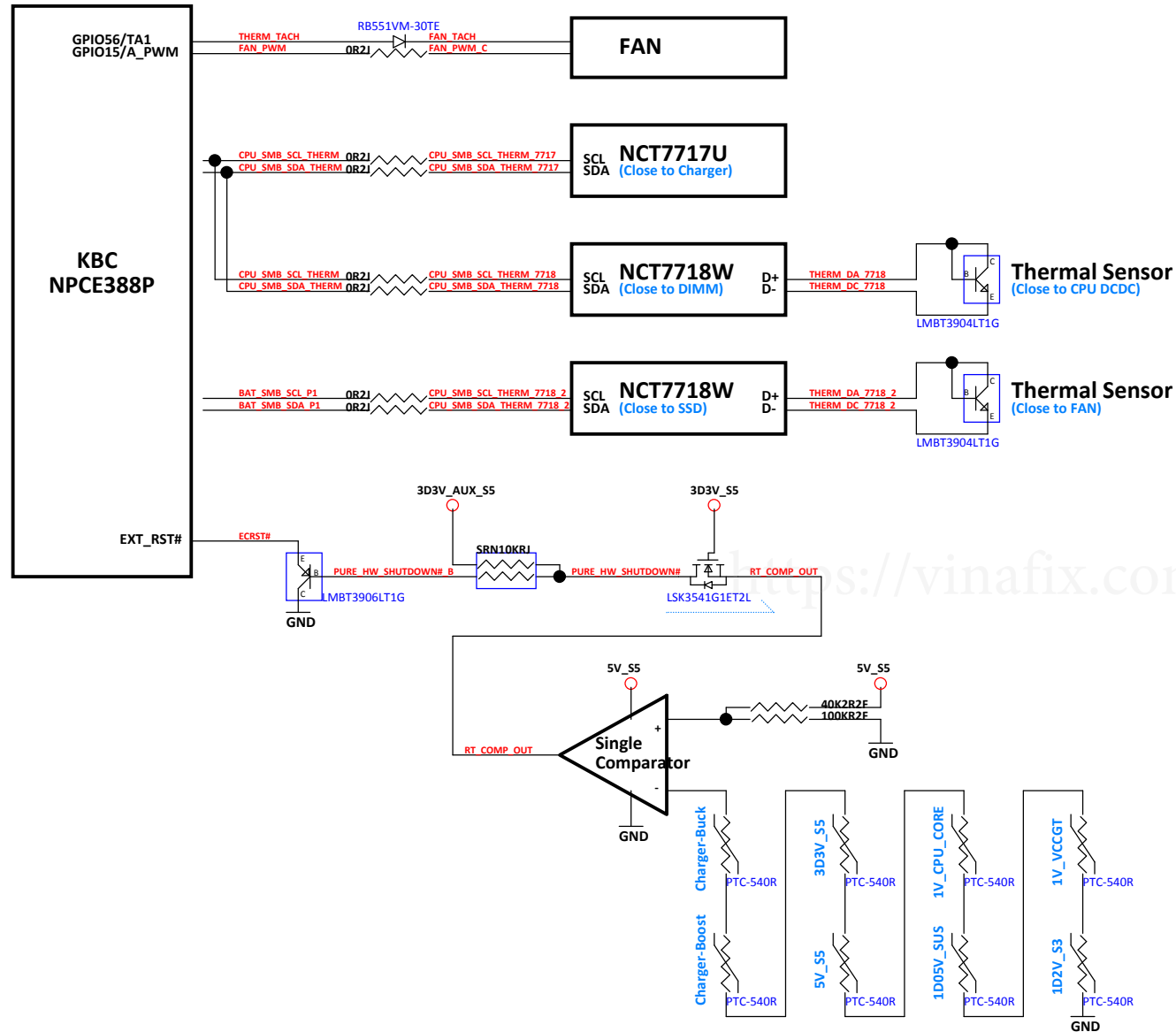
PCH SMBus/I2C Block Diagram



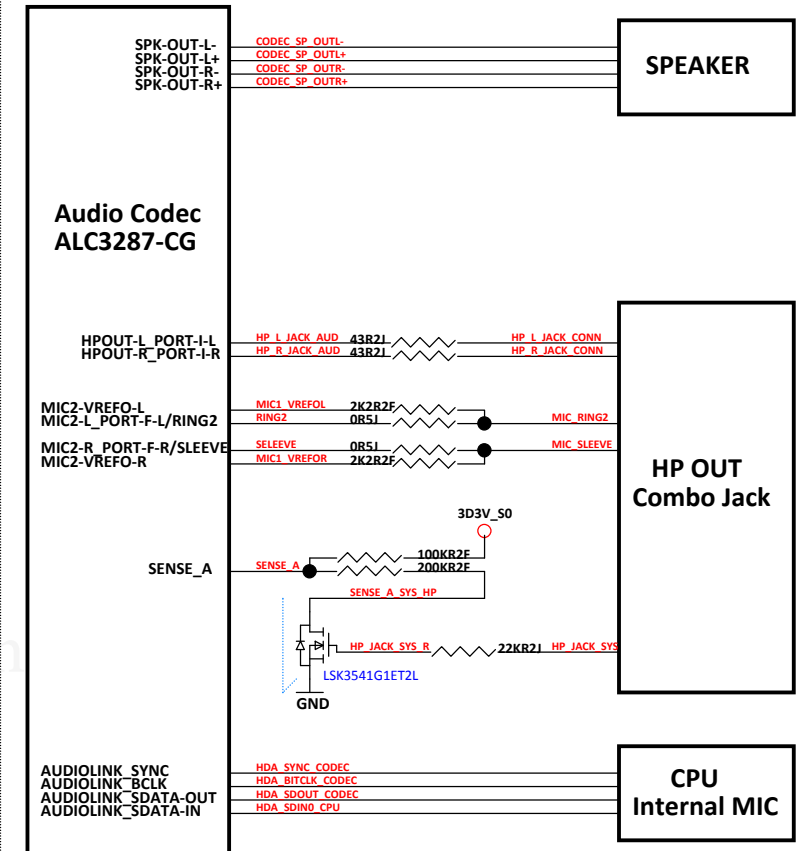
KBC SMBus/I2C Block Diagram

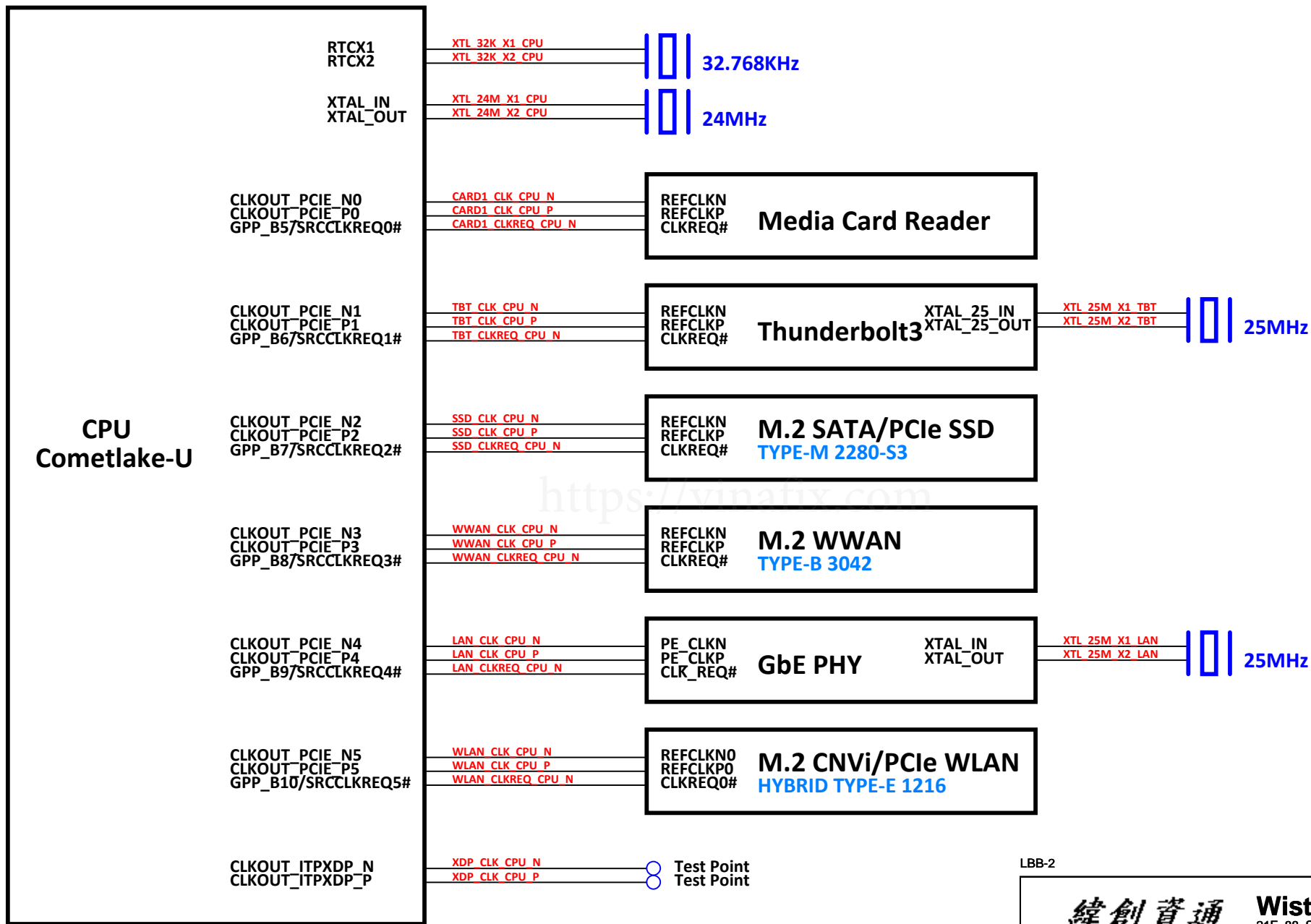


Thermal Block Diagram



Audio Block Diagram





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Title
CLK BLOCK DIAGRAM

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