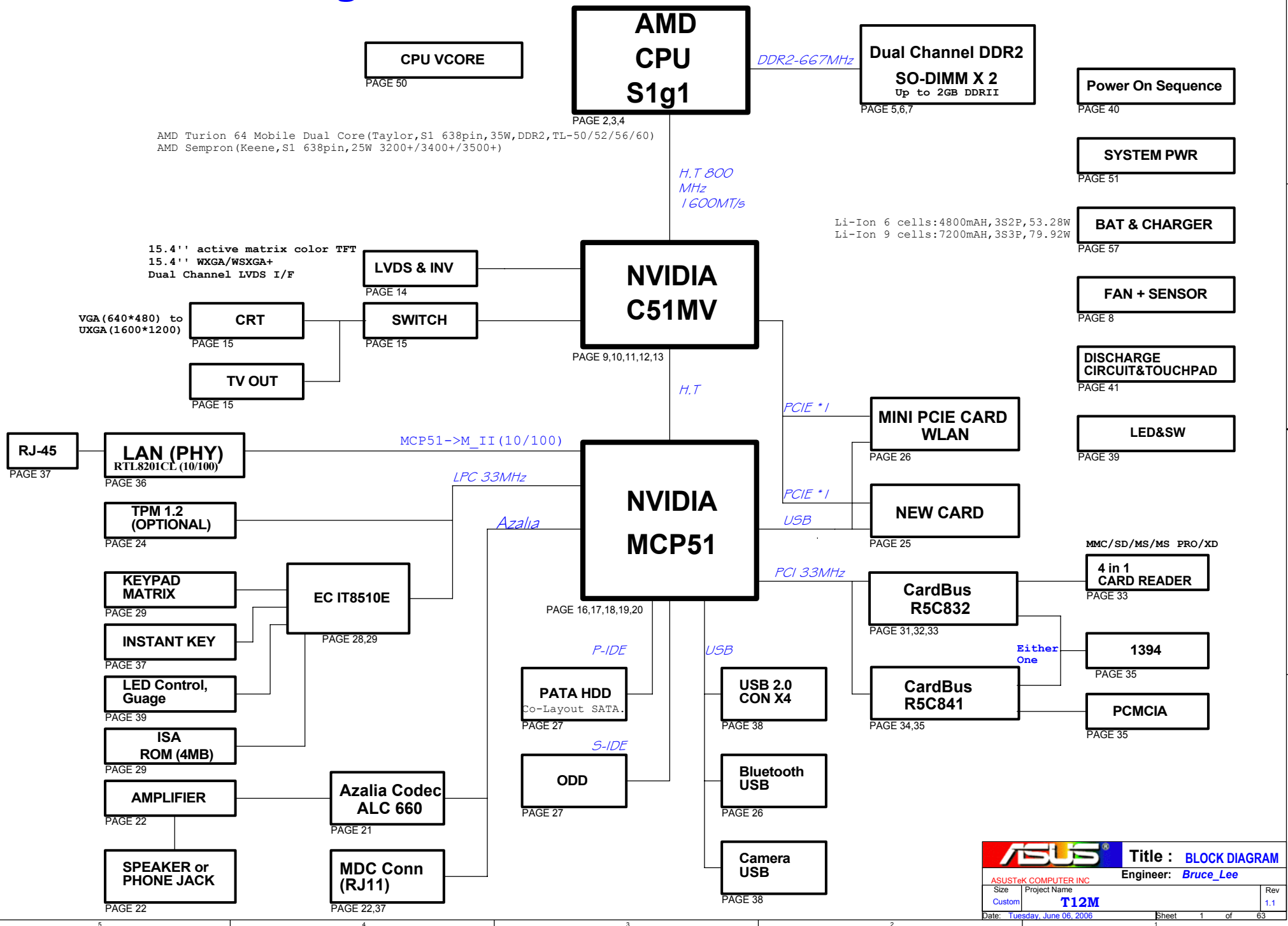
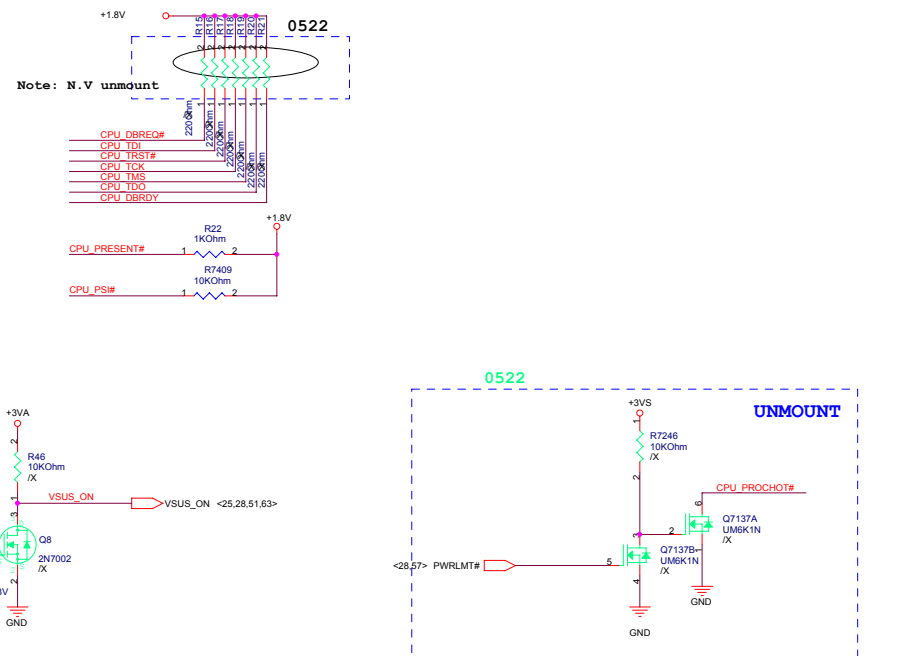
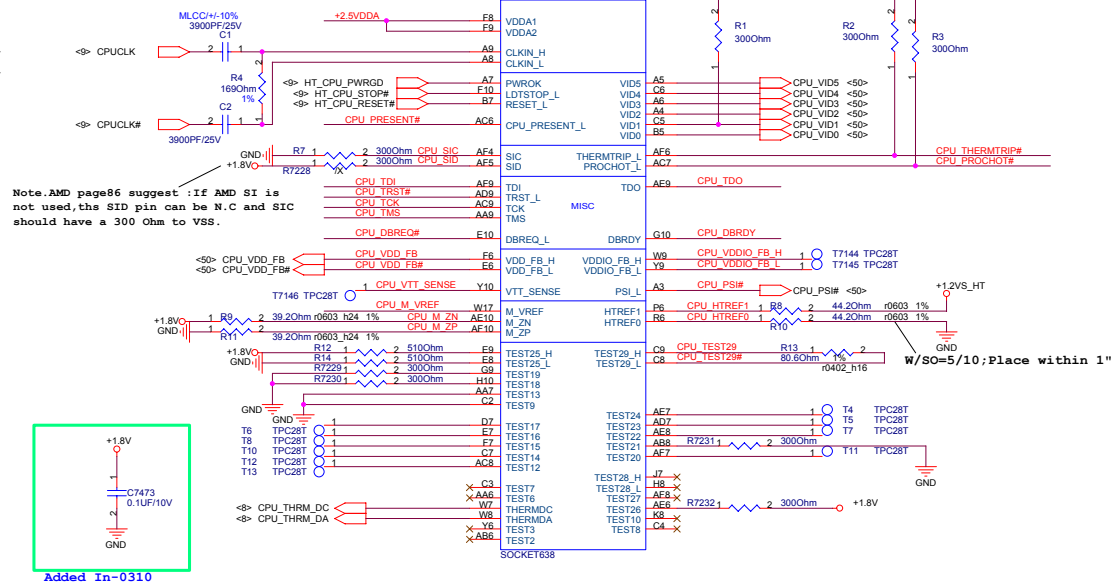
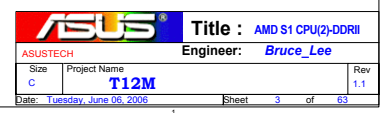
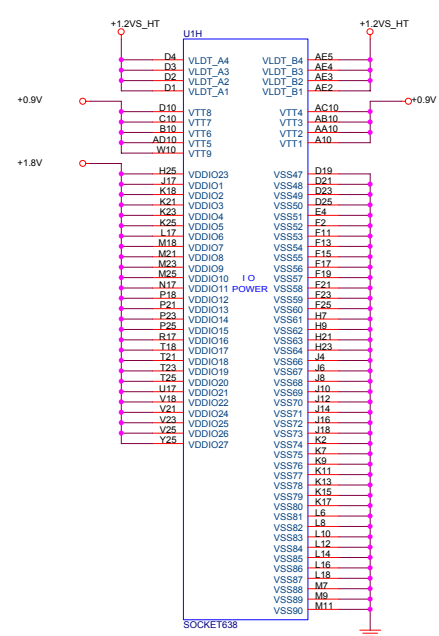
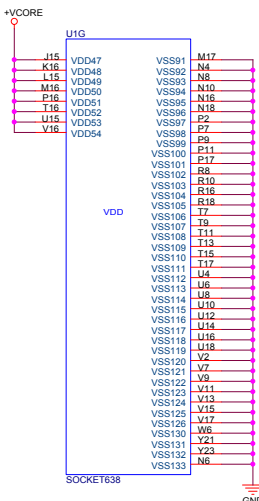
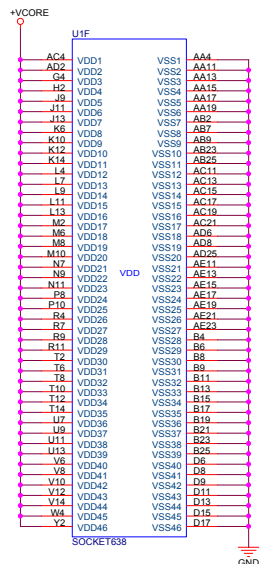


# T12M Block Diagram

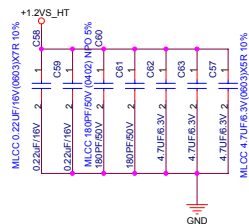
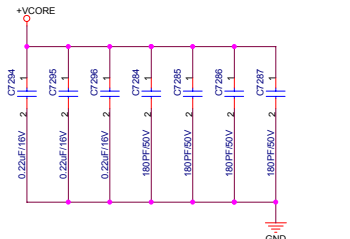
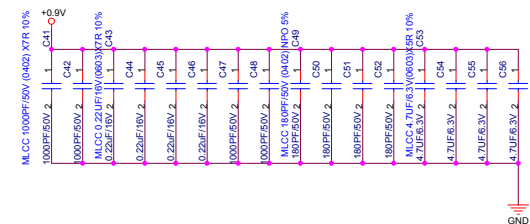
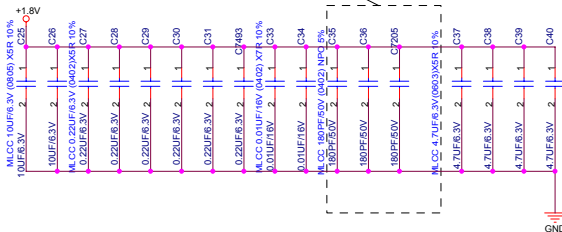
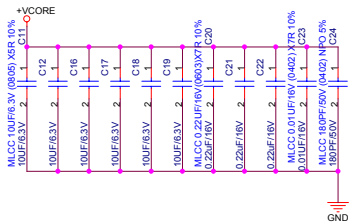




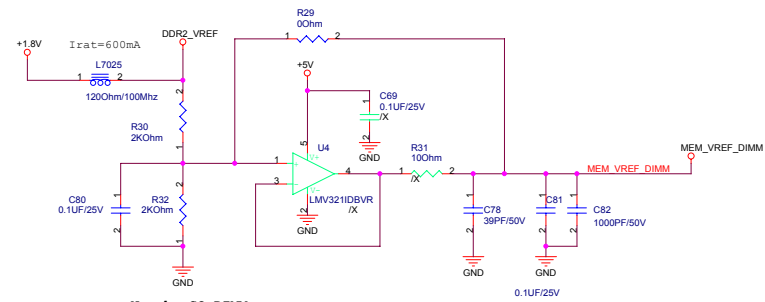
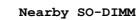




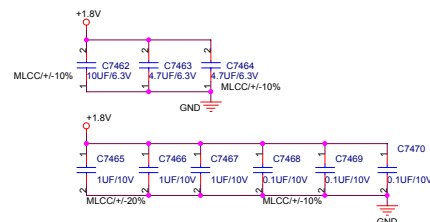
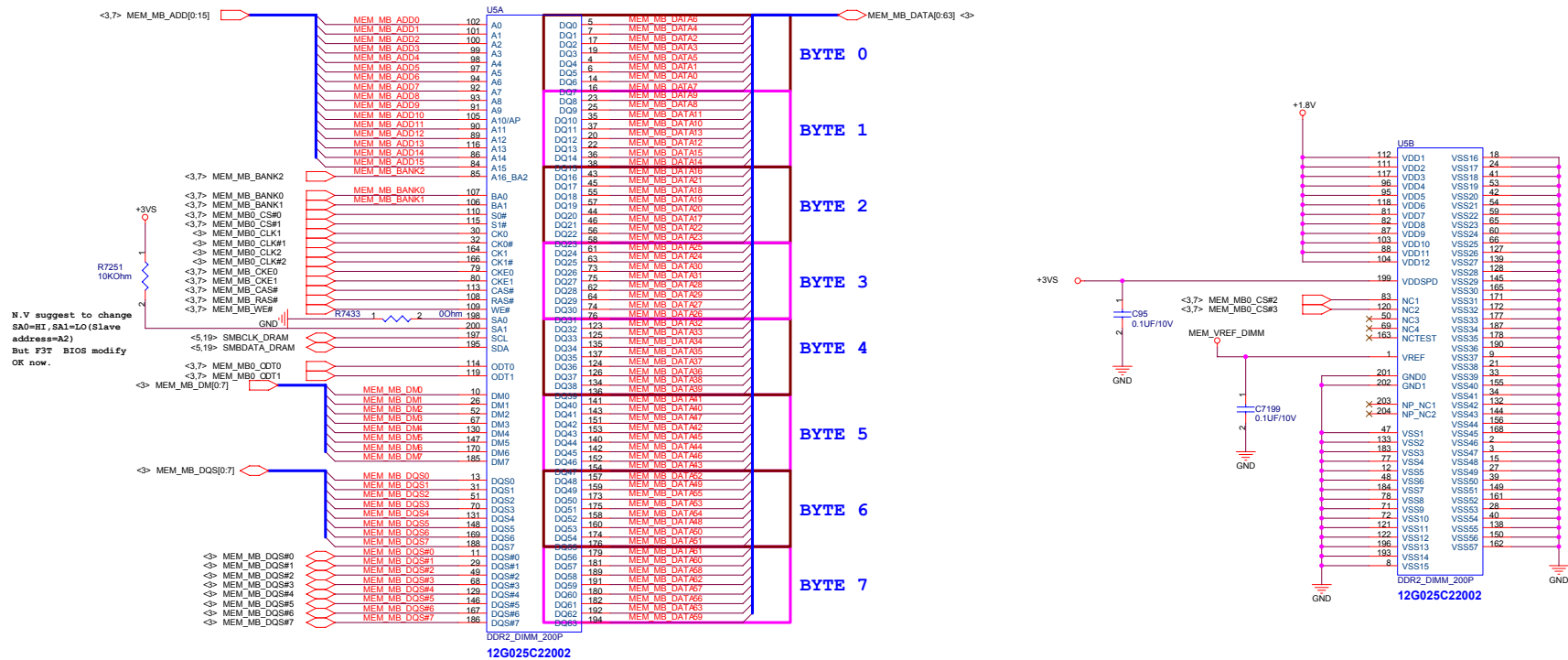
For DDR2 add/cmd refer to split plane.

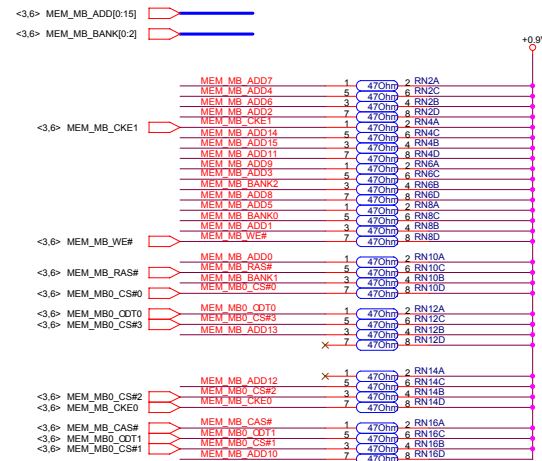
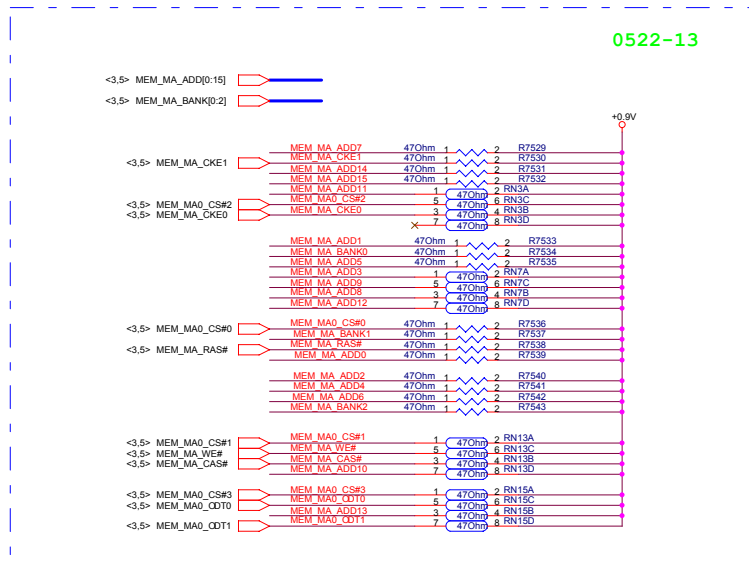


**12G02502200F**

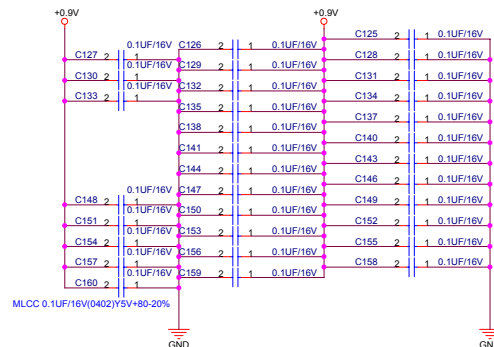


## Reserve Type H=9.2mm

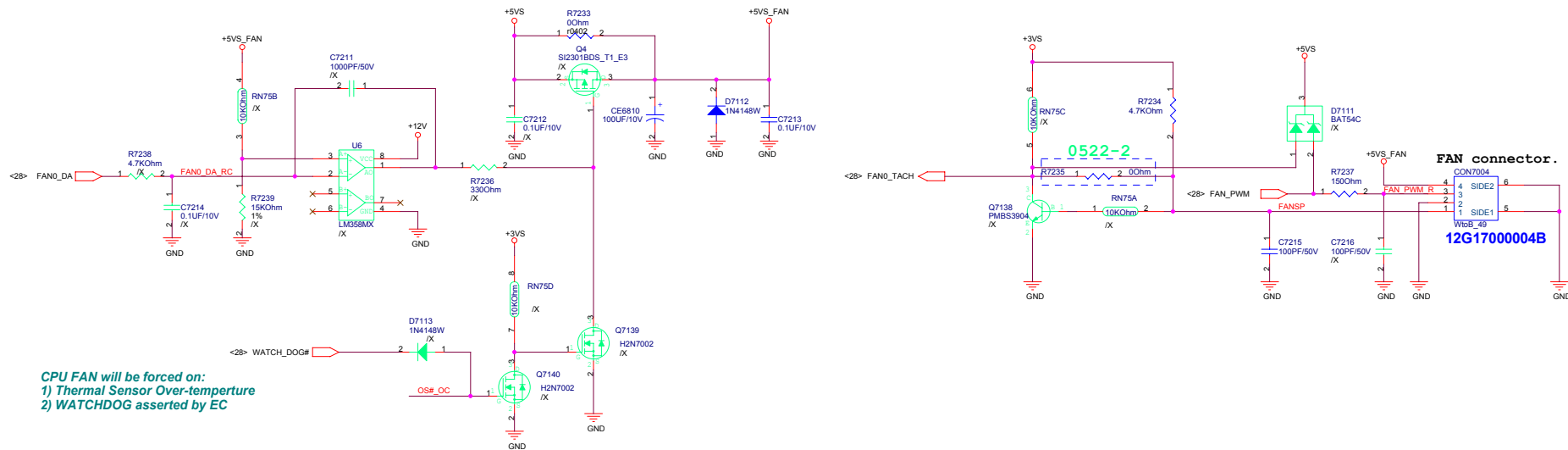




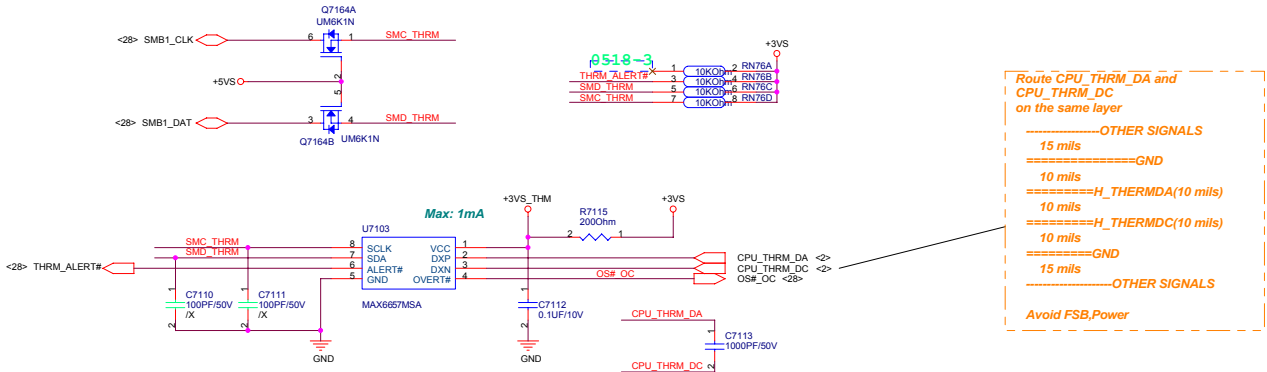
Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9V



# DC FAN control



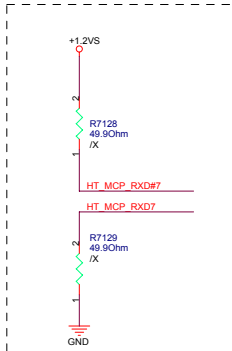
# Thermal Sensor





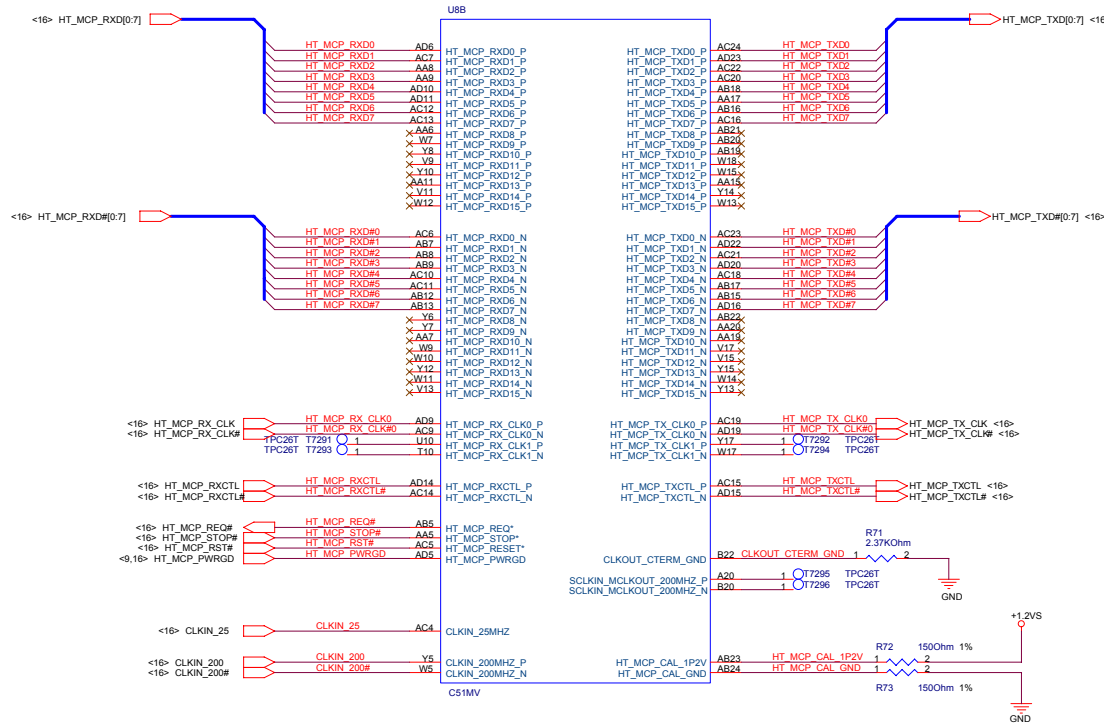


R close to IC within 1500 mils.  
Place these resistors without stubs.



4\*4 H.T link mode if mount R7128 and R7129.

Nvidia suggests to change 8\*8.  
Resisters setting can reference  
design guide chapter12 (Page  
176).

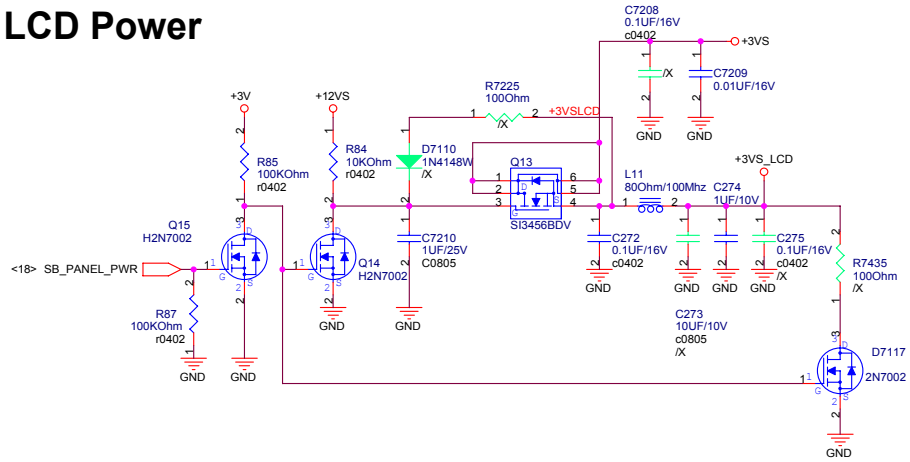




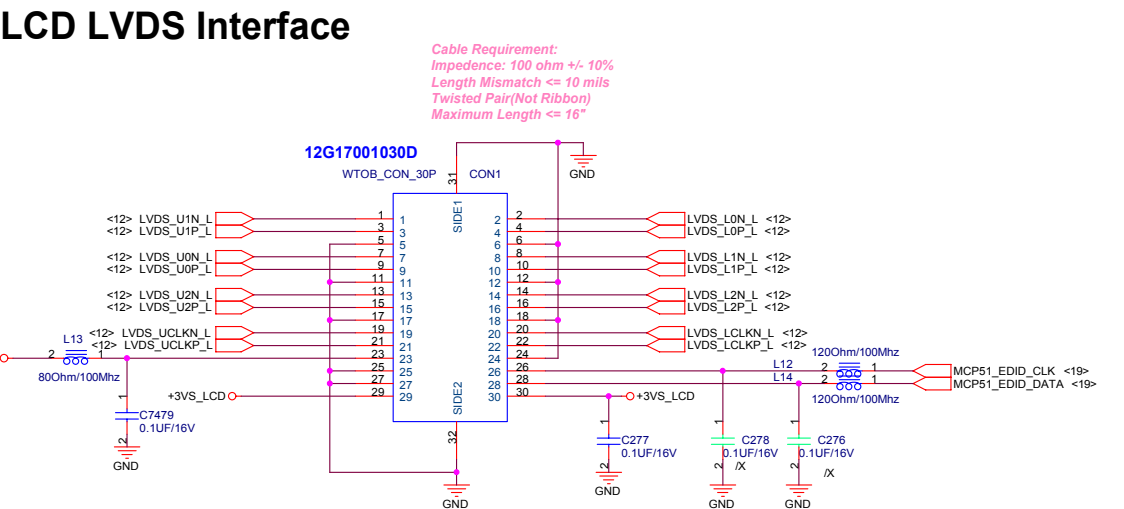




LCD Power



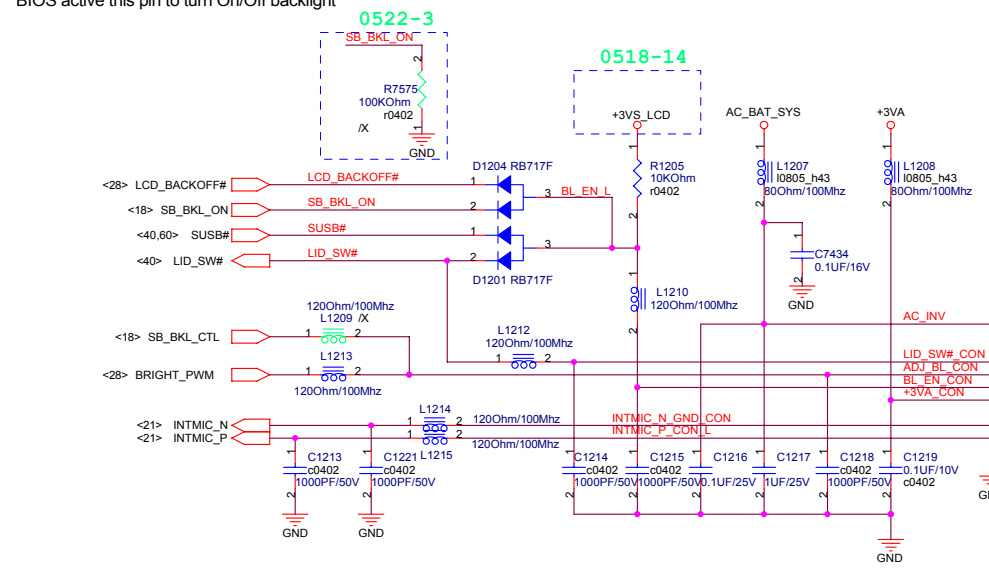
LCD LVDS Interface



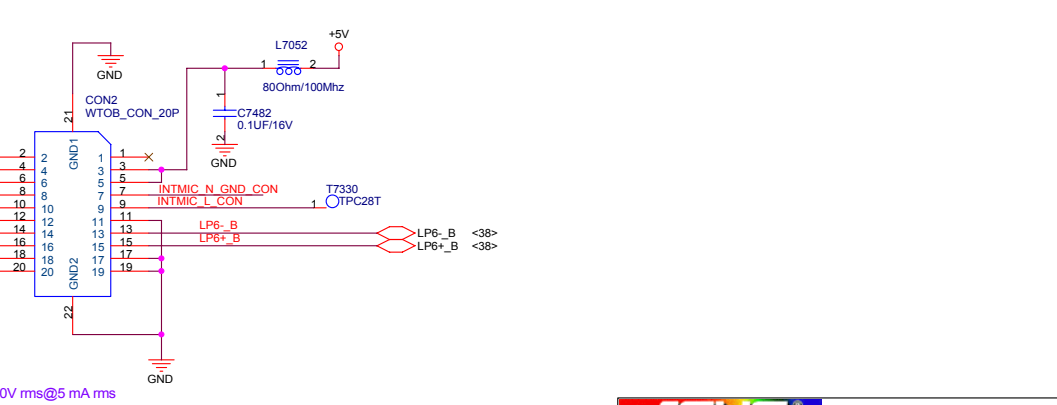
Inverter & Backlight Control

LCD Backlight Control 15.4" WXGA ,1280\*800

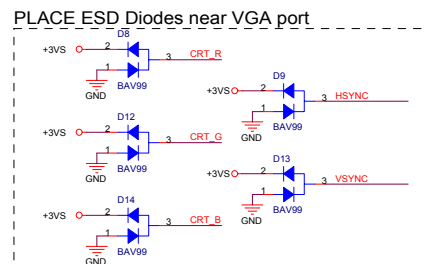
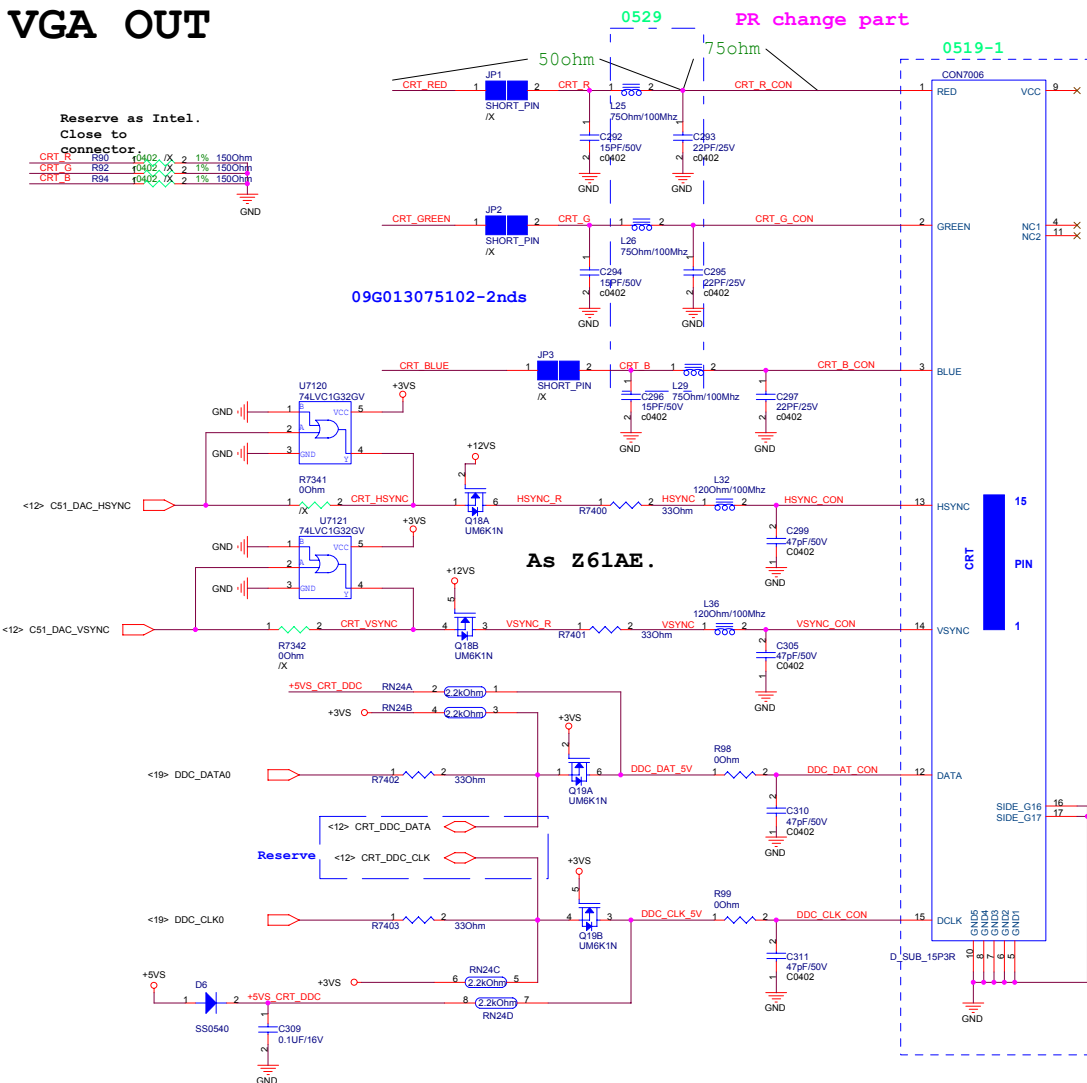
BIOS  
LCD\_BACKOFF#  
When user push "Fn+F7" button  
BIOS active this pin to turn On/Off backlight



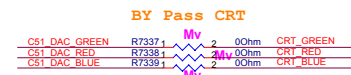
INVERTER Interface



## VGA OUT



## TV-OUT and VGA OUT Switch.



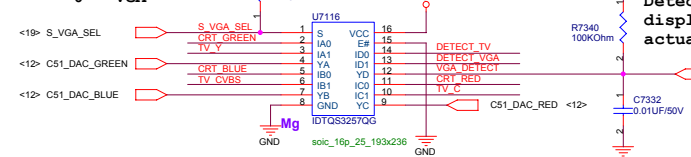
To support monochrome VGA display monitor detection.



Nvidia design guide page 39.

"1" =TV

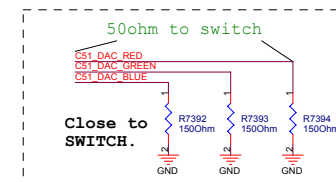
"0" =VGA



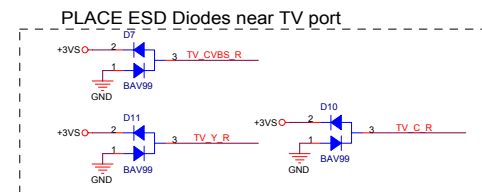
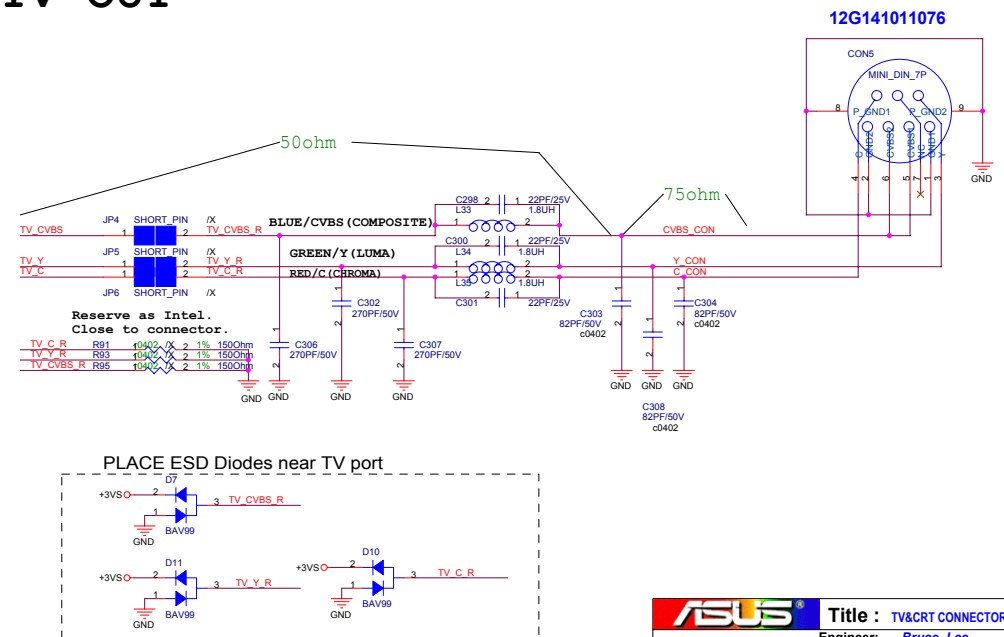
3V  
Used to detect load on the undriven output.

Detect whether a display(VGA or TV) is actually present.

Reference A8N-VM project.



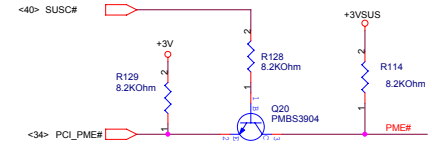
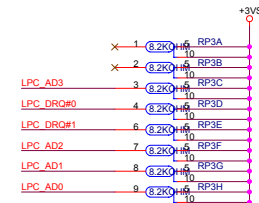
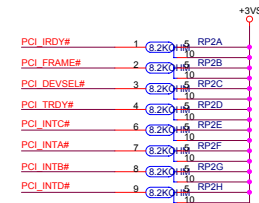
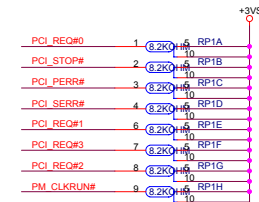
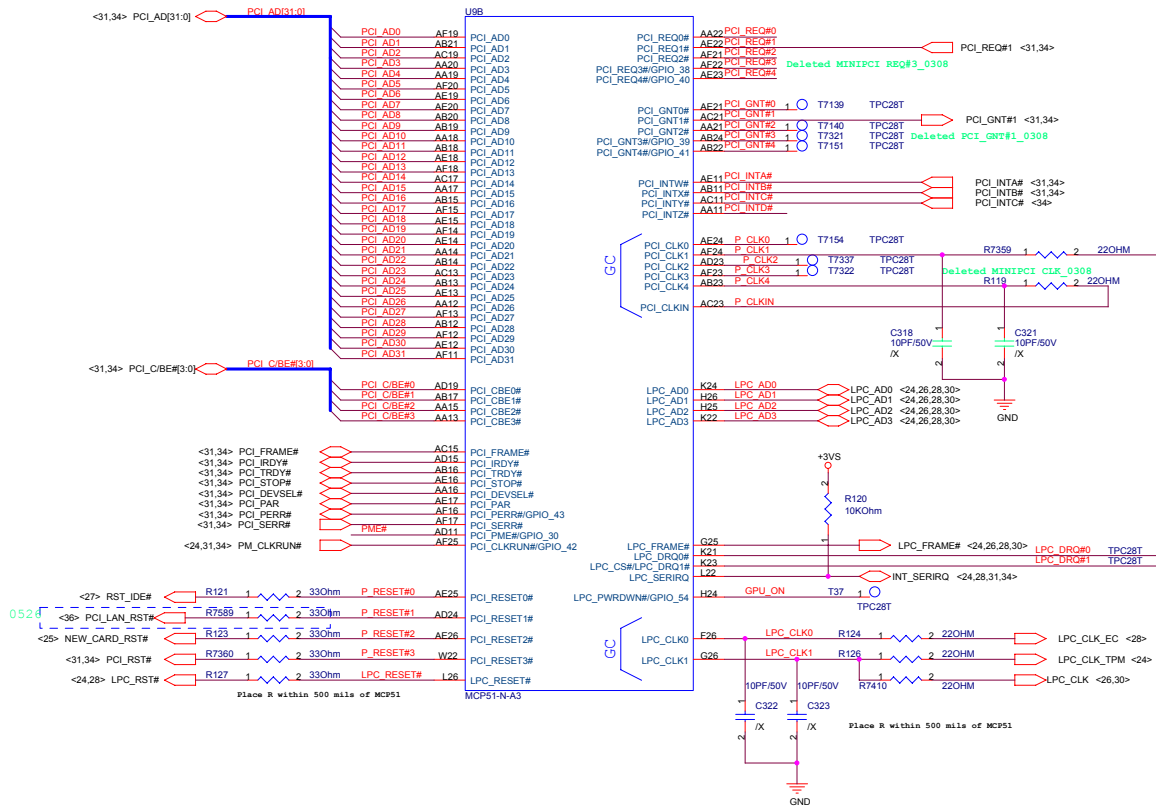
**TV OUT**



Nvidia suggests to change 8\*8.  
Resisters setting can reference design guide  
chapter12 (Page 176).





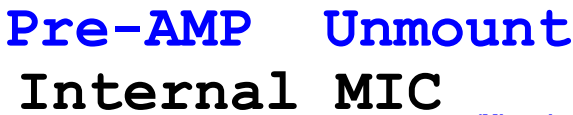




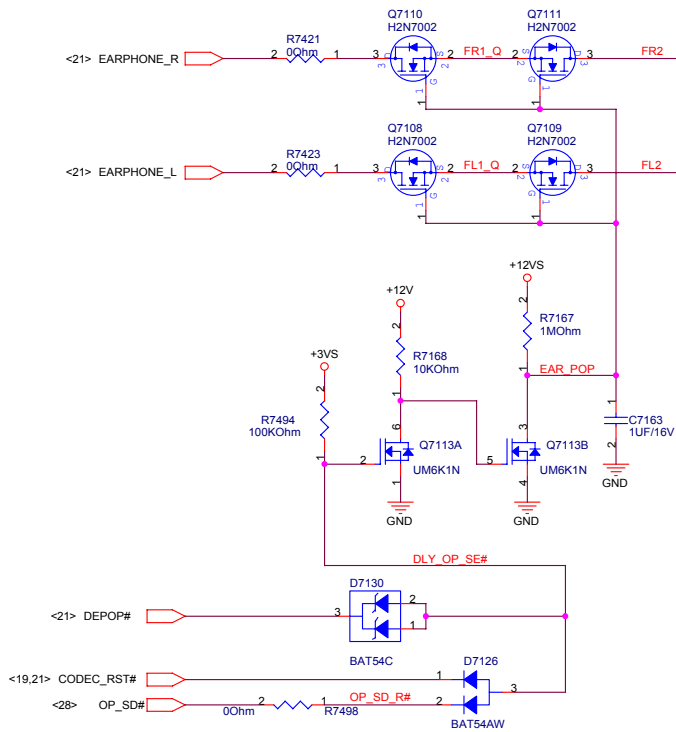




## 0524 Modified

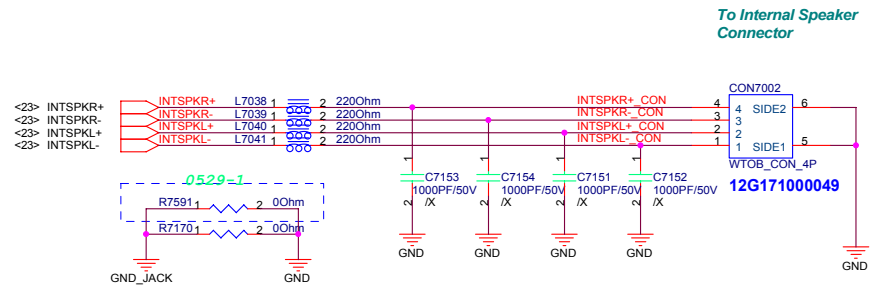


## DEPOP CIRCUIT

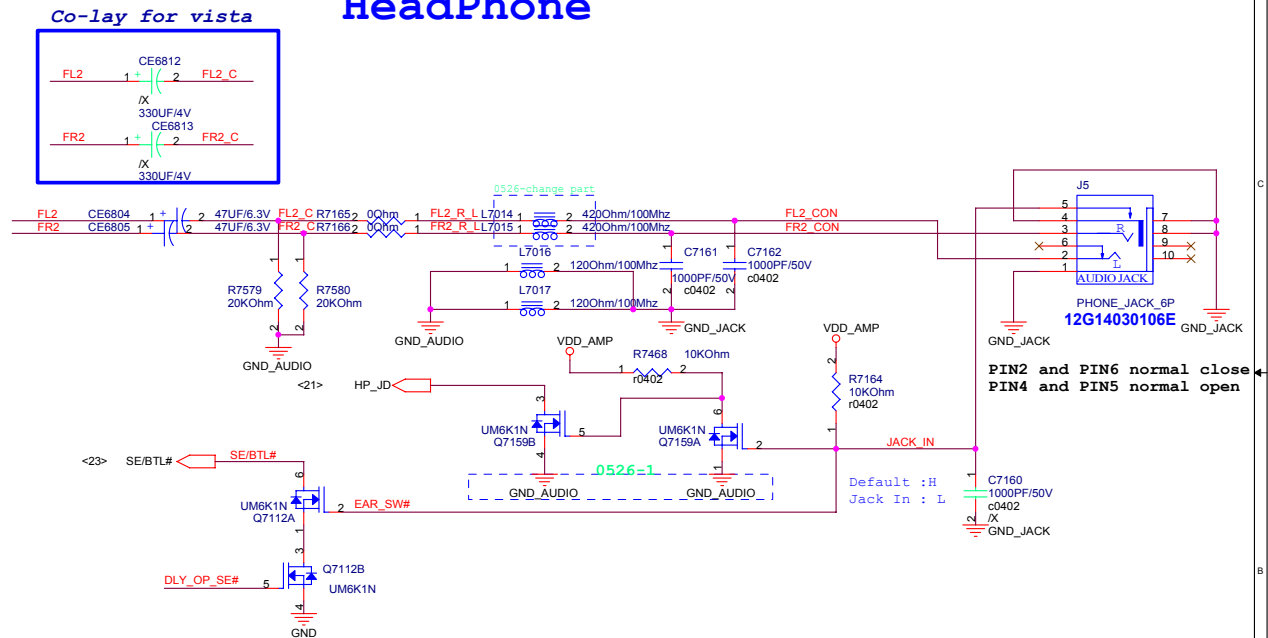


Fix POP of the internal speaker  
when power-on

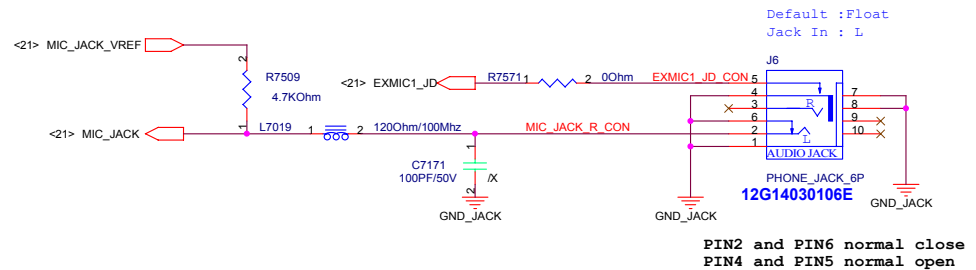
## SPEAKER



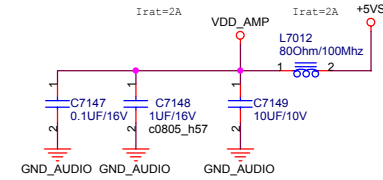
## HeadPhone



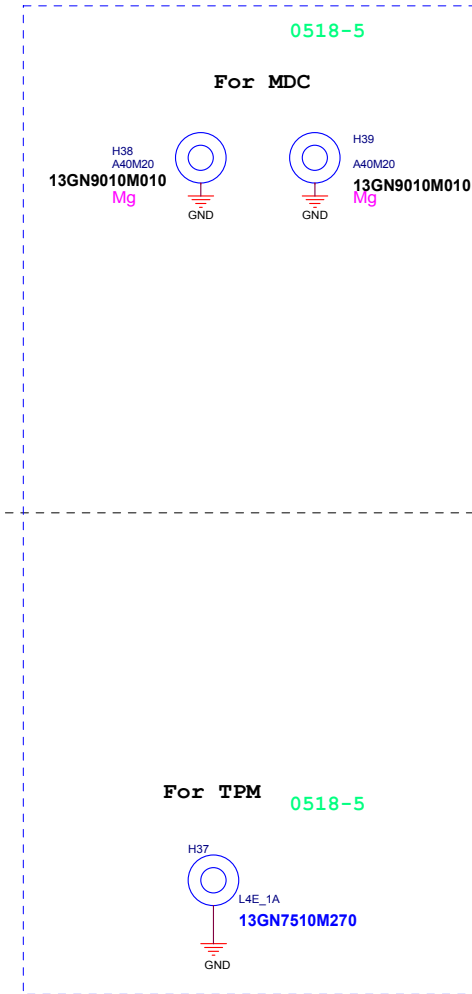
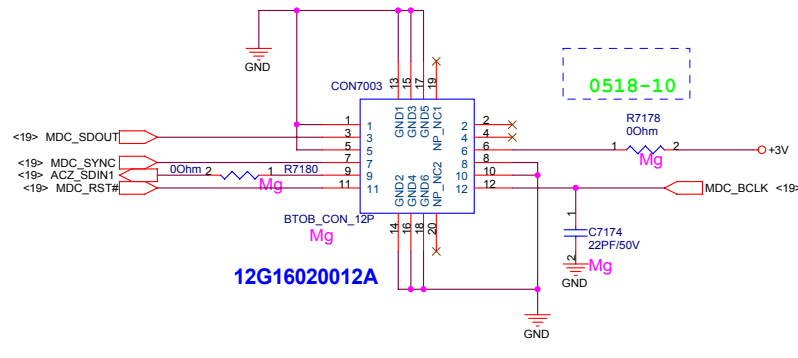
## External Microphone



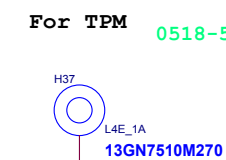
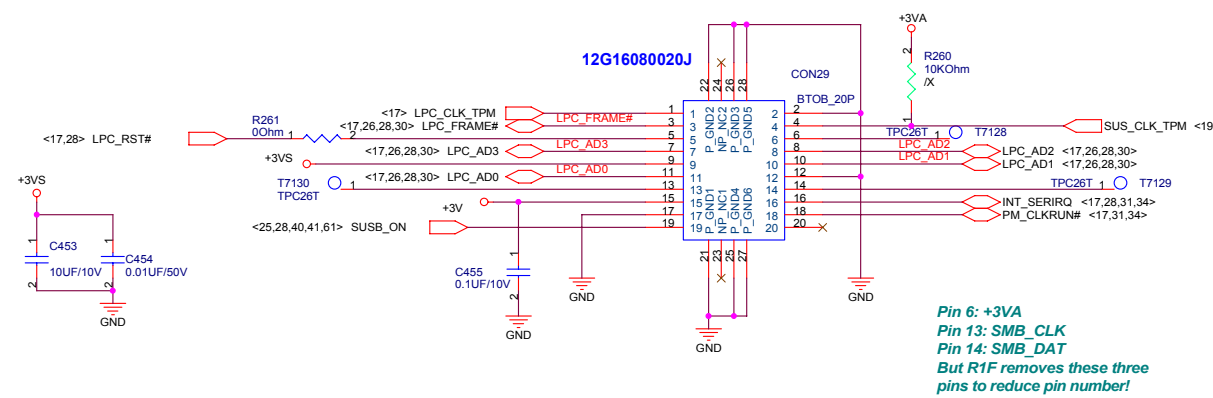
## TV-Tuner



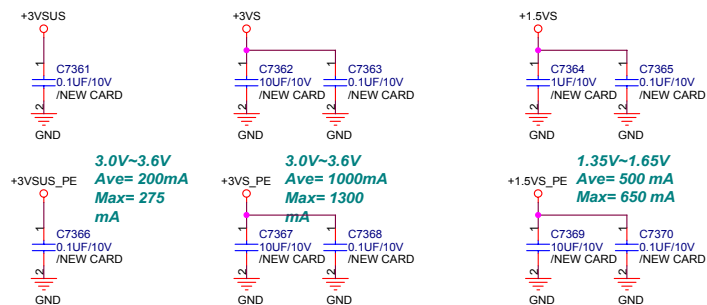
# MDC CONN.



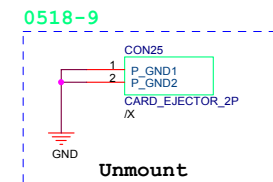
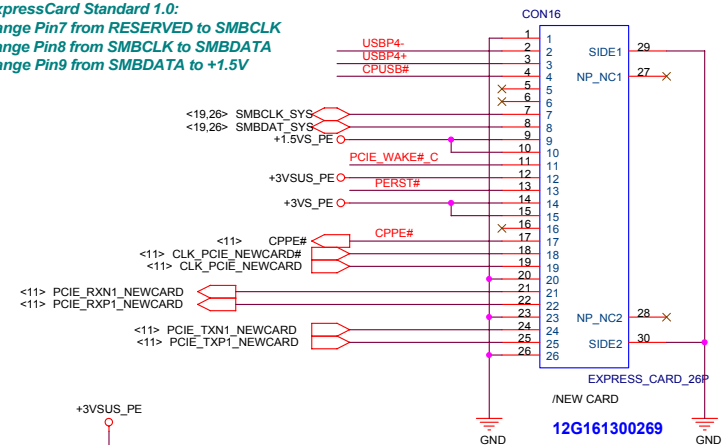
# TPM CONN.



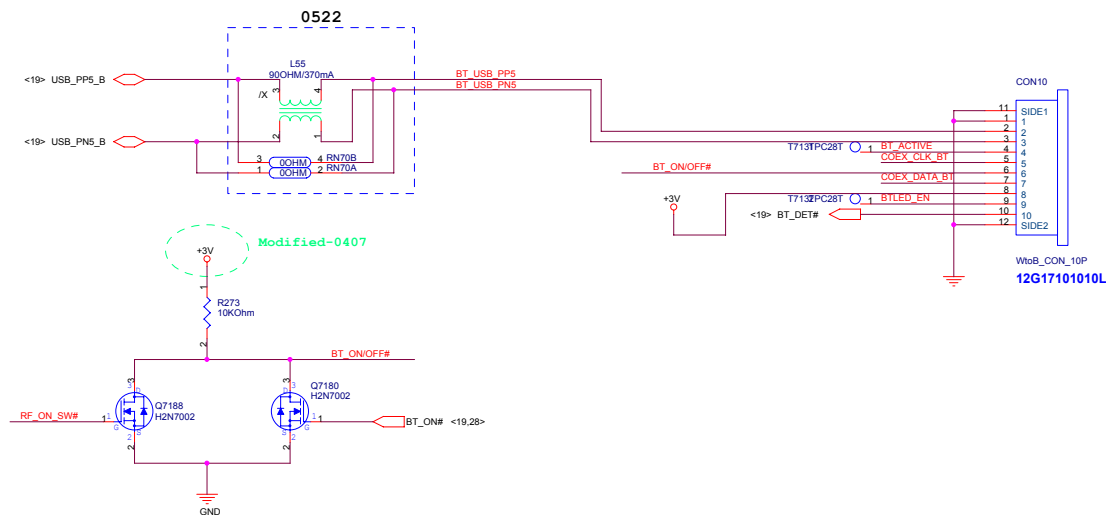
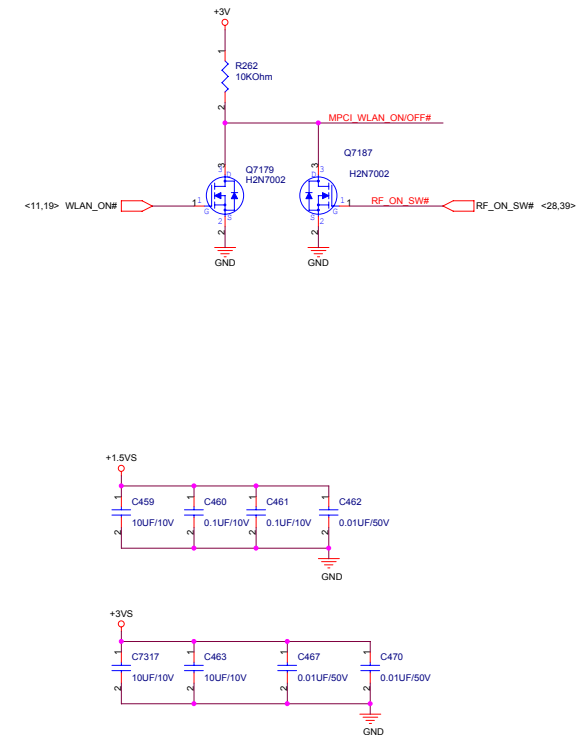




**!! ExpressCard Standard 1.0:**  
**Change Pin7 from RESERVED to SMBCLK**  
**Change Pin8 from SMBCLK to SMBDATA**  
**Change Pin9 from SMBDATA to +1.5V**

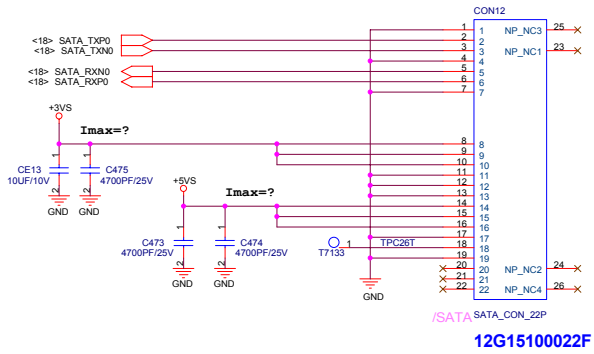


## BLUETOOTH CONNECTOR

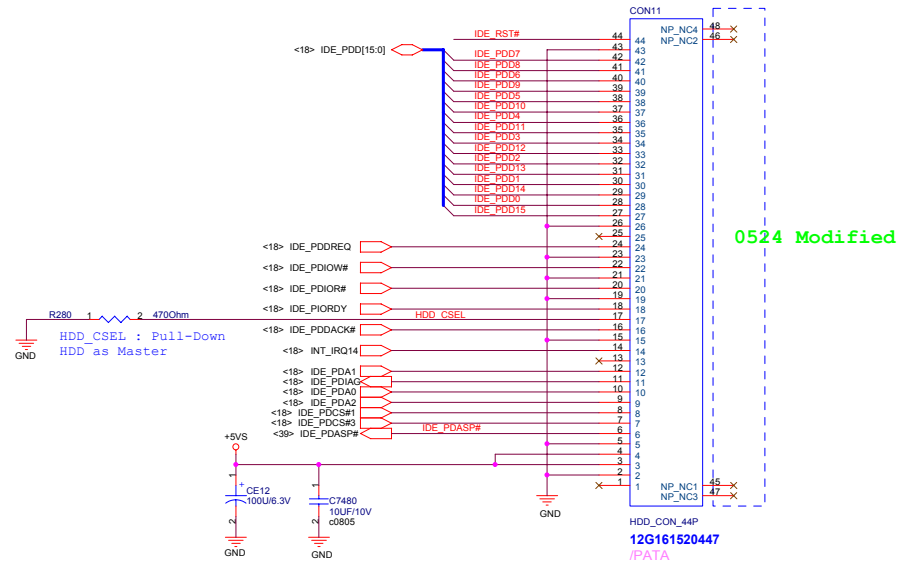


The schematic diagram shows the BT module connections. The BT module has two main signal lines: BT\_CLK and BT\_DATA. The BT\_CLK line is connected to the COEX\_CLK\_BT pin (pin 1) and the BT\_CHCLK pin (pin 2). The BT\_DATA line is connected to the COEX\_DATA\_BT pin (pin 1) and the BT\_DATA pin (pin 2). A 0Ohm resistor (R269) is connected between the BT\_CLK and BT\_CHCLK pins. A 100KOhm resistor (R272) is connected between the BT\_DATA pin and ground.

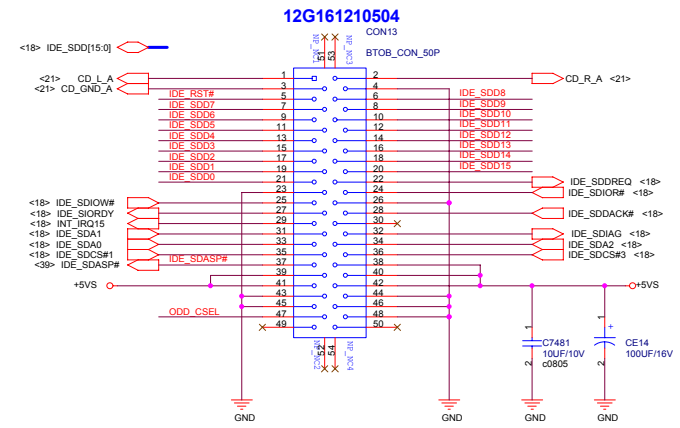
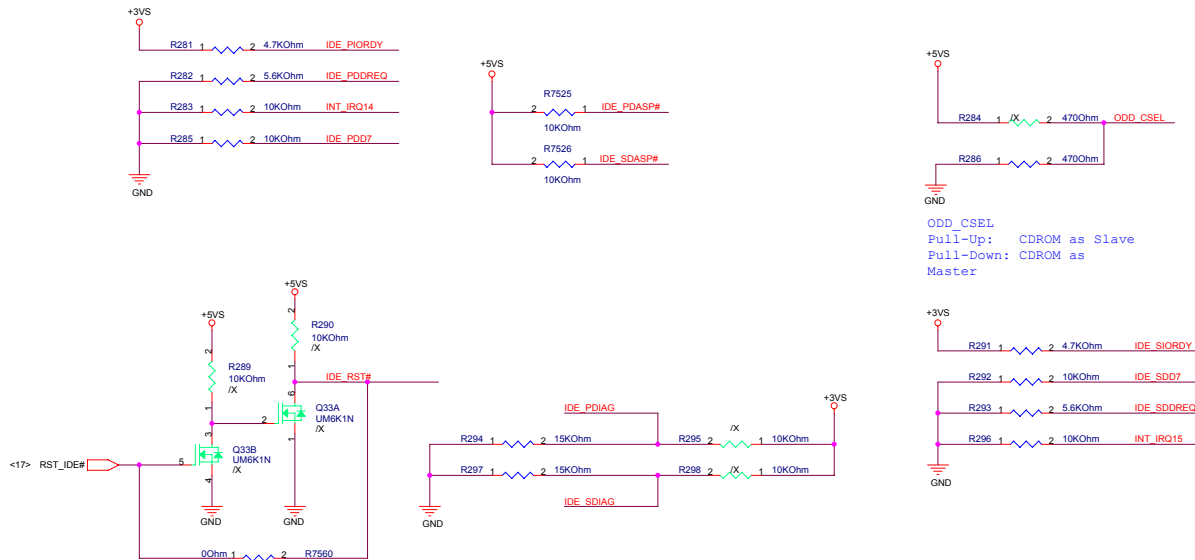
## SATA\_HDD



## PATA-HDD(Default)



## CD-ROM

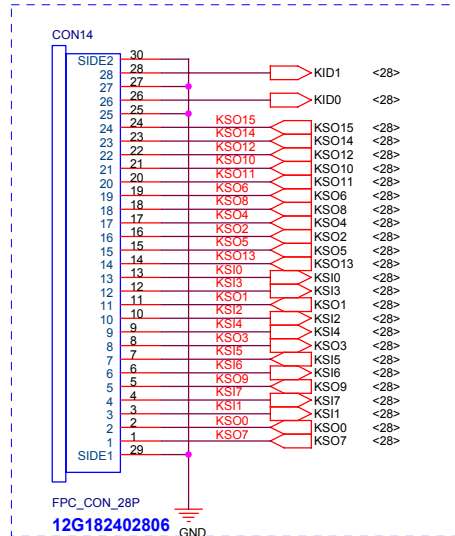




# KBC connector

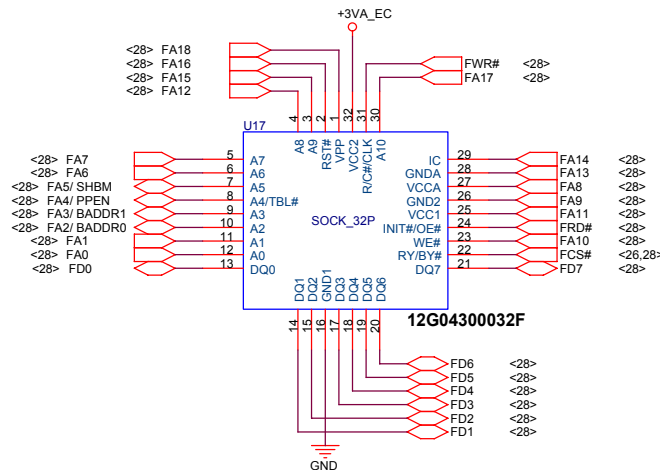
For Keyboard  
Matrix Define same Z94

0518-7



# ISA ROM

(4Mbits)



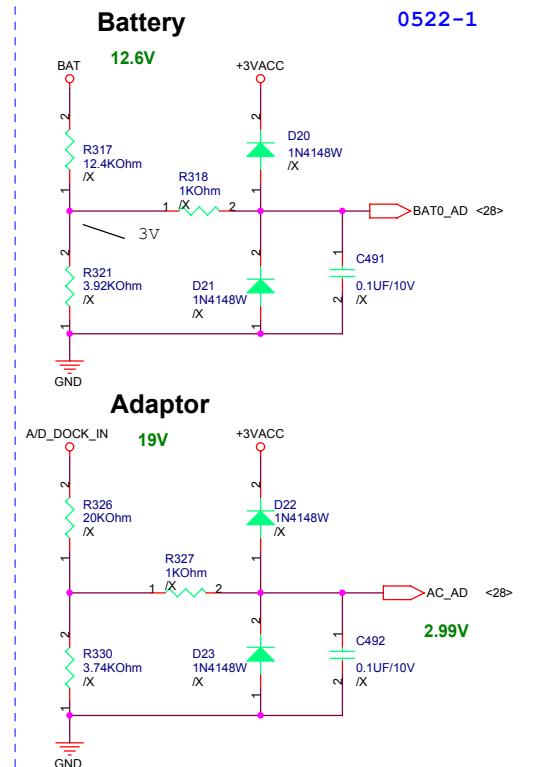
SST-PLCC32 4Mbits Flash ROM  
PN:05G001014110  
(FLASH SST SST39VF040-70-4C-NHE  
4M-70 PLCC-32)

If need to use 8Mbits ISA  
ROM, could choose  
SST39LF080.  
But it does not have PLCC32  
package.  
ASUS does not have part  
number yet.

Flash ROM PN:05G001014110

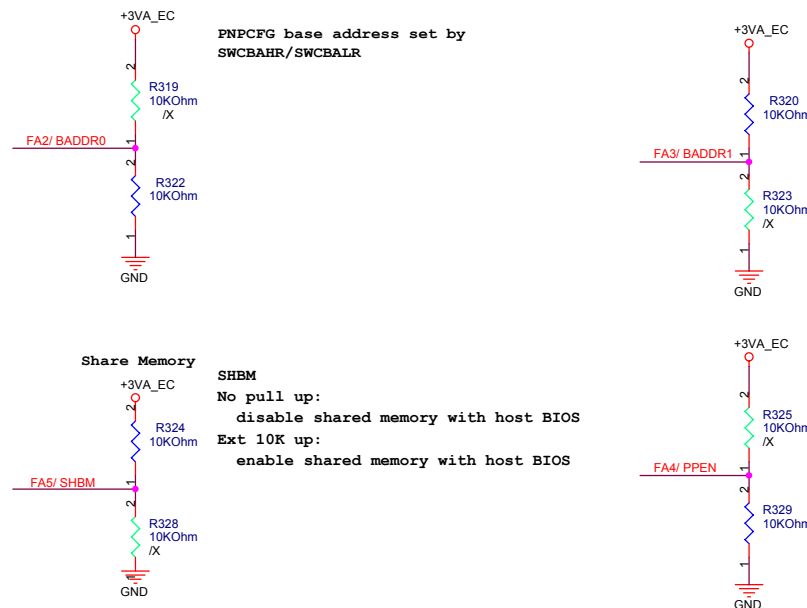
# EC ADC

0522-1



# EC Hardware Strap

strap value sampled after  
VSTBY power up reset



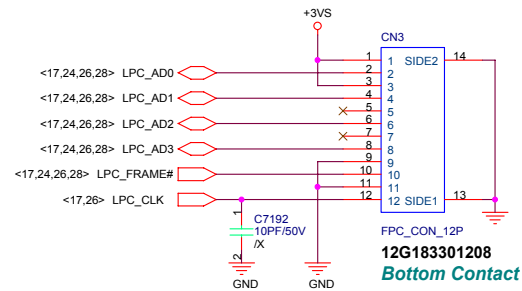
PNPCFG base address set by  
SWCBAHR/SWCBALR

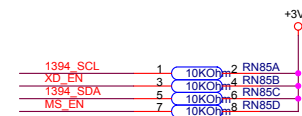
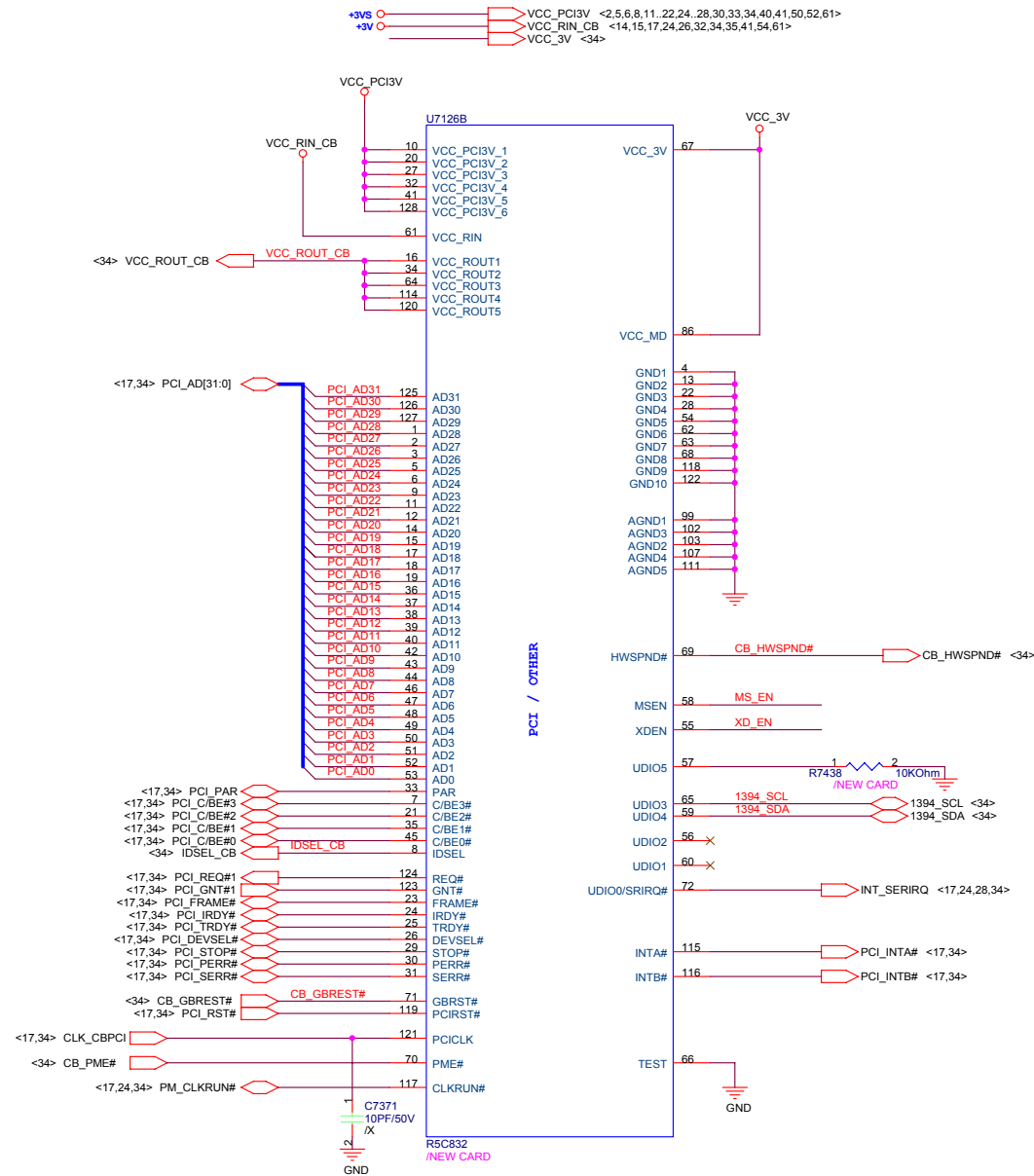
BADDR[1:0]  
No pull up:  
The register pair to access PNPCFG is  
002Eh and 002Fh.  
Ext 10K up on BADDR0:  
The register pair to access PNPCFG is  
004Eh and 004Fh.  
Ext 10K up on BADDR1:  
The register pair to access PNPCFG is  
determined by EC domain registers  
SWCBAHR and SWCBAHR.

SHBM  
No pull up:  
disable shared memory with host BIOS  
Ext 10K up:  
enable shared memory with host BIOS

PPEN  
No pull up:  
Normal  
Ext 10K up:  
KBS interface pins are switched  
to parallel port interface for  
in-system programming.

# LPC DEGUG CONNECTOR

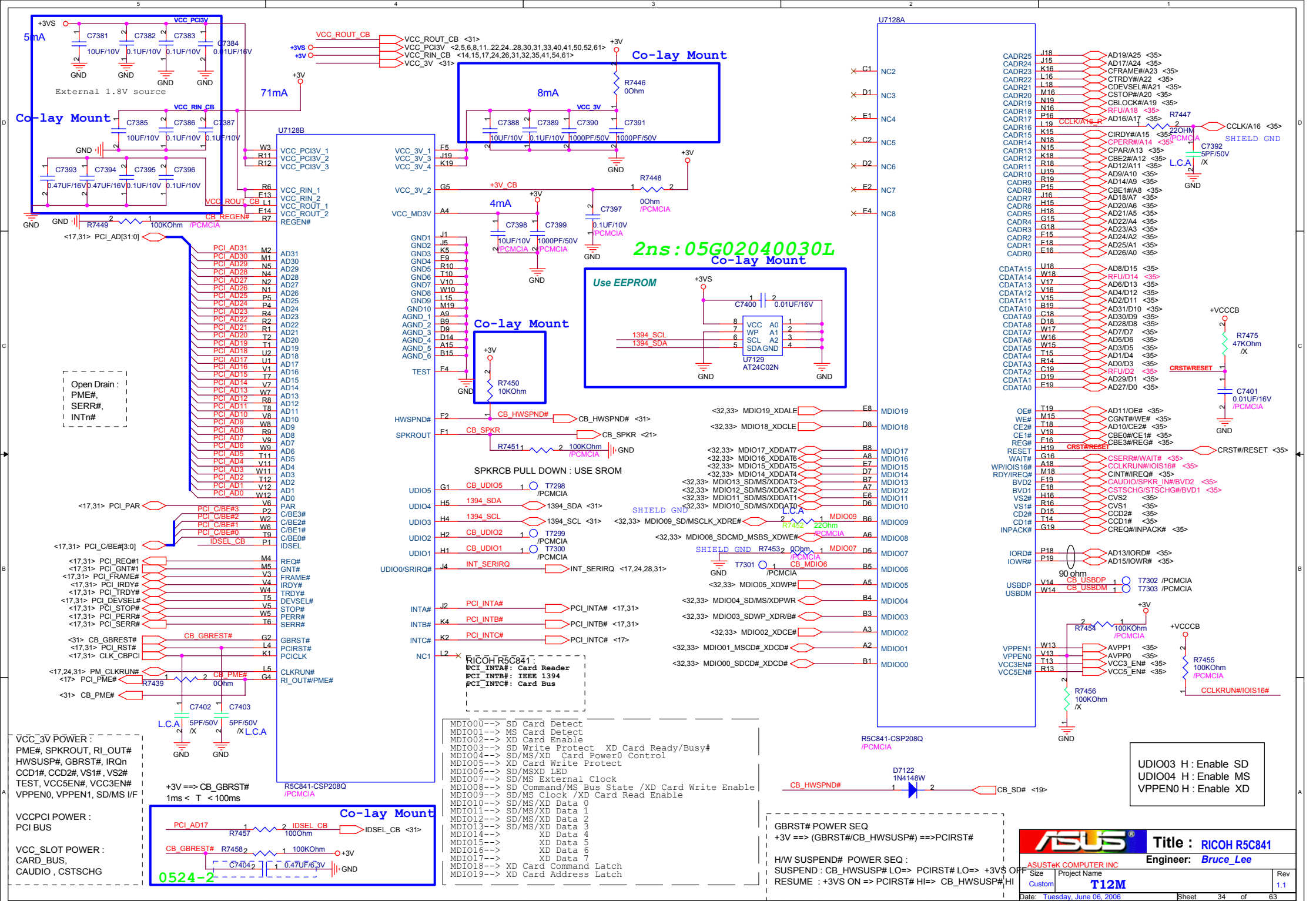




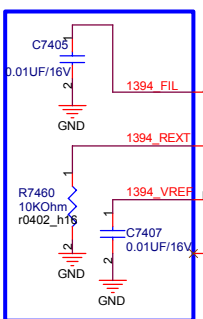




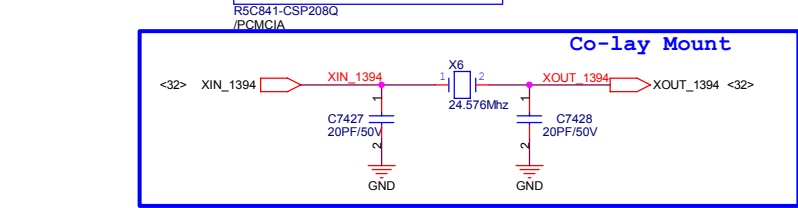




Co-lay Mount

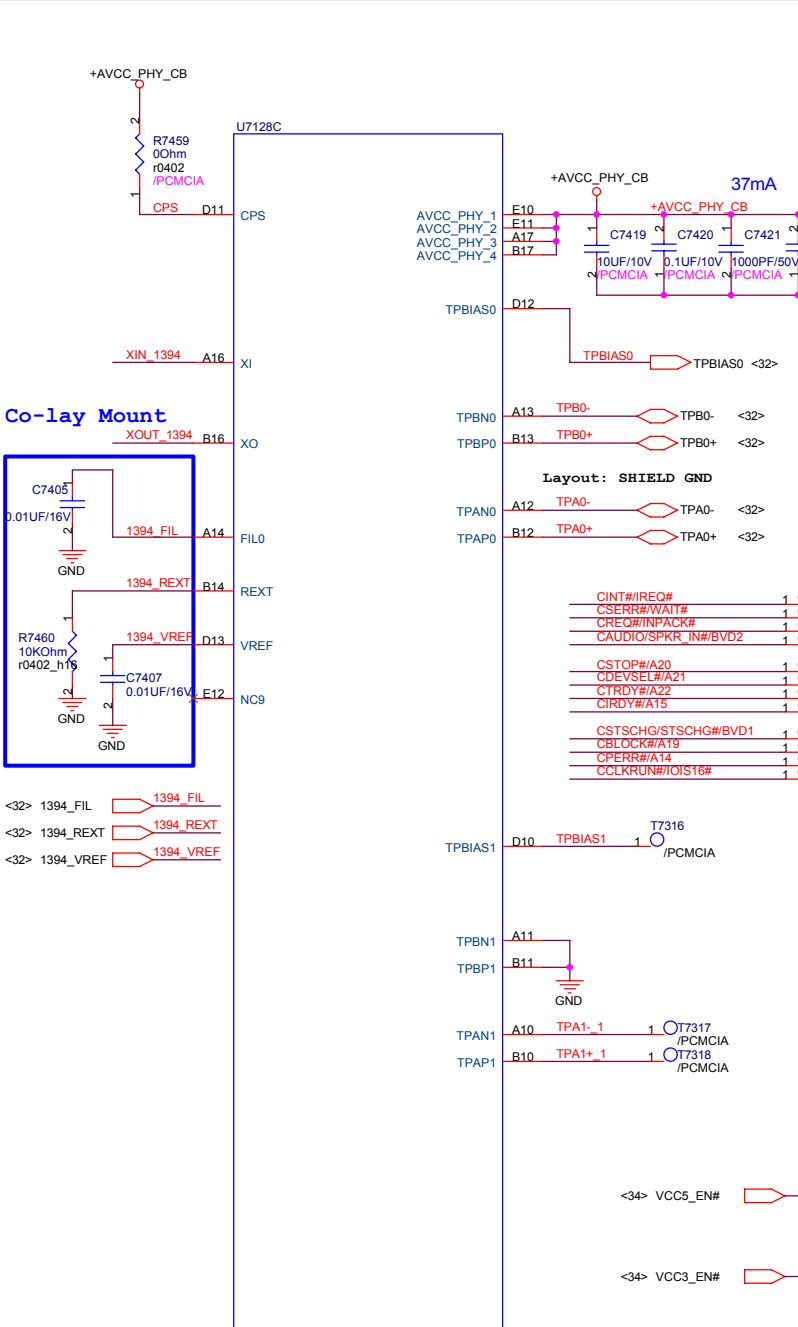


<32> 1394\_FIL 1394\_FIL  
<32> 1394\_REXT 1394\_REXT  
<32> 1394\_VREF 1394\_VREF



<32> XIN\_1394 XIN\_1394 XOUT\_1394 XOUT\_1394 <32>

5 4 3 2 1



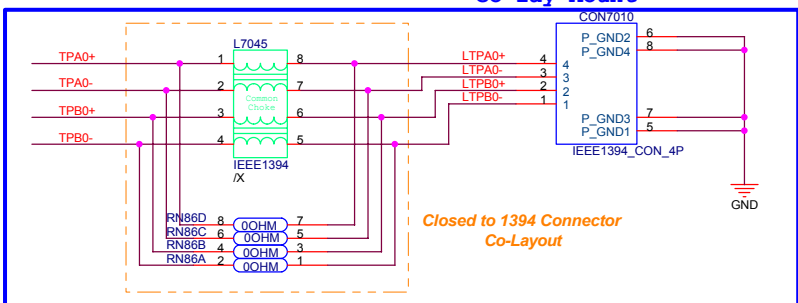
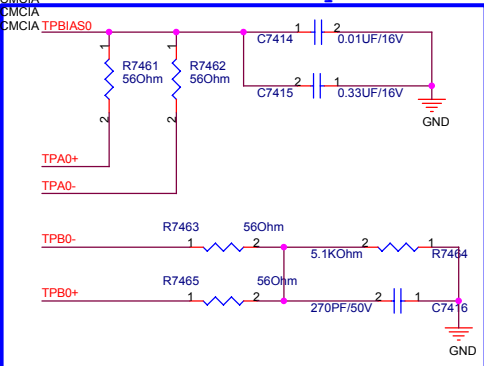
Layout: SHIELD GND

- CINT#/REQ# 1 T7304 /PCMCIA
- CSERR#/WAIT# 1 T7305 /PCMCIA
- CREQ#/INPACK# 1 T7306 /PCMCIA
- CAUDIO/SPKR\_IN#/BVD2 1 T7307 /PCMCIA
- CSTOP#/A20 1 T7308 /PCMCIA
- CDEVSEL#/A21 1 T7309 /PCMCIA
- CTRDY#/A22 1 T7310 /PCMCIA
- CIRDY#/A15 1 T7311 /PCMCIA
- CSTSCHG/STSCHG#/BVD1 1 T7312 /PCMCIA
- CBLOCK#/A19 1 T7313 /PCMCIA
- CPERR#/A14 1 T7314 /PCMCIA
- CCLKRUN#/IOIS16# 1 T7315 /PCMCIA

PCMCIA SOCKET 0524 Modified

CCD1#	CCD2#
L	L
OTHER	16bit
	32bit

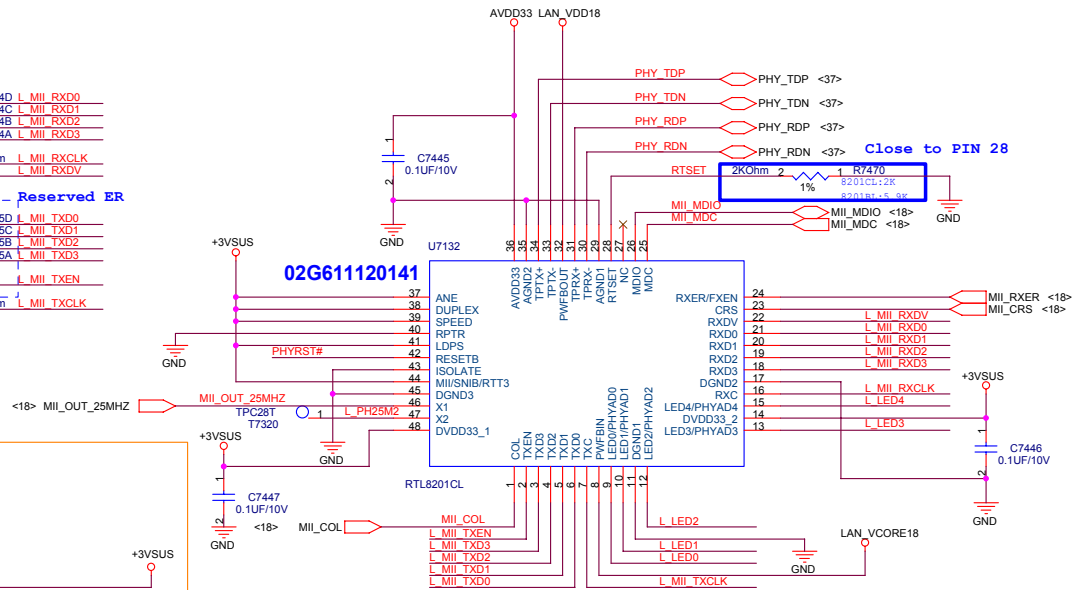
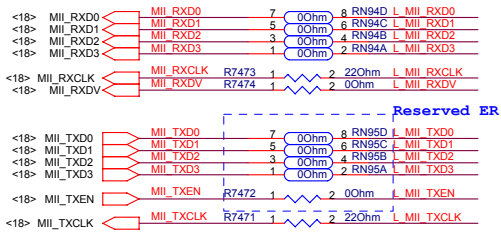
Co-lay Mount



Closed to 1394 Connector Co-Layout



ASUSTeK COMPUTER INC		Title : CARDBUS SOCKET	
Size A3		Engineer: Bruce_Lee	
T12M		Rev 1.1	
Date: Tuesday, June 06, 2006		Sheet 35 of 63	



## LAN LED

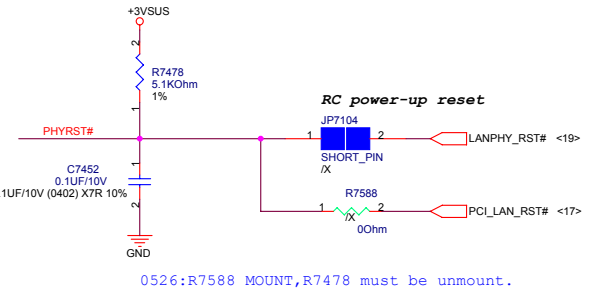
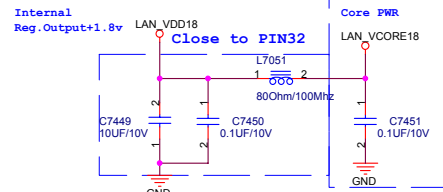
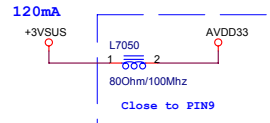
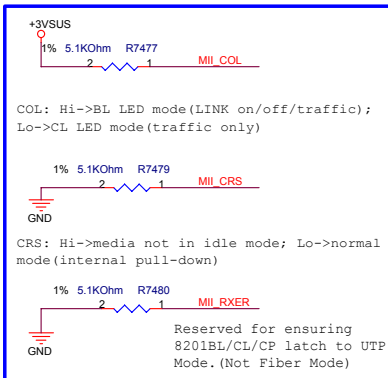
PHY Addr = 00001

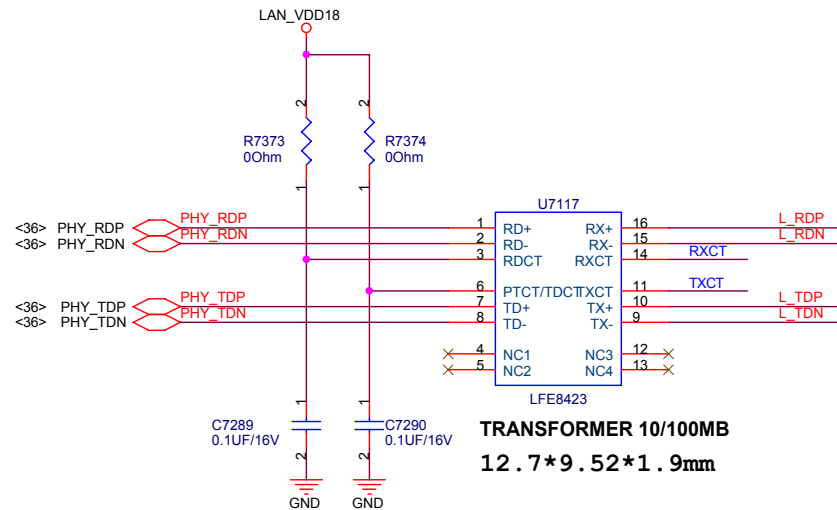
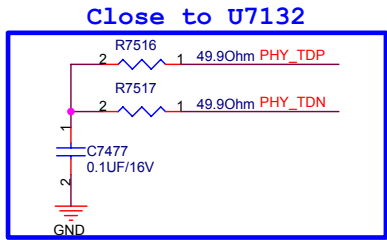
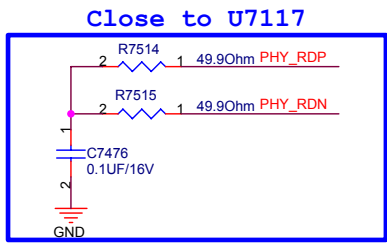
LED0 :LINK  
LED1 :Dupx  
LED2 :10ACT  
LED3 :100ACT  
LED4 :COL

LED test only.-0307

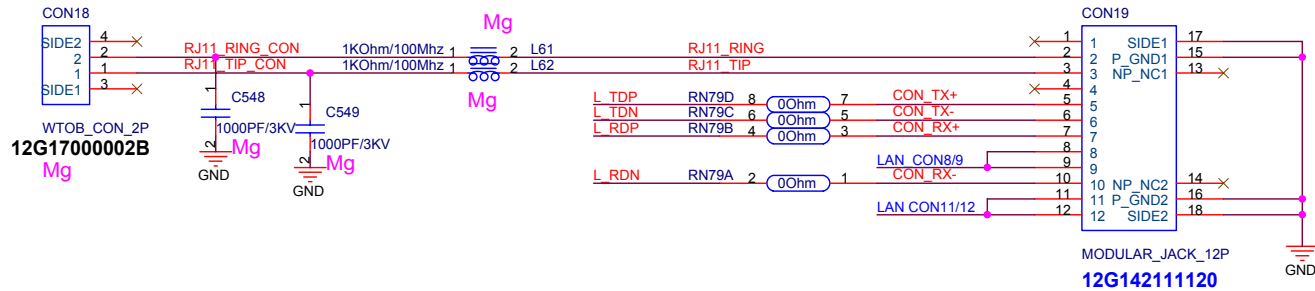
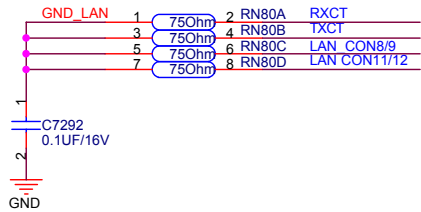
POR Latch low: LED signals are active high

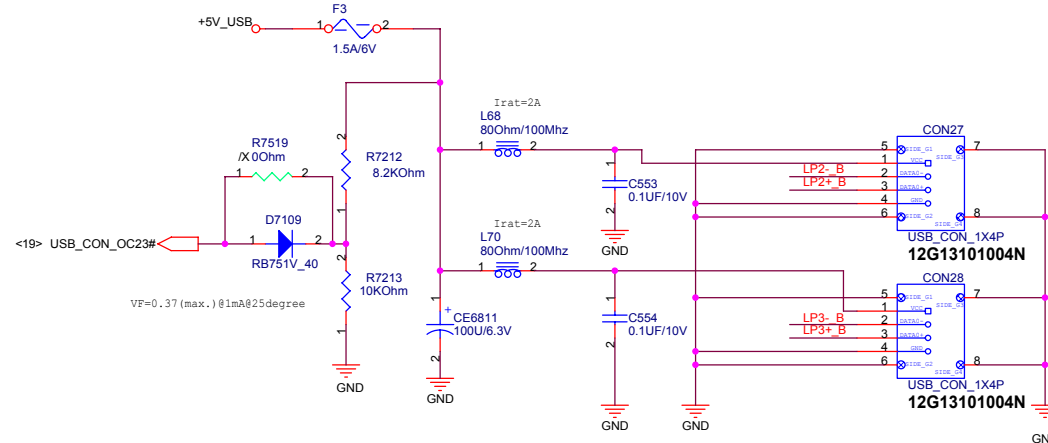
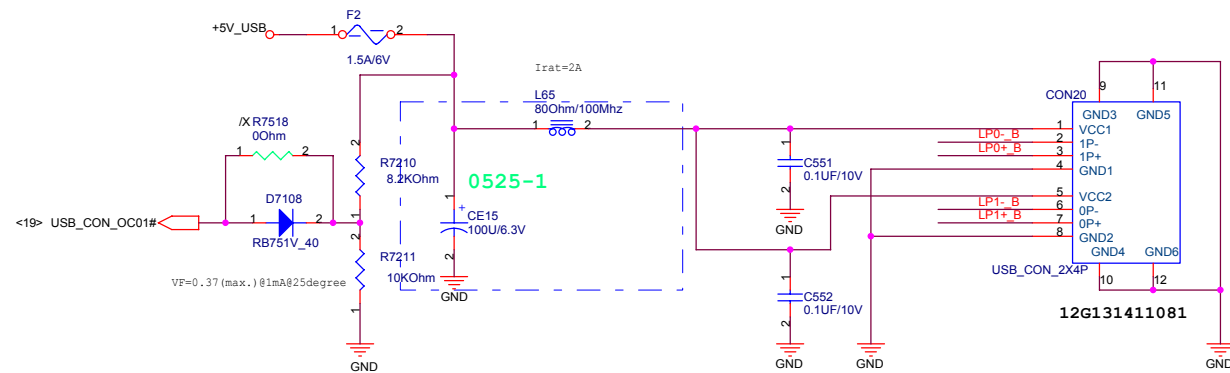
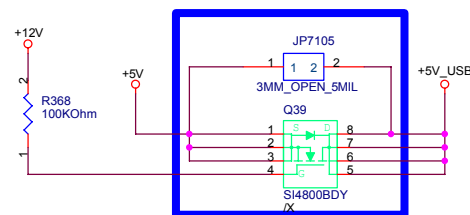
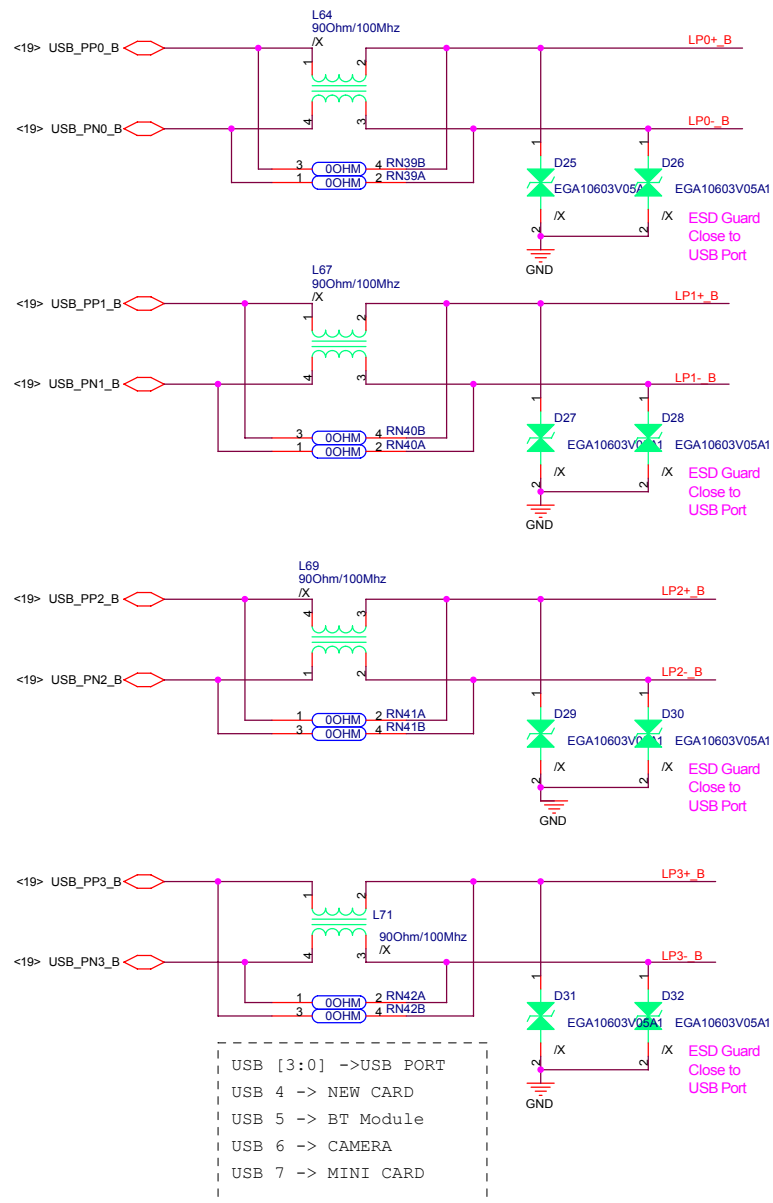
	POR latch status	
	HIGH	LOW
ANE	Auto Negotiation Enable	Force mode
DUPLEX	Enable Full Duplex	Disable
SPEED	Operates at 100Mbps	10Mbps
RPTR	Repeater mode	Normal mode
LPDS	LPDS mode	Normal mode
MIISNIB	MIIS mode	SNI mode



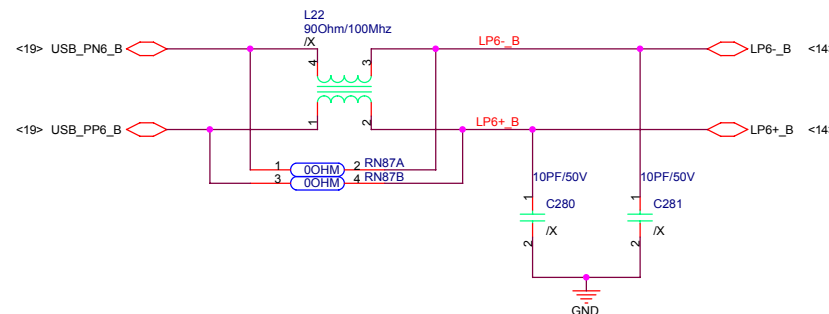


**RJ45+RJ11**  
**100/10M**

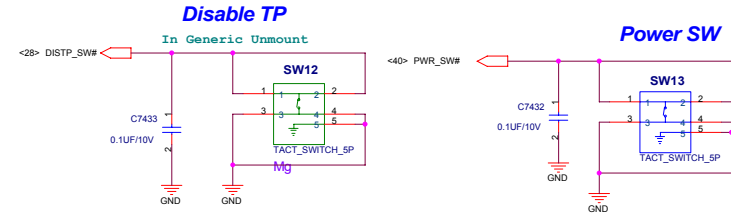




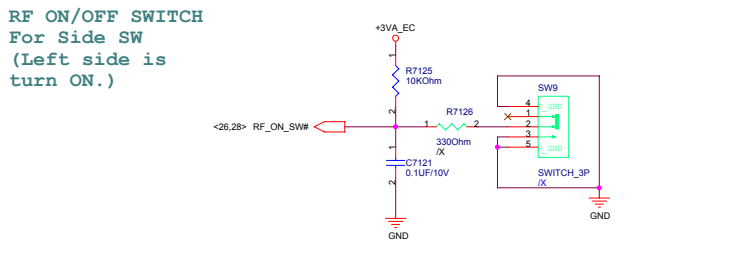
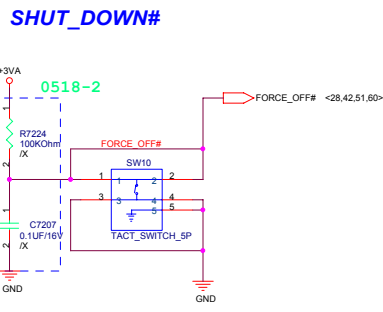
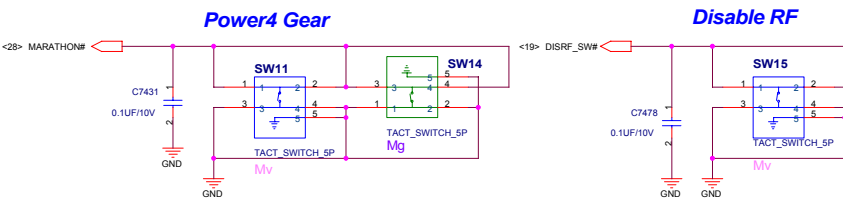
## USB PORT 6 for USB CAMERA



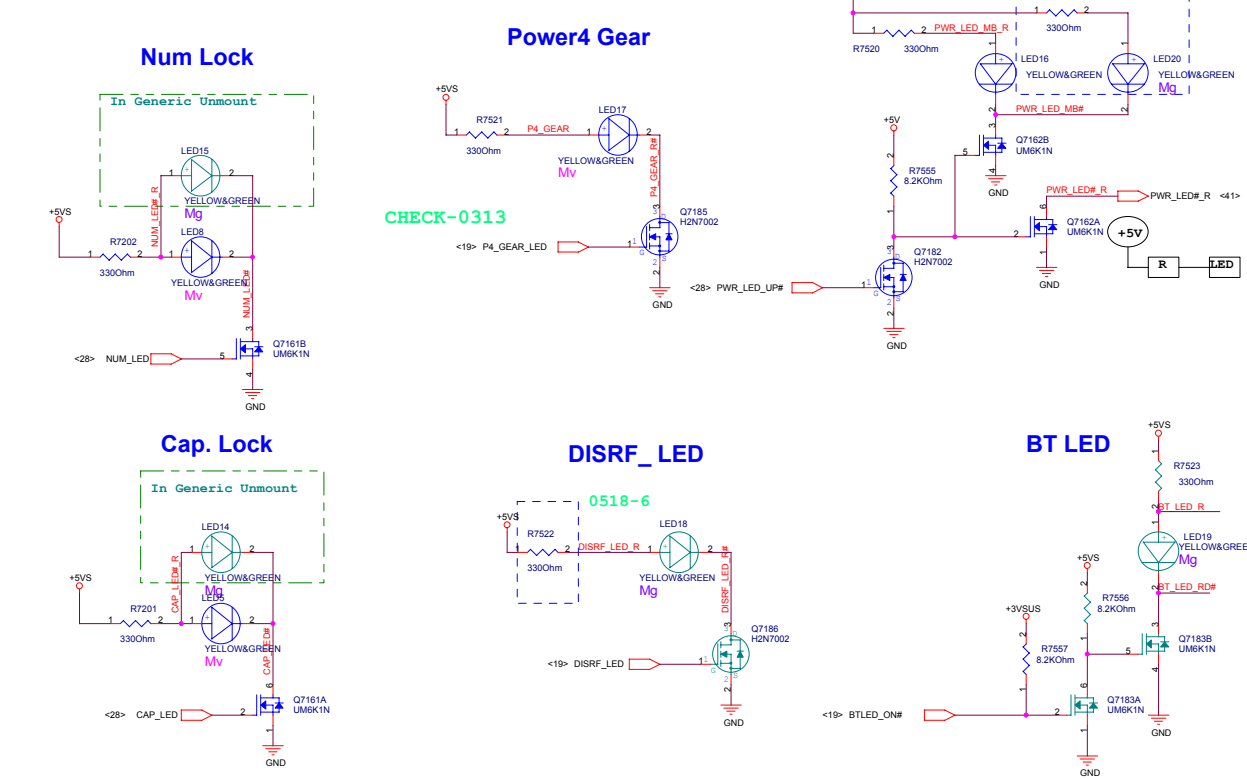
SW Button



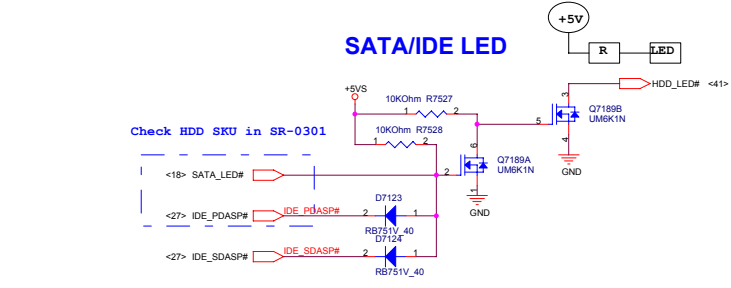
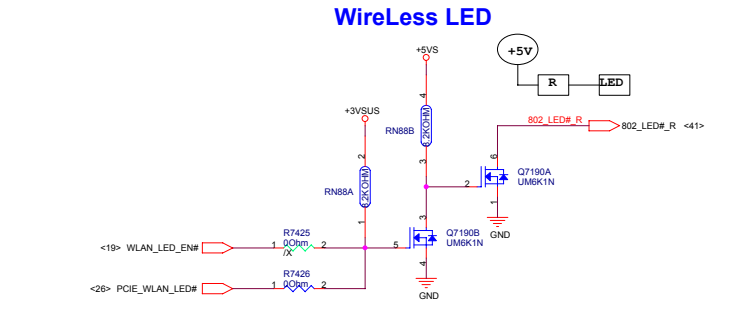
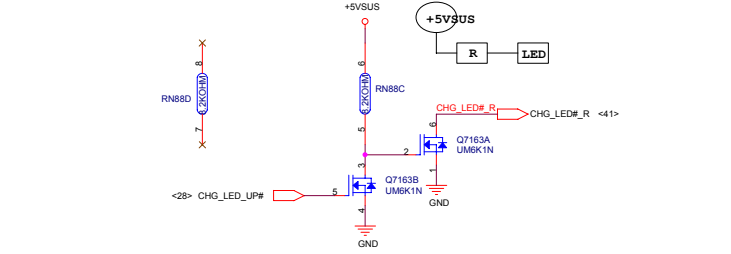
Mv:ParkerBell  
Mg: Generic



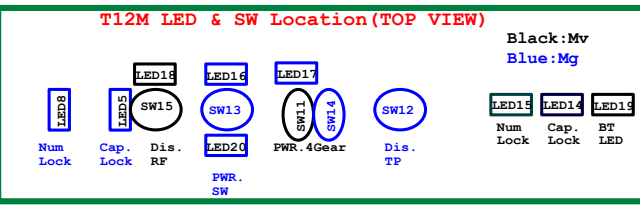
Main Board LED

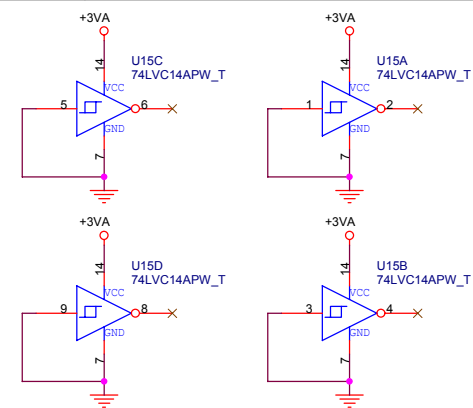
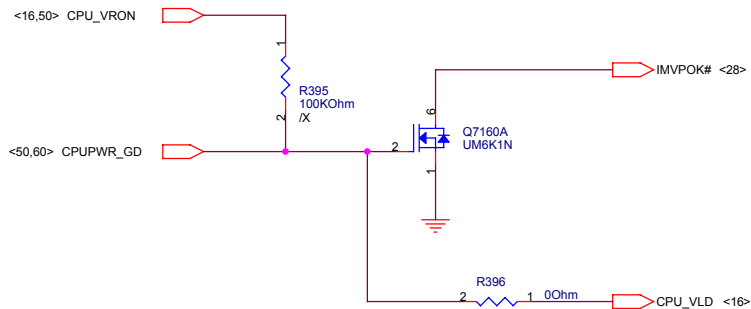
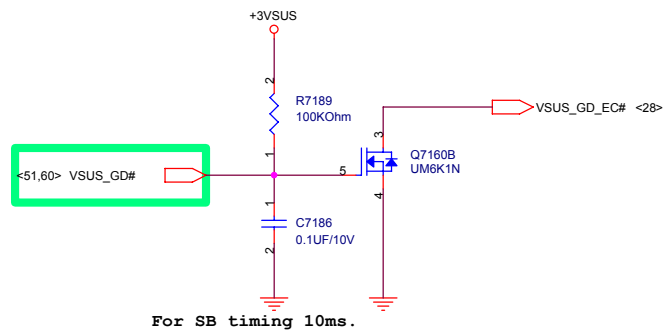
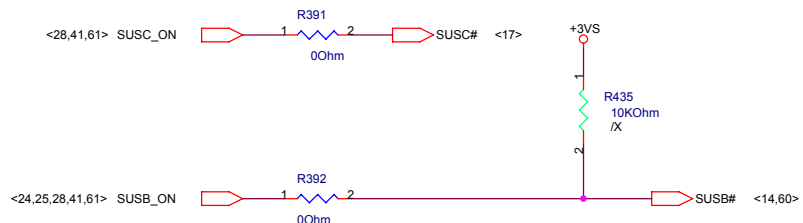


Touch PAD LED



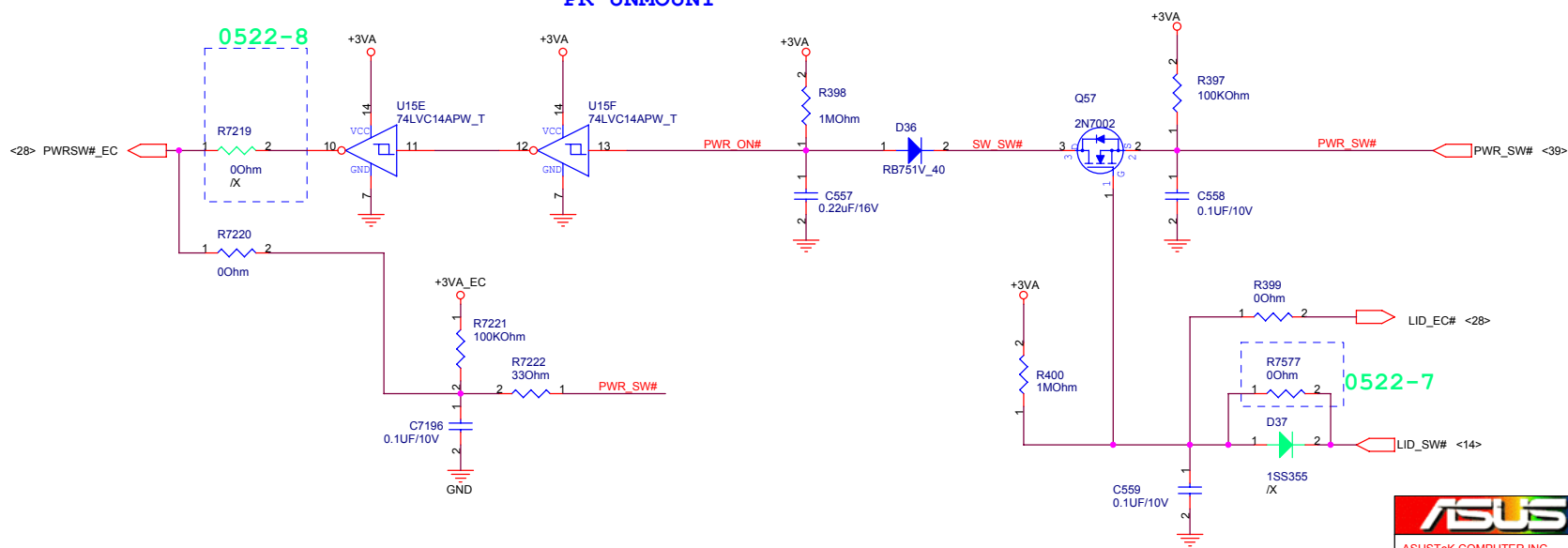
all sw and LED be mounted except sw14 in SR stage-0414





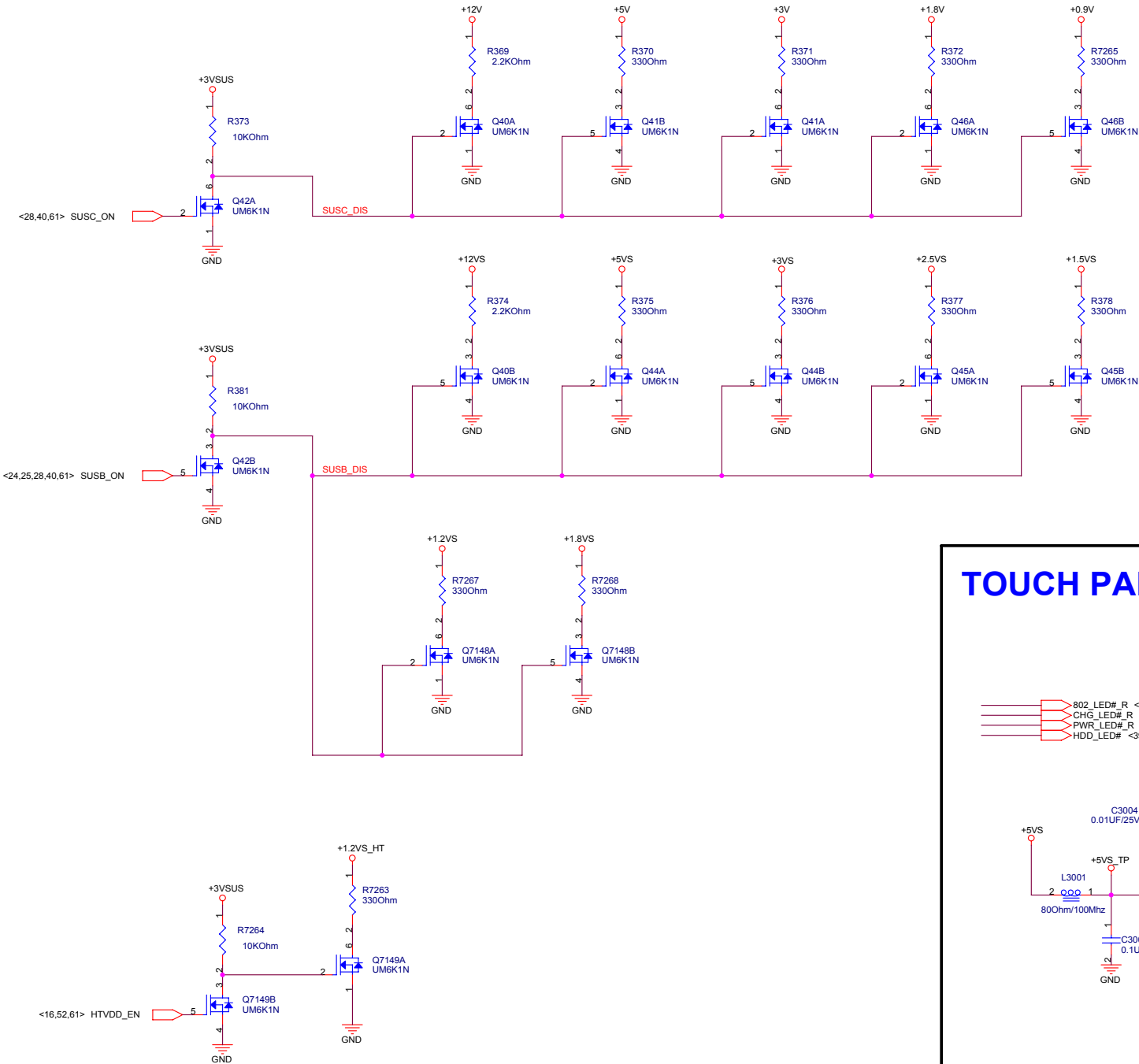
## POWER SWITCH

PR UNMOUNT

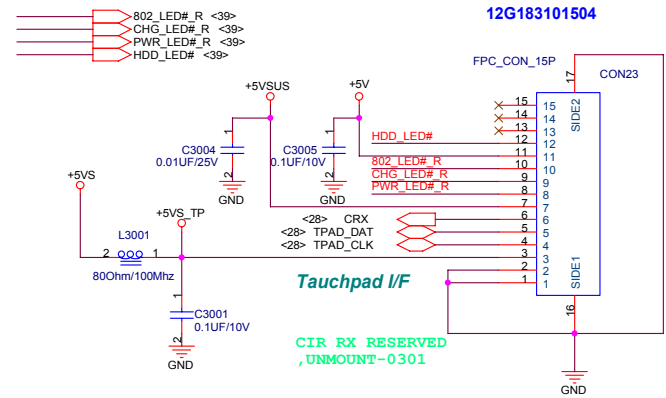




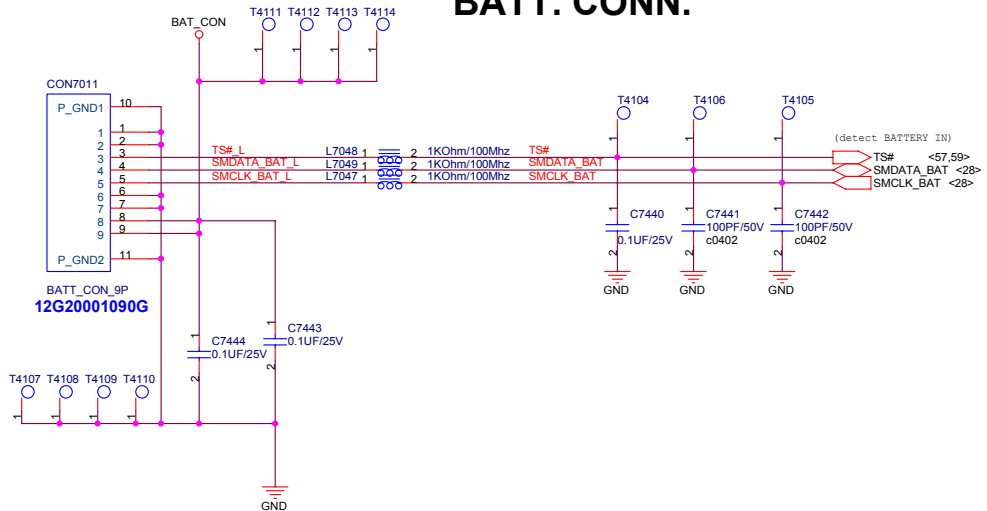
DISCHARGE CIRCUIT



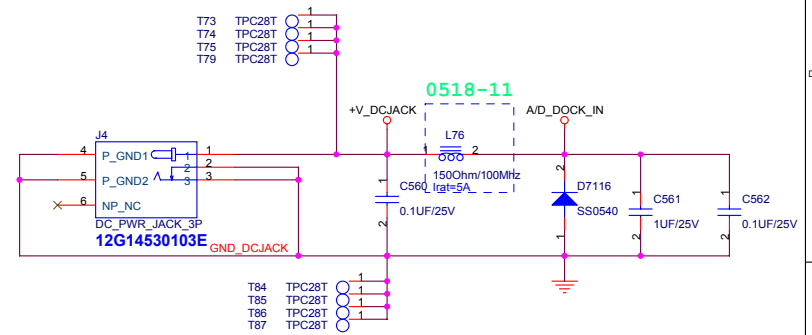
TOUCH PAD



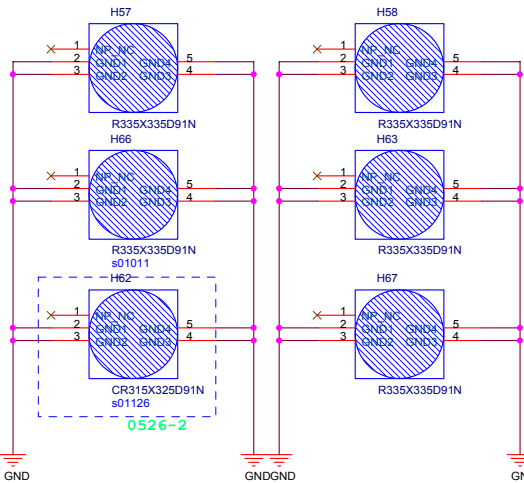
**BATT. CONN.**



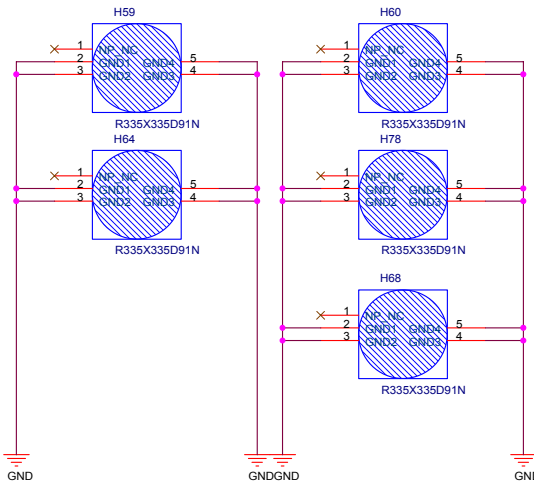
## DC Power Jack



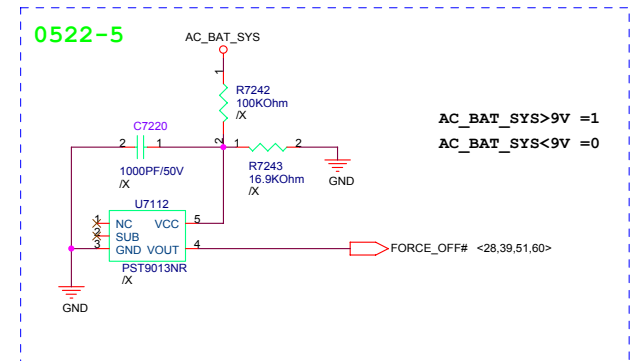
### ***A Hole / TOP Side***



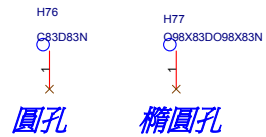
### ***A Hole / Bottom Side***



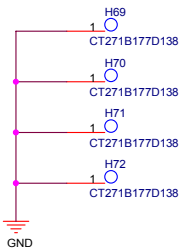
### ***Without Battery & Pull out Adapter***



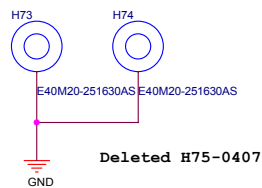
### ***Drill Hole for Fix***



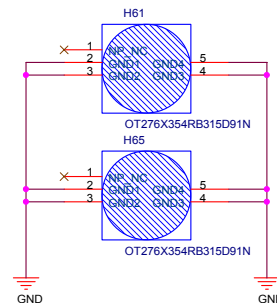
## *F Hole for CPU*



**銅柱 Hole for VGA  
13GNCF10M010**



***E Hole for  
Main board fix***







## T12M ER Update History

0518

0518-1: R7351 unmounted for LPC debug message display

0518-2: R7224 & C7207 unmounted for EC\_RST# timing impact,P-39

0518-3: Deleted OS#\_OC P-U to RN76A for EC\_RST# timing impact,P-8

0518-4:Mount C7353 &C7354,R7413/R7415,R7418 for internal MIC,P-21

0518-5:H37 ,H38/H39 changed PN,P-24

0518-6:Mount R7522,P-39

0518-7:Correct KBC pin definition in CON14,p-29

0518-8:C487 tolerance be changed to X5R,P-28

0518-9:CON25 unmounted,ASSY' part,p-25

0518-10:Removed "JP7103" for MDC power option,p-24

0518-11: "L76" be changed current rating to 5A,P-42

0518-12:Unmounted "R7195",p-26

0518-13:R131 be change to 2.4KOHM , R132 be changed to 1.47kohm For MAC Vref,p-18

0518-14:"R1205" P-U power be changed from"+3VS " to "+3VS\_LCD" for white screen when sys. reboot, p-14

0518-15:Added in "R7572"&"LED20" for brightness improvement,p-39

0519

0519-1:Changed D-SUB Conn. by ME ,P-15

0522

0522-1:EC ADC parts unmount ,P-29

0522-2:R7233 change part from"1.2kohm"to "0ohm',p-8

0522-3:R? reserved 100kohm,p-14

0522-4:N/A

0522-5:UNMOUNT FOR COST DOWN,P-42

0522-6:RESERVERD R? FOR CRX,P-28

0522-7:RESERVERD R? FOR COST DOWN,P-40

0522-8:UNMOUNTED R7219 and mounted R7220 power seq. controlled by EC,P-40

0522-9:BT\_ON# controlled by EC,P-28 &P-19

0522-10:BL controlled by EC form DAC to PWM,P-28

0522-11:UM6K1N body diode changed direction,p-28

0522-12:Changed R7196 from 10kohm to 100kohm and mount,p-26

0522-13:DDR termination resistor SWAP,P-7

0524

0524-1:1394 power changed from +3vs to +3v, resume form s3 detect fail,p-32

0524-2: C7404 changed to 0.47uf for pwr. up seq.,p-34

0524

0524-1:CE15 changed net-name by EMI,P-38

0524-2:C7496 added in CRX signal,P-28

0525

0525-1:Q7159 GND changed to GND\_AUDIO,EMI,P-22

0525-2:H62 change part no.,p-42

0529

0529-1-:Added in R7590 between GND and GND\_AUDIO,P-21

0529-2:Added in R7591 between GND and GND\_JACK,P-22

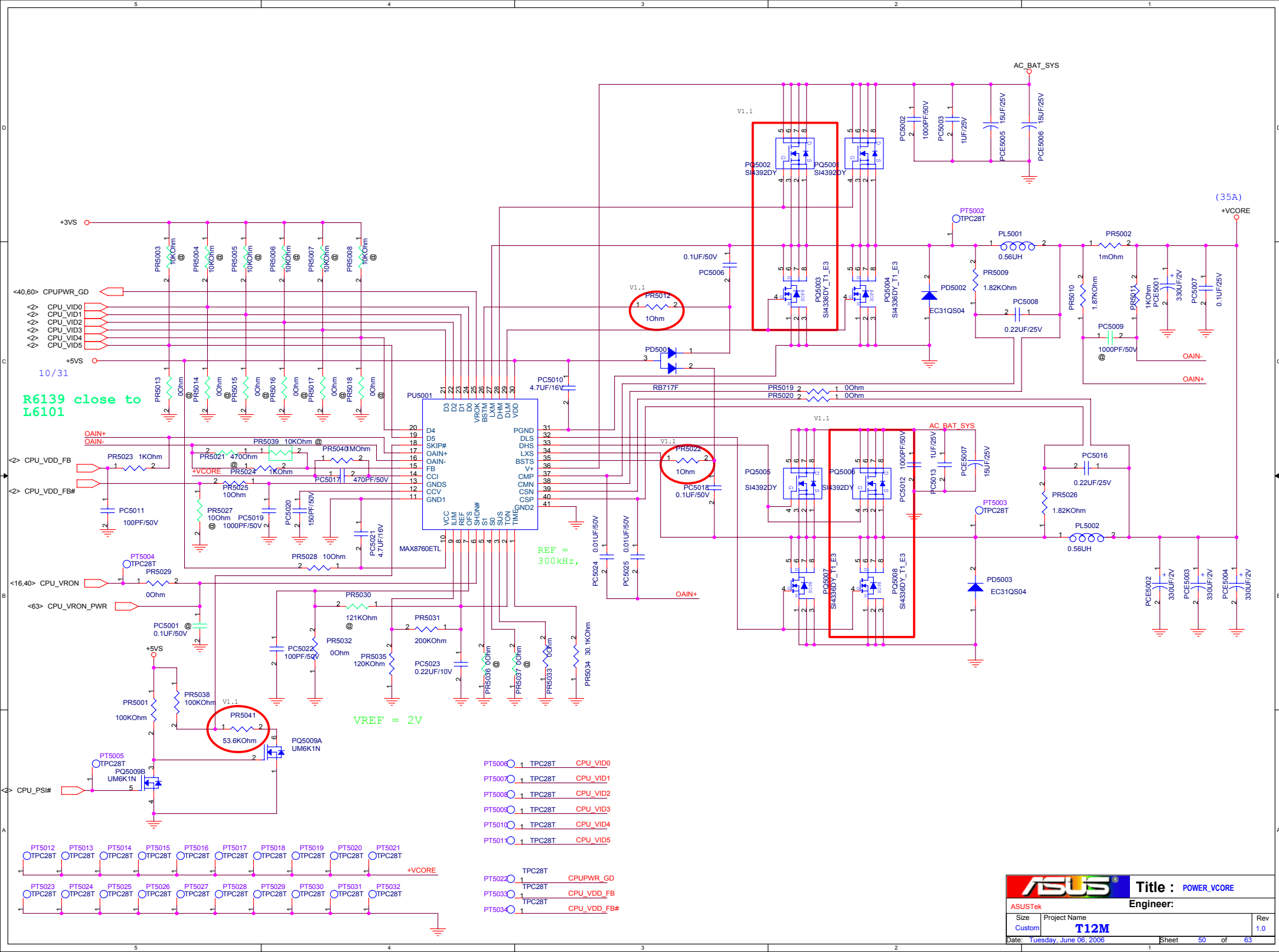












10/31  
R6139 close to  
L6101

REF =  
300kHz,

VREF = 2V

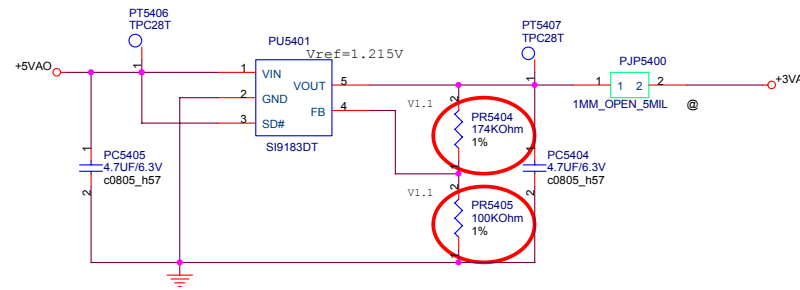
- PT5000 1 TPC28T CPU\_VID0
- PT5001 1 TPC28T CPU\_VID1
- PT5002 1 TPC28T CPU\_VID2
- PT5003 1 TPC28T CPU\_VID3
- PT5010 1 TPC28T CPU\_VID4
- PT5011 1 TPC28T CPU\_VID5
- PT5020 1 TPC28T
- PT5021 1 TPC28T
- PT5022 1 TPC28T CPUPWR\_GD
- PT5023 1 TPC28T CPU\_VDD\_FB
- PT5024 1 TPC28T CPU\_VDD\_FB#
- PT5025 1 TPC28T
- PT5026 1 TPC28T
- PT5027 1 TPC28T
- PT5028 1 TPC28T
- PT5029 1 TPC28T
- PT5030 1 TPC28T
- PT5031 1 TPC28T
- PT5032 1 TPC28T



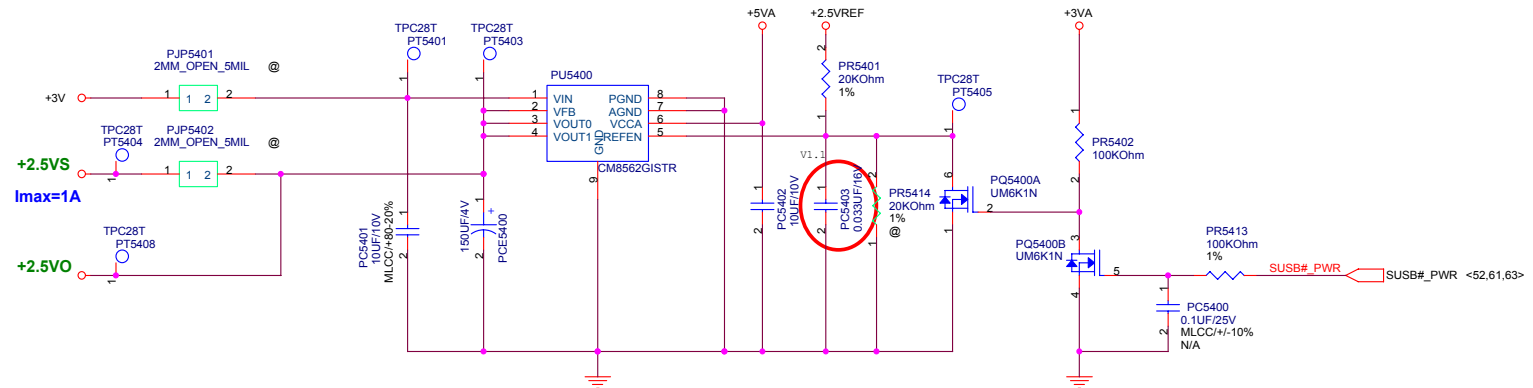




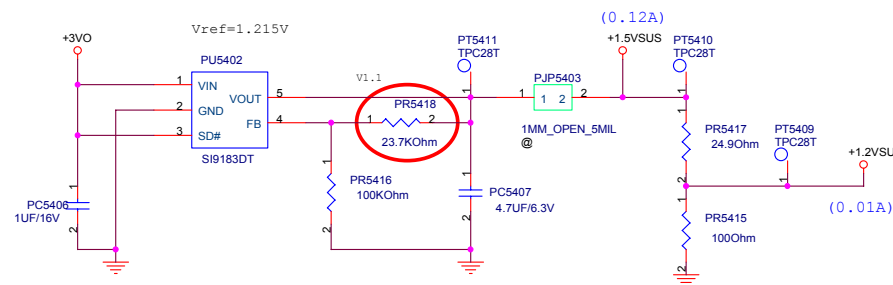
## +3VAO



## +2.5VS



## +1.5VSUS&+1.2VSUS

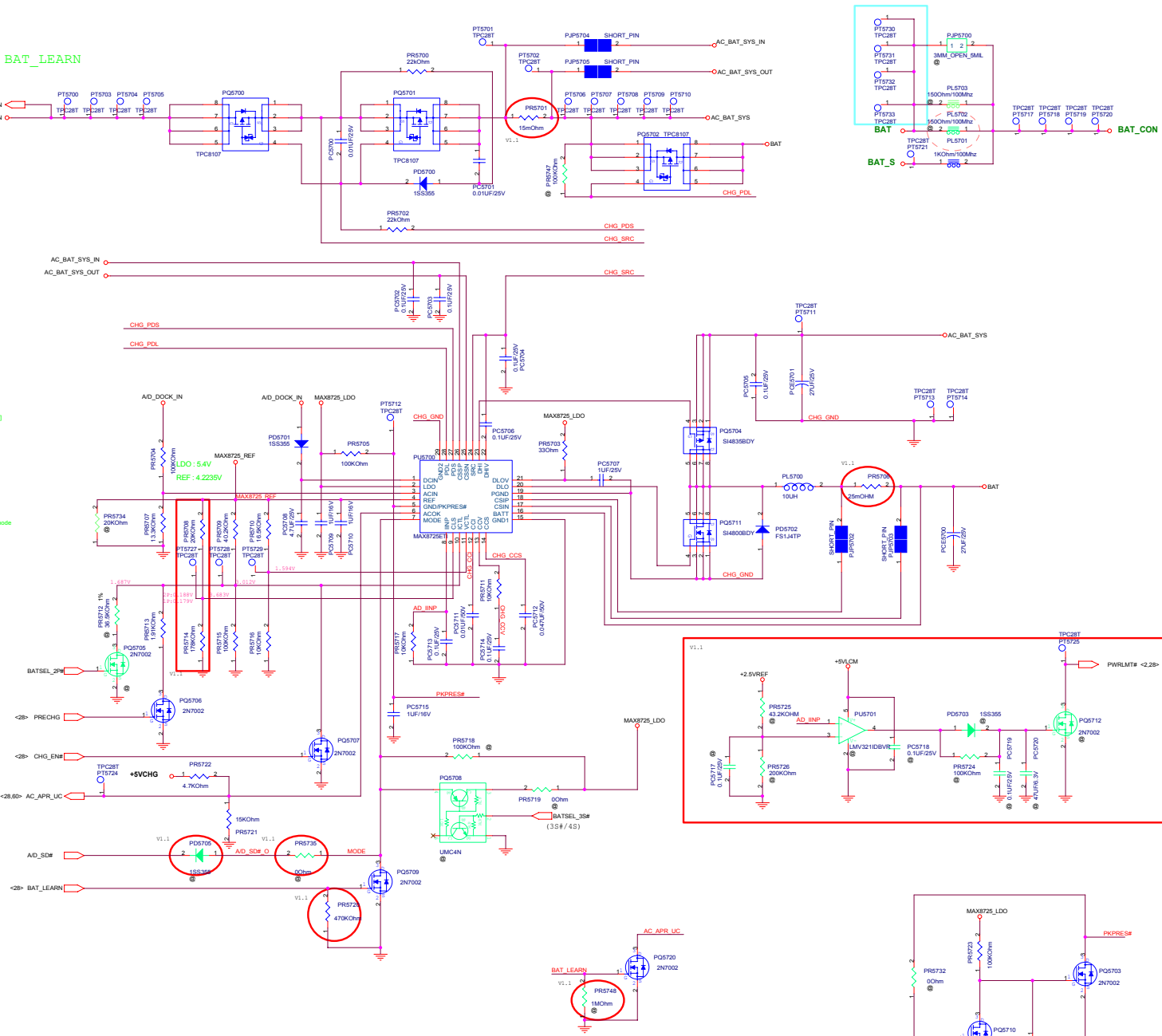






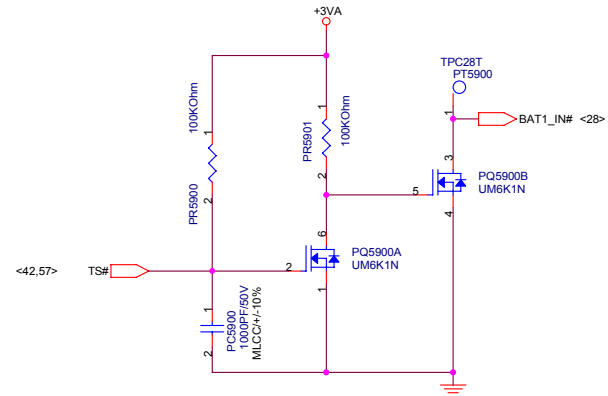


## POWER PATH & BAT LEARN

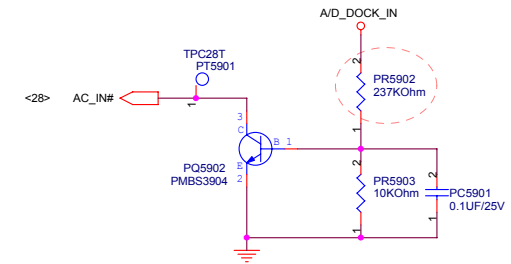




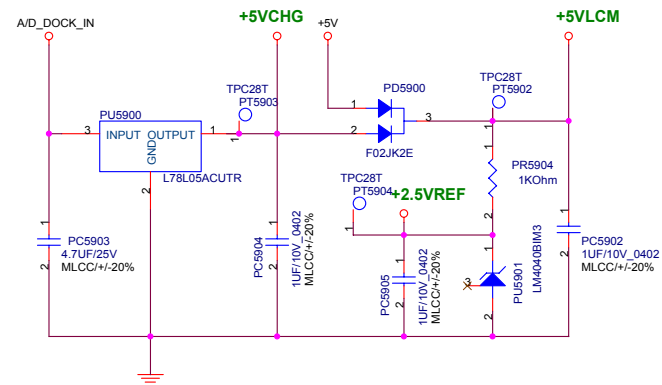
BATTERY IN DETECT



## ADAPTER IN DETECT

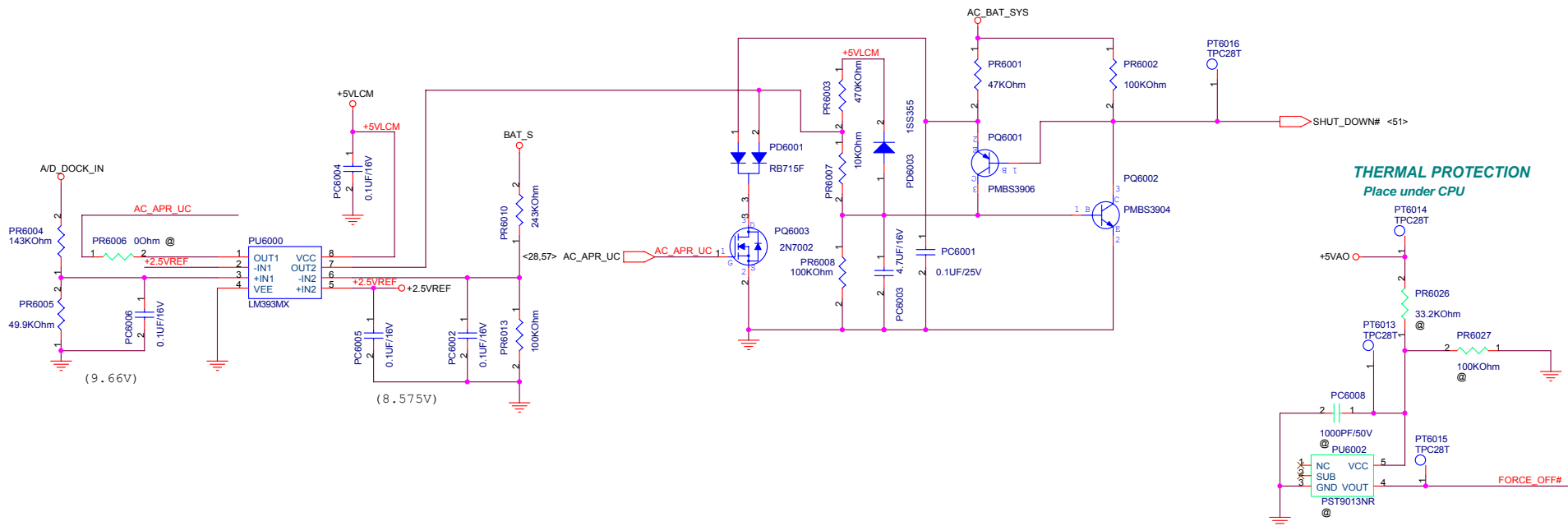


+5VLCM, +5VCHG & +2.5VREF

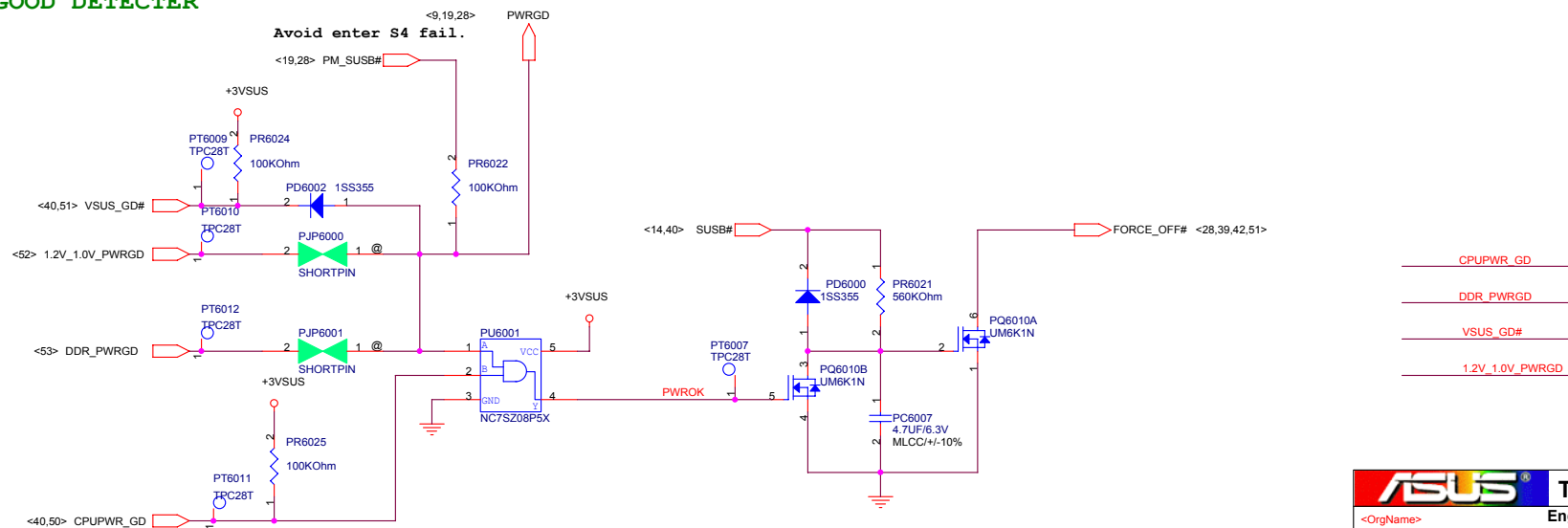


## V1.1

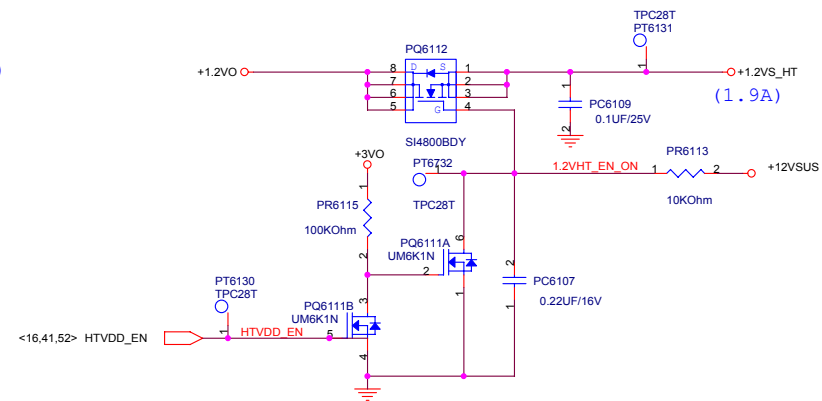
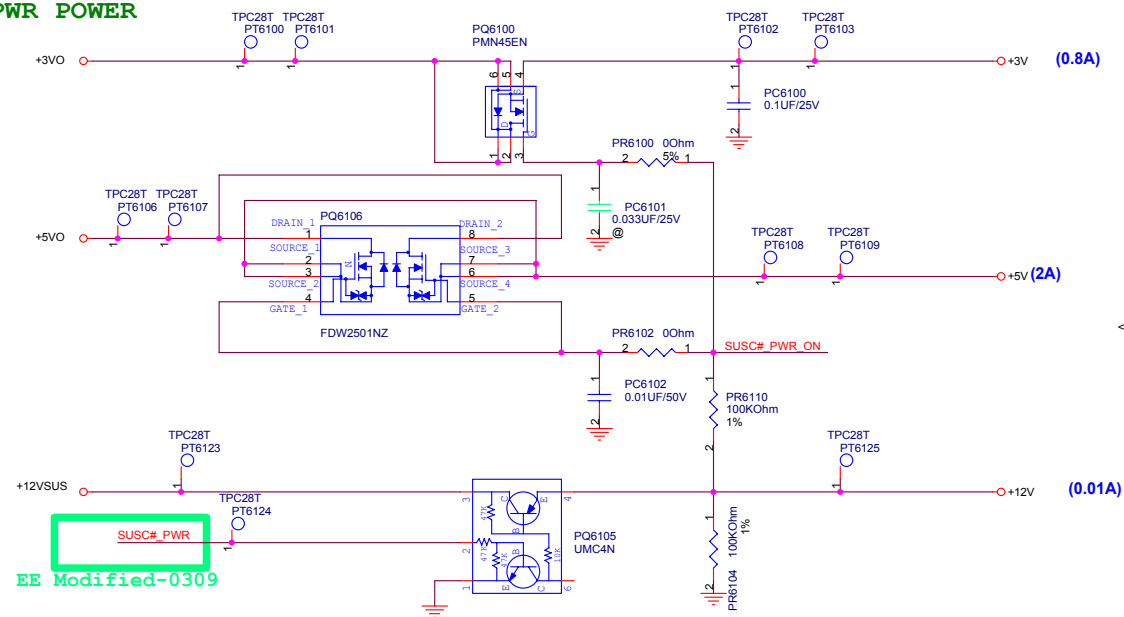
**THERMAL PROTECTION**  
Place under CPU



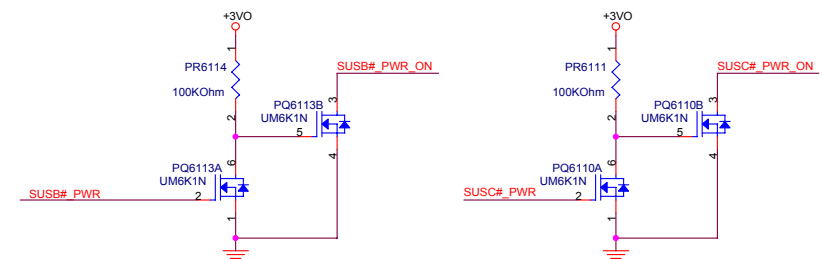
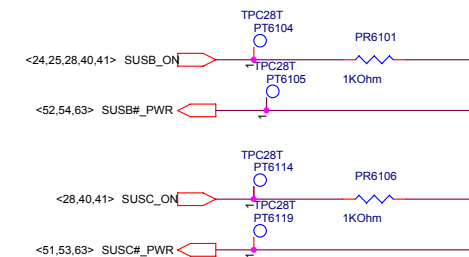
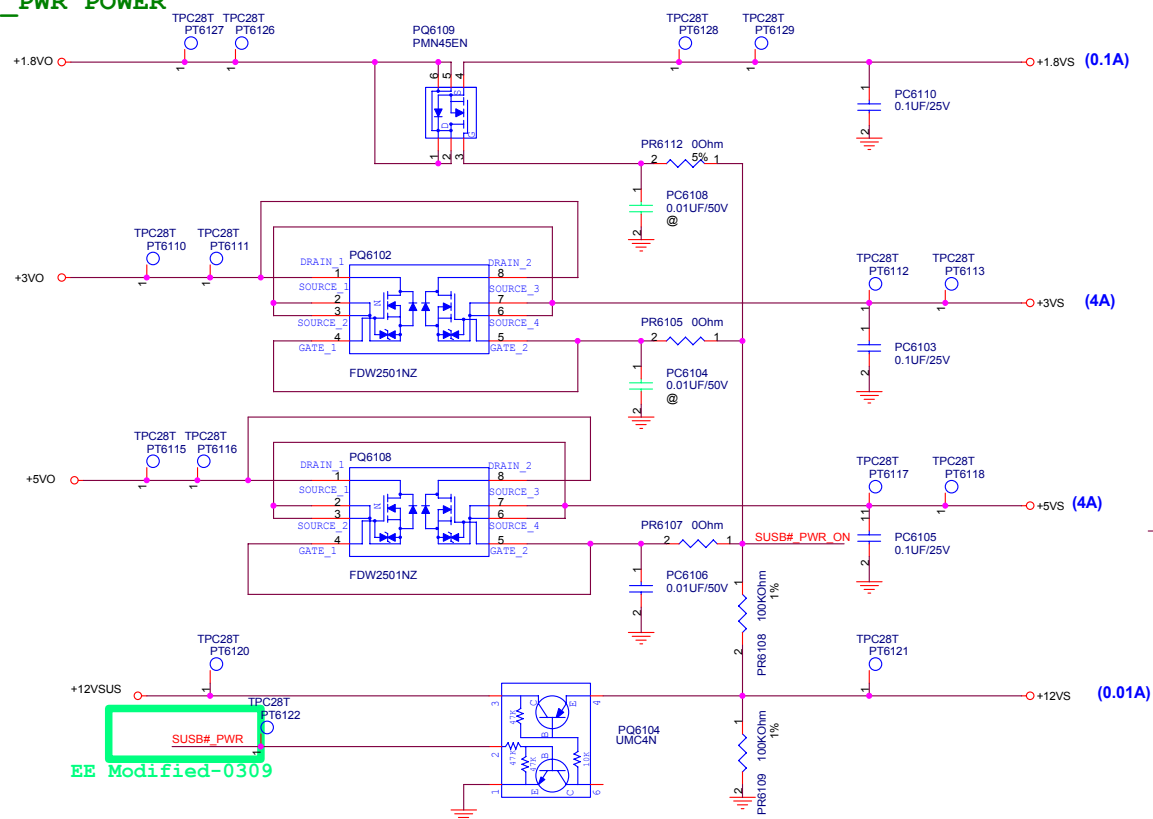
Avoid enter S4 fail.



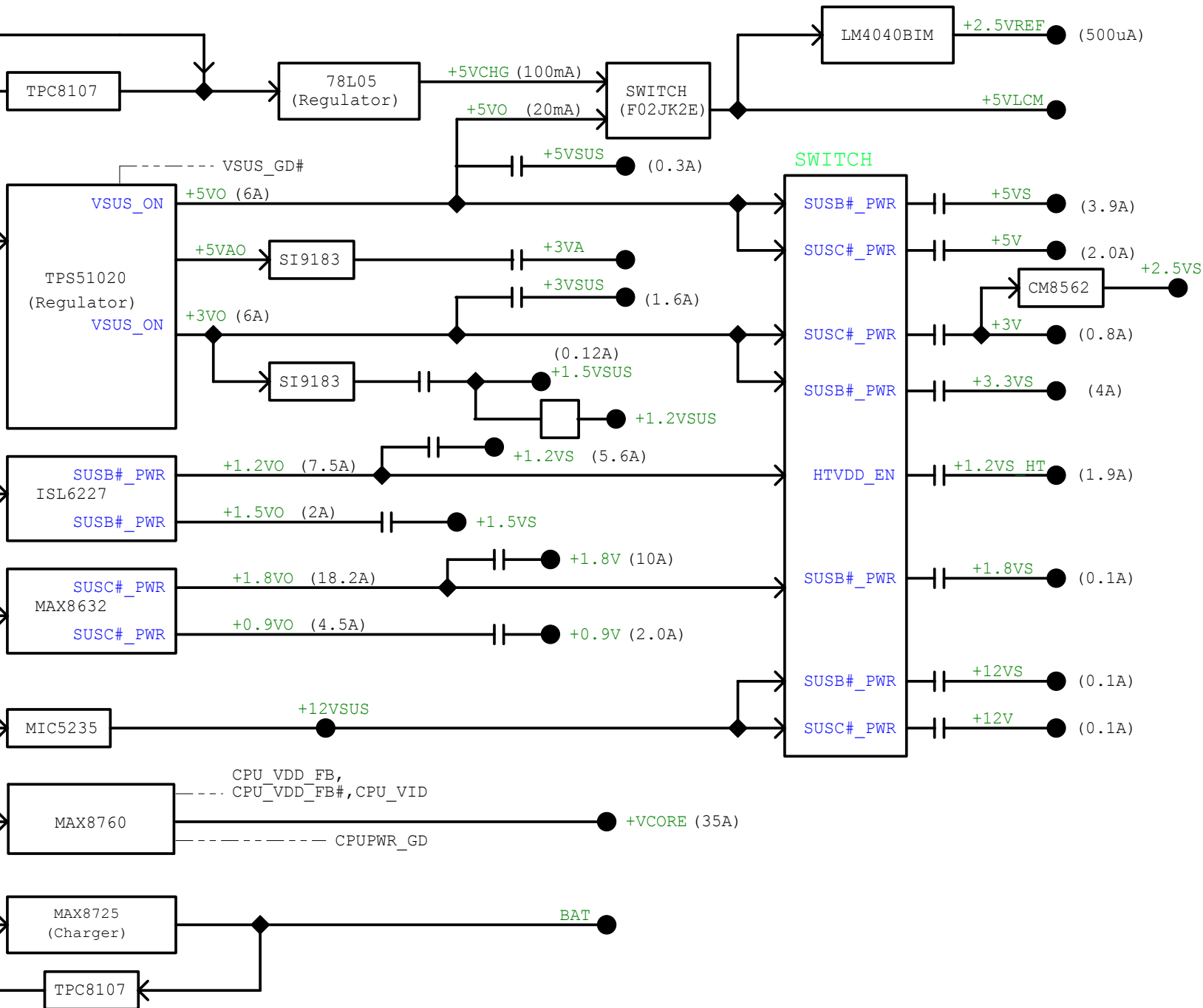
SUSC#	PWR	POWER
-------	-----	-------



SUSB#	PWR	POWER
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0
5	0	0
6	0	0
7	0	0
8	0	0
9	0	0
10	0	0
11	0	0
12	0	0
13	0	0
14	0	0
15	0	0
16	0	0
17	0	0
18	0	0
19	0	0
20	0	0
21	0	0
22	0	0
23	0	0
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27	0	0
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128	0	0
129	0	0
130	0	0
131	0	0
132	0	0
133	0	0
134	0	0
135	0	0
136	0	0
137	0	0
138	0	



A/D\_DOCK\_IN





FOR POWER TEST

