

ST-2 SWG LOGIC SCHEMATICS

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ST-2
VER0.1
August/12/2013

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80.DC/DC VCCCPUCORE(VT1334S)
81.BLANK
82.VCCCPUCORE DECOUPLING
83.DC/DC VCCGFXCORE_D (TPS51219)
84.BLANK
85.DC/DC VCC1R05AMT(VT384B)
86.DC/DC VCC1R35A(VT387B)
87.DC/DC VCC0R675B(TPS51200)
88.DC/DC VCC1R5VIDEO(VT382B)
89.DC/DC VCC1R05VIDEO_PLL(TPS74801)
90.BLANK
91.BLANK
92.DC/DC VCC1R5B(BU15TD2WNVX)
93.LOAD SW PCH SUS
94.LOAD SW LAN
95.LOAD SW VIDEO
96.LOAD SW B
97.BLANK
98.LOAD SW WWAN & WLAN
99.PTH FOR SCREW HOLES
100.3rd USB

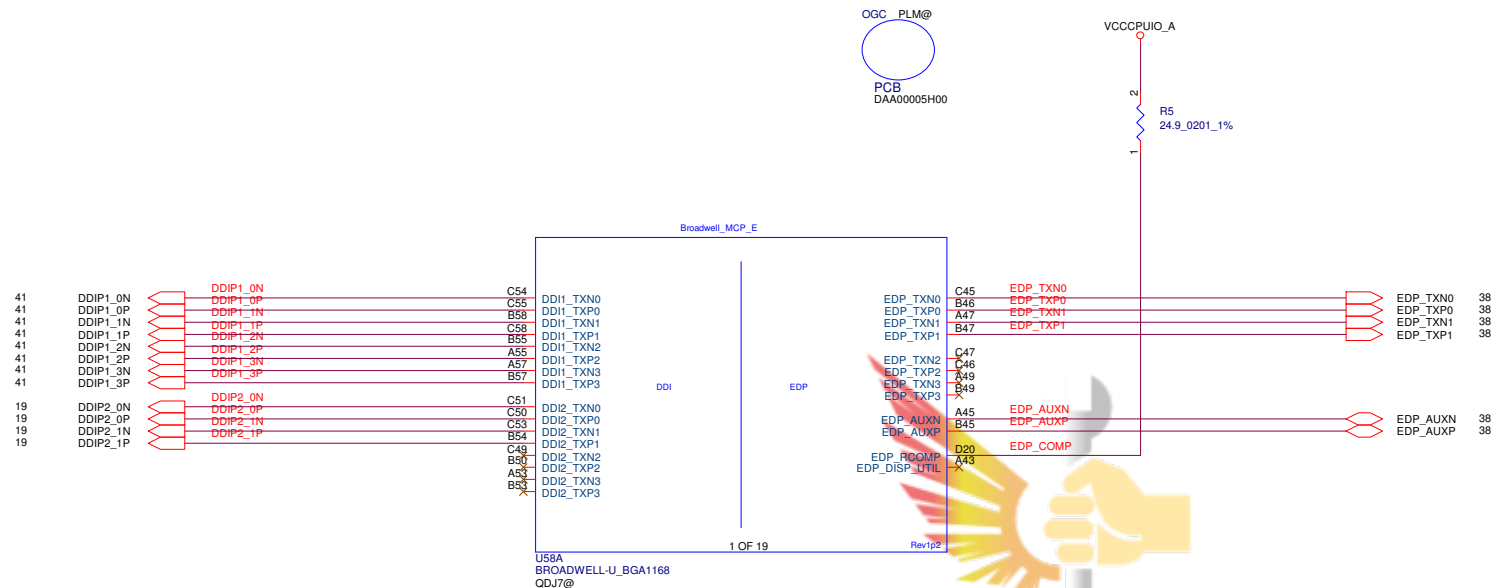
lenovo		
Project Name: ST-2 SWG	Title : TITLE PAGE	
Size : C	Document Number :	Rev : 0.24
Date: Thursday, December 18, 2014		Sheet : 1 of 100

EC Modify History

Date	EC version	File name
2013/8/28	ST-2_SWG_SDV_EC001-008	JV_ST-2_SWG_SDV_SCH_EC001-008_082801.pdf
2013/9/4	ST-2_SWG_SDV_EC009	JV_ST-2_SWG_SDV_SCH_EC001-009_090401.pdf



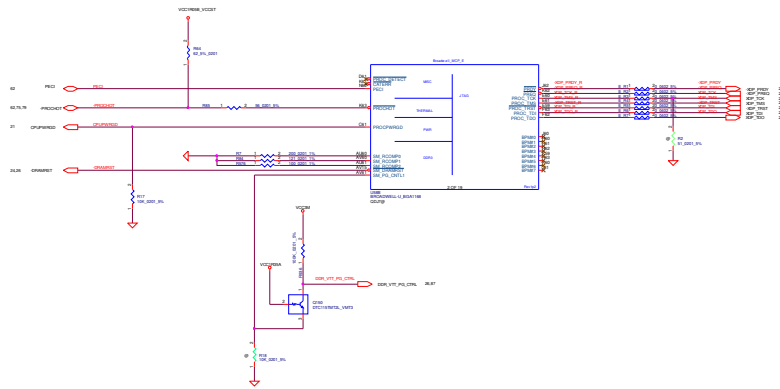
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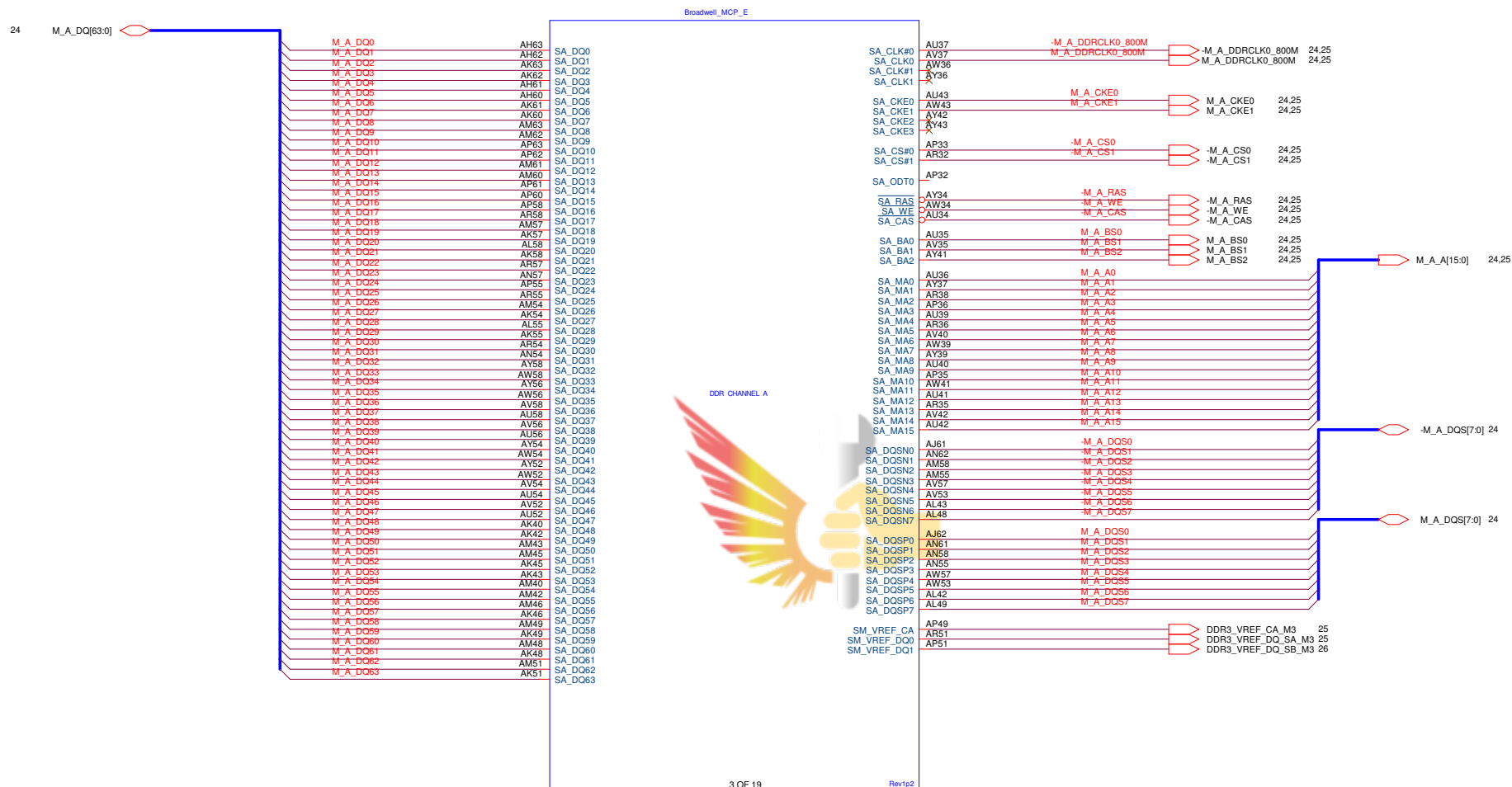


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Title		LA-XXXXP	
CPU(1/16) : DDI/EDP		Rev	0.1
Size	Document Number	LA-XXXXP	
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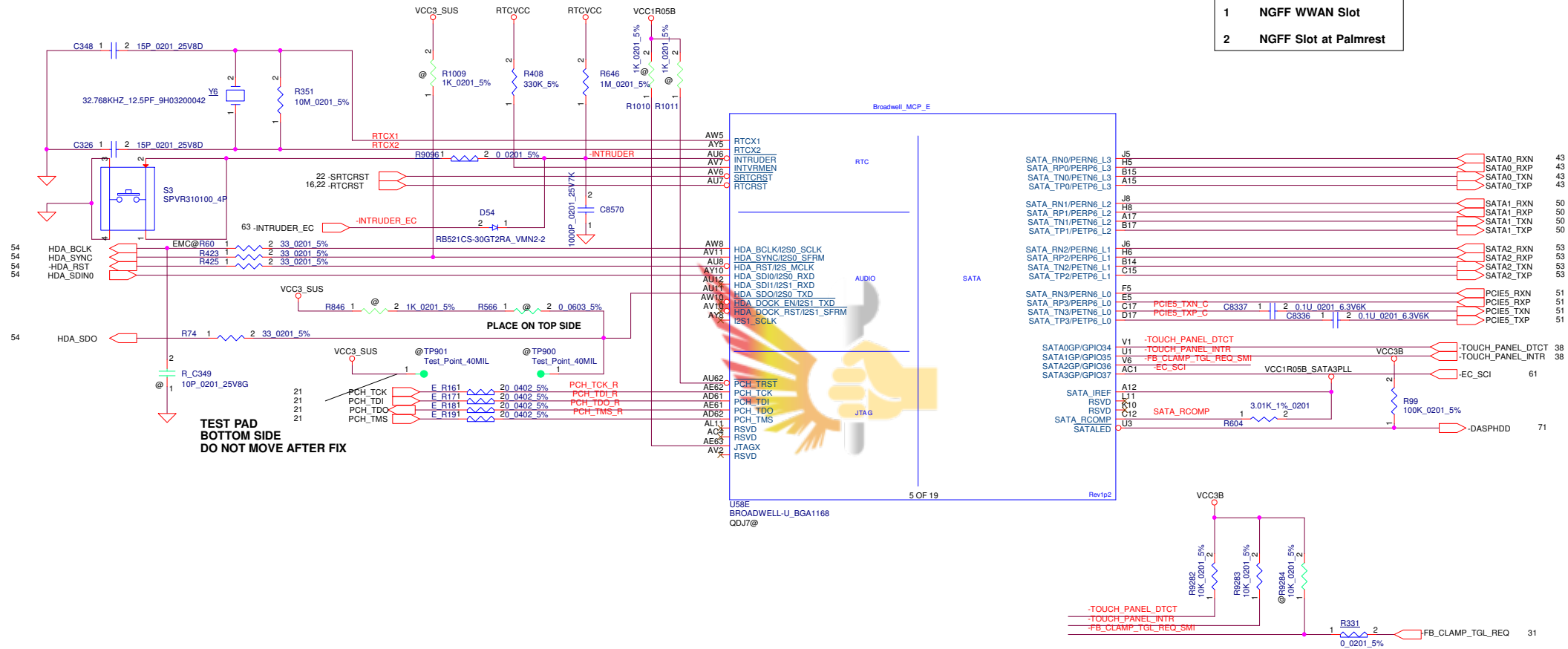



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BROADWELL-U_BGA1168
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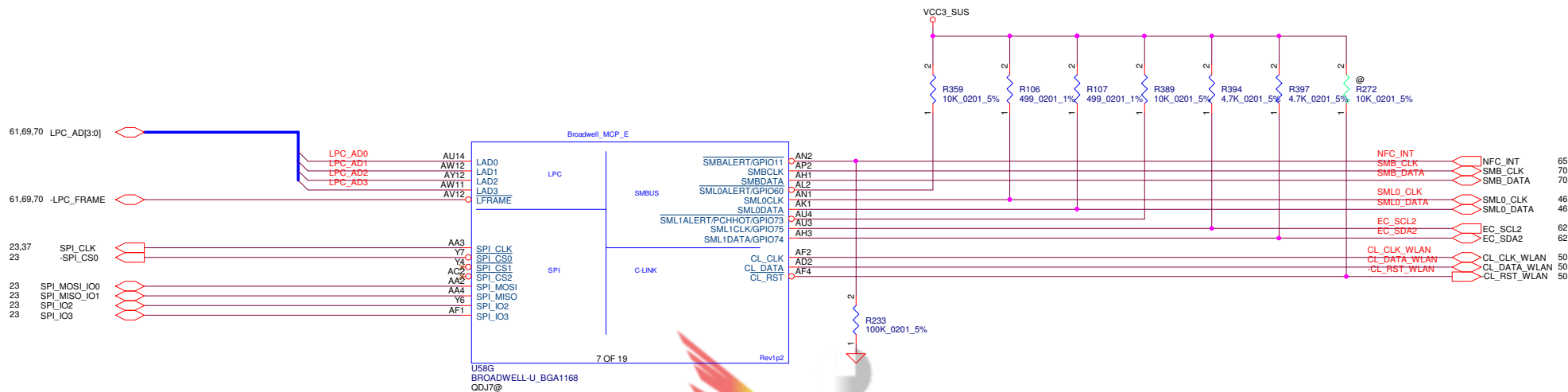
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CPU(3/16) : DDR3L CHANNEL-A		Rev	0.1
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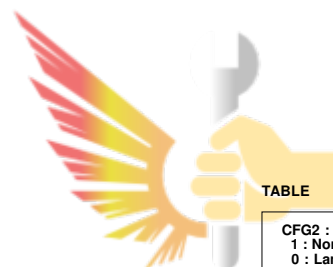
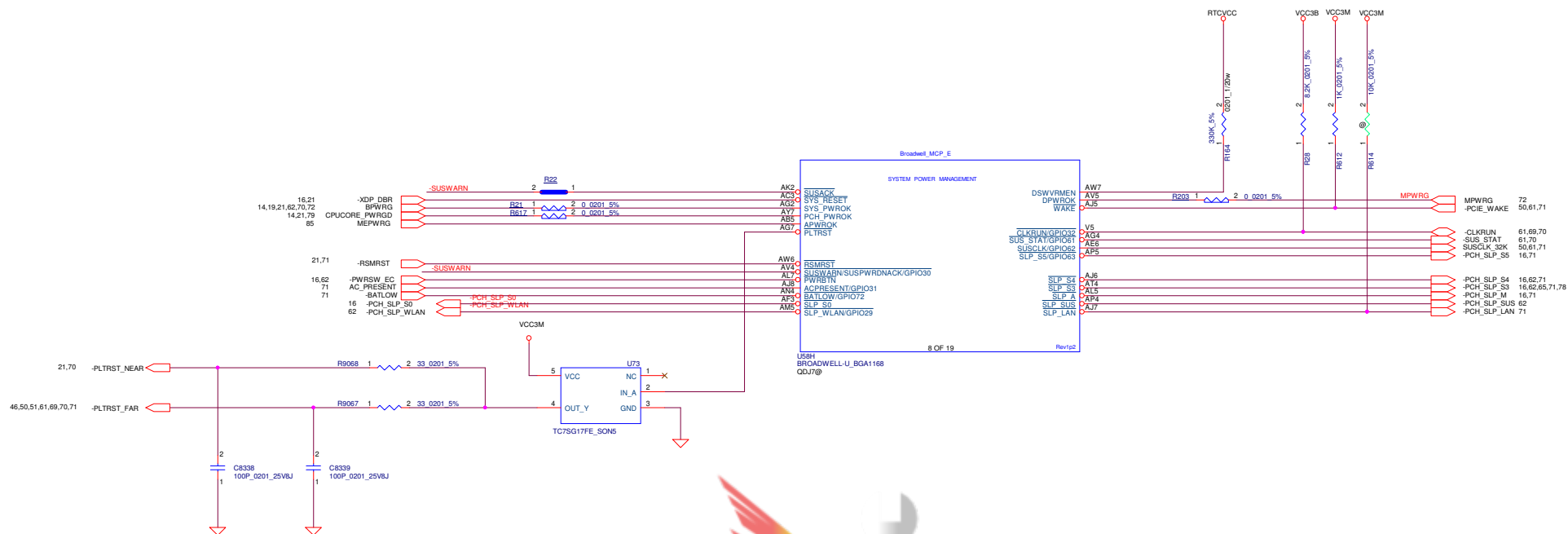
SATA Port Assignment	
0	HDD Connector
1	NGFF WWAN Slot
2	NGFF Slot at Palmrest



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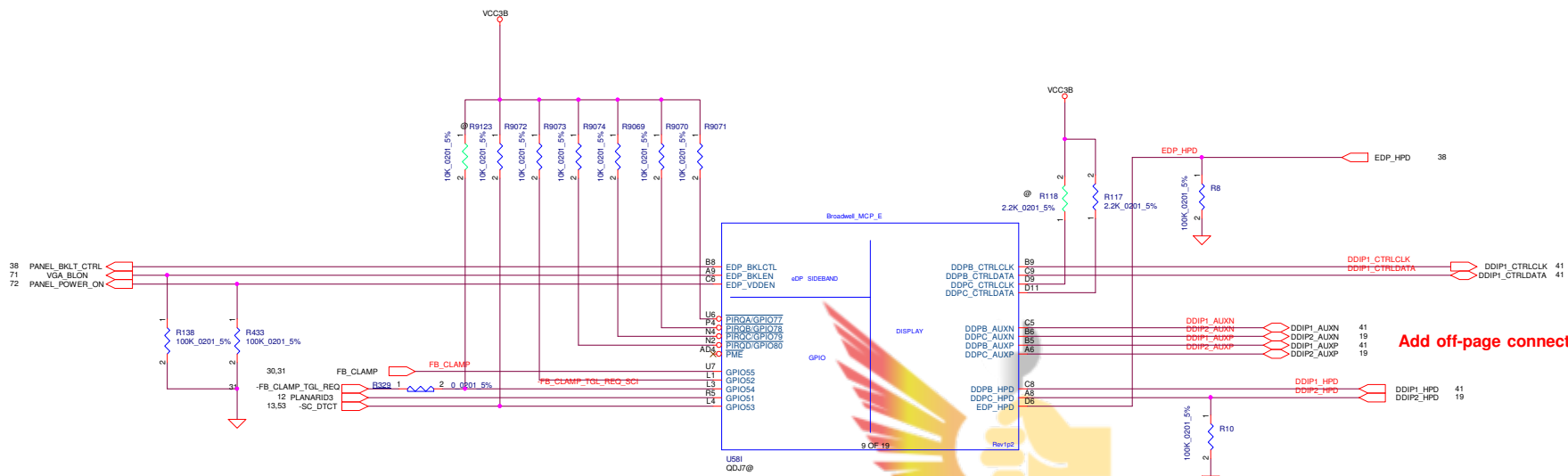
TABLE


CFG2 : PEG Static Lane Reversal
 1 : Normal Operation
 0 : Lane Reversal

CFG4 : Display Port Presence
 1 : Disabled
 0 : Enabled

CFG[6:5] : PEG Bifurcation
 11 : Func 1 Disabled, Func 2 Disabled (x16,---,---)
 10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---)
 01 : Func 1 Disabled, Func 2 Enabled
 00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

CFG7 : PEG Defer Training
 1 : PEG Train Immediately Following XXRESETB Deassertion
 0 : PEG Wait for BIOS for Training



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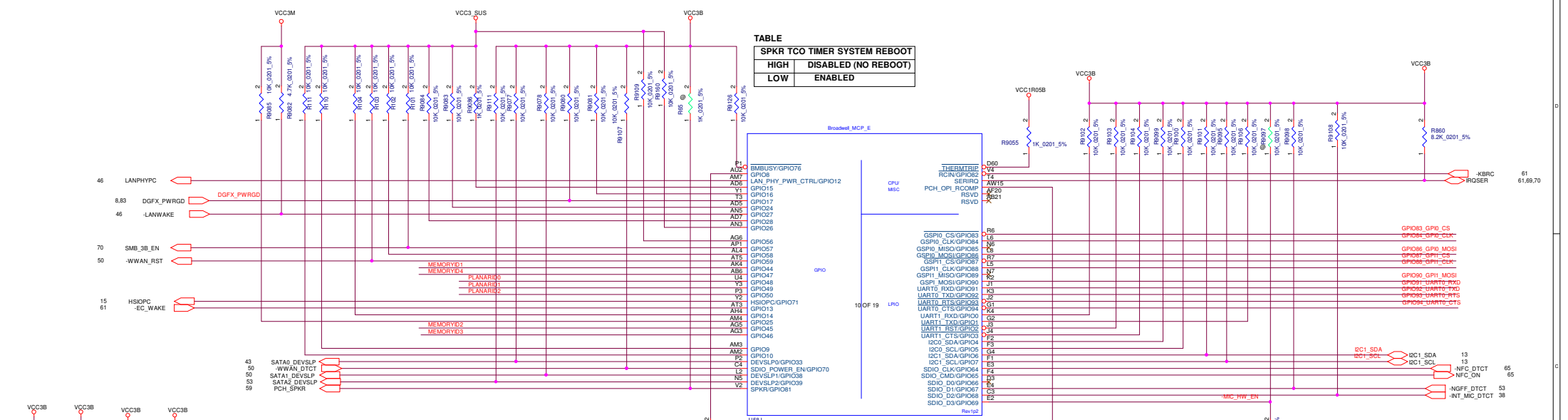
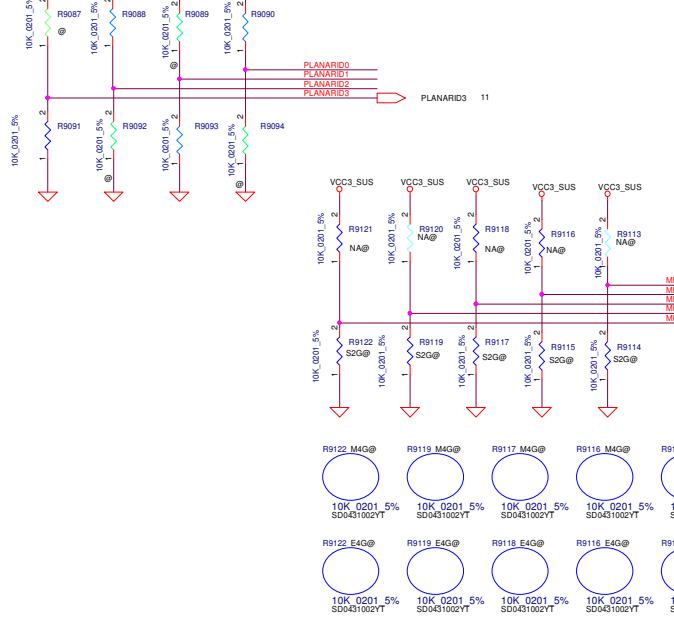
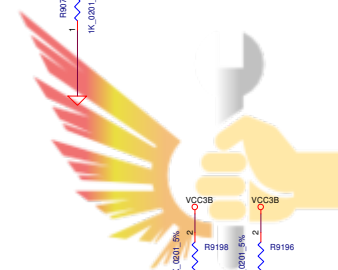


TABLE		
SPKR TCO TIMER SYSTEM REBOOT		
HIGH	DISABLED (NO REBOOT)	
LOW	ENABLED	



PLANAR ID TABLE	
LEVEL	PLANARID[3..0]
SDV	0000B
SDV2	0001B
FVT	0010B
FVT2	0011B
SIT	0100B
SVT	0101B



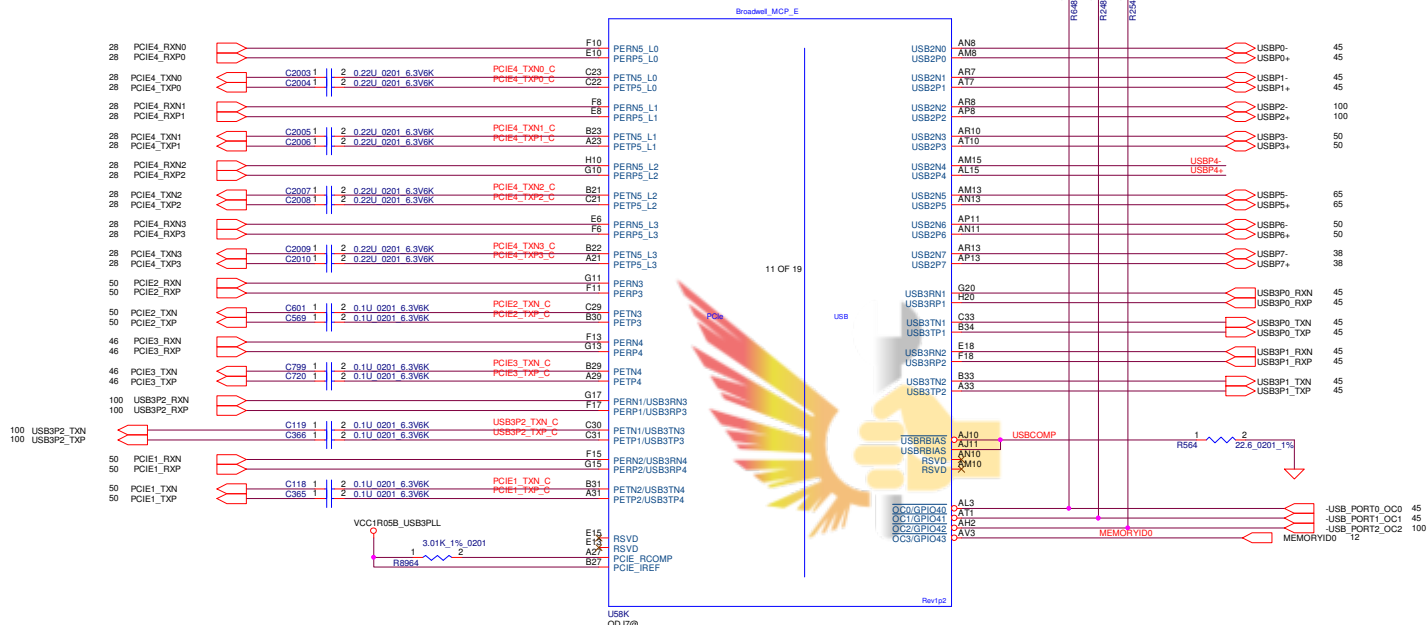
MemoryID0	MemoryID1	MemoryID2	MemoryID3	MemoryID4	Supplier	Density	P/N	BOM Structure
GPIO43#	GPIO44	GPIO45	GPIO46	GPIO47				
1	0	0	0	0	Samsung	8Gb	K4B8G1646Q-MYK0	S4G@
1	1	0	0	0	Micron	8Gb	MT41K512M16TNA-125:E	M4G@
1	1	1	0	0	Elpida	8Gb	EDJ8416E6MB-GN-F	E4G@
1	1	1	1	0	SK Hynix	8Gb	H5TC8G63AMR-PBA	H4G@
1	1	1	1	1	no on-board memory model	N/A	N/A	NA@

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Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2	USB3 2	USB3P1
Port 3	PCIE 1/USB3 3	USB3 3	USB3P2
Port 4	PCIE 2/USB3 4	PCIE 2	PCIE1
Port 5	PCIE 3	PCIE 3	PCIE2
Port 6	PCIE 4	PCIE 4	PCIE3
Port 7	PCIE 5 L0	PCIE 5 L0	PCIE4_0
Port 8	PCIE 5 L1	PCIE 5 L1	PCIE4_1
Port 9	PCIE 5 L2	PCIE 5 L2	PCIE4_2
Port 10	PCIE 5 L3	PCIE 5 L3	PCIE4_3
Port 11	PCIE 6 L0	PCIE 6 L0	PCIE5
Port 12	SATA 2/PCIE 6 L1	SATA 2	SATA2
Port 13	SATA 1/PCIE 6 L2	SATA 1	SATA1
Port 14	SATA 0/PCIE 6 L3	SATA 0	SATA0

Update PCIe Port Assignment.

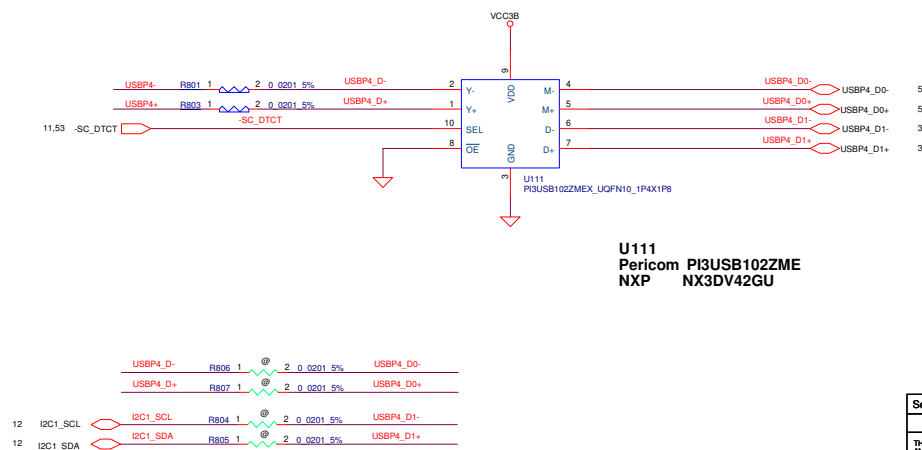
PCIe Port Assignment	
1	NGFF WLAN Slot Port1
2	NGFF WLAN Slot Port0
3	GbE PHY
4	(x4) Discrete GPU
5	(x1) Media Card Controller



USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	USB3.0 System Port (3rd USB)
3	NGFF WWAN Slot
4	Smart Card Slot/Touch panel
5	Fingerprint Reader
6	NGFF WLAN Slot
7	USB Camera

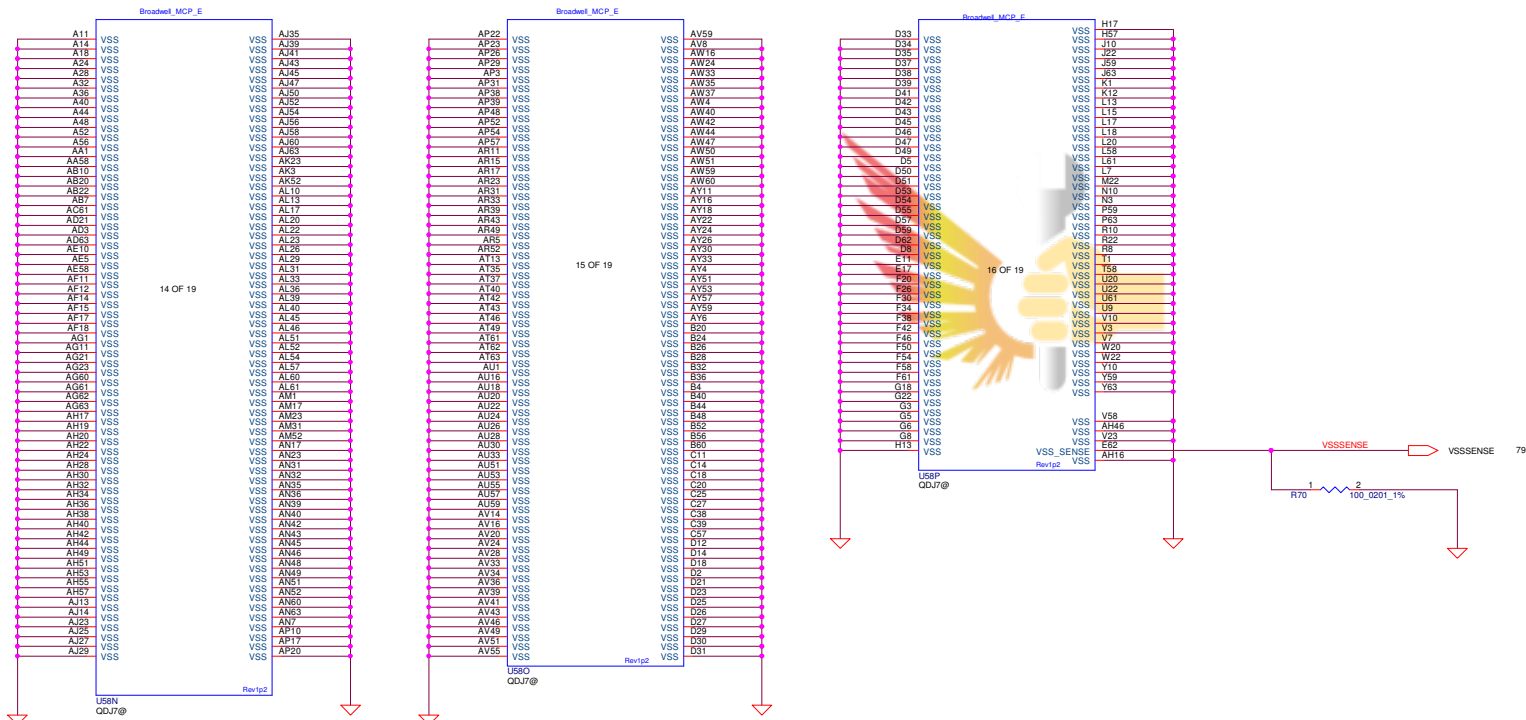
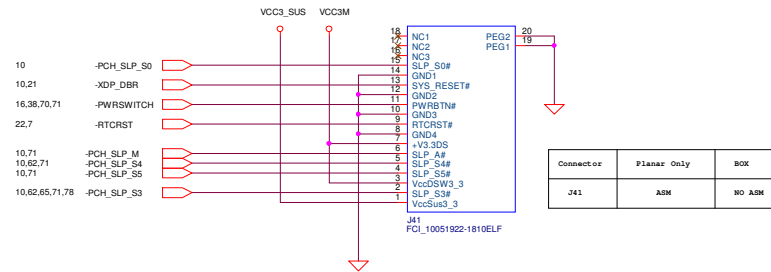
USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	USB3.0 System Port (3rd USB)


Device Selection	
0	Smart Card Slot
1	Touch Panel

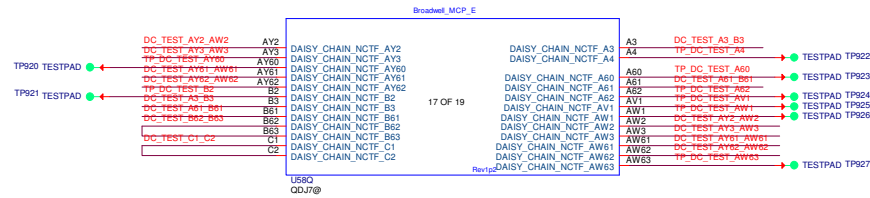



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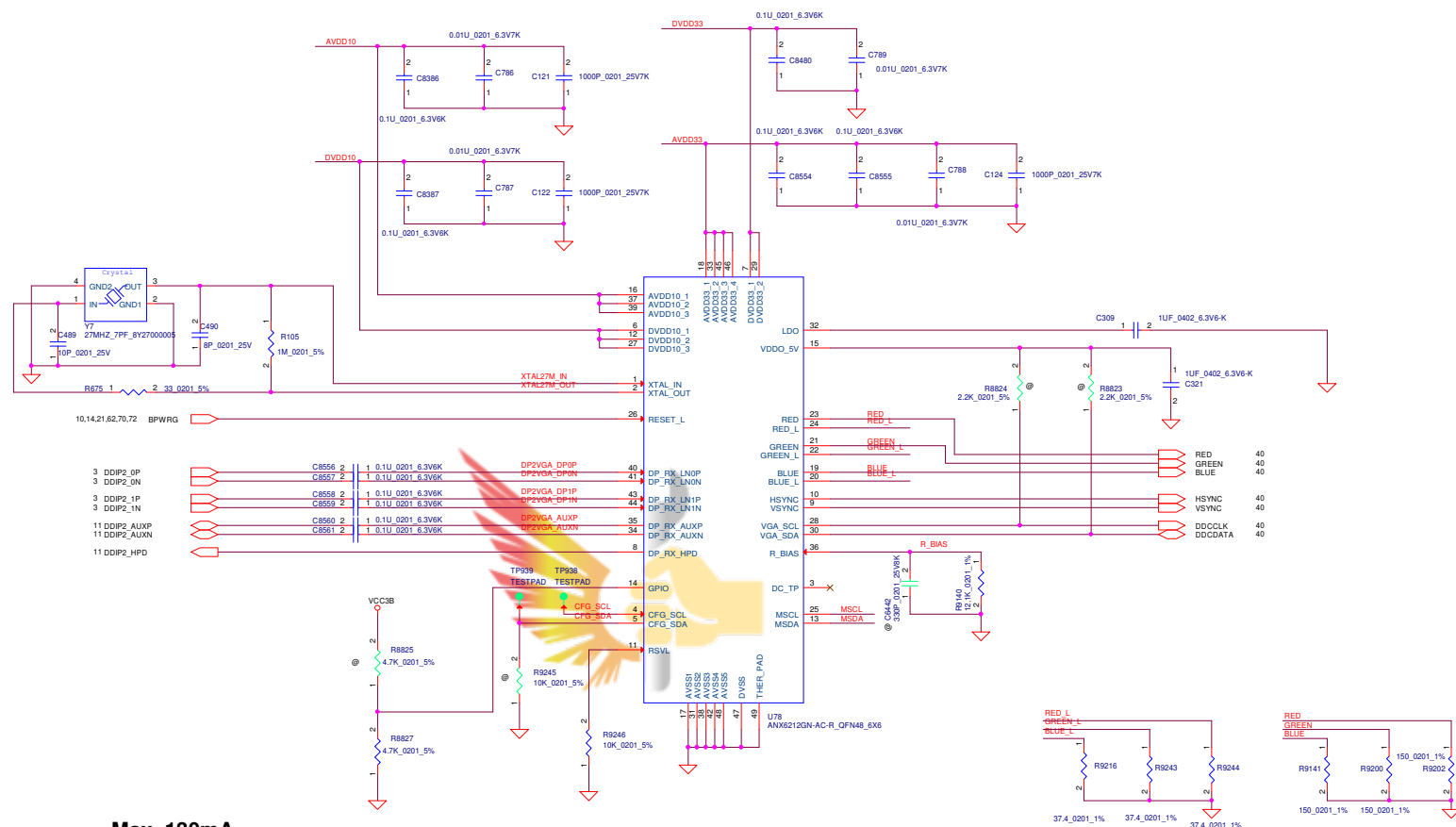
APS/PETS Interface



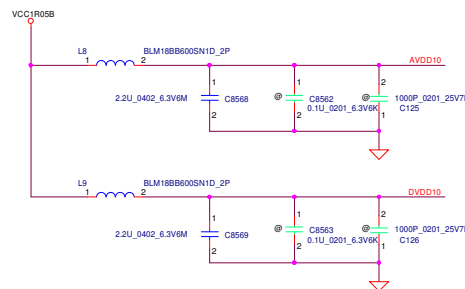
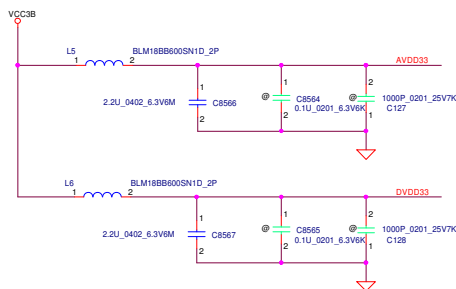
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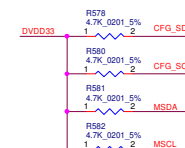
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Max 130mA




2.2uF, 0.1uF, 1000pF: Near filter



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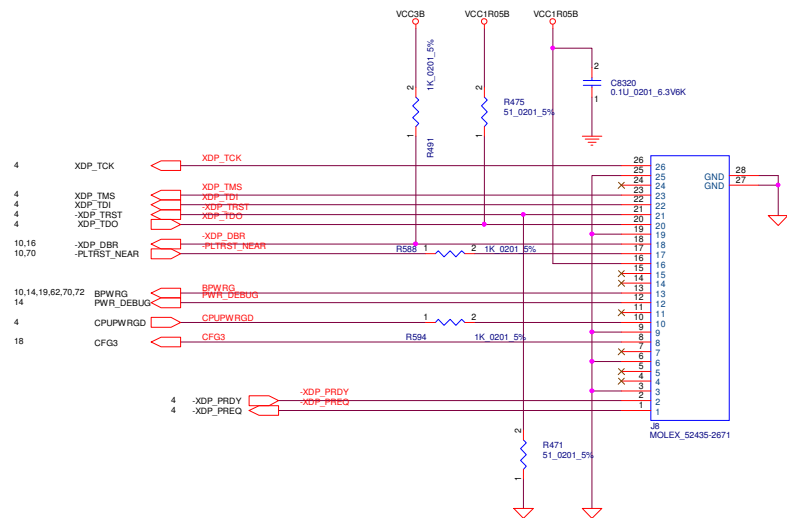


TABLE : CPU ITP DEBUG PORT

SIGNAL	REF DES	Planar Only	BOX
TDO	R475	ASM	ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	ASM
PWRGD	R594	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

NOTE : APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

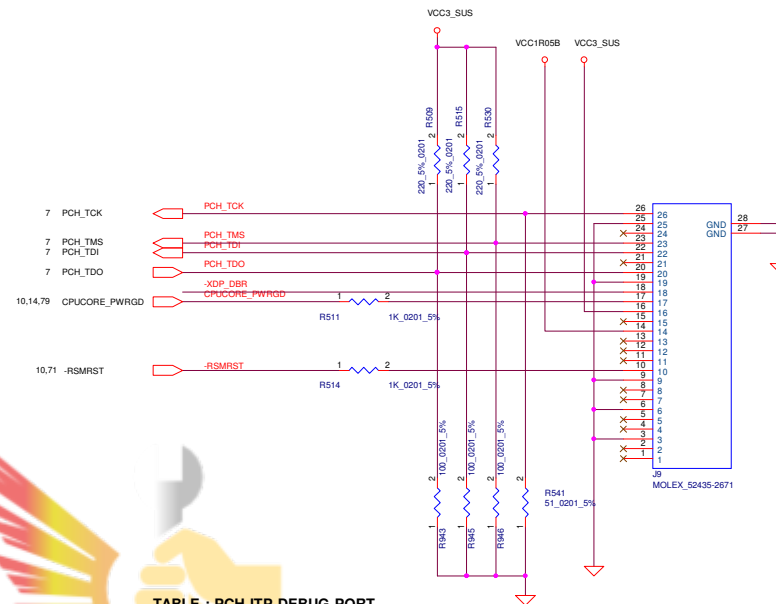
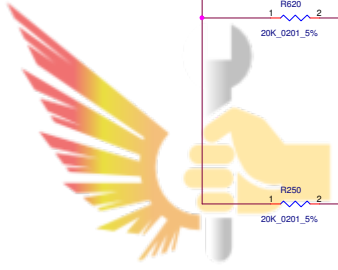
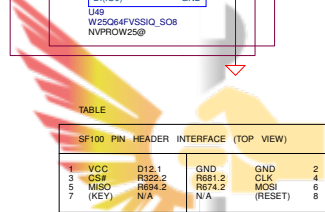


TABLE : PCH ITP DEBUG PORT

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R509	ASM	ASM
	R943	ASM	ASM
	R530	ASM	ASM
TMS	R946	ASM	ASM
	R515	ASM	ASM
TDI	R945	ASM	ASM
TCK	R541	ASM	ASM
CPUCORE_PWRGD	R511	ASM	ASM
-RSMRST	R514	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

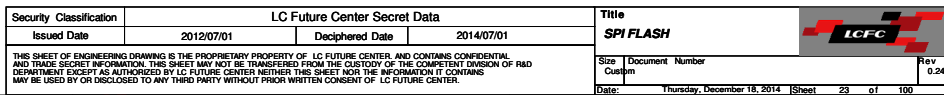
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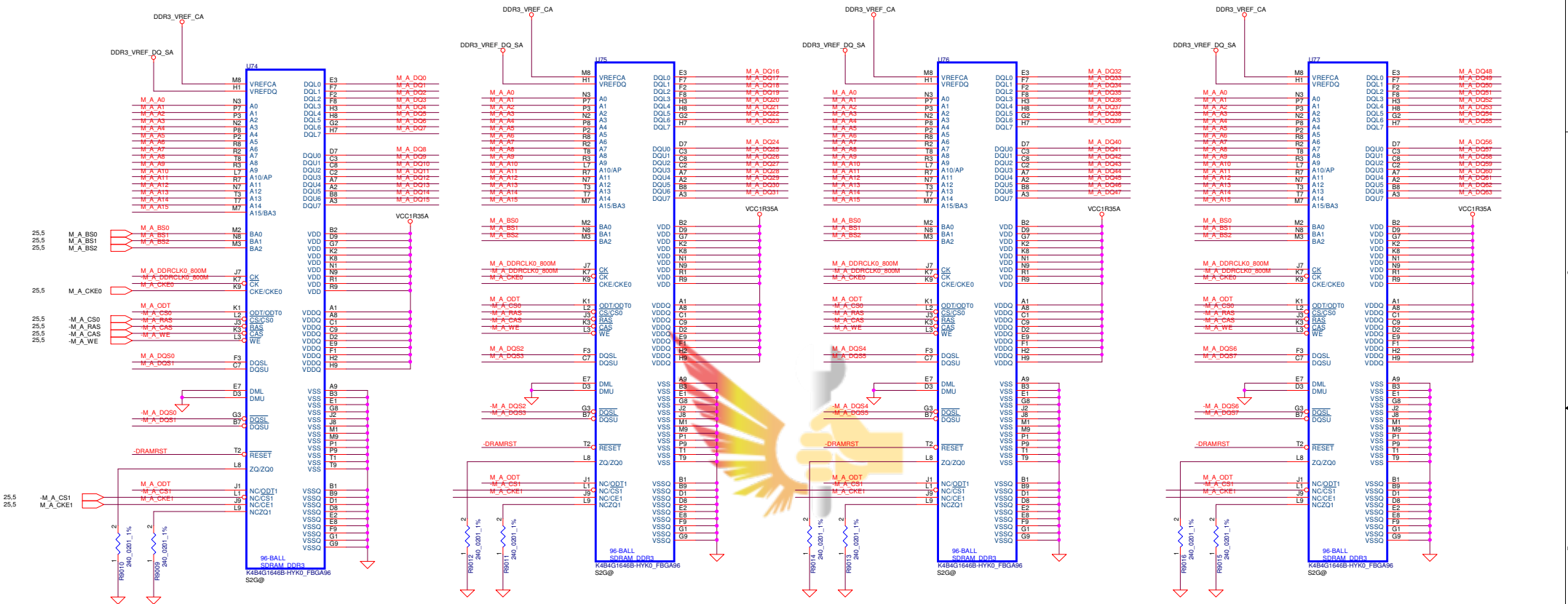


1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

vPro Model (16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12875FM2I-10G
MICRON	N25Q128A13ESEC0F



5 M_A_DQ[63:0]
5 -M_A_DQS[7:0]
5 M_A_DQS[7:0]
25.5 M_A_A[15:0]



25.5 M_A_DDRCLK0_800M M_A_DDRCLK0_800M

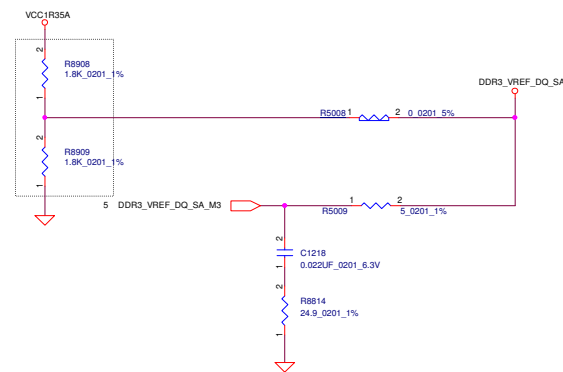
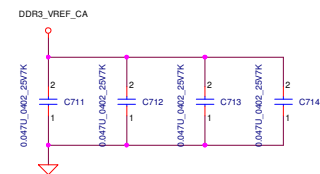
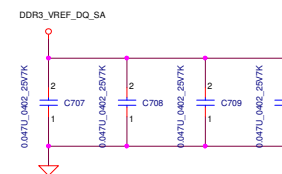
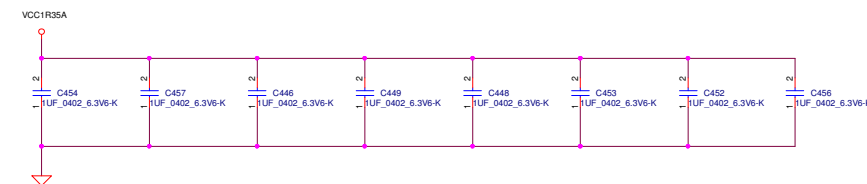
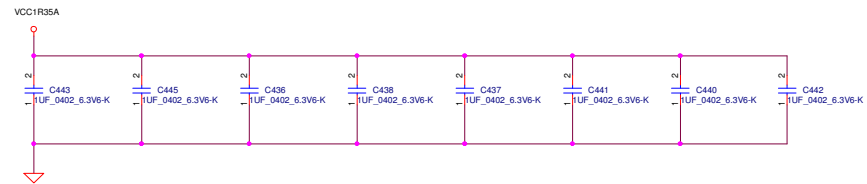
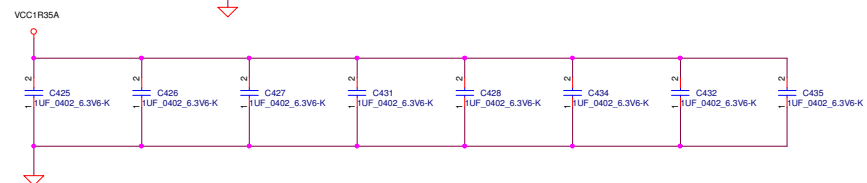
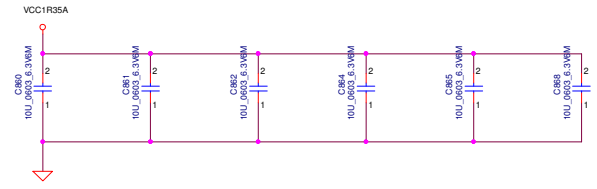
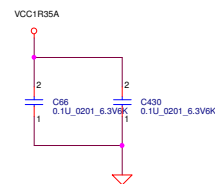
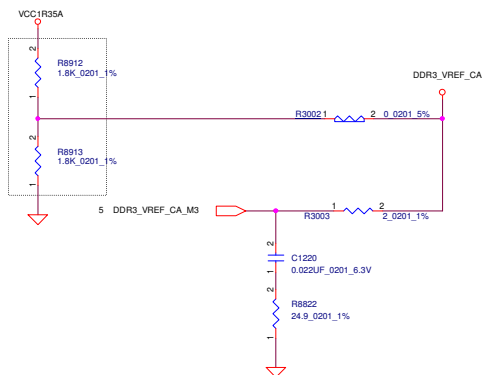
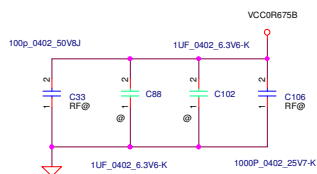
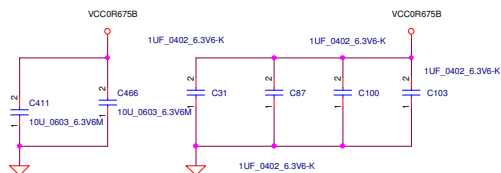
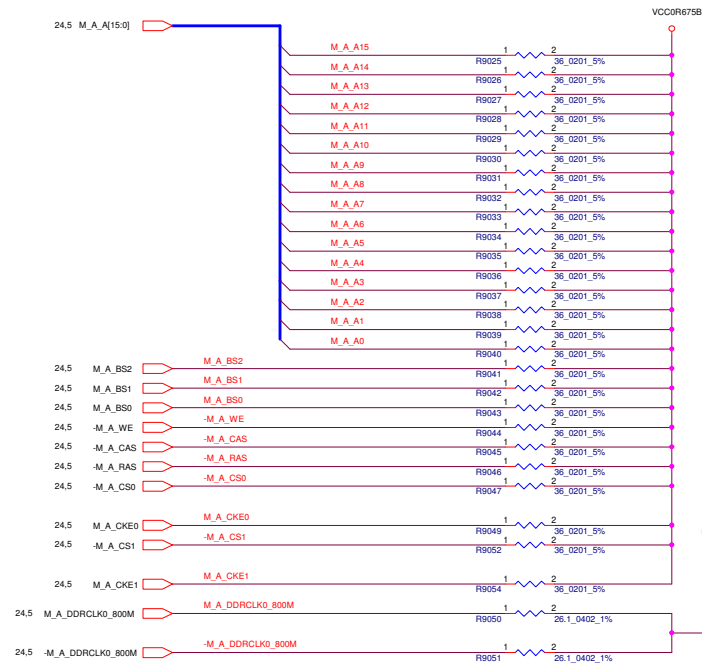
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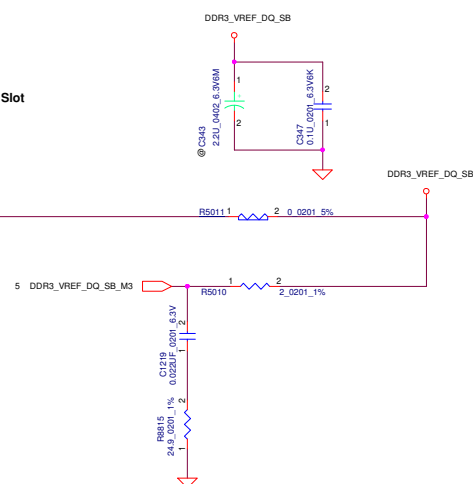
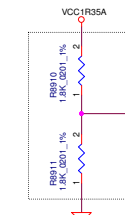
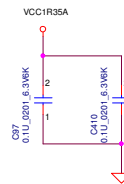
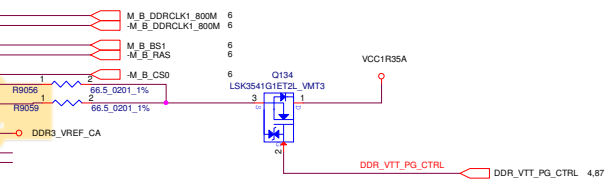
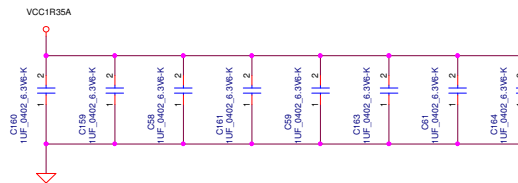
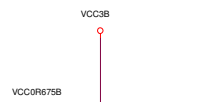
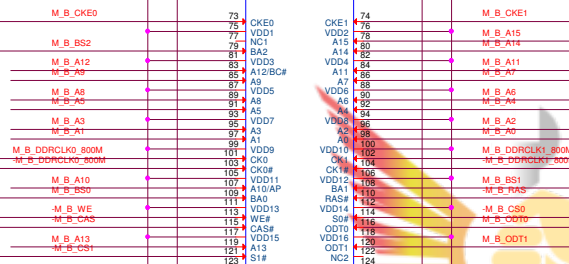
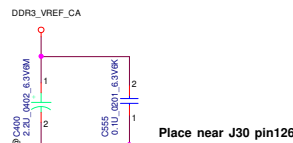
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				Date:	Thursday, December 18, 2014 (Sheet 24 of 100)



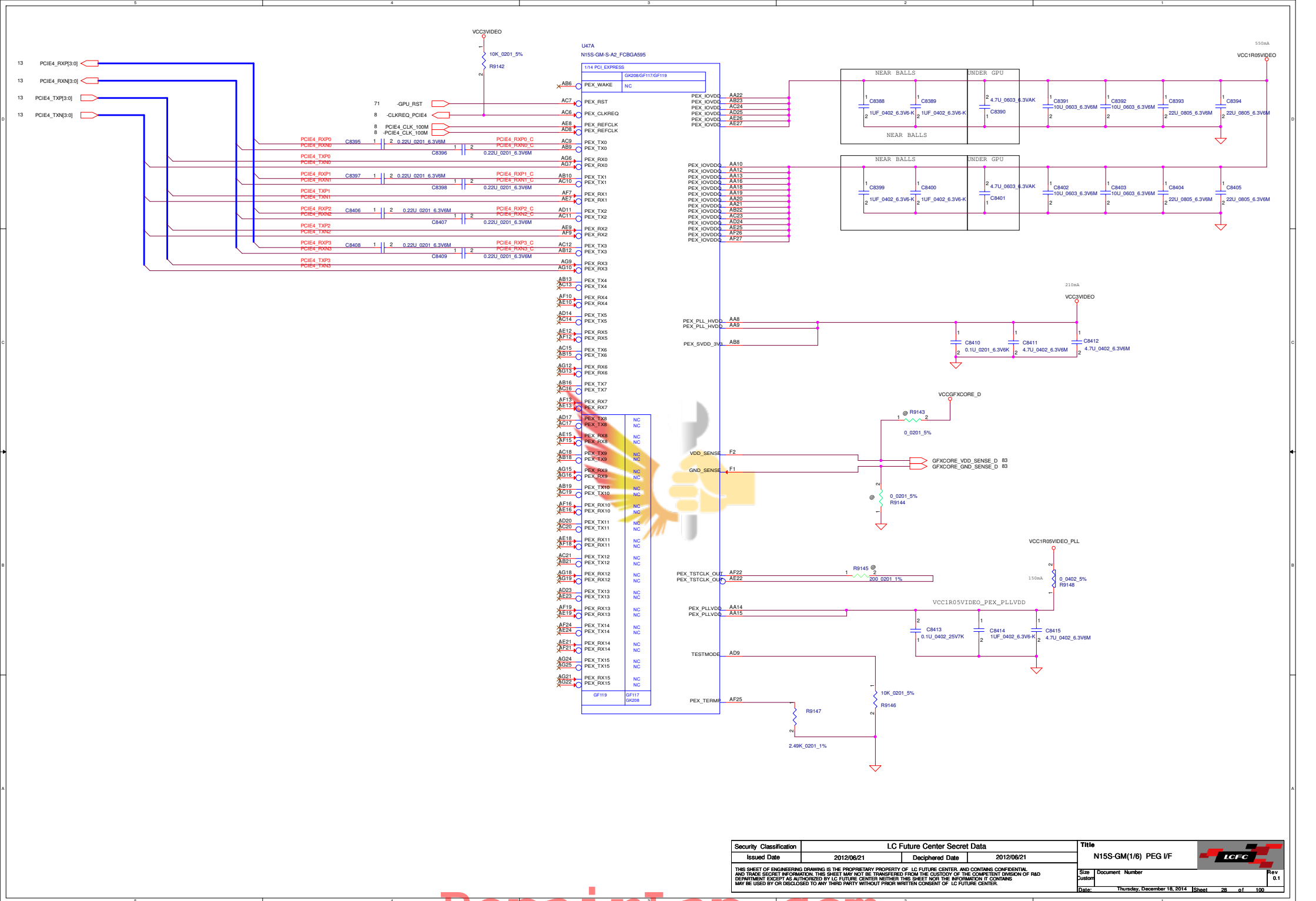
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Size		Document Number		Rev					
Date		Thursday, December 18, 2014		Sheet		25 of 100		0.1	

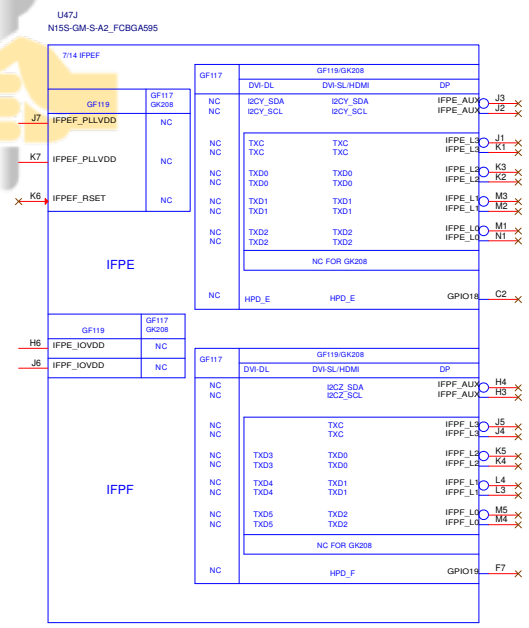
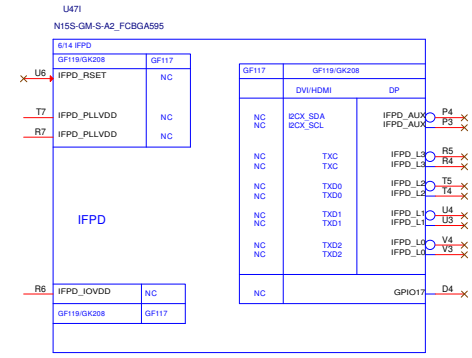
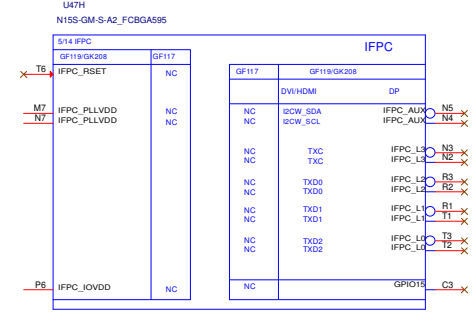
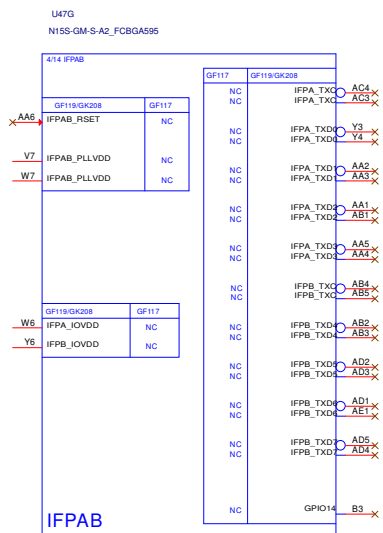


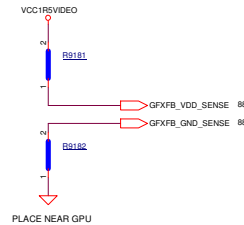
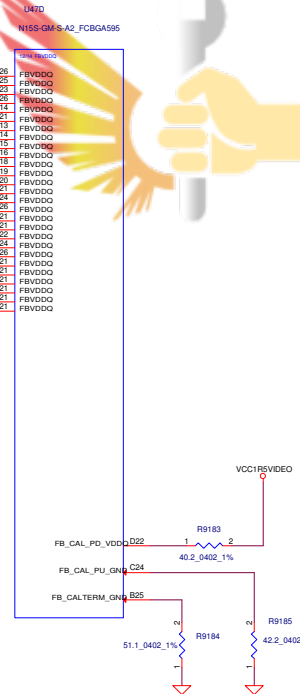
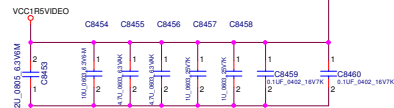
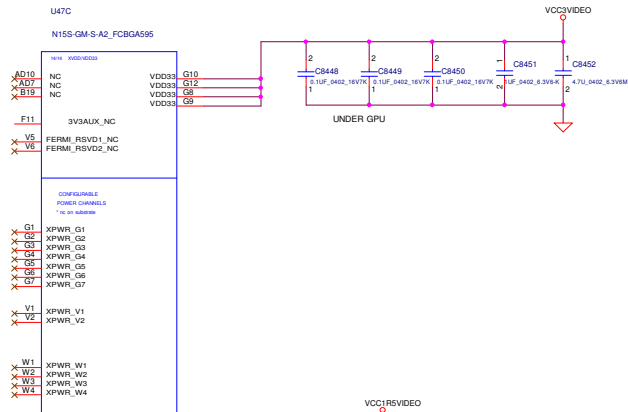
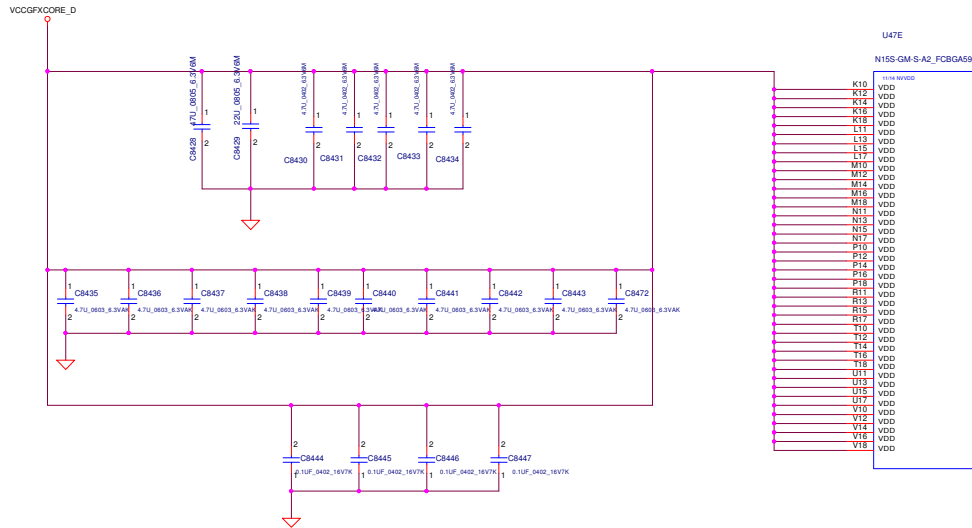
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2012/06/21		2012/06/21		SHN-5 SHB SWG			
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				Sheet		26 of 100	



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				Rev 0.1	
Size				Document Number	Date
Thursday, December 18, 2014				Sheet 27 of 100	

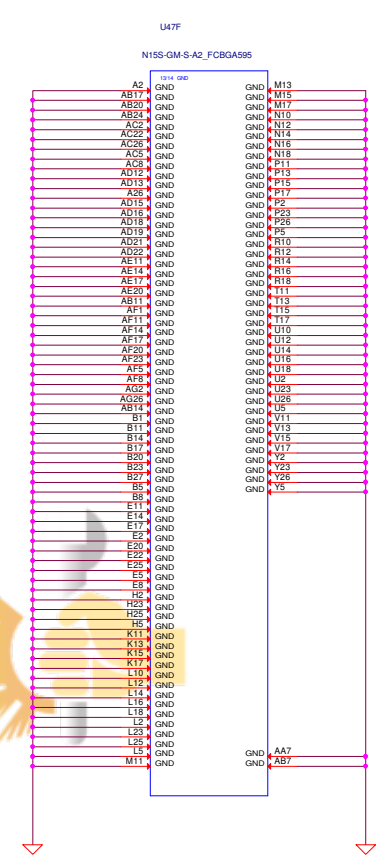
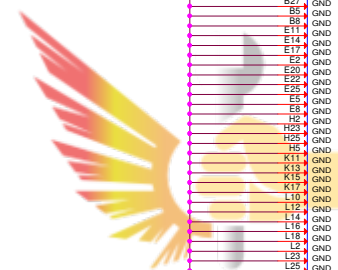






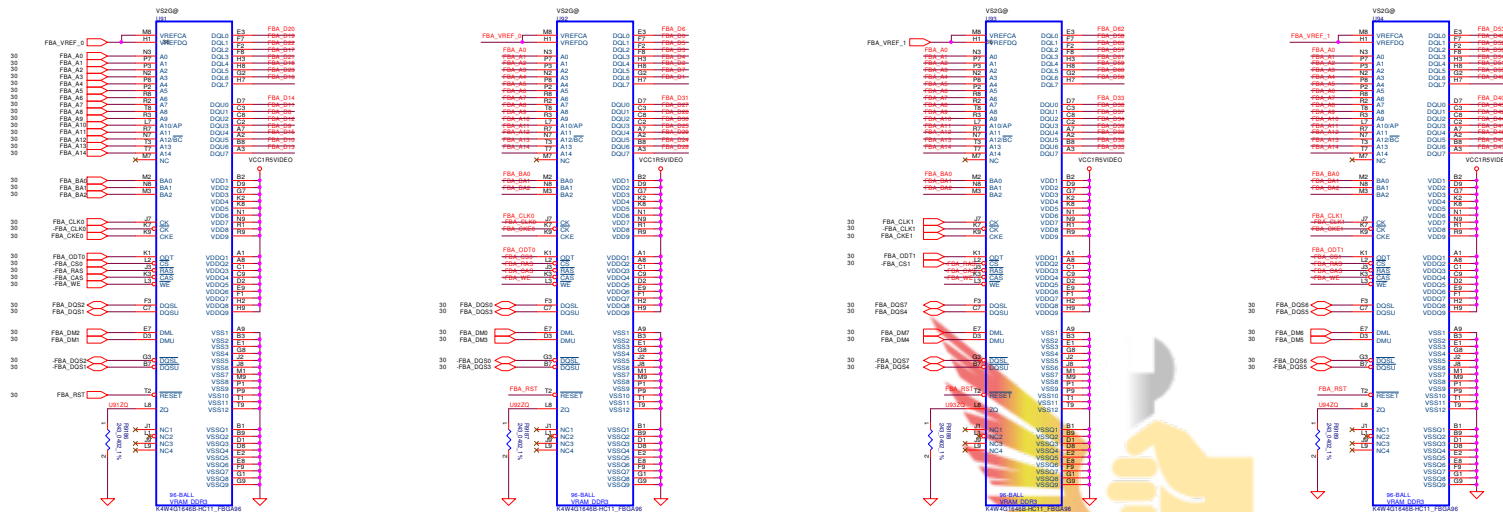
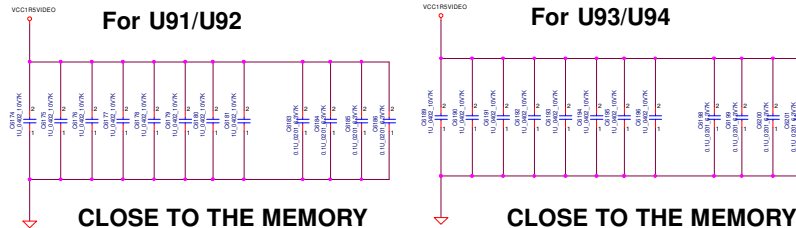
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Issued Date	2012/06/21	Deciphered Date	2012/06/21	N15S-GM(5/6) POWER	
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Custom			8.1		
Date:	Thursday, December 18, 2014	Sheet	32	of	100

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BOM Structure	VM1G@	Blank	VS1G@	VS2G@	Blank

Figure 1: Schematic representation of the four experimental conditions. The figure is divided into two main panels, each containing two sub-panels. The left panel shows conditions with a 100% hit rate, and the right panel shows conditions with a 50% hit rate. Each sub-panel contains a diagram of a 2x2 grid of stimuli. The stimuli are represented by circles containing a number (100 or 50) and a label (V100 or V50). The labels are placed around the circles, and the numbers are placed inside. The stimuli are arranged in a 2x2 grid, with the top row containing two identical stimuli and the bottom row containing two identical stimuli. The labels are placed around the circles, and the numbers are placed inside.

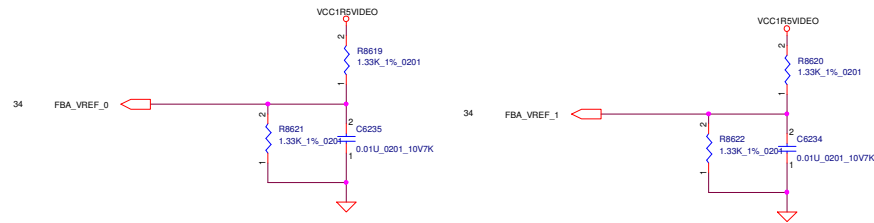
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No.	Docment Number	Rev	01
Date	Thursday, December 16, 2010	Sheet	34 of 100

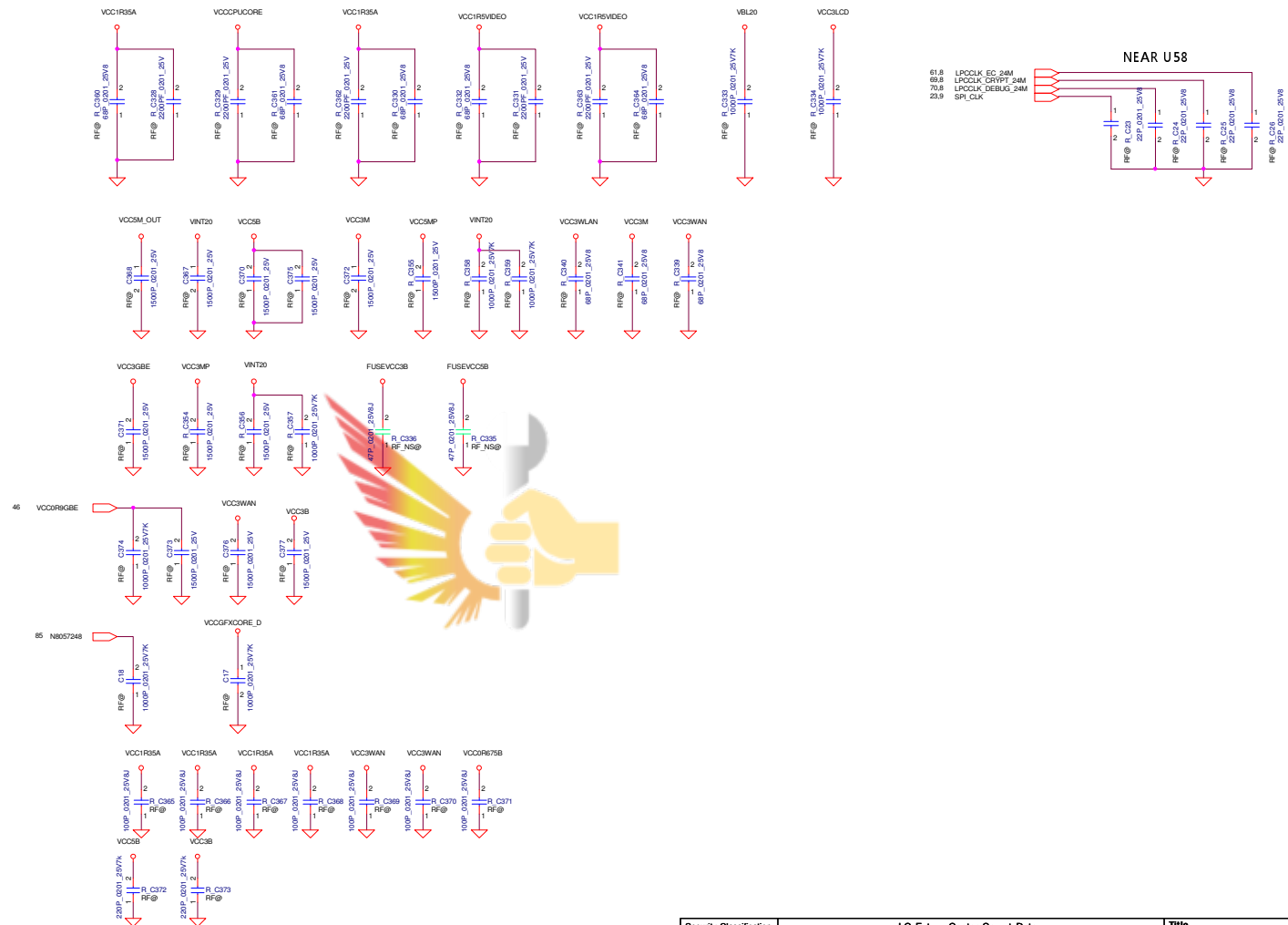


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Custom					0.1
Date:	Thursday, December 18, 2014		Sheet	37	of 100



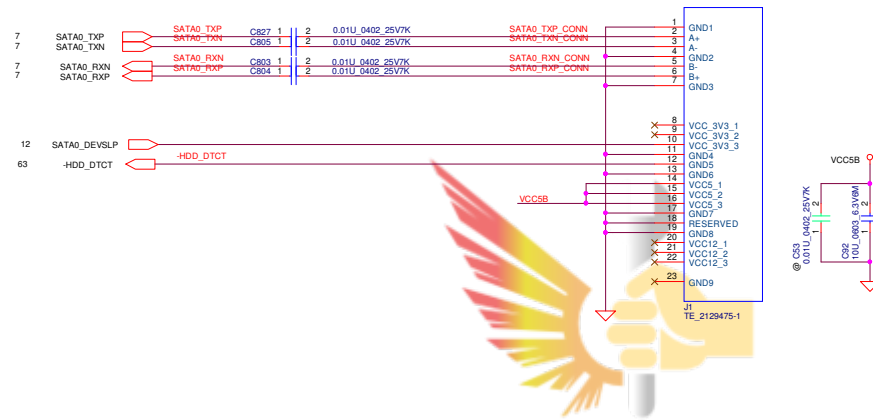
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Size Custom		Document		Number									
Date: Thursday, December 18, 2014												Sheet 39 of 100	




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lenovo		
Project Name : SW-5 SHIUMA		Title : BLANK
Size : C	Document Number :	Rev : 0.20
Date: Thursday, December 18, 2014		Sheet : 42 of 100



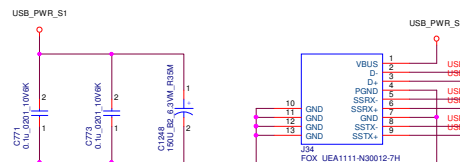
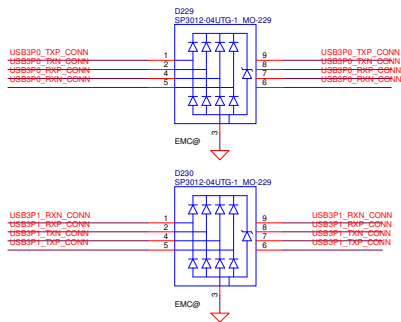
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Date:		Thursday, December 18, 2014		Sheet		43		of 100	

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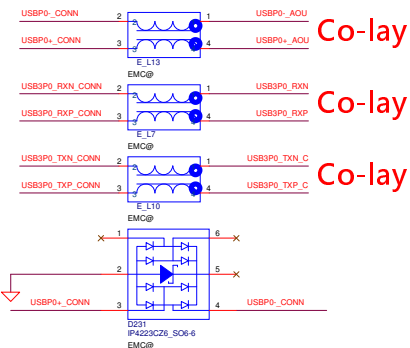


lenovo		
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Size : C	Document Number :	Rev : 0.20
Date: Thursday, December 18, 2014		Sheet : 44 of 100

D229,D230
1st: Littelfuse SP3012-04UTG-1
2nd: Amazing AZ1043-04F



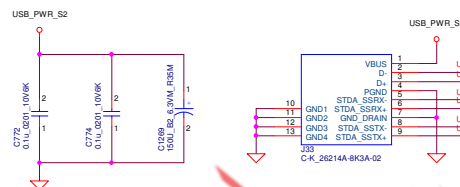
WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONNECTOR



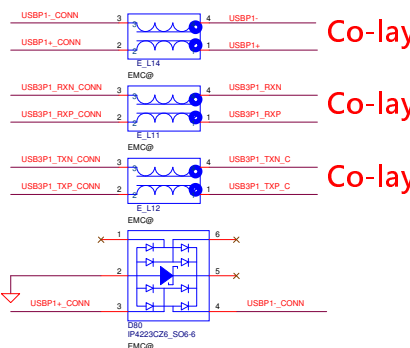
Co-lay

Co-lay

Co-lay



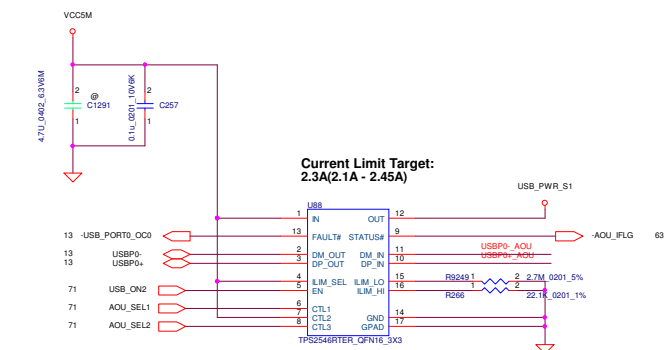
WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONNECTOR



Co-lay

Co-lay

Co-lay



Current Limit Target:
2.3A(2.1A - 2.45A)

Vendor	P/N
TI	TPS2546RTER
Pericom	PT505B2543

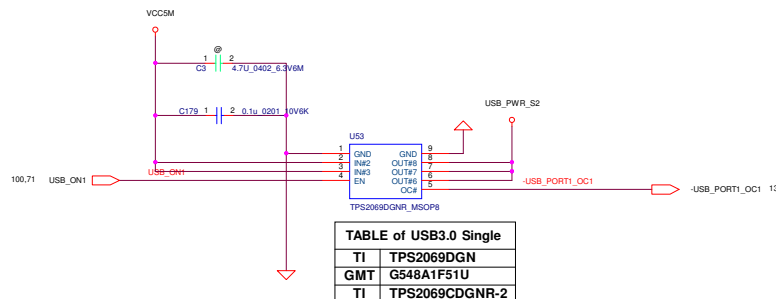
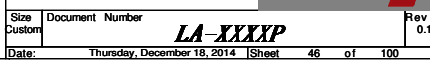


TABLE of USB3.0 Single	
TI	TPS2069DGN
GMT	G548A1F51U
TI	TPS2069CDGNNR-2

Security Classification	LC Future Center Secret Data
Issued Date	2012/07/01
Deciphered Date	2014/07/01

Title	USB POWER/CONN
Rev	0.24
Date	Thursday, December 18, 2014
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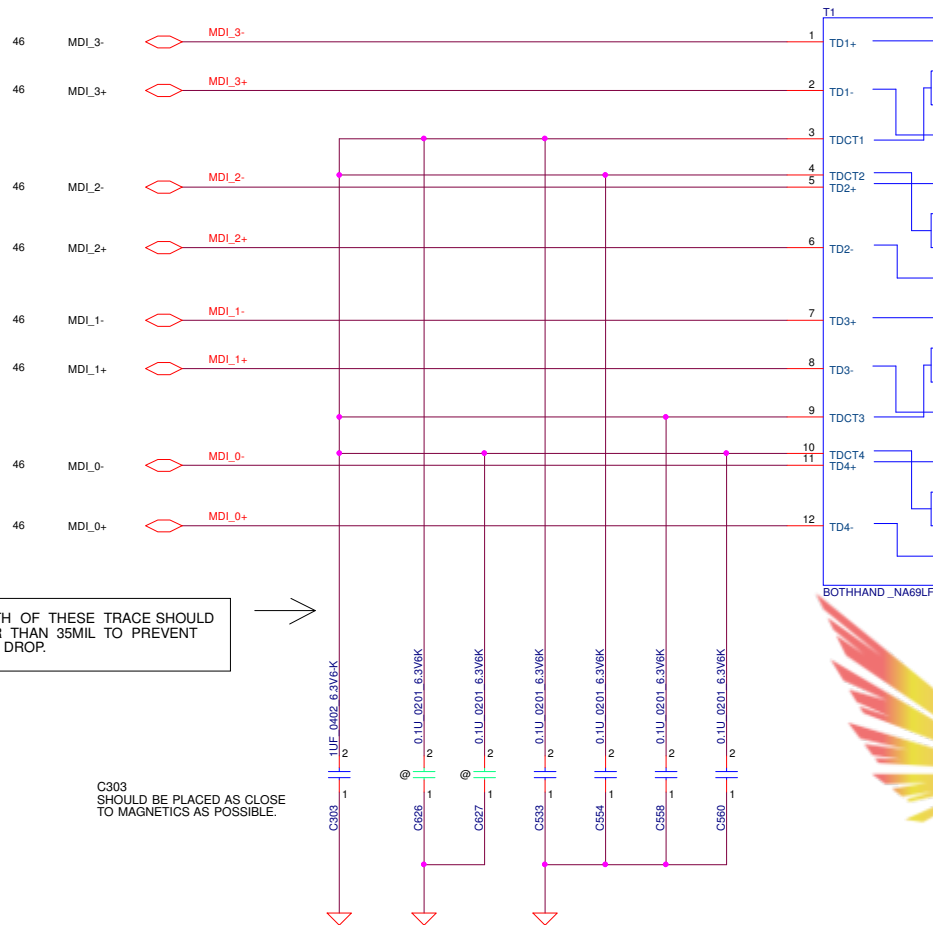




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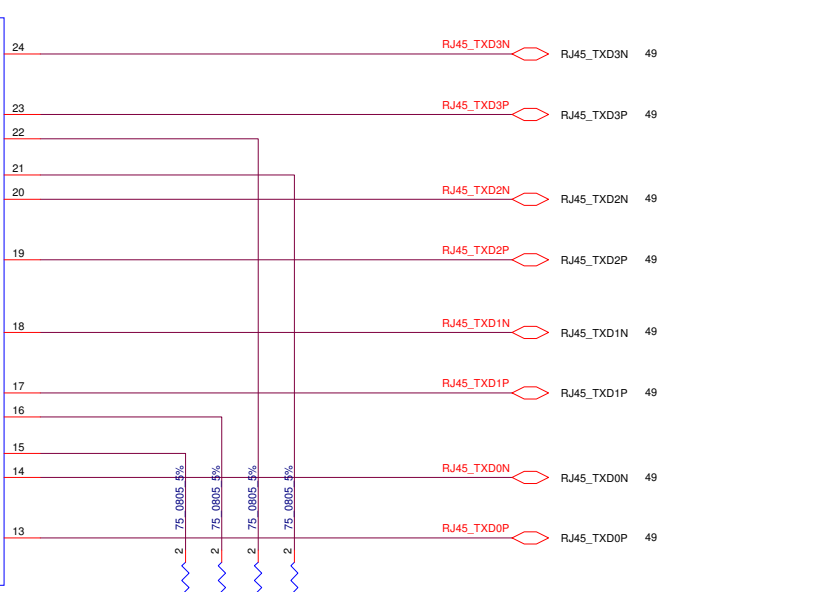
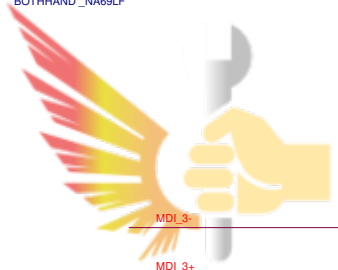
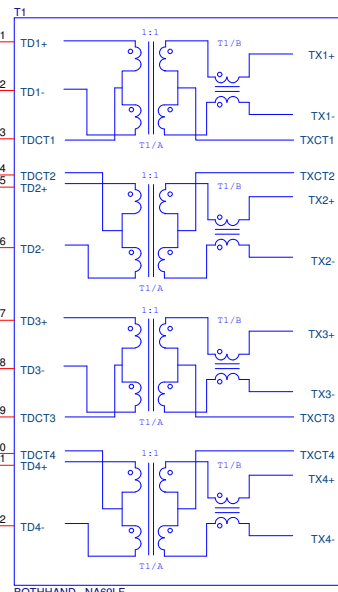
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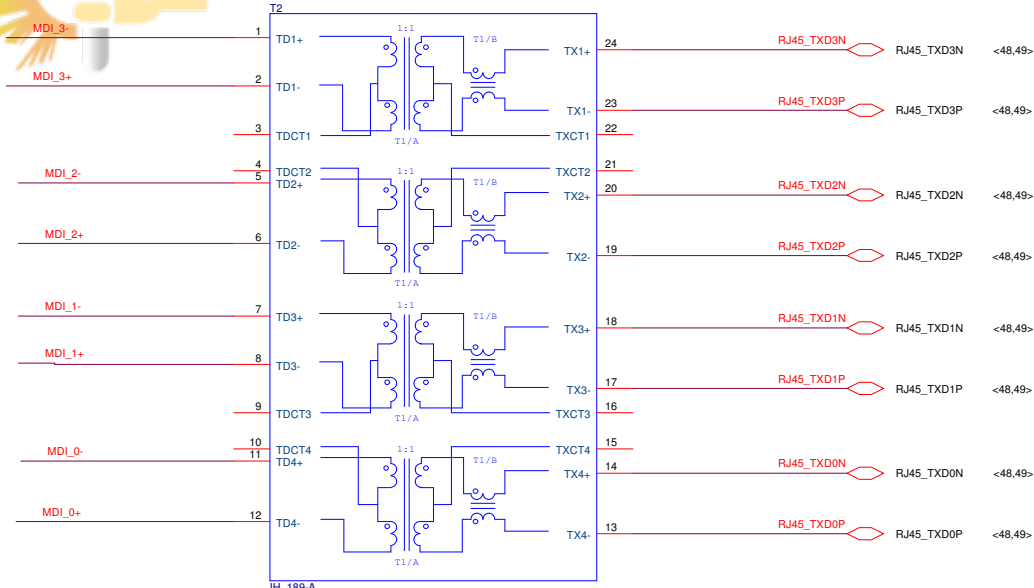


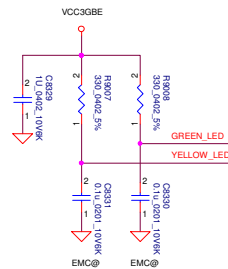
ESD REASON


Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF



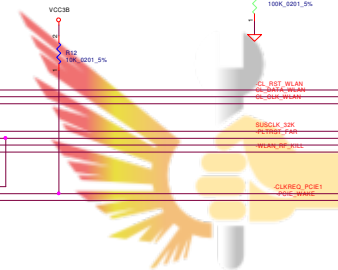
PATTERN MUST BE SHORT AND WIDE.
HIGH VOLTAGE 1500PF CAP IS OPTIONAL



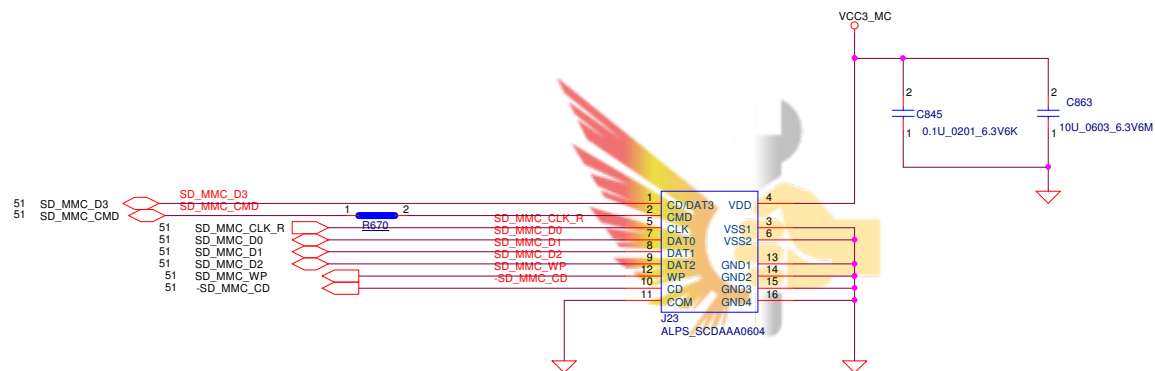


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Issued Date	2012/05/02	Deciphered Date	2012/5/02	RJ45 CONNECTOR		
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				Date: Thursday, December 18, 2014	Sheet 49 of 100	

3.2H CONNECTOR



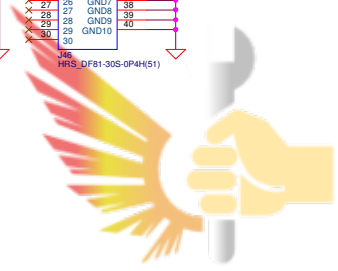
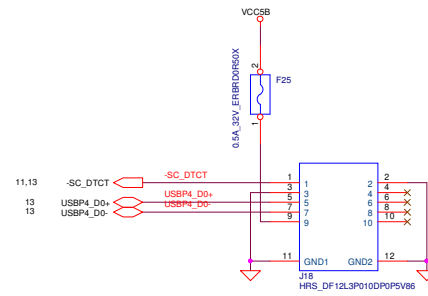
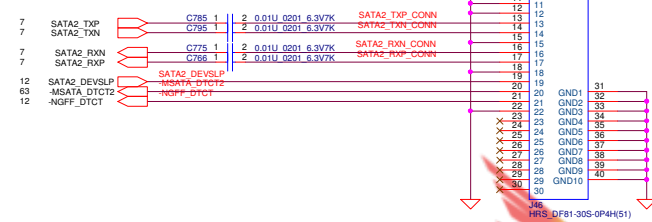
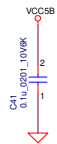
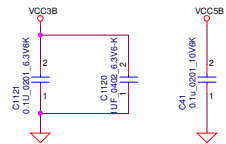
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		2012/12/01

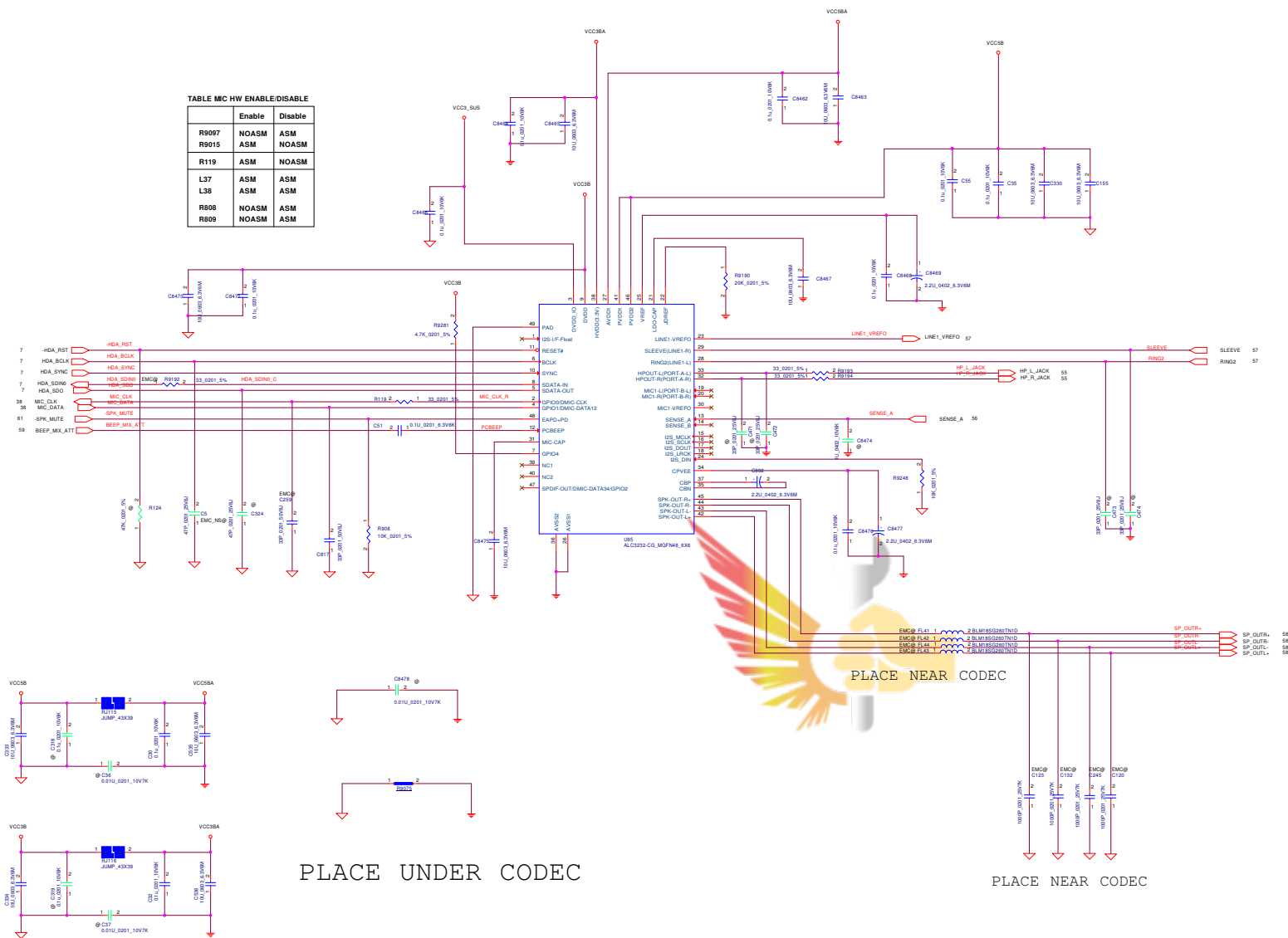
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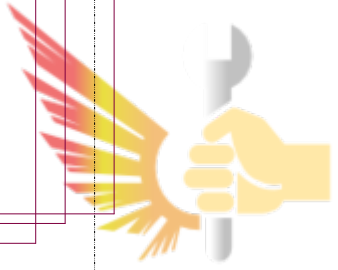
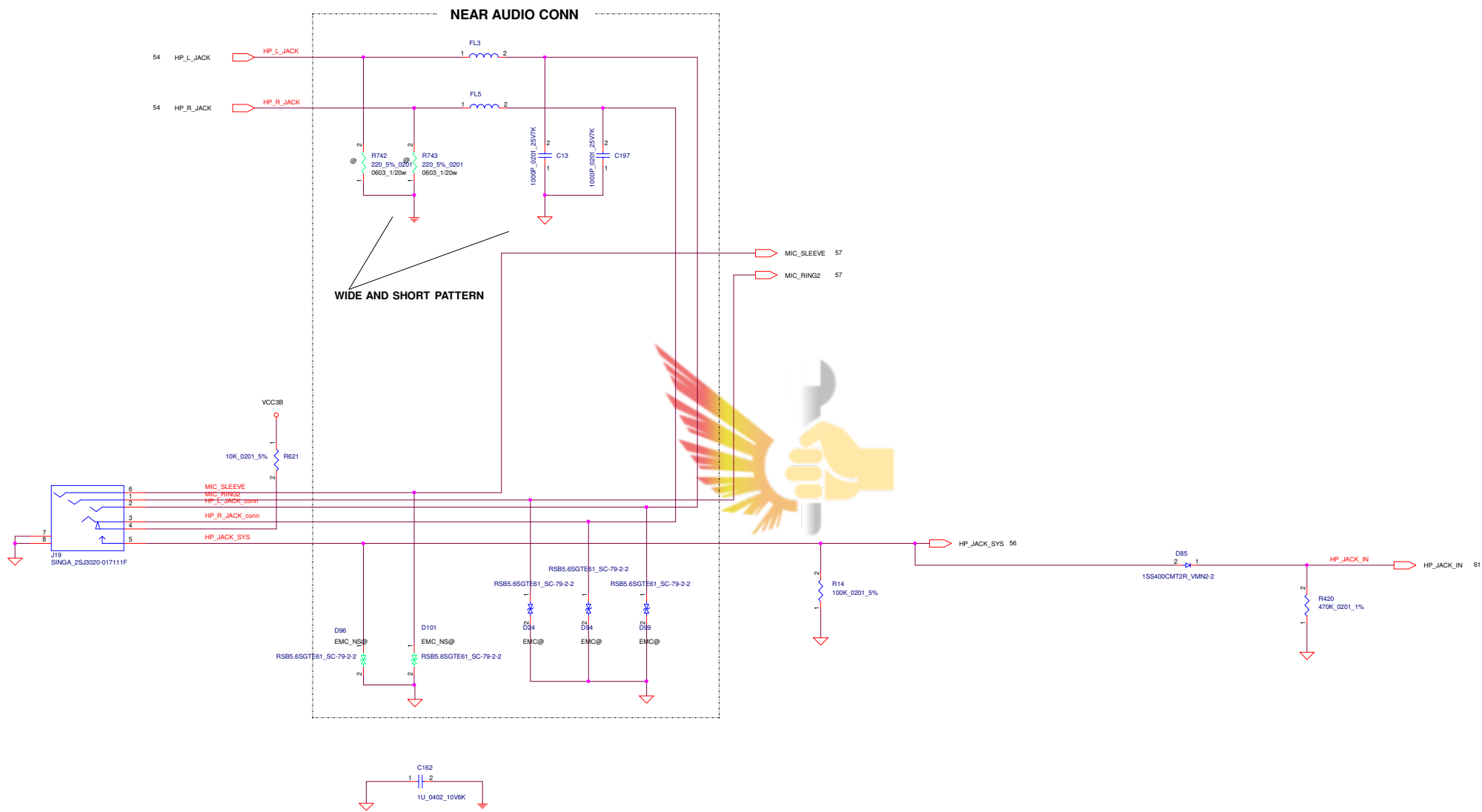
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Issued Date		Deciphered Date		SMART CARD I/F	
2012/07/01		2014/07/01		Size	
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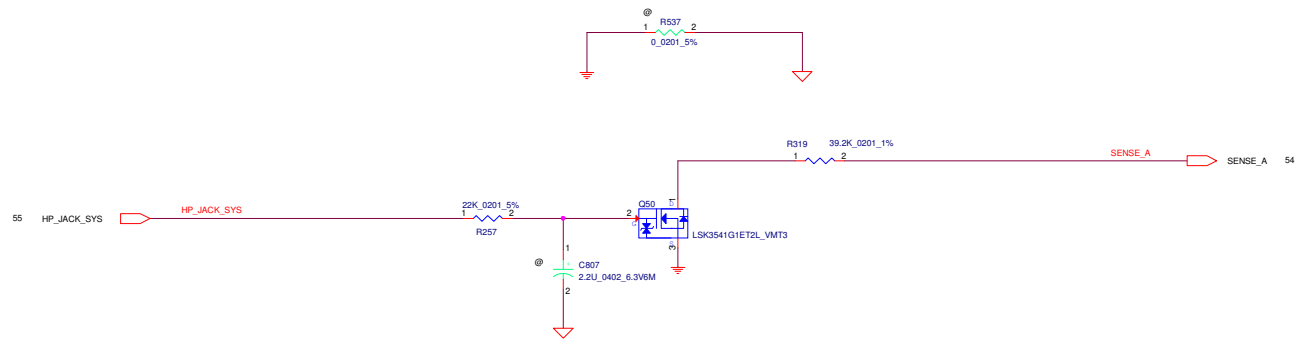
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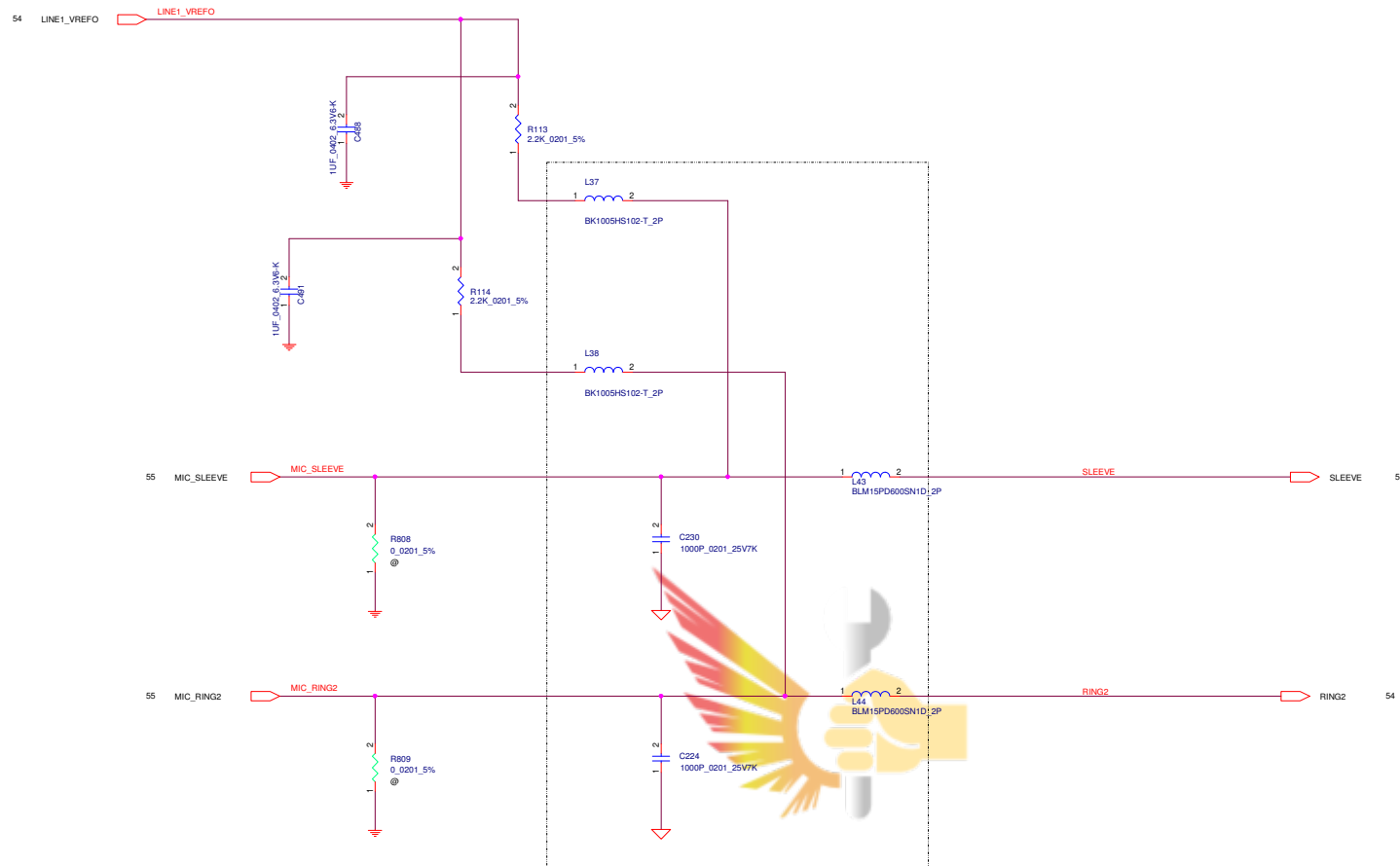


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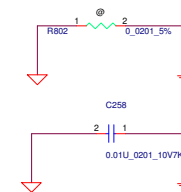
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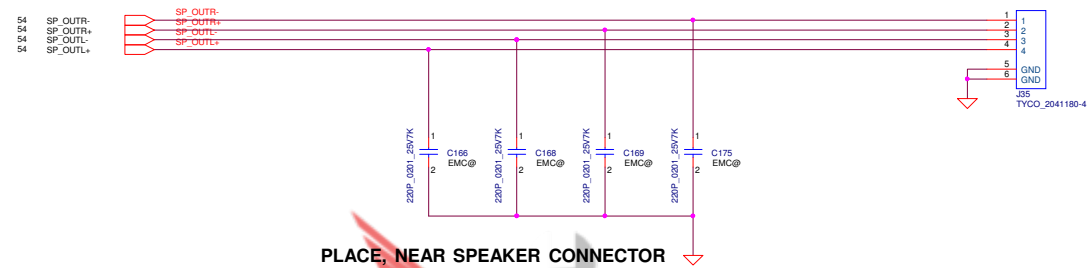
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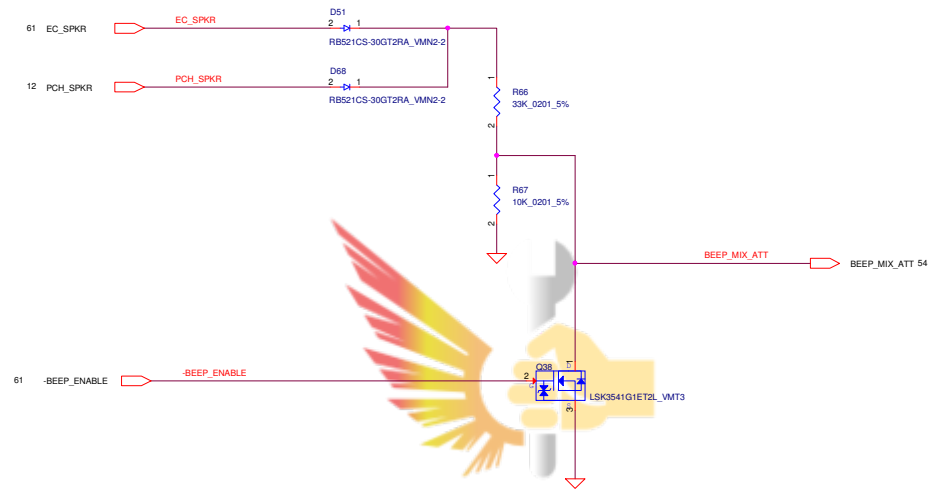
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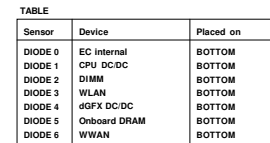


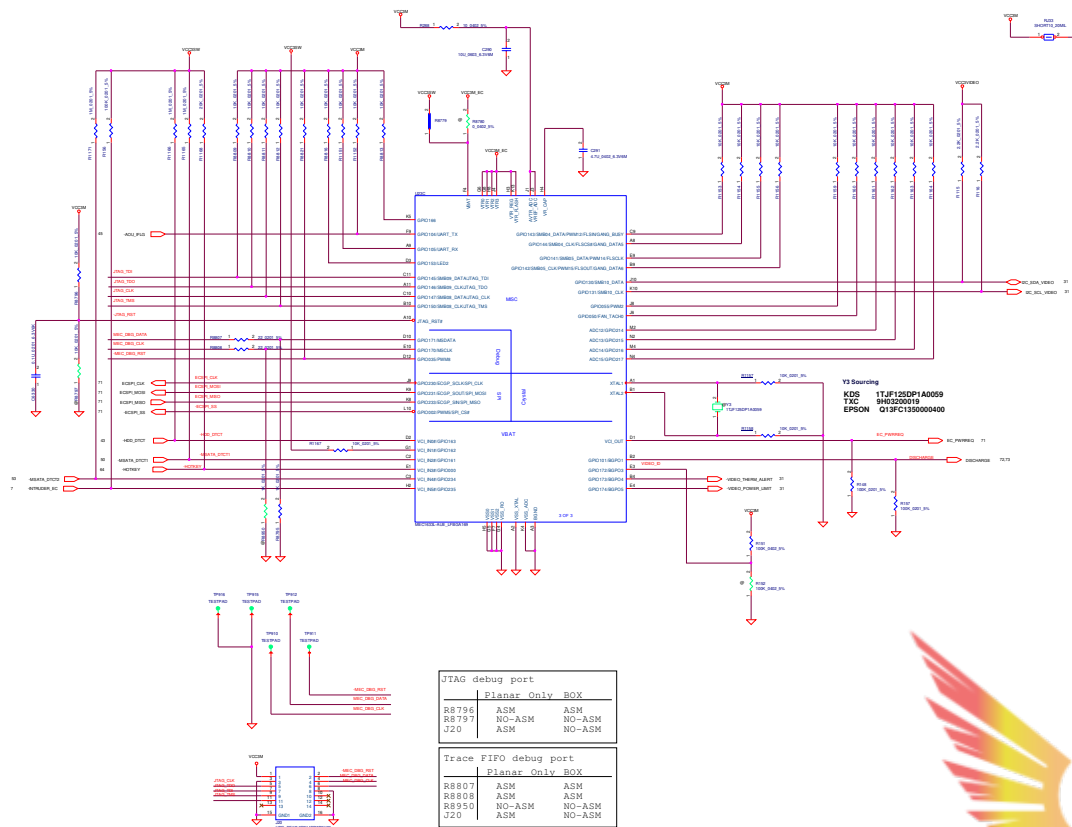
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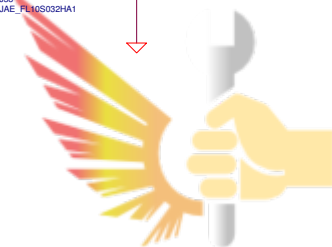
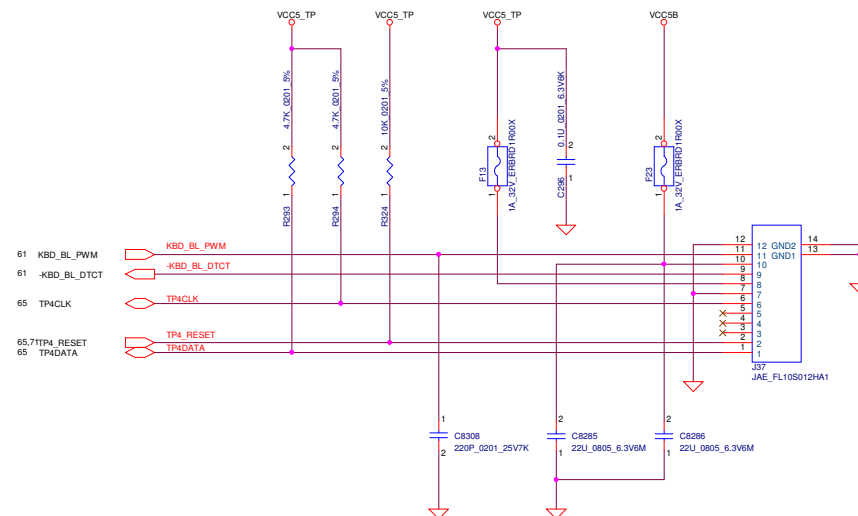
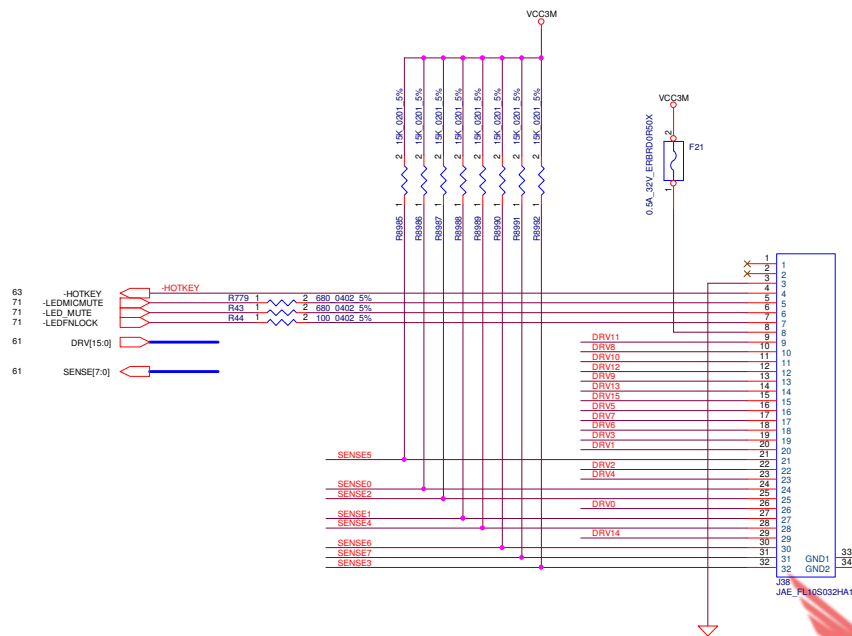


Rev 0.1



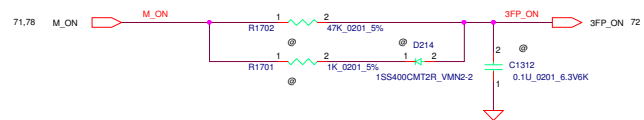
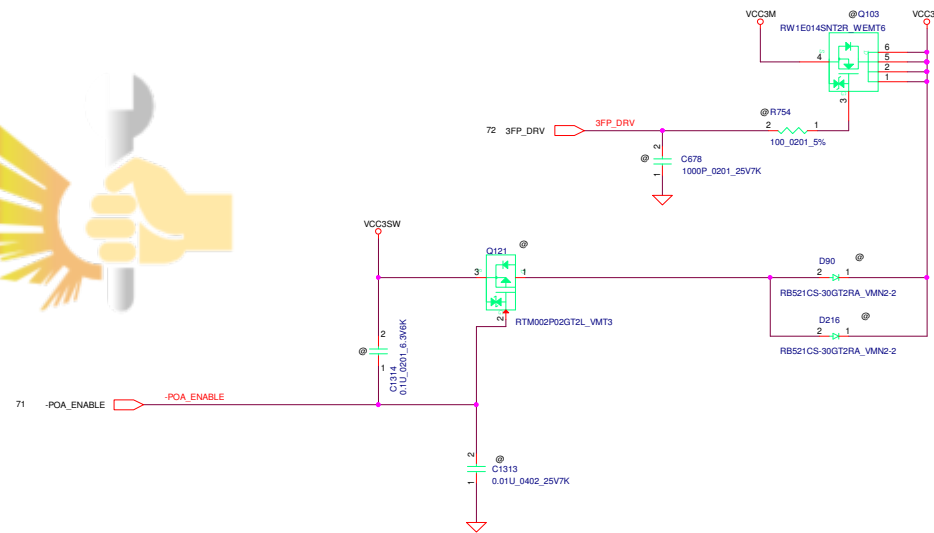
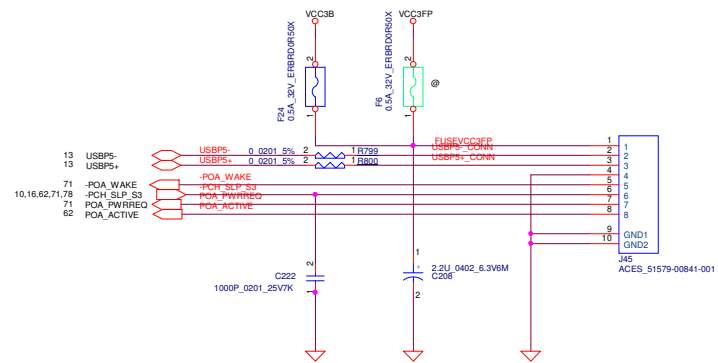









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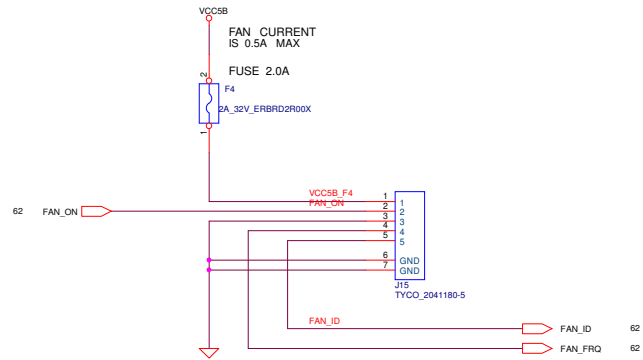
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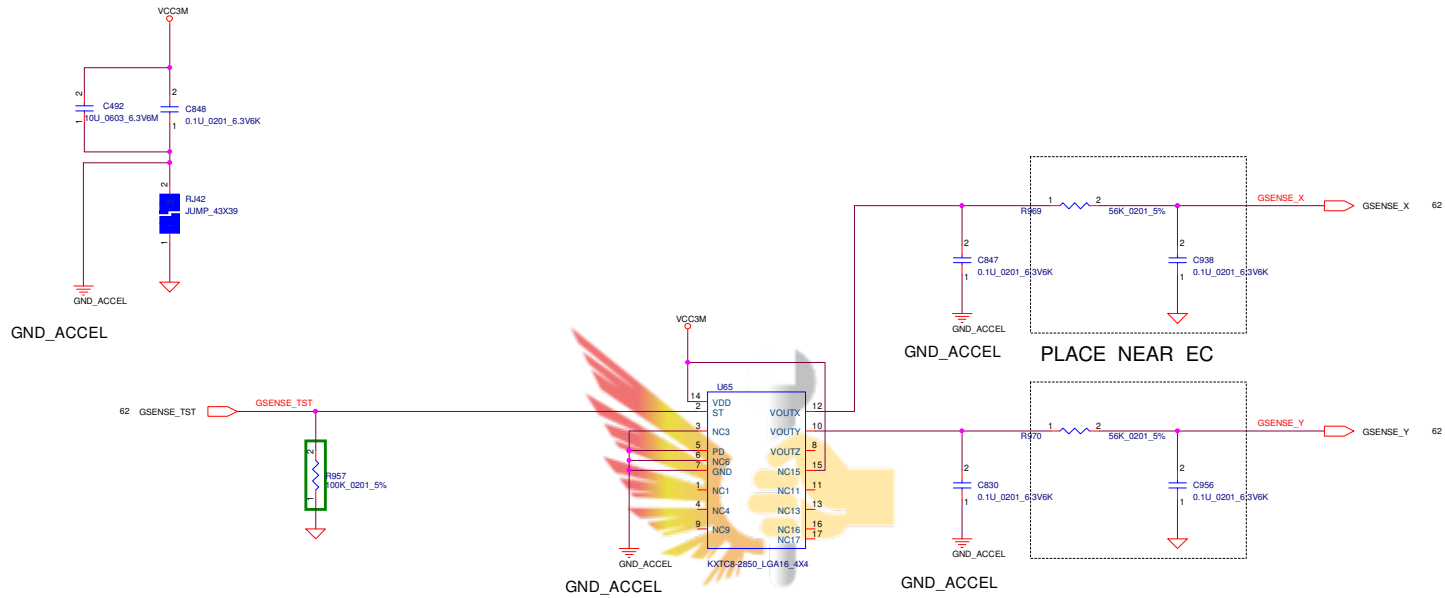
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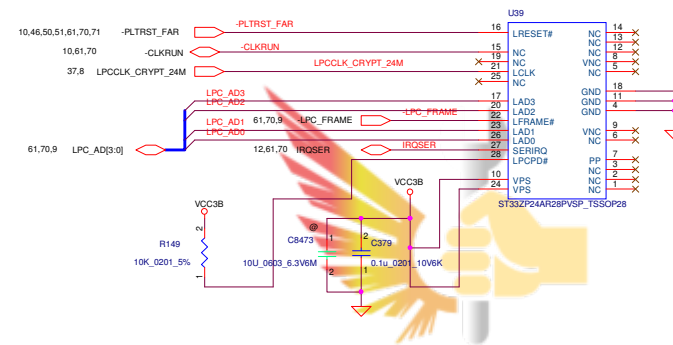



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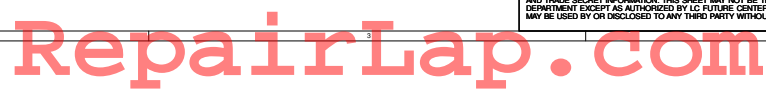
LOGIC
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U65 Q105	ASM ASM	NO_ASM NO_ASM	
R885 C829 C969	10-OHM ASM ASM	NO_ASM NO_ASM NO_ASM	
C830 C847	ASM ASM	NO_ASM NO_ASM	
R969 C938 R970 C956	56K ASM 56K ASM	NO_ASM NO_ASM NO_ASM NO_ASM	
C704 R344 C703	NO_ASM NO_ASM NO_ASM	NO_ASM NO_ASM NO_ASM	
R125	ASM	ASM	





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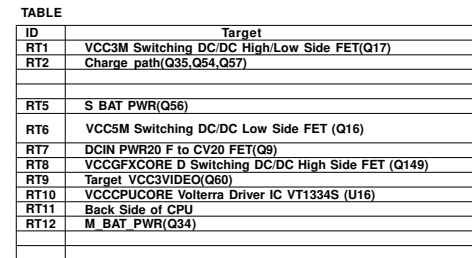

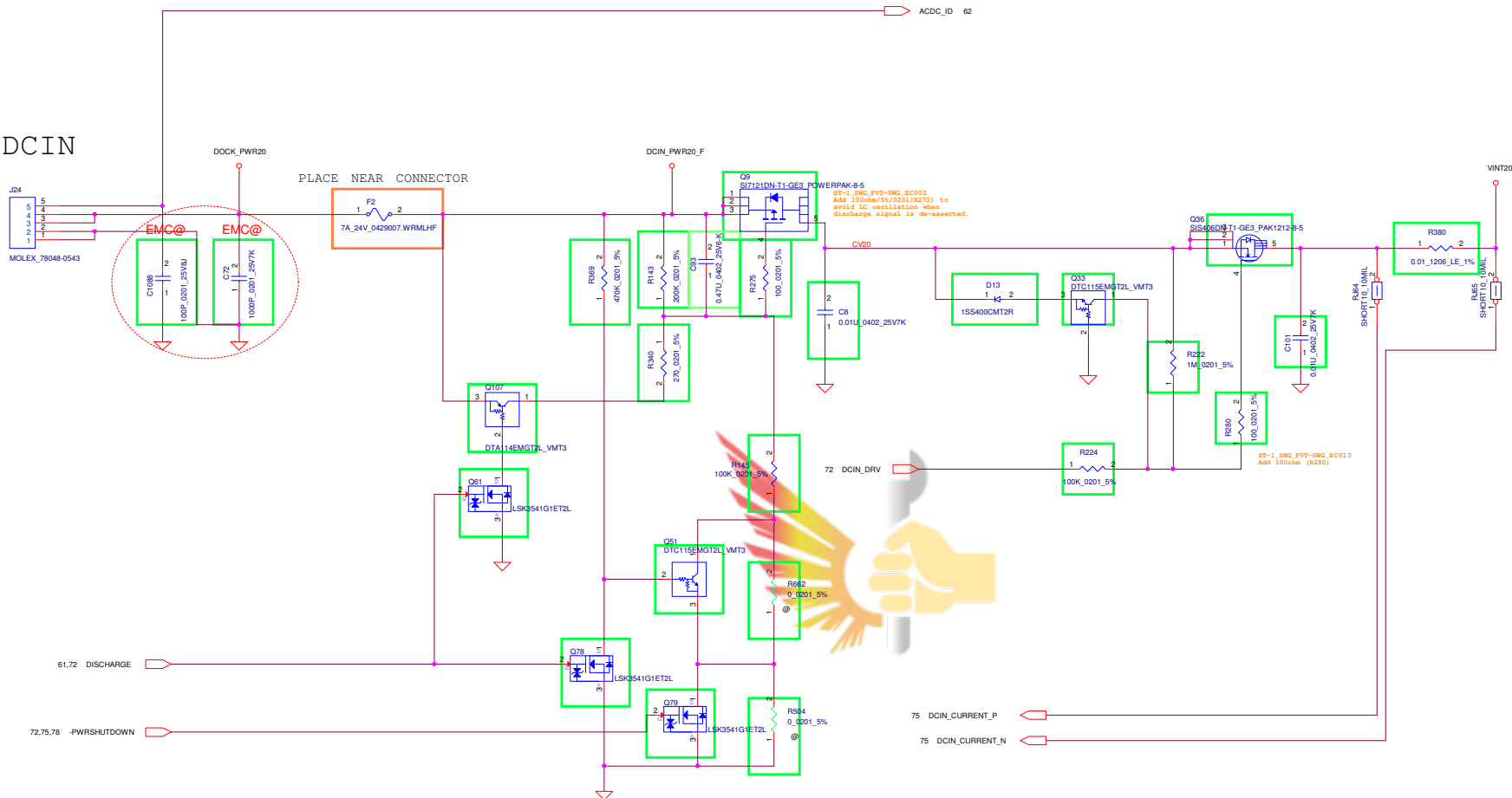


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D73	ASM	NO-ASM
R8931	ASM 100K-ohm	ASM 0-ohm

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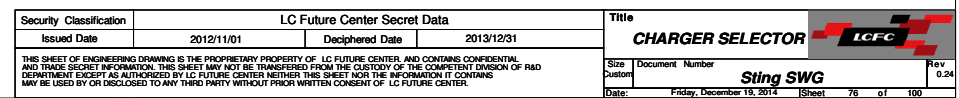
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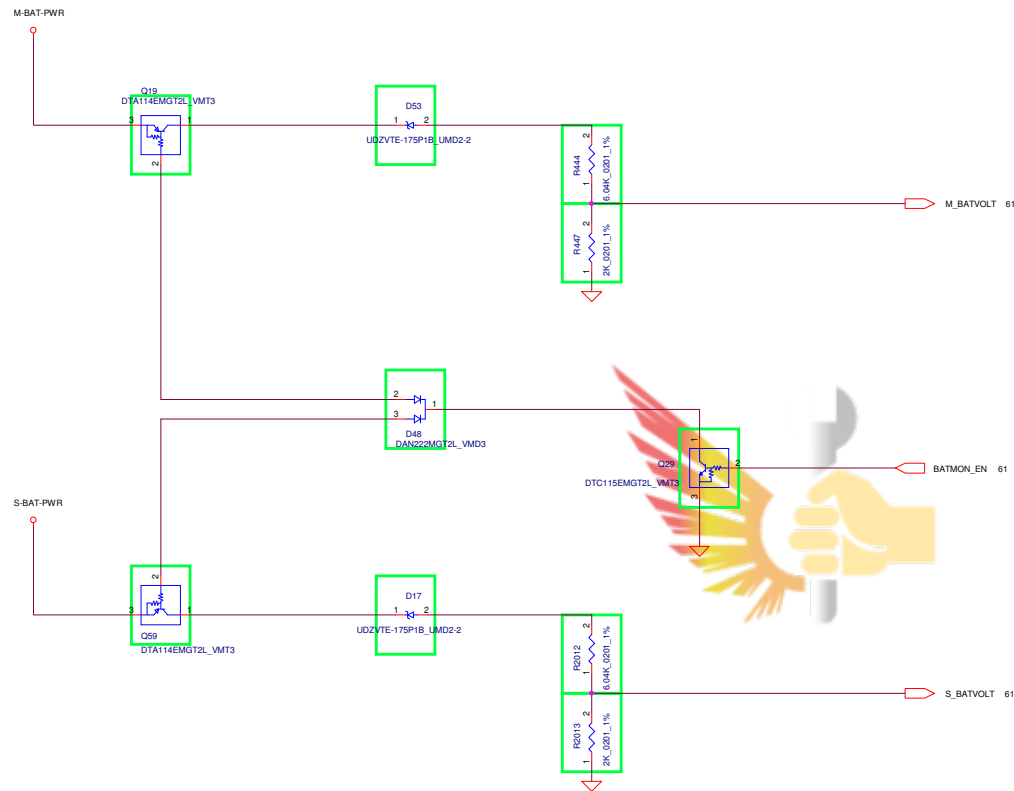
PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
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LOGIC

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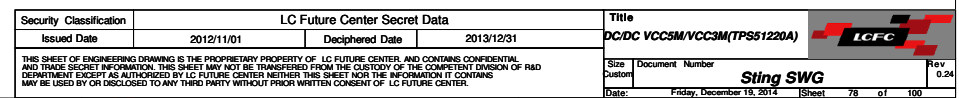


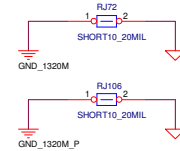





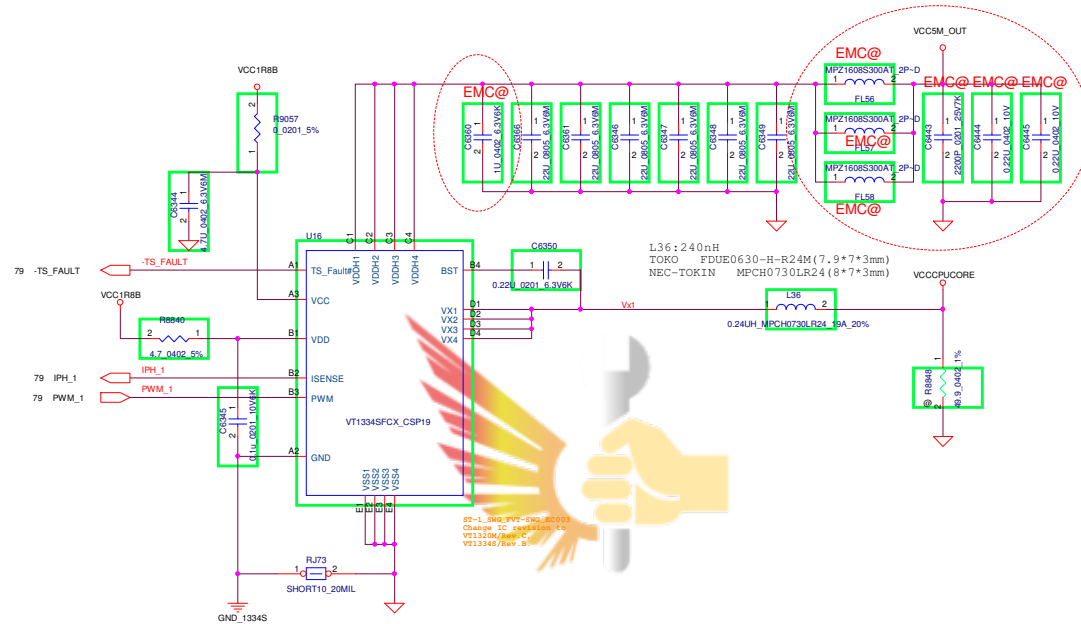
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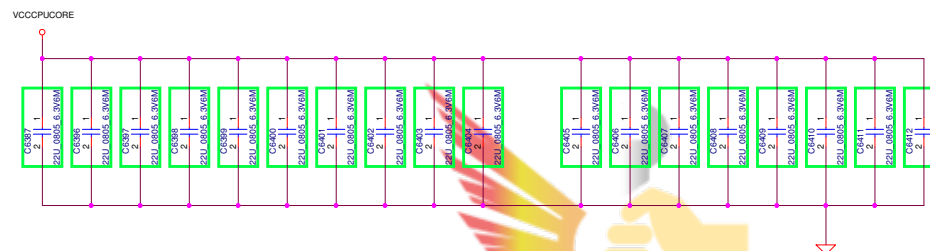


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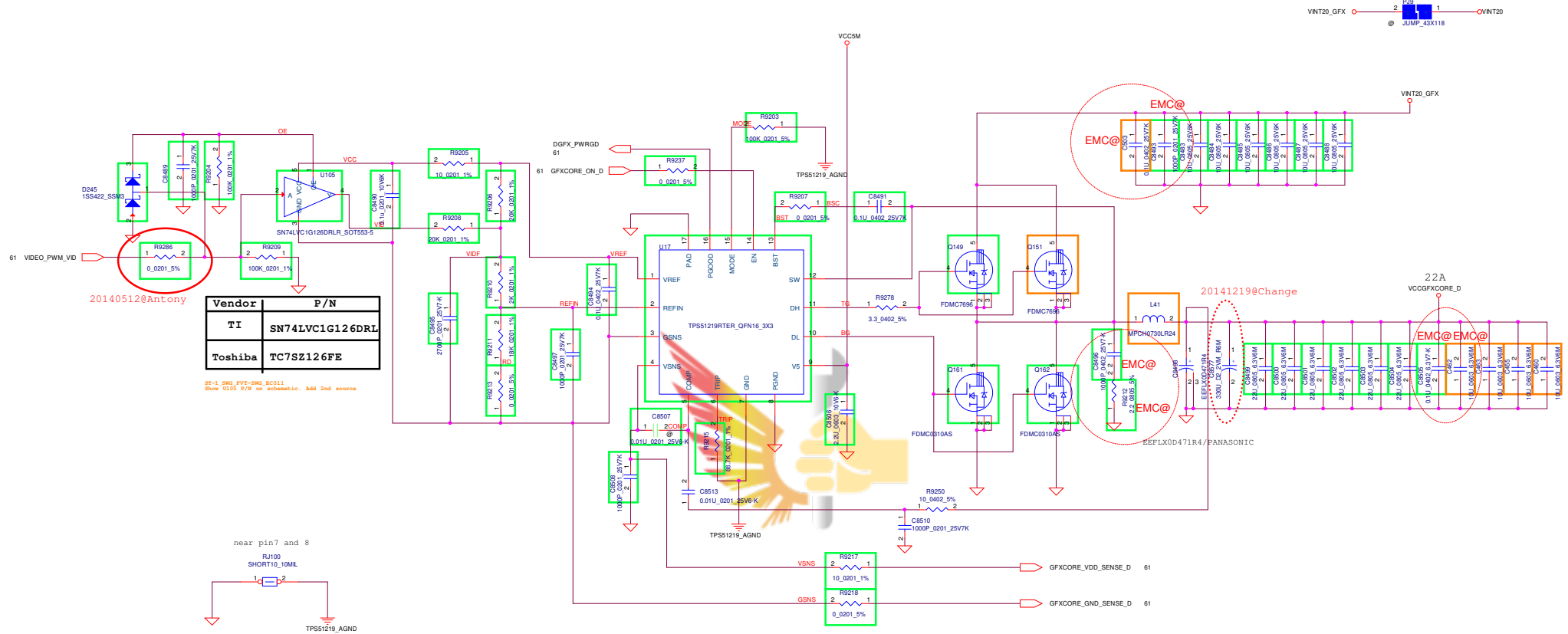
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16pcs 22uF for VCCCPUCORE of 25W ULT CPU
(14pcs 22uF for VCCCPUCORE of 15W ULT CPU)

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Issued Date		Deciphered Date		VCCCPUCORE DECOUPLING	
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Size		Document Number		Rev	
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Date:		Friday, December 13, 2014		Sheet 82 of 100	

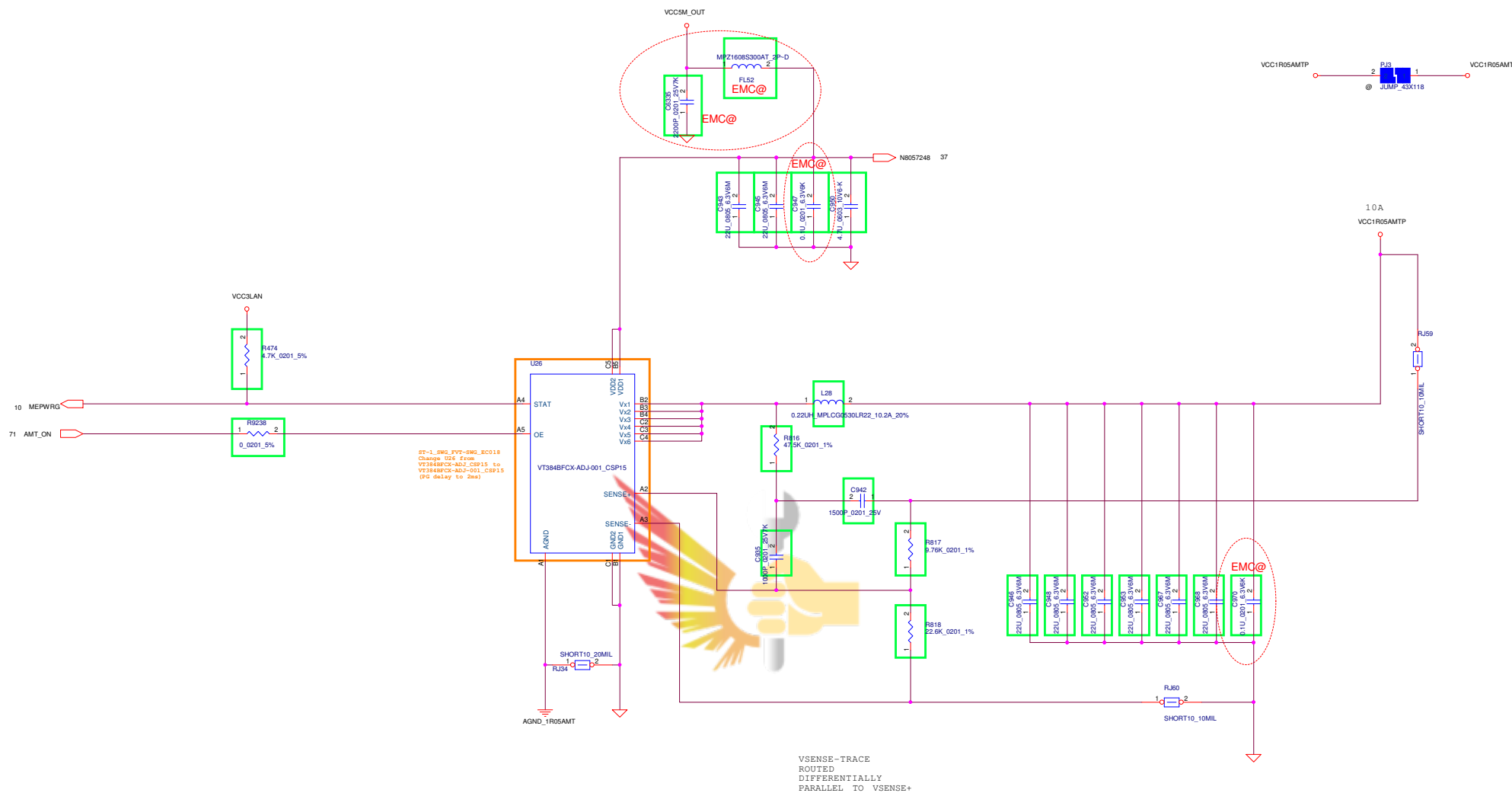
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200Kohm	NO_ASM	ASM	D_CAP	400KHz
100Kohm	NO_ASM	ASM	D_CAP	300KHz



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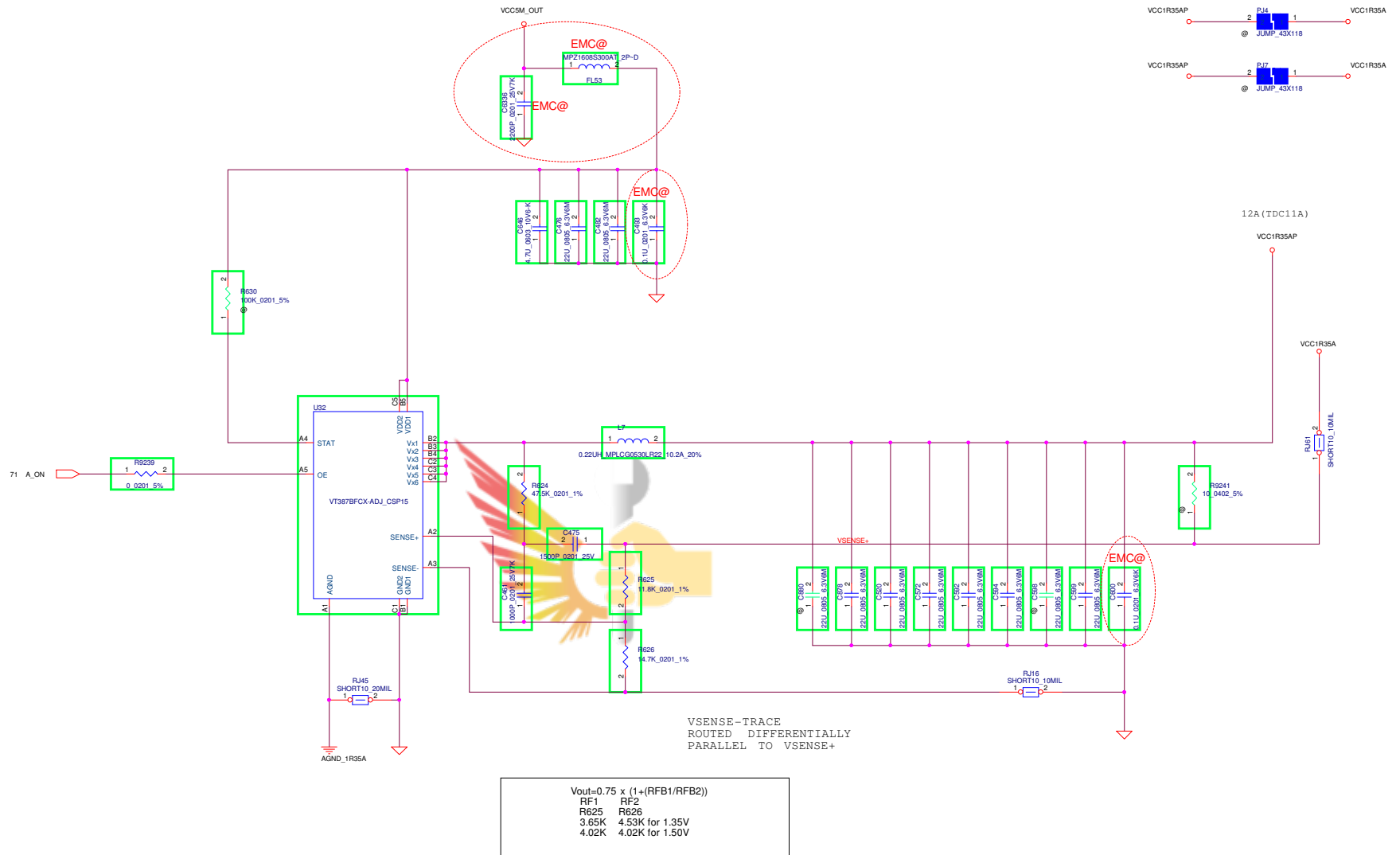
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$$V_{out} = 0.75 \times (1 + R_{817}/R_{818})$$

VSENSE-TRACE
ROUTED
DIFFERENTIALLY
PARALLEL TO VSENSE+

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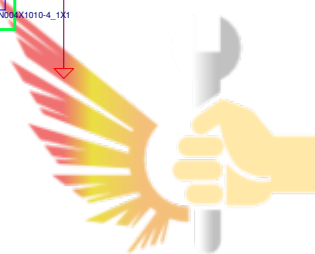
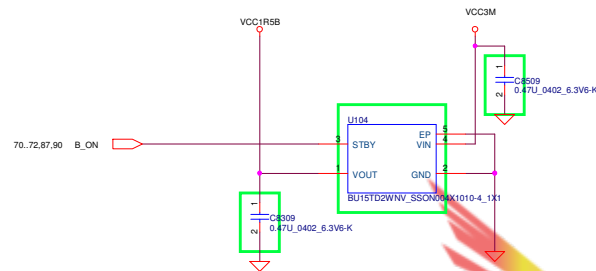
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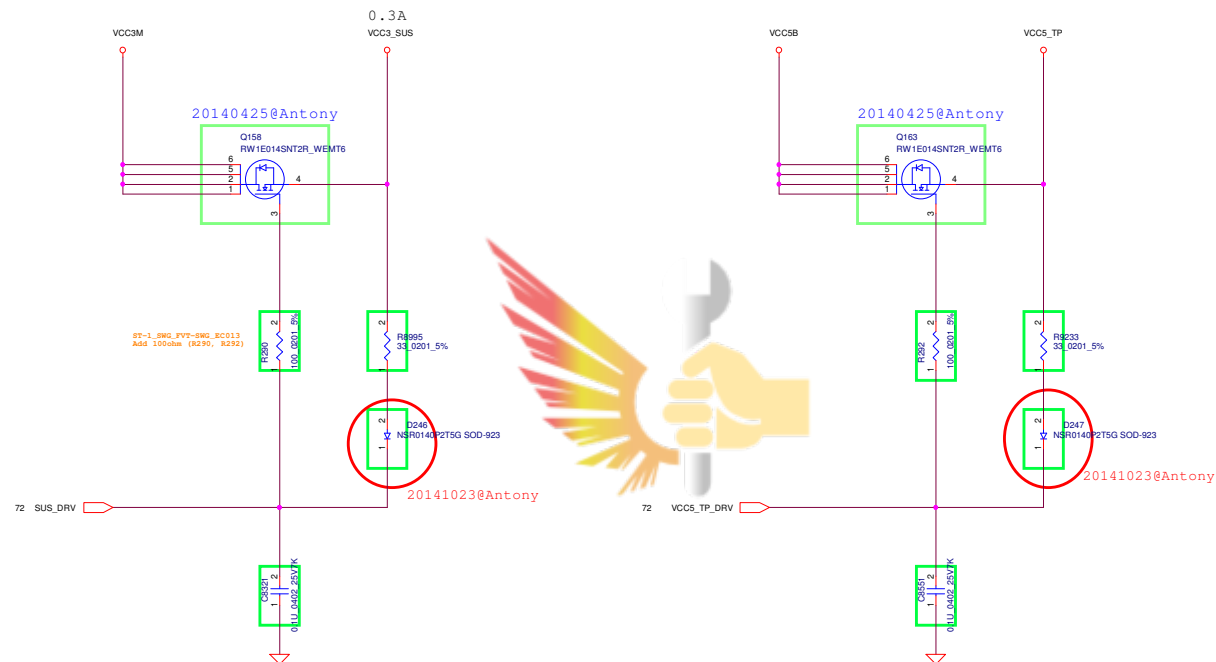
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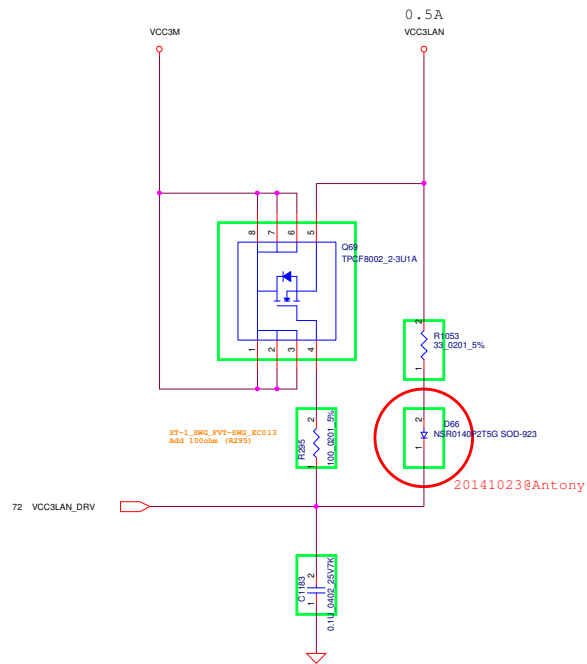
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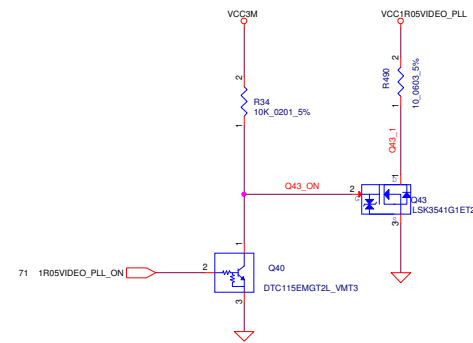
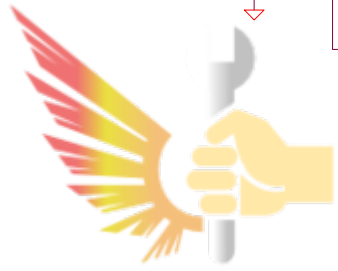
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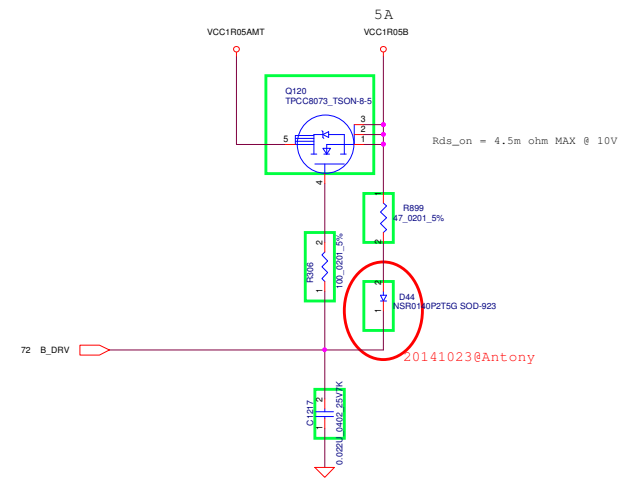
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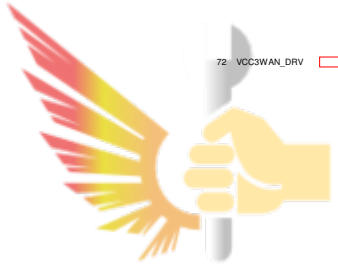


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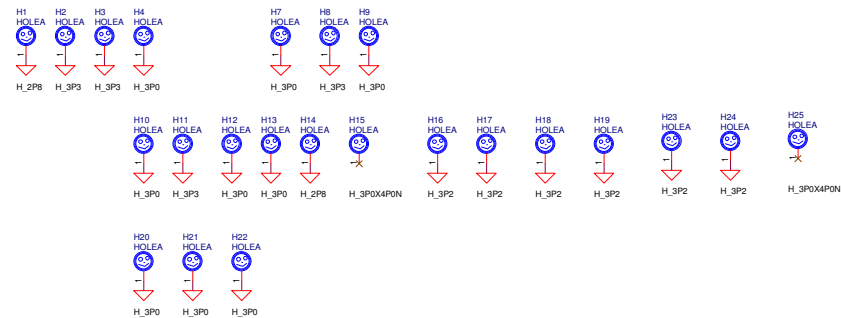
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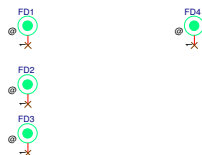
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C8283	ASM	NO-ASM
D238	ASM	NO-ASM

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
R8926	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM


LOGIC



FID
Board Area



FID
Component Area

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