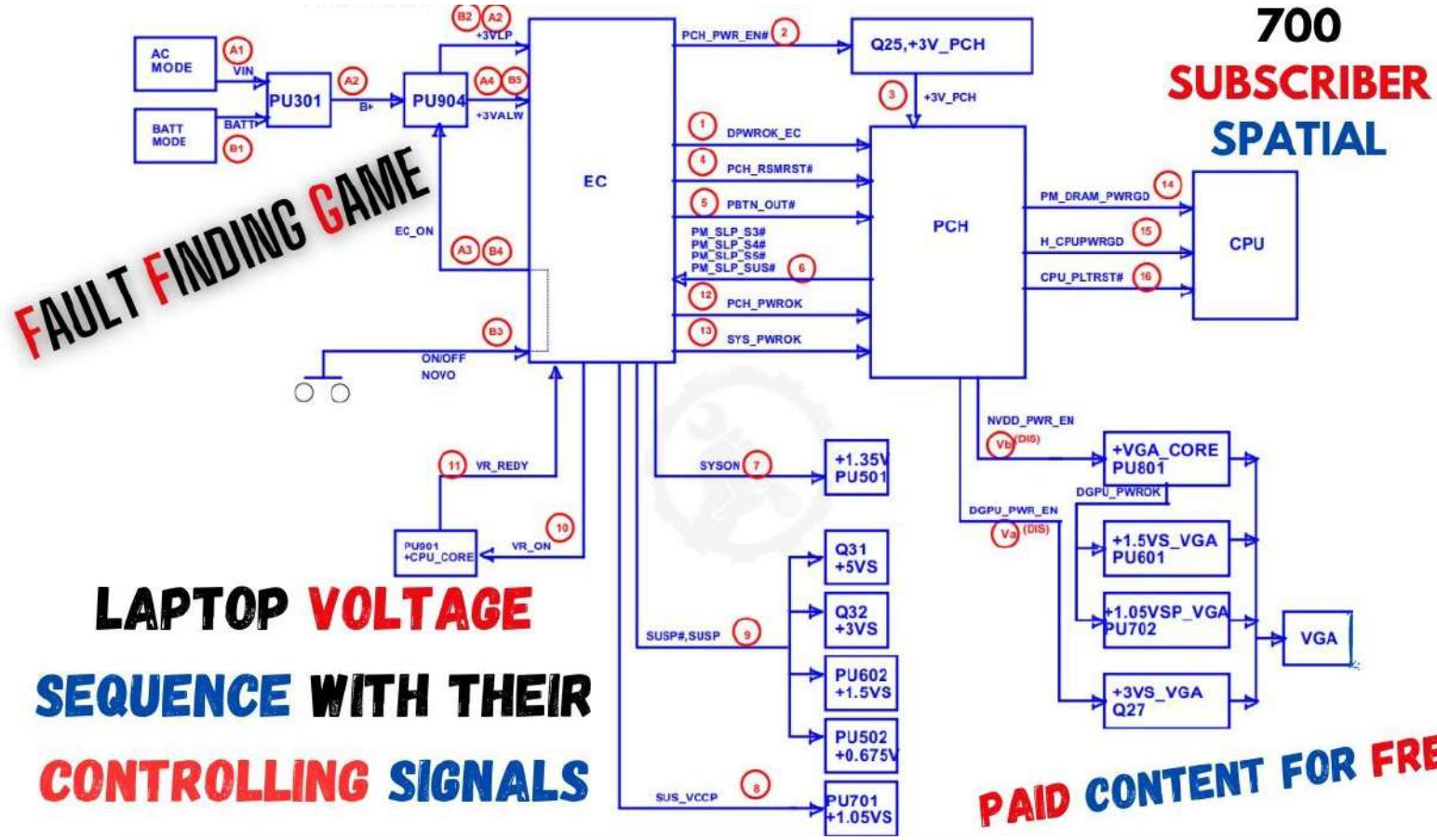

FAULT FINDING GAME

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LAPTOP VOLTAGE SEQUENCE WITH THEIR CONTROLLING SIGNALS

PAID CONTENT FOR FREE

Date : / /

① LAPTOP Voltage Sequenee Diagram (G3)

Stage → 1. +3.3V RTC vcc (cell)

(i) RTCRST#

(ii) SRTCRST#

(iii) Intruder#

(iv) 32.768 KHz crystal.

Stage → 2 +19V [redacted]_Power_SRC

[Charging ie Verification the +19V]

Stage → 3 Step Down Section (1)

(i) +3.3 Volt LDO / +3VREG 100mA

Triggen (1) (ii) +5V LDO or +5VREG 100mA

Stage → 4 Step Down Seetion (2)

(i) +5V_ALWS

TRIGGER(2) (ii) +3.3_ALWS Coil (S5)

Stage → 5 Sus_level Power (S4 or S3) (V5)

(i) +3V_Sus (iv) RAM Voltage (1.5 or 1.2) V

(ii) +5V_Sus (v) 2.5VPP (DDR4)

(iii) +1.5V_Sus (RAM)

Stage → 6 RUN_Level Power (S0) 1. LAN ic

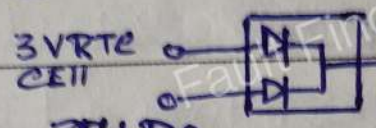
(i) +3V_RUN 2. AUDIO ic

(ii) +5V_RUN 3. VcoreTC

Date : / /

② Controlling Signal

Stage-1 3.3V RTC Voltage is created By RTC cell & 3V LDO



Stage→2 +19V in to the 1st Mosfet then 2nd mosfet & then current Sense resistor. 1 & 2 Mosfet Controlled by the Charging ic. [Verify the Charger]

Stage→3 LDO 3.3 & LDO 5V in Enable by LDO_EN signal

Stage-4 3.3V ALWS & 5V ALWS Coil Voltage in Enable by EC_ON (Control by the i/o)

Stage-5 SUS-PWR

Sus Level Power are Control by PCH or Io. (S4 or S3)

PCH → SLP_SA#

I/O → [redacted]_SYS-ON#

Stage-6 [redacted] SUSP#

Run level Power are Control by PCH or I/O

PCH → SLP_S3#

I/O → [redacted] Run_ON

Date : / /

(3)

(iii) + RAM - RUN

(iv) + 1.8 V - RUN

(v) + 1 V - RUN

(vi) + 1.05V - PCH OR Some-time VICE VERSA

Stage → 7 + CPU - CORE (Processor)

Stage → 8 + GFX_CORE (Processor)

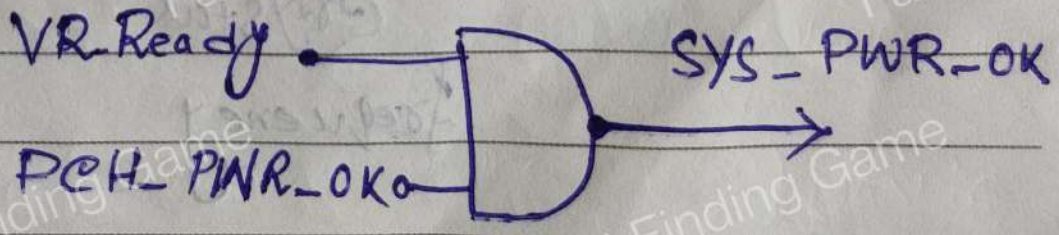
Date : / /

PCH_PWR_GD Enable the VccSA

Stage → 7

PCH Power good signal or RUN-Level Power good Signal received by the Sio, in return Sio gives us IMVP_VRON or VRON_EN. Which is Enable our Core Voltage.

Stage → 8 Whe Core Power_GD (VR_RDY) Received by the i/o i/o release GXF_EN to Enable the GPU of the Processor Power.



Date : / /

Sometime

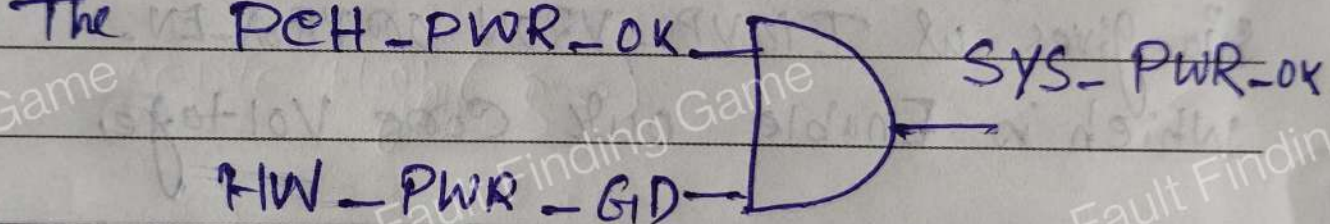
Vcore PWR GD received by the i/o

& I/O circuits

PCH_PWR_OK

&

HW_PWR_GD



& After PCH received the SYS_PWR_OK the Clock of the Mother board is Started

(25MHz or 24 MHz)

crystal

frequency

& then PLT_RST#. Distributed

Date : / /

(6)

to the mother board & Auto enable the CPU.

The CPU Start to read the bios.

After the bios reading CPU Activate the VIDS & core starts the Actual core Voltage with high current.

Now properly the Vcore Voltage is created with Proper CPU Wattage.

↓

DRAM_RST is created

↓

final Vcc Gfx.

(7)

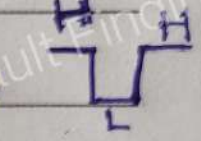
Date : / /

Triggering of the Laptop Motherboards.

LDO is present on the

(i) 3.3V, ON/off Switch.

(ii) i/o received the High Low high sequence



(iii) 3.3V Present on the i/o (LDO)

(iv) At this time I/O Also have the information about LID Switch.

Active High (3.3)

After triggering the Power Switch.

i/o out

(i) Power BT out (PBTN_OUT#)

(ii) LID Switch out (EC_LID_OUT#)

(iii) RSM_RST (EC_RSMRST#)

I/o Triggering Section is OK

Date : / /

(8)

PCH reply to the I/O with 3 signals.

(i) SLP_S5# (S5) → Step Down
(ii) SLP_S4# (S3) Sus Power
(iii) SLP_S3# (S0) Run Power

At this time PCH say to the i/o to turn ON all the Voltage regulators Step by Step.

Note:

(i) When SLP_S5# is received by the i/o then i/o created the Enable signal for 3.3V AlWS Power (S5)

When SLP_S4# is received by the i/o then i/o created the SYS_ON or SusP# to Starts the Sus_level Power. (S4 or S3)

(iii) finally when i/o received the SLP_S3# the i/o create the RUN_ON or RUN_PWR_ON (S0)

The Actual Voltage Sequence

(i) SLP_S5#

ii) 3 & 5 ALWS

iii) SLP_SA#

iv) 3 & 5 Sus Level Conversion with Ram & VPP (DDR-A)

(vi) SLP_S3#

(vi) all Run Level Supply