LAPTOP Clock Data & PLT

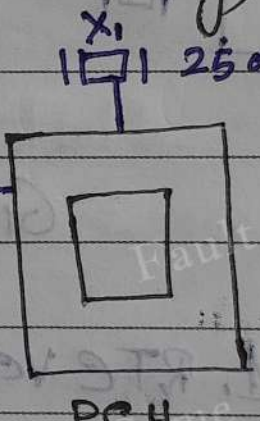
(1) CIK, Data, reset, X Date : 05/01/24

CIK, Plt, Data [CPD] ✓

1. Mother board Power Sequence is Complete. (Power level OK)

2. Then SYS_PWR_OK is created & SYS_PWR_OK is coming to the PCH.

3. PCH external 25 or 24 MHz Crystal is start oseillation (frequency).



(out) internal frequency

1. 33MHz → 4
2. 100 MHz → 10
3. 120 MHz → 1
4. 24 MHz → 1
5. 48 MHz → 1

use in

1. 33 MHz Clock → LPC Communication (PCI/LPC)
2. 100MHz → SM Bus Data & I²C logic
3. 24MHz → use for sound
4. 48 MHz → use for usb

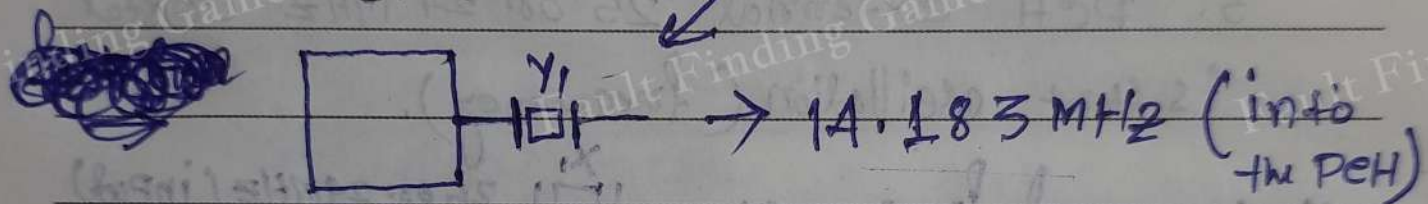
(2) Always remember 1st gen Motherboard has Clk generator IC

Date : / /

1. input Source frequency → 25MHz (1st gen 2nd, 3rd)

2. Soc on 4th gen (Acer) → 24MHz

Note: [redacted] Blue Clock / Green Clock



Green Clock

1. RTC Vcc → out Signal 3.3
2. 25MHz
3. 27MHz
4. 32.768 KHz RTC

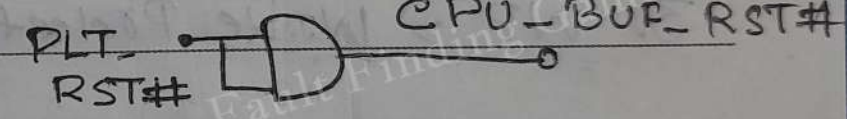
Date : / /

③

Note:- if 25MHz external PCH crystal is not working We have No Display. (Low Ampere). (Power on but no Display)

At that time if you Do the Bios then it could not work. (frequency is missing)

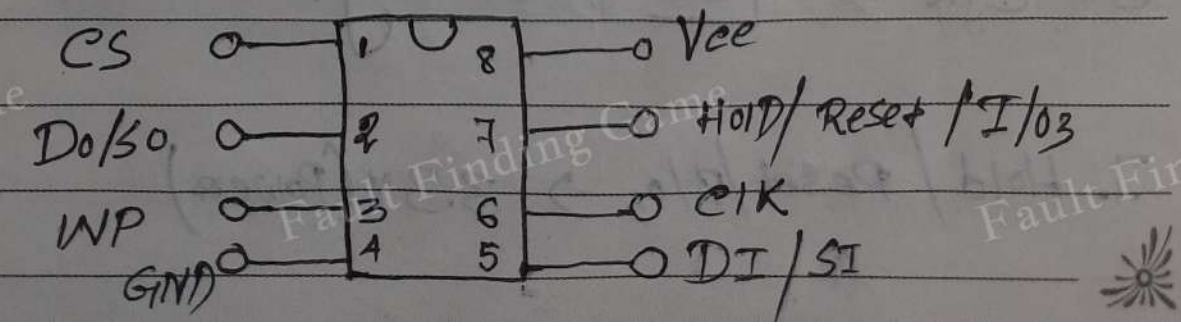
4. Clock is Distributed to the entire MBD & PLT_RST# is created by the PCH.



5. PLT_RST# is Auto enable the CPU & CPU ~~read~~ Stoart reading the Bios.

6. Now Data is created.

Main Bios (PCH Bios)

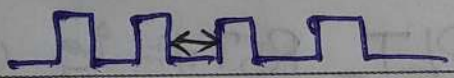


④ Date : / /

Pin Details With Graph

1. CS → Chip Select
   1. Chip Select
   2. RAM Select

2. Do/So → Data out / system out.
   1. Data output



3. WP → Write Protect (3.3V) (Power)

4. GND →

5. DI/SI → Data input / system input

6. Clk → Fix frequency.

7. Hold / Reset / $\overline{WP}$ → 3.3V (Power)

⑤ Date : / /

Vcc :- 3.3V Power.

So, for No Display Case
We Have to Check.

1. After Power
2. LPC_Clk & PCI-CLK 33MHZ DSO
3. ~~[redacted]~~ Check for PLT_RST# 3.3V.
4. Bios input & out Data.
5. LAD → Data. (LPC)

Remember This :-

PCH ↔ I/O → Communication occurs through LPC Bus

PCH ↔ Bios → SPI Bus Communication

Date : / /

* Note a very important Point here

On the SPI Communication line - There Was 2 resistance present on the Bios Data input or system input (DI/SI) line & Bios Data out or system out (Do/So) line.

This 2 resistor has low Value with very low tolerance level. (%1)

This resistor Carry Data with high frequency they tends to Break.

Means → Value Shift.

CPU & PCH.

Communication happens through DMI & FDI Path

CPU  RAM → Communication happen through SM Clock & SM Data *

(7) Date : / /

CPU RESET, DRAM ... RST#

RAS,

CAS,

Write Enable etc.

Now The important Note is:-

All the Communication line Should be Connected ProPerly (may be directly or through resistor)

if track in open or high resistance is present on the Communication line then You have a big Problem.

most cases We found that our Data line with high frequency track resistance gone bad.

Because This line carry high Current With Data Clock & Data line Must Check thoroughly

Date : / /

(8)

IO ⟷ Bios (EE Bios) Communication happen throug SPI lines

LAN Connector Data

OR ↕ ⟷ PCH

WLAN (Mini wifi card Data)

Communication happen through PCIE interface.