FAULT FINDING GAME

THEORY
&
PRACTICAL

Voltage SEQUENCE OF

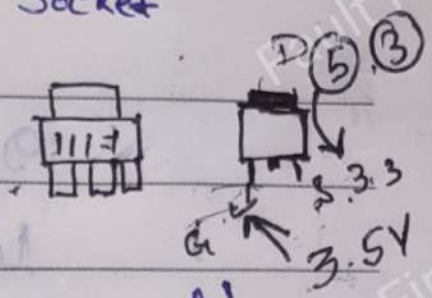
945, G41 G31
H55, H61
H81
H110
H310

STEP BY STEP VOLTAGE FORMATION AND THERE LOCATION ON MOTHERBOARDS

AMD PGA Pin Grid Array Voltage Sequence. LGA → Land Grid Array

Date: 03/12/23

G31, G41, 945 775 Socket



1. 3.3V LDO
2. RTC vee → SW
3. 3.3V Conversion (3.3V Dual)
4. 5V Conversion (5V Dual)
5. 1.8V or 1.5V Ram (DDR2 or DDR3)
6. VTT RAM (Half of Ram Voltage)
7. 1.05V Ich
9. 1.25V GMCH
10. 1.2V GMCH VTT
11. Vcore

H55, H61 1st & 2nd & 3rd gen (LGA 1155)

1. 3.3V LDO
2. RTC vee
3. 3.3V Conversion
4. 5V Conversion
5. 1.5V DDR
6. DDR VTT (0.75V)
7. 1.05V PCH
8. 1.8V CPU PLL

Date : / /

9. CPU VTT 1.05V

10. CPU Vcore

11. CPU GFX

H81 4th & 5th gen (LGA 1150)

Note :- 4th & 5th gen CPU has Fivr technology.

Fivr → Fully integrated Voltage regulator. (6 regulators inside the CPU)

1.8V
VccSA } ect
VccST }
VccIO

1. 3.3V LDO
2. RTC Vcc
3. 3.3 & 5V Conversion
4. 1.5V RAM
5. 0.75V VTT for RAM

Date : / /

6. 1.05V PCH
7. 1.5V PCH
8. Vcore for CPU

No GFX in present on this 4th generation. H81
Because of Fivr tech.

H110. 6th & 7th gen (1151)

1. 3.3V LDO
2. RTC Vee
3. 3 & 5V Conversion (Dual)
4. 1.2V VDDQ
5. 0.6V DDR VTT
6. 2.5V VPP
7. 1.05V PCH
9. VCCSA
10. VCCIO
11. VCCST_VCCPLL
12. VCore
13. VCCGT

Date : / /

Some of H110, H310 No Difference (1151)

8th & 9th gen

1. 3.3V LDO
2. RTC vee
3. 3.3 & 5V Conversion (Dual)
4. 1.2V VDDQ
5. 0.6V VTT RAM
6. 2.5V VPP
7. 1.0V PCH
8. VccSA
9. VccIO
10. VccST_ VccPLL
11. CPU VCore
12. CPU GT

VccSA = 1.05V

VccIO = 0.95V

VccST_ VccPLL = 1V