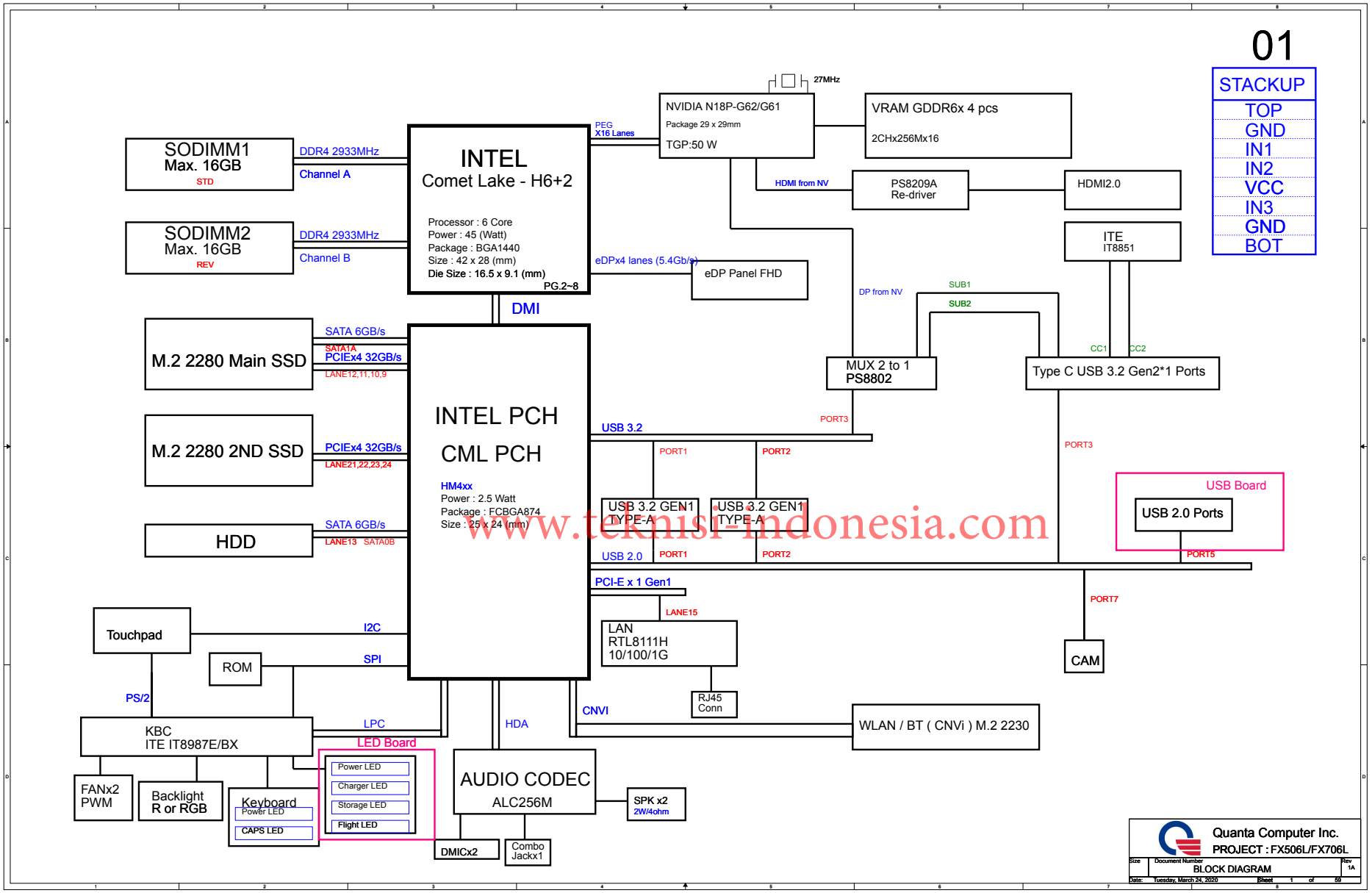

Model

FX506LT
FX706LT

REV

ER

PR

CHANGE LIST

Item	Stage	Page	Owner	Change explanation
01	ER	29	EE	ER-E00:Del RUN_ON for 1.2V_MUX enable....1113
02	ER	29	EE	ER-E01:Change G9090 to G9661 to solve PD issue.and +1.2V_HDMI ripple issue....1113
03	ER	29	EE	ER-E02:Add N-MOSFET to +1.2V_HDMI for ripple issue....1113
04	ER	39	EE	ER-E04:Change +1.2V to +1.2V_HDMI power rail name....1113
05	ER	29	EE	ER-E05:Del +3V power rail and SR9 and SR7 to shortpad....1113.
06	ER	29	EE	ER-E06:Change +3V_PD to LDO for ripple issue....1113.
07	ER	39	EE	ER-E07:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113
08	ER	29	EE	ER-E08:No mount SR82 for surge issue....1113.
09	ER	29	EE	ER-E09:DEL PD to MUX SMBUS....1113.
10	ER	29	EE	ER-E10:Change no mount:SQ1,SR66,SR67, NO USED....1113.
11	ER	39	EE	ER-E11:Change no mount:HQ3, NO USED....1113.
12	ER	29	EE	ER-E12:Change SR61,SR62,SR63 TO NO-MOUNT for shortpad....1113.
13	ER	11	EE	ER-E13:Change R206 TO NO-MOUNT for shortpad....1113.
14	ER	16	EE	ER-E14:Change R858 and C1094,R856 TO NO-MOUNT....1113.
15	ER	7	EE	ER-E15:Change C269 1000P to 10U_4 for power ripple....1113.
16	ER	18	EE	ER-E16:Add 0.1U near MR5....1113.
17	ER	19	EE	ER-E17:Add 0.1U near MR10....1113.
18	ER	32	EE	ER-E18:Change C1116 *47U to 10U_4 for ripple....1113.
19	ER	22	EE	ER-E19:Change GPIO27_IFPC_HPD to GPIO27_IFPC_HPD# for Low active....1113.
20	ER	22	EE	ER-E20:Change GPIO18_IFPE_HPD to GPIO18_IFPE_HPD# for Low active....1113.
21	ER	28	EE	ER-E21:Del RP1/RP2/RP3/RP4 and EMI by pass for EMI request....1113.
22	ER	07	EE	ER-E22:Change C289,C73,C72 From 47uF to 22uF for PASS VRTT...1119
23	ER	29	EE	ER-E23:Change SU10 part number for E ver and 08FW to fix PD2.0 fail issue....1120.
24	ER	36	EE	ER-E24:Change KR122 0ohm to no-mount for no support....1120
25	ER	28	EE	ER-E25:Change EMIL5,EMIL6 to BLM15AG221SN1D and C1072 C1073 to 10P For EMI issue and signal pass....1122.
26	ER	31	EE	ER-E26: Change 2.1ohm to 5.1ohm for fix TDR issue....1122.
27	ER	12	EE	ER-E27: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.
28	ER	23	EE	ER-E28: Change VR113 to 10K6for fixed GPU timing issue....1122.
29	ER	34	EE	ER-E29: Change C355,C356 to no-mount for fix TP timing issue....1122.
30	ER	35	EE	ER-E30:Add AR47 moat resistor between AGND&DGND and connect to AU1 pin20 for active speaker noise issue in S5...1122.
31	ER	37	EE	ER-E31:Del KQ15/KQ13 for no support Red backlight....1125.
32	ER	53	Power	ER-001:PR358 from 100ohm to 105ohm for +1.0V_GPU output voltage.
33	ER	48	Power	ER-002:Add PC169 & PC170 47pF for ASUS SOW.
34	ER	41	Power	ER-003:Change PR1093 from 16.9k to 1.87k to set IA iccmax 128A for CMH base.
35	ER	41	Power	ER-004:Change PC1081 from 68pF to 330pF to correct L- DCR matching.
36	ER	41	Power	ER-005:Change PR1078 from 422 to 412 ohm to to set OCP 180A for H62.
37	ER	41	Power	ER-006:Change PC1068 from NI to 47nF to correct L-CDR matching.
38	ER	41	Power	ER-007:Change PR1057 from 107k to 113k to correct IMONA for H62.
39	ER	41	Power	ER-008:Change PR1078 from 365 to 287 ohm to set OCP 116A for H42.
40	ER	41	Power	ER-009:Change PR1057 to 76.8k to correct IMONA for H42.
41	ER	41	Power	ER-010:Change PR1070 from 5.11k to 3.48k to correct DCLL for H42.
42	ER	43	Power	ER-011:PC1333,PC1334,PC1335,PC1336,PC1337,PC1338 add 22uF to pass Intel 20mV Ripple voltage at PS0 , original 25mV Ripple failure Intel Ripple voltage spec for H62/H42 GT.
43	ER	41	Power	ER-012:Change PC1044 from 10nF to 15nF to correct L DCR matching for H62/H42 SA.
44	ER	41	Power	ER-013:Change PC1050 from 220pF to 680pF to reduce undershoot for H62/H42 SA.
45	ER	47	Power	ER-014:Delete PD13 & PD14 for SHDN# issue.
46	ER	47	Power	ER-015:PC157 1000P change to 2200P for meet HDD rise time SPEC.
47	ER	47	Power	ER-016:PC164 1000P change to 680P for meet TP rise time SPEC.
48	ER	45	Power	ER-017:PR642 change to 6.49K+-1% for output voltage up.
49	ER	49	Power	ER-018:PD11 & PQ40 change mount & PR240 change no-mount for ADP plug-out issue.
50	ER	41~55	Power	ER-019:0ohm change to short pad.
51	ER	44~53	Power	ER-020:Remove output short pad.
52	ER	45	Power	ER-021:PU1327 all component change to non-mount & +1.05V_VCCSTG source change to PU32 side for EE request.
53	ER	35	EE	ER-E31:AR14 and AR5 change from 22 ohm to 10 ohm increasing the FSOV margin.
54	ER	30	EE	ER-E32:Remove CON6 for USB board FFC CONN
55	ER	47~49	Power	ER-022:Add test point PTP1~PTP6 for ASUS request.
56	ER	47	Power	ER-023:Reserve PEC61 0.1uF for EMI request.
57	ER	30	EE	ER-E33:Reserve CON6 for USB board FFC CONN
58	ER	31	EE	ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brigtness
59	ER	49	Power	ER-024:PR238 change to 0ohm & PR232 change to 16Kohm for Psys Pmax setting.
60	ER	16	EE	ER-E35:Reserve U26 for C10 GATE# support.
61	ER	48	Power	ER-025:PCN1 change to DFHD06MR208 for blistering issue, so the manufacturer changed the material from PA6T CHANGE TO LCP.
62	ER	35	EE	ER-E36:AL5,AL6 change to CX801T20001 and AR14,AR15 change to 22 ohm for FSOV
63	ER	17	EE	ER-E37:Add EMIC87,EMIC88 for RF
64	ER	29	EE	ER-E38:SU12 change from SY6863B3ABC to G518B1TP1U, SR55 change to 18.7K, SR54 change to 8.87K for ILIM.
01	PR	35	EE	PR-E01:ACN1 Change PIN Define
02	PR	30	EE	PR-E02:Remove CON6 for USB board FFC CONN
03	PR	29	EE	PR-E03:Mount SU15 for DP HPD
04	PR	14	EE	PR-E04:Add BOARD ID0 difine for i7&i5
05	PR	17	EE	PR-E05:Add EMC89/EMC91/EMC93 0.1uF and EMC90/EMC92/EMC94 for EMI, EMC89 and EMC90 un-mount for Height limitation
06	PR	30	EE	PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF
07	PR	17	EE	PR-E07:EMIC35/EMIC57/EMIC38/EMIC42 change from 100p to 2200p, EMIC37/EMIC47/EMIC40 change from 100p to 0.1u for EMI
08	PR	39	EE	PR-E08:HDMI DDC pull-up resister HR20/HR21 change from 2.2K to 3K for HDMI protocol issue
09	PR	48	Power	PR-001:Add PEC27 0.1uF for EMI request.
10	PR	49	Power	PR-002:Add PEC28 2200pF for EMI request.
11	PR	4/11	EE	PR-E09:mount R190, R193, R12 and remove R872, R873 for HDMI lag issue
11	PR	37	EE	PR-E10:KR84, KR86 change from 220 ohm to 2.2K ohm for ID KB LED brightness request.

DOC NO.	PROJECT MODEL :	BKLG/BKLH	APPROVED BY:		DATE:	2018/01/17
	PART NUMBER:		DRAWING BY:		REVISON:	1A

02

Quanta Computer Inc.
PROJECT : FX506L/FX706L
POWER UP SEQUENCE
Rev 1A
Tuesday, March 24, 2020

Comet Lake Processor (CLK,MISC,JTAG)

03

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

Processor Strapping

The CFG signals have a default value of "1" if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;

Mark eDP mode Enabled

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Configuration Signals:		The CFG signals have a default value of "1" if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to **HOOK[2]. This route is not needed on a OxM board.**	
CFG[2]	**PCI Express Static Lane Reversal**	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE
Close to CPU
SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS
Close to CPU
SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS
Close to CPU
SVID DATA

CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

Under CPU

Placement close to CPU.

11/21 updated FP

Quanta Computer Inc.
PROJECT : FX506L/FX706L
CML 1/7 (JTAG/MISC)
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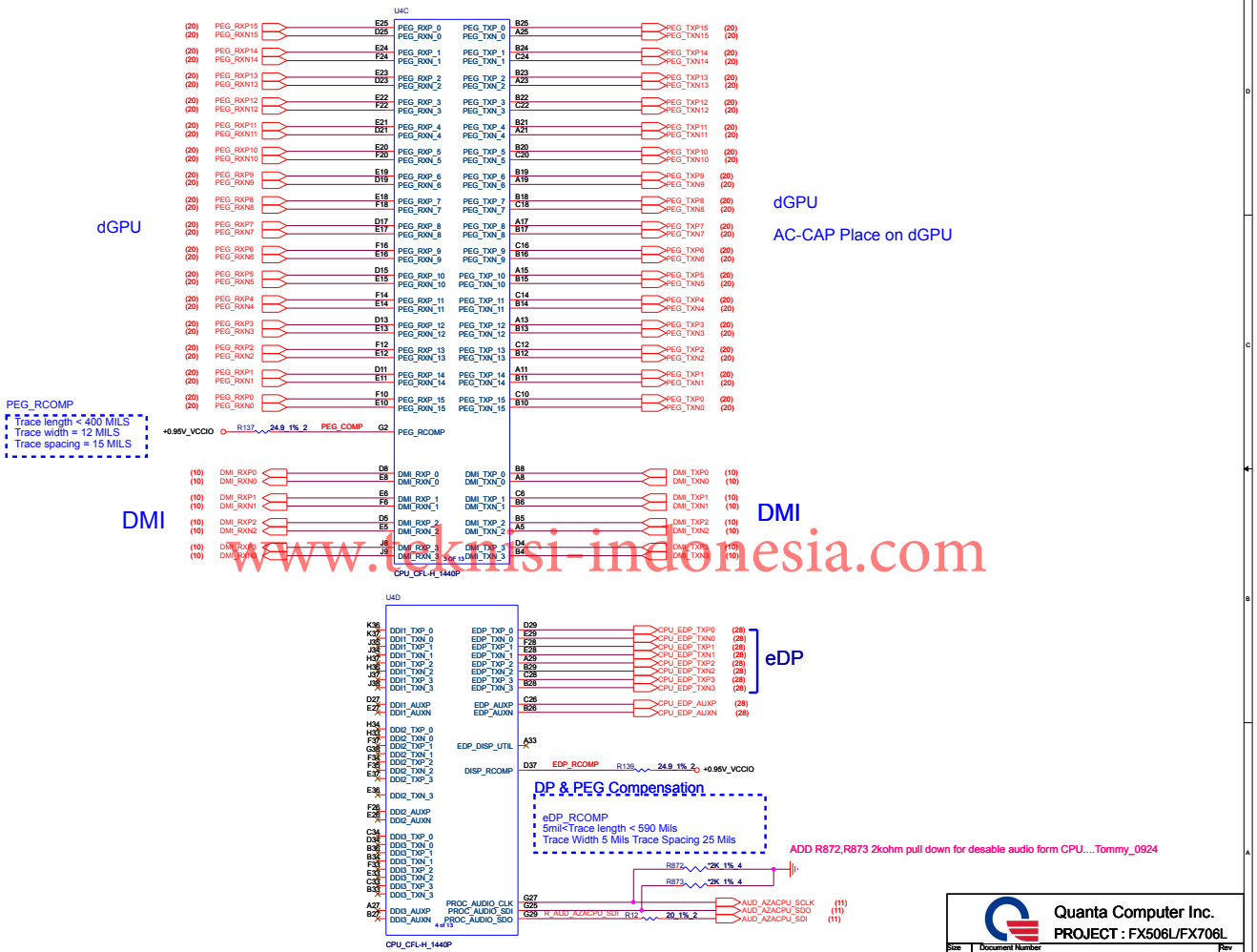
Comet Lake Processor (DMI,PEG,FDI)

04



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PROJECT : FX506L/FX706L

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	CML 2/7 (DMI/EDP/PEG)	2A

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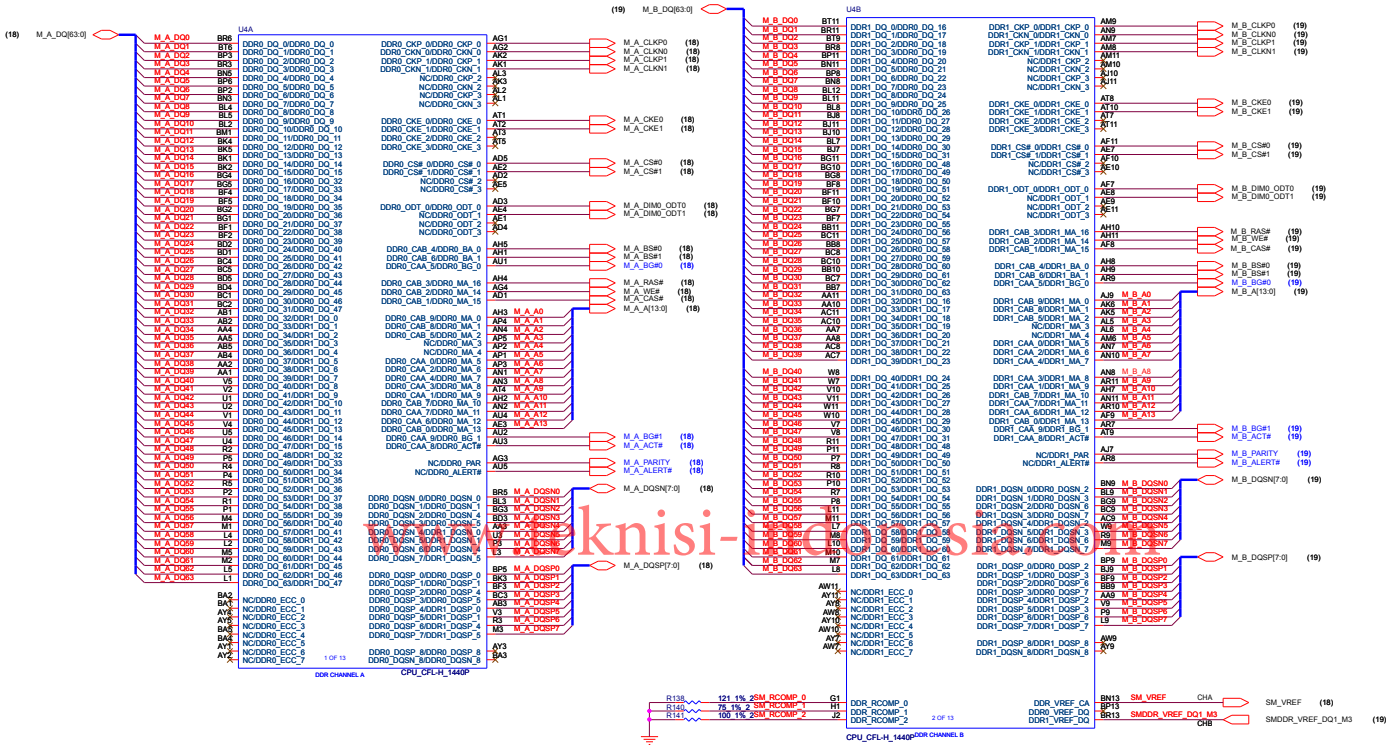
Comet Lake Processor (DDR4)

Interleaved

05



Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	CML 3/7 (DDR4 I/F)	2A

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CML Processor (POWER)

06

Follow CML H page 126 to 45W(GT2): +VCCGT=32A

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	CML 4/7 (POWER/GT)	2A

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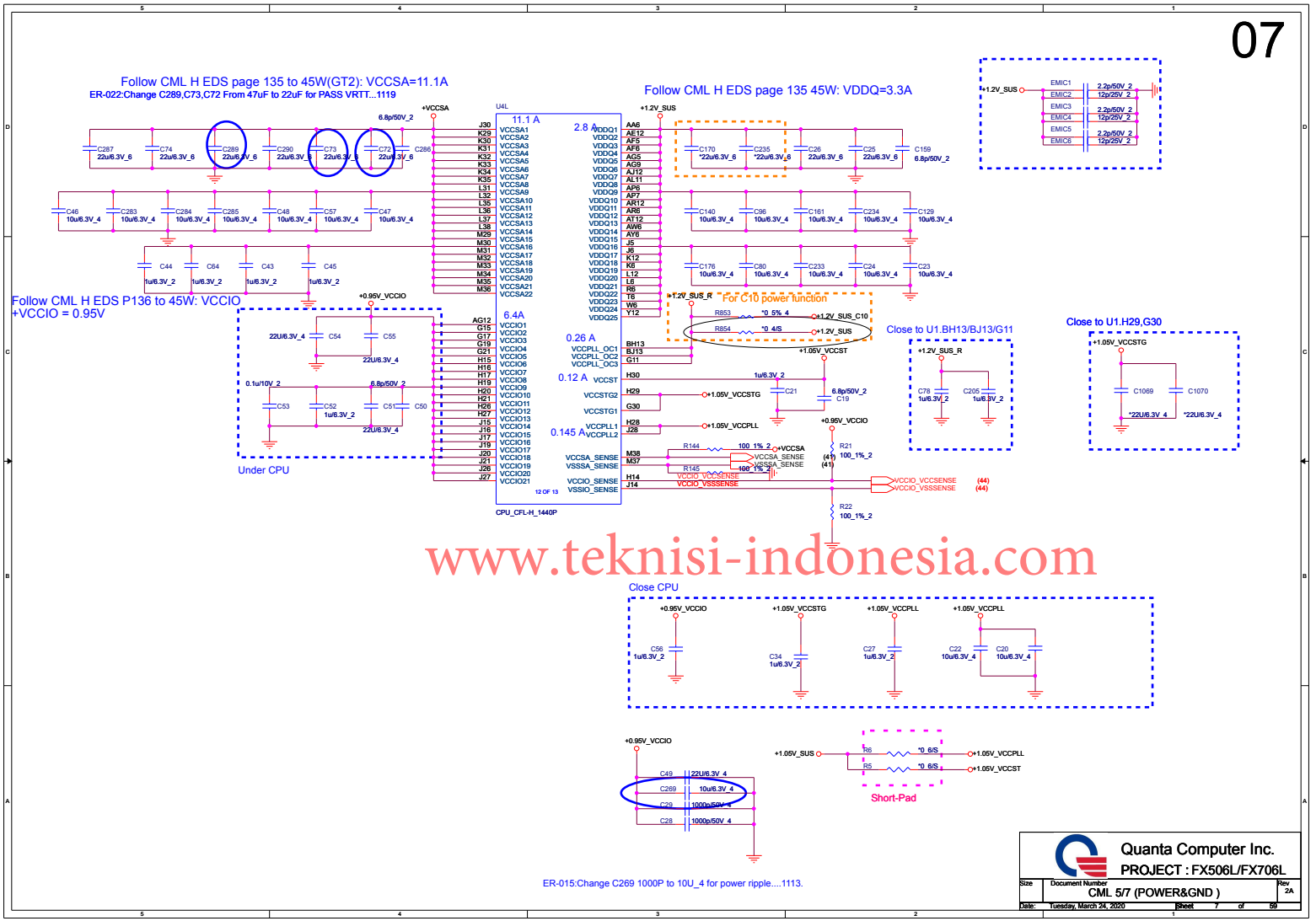
Follow CML H EDS page 135 to 45W(GT2): VCCSA=11.1A
ER-022:Change C289,C73,C72 From 47uF to 22uF for PASS VRTT...1119
Follow CML H EDS page 135 45W: VDDQ=3.3A
Follow CML H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V
Under CPU
Close to U1.BH13/BJ13/G11
Close to U1.H29,G30
For C10 power function
Close CPU
Short-Pad
CPU_CFL-H_1440P
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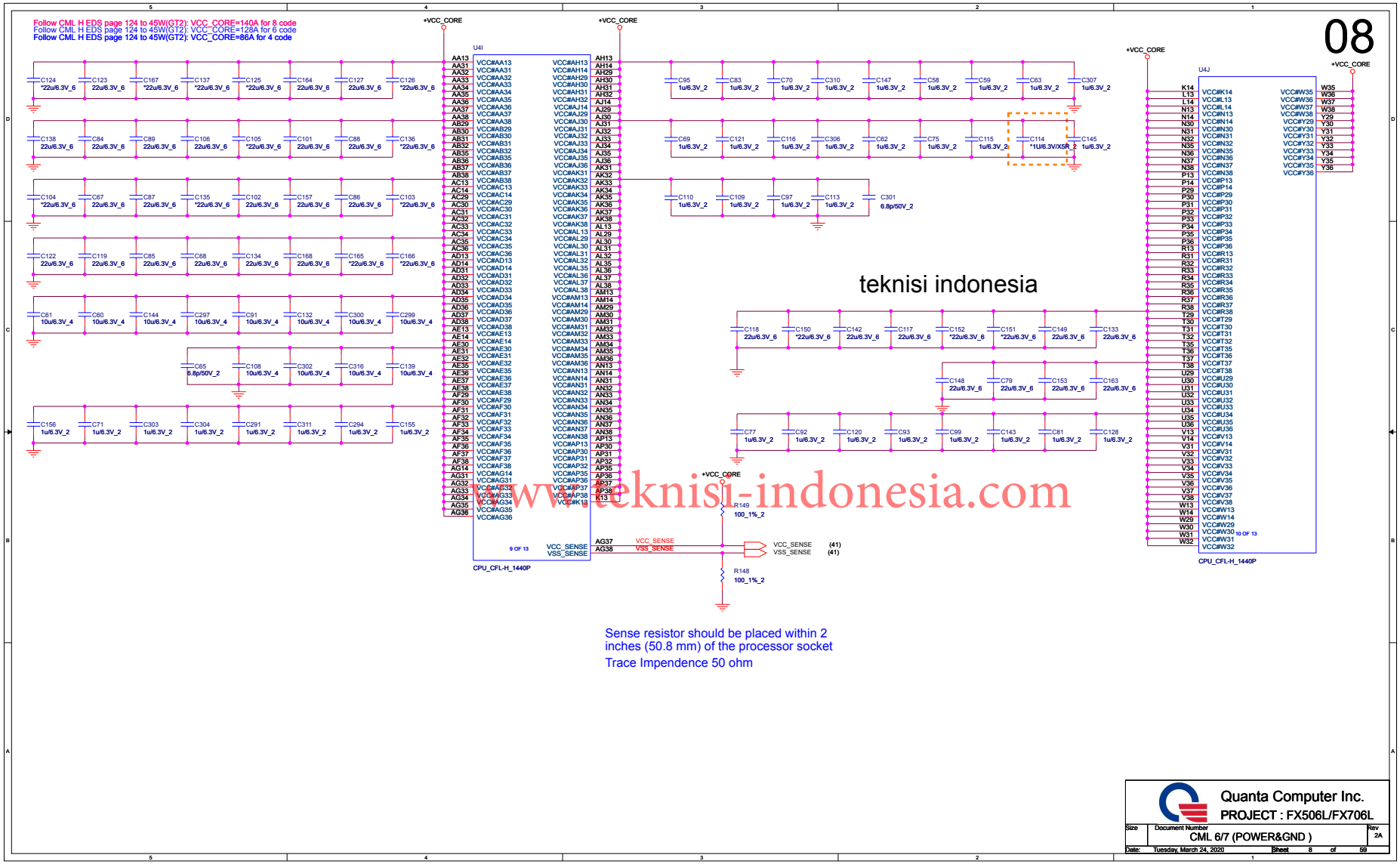
ER-015:Change C269 1000P to 10U_4 for power ripple....1113.
Quanta Computer Inc.
PROJECT : FX506L/FX706L
CML 5/7 (POWER&GND)
Tuesday, March 24, 2020


Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=140A for 8 code
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=128A for 6 code
Follow CML H EDS page 124 to 45W(GT2): VCC_CORE=86A for 4 code
08
+VCC_CORE
U4I
U4J
CPU_CFL-H_1440P
VCC_SENSE
VSS_SENSE
R149
100_1%_2
R148
100_1%_2
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impendence 50 ohm
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PROJECT : FX506L/FX706L
CML 6/7 (POWER&GND)
Tuesday, March 24, 2020
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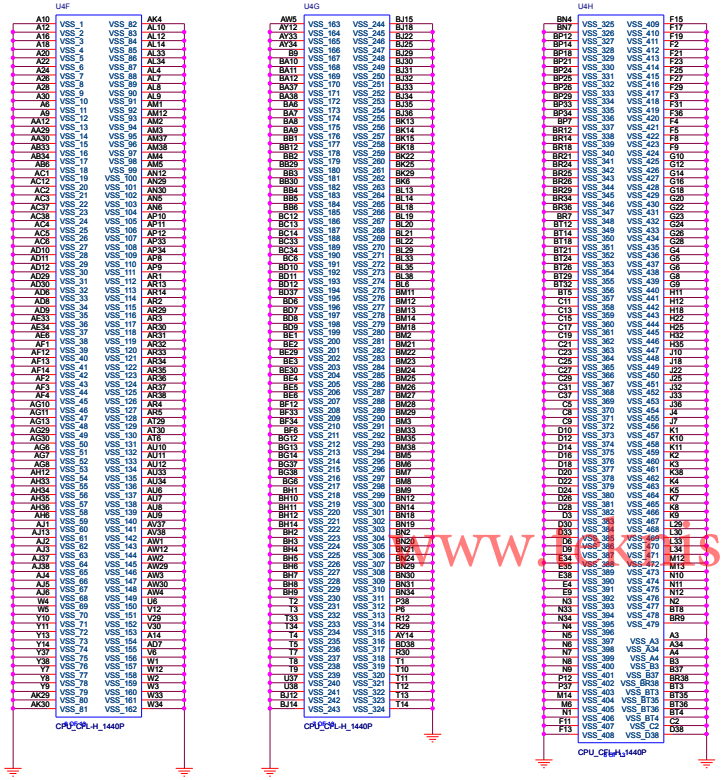
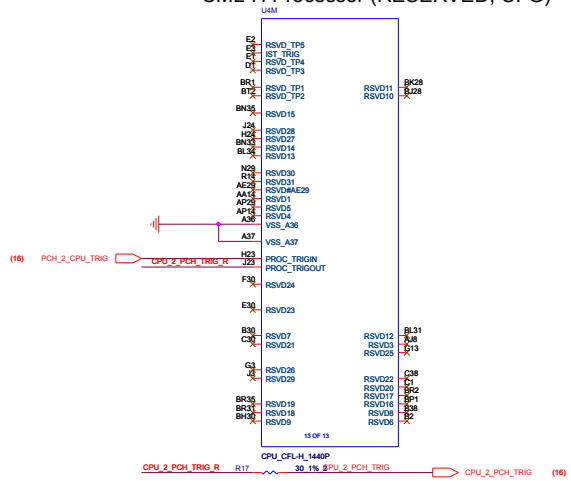
CML-H Processor (GND)



CML-H Processor (RESERVED, CFG)



Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	CML 7/7 (GND)	2A

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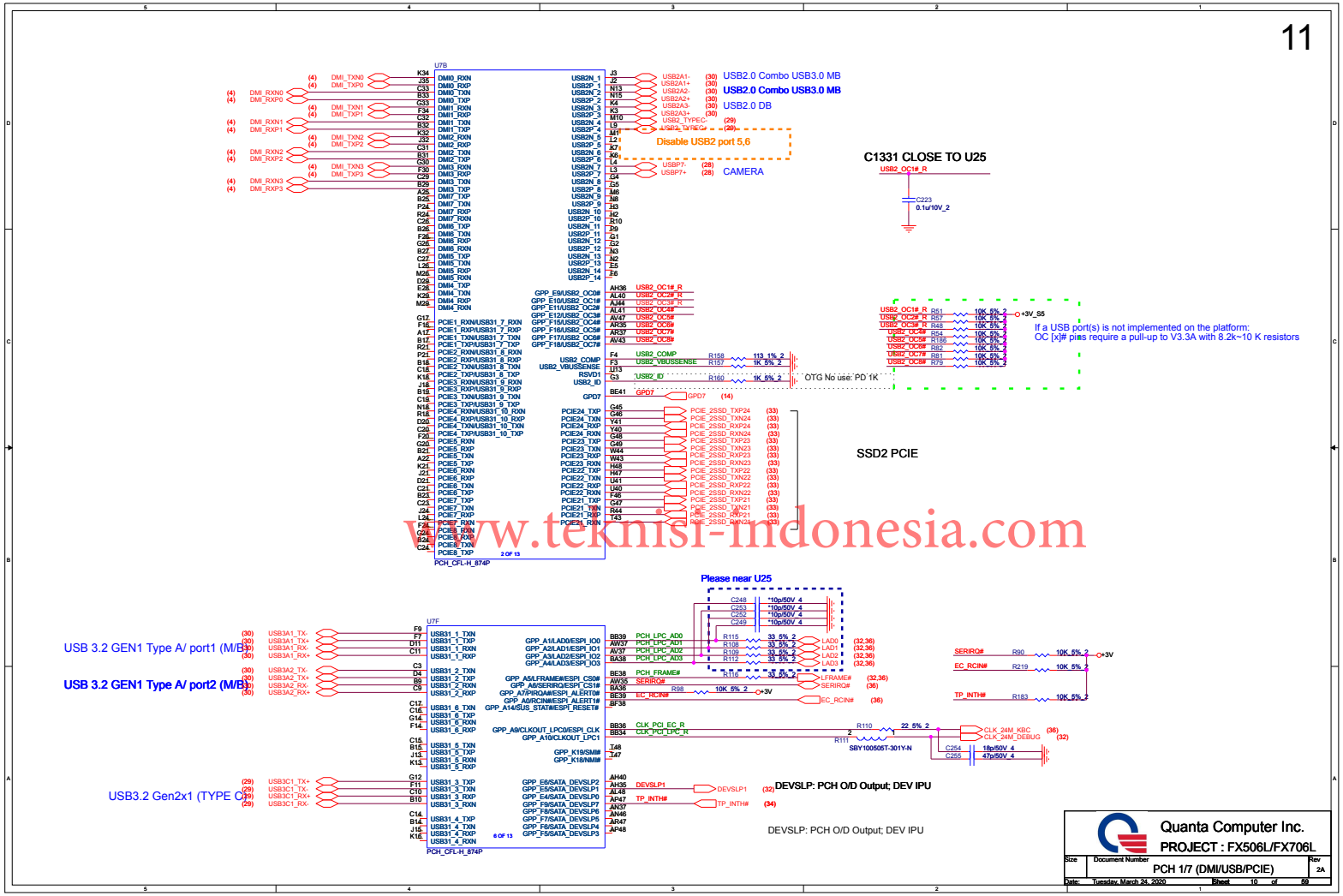

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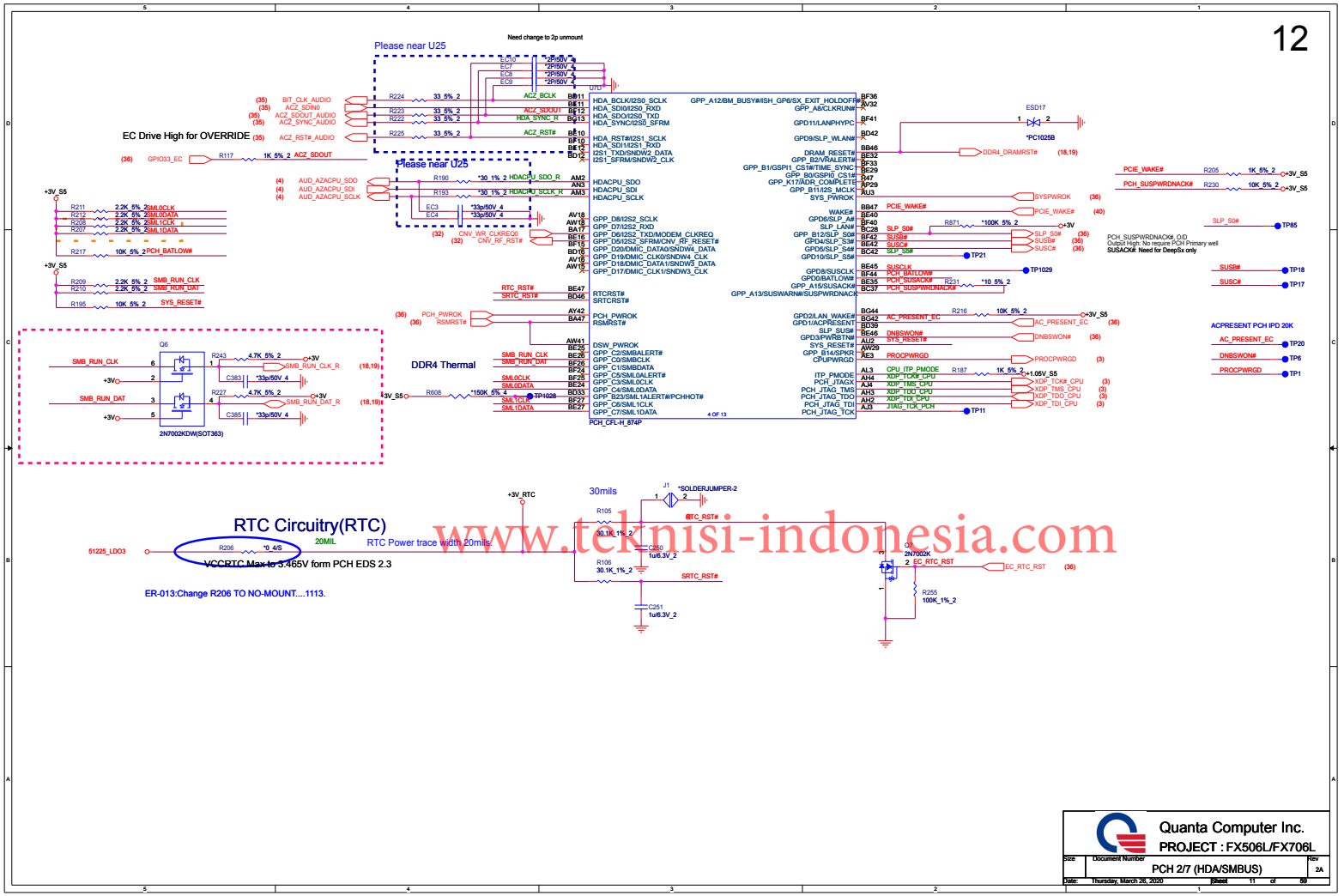
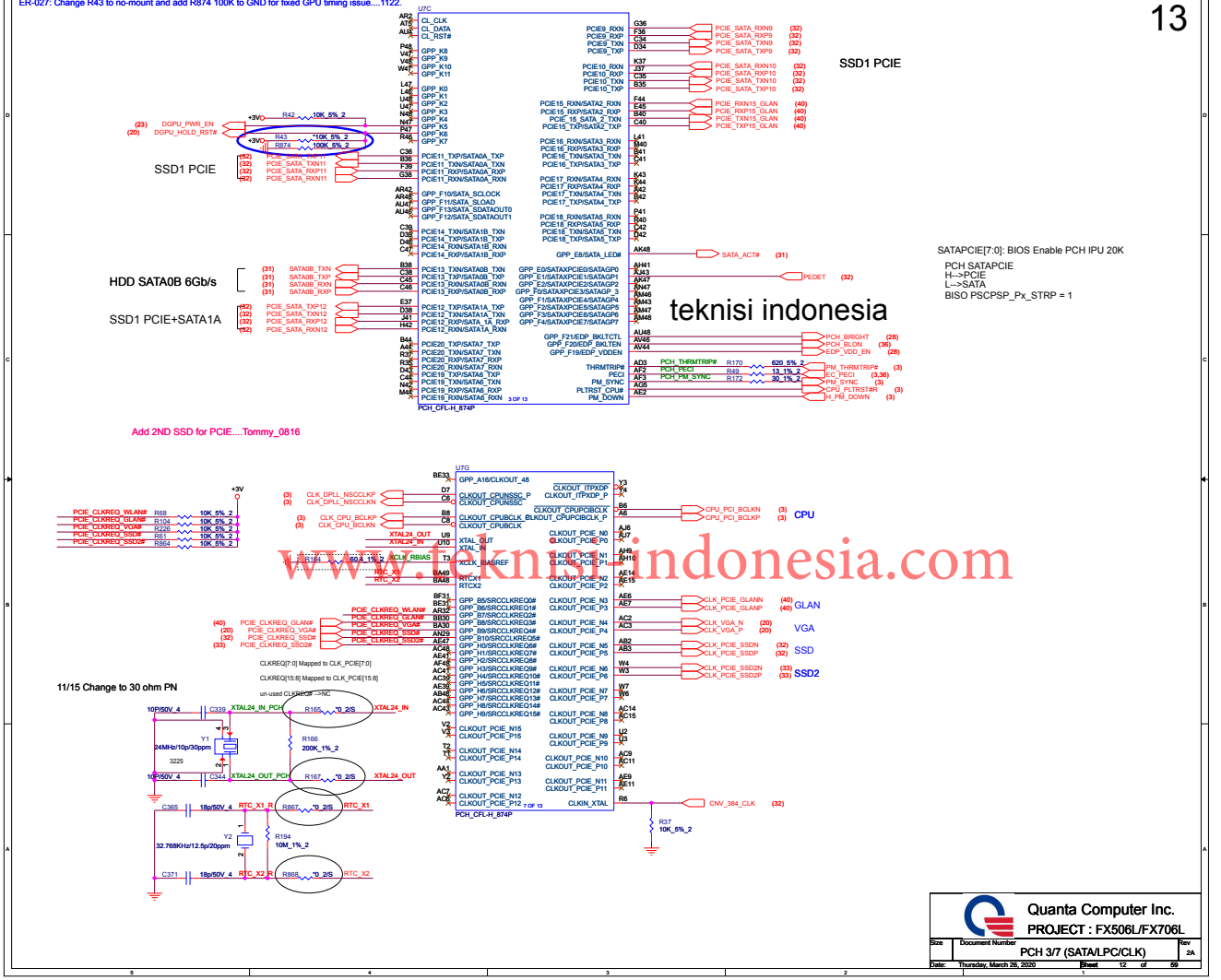


ER-027: Change R43 to no-mount and add R874 100K to GND for fixed GPU timing issue....1122.



Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	PCH 3/7 (SATA/LPC/CLK)	2A

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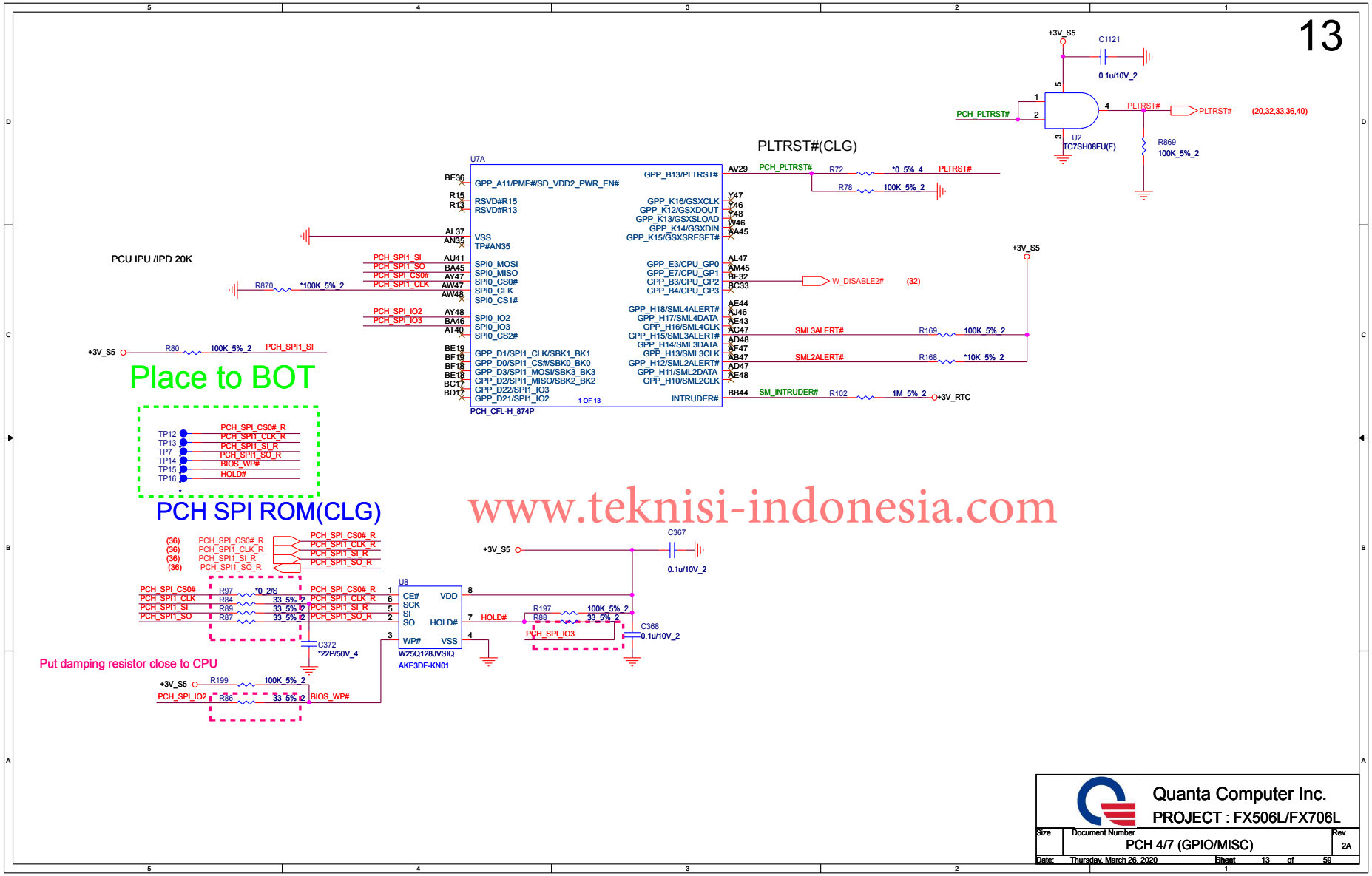

Quanta Computer Inc.			
PROJECT : FX506L/FX706L			
Size	Document Number		Rev
	PCH 4/7 (GPIO/MISC)		2A
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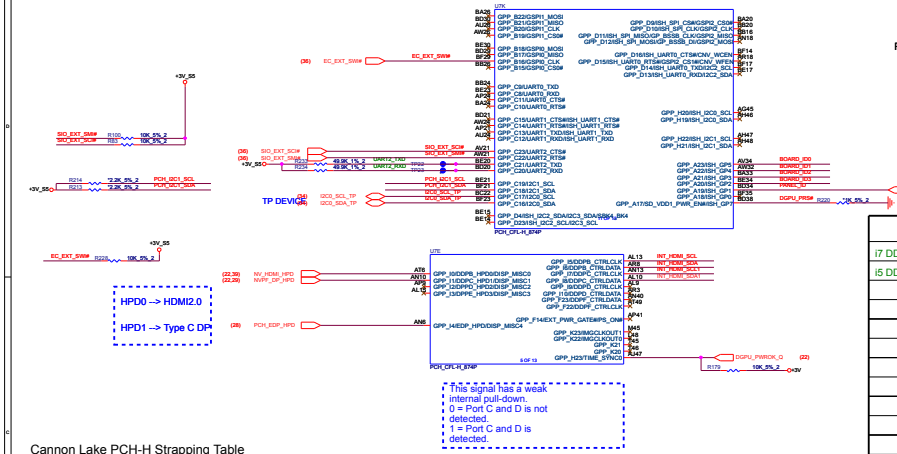

	BOARD_ID0	
i7 DDR 3200MHz	0	
i5 DDR 2933MHz	1	

Cannon Lake PCH-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	**PCH_PWROK**	**0 = *Disable Top Swap (IPD 20K) Default** 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) Default **1 = Enable No Reboot Mode**	
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	**0 = *Disable Intel ME Cryp to TLS(IPD 20K) Default** **1 = Enable Intel ME Cryp to TLS** PU to support AMT TLS	
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	**0 = *SPI (IPD 20K) Default** **1 = LPC**	
GPP_C5 (SMLDALERT#)	eSPI or LPC	RSMRST#	**0 = *LPC is selected for EC (IPD 20K) Default** **1 = eSPI selected for EC**	
SPI0_MOSI	Reserved	RSMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(IPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO2	Reserved	RSMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	
SPI0_IO3	Reserved	RSMRST#	(IPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	**0 = *Enable security in the Flash Description (IPD 20K) Default** **1 = Disable Flash Descriptor Security (Override)**	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSMRST#	**0 = *Master Attached Flash Sharing (MAFS) enabled (IPD 20K)Default** **1 = Slave Attached Flash Sharing (SAFS) enabled.**	Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	**0 = *Port B is not detected (IPD 20K) (Default)** **1 =Port B is detected**	Change R58,R59,R843,R842 mount to no mount for no support DDI....Tommy_0903
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	**0 = *Port C is not detected (IPD 20K) (Default)** **1 =Port C is detected**	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	**PCH_PWROK**	**0 = *Port D is not detected (IPD 20K) (Default)** **1 =Port D is detected**	
GPP_F23	**Display Port F Detected**	**PCH_PWROK**	0 = *Port F is not detected (IPD 20K) (Default) **1 =Port F is detected**	CFL - H CPU Not Support DDI Port F
GPP_J4 CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	**RSMRST#**	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. **0 = *38.4MHz XTAL frequency selected. (IPD 20K) (Default)** **1 = 24MHz XTAL frequency selected.**	PCH Strap: GPP_J4 = XTAL SELECT-1 HIGH -> 24 MHZ / LOW -> 38.4 MHZ
GPP_J6 CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	**RSMRST#**	An external pull-up or pull-down is required. **0 = Integrated CNVi enable. (Default)** **1 = Integrated CNVi disable.**	PCH Strap: GPP_J6 = M.2 CNVI STRAP HIGH -> DISABLE / LOW -> ENABLE
GPP_J9	1.8V VCCPSPI	RSMRST#	**0 = *VCCSPI is connected to 3.3V rail. (IPD 20K) (Default)** **1 = VCCSPI is connected to 1.8V rail**	Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	**DSW_PWROK**	This strap should sample HIGH. There should NOT be any on-board device **driving it to opposite direction during strap sampling.**	**External pull-up is required. Recommend 100K.**

Quanta Computer Inc.
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PCH 5/7 (GPIO/PCH STRAPS)
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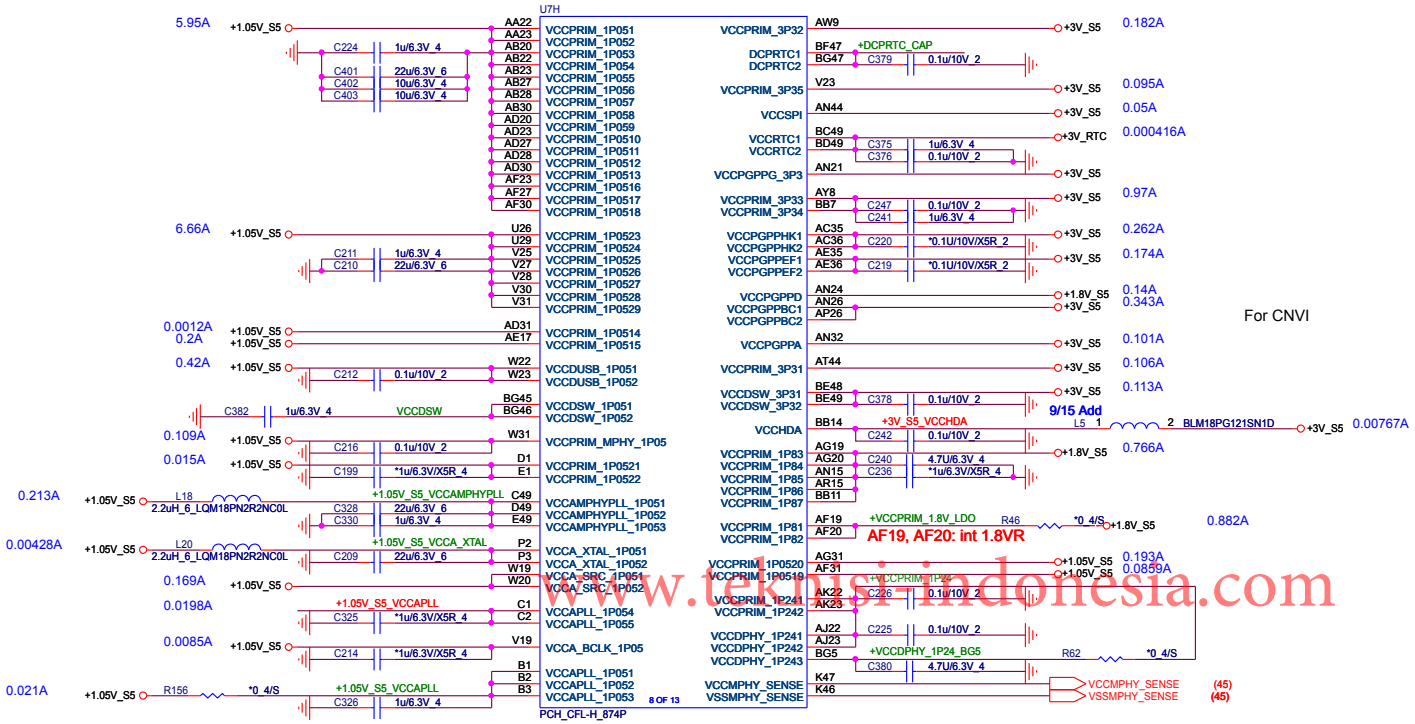
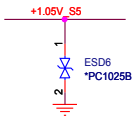
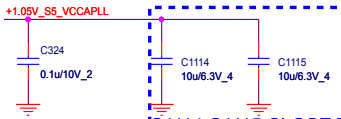
need to add +1.05V power rail



ESD6 CLOSE TO U7



C324 CLOSE TO U7.B2



C1114,C1115 CLOSE TO U7.C1 pin

1.24V for CNVi logic = VCCDPHY_1P24 & +VCCPRIM_1P24
This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.
Refer to the Platform Design Guide for implementation details.

Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
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	PCH 6/7 (POWER)	2A
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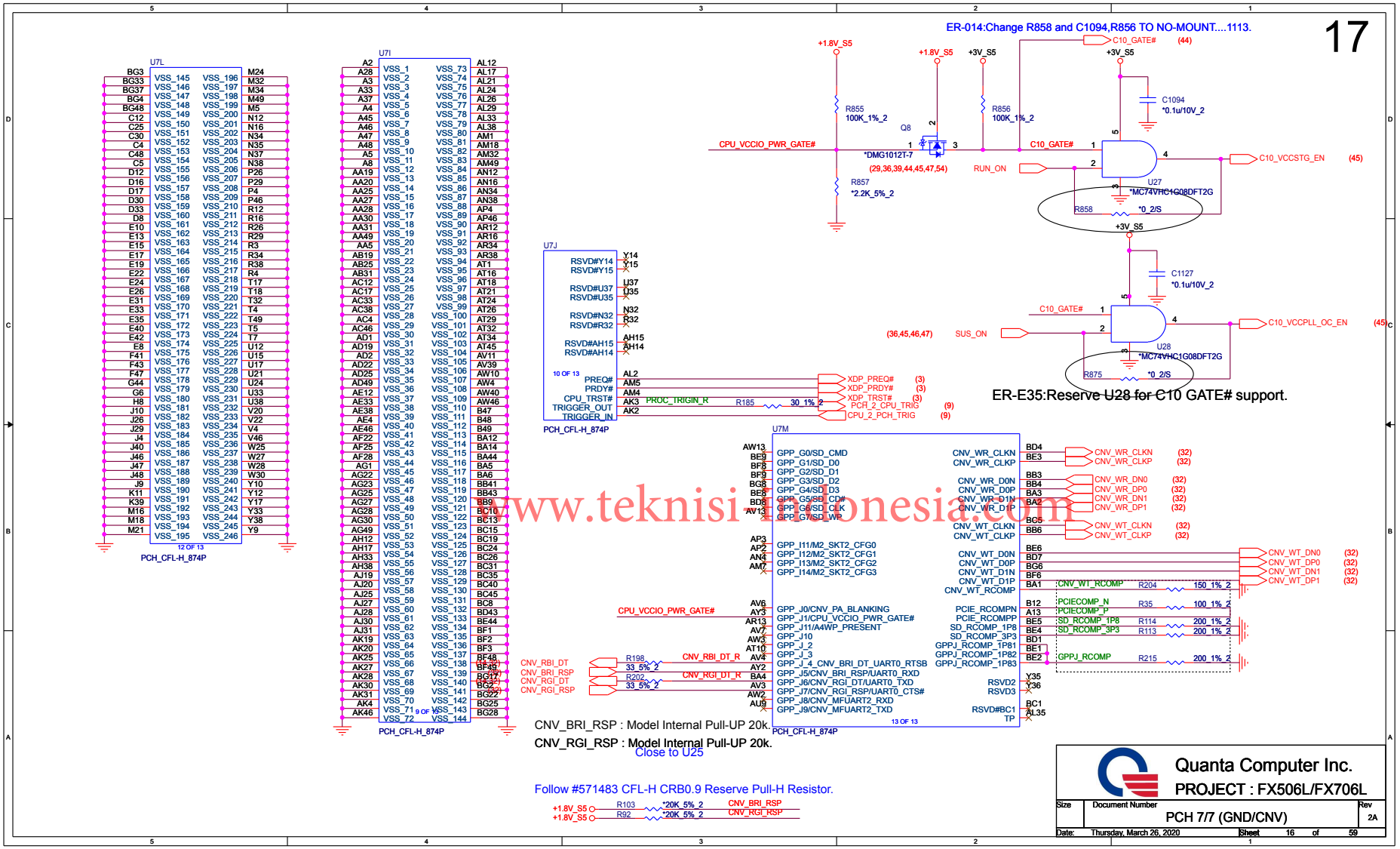

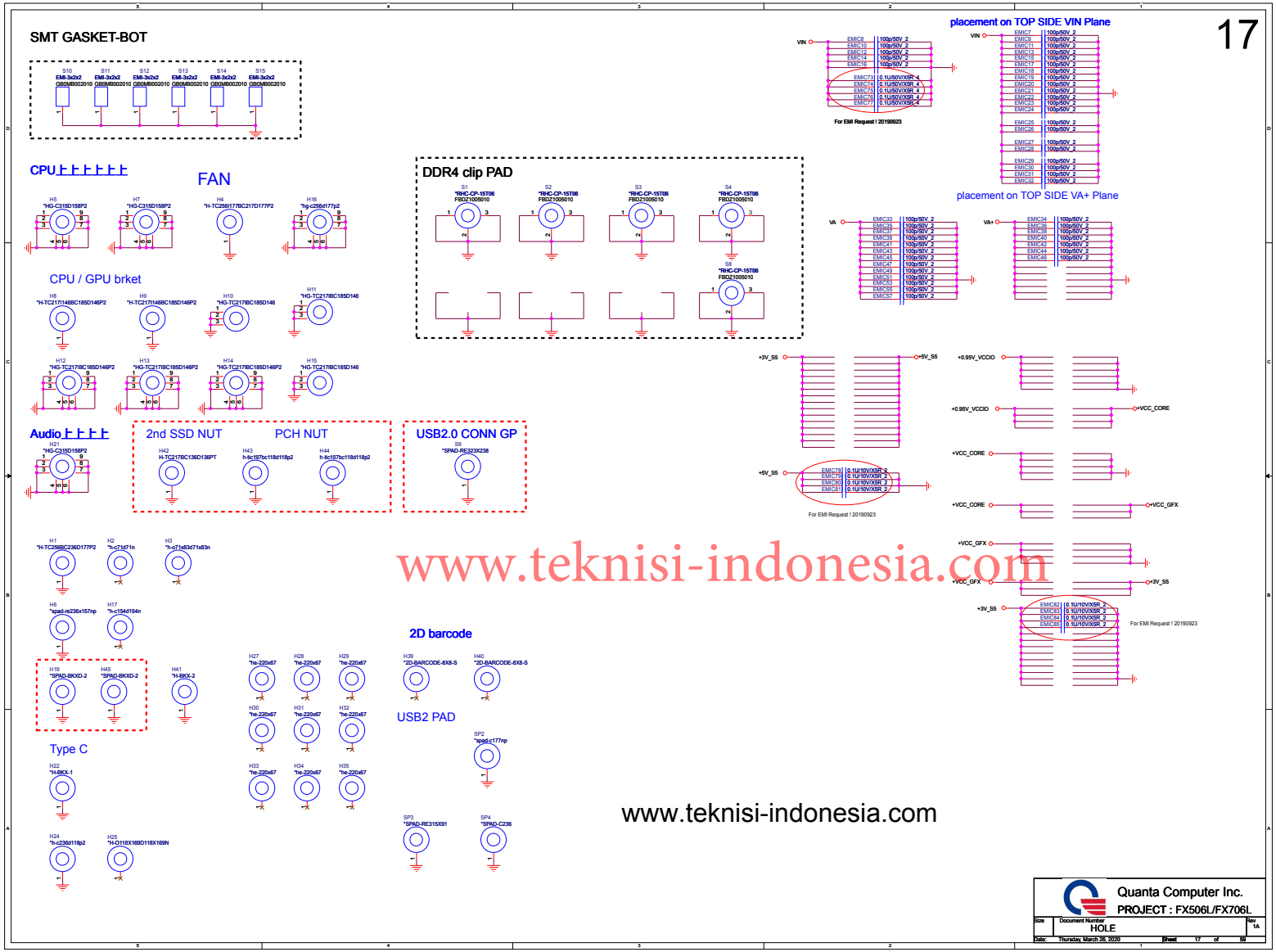

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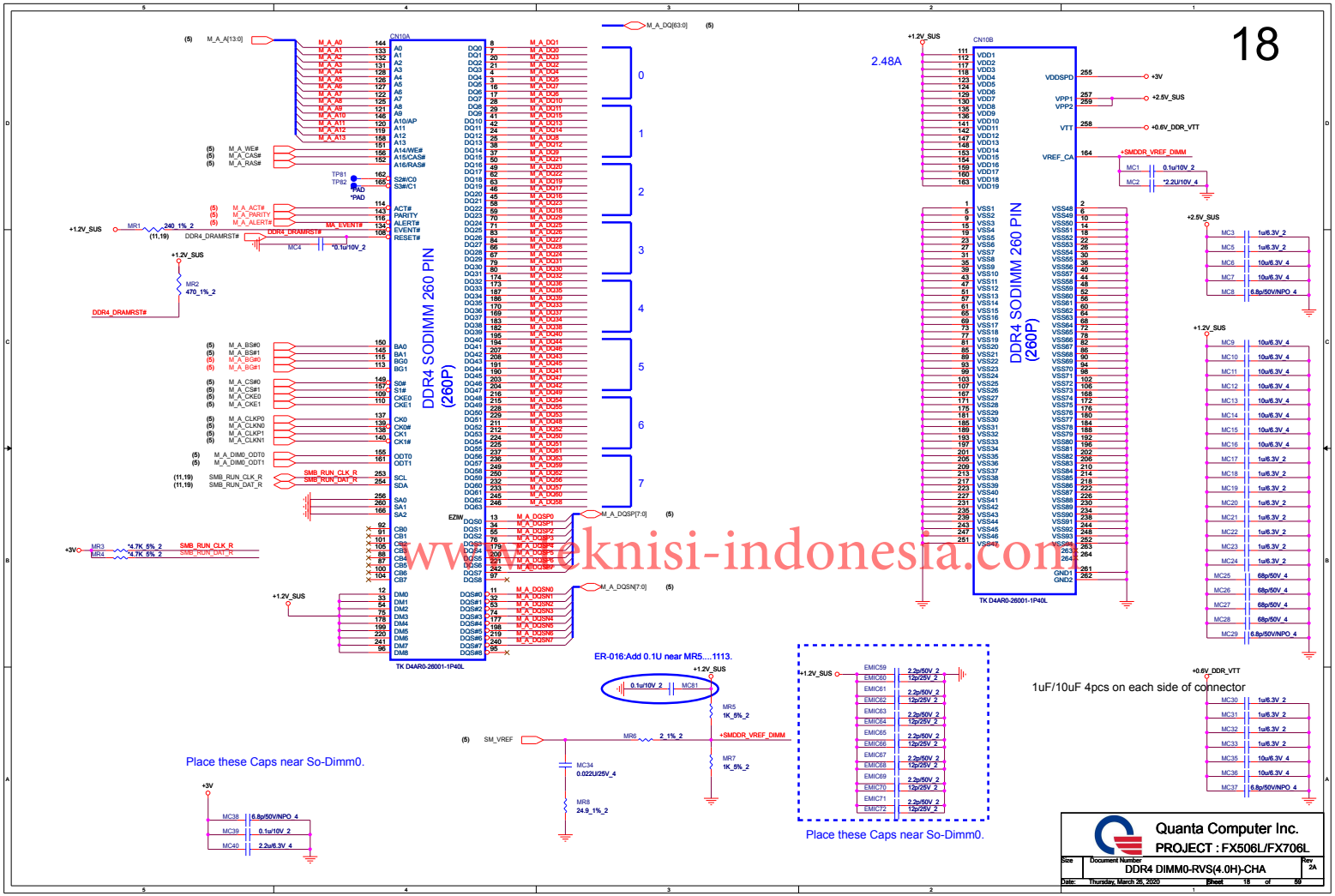

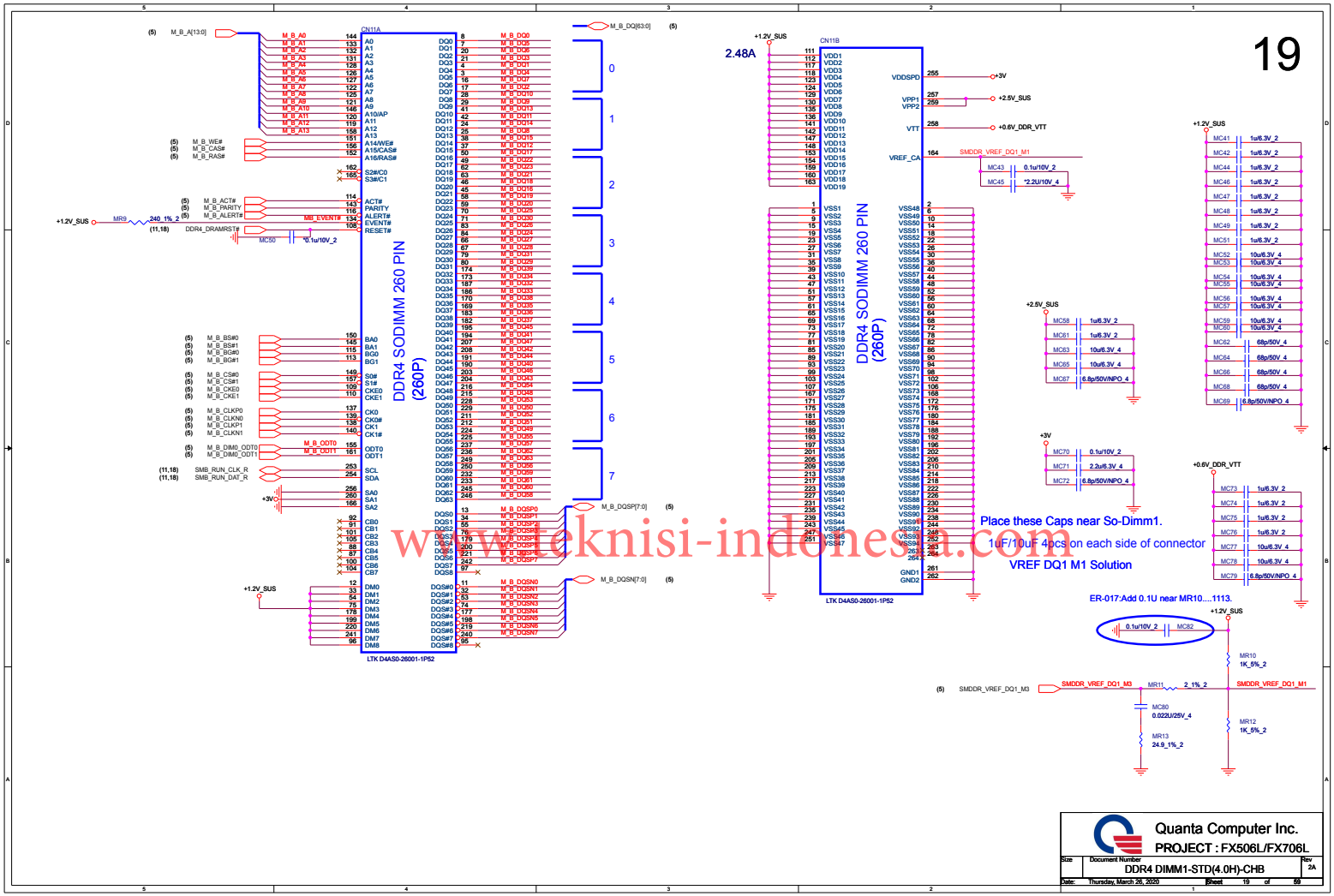

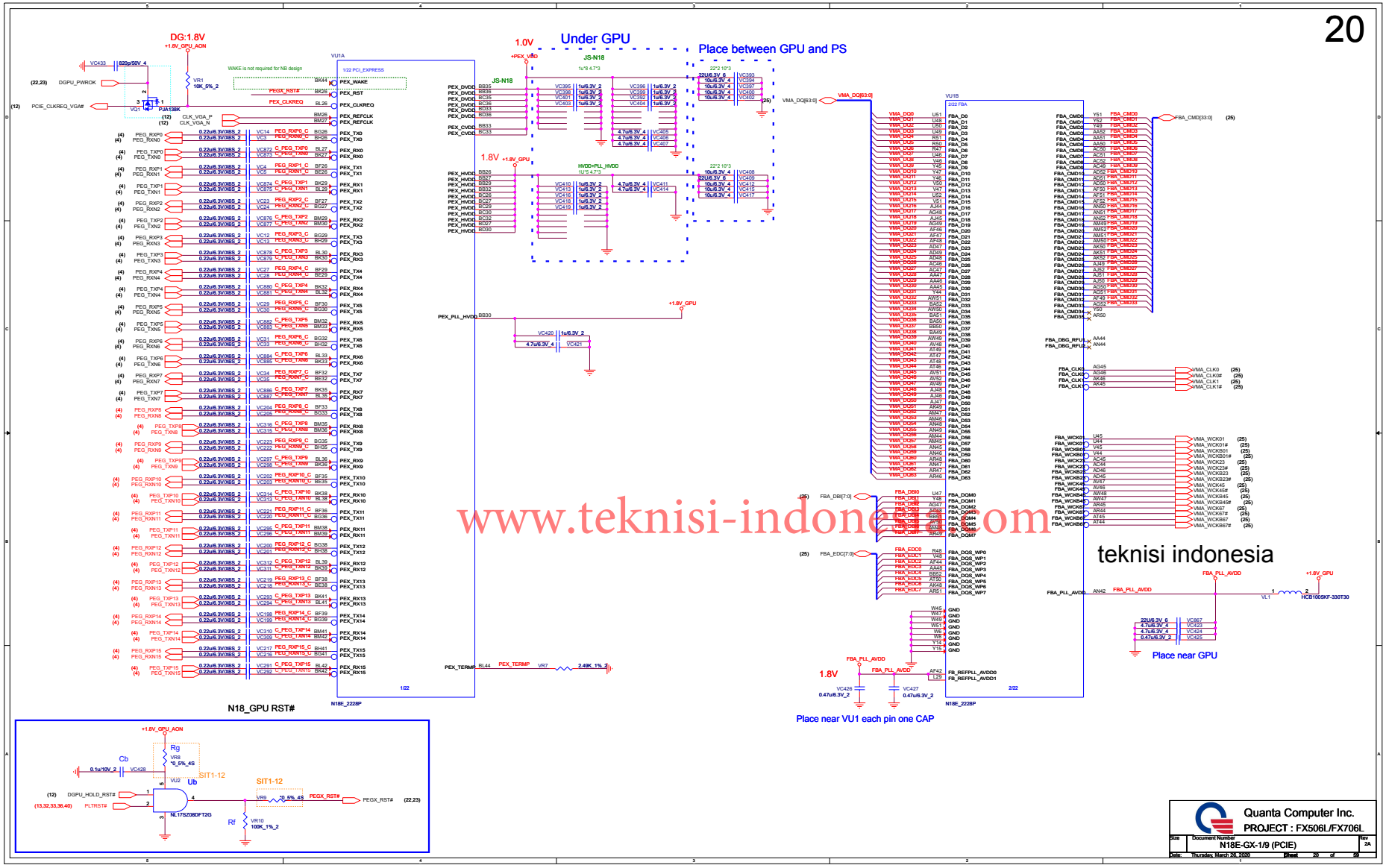
DG:1.8V
+1.8V_GPU_AON
Under GPU
Place between GPU and PS
1.0V
+PEX_VDD
1.8V
+1.8V_GPU
JS-N18
HVDD+PLL_HVDD
VMA_DQ[63:0]
VU1A
VU1B
1/22 PCI_EXPRESS
2/22 FBA
1/22
2/22
N18E_2228P
N18_GPU RST#
Place near VU1 each pin one CAP
Place near GPU
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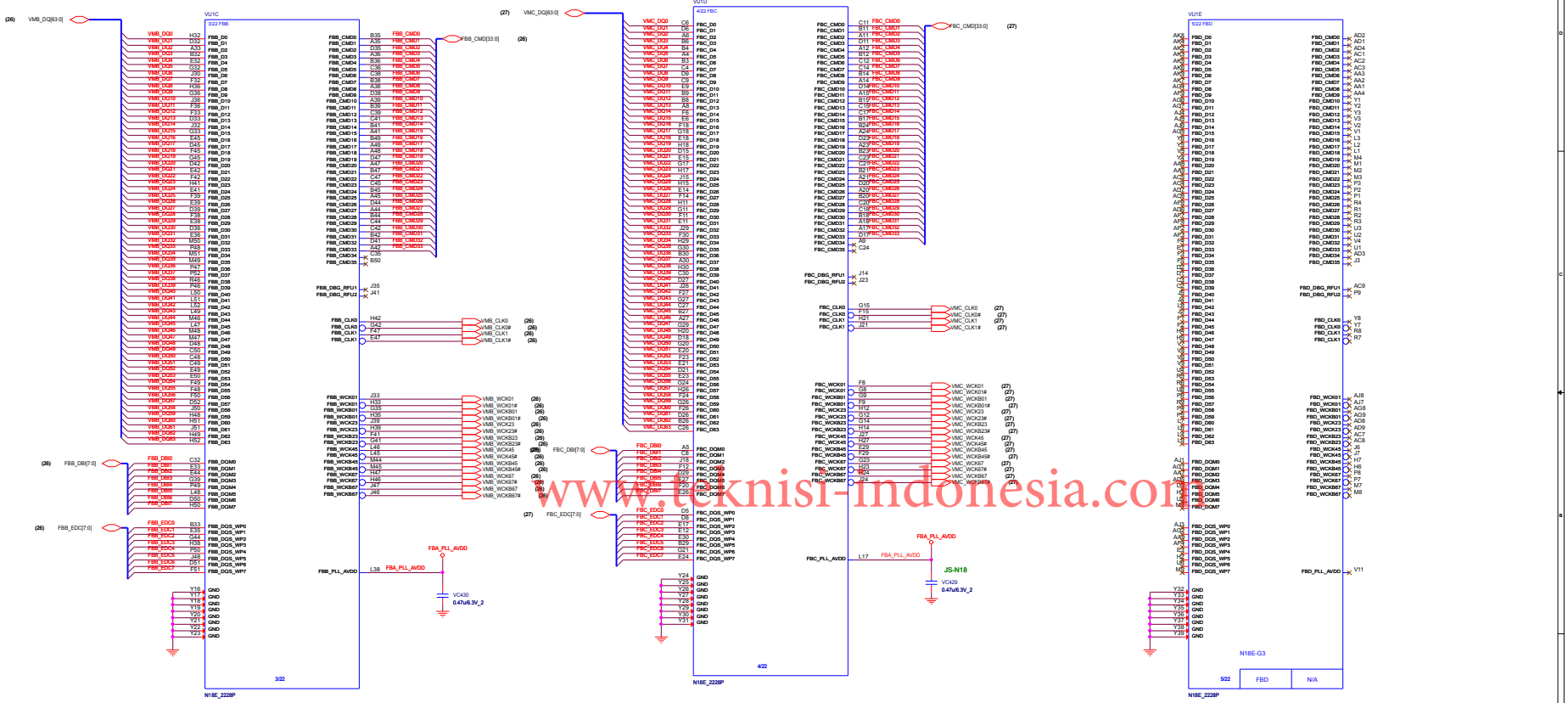
PROJECT : FX506L/FX706L
N18E-GX-1/9 (PCIE)
Thursday, March 26, 2020



Quanta Computer Inc.
PROJECT : FX506L/FX706L

Size	Document Number	Rev
	N18E-GX-2/9 (Memory)	3A
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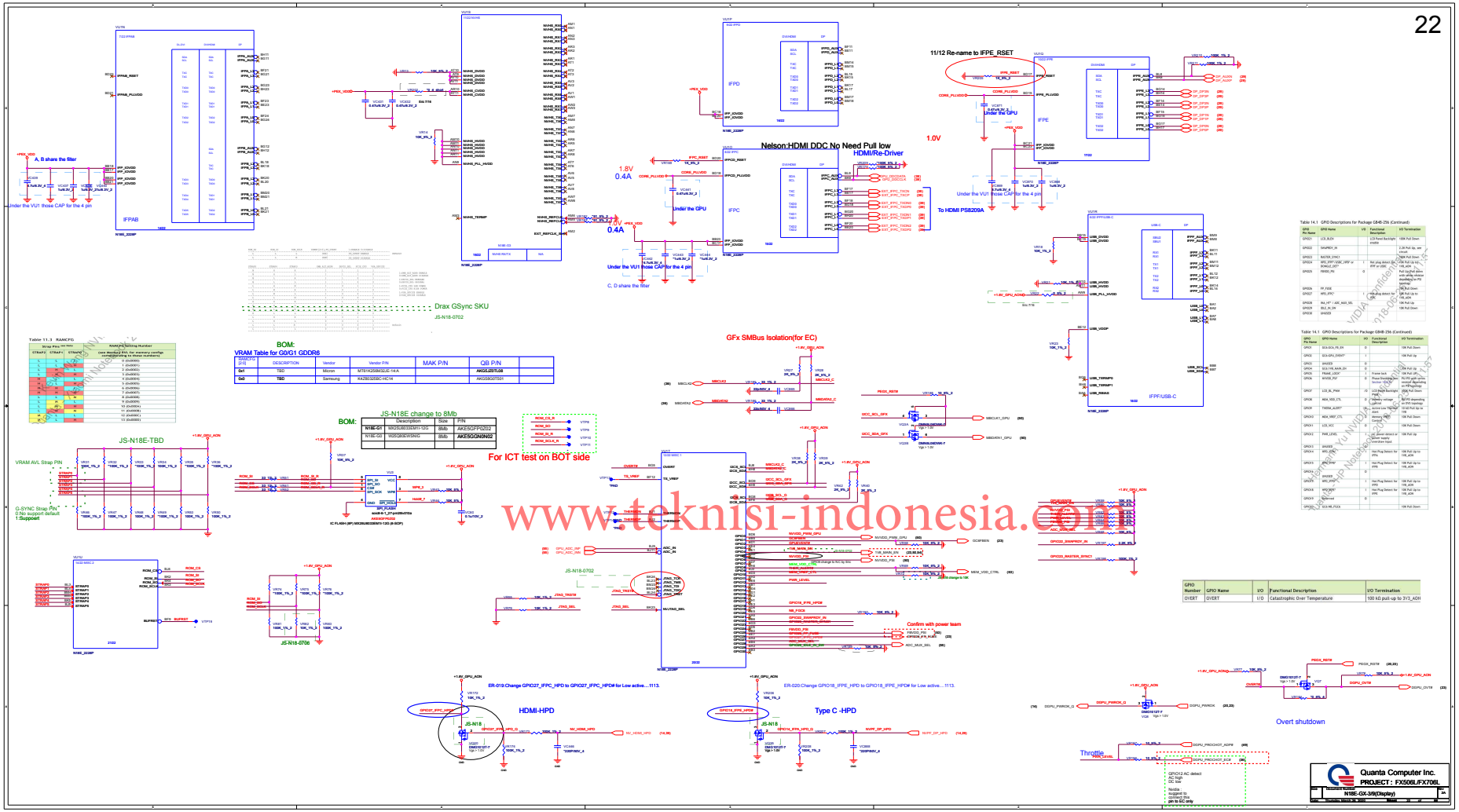
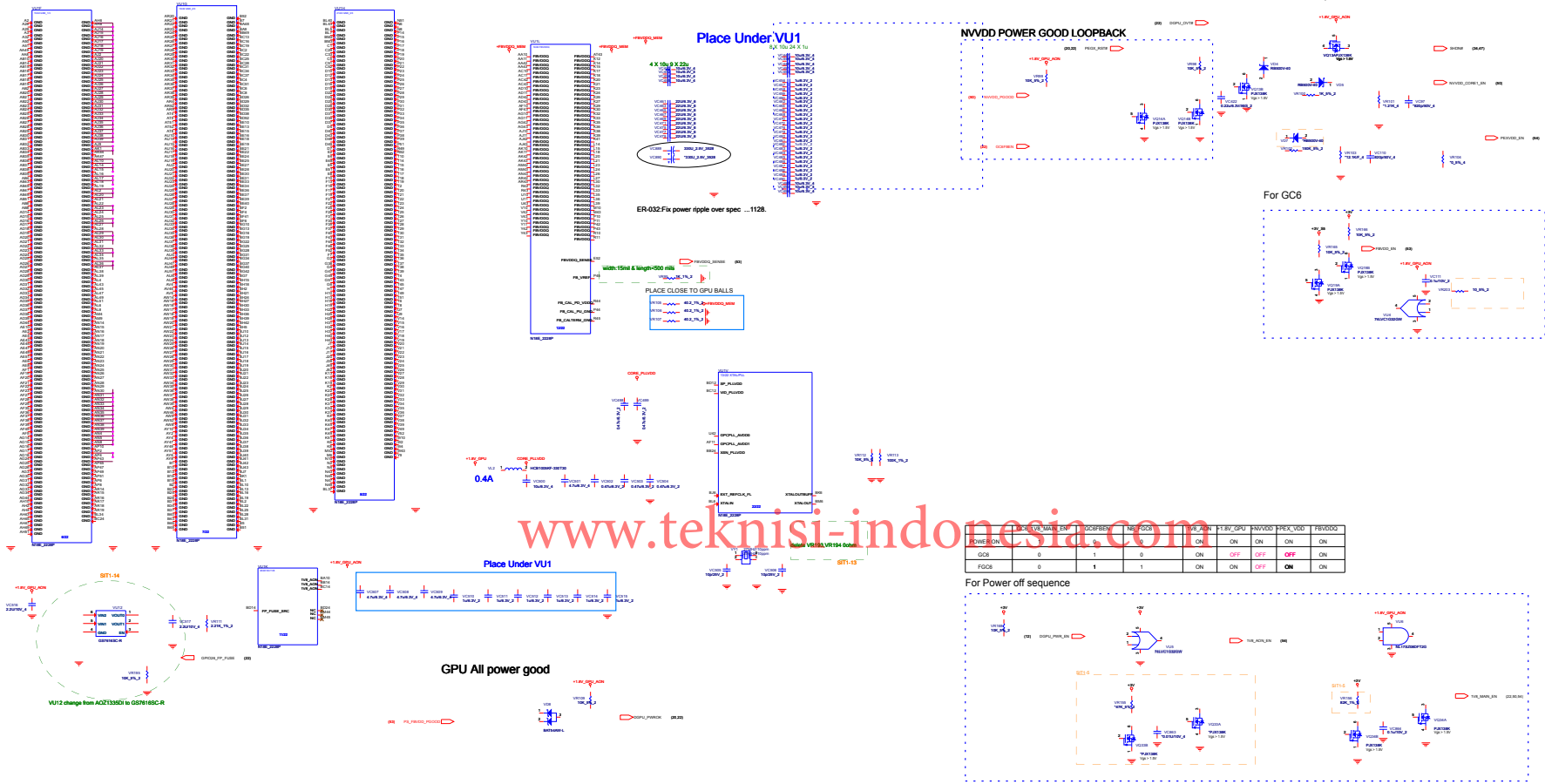


Overt temp ckt for NVVDD



	MOS_VR_MAIN_EN	GCSFBEN	NS_FGC6	VR_AON	+1.8V_GPU	+NVVDD	+PEX_VDD	FBVDDQ
POWER ON				ON	ON	ON	ON	ON
GC6	0	1	0	ON	OFF	OFF	OFF	ON
FGC6	0	1	1	ON	ON	OFF	ON	ON

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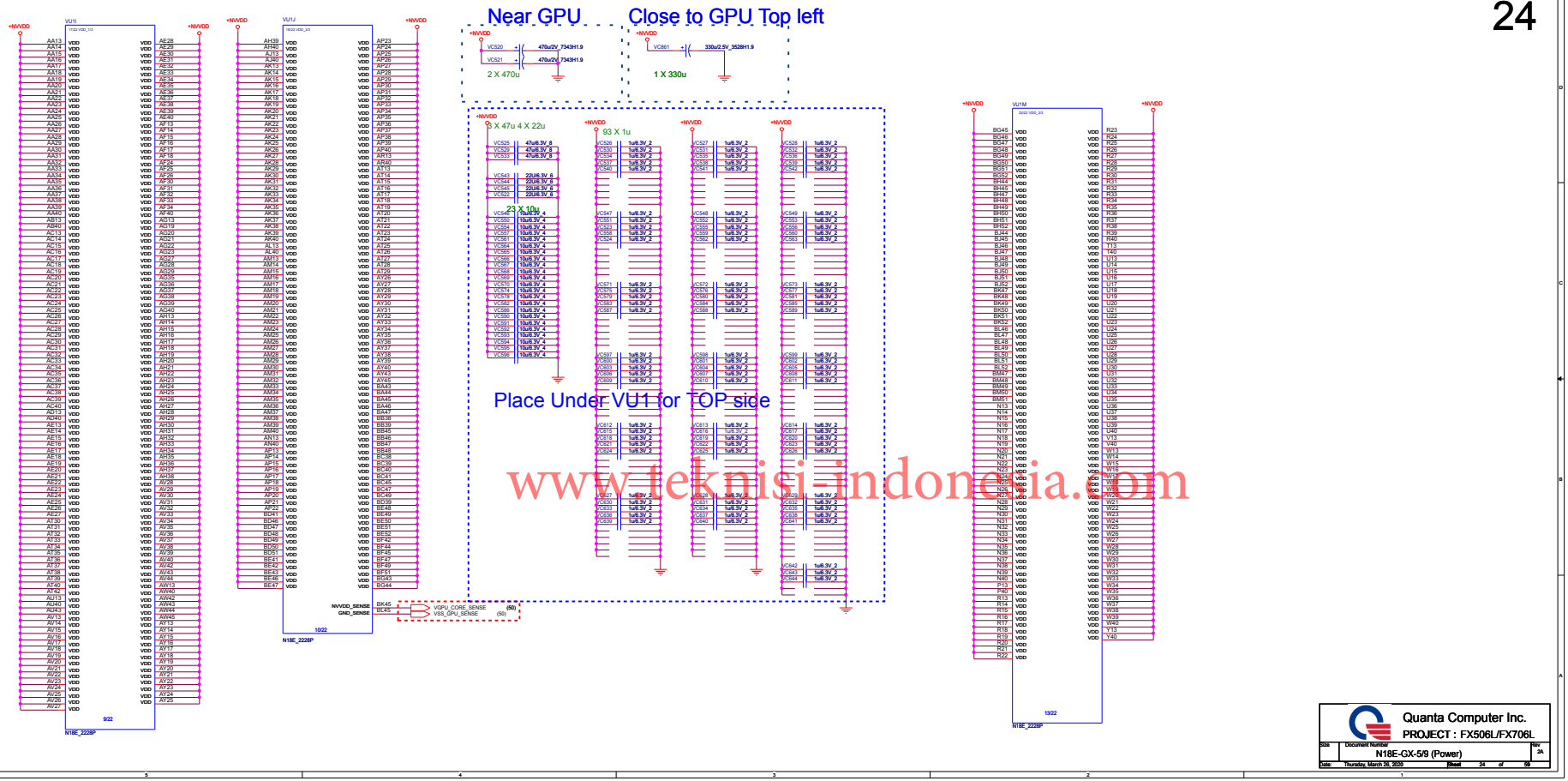
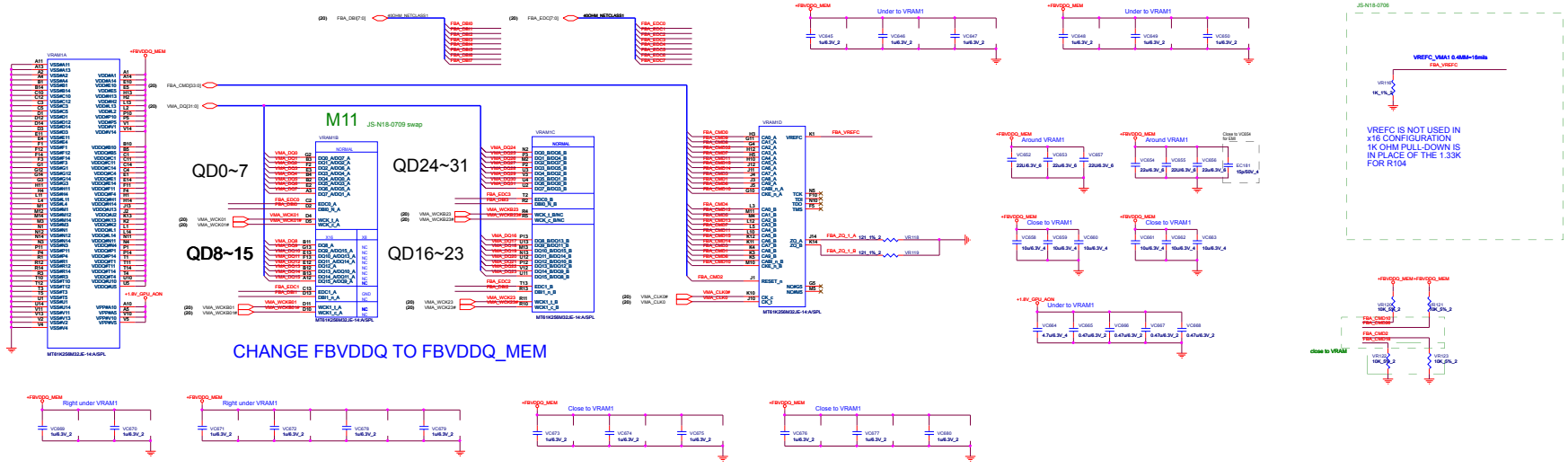
Quanta Computer Inc.
PROJECT : FX508L/FX706L
N18E-GX -4/9 (MISC)

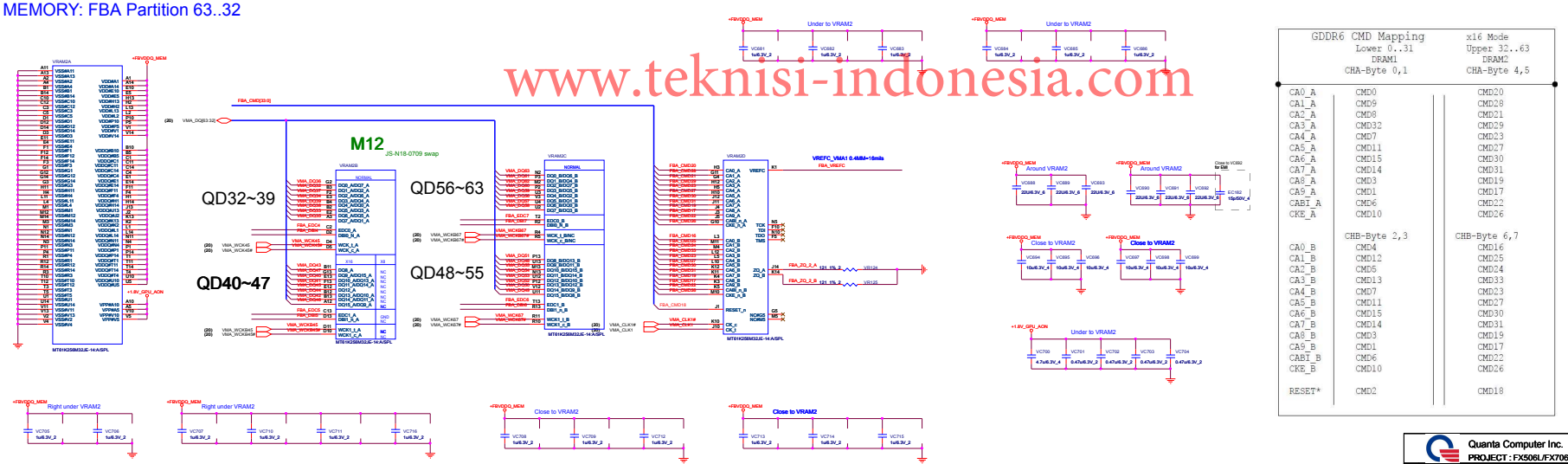


Quanta Computer Inc.
PROJECT : FX506L/FX706L
Size: Document Number: N18E-GX-5/9 (Power) Rev: 2A
Date: Thursday, March 26, 2020 Sheet 24 of 59

MEMORY: FBA Partition 31..0



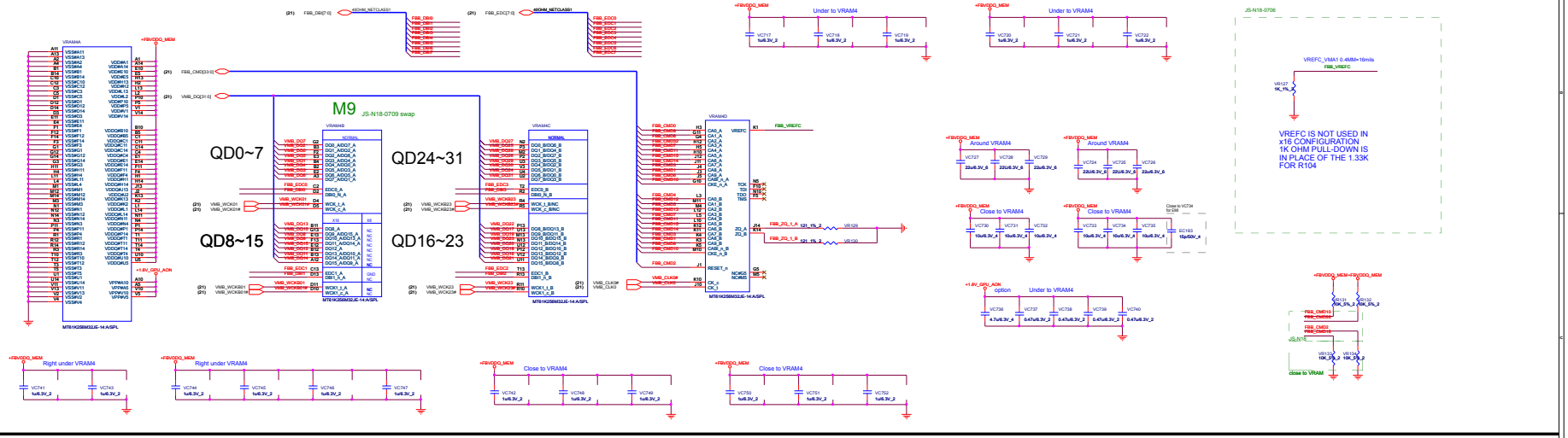
MEMORY: FBA Partition 63..32



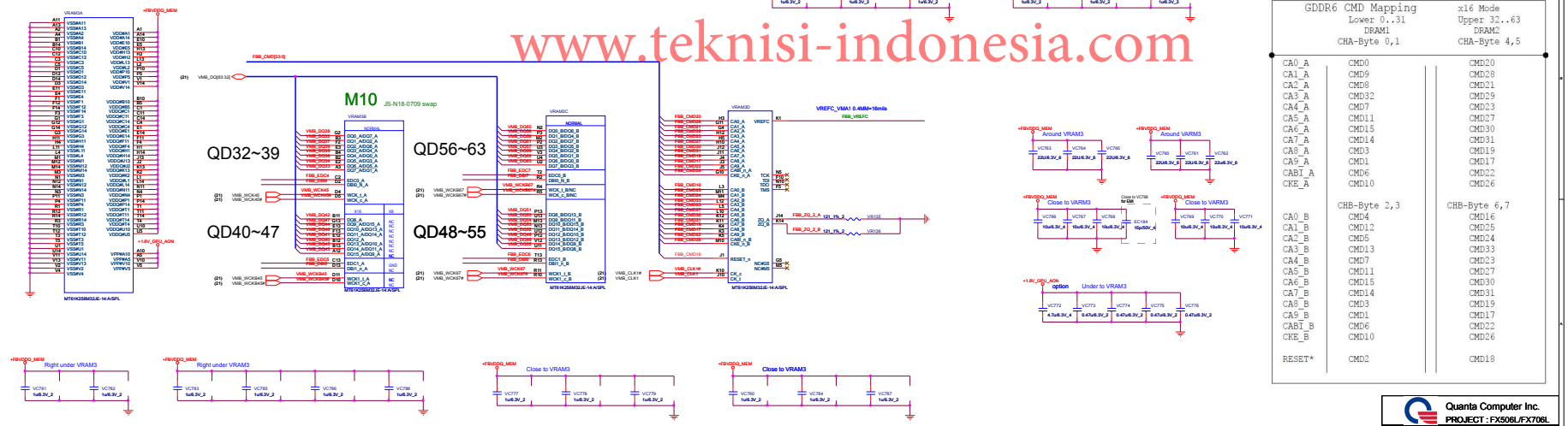
GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

Quanta Computer Inc.
PROJECT : FX506L/FX706L
Document Number: N18E-GX-6/9(GDDR5)
Rev: 2A
Date: Thursday, March 26, 2020 Sheet 25 of 30

MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

Quanta Computer Inc.
PROJECT : FX506L/FX706L
Document Number: N18E-GX-6/9(GDDR5)
Rev: 2A
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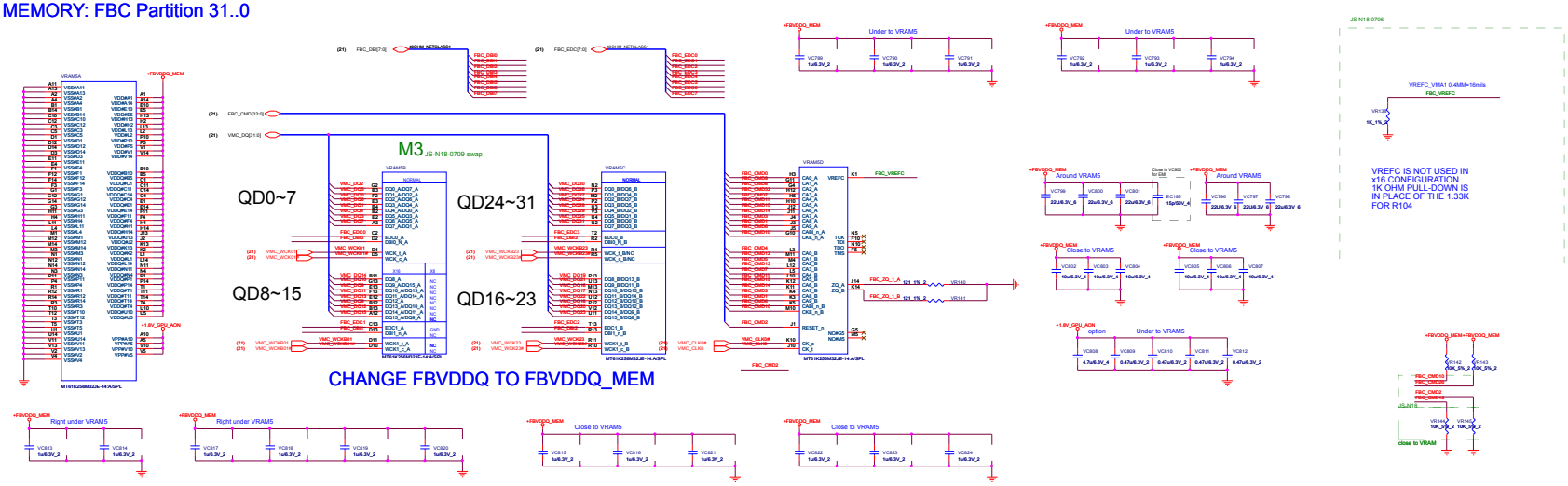
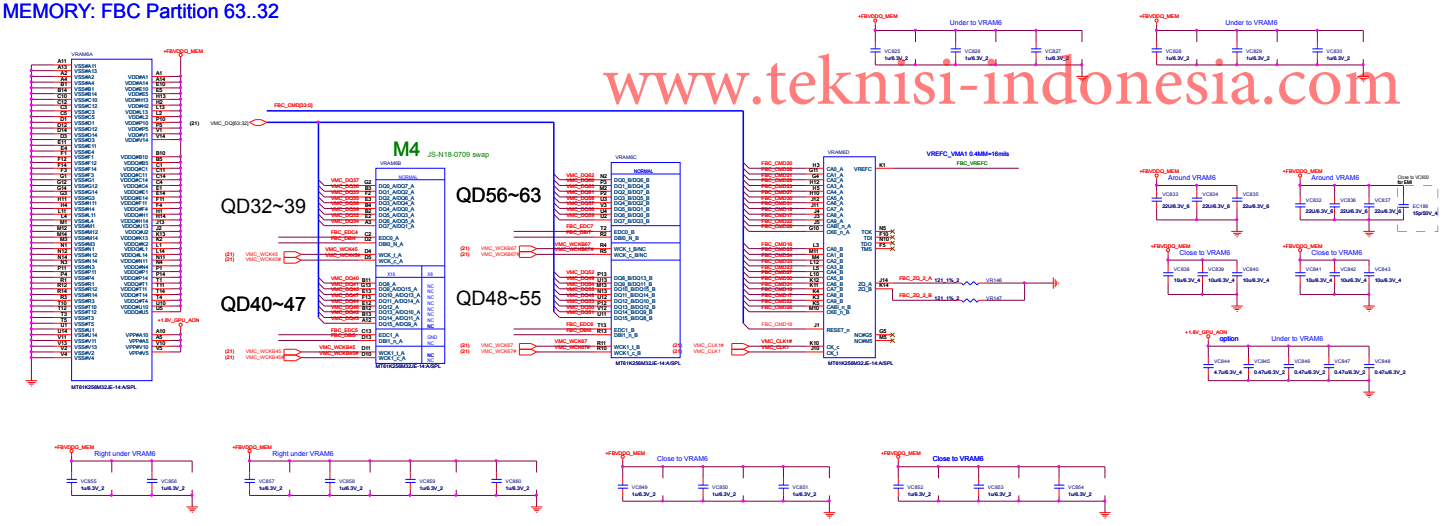
MEMORY: FBC Partition 31..0

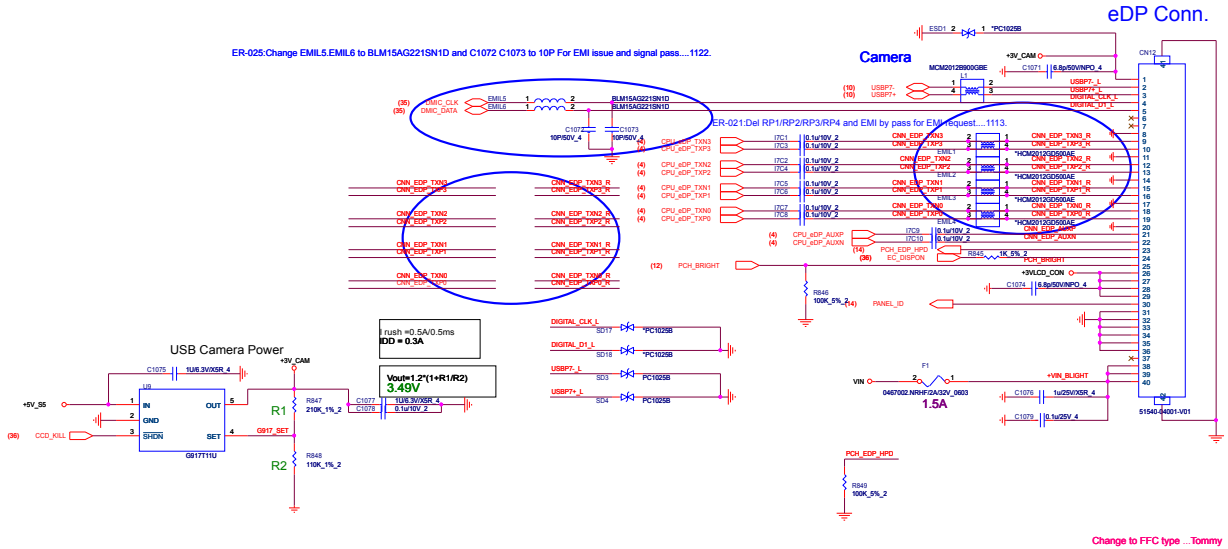


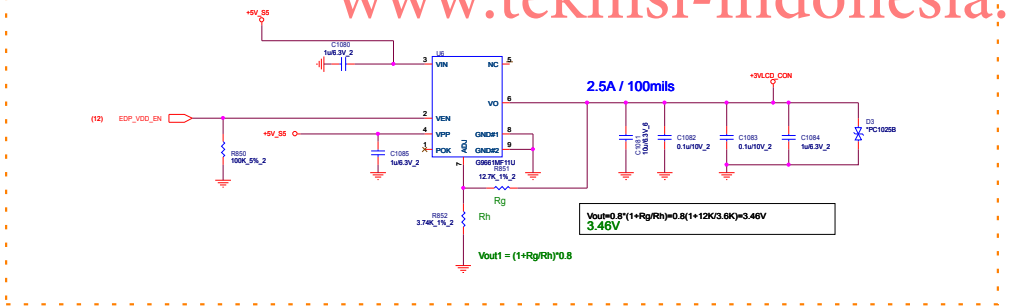
MEMORY: FBC Partition 63..32



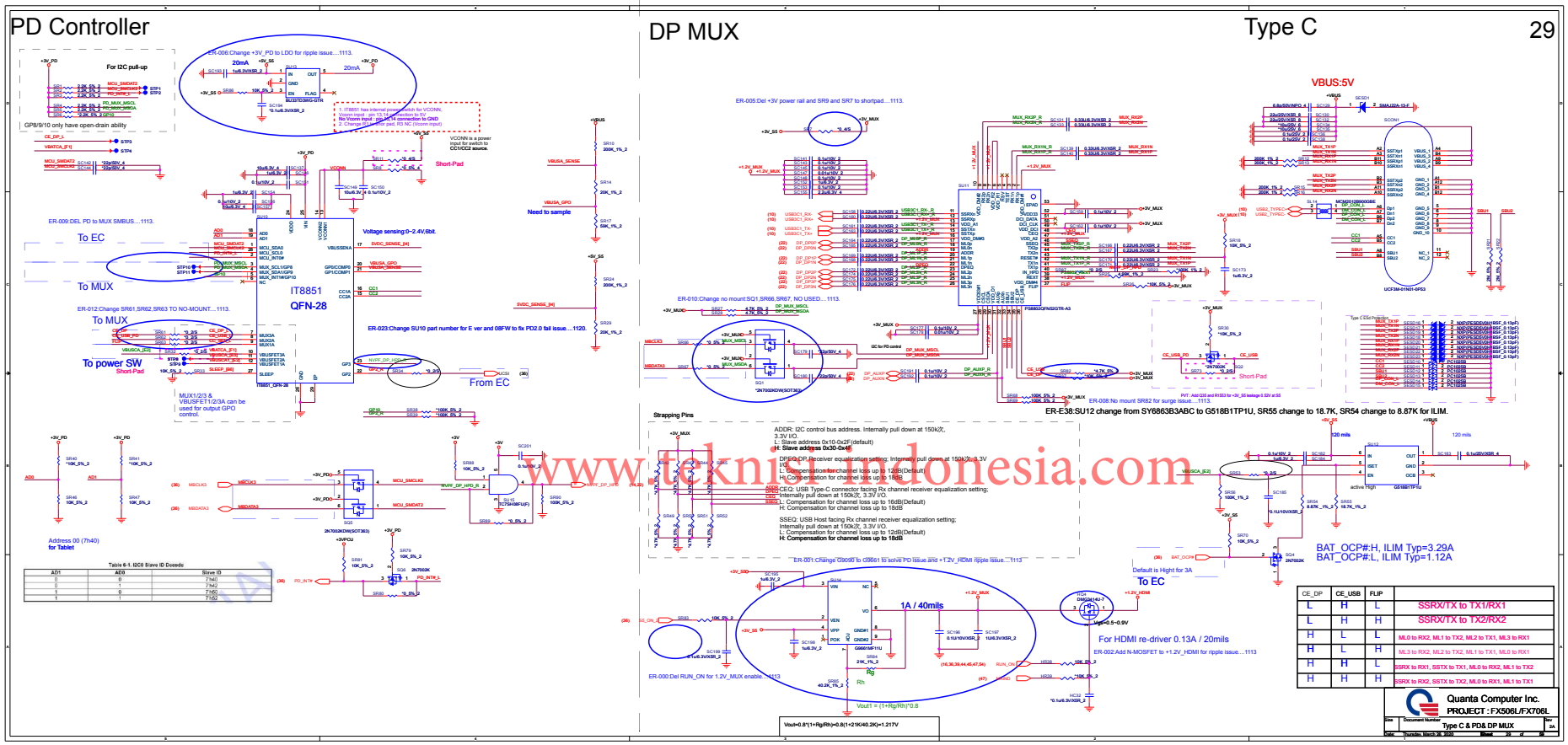
GDDR6 CMD Mapping	x16 Mode
Lower 0..31	Upper 32..63
DRAM1	DRAM2
CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABI_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABI_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

Quanta Computer Inc.
PROJECT : FX506L/FX706L
Document Number: N18E-GX-69(GDDR5)
Rev: 2A
Date: Thursday, March 26, 2020 Sheet 27 of 69



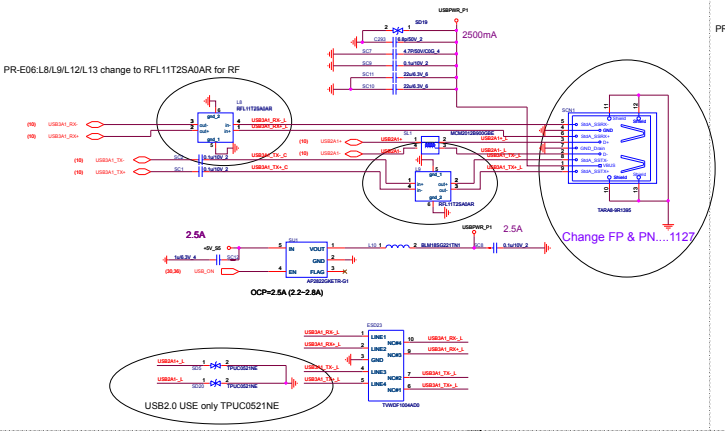


Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
Size	Document Number: eDP CONN/CAM/D-MIC	Rev: 2A
Date: Thursday, March 26, 2020	Sheet 28 of 59	



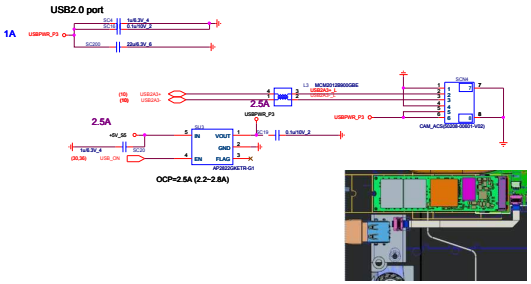
CE_DP	CE_USB	FLIP	
L	H	L	SSRX/TX to TX1/RX1
L	H	H	SSRX/TX to TX2/RX2
H	L	L	ML0 to RX2, ML1 to TX2, ML2 to TX1, ML3 to RX1
H	L	H	ML3 to RX2, ML2 to TX2, ML1 to TX1, ML0 to RX1
H	H	L	SSRX to RX1, SSTX to TX1, ML0 to RX2, ML1 to TX2
H	H	H	SSRX to RX2, SSTX to TX2, ML0 to RX1, ML1 to TX1

USB 3.2 GEN1 Type A/ PORT1

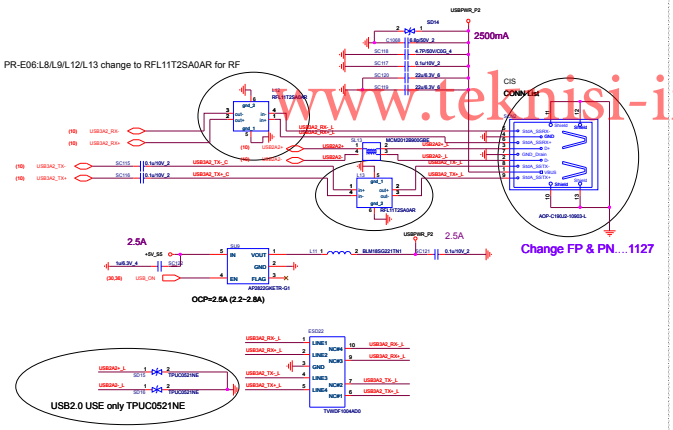


USB 2.0 PORT1

PR-E02:Remove CON6 for USB board FFC CONN.....0217

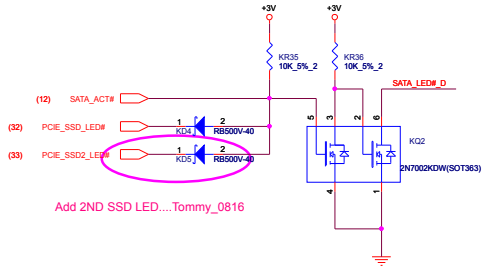


USB 3.2 GEN1 Type A/PORT2

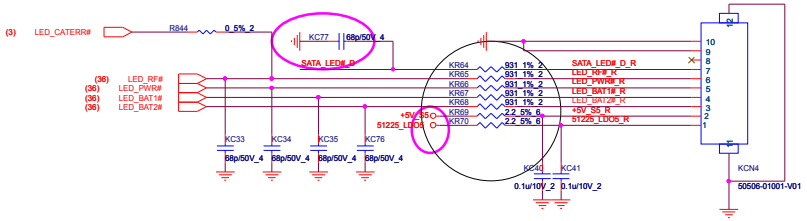


Quanta Computer Inc.
PROJECT : FX506L/FX706L
USB3.0/USB2.0

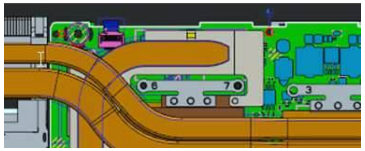
LED



Add 68P for EMI....Tommy_0912

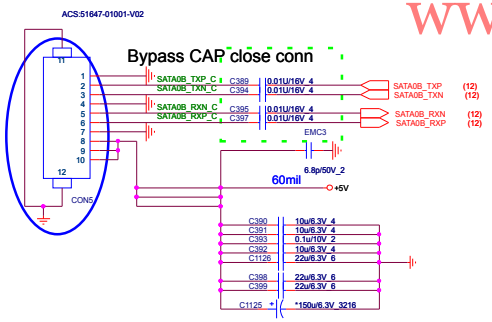


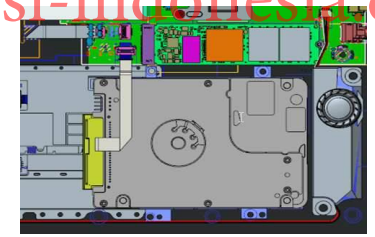
ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brigtness



SATA HDD FFC

ER-032:Change HDD FFC pin define for ME cable routing....1126





Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
Size	Document Number: HDD/LED	Rev: 2A
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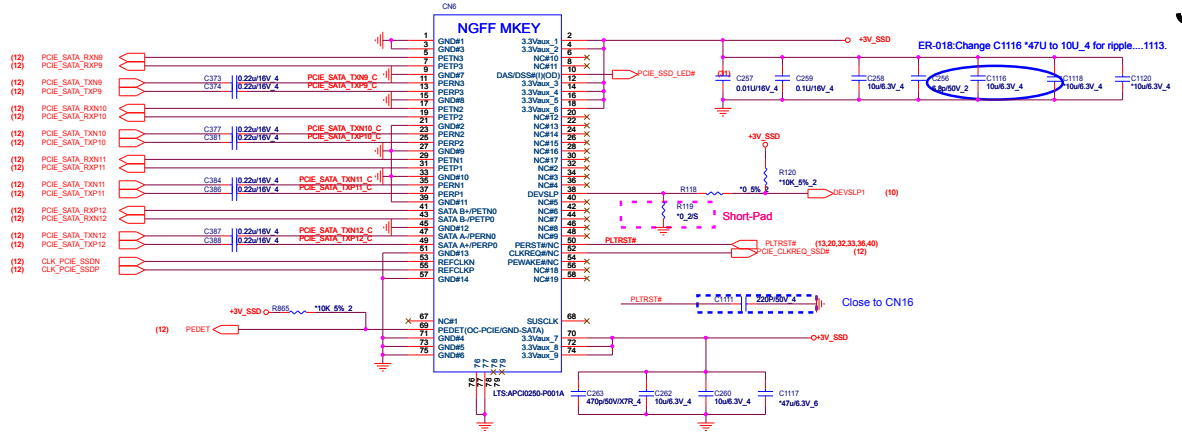
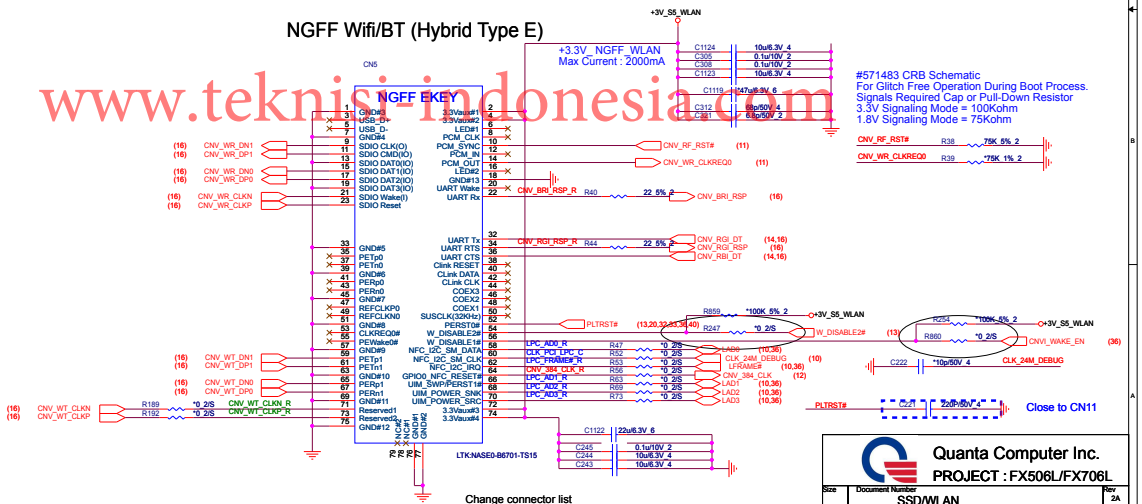
Main SSD



Change connector list

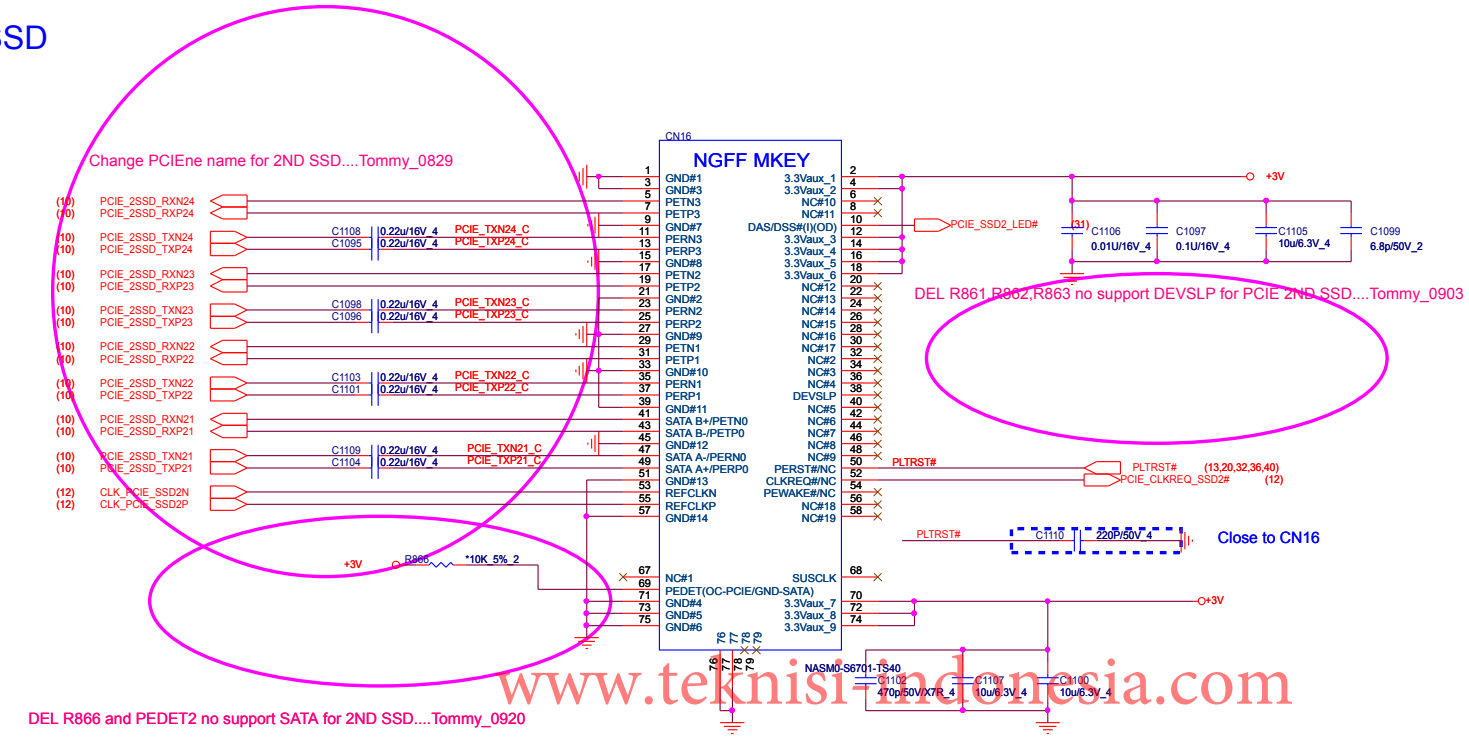
WLAN/BT



Change connector list

Quanta Computer Inc.
PROJECT : FX506L/FX706L
SSD/WLAN
Rev 2A
Date: Thursday, March 26, 2020 Sheet 32 of 59

2ND SSD

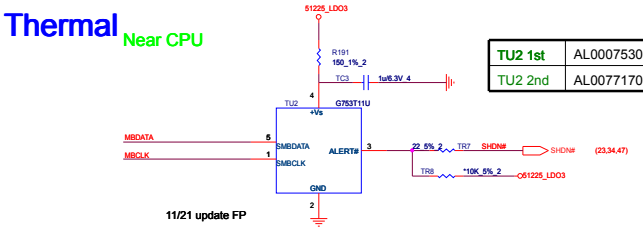


Quanta Computer Inc.		
PROJECT : FX506L/FX706L		
Size	Document Number: 2ND SSD	Rev: 2A
Date: Thursday, March 26, 2020	Sheet 33 of 59	

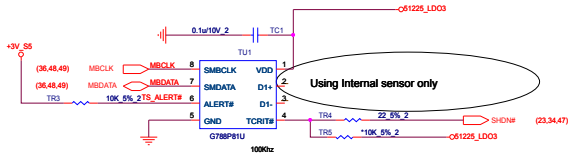
Thermal

Near CPU

TU2 1st	AL000753000
TU2 2nd	AL007717000

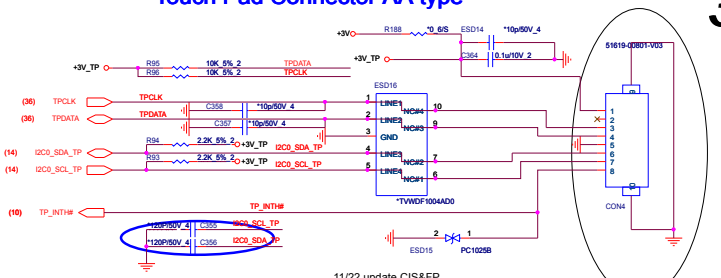


11/21 update FP



Near GPU

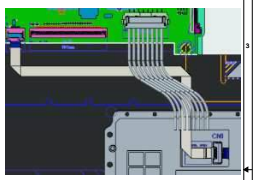
Touch Pad Connector AA type



11/22 update CIS&FP

ER-029: Change C355,C356 to no-mount for fix TP timing issue ...1122.

Change connector list

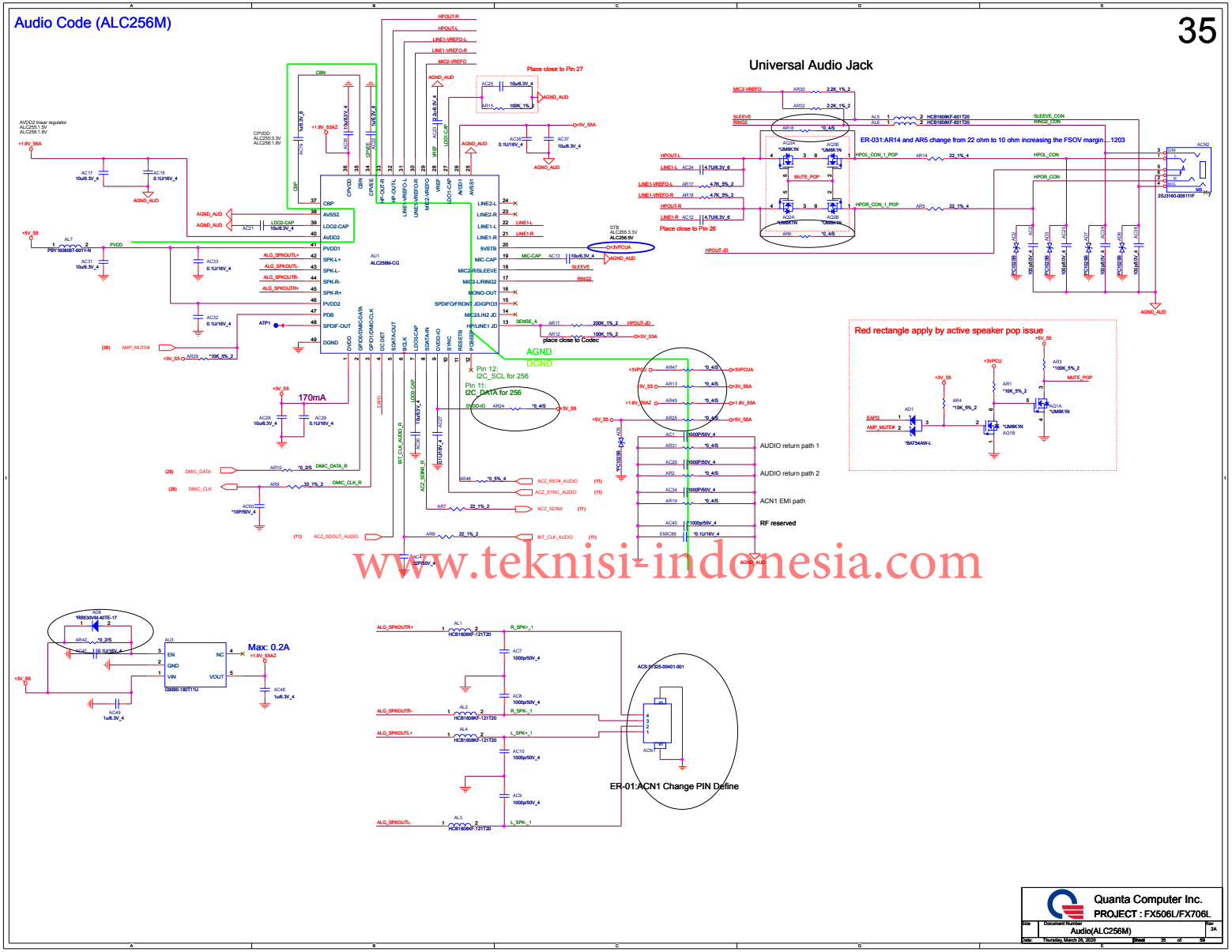


Quanta Computer Inc.
PROJECT : FX506L/FX706L

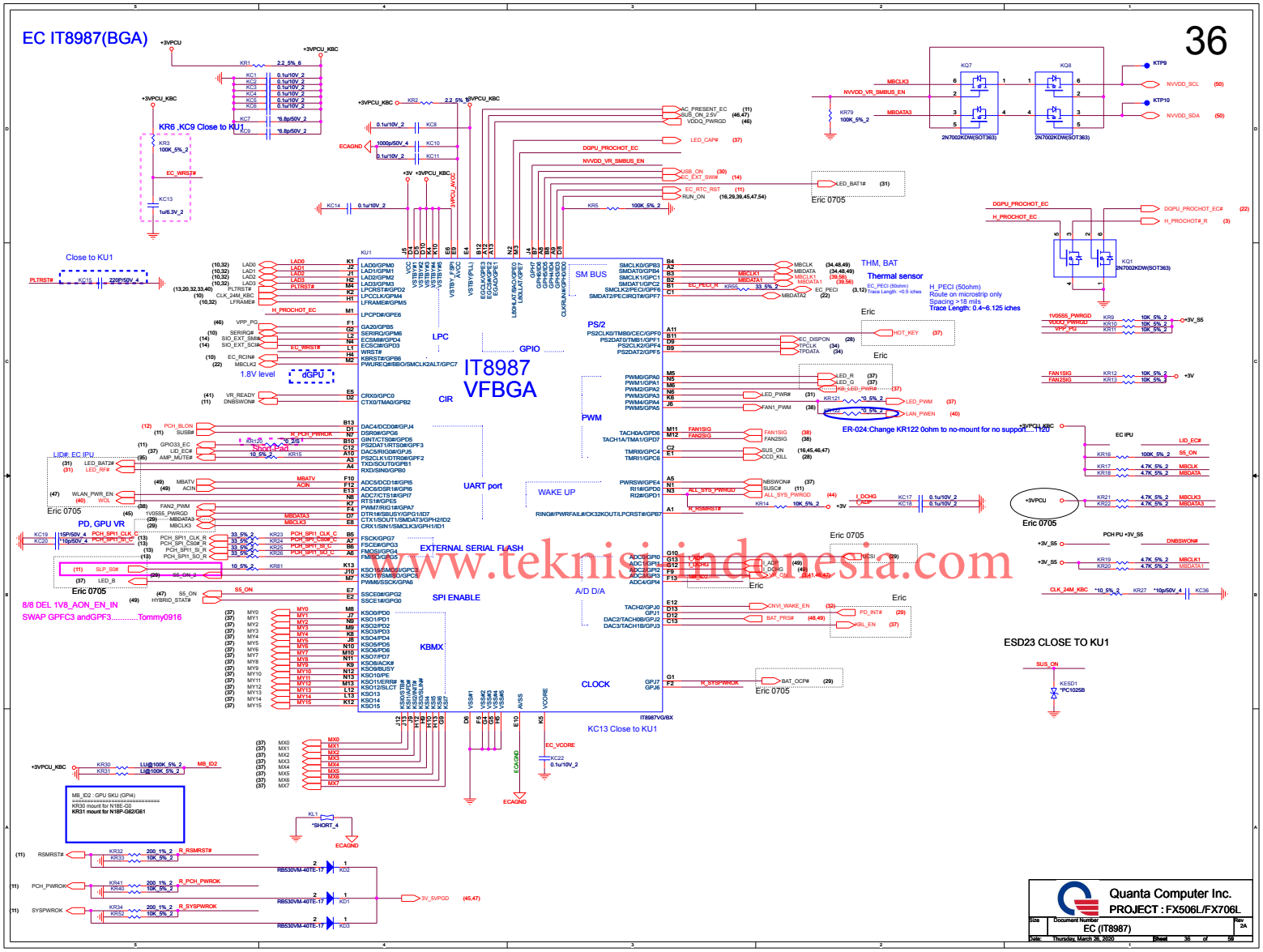
Size	Document Number	Rev
	TP/Thermal	2A

Date: Thursday, March 26, 2020 Sheet 34 of 59

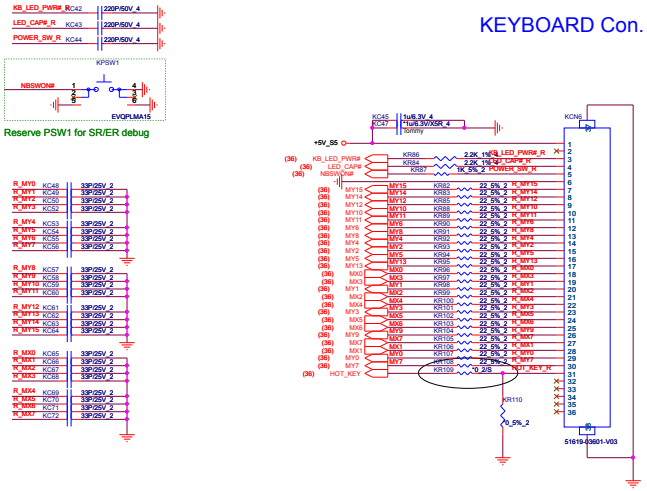
Audio Code (ALC256M)



Quanta Computer Inc.
PROJECT : FX506L/FX706L
Audio(ALC256M)
Thursday, March 28, 2019



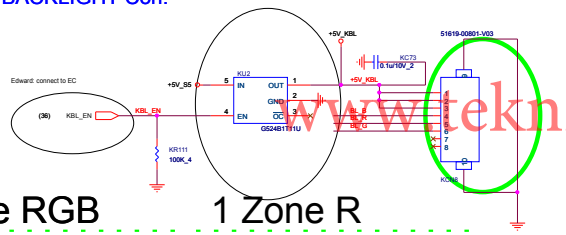
KEYBOARD Con.



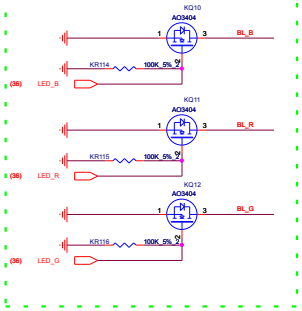
Reserve PSW1 for SR/ER debug

KEYBOARD BACKLIGHT Con.

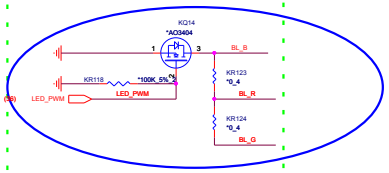
8/7 Change to footprint.



1 Zone RGB

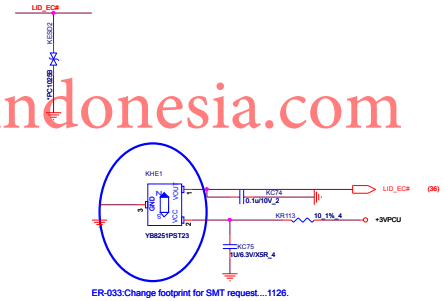


1 Zone R



ER-031:Del KQ15/KQ13 for no support Red backlight....1125.

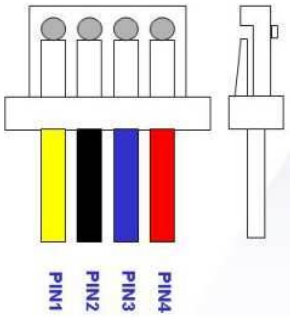
ESD23 CLOSE TO KHE1



ER-033:Change footprint for SMT request....1126.

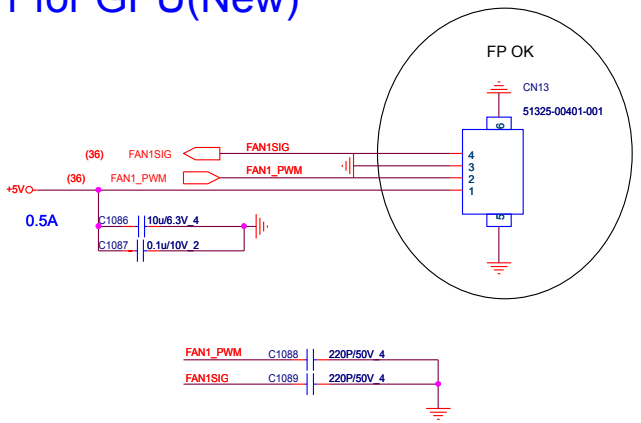
Quanta Computer Inc.
PROJECT : FX506L/FX706L
DB/KB/LID
Thursday, March 26, 2020

4Pins Fan Connector Pins Definition

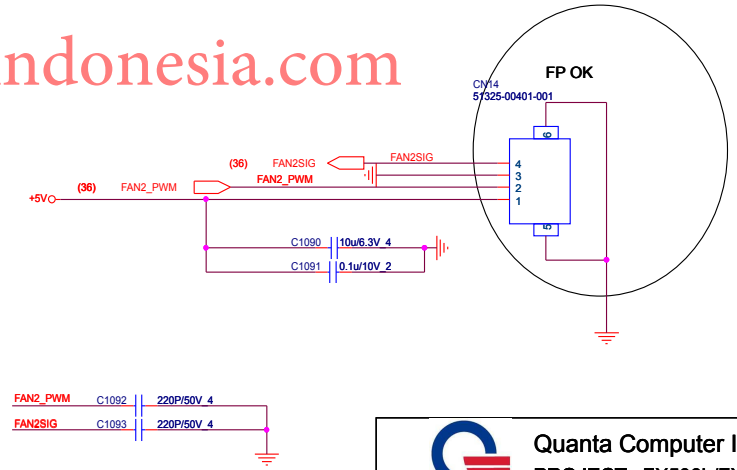


Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

FAN1 for GPU(New)



FAN2 for CPU



Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	FAN	2A

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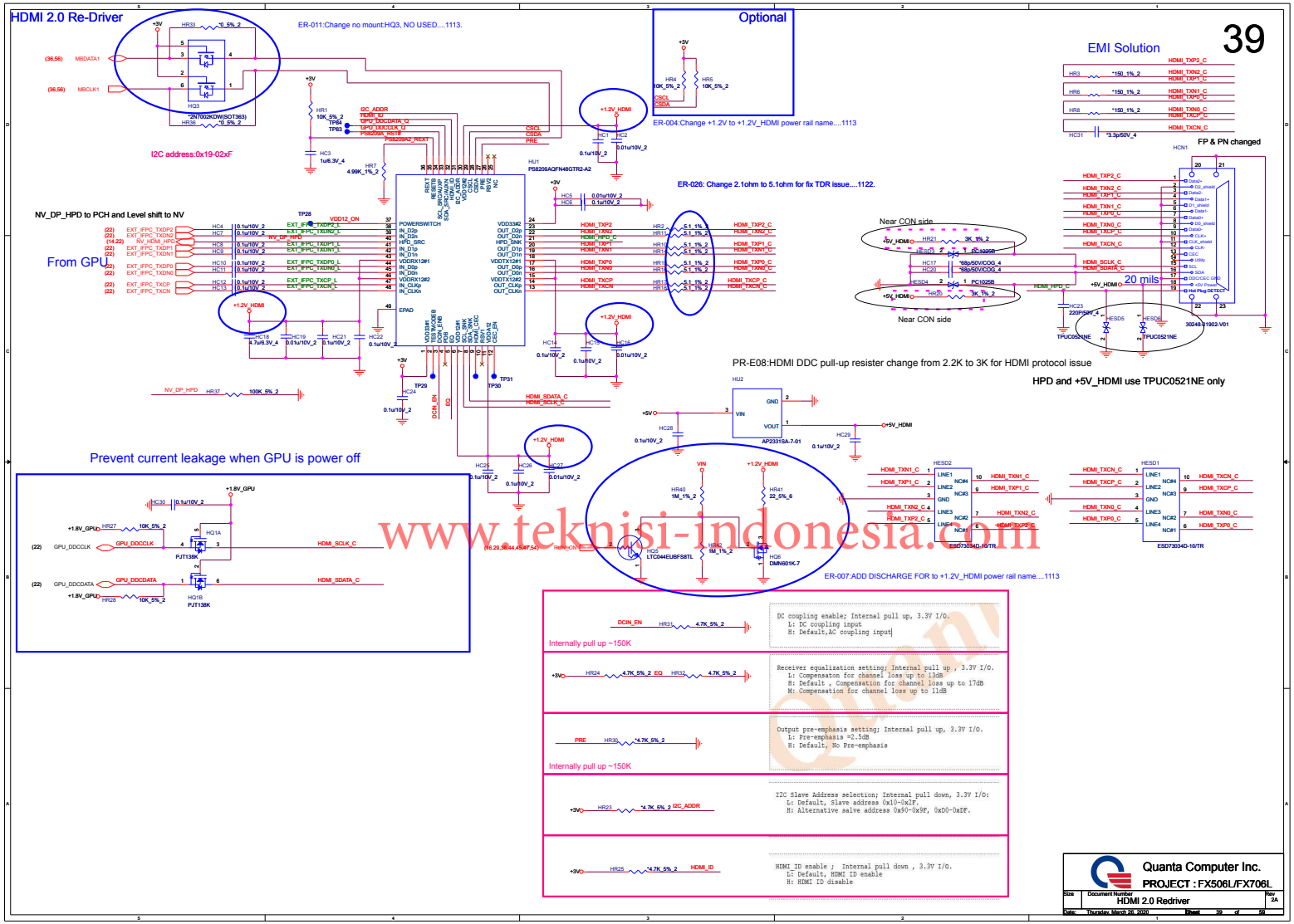
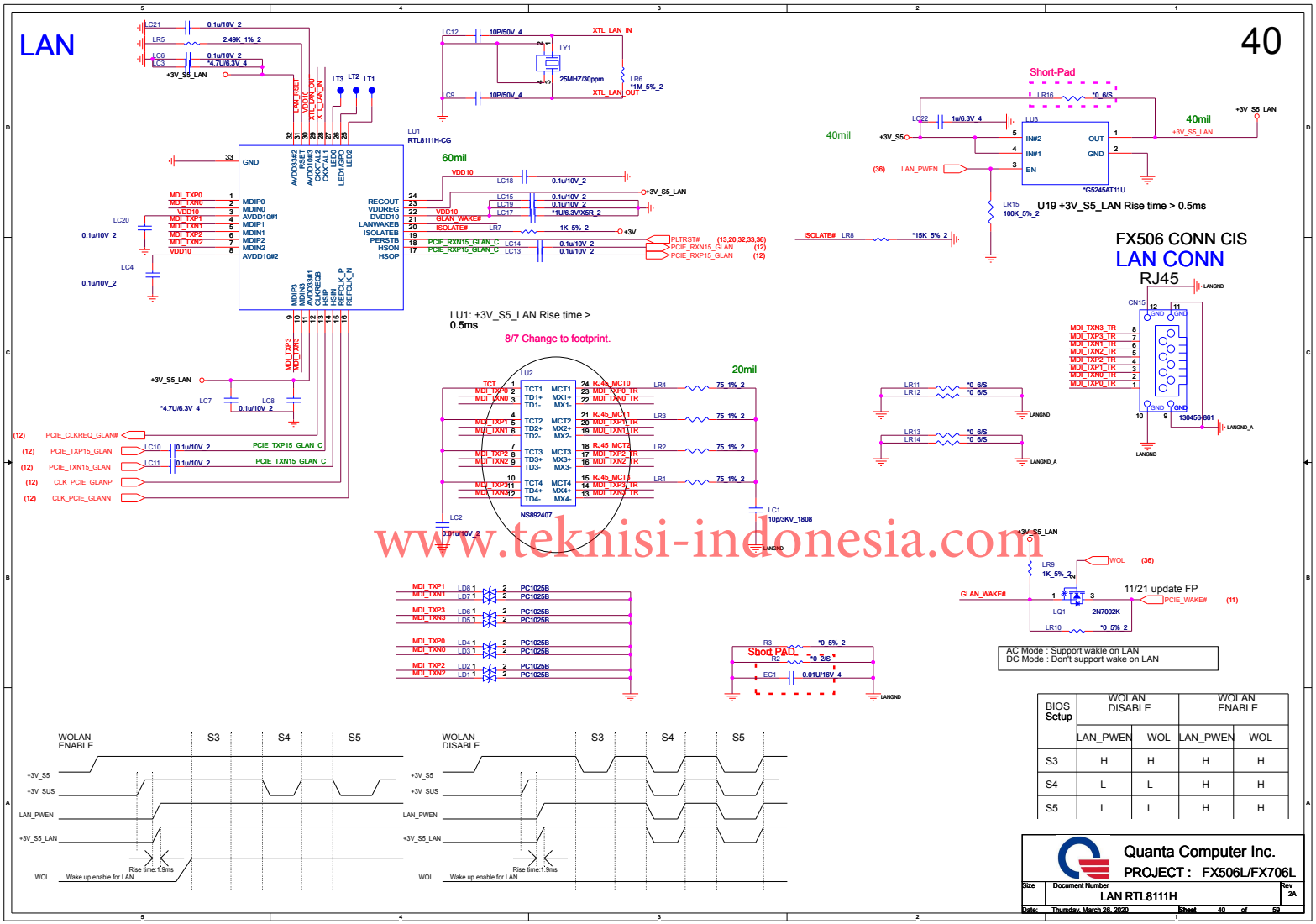


LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	LAN RTL8111H	2A
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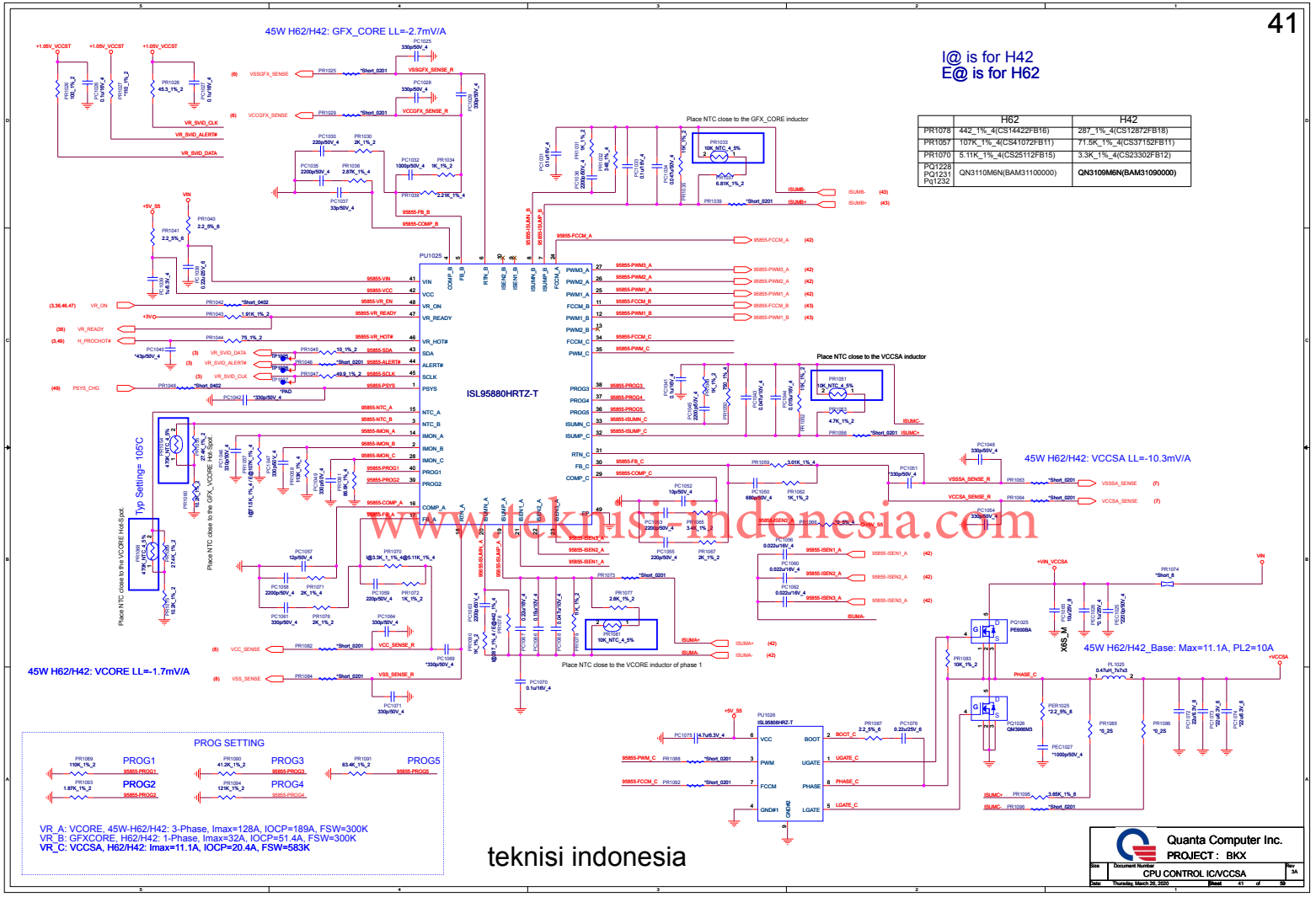
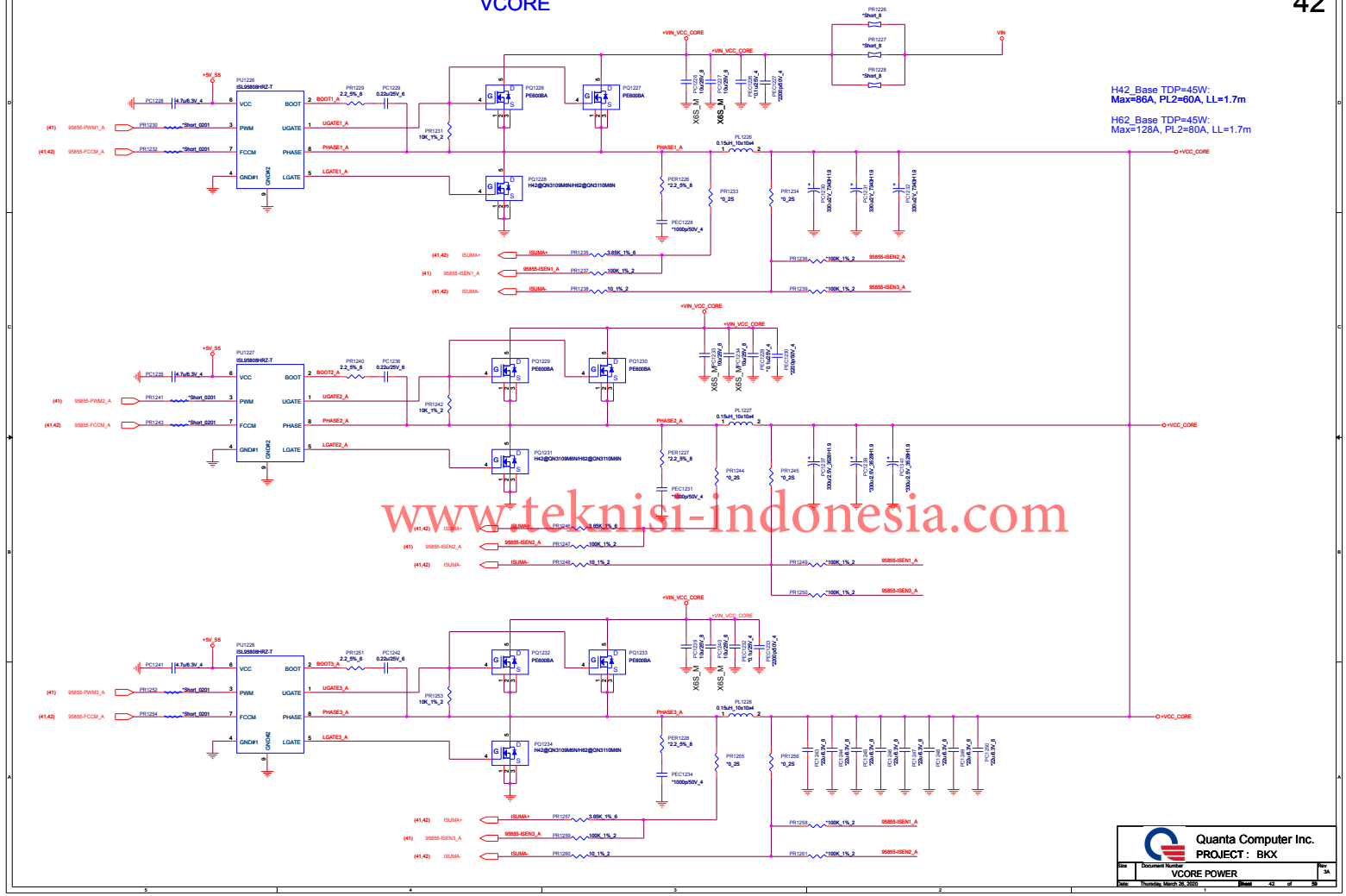
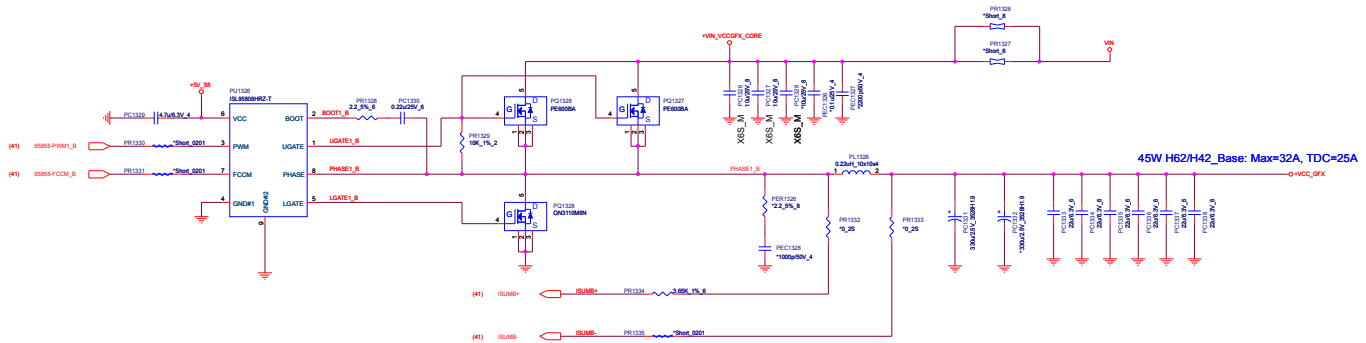


	H62	H42
PR1078	442_1%_4(CS14422FB18)	287_1%_4(CS12872FB18)
PR1057	107K_1%_4(CS41072FB11)	71.5K_1%_4(CS37152FB11)
PR1070	5.11K_1%_4(CS25112FB15)	3.3K_1%_4(CS23302FB12)
PQ1228 PQ1231 Pq1232	QN3110M6N(BAM31100000)	**QN3109M6N(BAM31090000)**

VCORE



GFX_CORE



Quanta Computer Inc.
PROJECT : BKX

Size	Document Number	Rev
	GFX CORE POWER	3A
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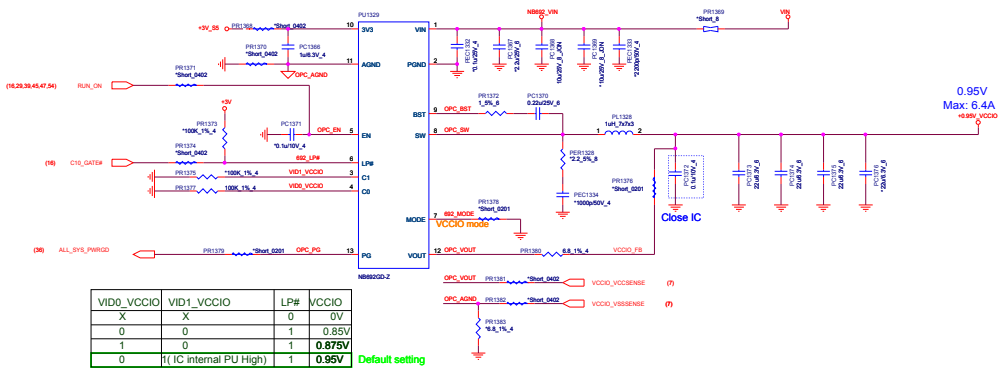
VCCIO



VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	**0.875V**
0	1(IC internal PU High)	1	**0.95V**

Quanta Computer Inc.
PROJECT : BKX
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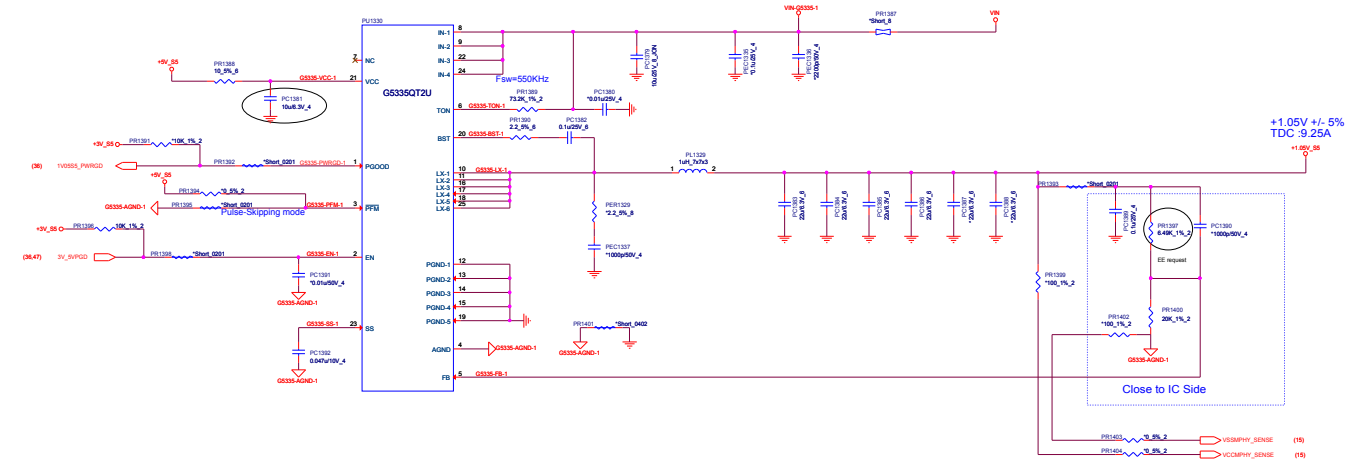
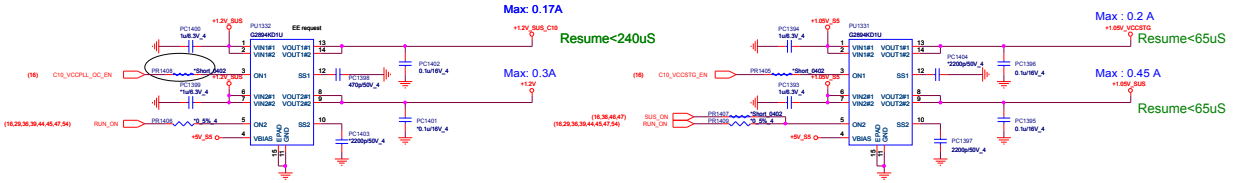
+1.05V_S5





Quanta Computer Inc.		
PROJECT : BKX		
Size	Document Number	Rev
	POWER 1.05V_S5(G5335)	2A
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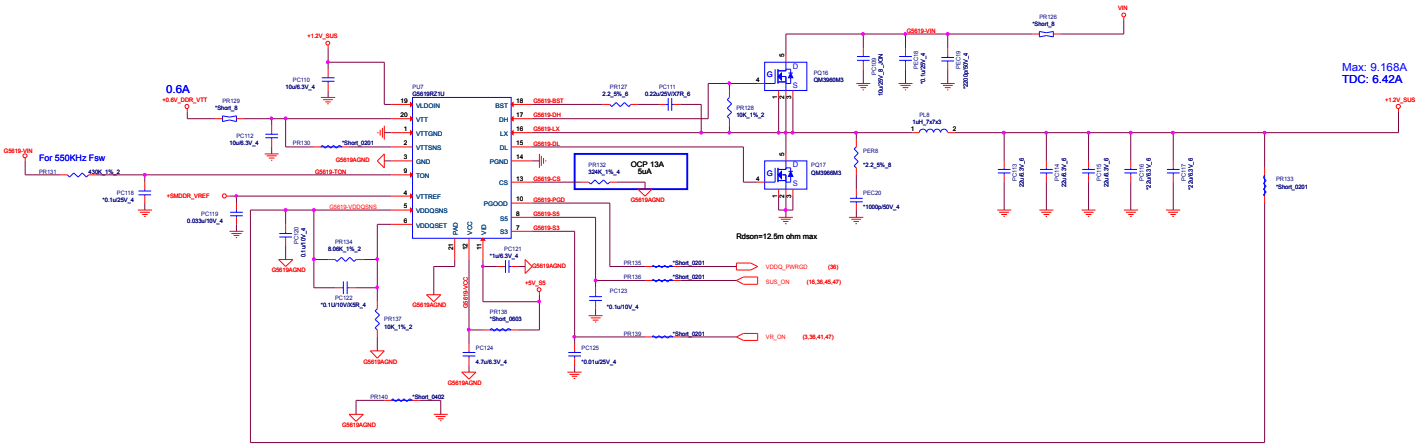
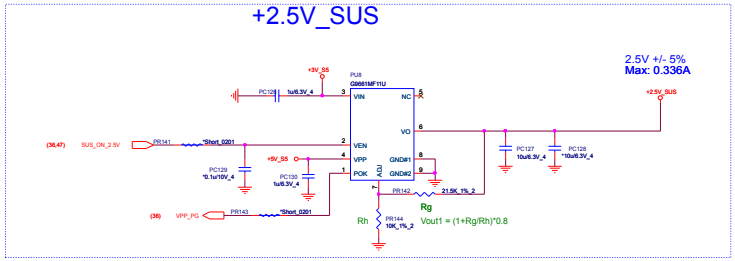
1.2VSUS & VTT_MEM



STATE	S3	S5	+1.2V_SUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

+2.5V_SUS



Quanta Computer Inc.
PROJECT : BKX

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	1.2VSUS/VTT	3A
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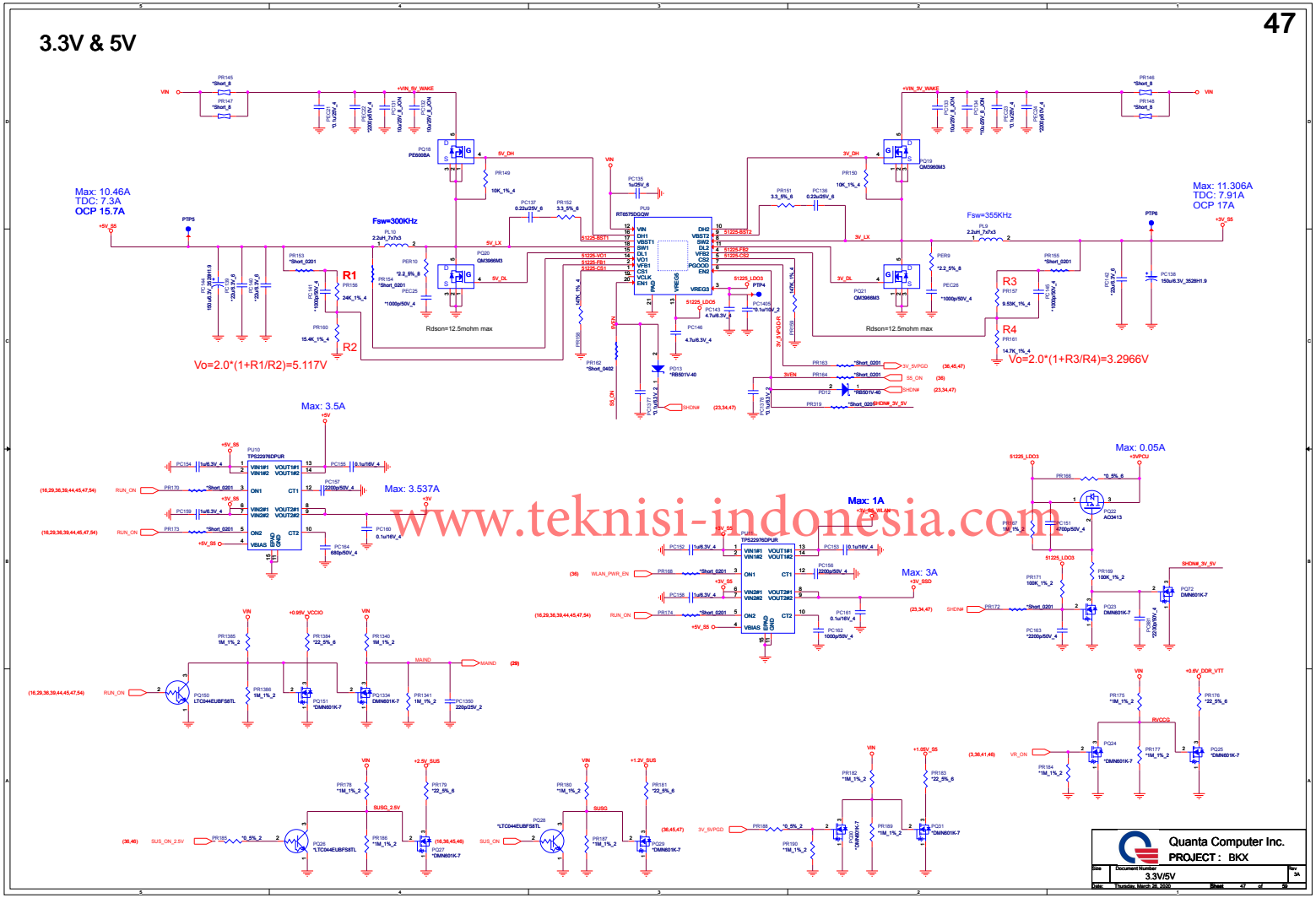
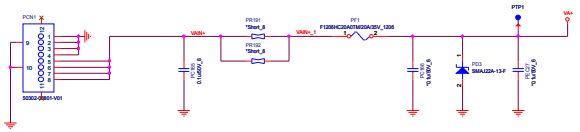
3.3V & 5V



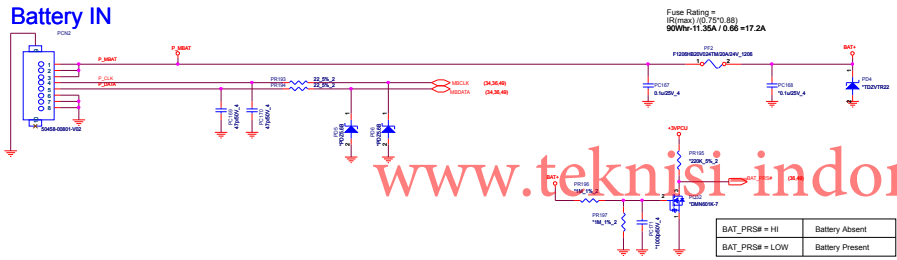
AC IN (On-Board DC-Jack)

Fuse Rating =
IR(max) /(0.75*0.88)
230W/19.5V / 0.66 =17.87A



Battery IN

Fuse Rating =
IR(max) /(0.75*0.88)
90Whr-11.35A / 0.66 =17.2A



BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present

Quanta Computer Inc.
PROJECT : BKX
AD IN/BAT IN
Rev 3A
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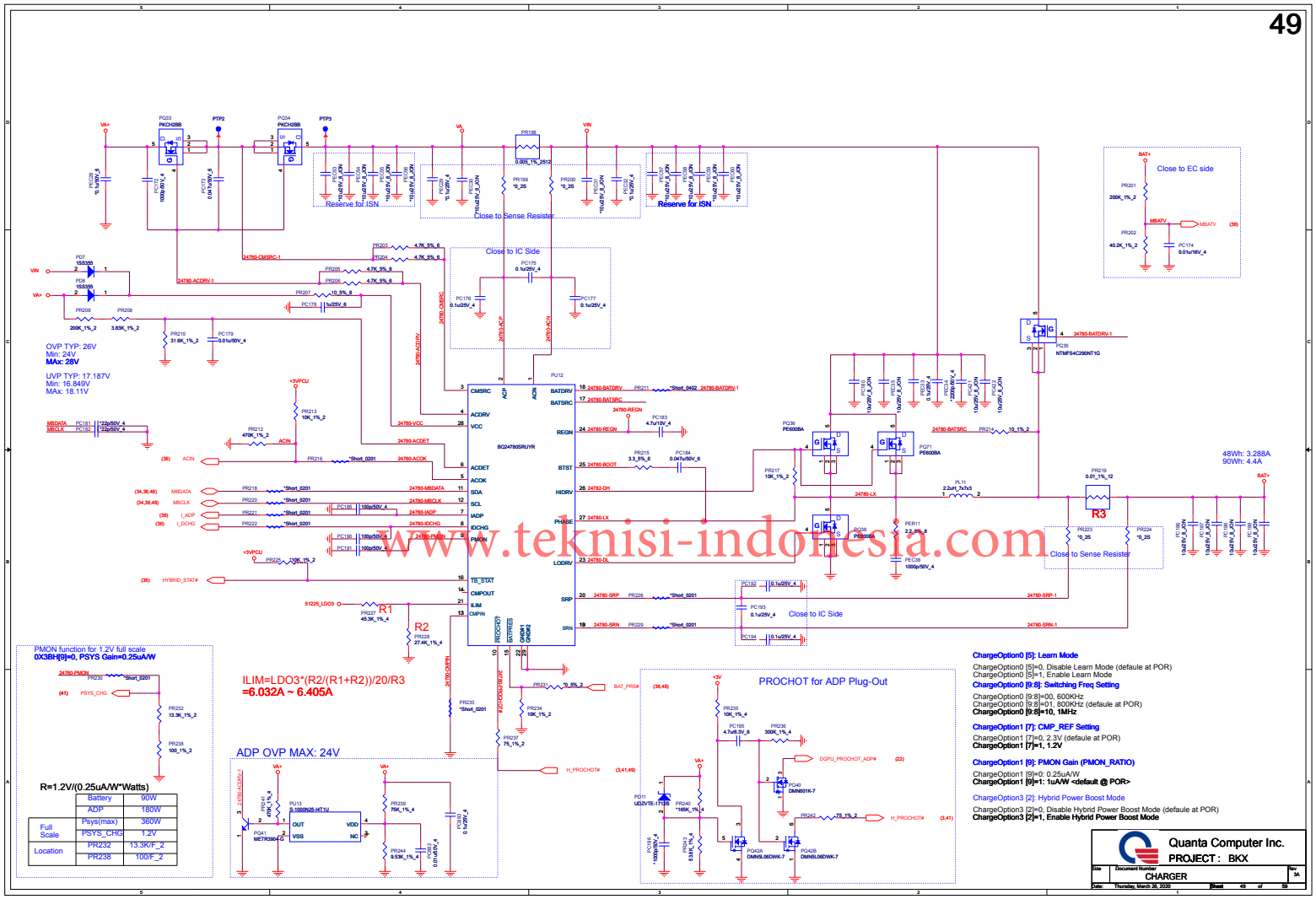
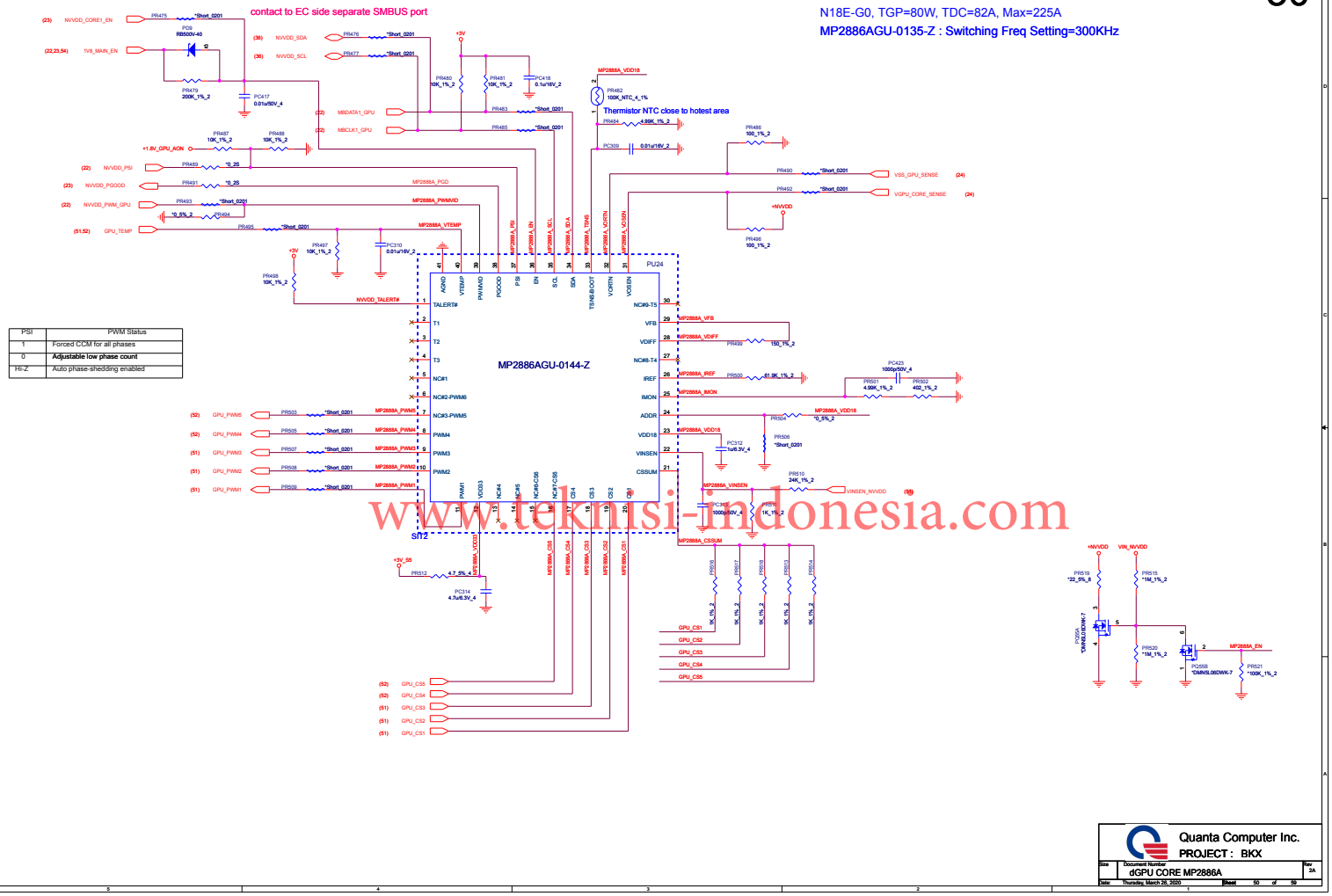
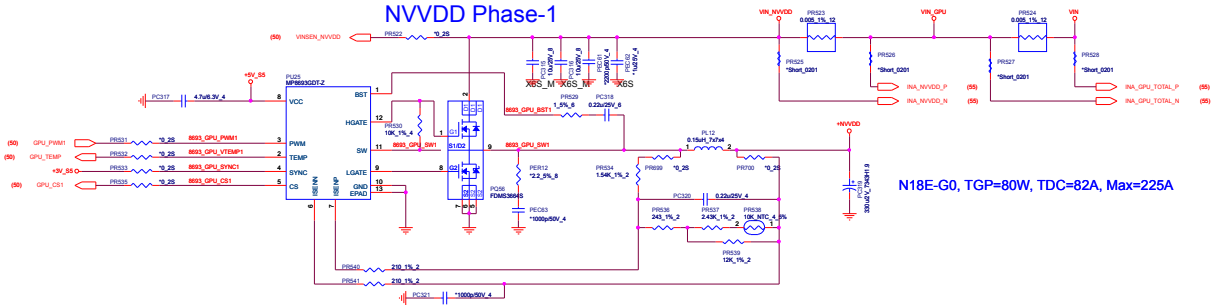


	Battery	90W
	ADP	180W
Full Scale	Psys(max)	360W
	PSYS_CHG	1.2V
Location	PR232	13.3K/F_2
	PR238	100/F_2

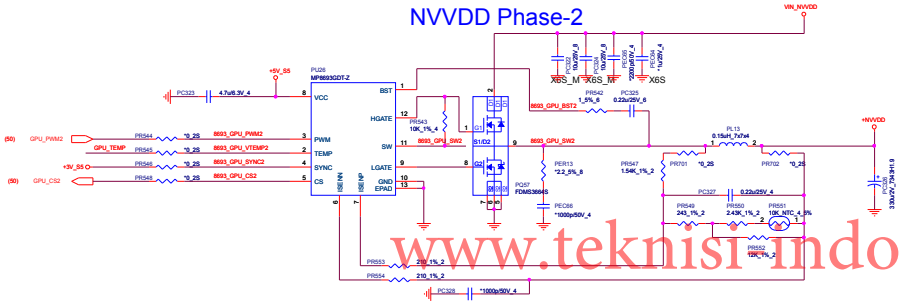


NVVDD Phase-1

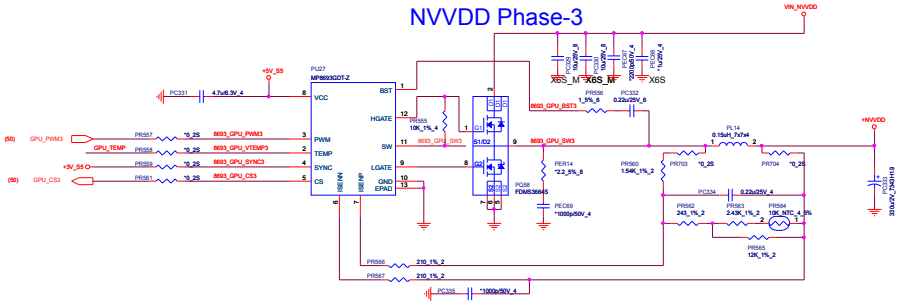


N18E-G0, TGP=80W, TDC=82A, Max=225A

NVVDD Phase-2



NVVDD Phase-3



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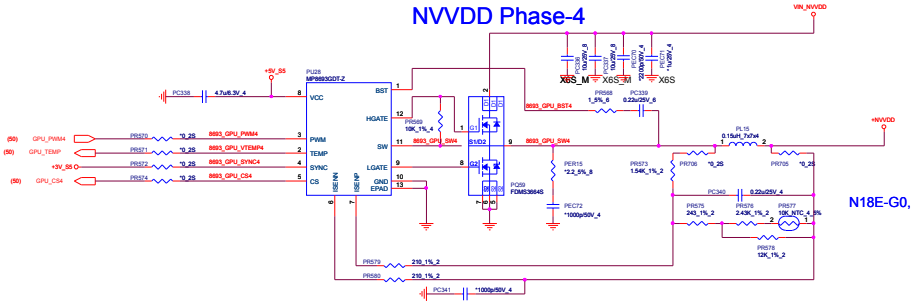
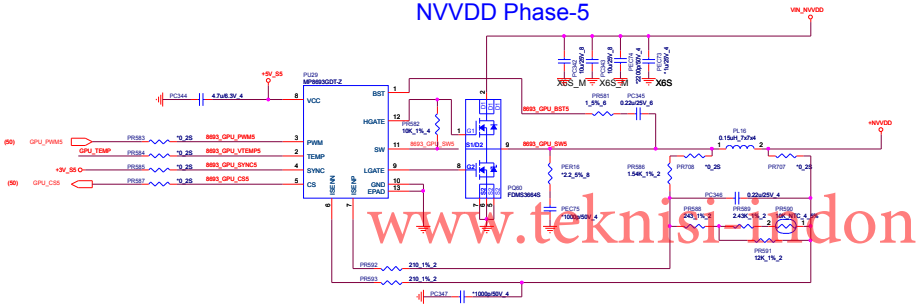
NVVDD Phase-4



N18E-G0, TGP=80W, TDC=82A, Max=225A

NVVDD Phase-5



Quanta Computer Inc.
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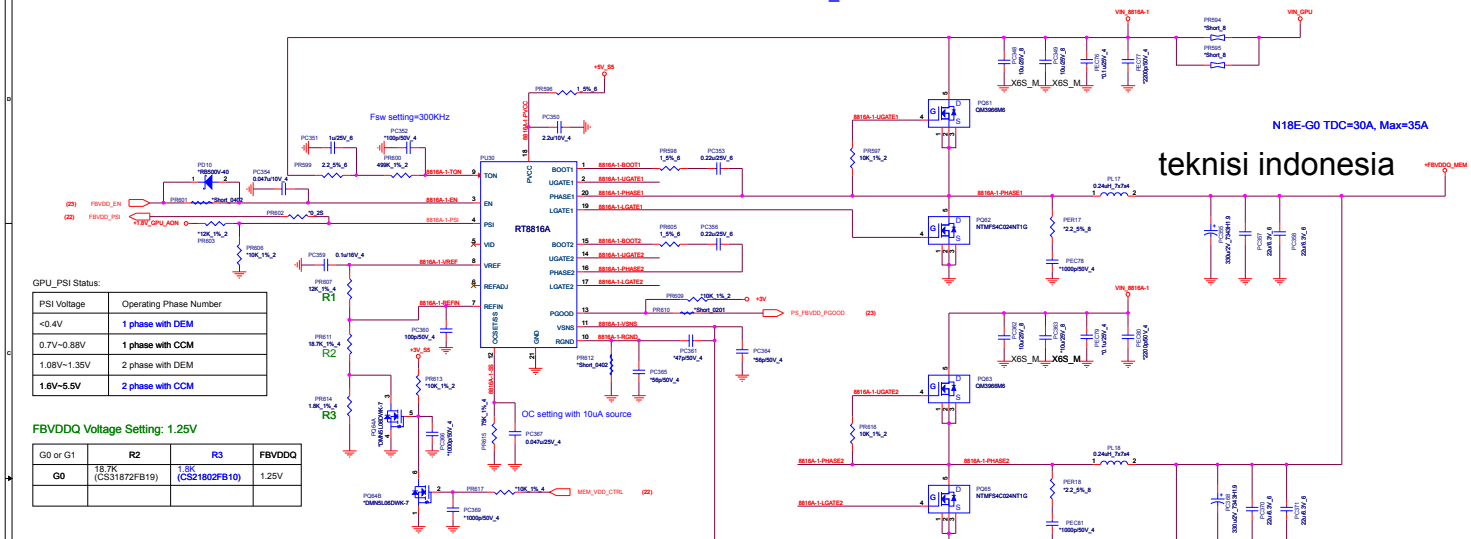
+FBVDDQ_MEM



GPU_PSI Status:

PSI Voltage	Operating Phase Number
<0.4V	1 phase with DEM
0.7V~0.88V	1 phase with CCM
1.08V~1.35V	2 phase with DEM
1.6V~5.5V	2 phase with CCM

FBVDDQ Voltage Setting: 1.25V

G0 or G1	R2	R3	FBVDDQ
G0	18.7K (CS31872FB19)	1.8K (CS21802FB10)	1.25V

Quanta Computer Inc.
PROJECT : BKX

+FBVDDQ_MEM (RT8816A)

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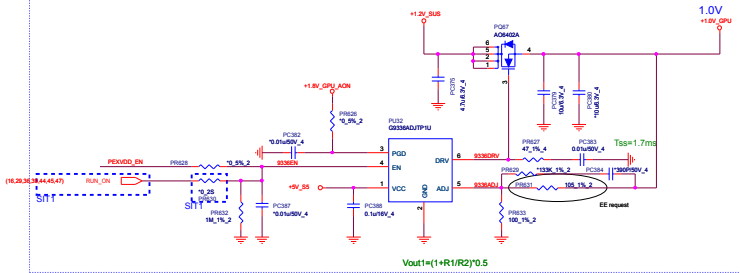
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

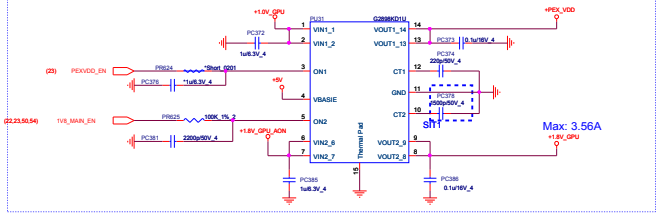
+1.0V_GPU

N18E-G0 TDC=1.6A, Max=2.5A

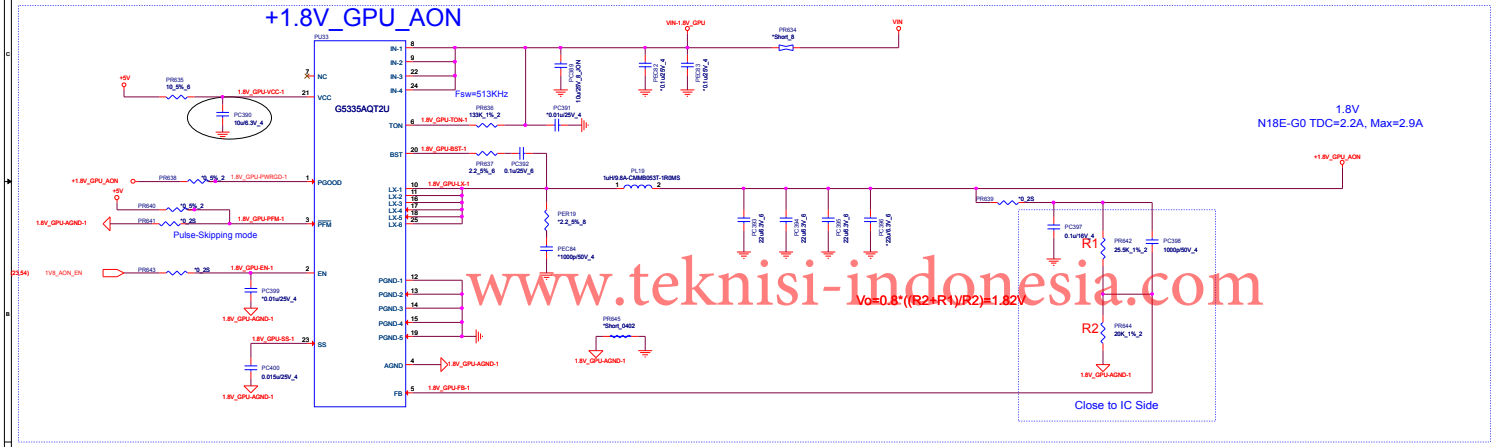


Load Switch for GPU

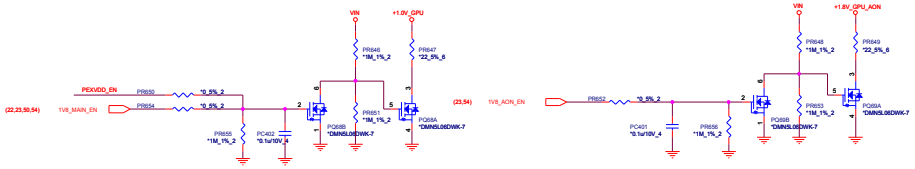
N18E-G0 TDC=1.6A, Max=2.5A

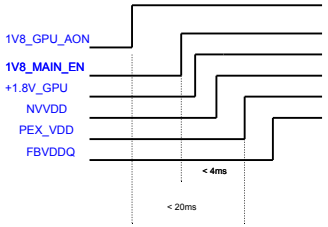


+1.8V_GPU_AON



Discharge





Quanta Computer Inc.
PROJECT : BKX
+1.8V_GPU_AON / 1.0V_GPU
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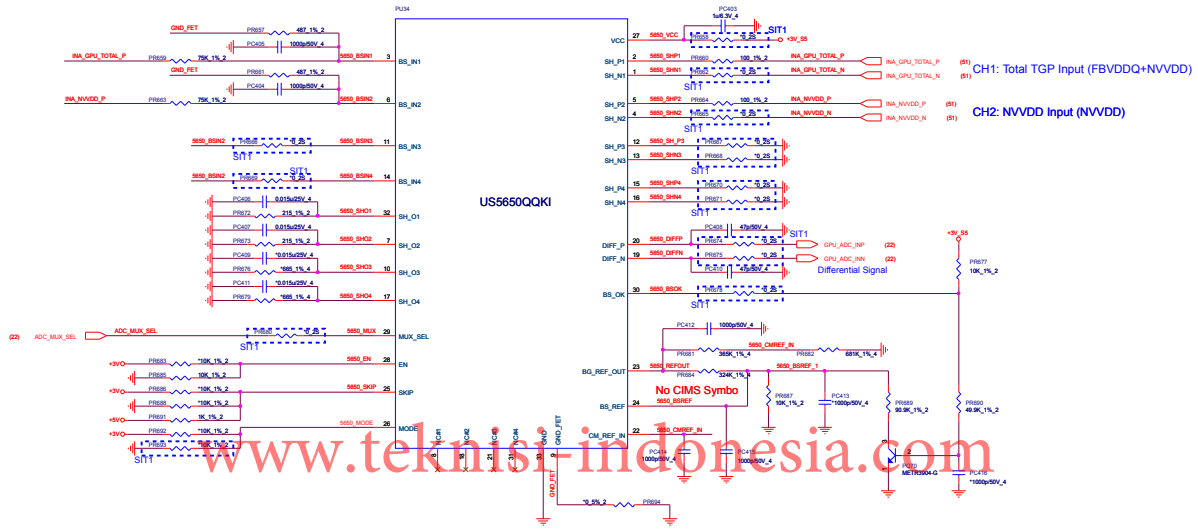
OVR-M



Quanta Computer Inc.
PROJECT : BKX
Document Number: VGAMON (OVR-M, US5650PQKI)
Rev: 2A
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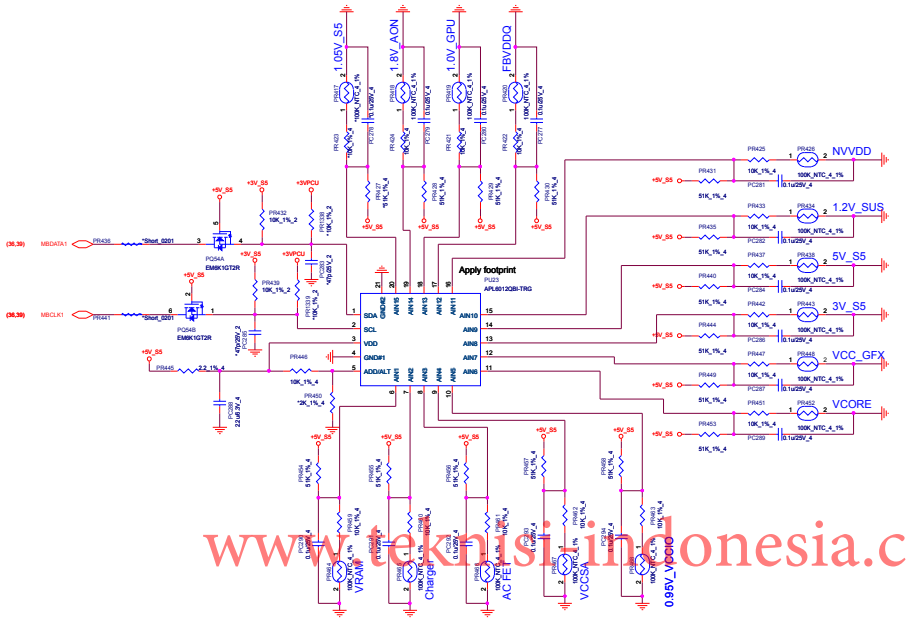
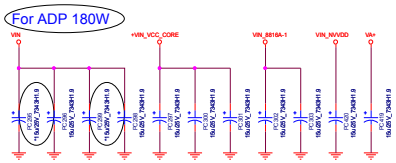
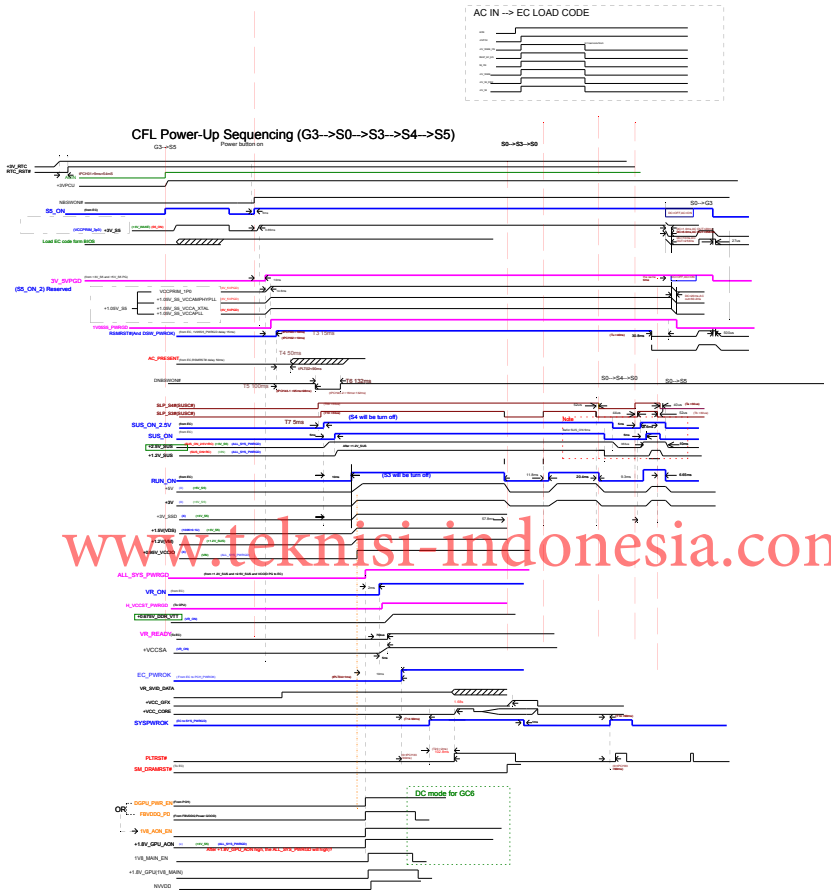
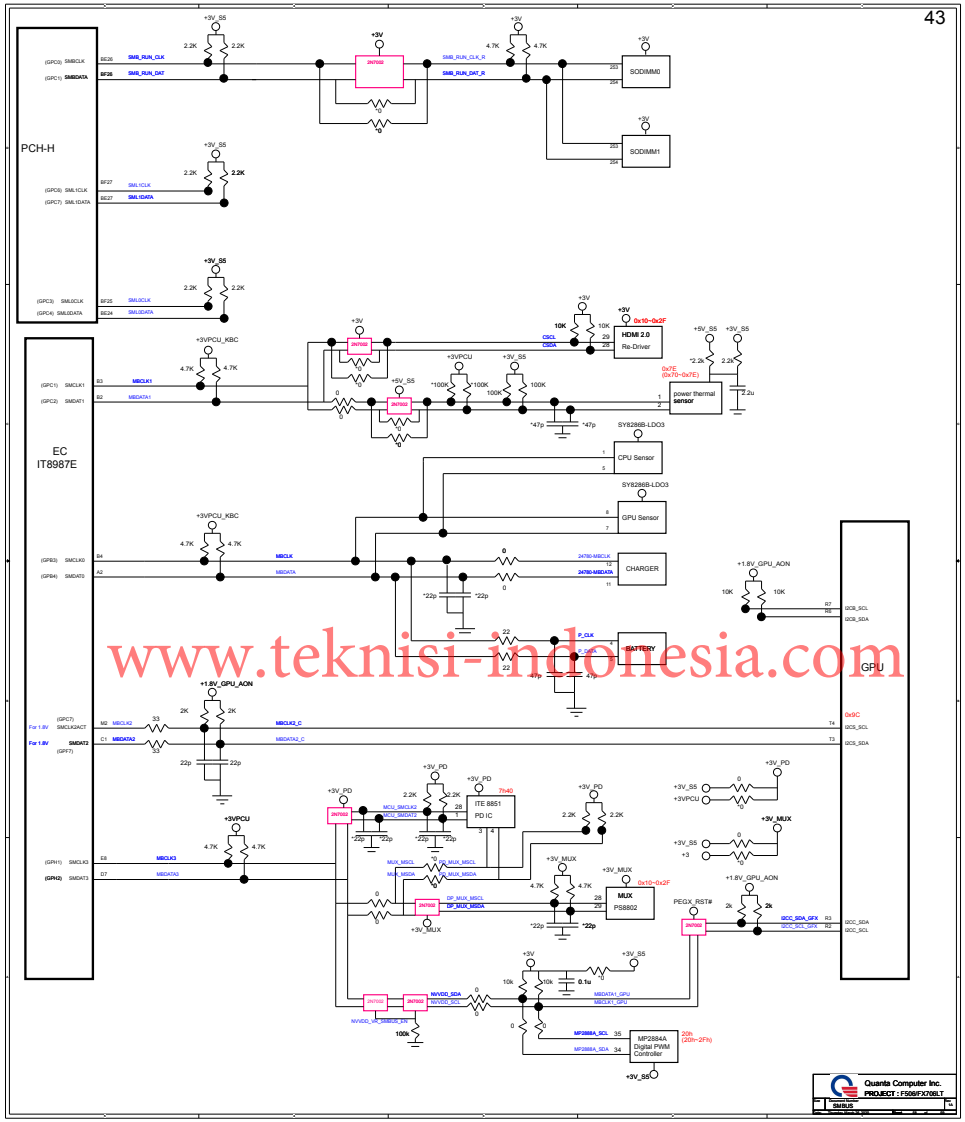




Quanta Computer Inc.
PROJECT : BKX
VGAMON (OVR-M, US5650POKI)
Thursday, March 26, 2020





OS status	S0	S0ix	S3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	C10	S3	S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")	
RUN_ON	H	H	L	L	L	L	L	
+3V	H	H	L	L	L	L	L	
+5V	H	H	L	L	L	L	L	
+0.675V_DDR_VTT	H	H	L	L	L	L	L	
+VCCSA	H	H	L	L	L	L	L	
+VCC_GFX	H	H	L	L	L	L	L	
+VCC_CORE	H	H	L	L	L	L	L	
C10_GATE	H	L	L	L	L	L	L	
+1.05V_VCCSTG	H	L	L	L	L	L	L	
+0.95V_VCCIO	H	L	L	L	L	L		
+1.2V_SUS_C10(VCCPLL_OC)	H	L	L	L	L	L	L	
SUS_ON	H	H	H	L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H	H	L	L	L	L	
+1.05V_SUS	H	H	H	L	L	L	L	
+1.2V_SUS	H	H	H	L	L	L	L	
SUS_ON_2.5V	H	H	H	L	L	L	L	
+2.5V_SUS	H	H	H	L	L	L	L	
S5_ON_2	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	L	L	
+1.8V_S5(From PCH)	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	

Quanta Computer Inc.
PROJECT : FX506L/FX706L

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	POWER MAP	1A

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