BAD50 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

D12G

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Title: *Cover Page*		
Size: A3	Document Number: BA40/50-HR	Rev: SD
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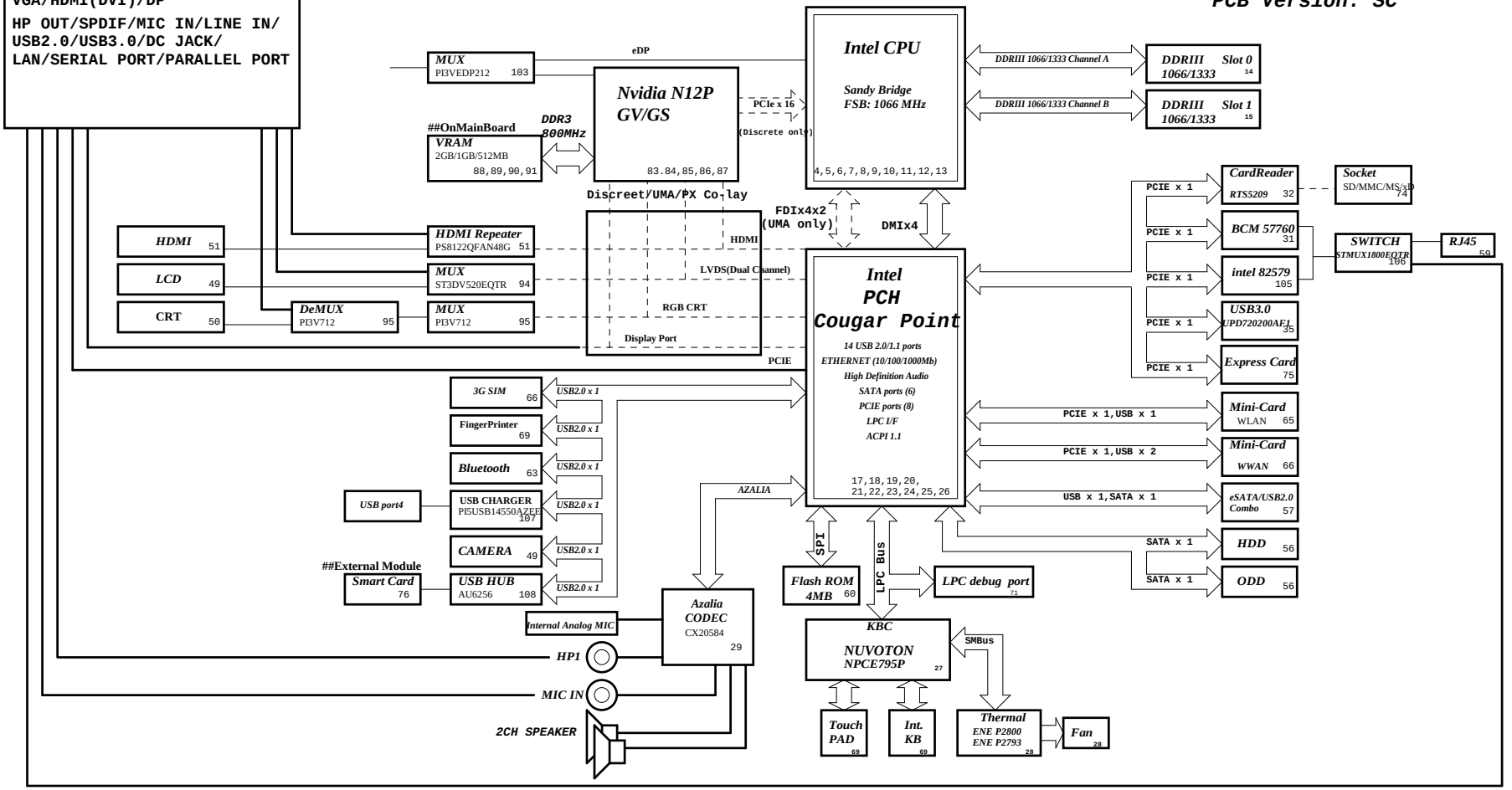
BAD50-HR Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4NM01.001
Project Name: BAD50_HR
PCB No: 10309
PCB Version: SC

Buttom Docking

VGA/HDMI(DVI)/DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



SYSTEM DC/DC TPS5146 48

INPUTS	OUTPUTS
5V_S5	0D85V_S0

CPU DC/DC VT1317SFCX 42~43

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8237AGQW 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8239CGQW 41

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207LGQW 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT1317SFCX 44

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208AGQW 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40

INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8015AGQW 47

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC

INPUTS	OUTPUTS

Switches

INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L5:Power
L2:GND L6:Signal
L3:Signal L7:GND
L4:Signal L8:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: ***Table of Content***

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A
SANDY

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Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

全改MUX

20100614 V1.1

Stuff to disable internal graphics function for power saving.

R404 Do Not Stuff DIS
RN401 Do Not Stuff DIS

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

UMA_EDP
Q401
Do Not Stuff
2ND = 84.2N702.031

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Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: BAD50-HR | Rev: SD
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SSID = CPU

CPU1B
SANDY

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SANDY

MISC
- 18 H_SNB_IVB# → C26 SNB_IVB#
- JE40 modify → AN34 SKTOCC#

THERMAL
- JE40 modify → AL33 CATERR#
- 22,27 H_PECI ↔ AN33 PECI
- 27,42 H_PROCHOT# → R513 56R2J-4-GP → H_PROCHOT#_R → AL32 PROCHOT#
- 22,36 H_THERMTRIP# ← AN32 THERMTRIP#

PWR MANAGEMENT
- 19 H_PM_SYNC ↔ AM34 PM_SYNC
- 22,36,97 H_CPUPWRGD → R503 10KR2J-GP → AP33 UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD → R505 DY Do Not Stuff → V8 SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# → AR33 RESET#

CLOCKS
- BCLK → A28 CLK_EXP_P 20
- BCLK# → A27 CLK_EXP_N 20
- DPLL_REF_SSCLK → A16 CLK_DP_P_R → CLK_DP_P_R 20
- DPLL_REF_SSCLK# → A15 CLK_DP_N_R → CLK_DP_N_R 20

DDR3 MISC
- SM_DRAMRST# → R8 R502 4K99R2F-L-GP → SM_DRAMRST# 37
- SM_RCOMP0 → AK1 SM_RCOMP_0 R506 140R2F-GP
- SM_RCOMP1 → A5 SM_RCOMP_1 R507 25D5R2F-GP
- SM_RCOMP2 → A4 SM_RCOMP_2 R508 200R2F-L-GP

JTAG & BPM
- PRDY# → AP29
- PREQ# → AP27
- JE40 modify
- TCK → AR26
- TMS → AR27
- TRST# → AP30 XDP_TRST#
- TDI → AR28
- TDO → AP26 XDP_TDO
- DBR# → AL35 XDP_DBRESET#
- BPM#0 → AT28
- BPM#1 → AR29
- BPM#2 → AR30
- BPM#3 → AT30
- BPM#4 → AP32
- BPM#5 → AR31
- BPM#6 → AT31
- BPM#7 → AR32
- JE40 modify

1D05V_VTT → R501 62R2J-GP → H_PROCHOT#
C502 SC47P50V2JN-3GP

C502:
47pf@CRB
43pf@CEKLT

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CLK_DP_N_R 2 / CLK_DP_P_R 1 → RN502 DIS Do Not Stuff → 1D05V_VTT

1D05V_VTT → RN501 SRN51J-GP
XDP_TDO 2
XDP_TRST# 1

3D3V_S0 → RN503 SRN1K5J-1-GP
XDP_DBRESET# 1
PLT_RST# 3
BUF_CPU_RST# 5
35,36,65,66,71,75,82,83,97,105,108

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Title: **CPU (THERMAL/CLOCK/PM)**

Size: Custom | Document Number: **BA40-HR** | Rev: **SD**

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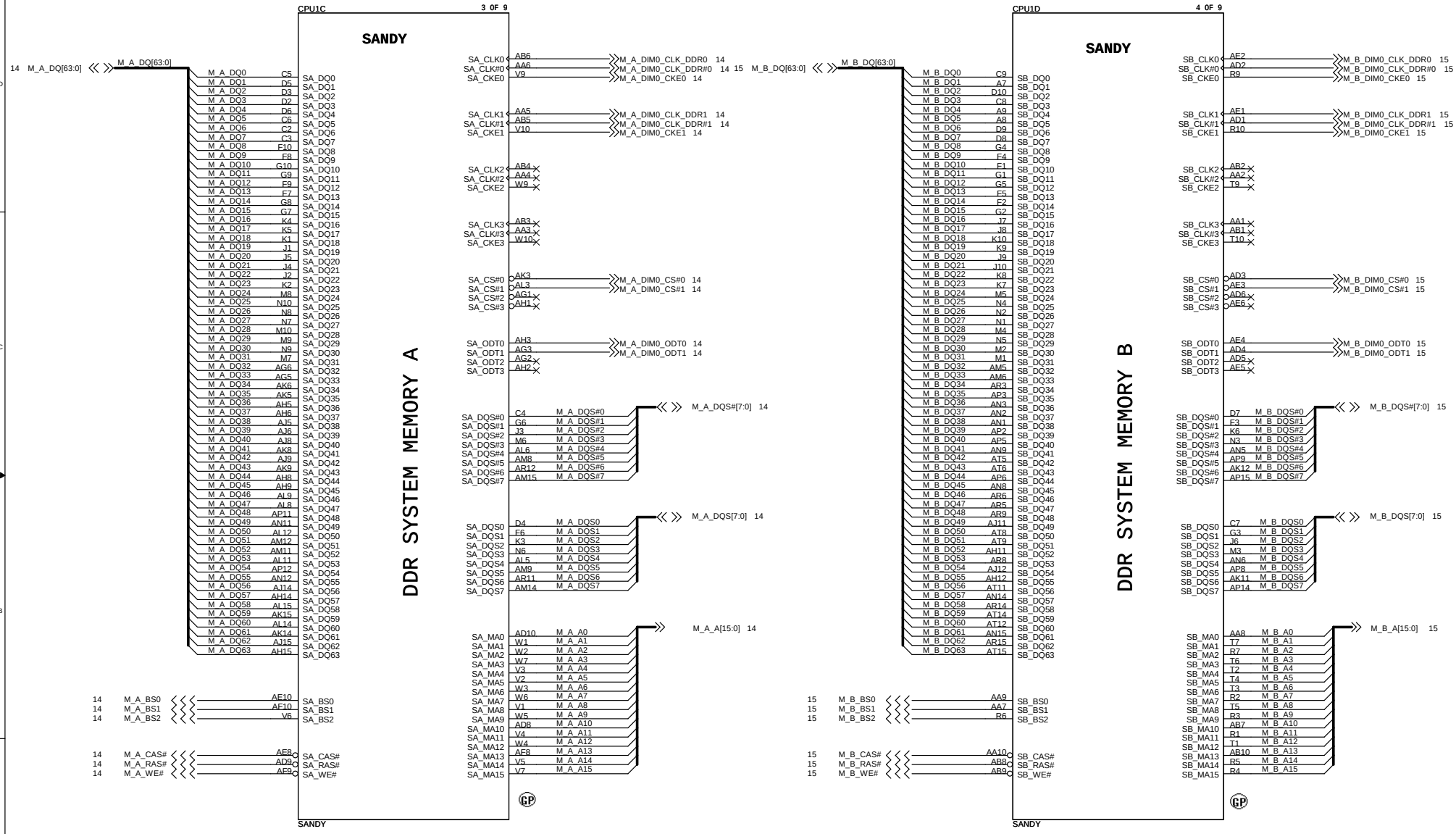
SSID = CPU



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Title	CPU (DDR)
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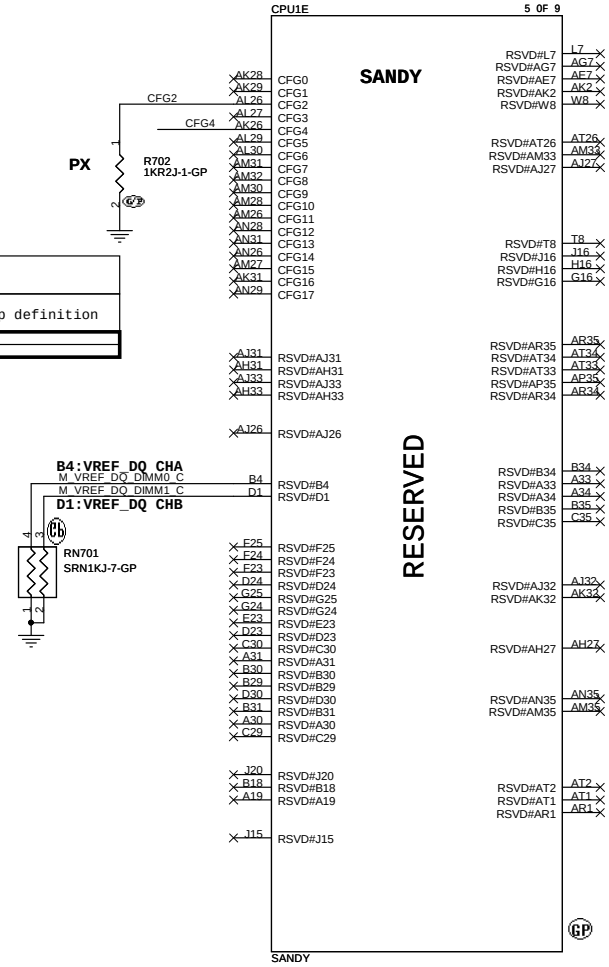
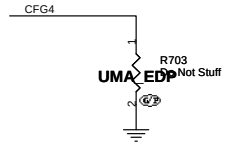
SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed





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Title: CPU (RESERVED)		
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SSID = CPU

POWER

CPU1F

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SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A

VCC_CORE

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT 42

R801,R802 close to CPU

R801 Do Not Stuff

R802 Do Not Stuff

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

VCCIO_SENSE B10 VCCIO_SENSE 45
VSSIO_SENSE A10 VSSIO_SENSE 45

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Title: CPU (VCC_CORE)

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

+VCC_GFXCORE

R906 DY Do Not Stuff

VCC_AXG_SENSE
VSS_AXG_SENSE

R907 DY Do Not Stuff

PROCESSOR VAXG: 24A

CPU1G 7 OF 9

SANDY

GRAPHICS

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 DY Do Not Stuff
C910 SC10U6D3X6MX-L-GP
C911 SC10U6D3X6MX-L-GP
C912 SC10U6D3X6MX-L-GP
C913 SC10U6D3X6MX-L-GP
C914 DY Do Not Stuff

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 DY Do Not Stuff
C915 SC10U6D3X6MX-L-GP

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

SA RAIL

0D85V_S0

R902 10R2J-2-GP

R902 need be close to pin H23.

VCCSA_SENSE H23 → VCCUSA_SENSE → TP901 Do Not Stuff

FC_C22 C22 → H_FC_C22
VCCSA_VID1 C24 → VCCSA_SEL 48

RN901 SRN1KJ-7-GP

MISC

1.8V RAIL

+VCC_GFXCORE

R903 DIS Do Not Stuff
R904 DIS Do Not Stuff
R905 DIS Do Not Stuff
R901 DIS Do Not Stuff

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6, A6, A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

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Title: **CPU (VCC_GFXCORE)**

Size: A3 | Document Number: **BA40-HR** | Rev: **SD**

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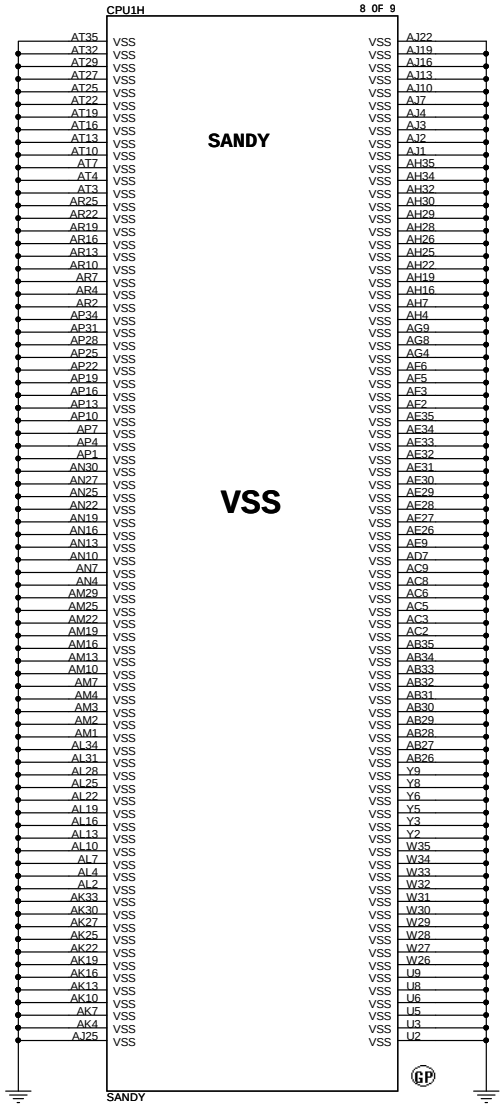
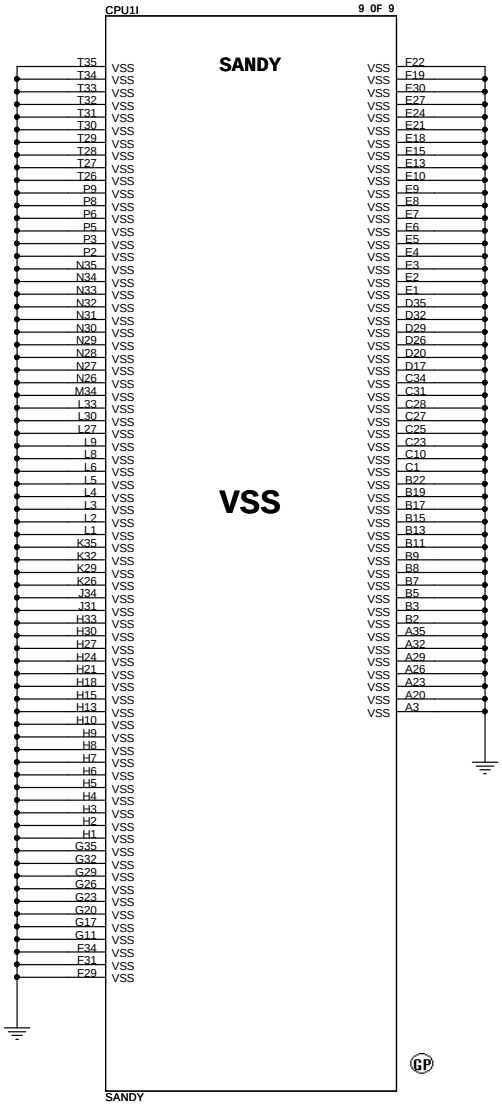
SSID = CPU





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Title: *CPU (VSS)*

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JE40 delete XDP function

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Title	***XDP***
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Title: ***Reserved***

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Title: ***Reserved***

Size	Document Number	Rev
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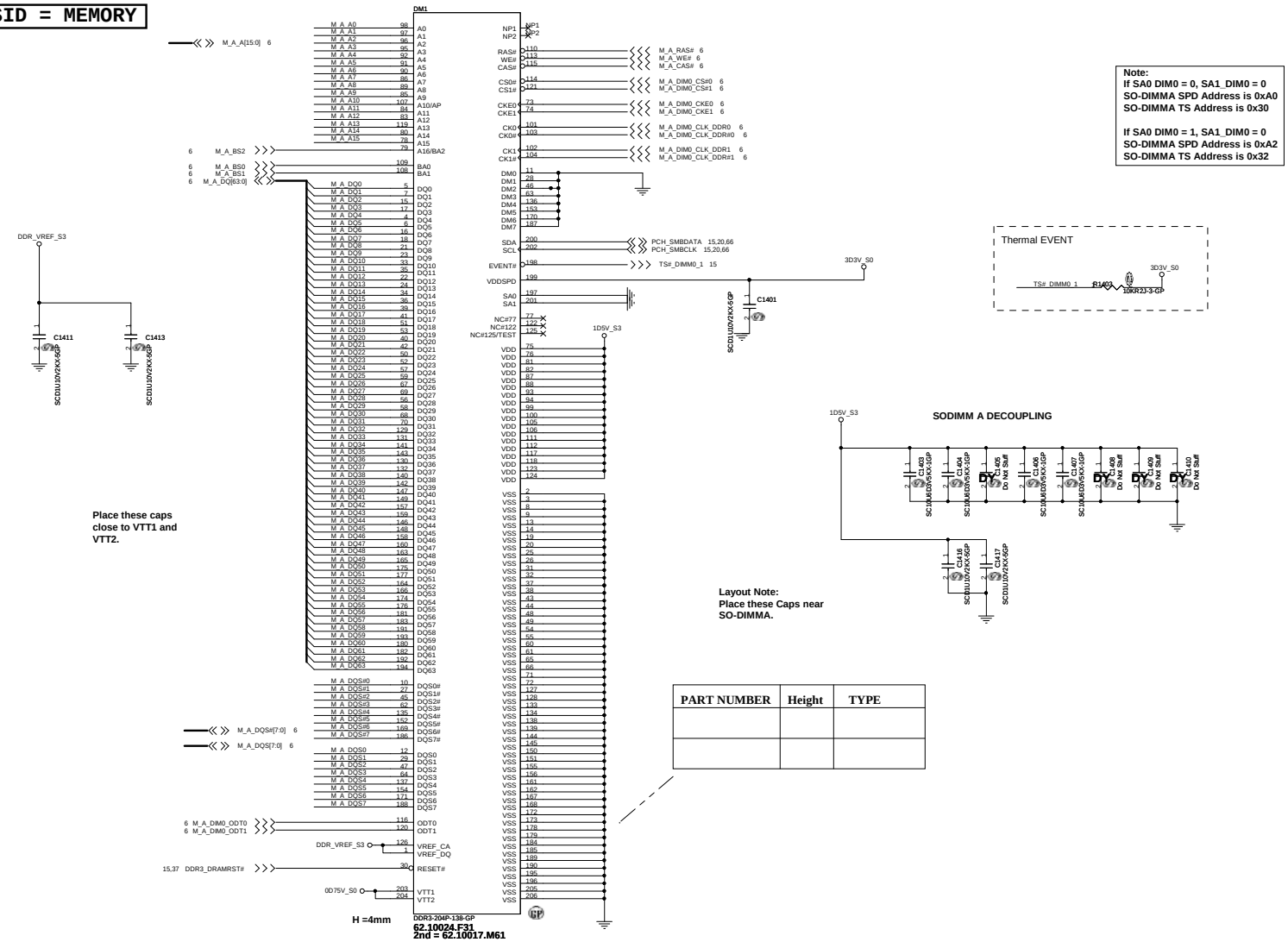
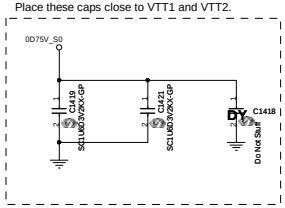
SSID = MEMORY



PART NUMBER	Height	TYPE

Place these caps close to VTT1 and VTT2.



D12G

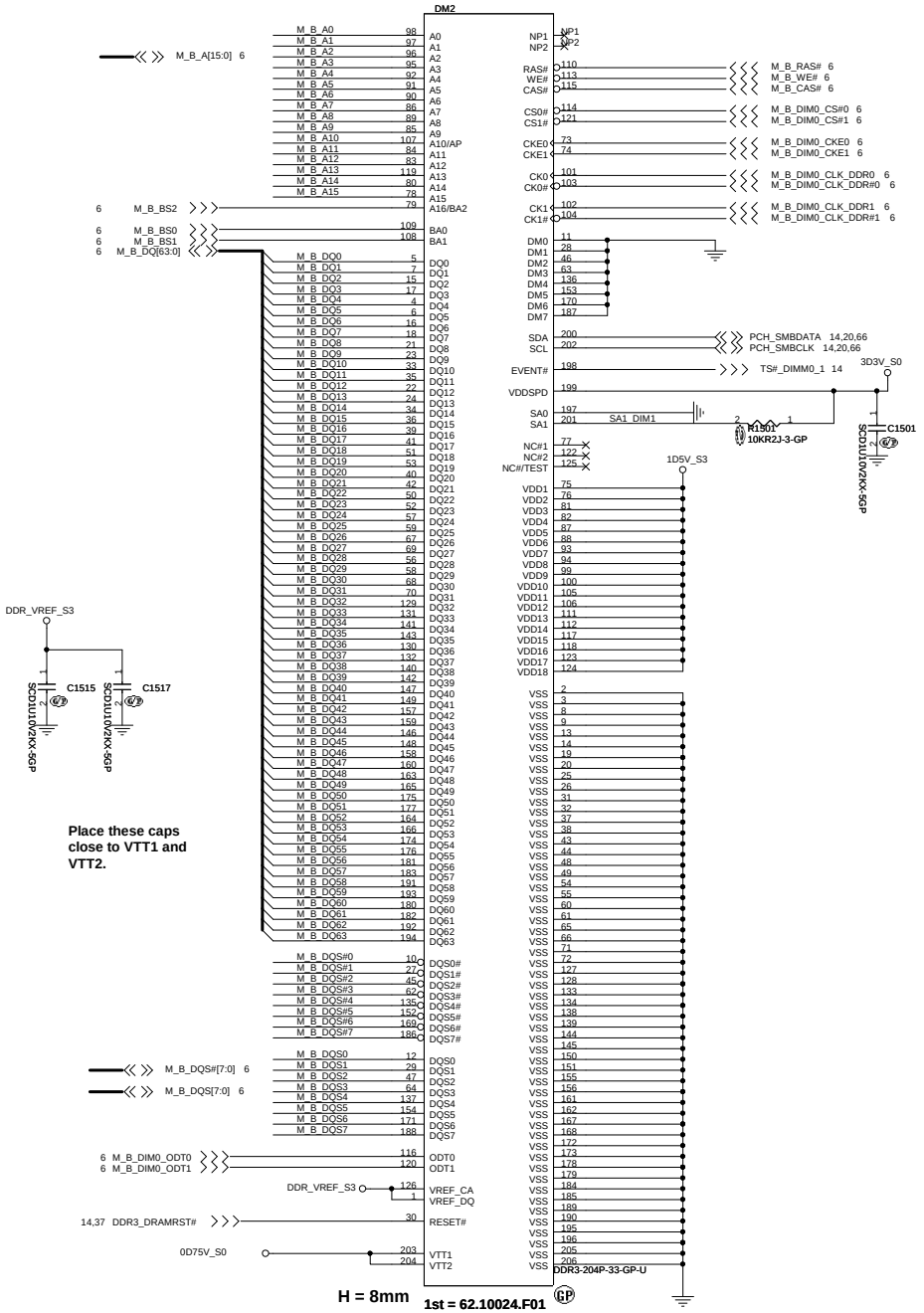
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 14 of 109

SSID = MEMORY



Place these caps close to VTT1 and VTT2.

H = 8mm

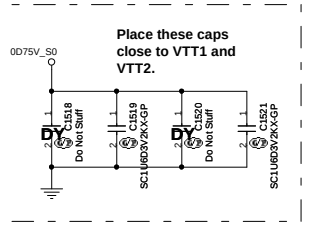
1st = 62.10024.F01

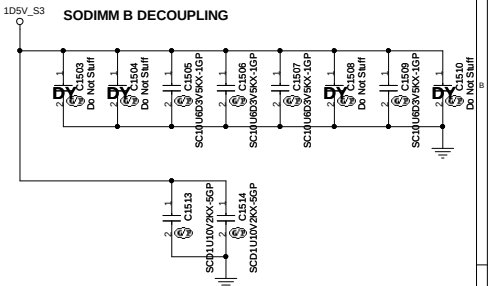
2nd = 62.10017.M71

Due to strange symbol of 62.10024.F01,
we use 62.10017.M31 symbol. (62.10017.M31 was deleted by connector list)

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA





Layout Note:
Place these Caps near SO-DIMMB.

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR3-SODIMM2*

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 15 of 109

(Blanking)

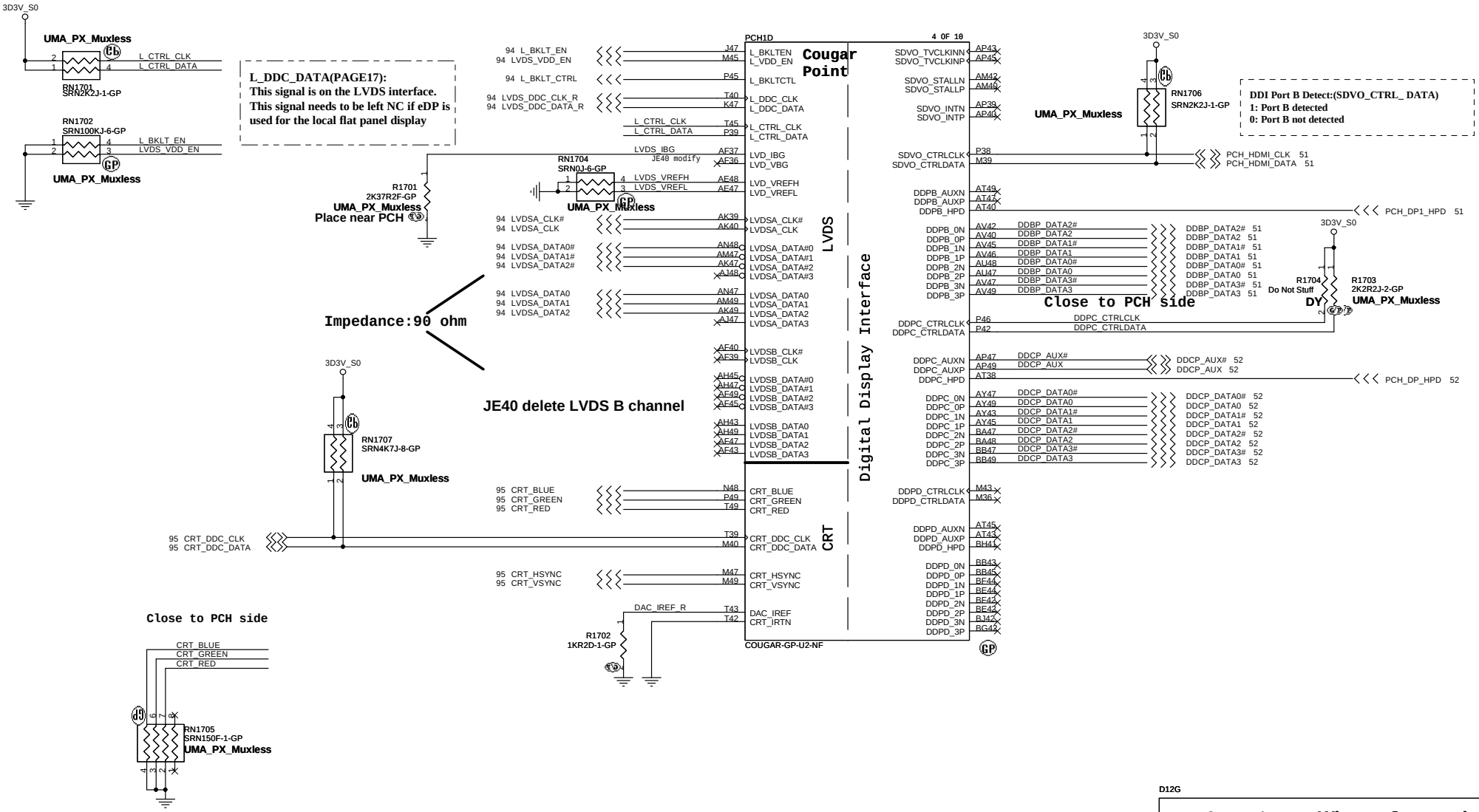
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR3-SODIMM2*

Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 16 of 109



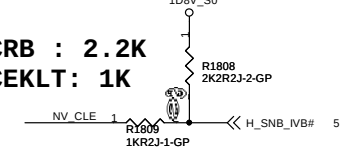
D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (LVDS/CRT/DDI)***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 17 of 109	

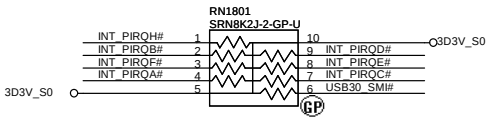
SSID = PCH

check R1808 R1809 阻值

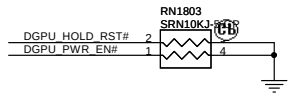
CRB : 2.2K
CEKLT: 1K



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	3G Card
1	USB port1(SATA Combo),on M/B
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	Dock
6	X
7	X
8	USB port4 on S/B(usb charger)
9	USB port 2 on S/B
10	USB port 3 (only when 3.0 not support)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

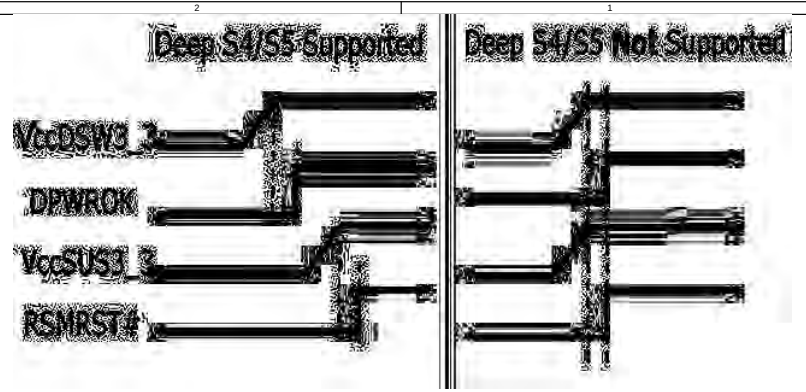
Title: PCH (PCI/USB/NVRAM)

Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 18 of 109

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10 — Cougar Point — DMI / FDI / System Power Management

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

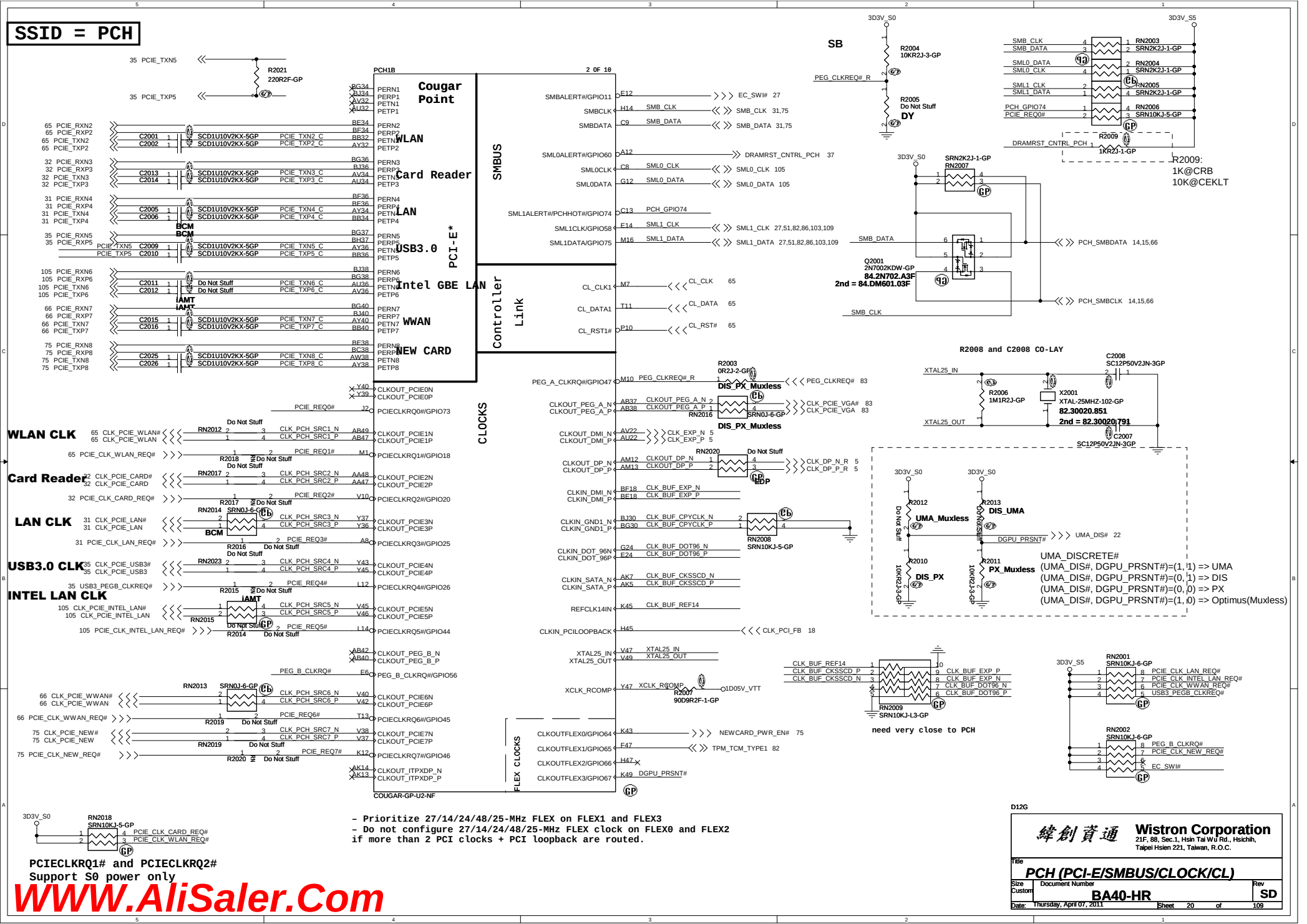
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 19 of 109

SSID = PCH



D12G

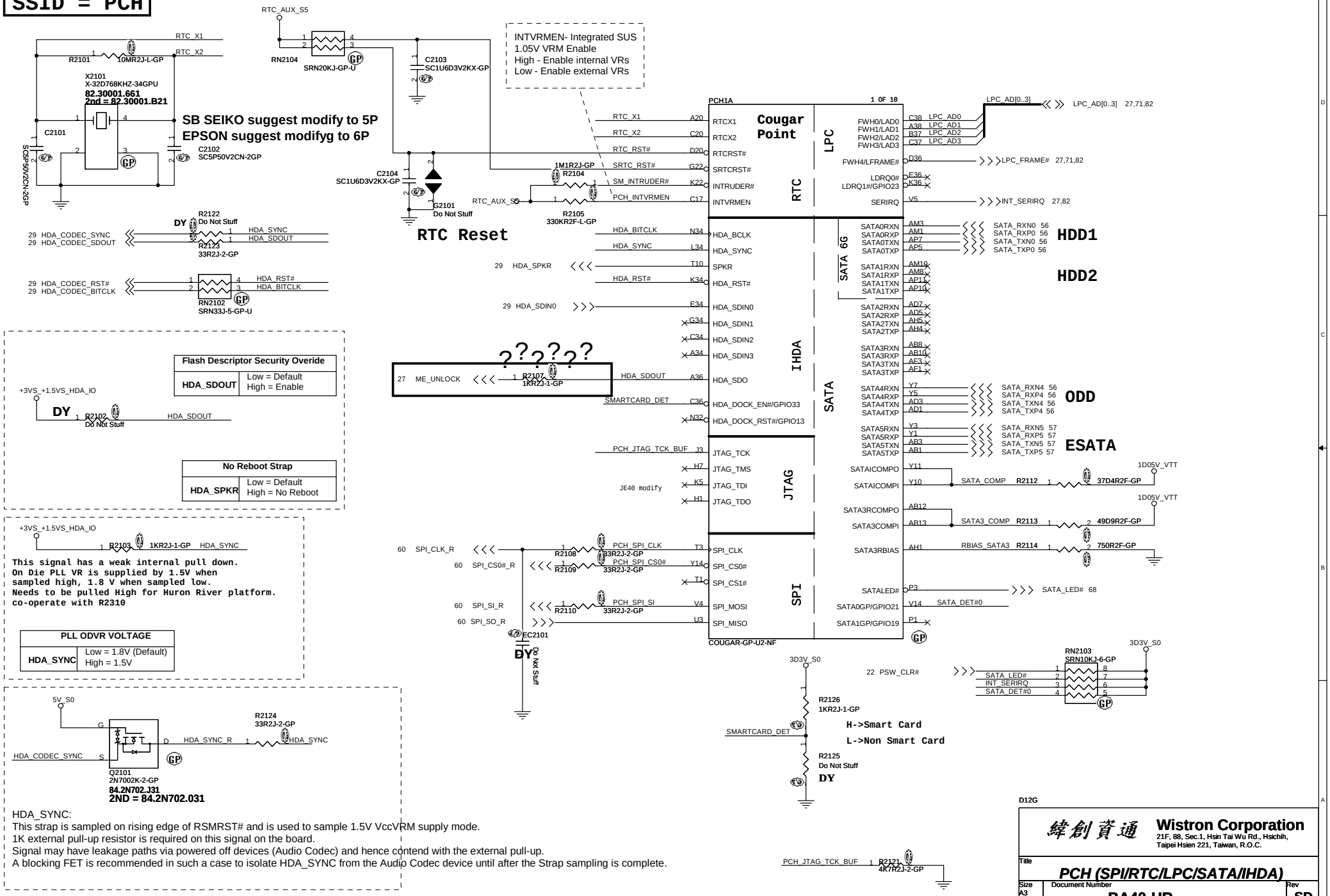
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 20 of 109

SSID = PCH



HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.
1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 21 of 109

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Password Clear

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

VRAM Frequency
PCH_GPIO22=1 : 800MHZ
PCH_GPIO22=0 : 900MHZ

VRAM Size

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 22 of 109

SSID = PCH 6A

PCH1G **POWER** 7 OF 10

Cougar Point

VCC CORE | CRT | LVDS | HVCMOS | DMI | NAND / SPI | FDI | VCCIO

1D05V_VTT 1.3A (1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP; C2302 SCLU6D3V2KX-GP; C2303 SCLU6D3V2KX-GP; C2304 SCLU6D3V2KX-GP

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 VCCCORE

1D05V_VTT AN19 VCCIO

JE40 modify 07/16

BJ22 VCCAPLLEXP

1D05V_VTT 2.925A(Total current of VCCIO)

DY C2306 Do Not Stuff; C2307 SCLU6D3V2KX-GP; C2308 SCLU6D3V2KX-GP; C2309 SCLU6D3V2KX-GP

(1uF x4)

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 VCCIO

0.266A (Totally VCC3_3 current)

3D3V_S0 (0.1uF x1) C2310 SCD01U10V2KX-5GP

BH29 VCC3_3

VCCVRM 1D5V_S0 R2316 0R3J-0-U-GP; 1D8V_S0 R2317 DY Do Not Stuff

VCCVRM AP16 VCCVRM

0.159A(Totally current of VCCVRM)

BG6 VCCAFDIPLL

0806 check VCCAFDIPLL

1D05V_VTT AP17 VCCIO

1D05V_VTT AU20 VCCDMI

0.042A (Totally current of VCCDMI)

COUGAR-GP-U2-NF

VCCADAC U48 +VCCA_DAC_1_2

VSSADAC U47

(0.1uF/0.01uF x1) (10uF x1_0603)

C2313 SCD01U10V2KX-3GP; C2314 SCD01U10V2KX-5GP; C2315 DY Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

R2315 0R5J-5-U 3D3V_DAC_S0 UMA_PX_Muxless

0.001A

VCCALVDS AK36 +3VS_VCCA_LVDS

VSSALVDS AK37

DIS R2304 0R3J-0-U-GP 3D3V_S0 UMA_PX_Muxless

R2303 Do Not Stuff

VCCTX_LVDS AM37 AM38 AP36 AP37

+1.8VS_VCCTX_LVDS

0.06A

R2309 DIS Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

C2316 SCD01U16V2KX-3GP; C2317 SCD01U16V2KX-3GP; C2318 DY Do Not Stuff

R2305 0R5J-5-U 1D8V_S0

(0.01uF x2) (22uF x1)

U2301 for ANNIE flicker issue
R2312 for don't flicker solution

3.3V CRT LDO

U2301 G9091-330T11U-GP 74.09091.J3F

5V_S0 C2311 SC1U10V2KX-1GP

VIN GND EN VOUT NC#4

UMA_PX_Muxless

2nd = 74.70233.031 UMA_PX_Muxless

3D3V_DAC_S0 C2312 SCU6D3V2KX-GP; C2327 SC10U6D3V3MX-GP

SB add C2327

UMA_PX_Muxless

VCC3_3 V33 V34

3D3V_S0 (0.1uFx1)

C2319 SCD1U10V2KX-5GP

VCCVRM AT16 VCCVRM

VCCDMI AT20 JE40 modify 1D05V_VTT (1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI AB36

+1.05VS_VCC_DMI_CCI

0.02A

L2303 0R3J-0-U-GP 1D05V_VTT (1uFx1) (10uFx1)

C2321 SC1U6D3V2KX-GP; C2325 DY Do Not Stuff

VccDFTERM AG16 AG17 AJ16 AJ17

1D8V_S0 0.19A JE40 modify

C2326 SCD1U10V2KX-5GP; C2322 SCD1U10V2KX-5GP

VCCSPI V1

0.02A (1uFx1)

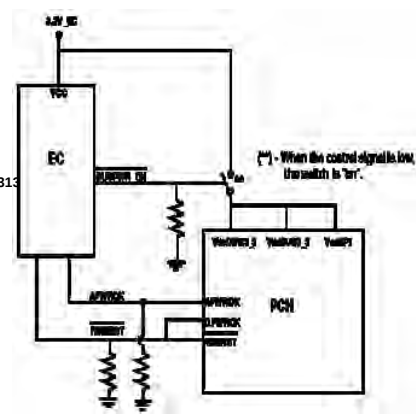
3D3V_S5

C2323 SC1U6D3V2KX-GP

SB 公板suggest delete 3D3V_S0, R2313
SPI only support 3D3V_S5

The same BIOS SPI ROM power

Refer to NPCE795 shared SPI flash architecture



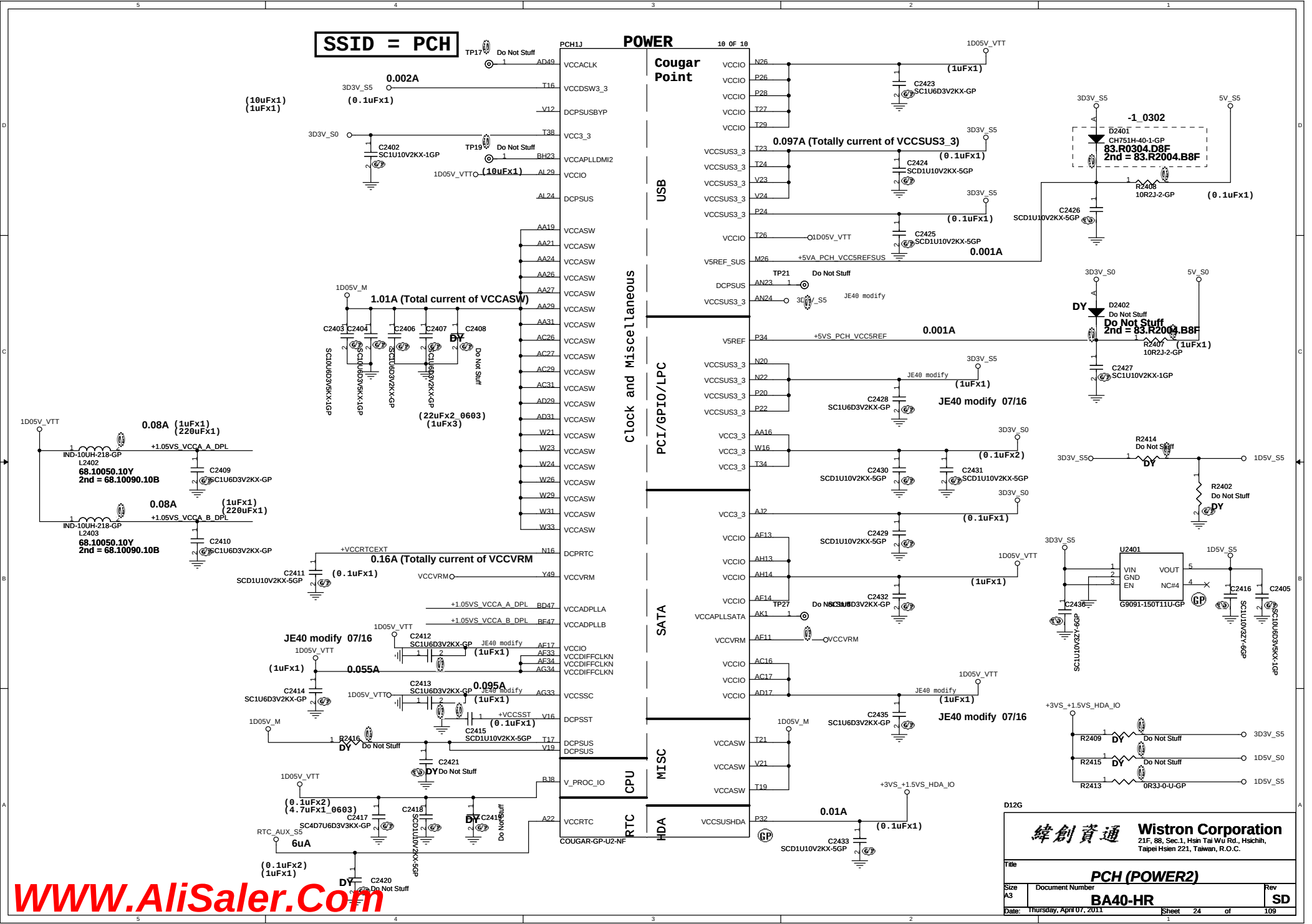
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

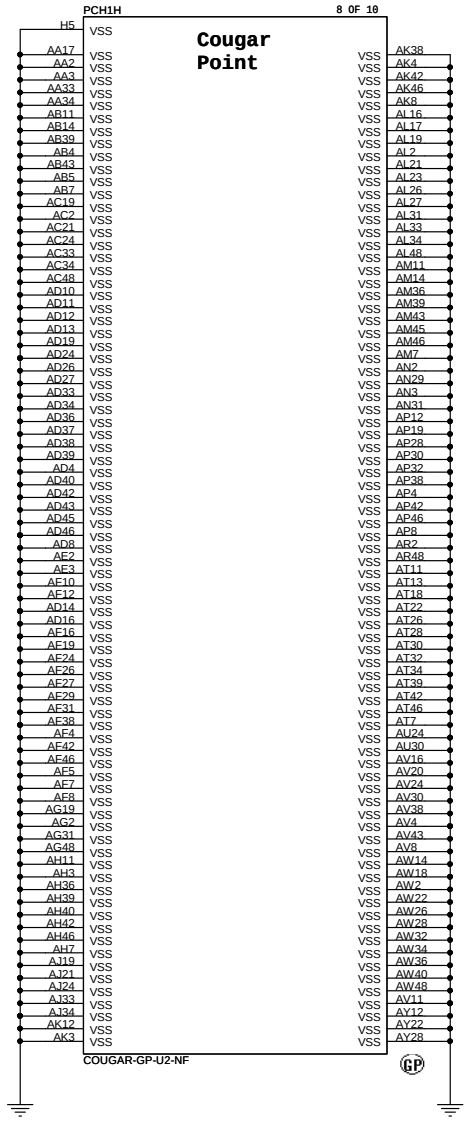
Title: PCH (POWER1)

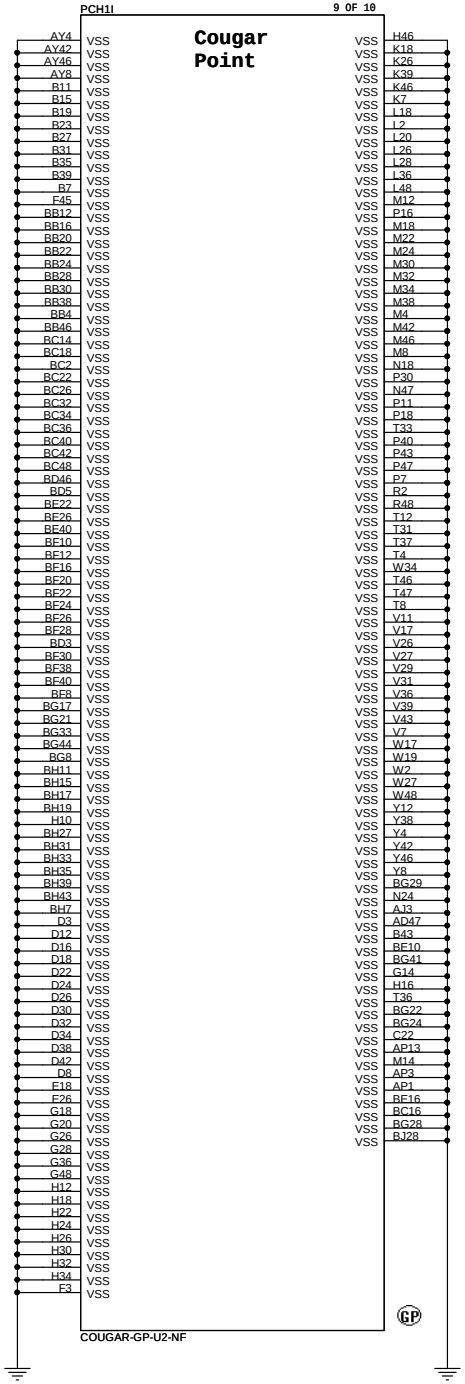
Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 23 of 109



SSID = PCH





D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (VSS)***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 25 of 109	

D12G

緯創資通

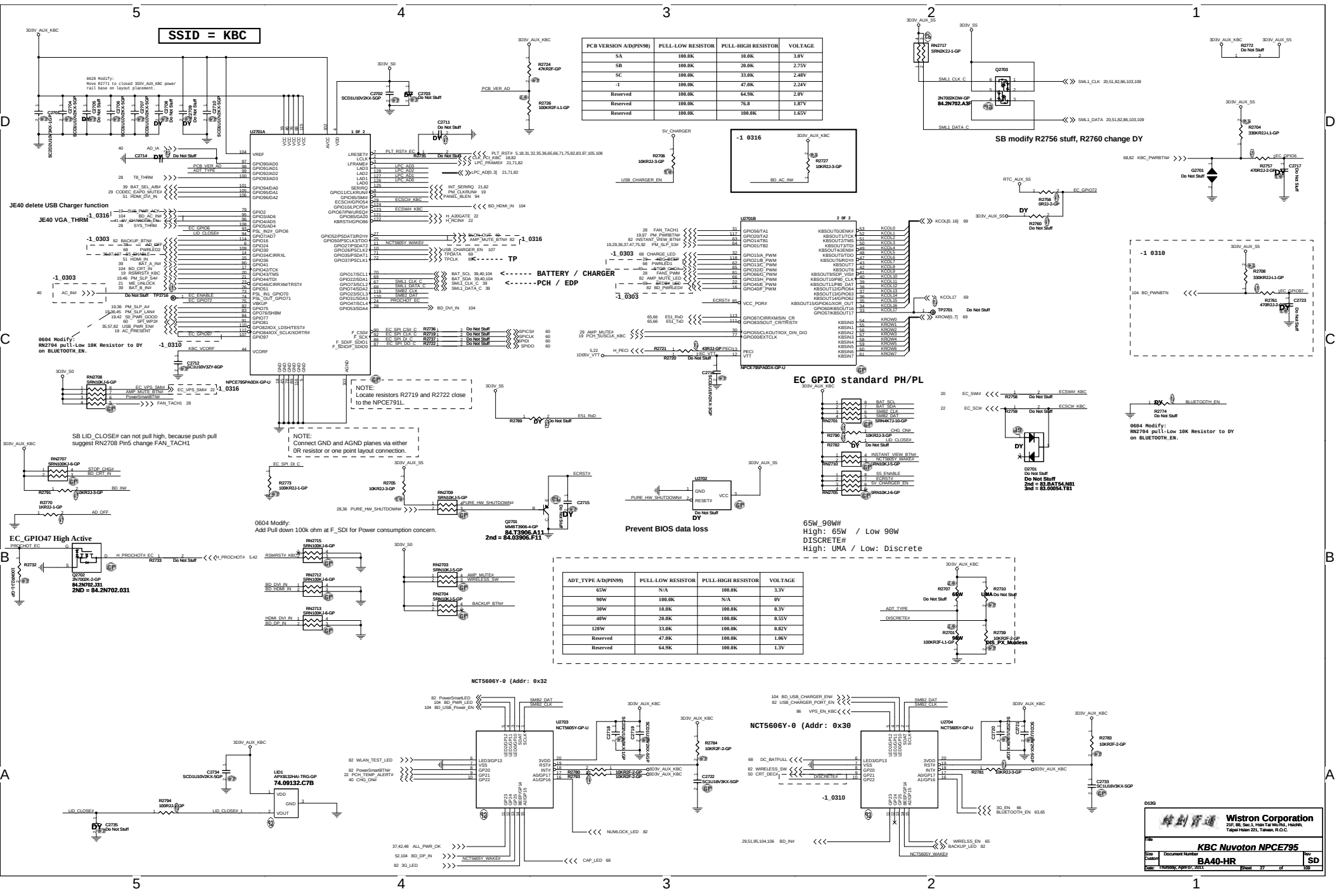
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Clock(colay)

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 26 of 109

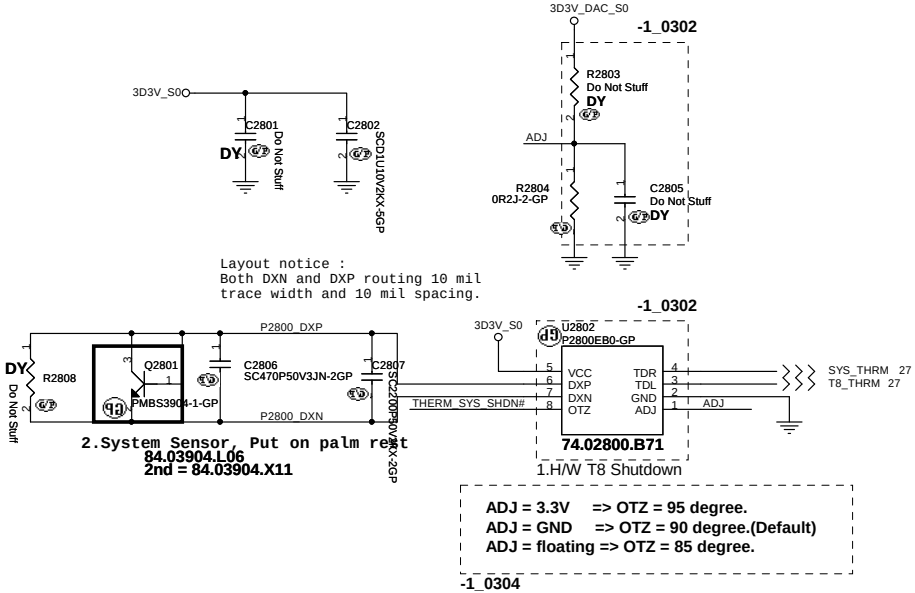


PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

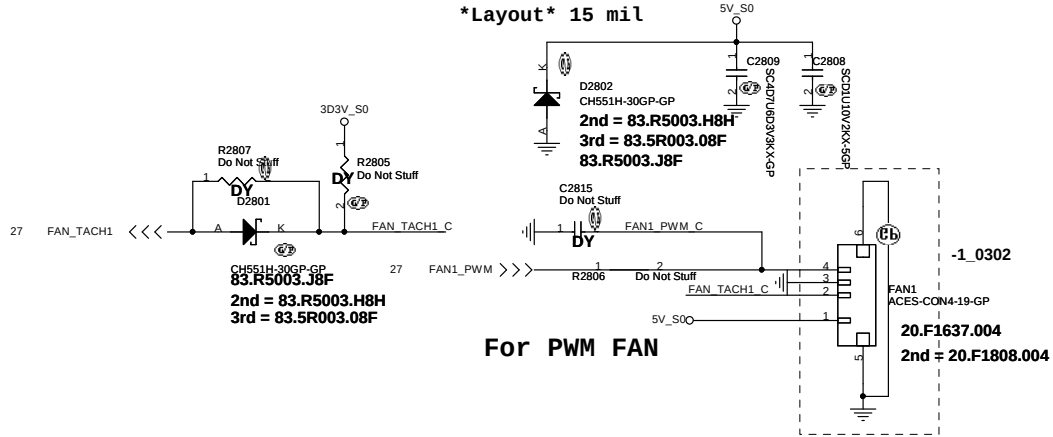
SSID = Thermal

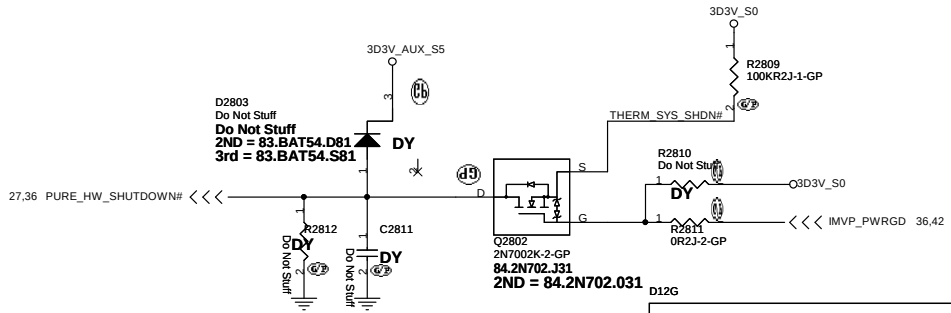
Thermal sensor P2800



Fan controller P2793

Layout 15 mil



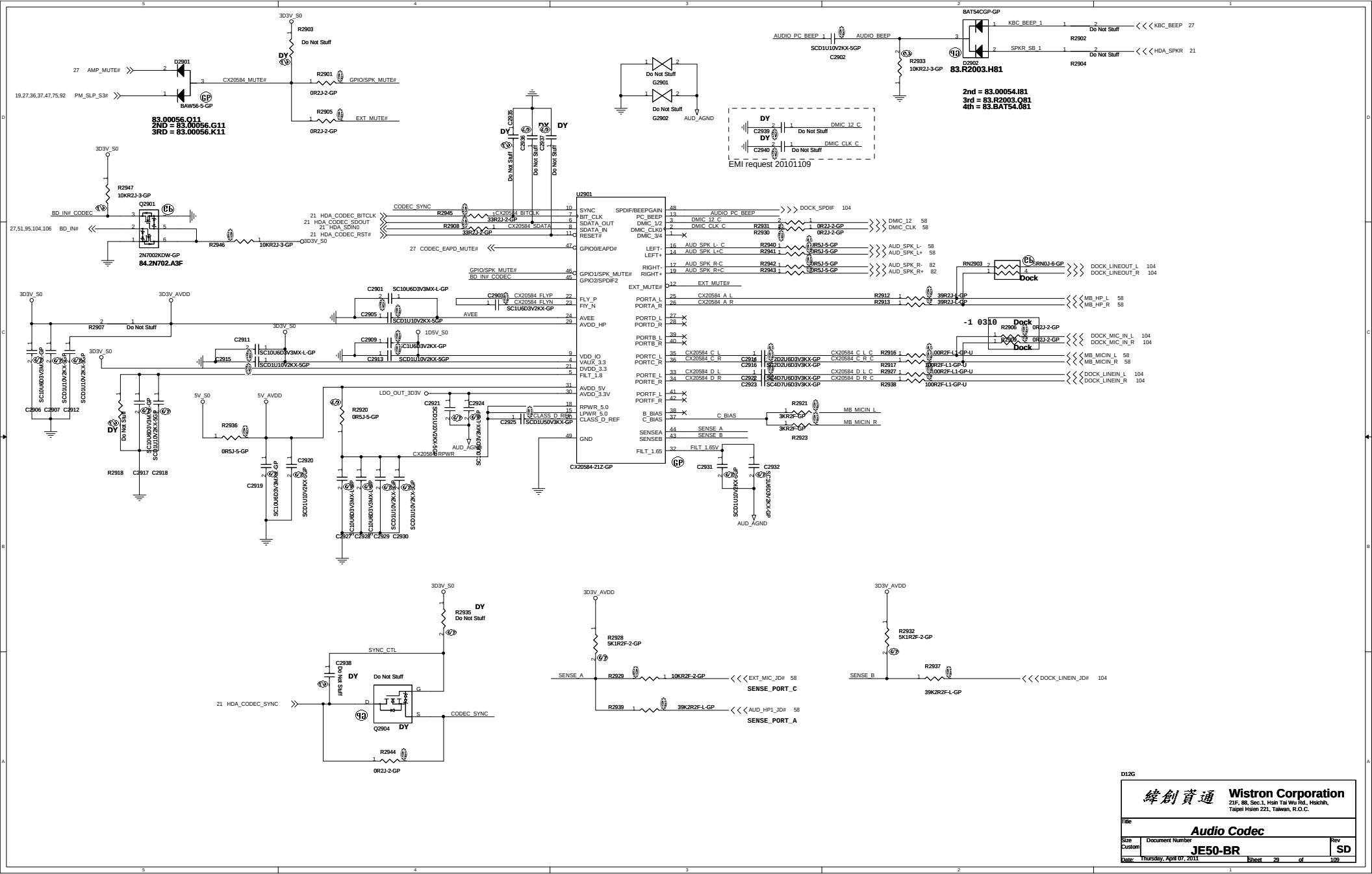


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 28 of 109



D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Audio Codec***	
Size: Custom	Document Number: **JE50-BR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 29 of 109	

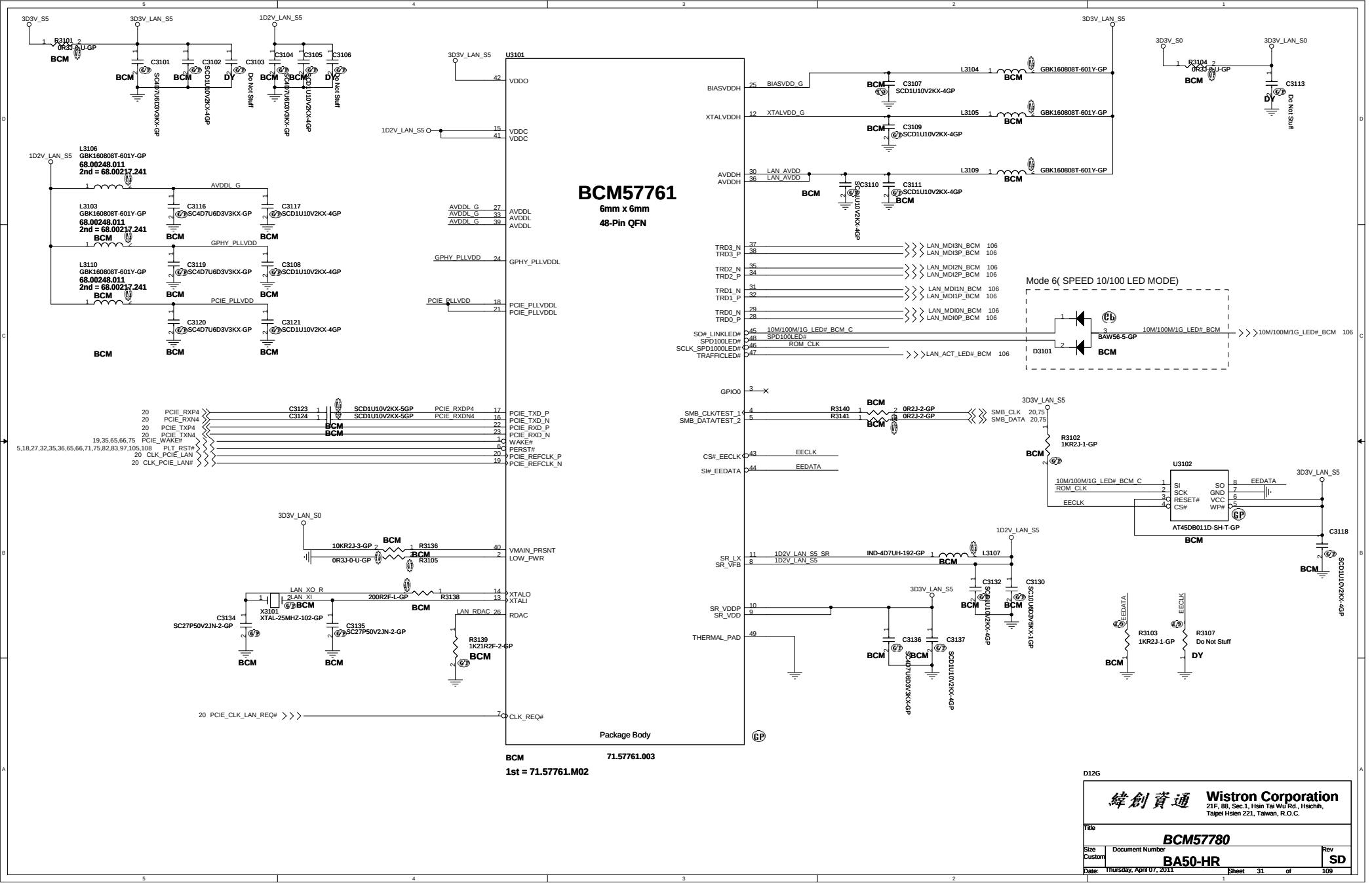
AUDIO OP AMPLIFIER

JE40 delete AMP function

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

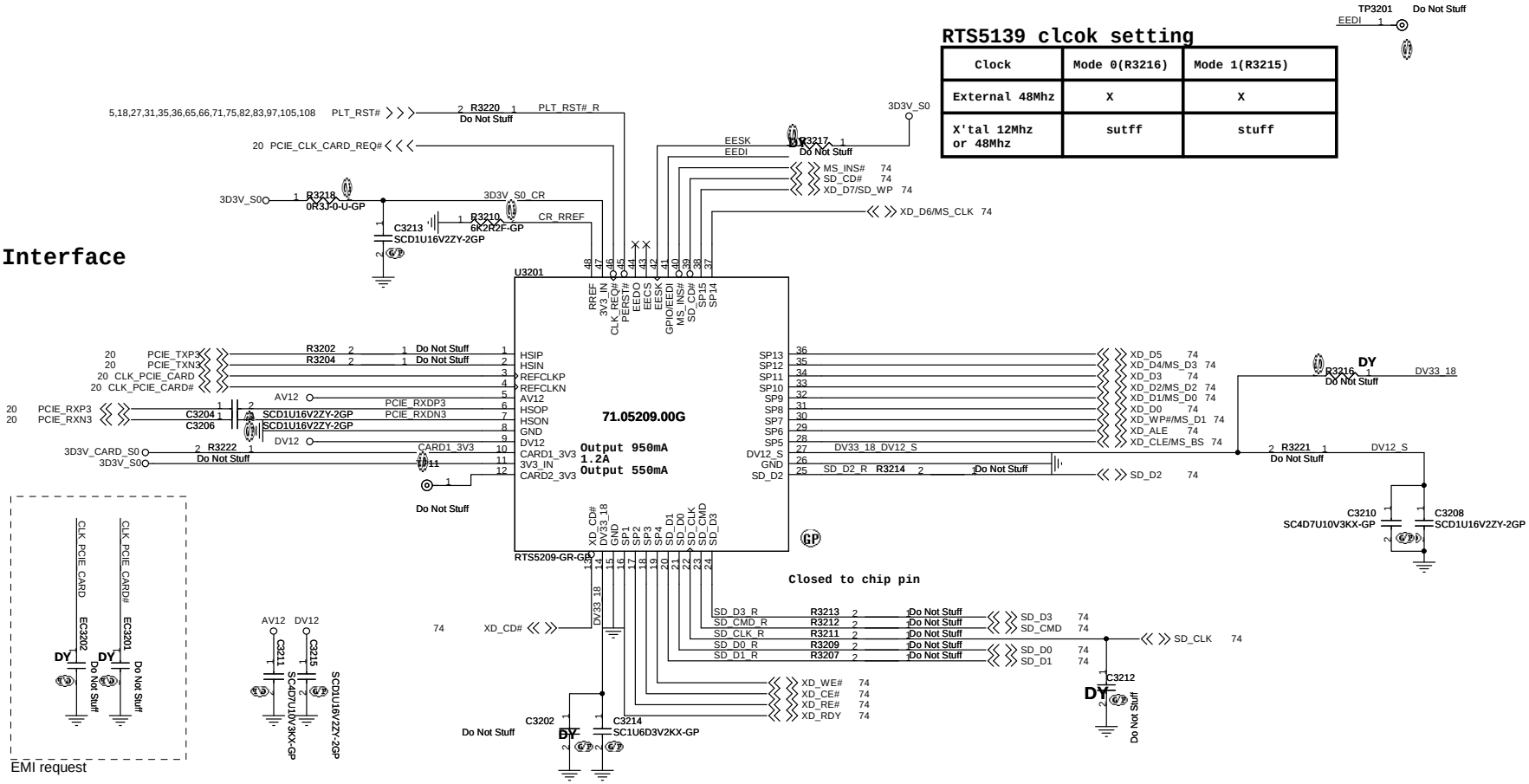
Title: *Audio AMP*		
Size: A4	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 30 of 109	


BCM57761
6mm x 6mm
48-Pin QFN
Package Body
BCM
71.57761.003
1st = 71.57761.M02
U3101
VDDO
VDDC
VDDC
AVDDL
AVDDL
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_PLLVDDL
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
CLK_REQ#
VMAIN_PRSNT
LOW_PWR
XTALO
XTALI
RDAC
BIASVDDD_G
XTALVDDD_G
LAN_AVDD
LAN_AVDD
LAN_MDI3N_BCM
LAN_MDI3P_BCM
LAN_MDI2N_BCM
LAN_MDI2P_BCM
LAN_MDI1N_BCM
LAN_MDI1P_BCM
LAN_MDI0N_BCM
LAN_MDI0P_BCM
10M/100M/1G_LED#_BCM_C
SPD100LED#
ROM_CLK
LAN_ACT_LED#_BCM
GPIO0
SMB_CLK
SMB_DATA
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
THERMAL_PAD
Mode 6(SPEED 10/100 LED MODE)
D3101
BAW56-5-GP
AT45DB011D-SH-T-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM57780
BA50-HR
SD
Thursday, April 07, 2011
Sheet 31 of 109

RTS5209==>PCI-E Interface

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	sutff	stuff



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTS5209(CARD READER)**

Size: A3 | Document Number: **BAD50-HR** | Rev: **SD**

Date: Thursday, April 07, 2011 | Sheet 32 of 109

(Blanking)

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 33 of 109

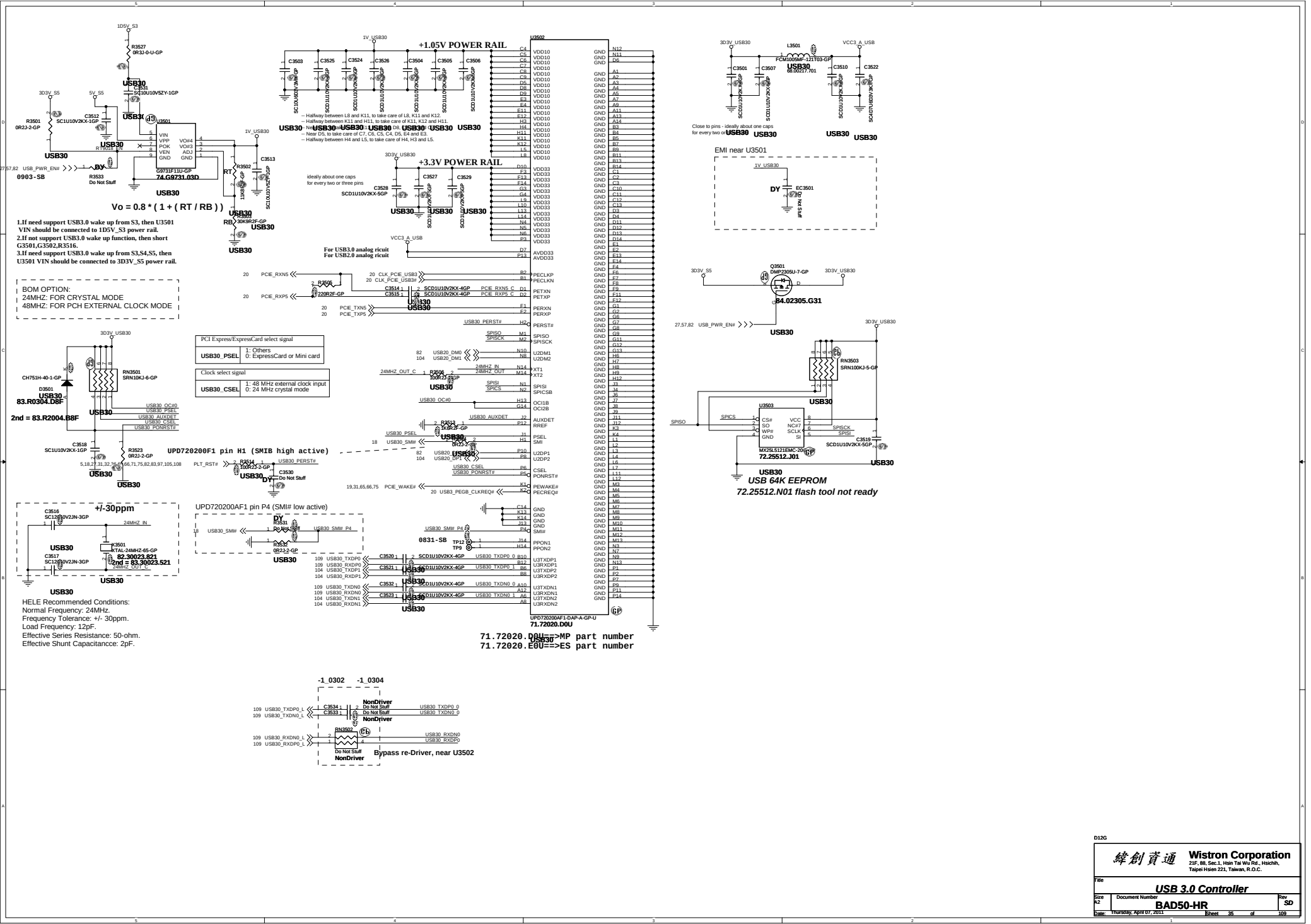
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BA40-HR	SD

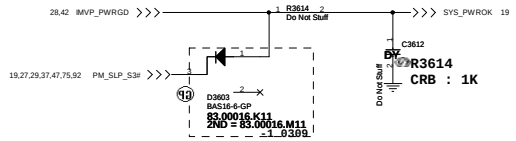
Date: Thursday, April 07, 2011 Sheet 34 of 109



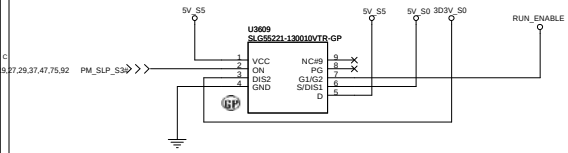
D12G

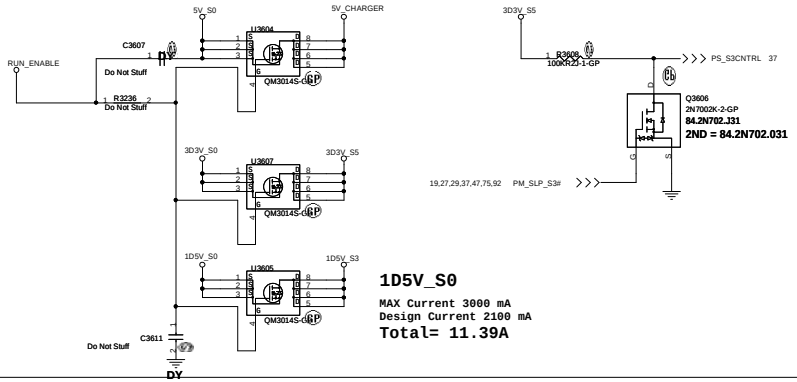
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB 3.0 Controller***
Size A2 / Document Number	**BAD50-HR** / Rev *SD*
Date: Thursday, April 07, 2011	Sheet 35 of 109

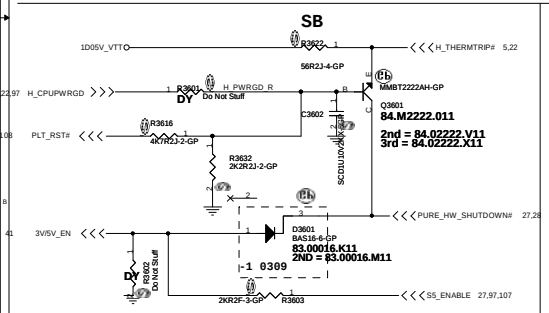
Power Sequence



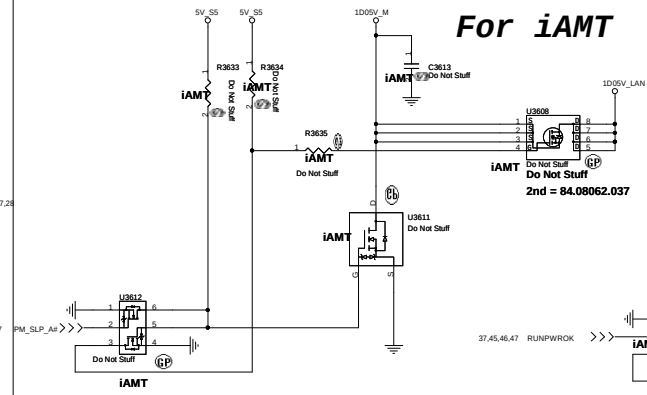
ANNIE Run Power

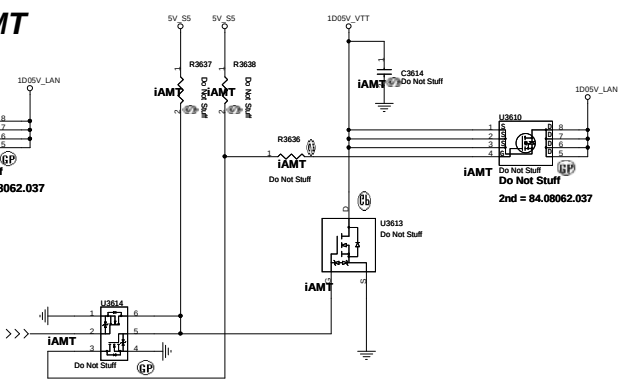


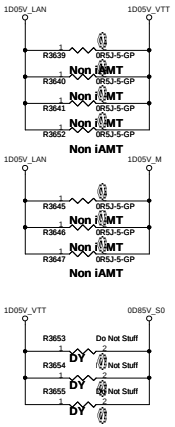


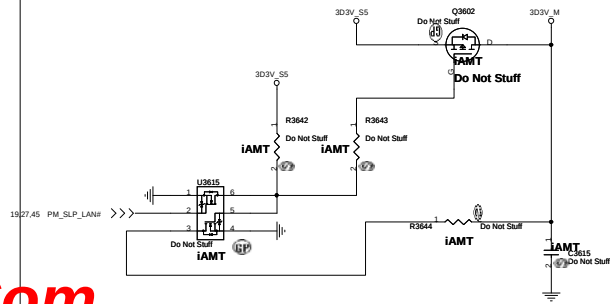


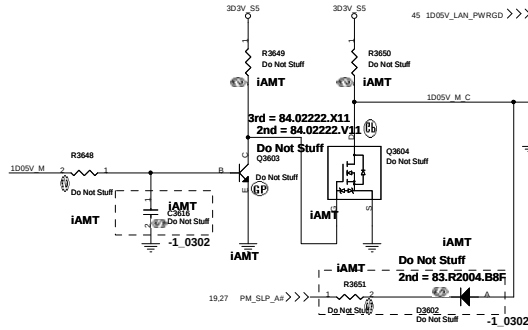
For iAMT







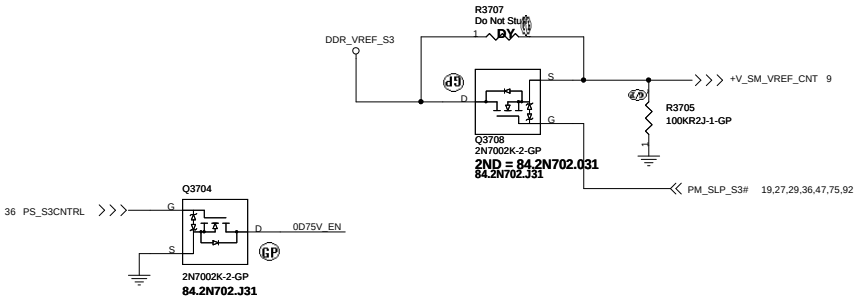




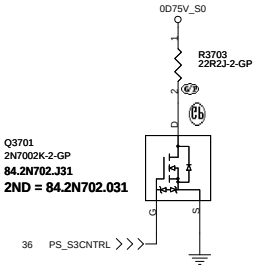
D12G

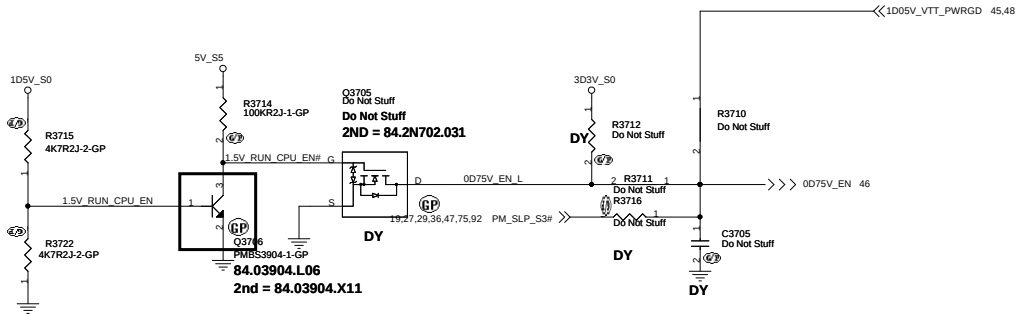
緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Power Plane Enable
Size A2	Document Number BA40-HR
Rev	SD
Date: Thursday, April 07, 2011	Sheet 36 of 109

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

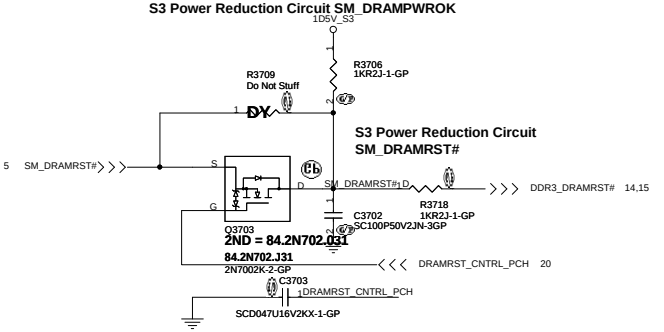


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

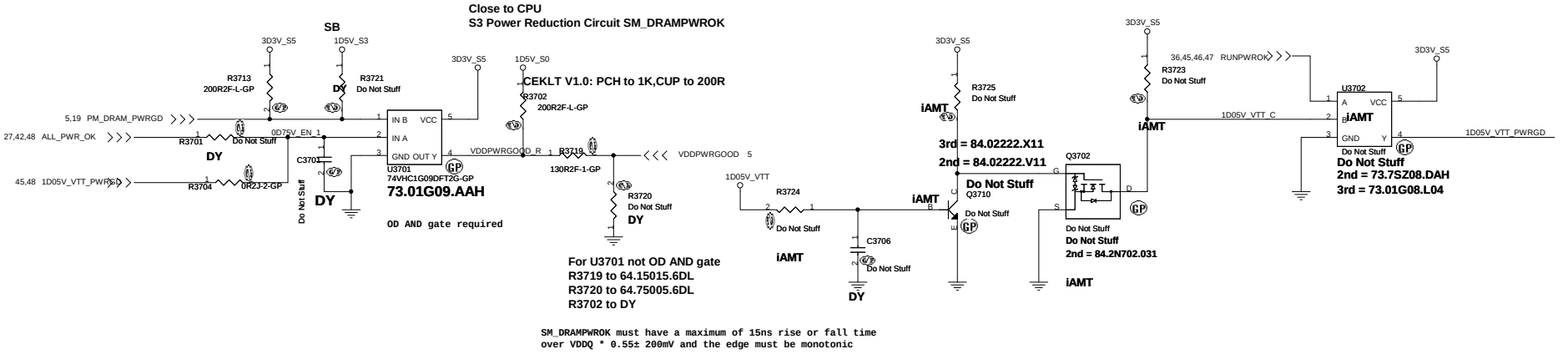




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size	Document Number	Rev
Custom	BA40-HR	SD

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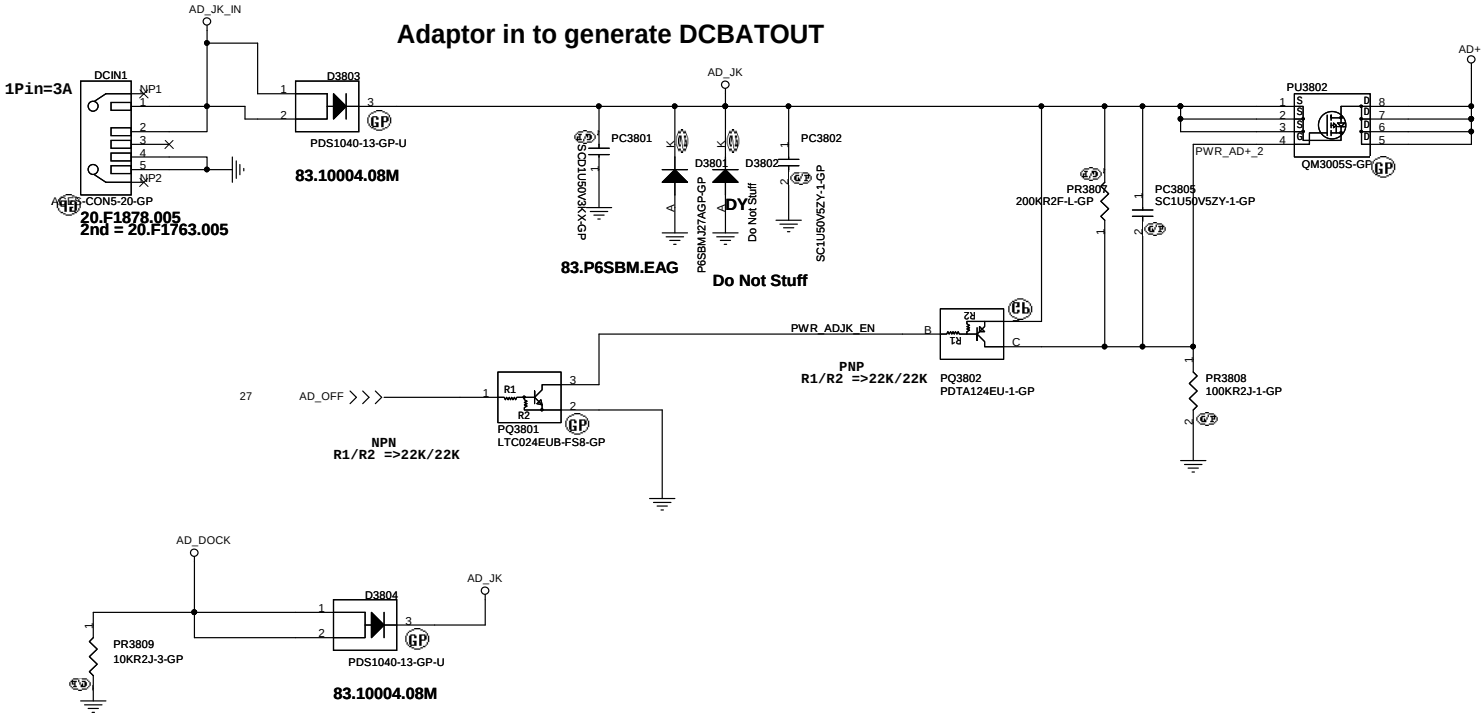
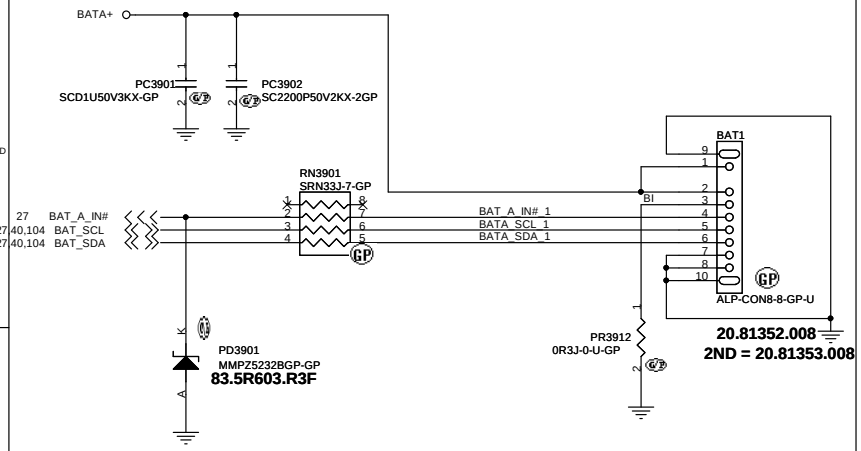
ANNIE solution



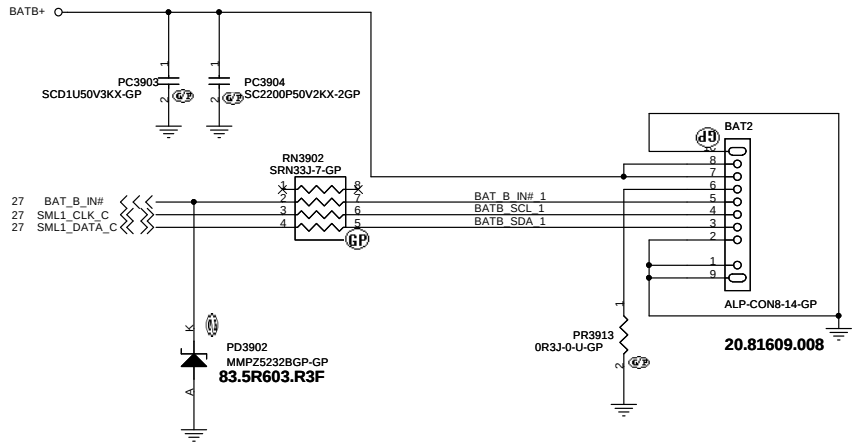
D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: A3	Document Number: BA40/50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 38 of 109	

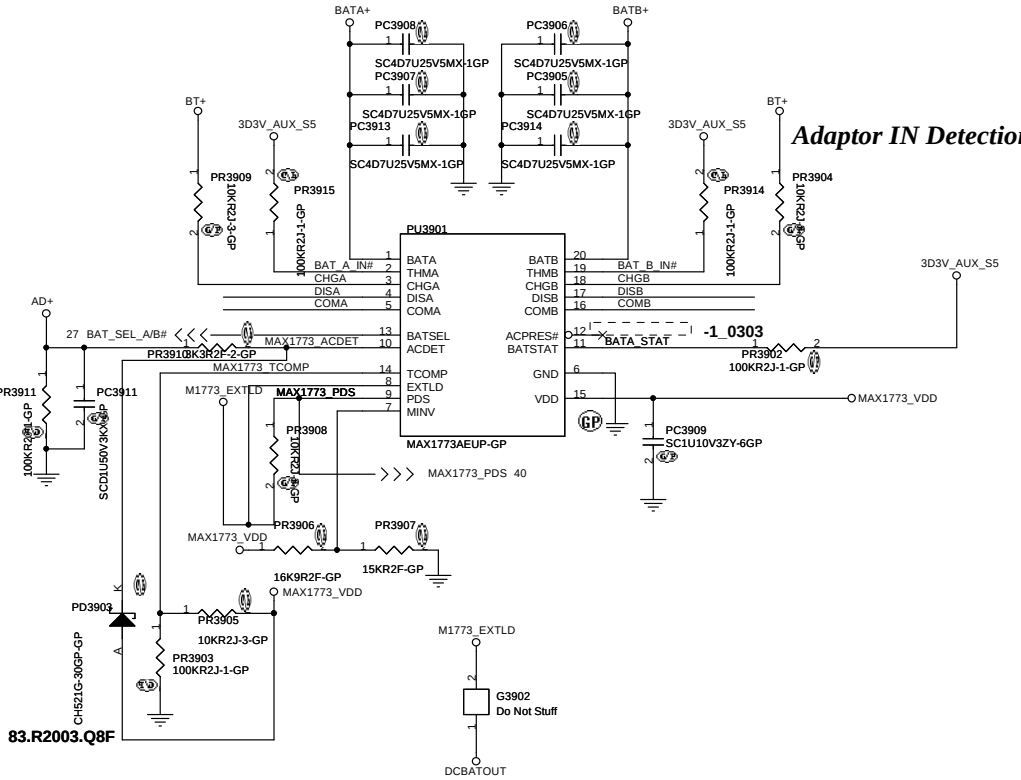
MAIN BATTERY CONNECTOR



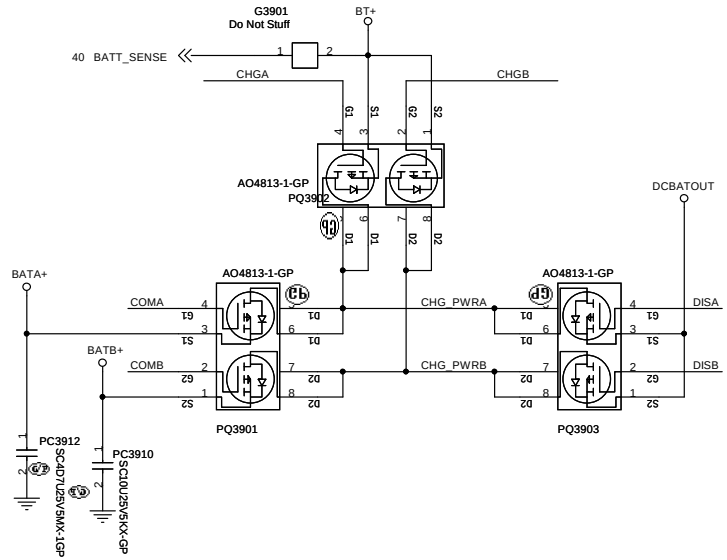
2nd BATTERY CONNECTOR



BATTERY SWITCH



Adaptor IN Detection



D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT_CONN***

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A3	BA40/50-HR	SD

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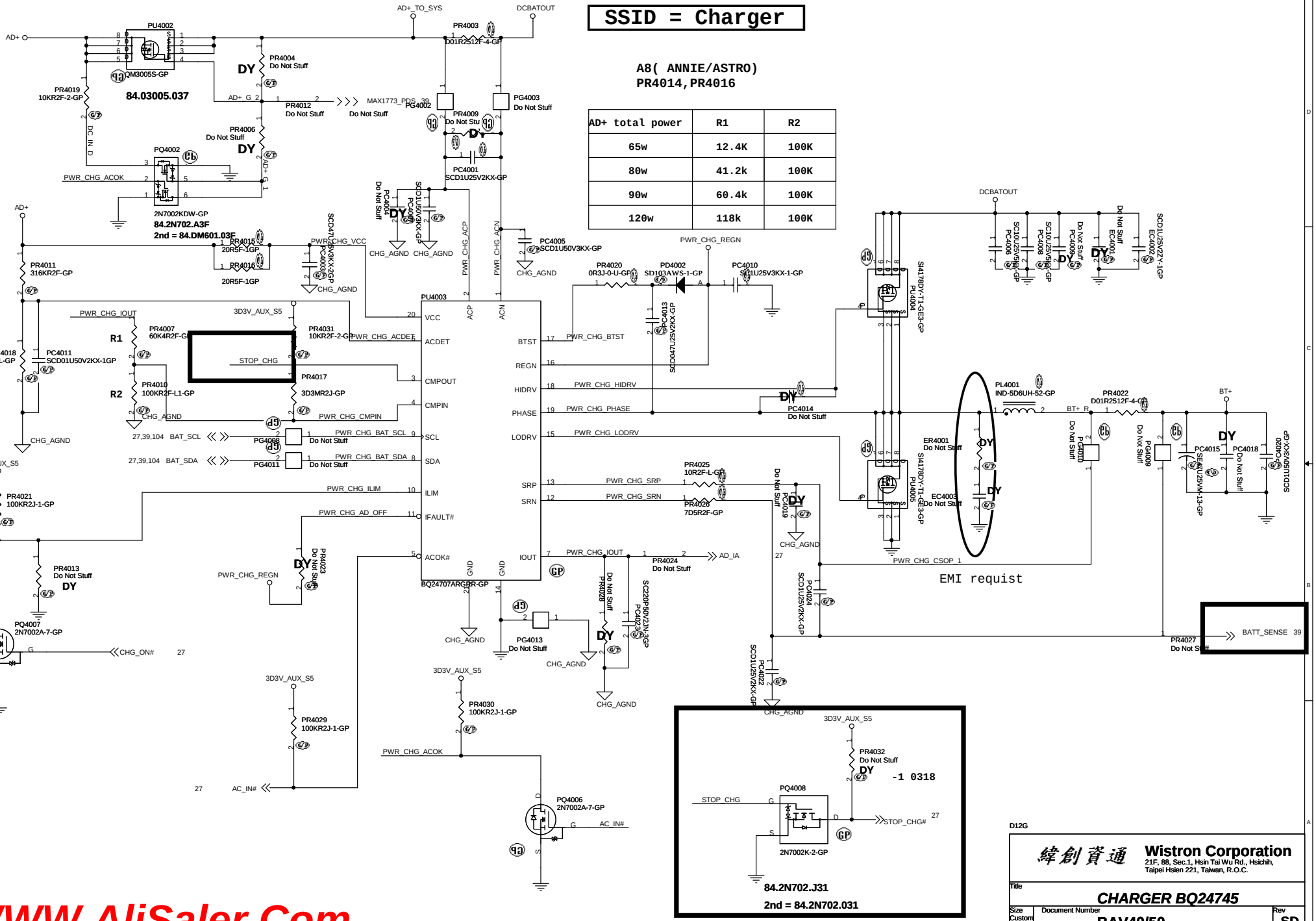
SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



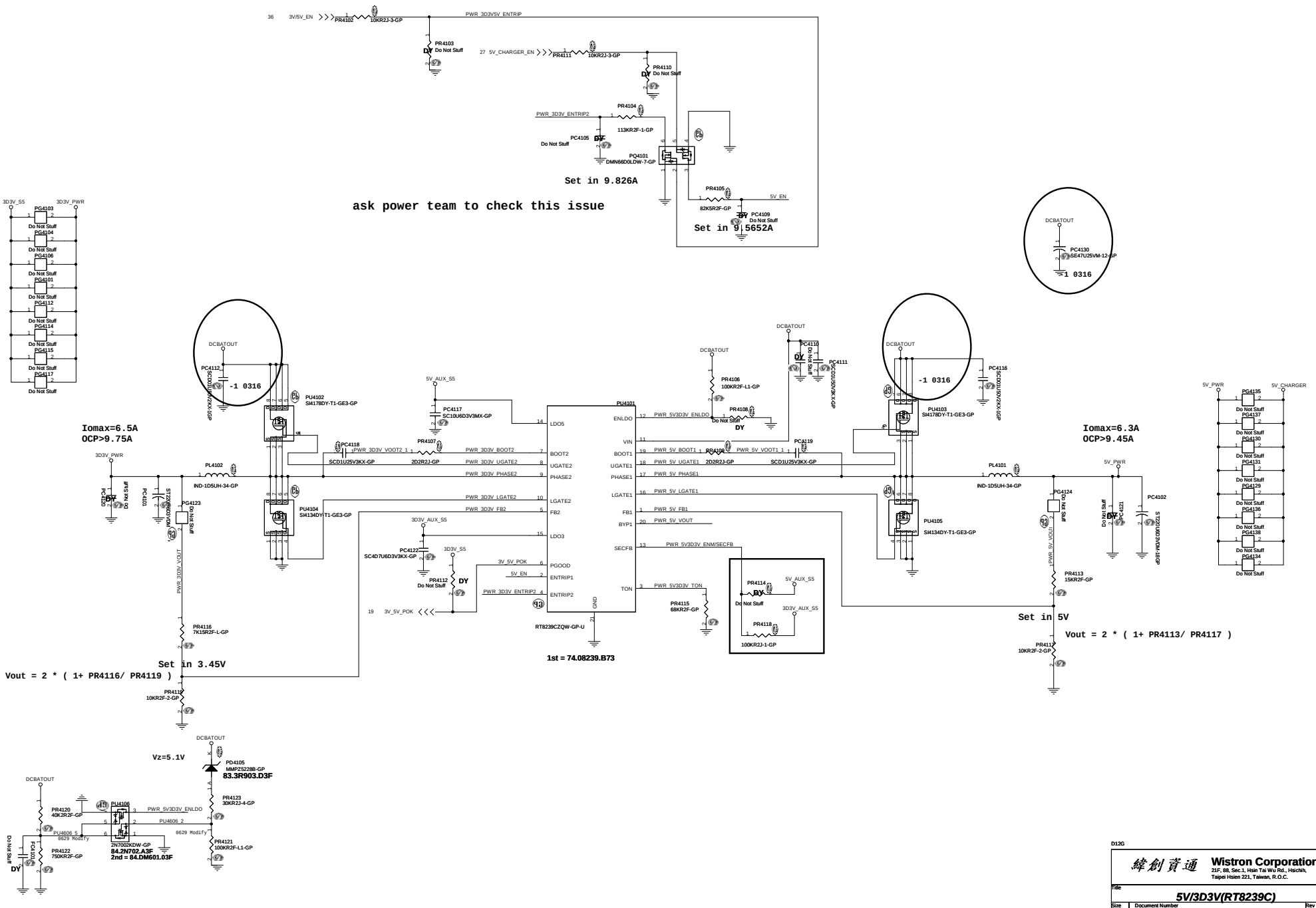
D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

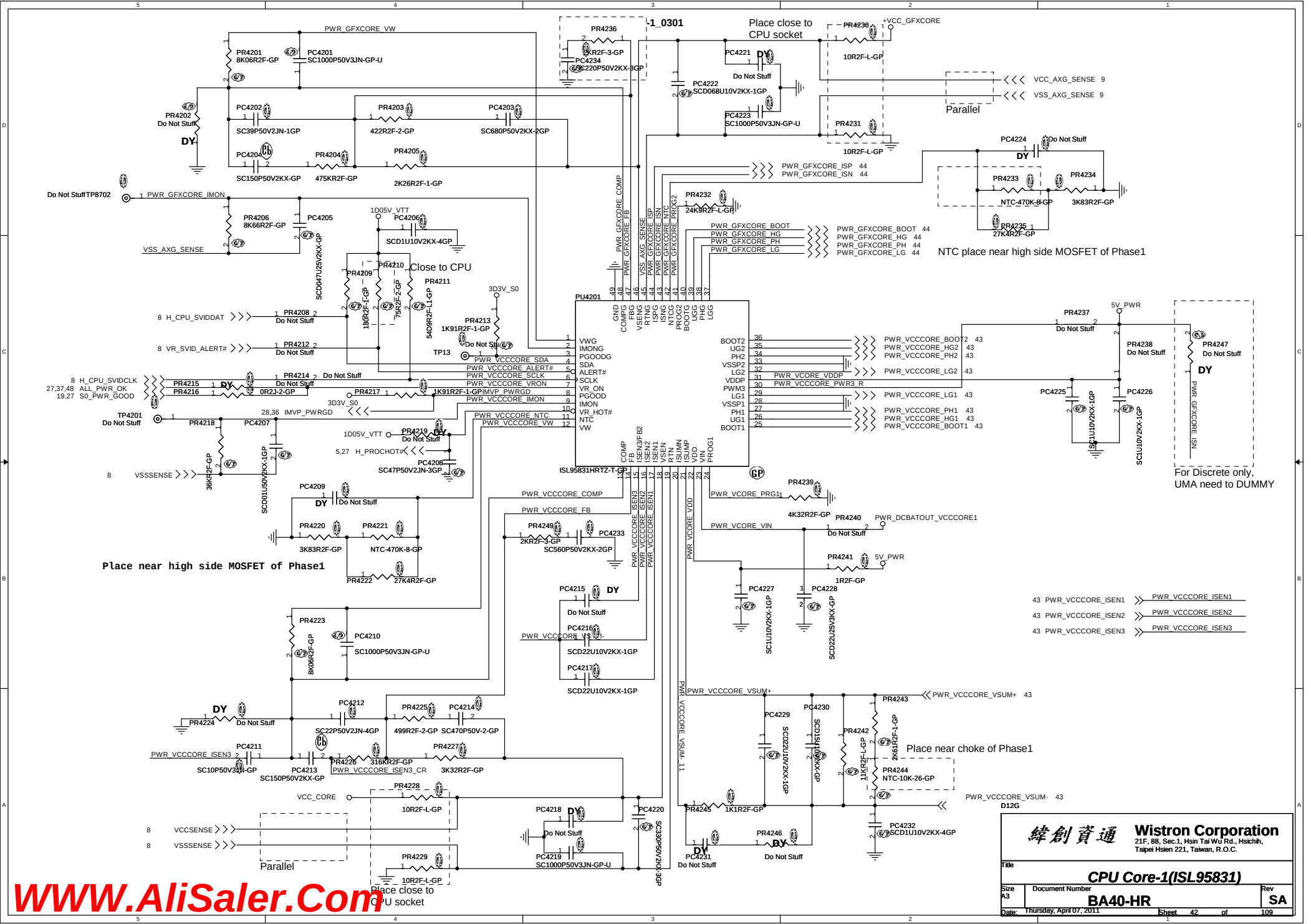
Size: Custom | Document Number: BAV40/50 | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 40 of 109

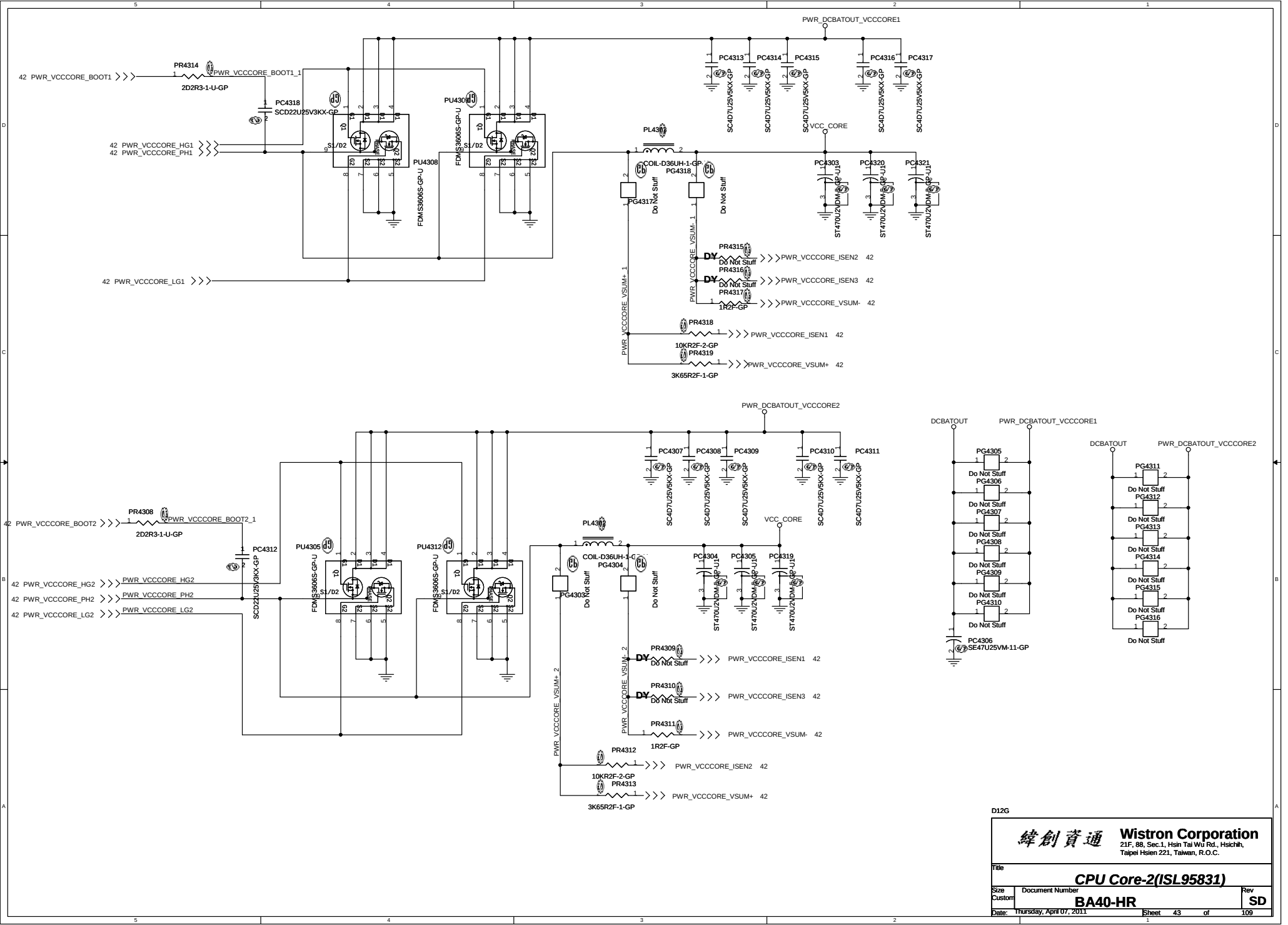


D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 5V/3D3V(RT8239C)		
Size: A2	Document Number: BAV40/50	Rev: SD
Date: Thursday, April 07, 2011	Sheet 41 of 109	



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU Core-1(ISL95831)
Size A3	Document Number BA40-HR
Rev	SA
Date: Thursday, April 07, 2011	Sheet 42 of 109



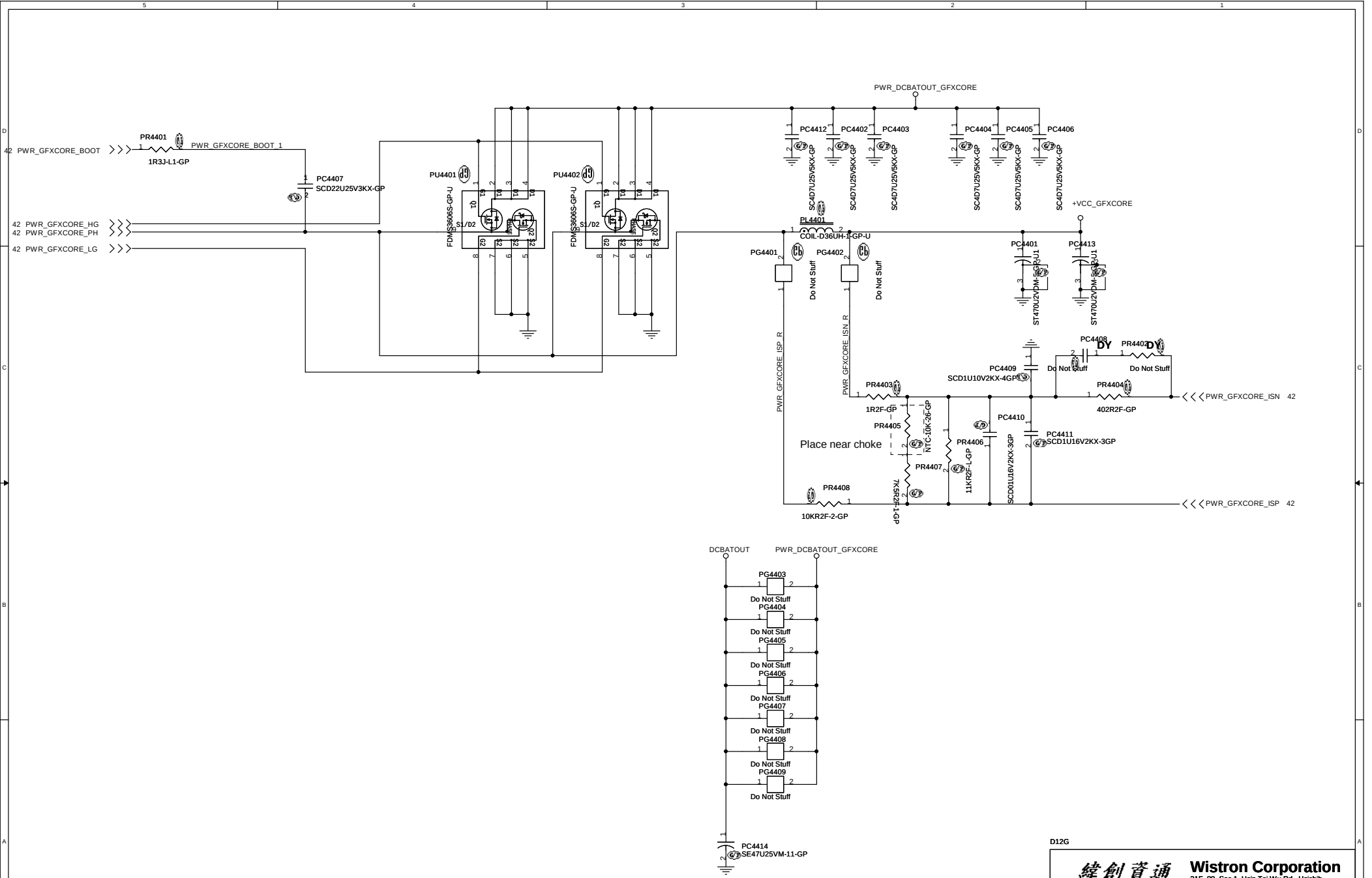
D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Core-2(ISL95831)***

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 43 of 109



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-3(ISL95831)

Size	Document Number	Rev
A3	BA40-HR	SD

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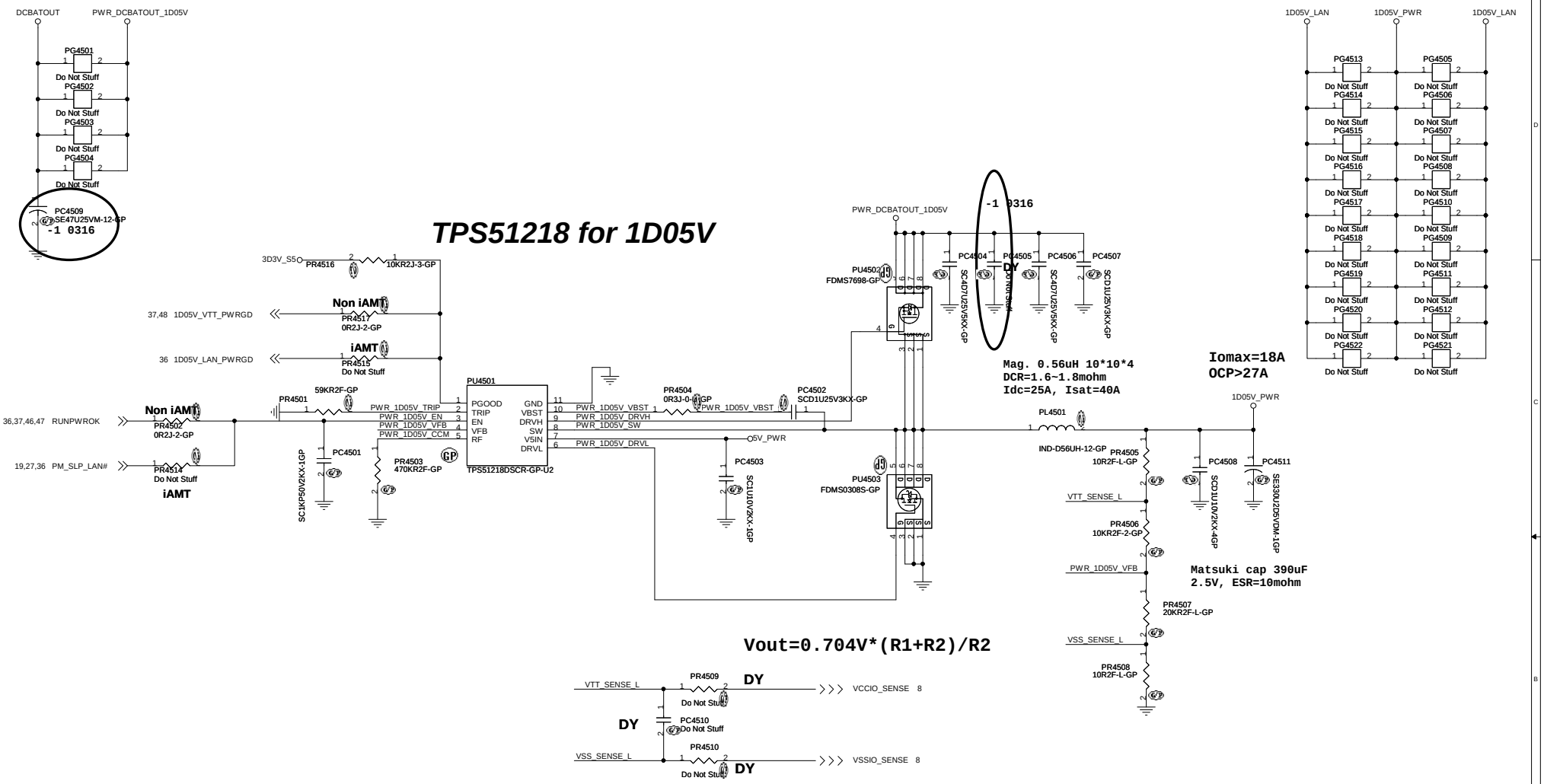
TPS51218 for 1D05V



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC to DC 1D05V(TPS51218D)***

Size	Document Number	Rev
Custom	BA40/50-HR	SD

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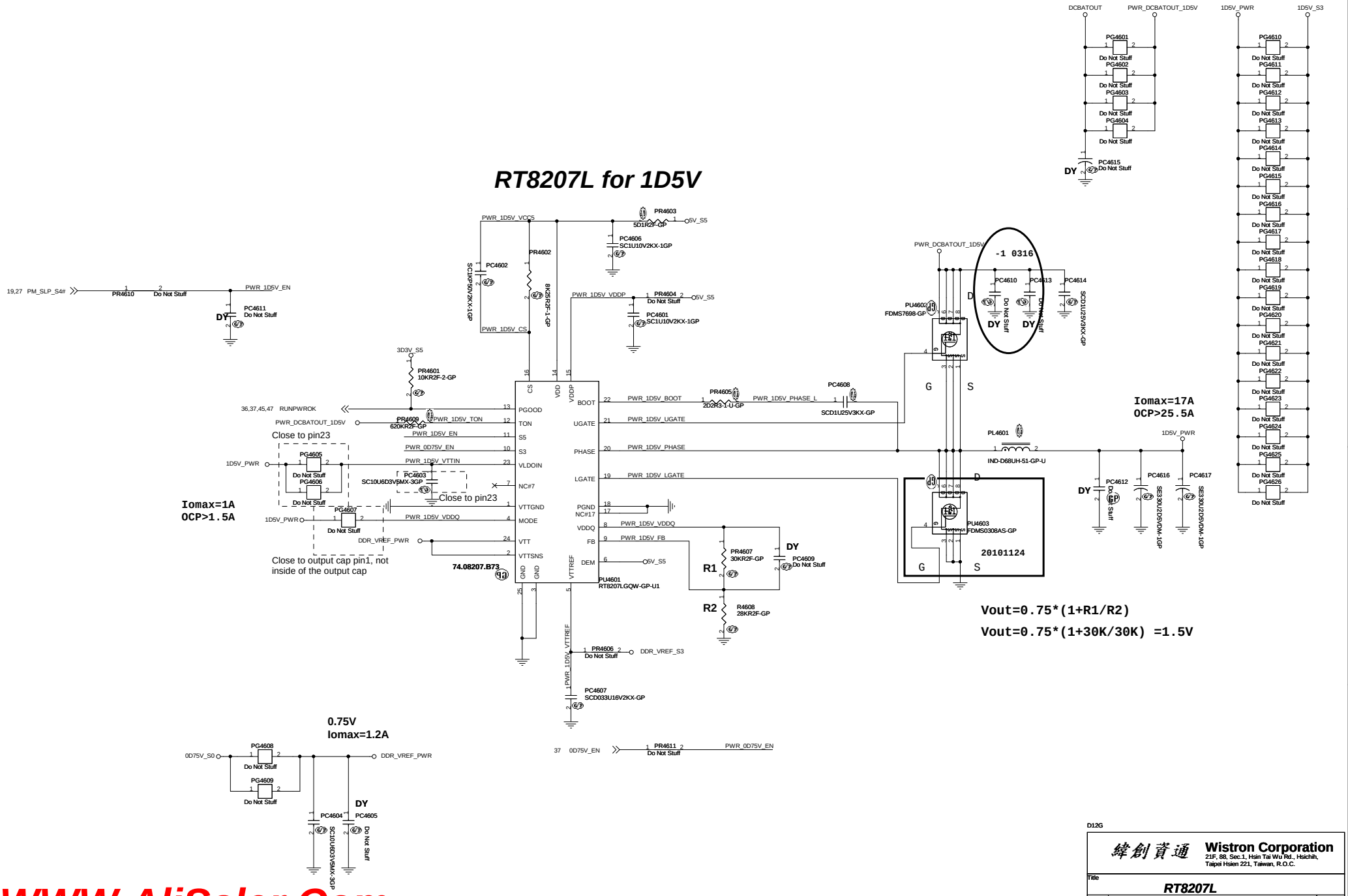
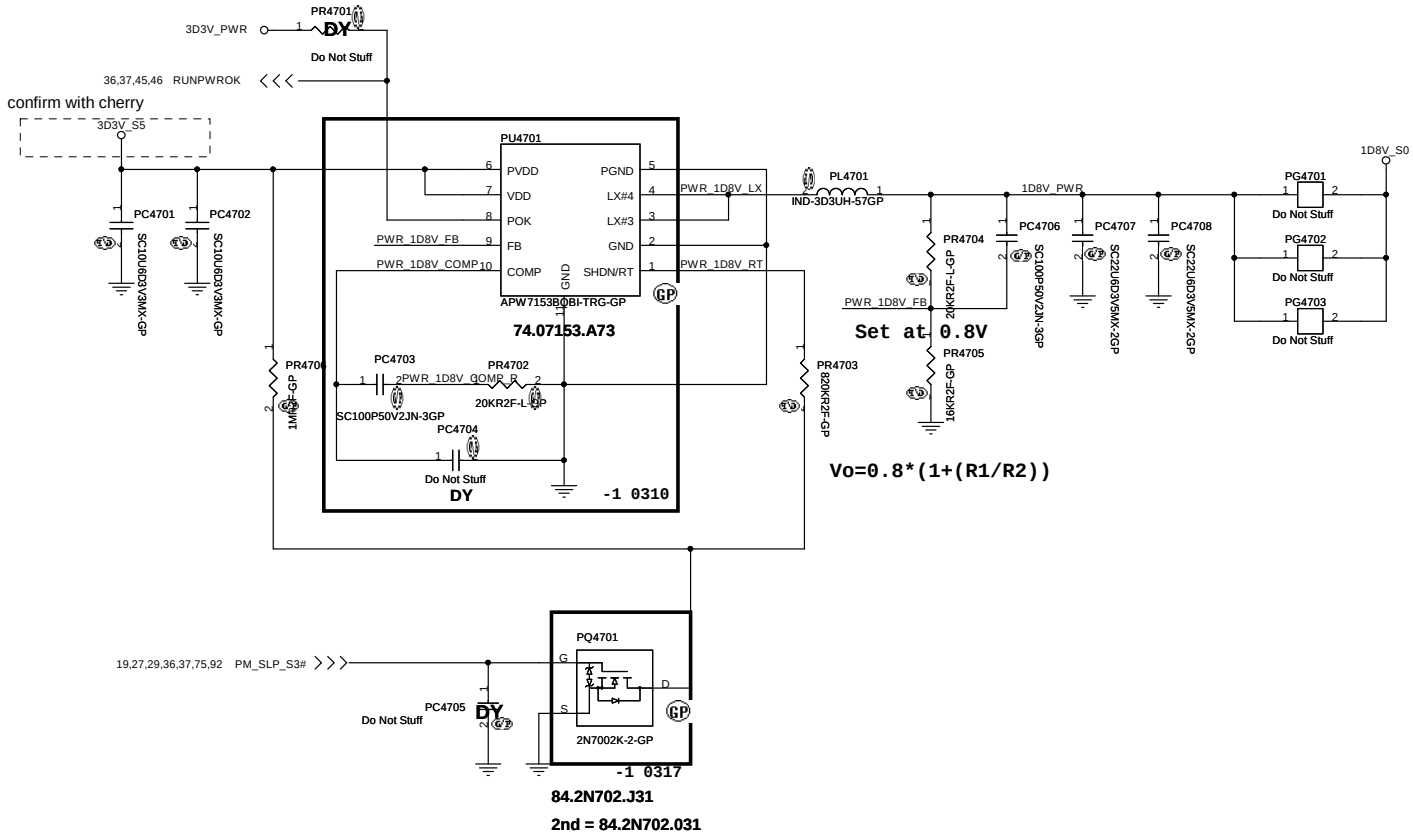
RT8207L for 1D5V



D12G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8207L	
Size: Custom	Document Number: BA40/50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 46 of 109	

RT8015B for 1D8V_S0



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO_1D8V(RT8015)*

Size	Document Number	Rev
A3	BA40/50-HR	SD

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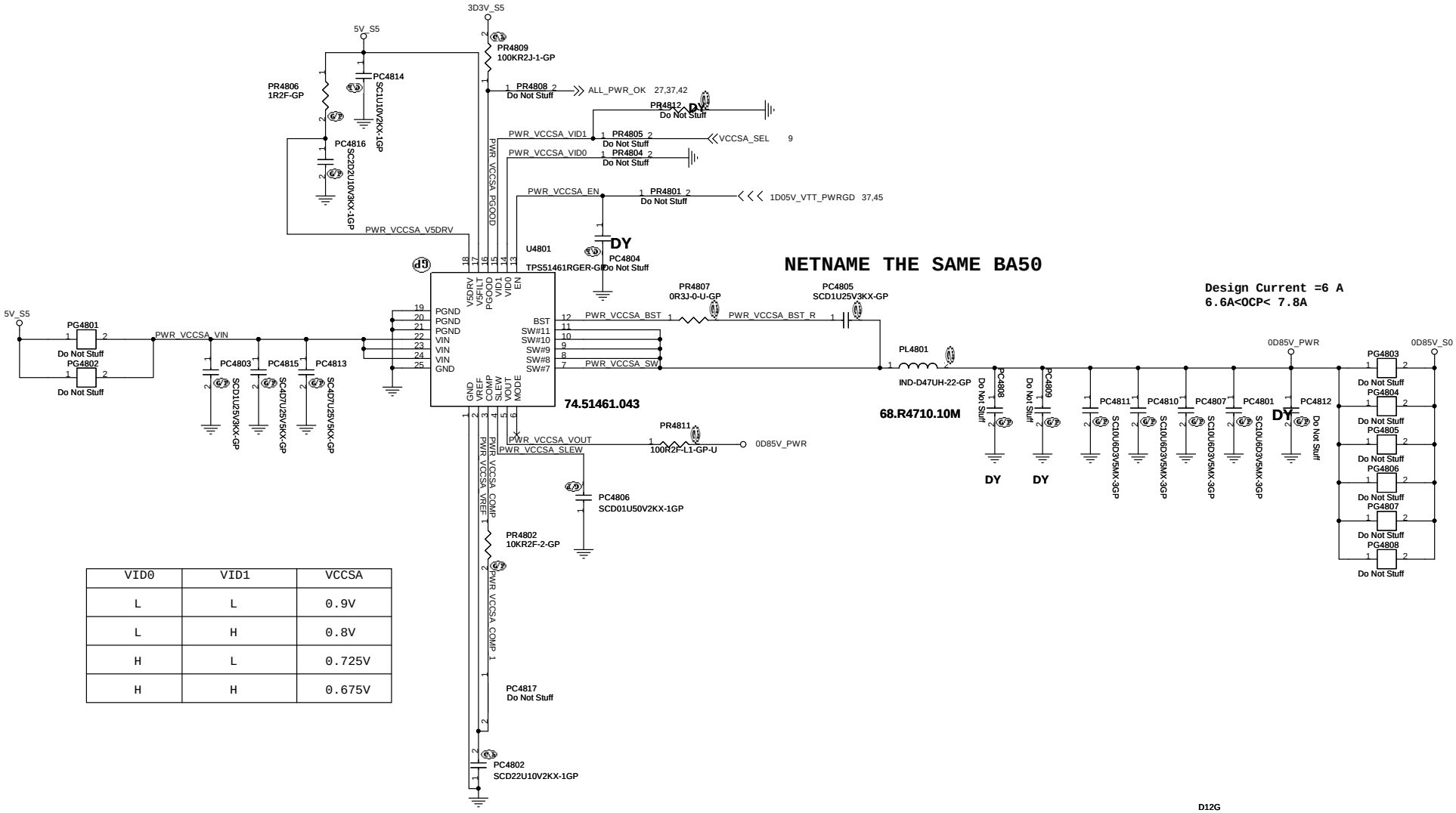
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO_VCCSA(APL5916)

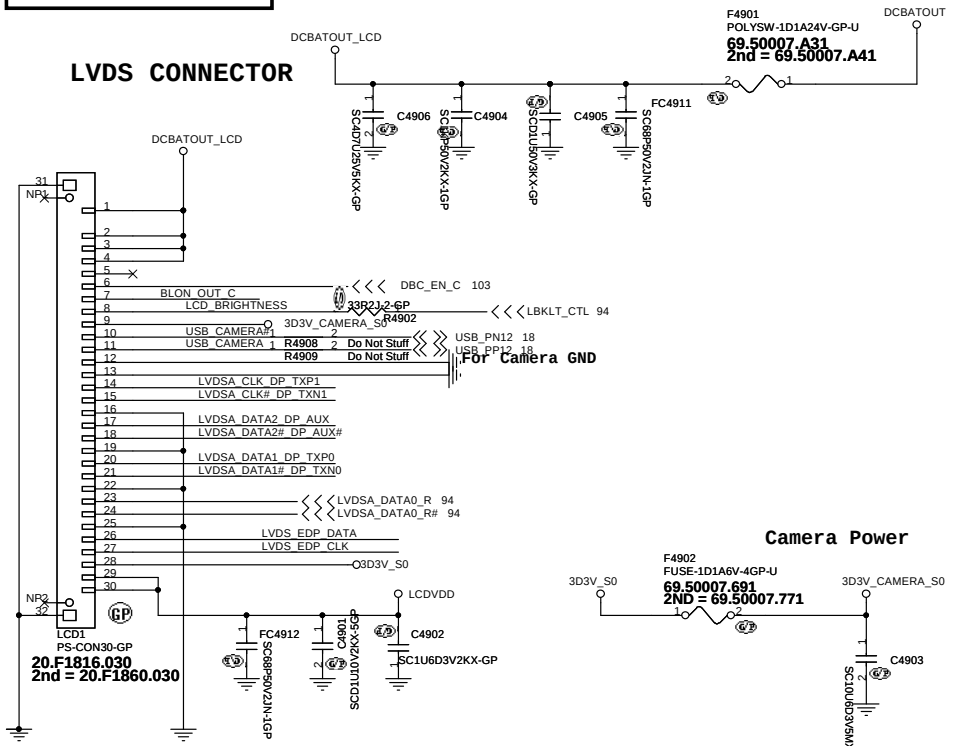
Size: A3 | Document Number: BA40/50-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 48 of 109

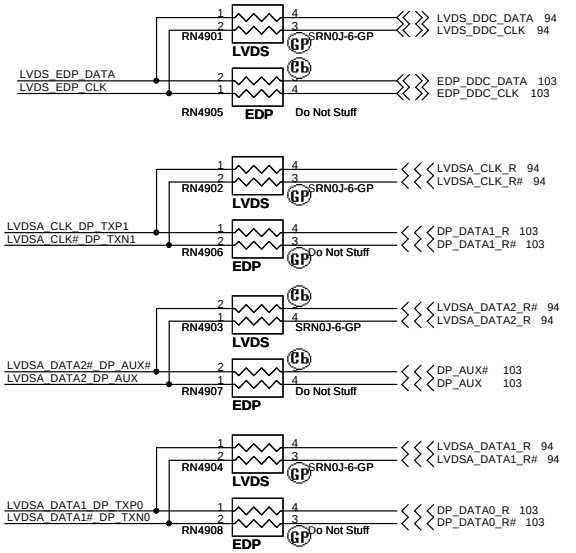
SSID = VIDEO

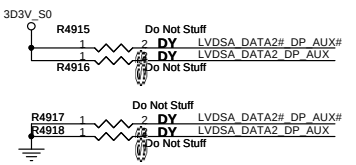
INVERTER POWER

LVDS CONNECTOR



Camera Power

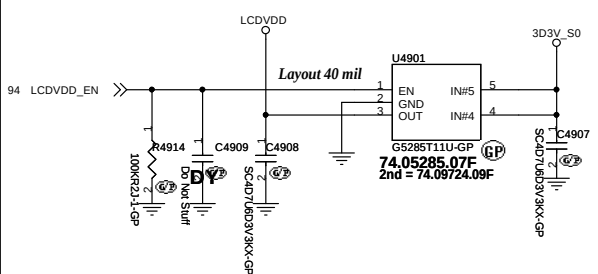




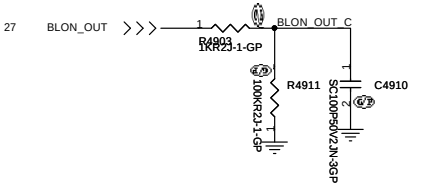
Close to LVDS connector

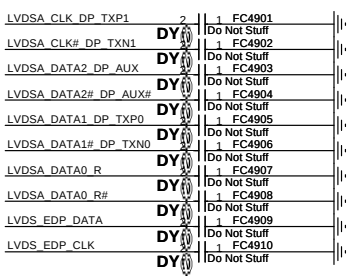
SSID = VIDEO

LCD POWER for ANNIE



-1 0310





D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size	Document Number	Rev
A3	BA40-HR	SD

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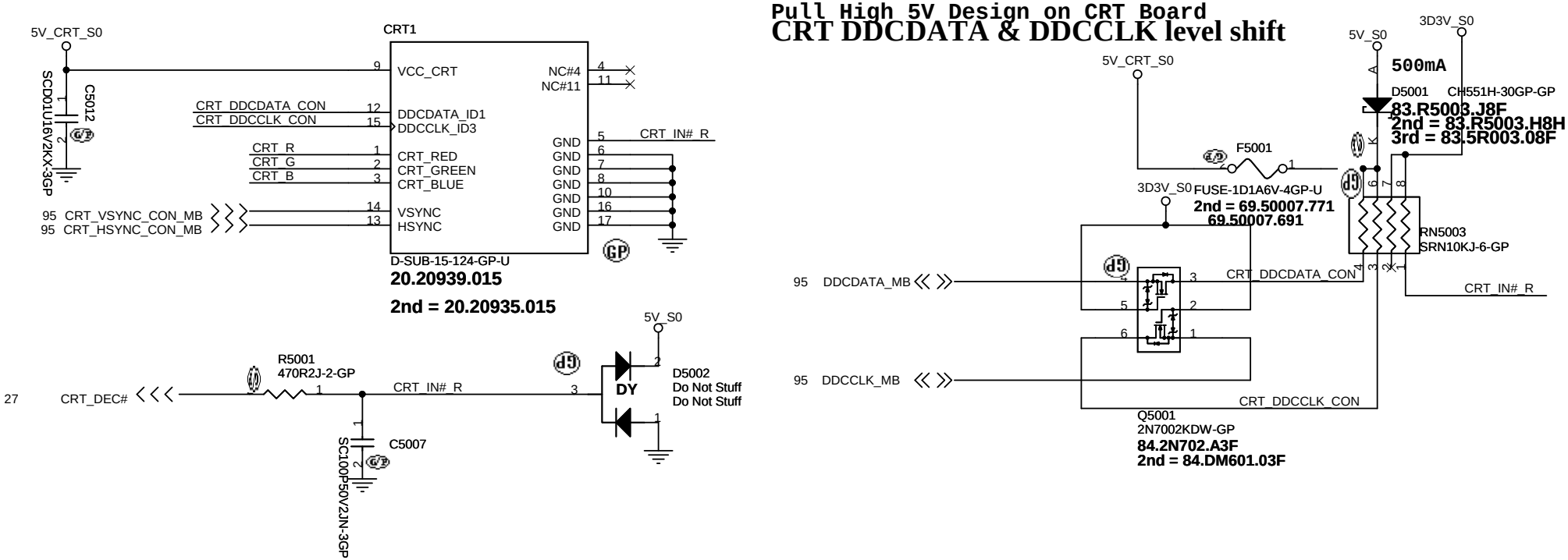
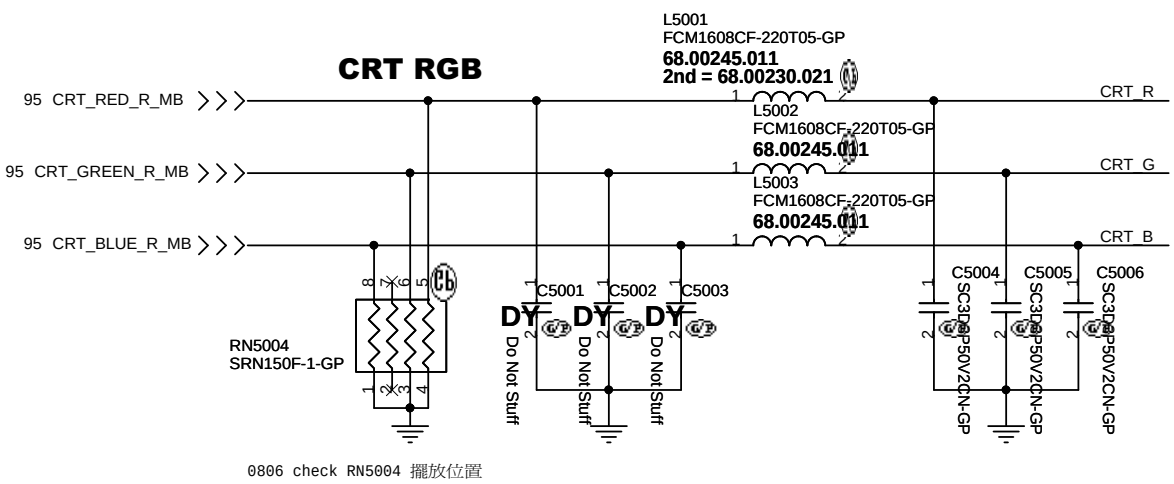
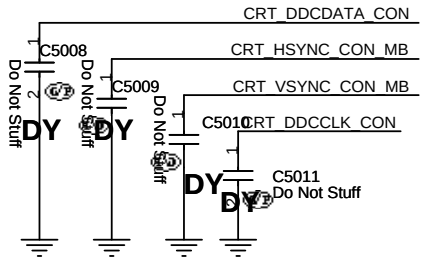
Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift



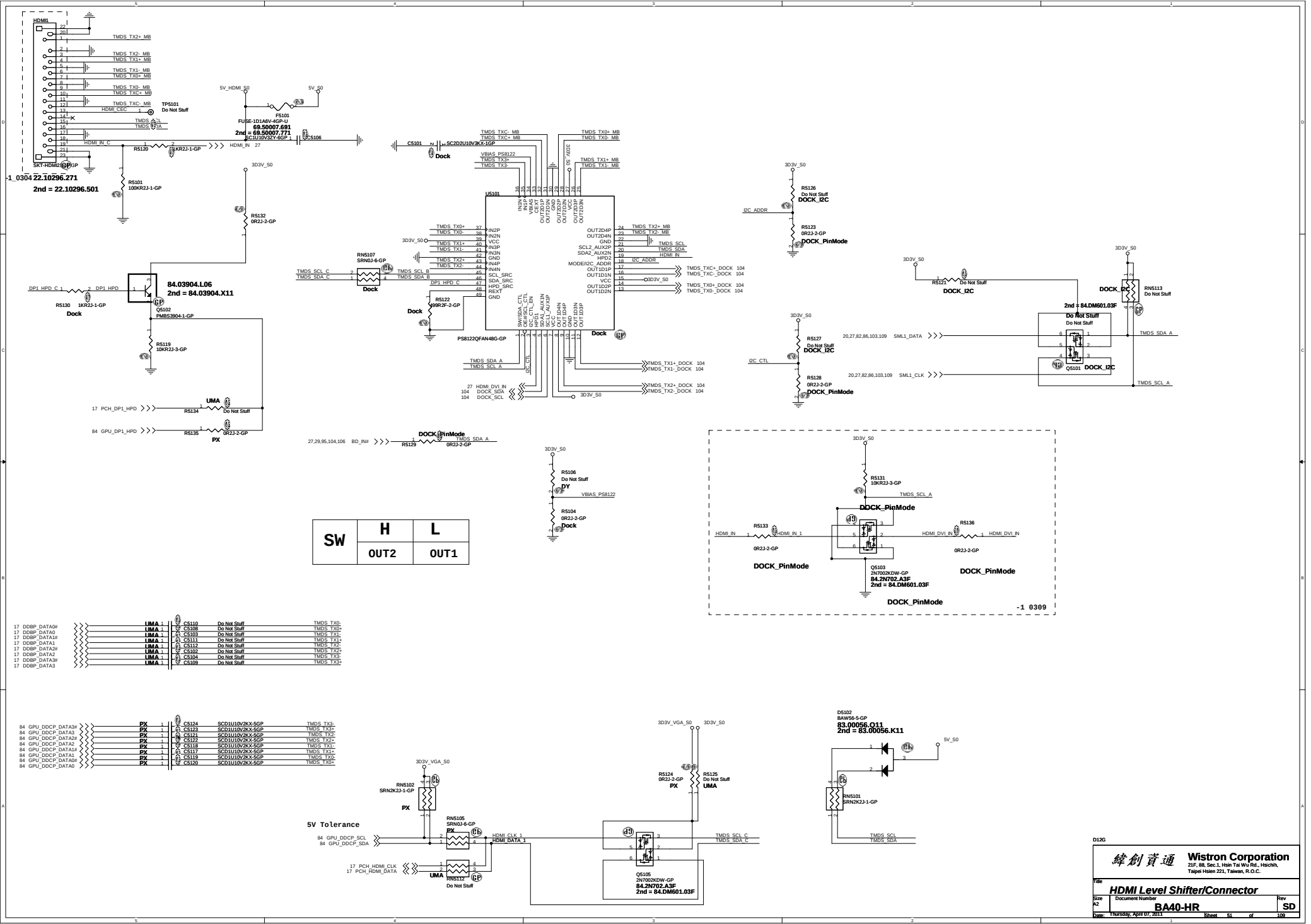


0806 check RN5004 擺放位置

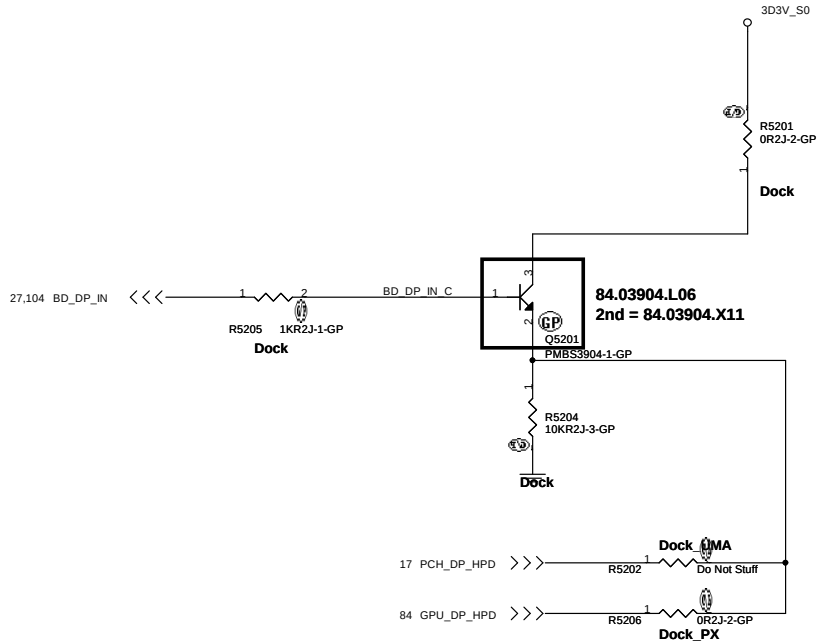


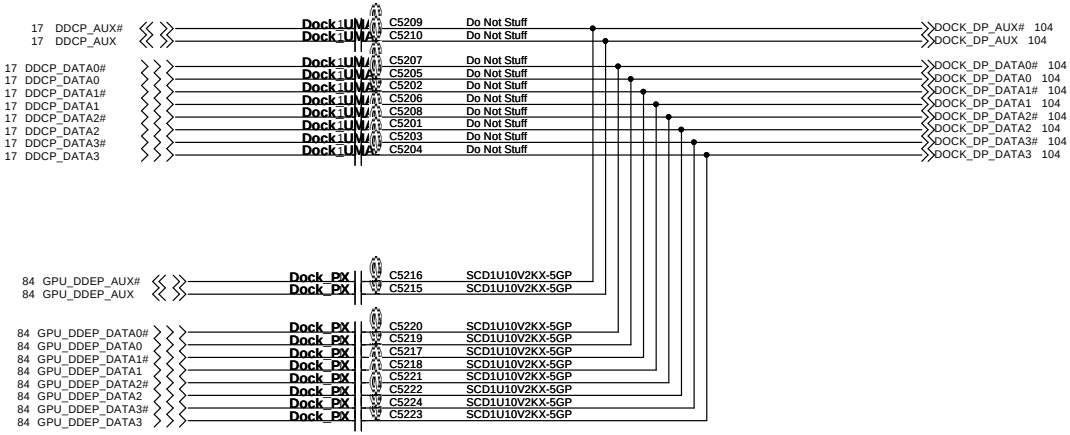
D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size A4	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 50 of 109	


HDMI
TMDS_TX2+ MB
TMDS_TX2- MB
TMDS_TX1+ MB
TMDS_TX1- MB
TMDS_TX0+ MB
TMDS_TX0- MB
TMDS_TXC+ MB
TMDS_TXC- MB
HDMI_CEC
TPS5101
Do Not Stuff
5V_HDMI_S0
5V_S0
F5101
FUSE-1D1A6V-XGP-U
69.50007.691
2nd = 69.50007.771
SC1U10V2ZY-4GP
VCS106
HDMI_IN_C
R5120
2K2R2J-1-GP
HDMI_IN 27
SKT-HDMI20-GP
-1_0304 22.10296.271
2nd = 22.10296.501
R5101
100KR2J-1-GP
3D3V_S0
R5132
0R2J-2-GP
DP1_HPD_C 1
DP1_HPD
R5130
1KR2J-1-GP
Dock
84.03904.L06
2nd = 84.03904.X11
Q5102
PMBS3904-1-GP
R5119
10KR2J-3-GP
17 PCH_DP1_HPD
UMA
R5134
Do Not Stuff
84 GPU_DP1_HPD
R5135
0R2J-2-GP
PX
C5101
SC2D2U10V3KX-1GP
Dock
VBIAS_PS8122
U5101
PS8122QFAN48G-GP
RN5107
SRN0J-6-GP
R5122
499R2F-2-GP
TMDS_SCL_C
TMDS_SDA_C
TMDS_SCL_B
TMDS_SDA_B
DP1_HPD_C
SW/SDA_CTL
OE#/SCL_CTL
I2C_CTL_EN
I2C_SEL
SDA1_AUX1N
SCL_AUX1P
VCC
OUT1D4N
GND
OUT1D3N
OUT1D3P
I2C_CTL
TMDS_SDA_A
TMDS_SCL_A
TMDS_TX1+_DOCK 104
TMDS_TX1-_DOCK 104
TMDS_TX2+_DOCK 104
TMDS_TX2-_DOCK 104
27 HDMI_DVI_IN
104 DOCK_SDA
104 DOCK_SCL
3D3V_S0
R5126
Do Not Stuff
DOCK_I2C
I2C_ADDR
R5123
0R2J-2-GP
DOCK_PinMode
R5127
Do Not Stuff
DOCK_I2C
I2C_CTL
R5128
0R2J-2-GP
DOCK_PinMode
20,27,82,86,103,109 SML1_DATA
20,27,82,86,103,109 SML1_CLK
R5122
Do Not Stuff
DOCK_I2C
RN5113
Do Not Stuff
2nd = 84.DM601.03F
Do Not Stuff
Q5101
DOCK_I2C
TMDS_SDA_A
TMDS_SCL_A
27,29,95,104,106 BD_IN#
R5129
0R2J-2-GP
DOCK_PinMode
R5106
Do Not Stuff
DY
R5104
0R2J-2-GP
Dock
VBIAS_PS8122
SW
H
L
OUT2
OUT1
R5131
10KR2J-3-GP
DOCK_PinMode
R5133
0R2J-2-GP
R5136
0R2J-2-GP
HDMI_IN
HDMI_IN_1
HDMI_DVI_IN
HDMI_DVI_IN
Q5103
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
DOCK_PinMode
DOCK_PinMode
DOCK_PinMode
-1 0309
17 DDBP_DATA0#
17 DDBP_DATA0
17 DDBP_DATA1#
17 DDBP_DATA1
17 DDBP_DATA2#
17 DDBP_DATA2
17 DDBP_DATA3#
17 DDBP_DATA3
UMA
C5110 Do Not Stuff TMDS_TX0-
C5108 Do Not Stuff TMDS_TX0+
C5103 Do Not Stuff TMDS_TX1-
C5111 Do Not Stuff TMDS_TX1+
C5112 Do Not Stuff TMDS_TX2-
C5102 Do Not Stuff TMDS_TX2+
C5104 Do Not Stuff TMDS_TX3-
C5109 Do Not Stuff TMDS_TX3+
84 GPU_DDCP_DATA3#
84 GPU_DDCP_DATA3
84 GPU_DDCP_DATA2#
84 GPU_DDCP_DATA2
84 GPU_DDCP_DATA1#
84 GPU_DDCP_DATA1
84 GPU_DDCP_DATA0#
84 GPU_DDCP_DATA0
PX
C5124 SCD1U10V2KX-5GP TMDS_TX3-
C5123 SCD1U10V2KX-5GP TMDS_TX3+
C5121 SCD1U10V2KX-5GP TMDS_TX2-
C5122 SCD1U10V2KX-5GP TMDS_TX2+
C5118 SCD1U10V2KX-5GP TMDS_TX1-
C5117 SCD1U10V2KX-5GP TMDS_TX1+
C5119 SCD1U10V2KX-5GP TMDS_TX0-
C5120 SCD1U10V2KX-5GP TMDS_TX0+
3D3V_VGA_S0
RN5102
SRN2K2J-1-GP
PX
5V Tolerance
RN5105
SRN0J-6-GP
PX
84 GPU_DDCP_SCL
84 GPU_DDCP_SDA
HDMI_CLK_1
HDMI_DATA_1
17 PCH_HDMI_CLK
17 PCH_HDMI_DATA
UMA
RN5112
Do Not Stuff
3D3V_VGA_S0
3D3V_S0
R5124
0R2J-2-GP
PX
R5125
Do Not Stuff
UMA
Q5105
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
TMDS_SCL_C
TMDS_SDA_C
D5102
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
5V_S0
RN5101
SRN2K2J-1-GP
TMDS_SCL
TMDS_SDA
D12G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Level Shifter/Connector
Size
A2
Document Number
BA40-HR
Rev
SD
Date: Thursday, April 07, 2011
Sheet 51 of 109

DP





D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display Port**

Size	Document Number	Rev
A3	BAD50-HR	SD

Date: Thursday, April 07, 2011 Sheet 52 of 109

(Blanking)

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 53 of 109

(Blanking)

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

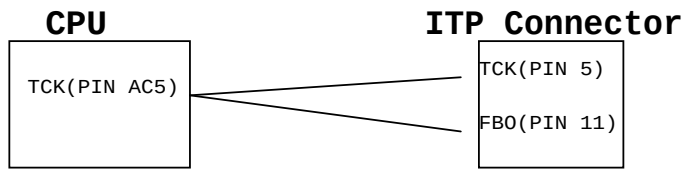
Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 54 of 109

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



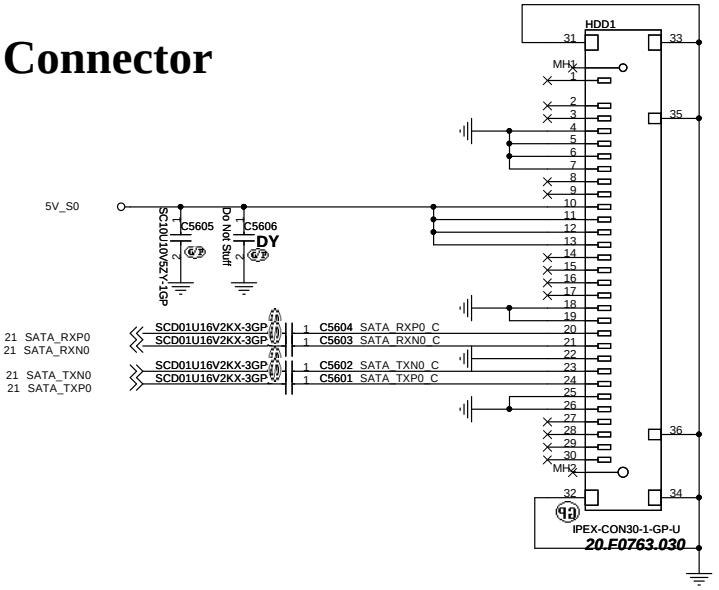
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

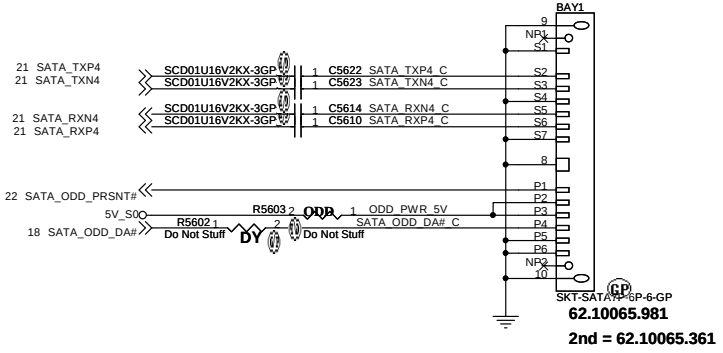
Title: *ITP*		
Size: A4	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 55 of 109	

SSID = SATA

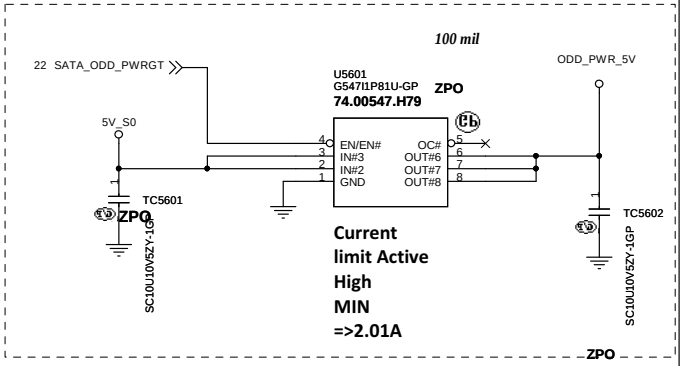
SATA HDD Connector



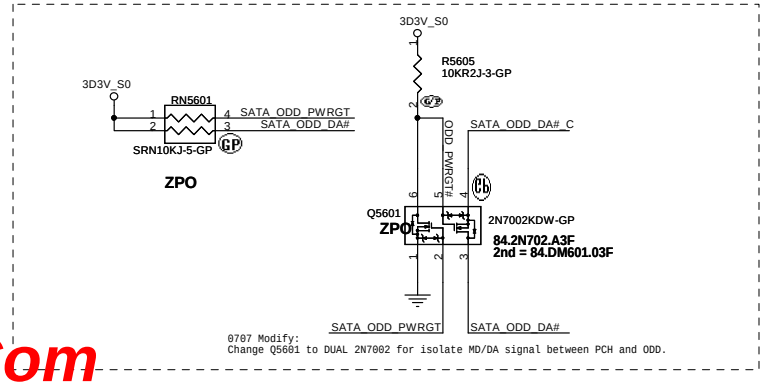
ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



SATA Zero Power ODD



SATA Zero Power ODD



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

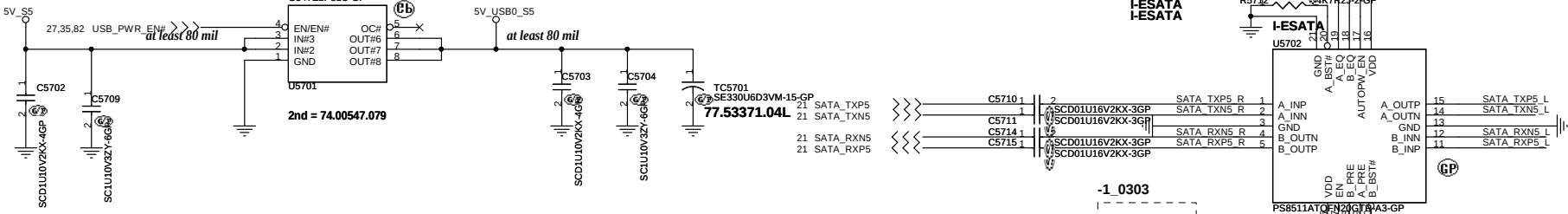
Title: HDD/ODD

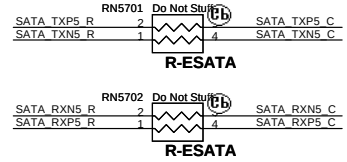
Size: A3 | Document Number: BA40-HR | Rev: SD

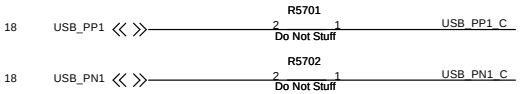
Date: Thursday, April 07, 2011 | Sheet 56 of 109

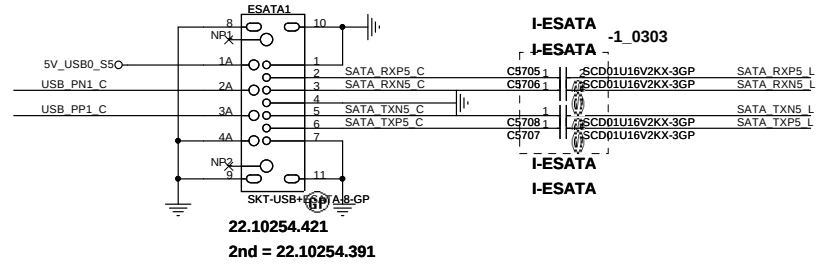
ESATA Power

MIN Current limit 2.5A
LOW ACTIVE TYPE!







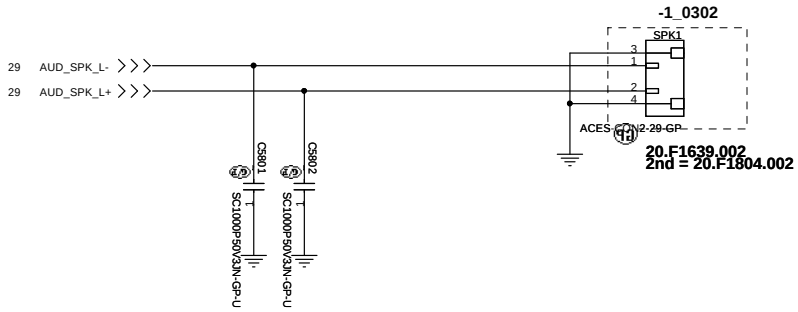


D12G

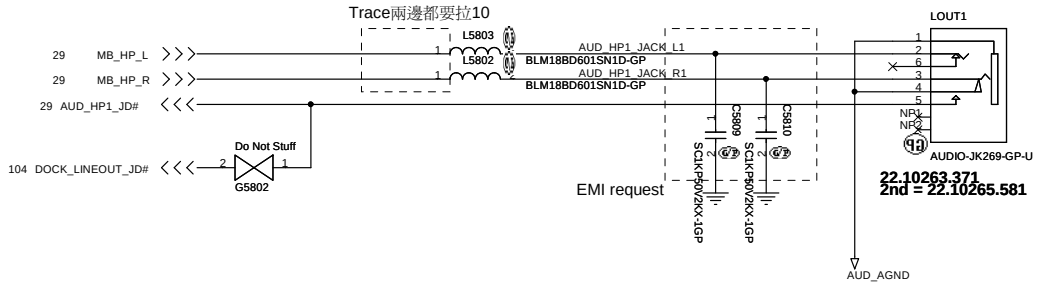
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***E-SATA/USB CHARGER***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 57 of 109	

SSID = AUDIO

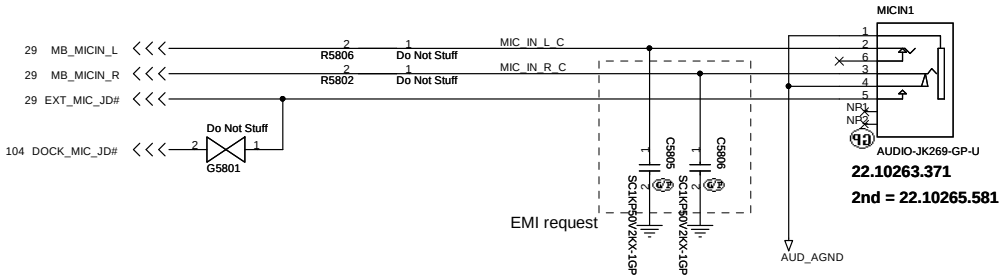
Speaker Connector

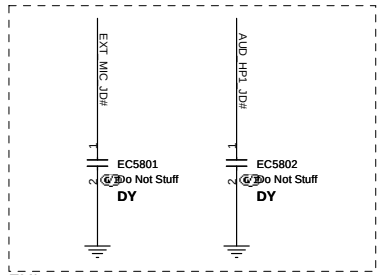


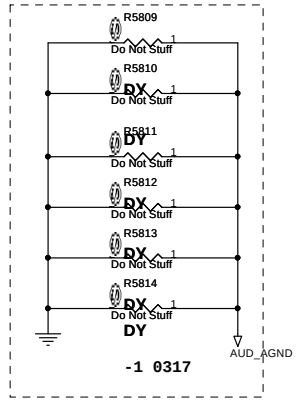
LINE1 OUT



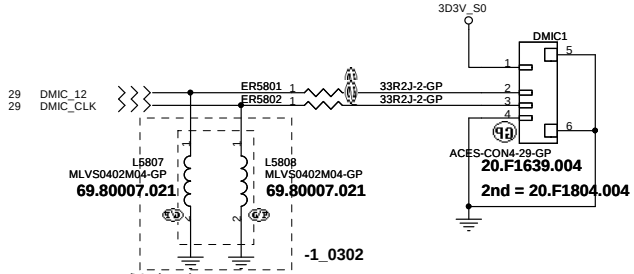
MIC IN







Internal Microphone



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

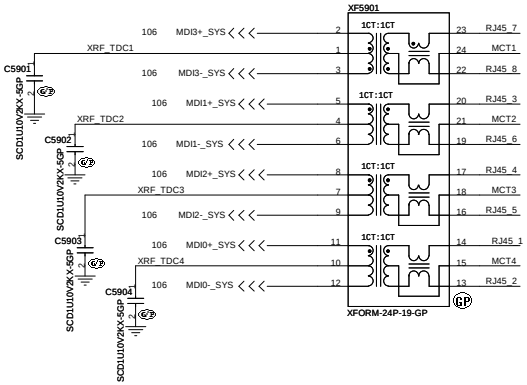
Size	Document Number	Rev
A3	BA40-HR	SA

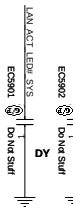
Date: Thursday, April 07, 2011 Sheet 58 of 109

GIGA Lan Transformer

SSID = LOM

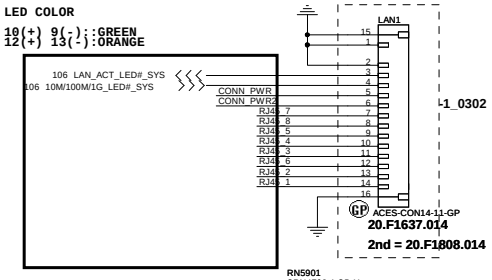
LAN MDI Off-Page

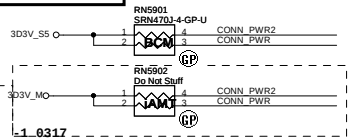




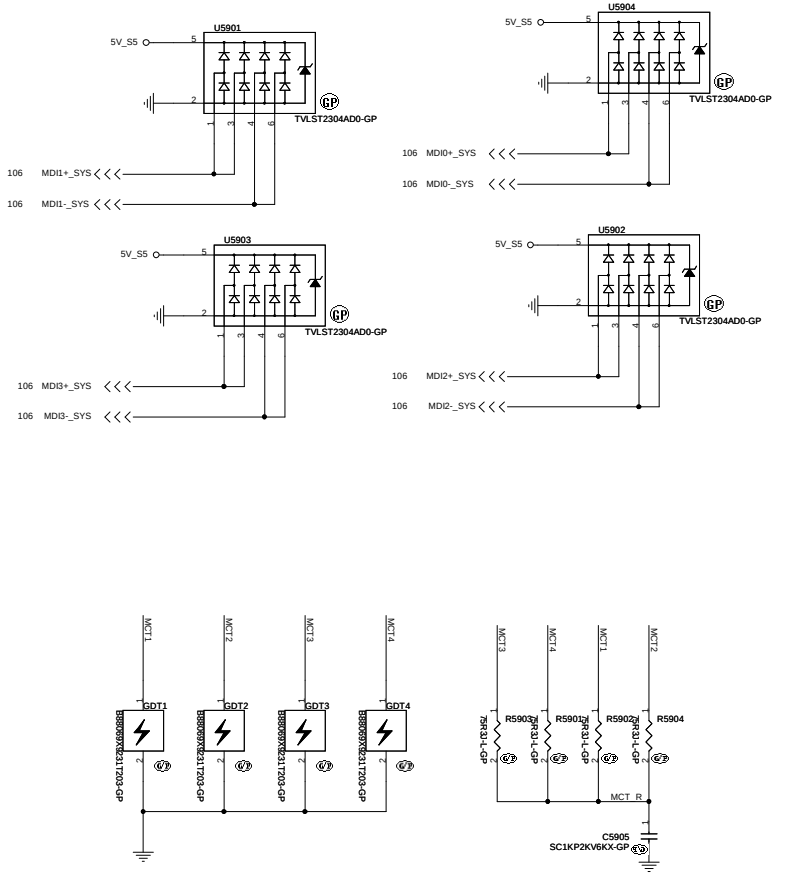
LED COLOR

10(+) 9(-)::GREEN
12(+) 13(-):ORANGE





For EMI



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

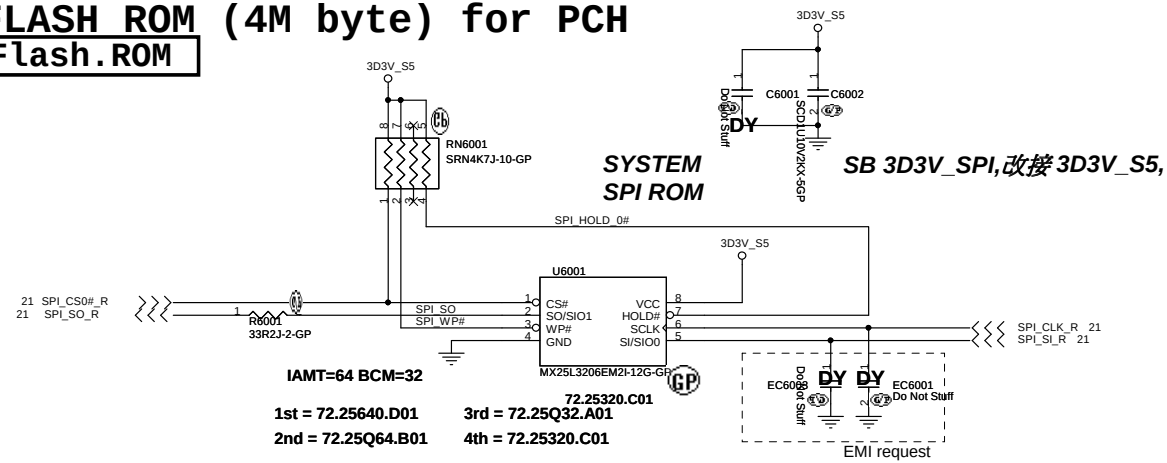
Title: ***LAN CONNECTOR***

Size	Document Number	Rev
Custom	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 59 of 109

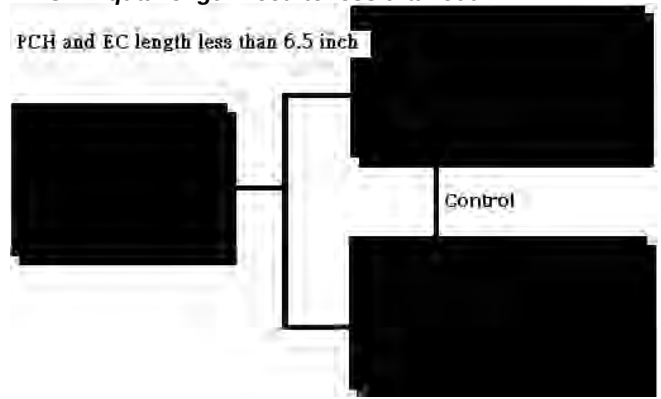
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

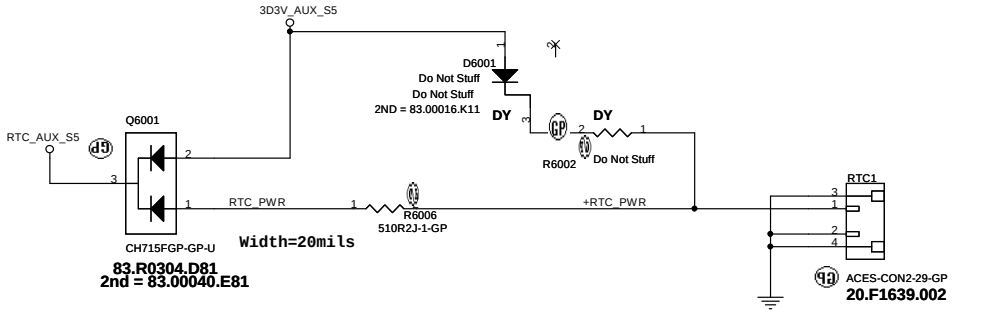


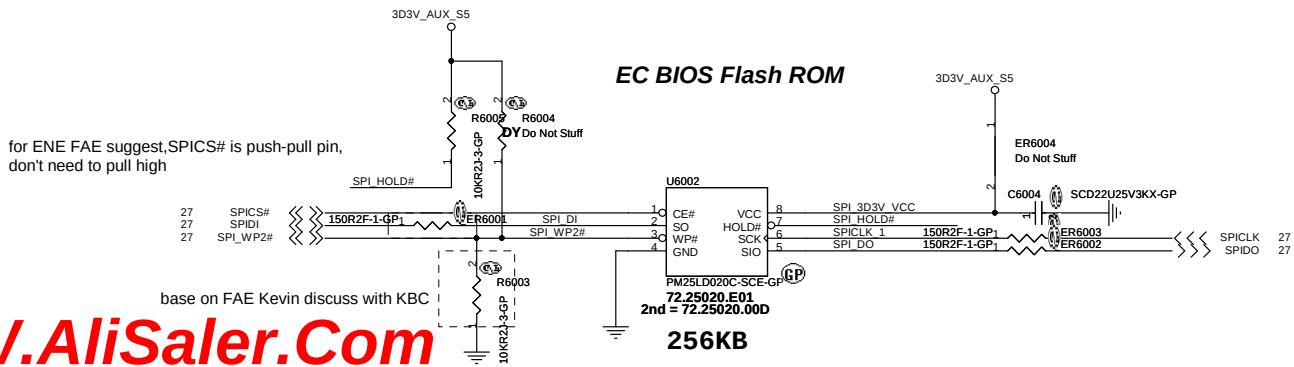
SB 3D3V_SPI,改接 3D3V_S5,

SPI ROM Equal length need to less than 500mil



SSID = RBATT





D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size: Custom | Document Number: **BA40-HR** | Rev: **SD**

Date: Thursday, April 07, 2011 | Sheet 60 of 109

SSID = USB

D12G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 61 of 109

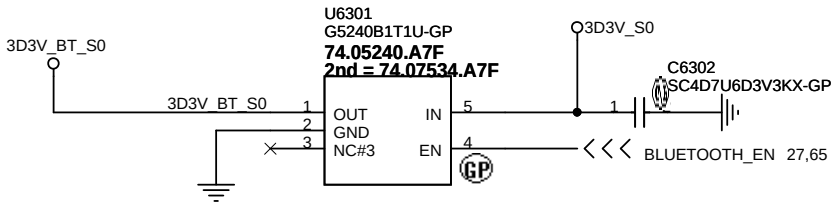
D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB 3.0 Port***
Size: A3	Document Number: **BA40-HR**
Rev: **SD**	
Date: Thursday, April 07, 2011	Sheet 62 of 109

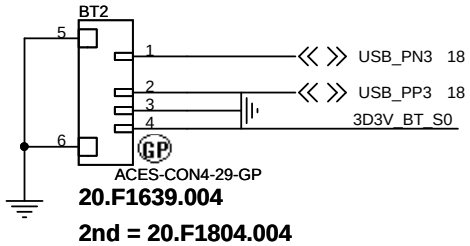
SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 63 of 109	

Finger printer

JE40 delete FP function

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

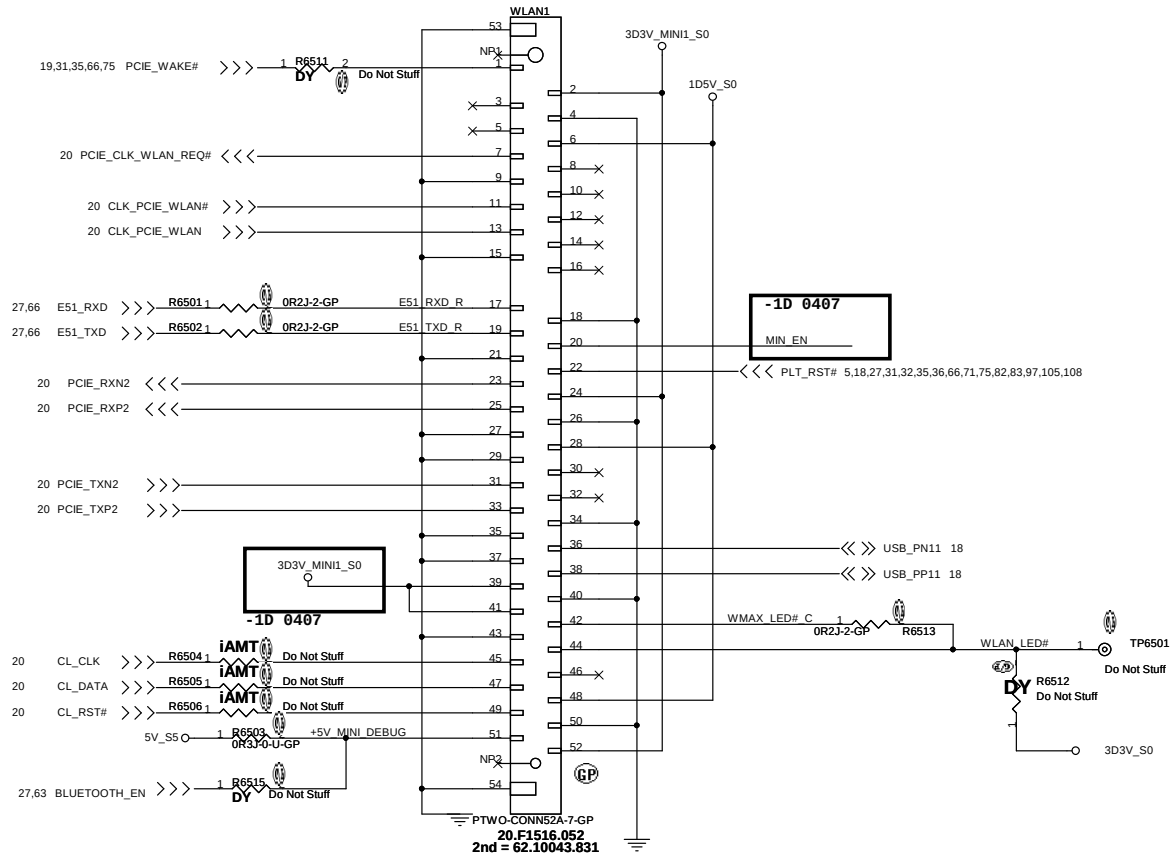
Title: ***RESERVED***

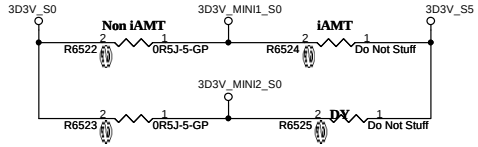
Size	Document Number	Rev
A4	BA40-HR	SD

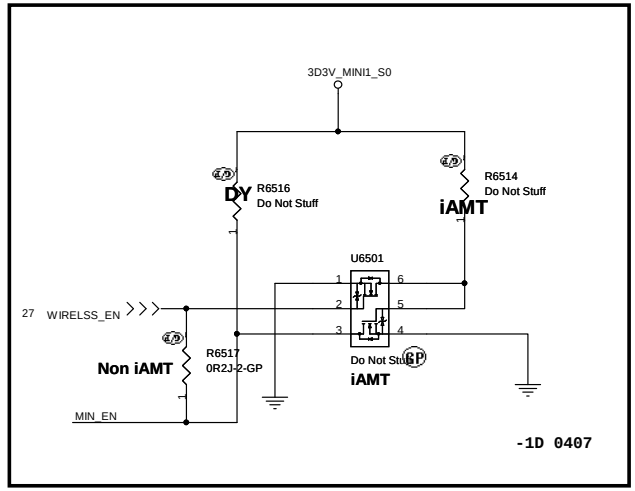
Date: Thursday, April 07, 2011 Sheet 64 of 109

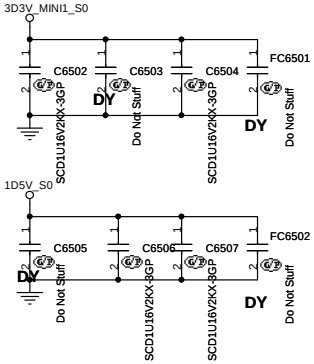
SSID = Wireless

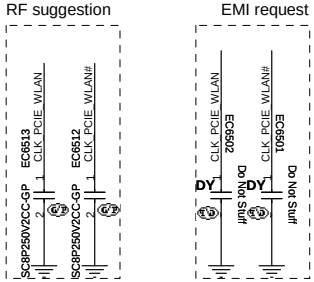
Mini Card Connector(802.11a/b/g/n)











D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MINICARD(WLAN)/ITP CONN*

Size	Document Number	Rev
A3	BA40-HR	SD

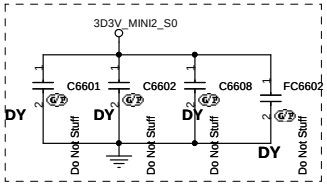
Date: Thursday, April 07, 2011 Sheet 65 of 109

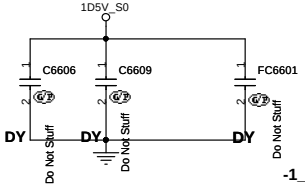
SSID = Wireless

Mini Card Connector(WWAN)

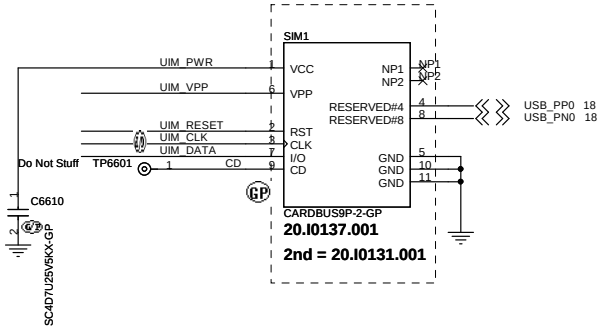
20100712 V1.5

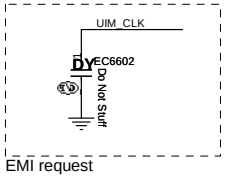
Place near MINI Card CONN



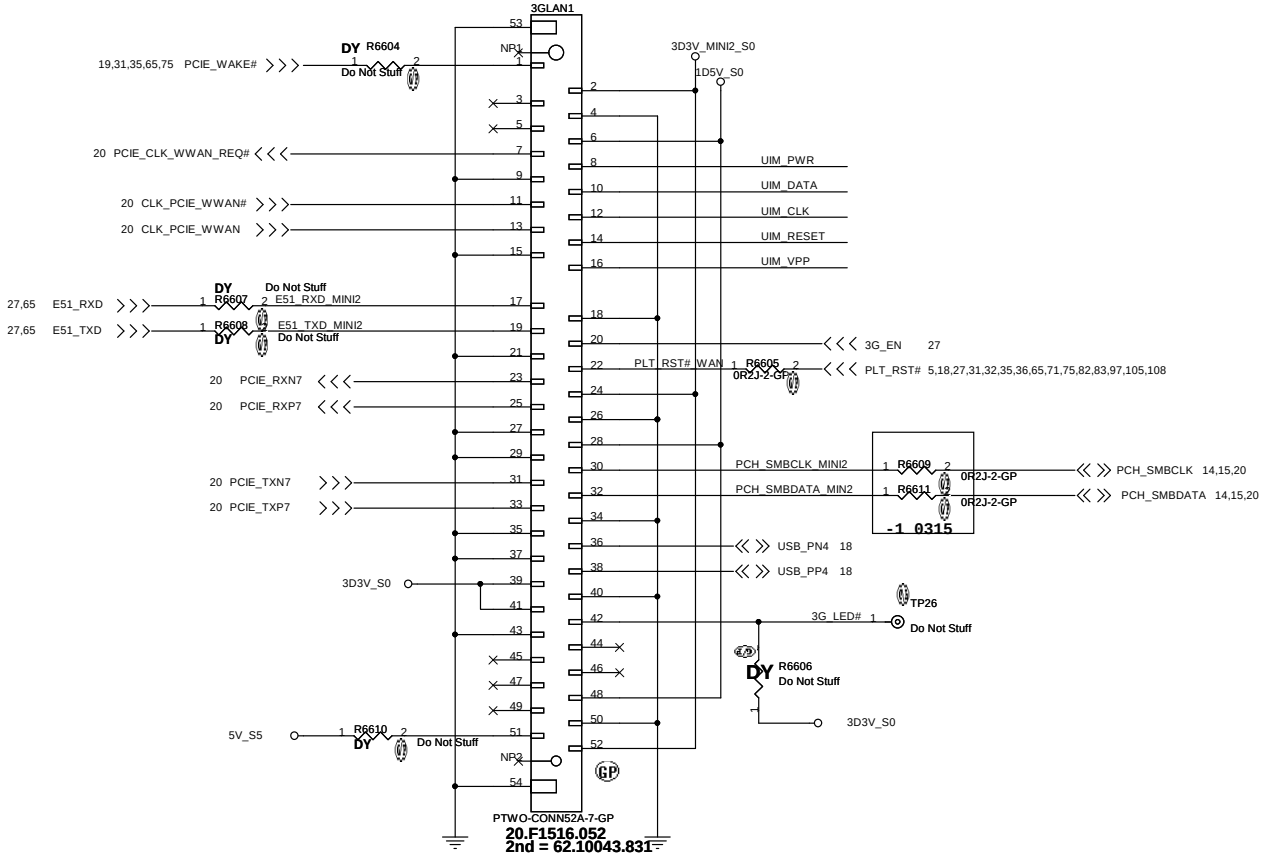


-1_0304





EMI request



D12G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WWAN Connector	
Size A3	Document Number BA40-HR	Rev SD
Date: Thursday, April 07, 2011	Sheet 66 of 109	

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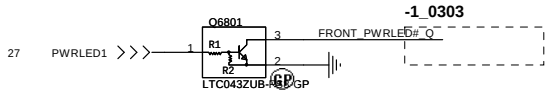
D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 67 of 109	

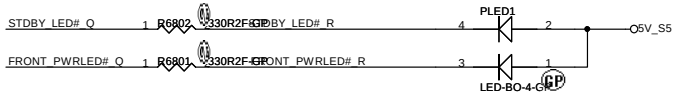
SSID = User.Interface

Power button LED

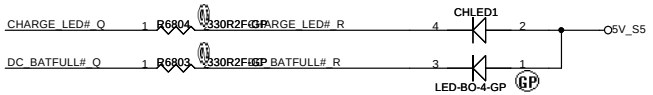


2nd = 84.05143.011

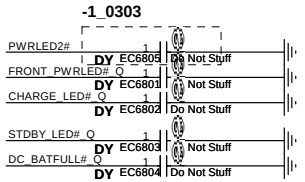
3rd = 84.00143.E1K



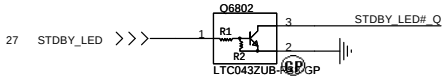
83.00195.G70



83.00195.G70



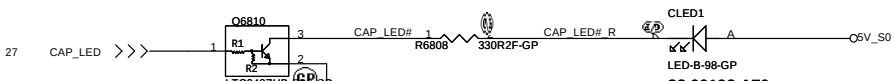
Power STDBY_LED



2nd = 84.05143.011

3rd = 84.00143.E1K

Caps Lock LED

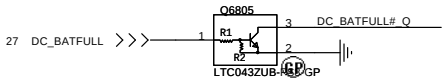


2nd = 84.05143.011

3rd = 84.00143.E1K

83.00193.A70

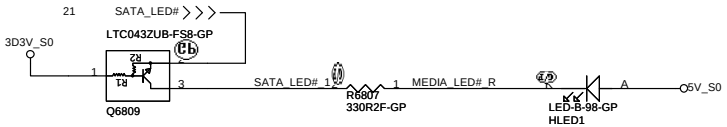
Battery LED2(DC_BATFULL)



2nd = 84.05143.011

3rd = 84.00143.E1K

SATA HDD LED

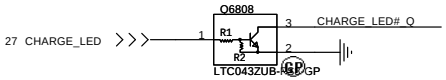


2nd = 84.05143.011

3rd = 84.00143.E1K

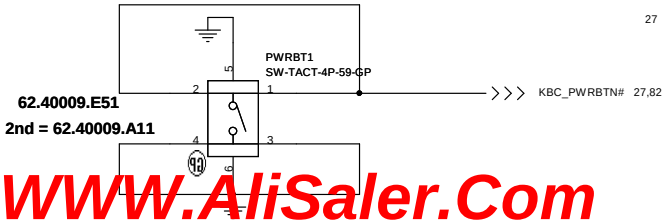
83.00193.A70

Battery LED1(CHARGE)



2nd = 84.05143.011

3rd = 84.00143.E1K



62.40009.E51

2nd = 62.40009.A11

2nd = 84.05143.011

3rd = 84.00143.E1K

83.00193.A70

for factory test

D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

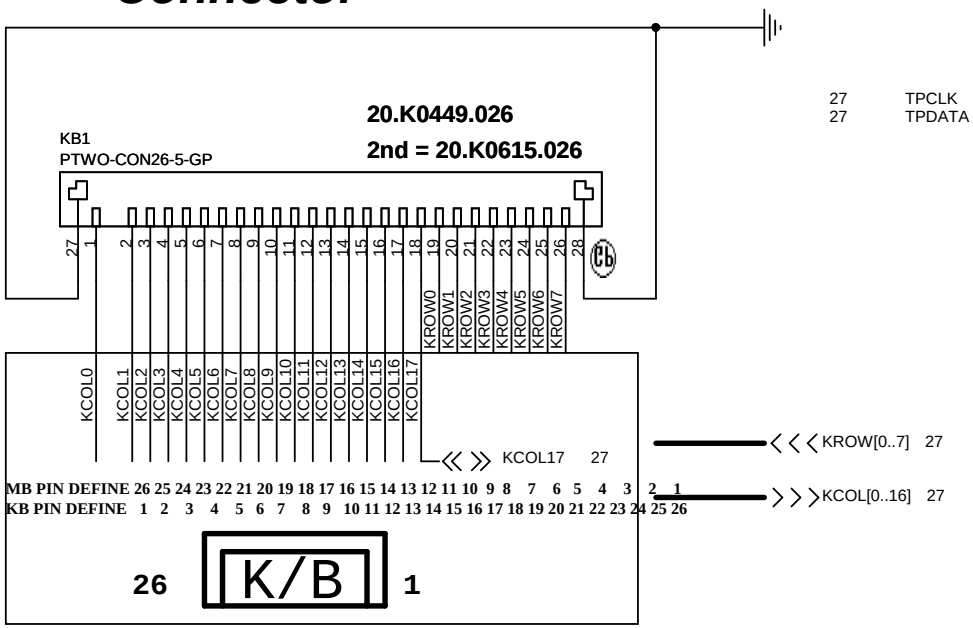
Size: Custom | Document Number: BA40-HR | Rev: SD

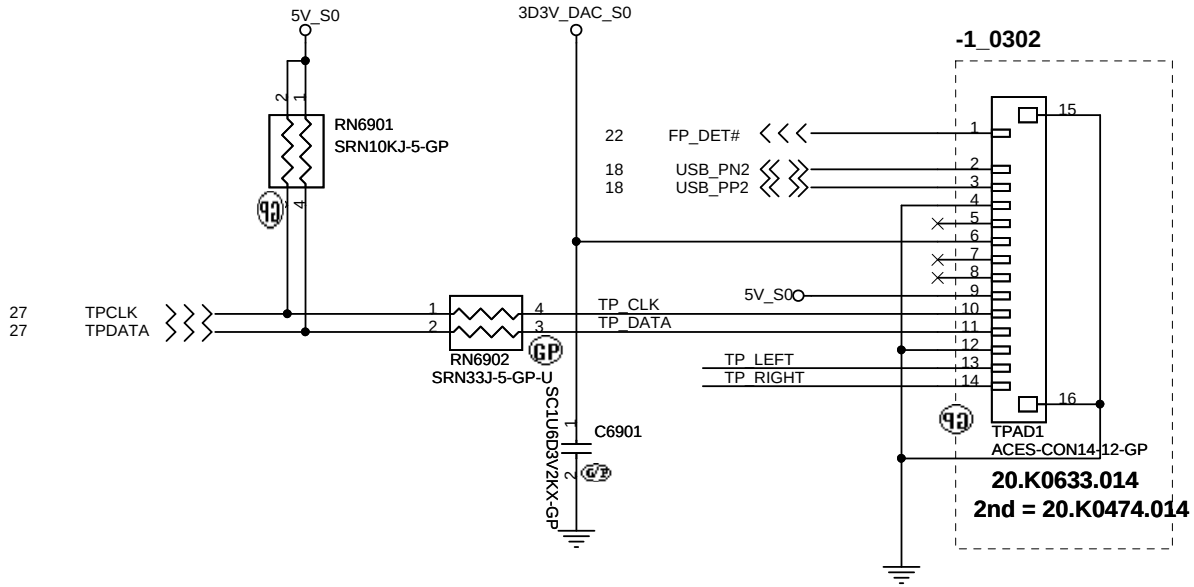
Date: Thursday, April 07, 2011 | Sheet 68 of 109

TOUCH PAD

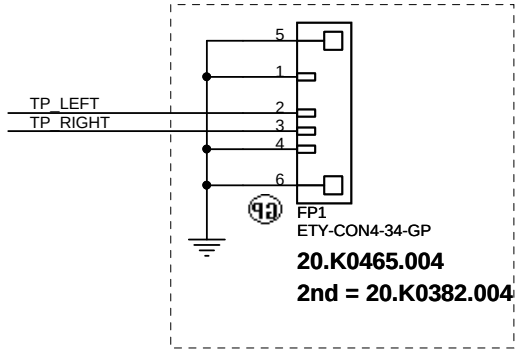
SSID = KBC

Internal KeyBoard Connector





Rubber Dome



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 69 of 109

D12G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

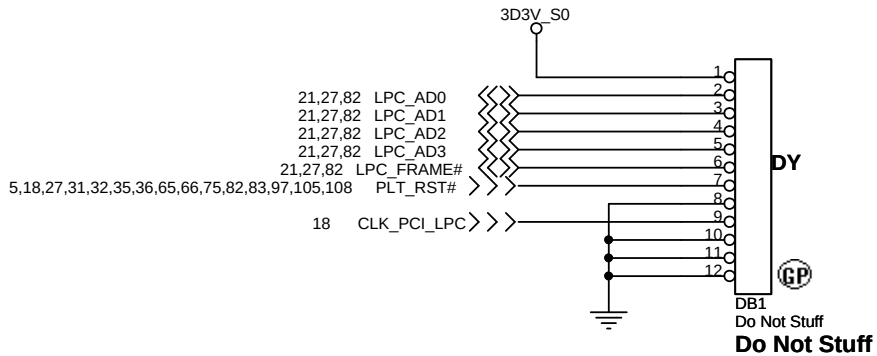
Title

Hall Sensor

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 70 of 109

SB modify to test pad



Do Not Stuff

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 71 of 109

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D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A3	Document Number: **BA40-HR**
Rev: **SD**	
Date: Thursday, April 07, 2011	Sheet 72 of 109

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 73 of 109

SD/XD/MS Card Reader

SSID = SDIO

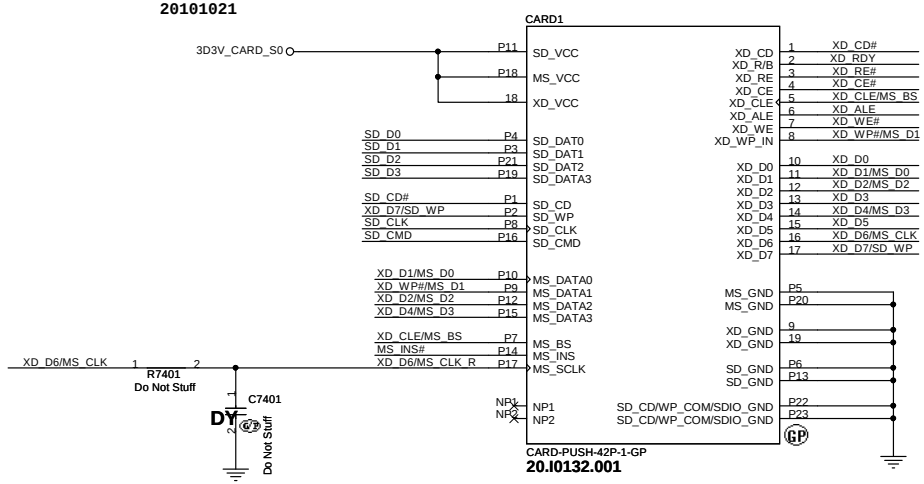
32 XD_CD#
32 SD_D1
32 SD_D0
32 SD_D2
32 SD_D3

32 SD_CLK
32 SD_CMD

32 SD_CD#
32 MS_INS#

32	XD_RDY	**SP1(N0 SD_D7)**
32	XD_RE#	**SP2(NO SD_D6)**
32	XD_CE#	**SP3(NO_SD_D5)**
32	XD_WE#	**SP4(No SD_D4)**
32	XD_CLE/MS_BS	**SP5**
32	XD_ALE	**SP6**
32	XD_WP#/MS_D1	**SP7**
32	XD_D0	**SP8(NO MS_D4)**
32	XD_D1/MS_D0	**SP9**
32	XD_D2/MS_D2	**SP10**
32	XD_D3	**SP11(MS_D6)**
32	XD_D4/MS_D3	**SP12**
32	XD_D5	**SP13**
32	XD_D6/MS_CLK	**SP14**
32	XD_D7/SD_WP	**SP15**

20101021

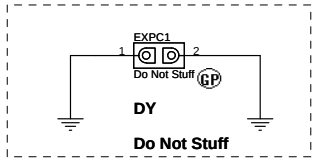


D12G

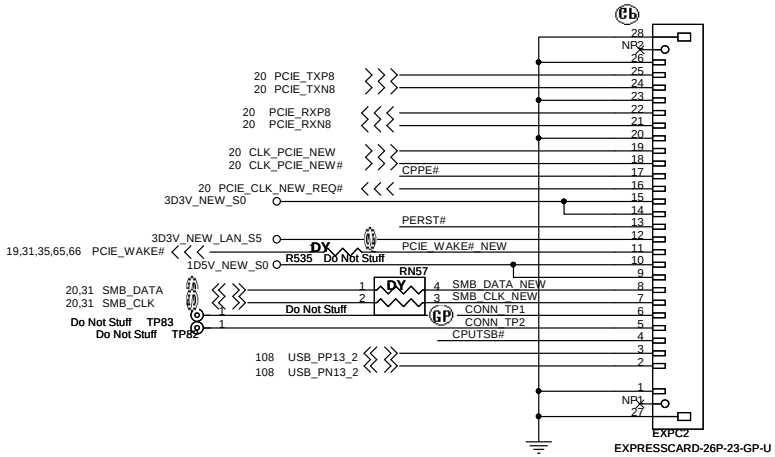
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CARD Reader CONN***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 74 of 109	

SSID = ExpressCard

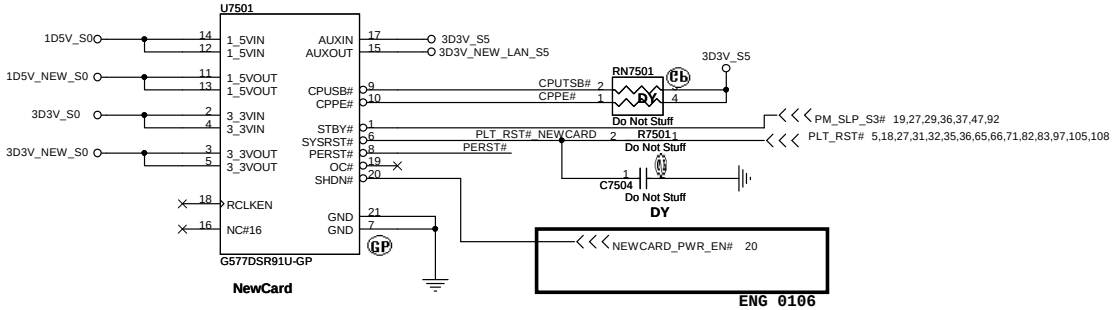
For Expresscard socket



+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

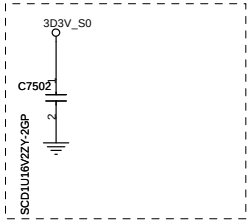


62.10081.461

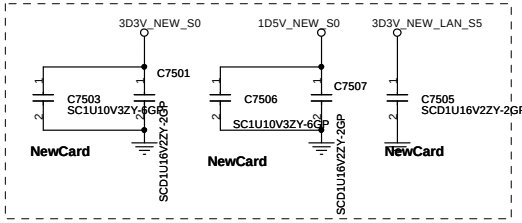


ENG 0106

Place them Near to Chip



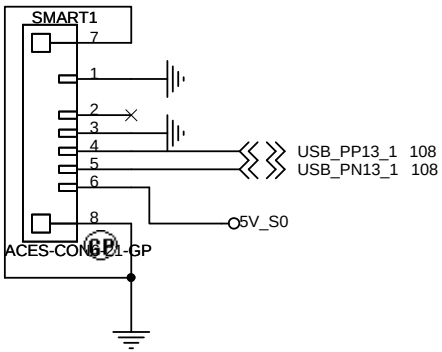
Place them Near to Connector



For EMI

D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *New Card*		
Size: A3	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 75 of 109	



20.K0473.006
2nd = 20.K0392.006

D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 76 of 109	

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	**BA40-HR**	**SD**

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 78 of 109

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
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Date: Thursday, April 07, 2011 Sheet 79 of 109

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BA40-HR	SD

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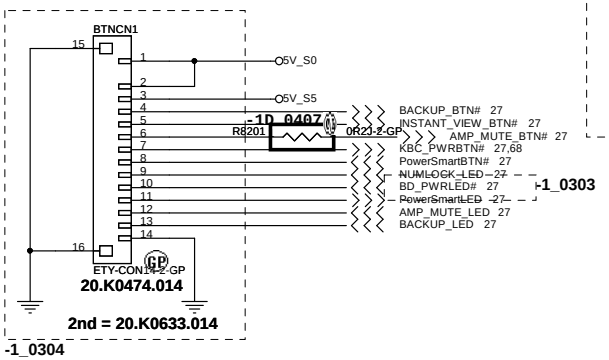
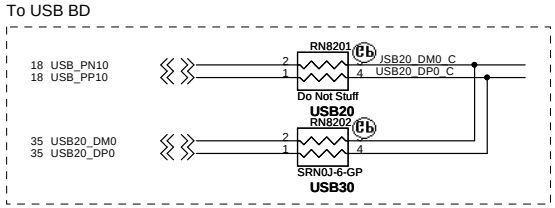
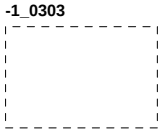
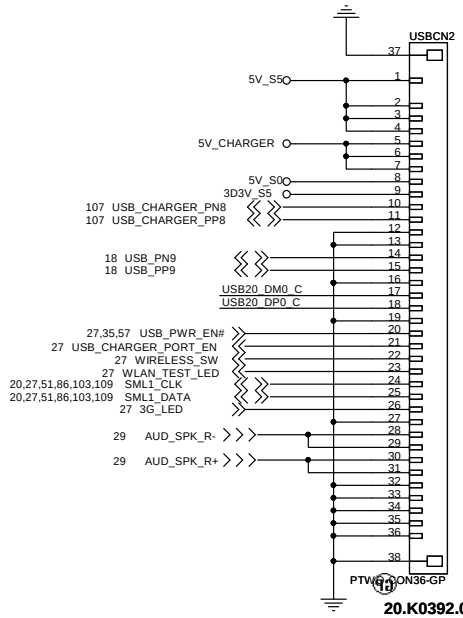
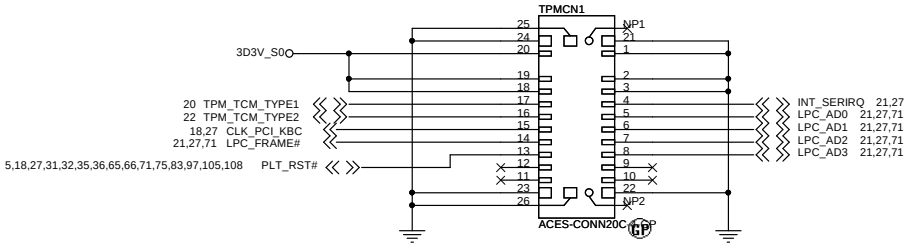
PWRCN1 FFC 異面

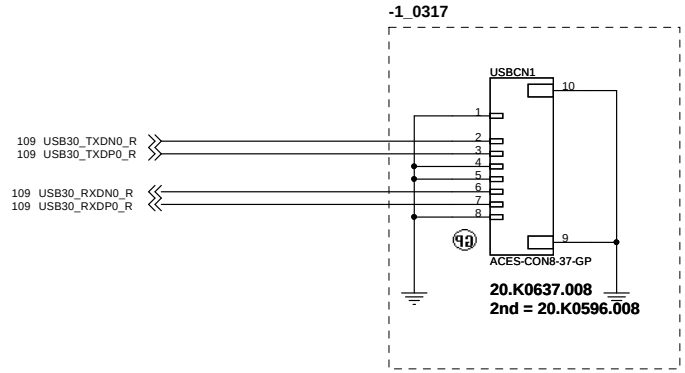






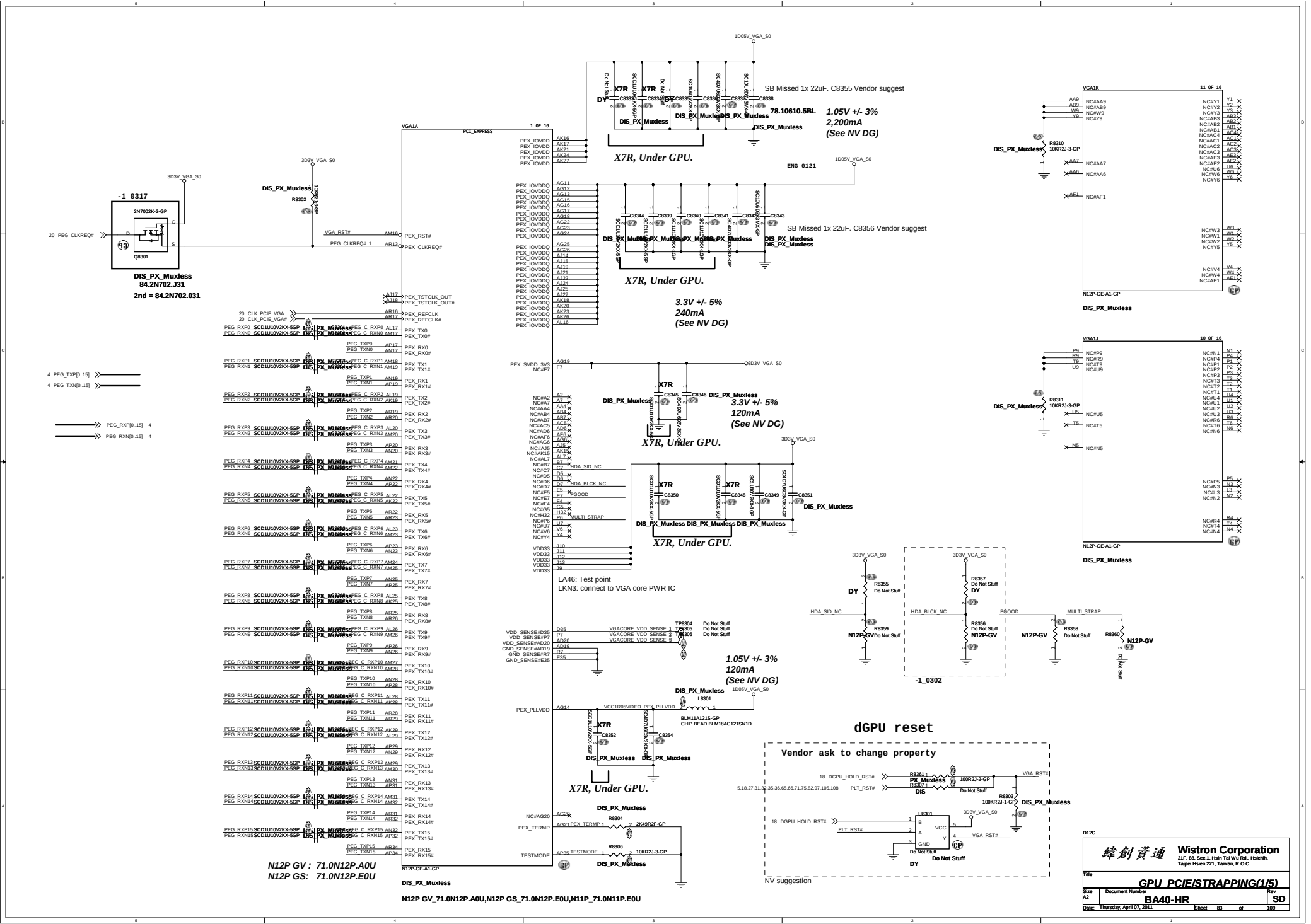






D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***IO Board Connector***
Size A3	Document Number **BA40-HR** Rev **SD**
Date: Thursday, April 07, 2011	Sheet 82 of 109


VGA1A
PCI_EXPRESS
1 OF 16
N12P-GE-A1-GP
DIS_PX_Muxless
N12P GV_71.0N12P.A0U,N12P GS_71.0N12P.E0U,N11P_71.0N11P.E0U
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
1D05V_VGA_S0
3D3V_VGA_S0
SB Missed 1x 22uF. C8355 Vendor suggest
78.10610.5BL
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
ENG 0121
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
3.3V +/- 5%
120mA
(See NV DG)
1.05V +/- 3%
120mA
(See NV DG)
LA46: Test point
LKN3: connect to VGA core PWR IC
-1 0317
2N7002K-2-GP
Q8301
84.2N702.J31
2nd = 84.2N702.031
VGA1K
11 OF 16
VGA1J
10 OF 16
dGPU reset
Vendor ask to change property
-1_0302
NV suggestion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_PCIE/STRAPPING(1/5)
BA40-HR
Rev SD
Thursday, April 07, 2011
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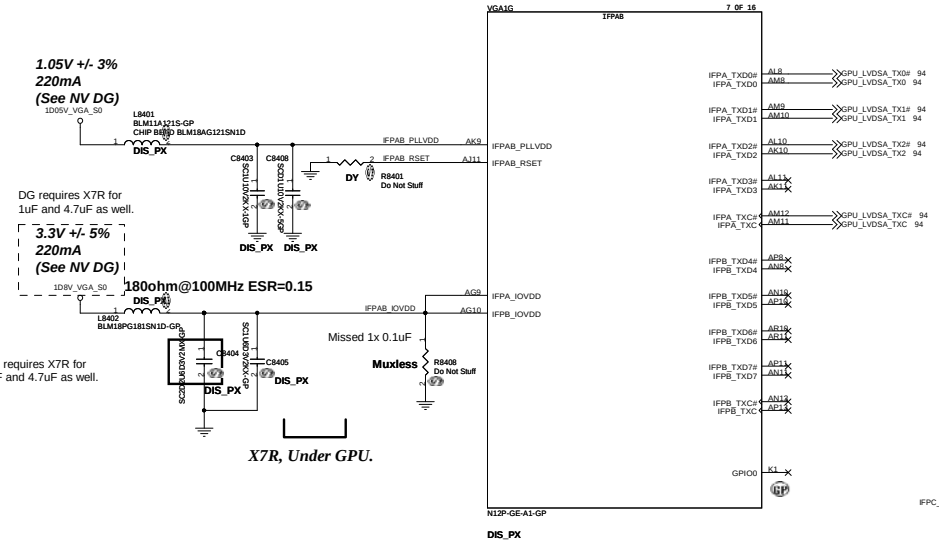
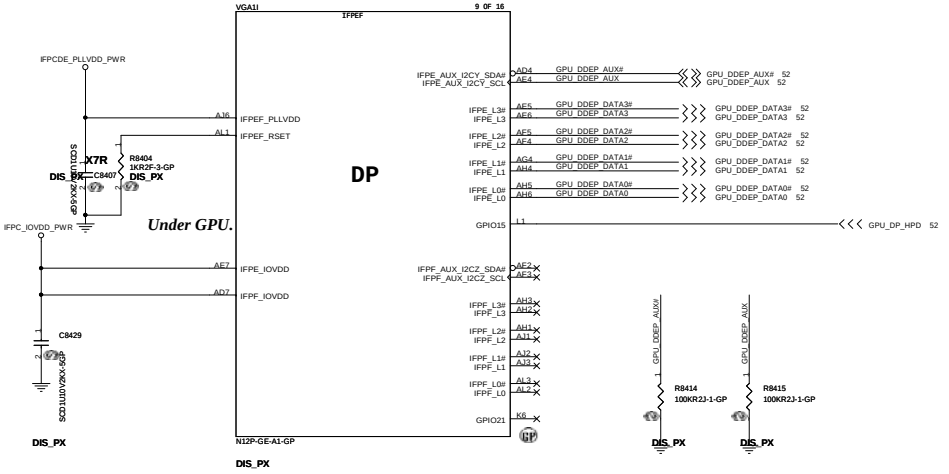
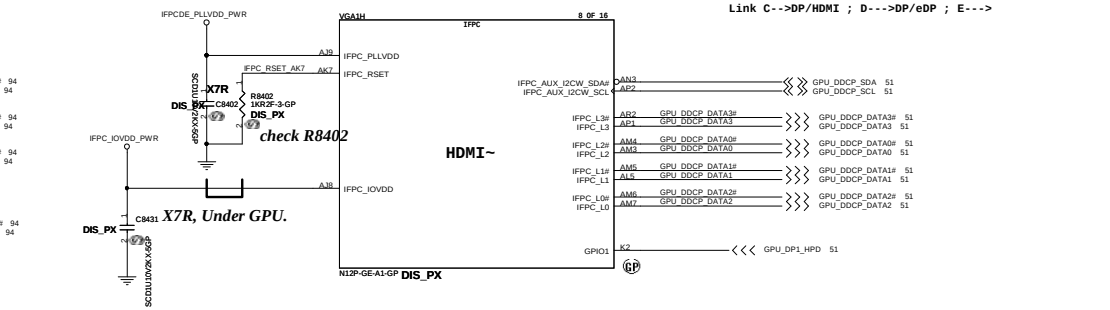
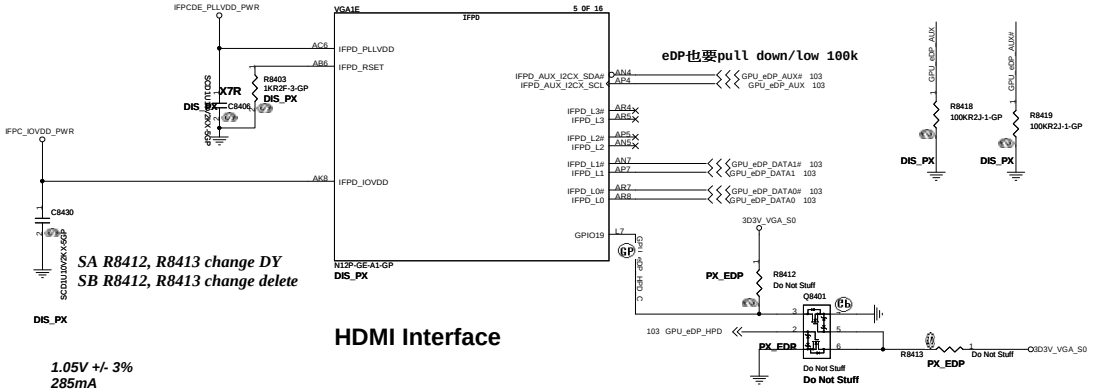
LVDS Interface

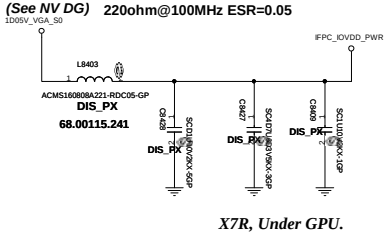


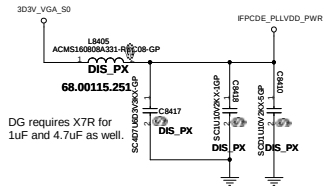






HDMI Interface





D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

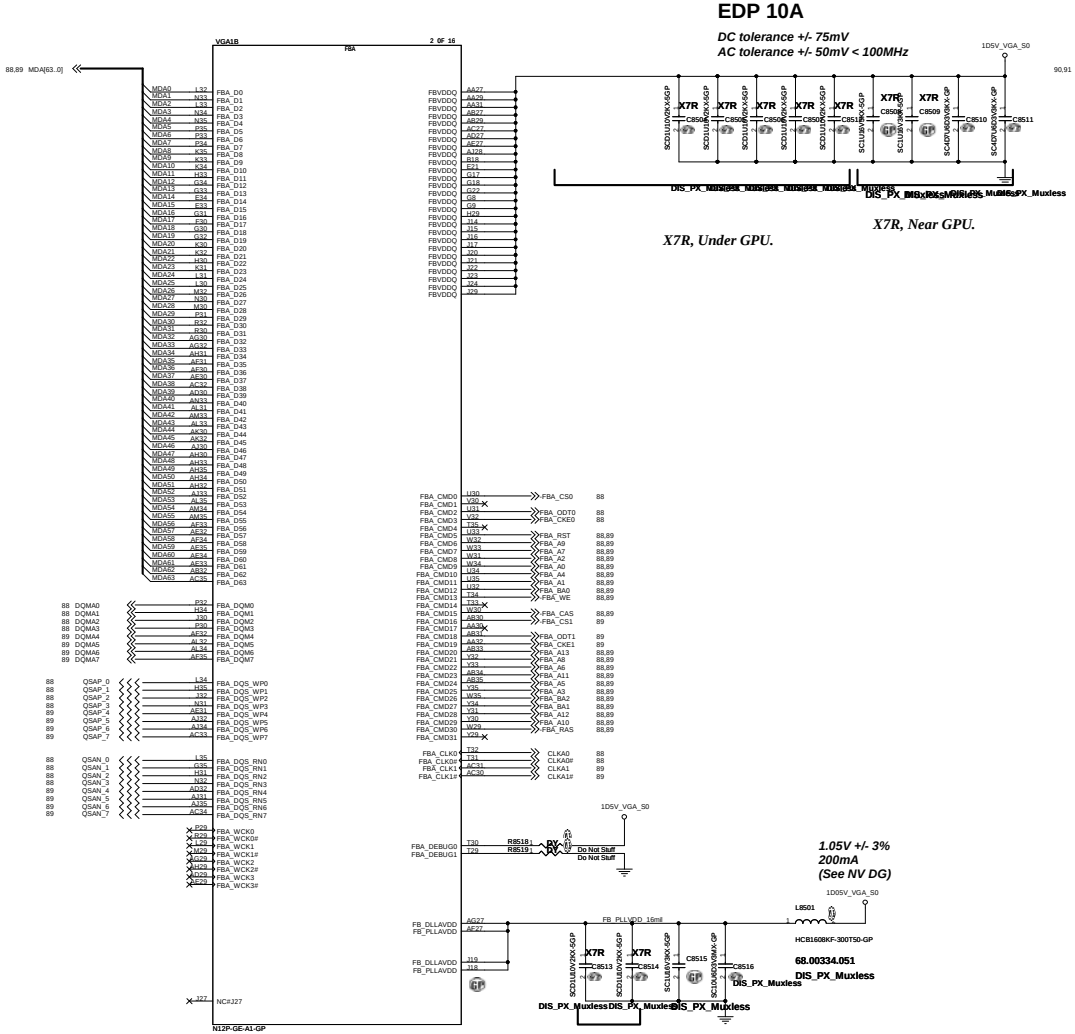
Title: GPU Memory(2/5)

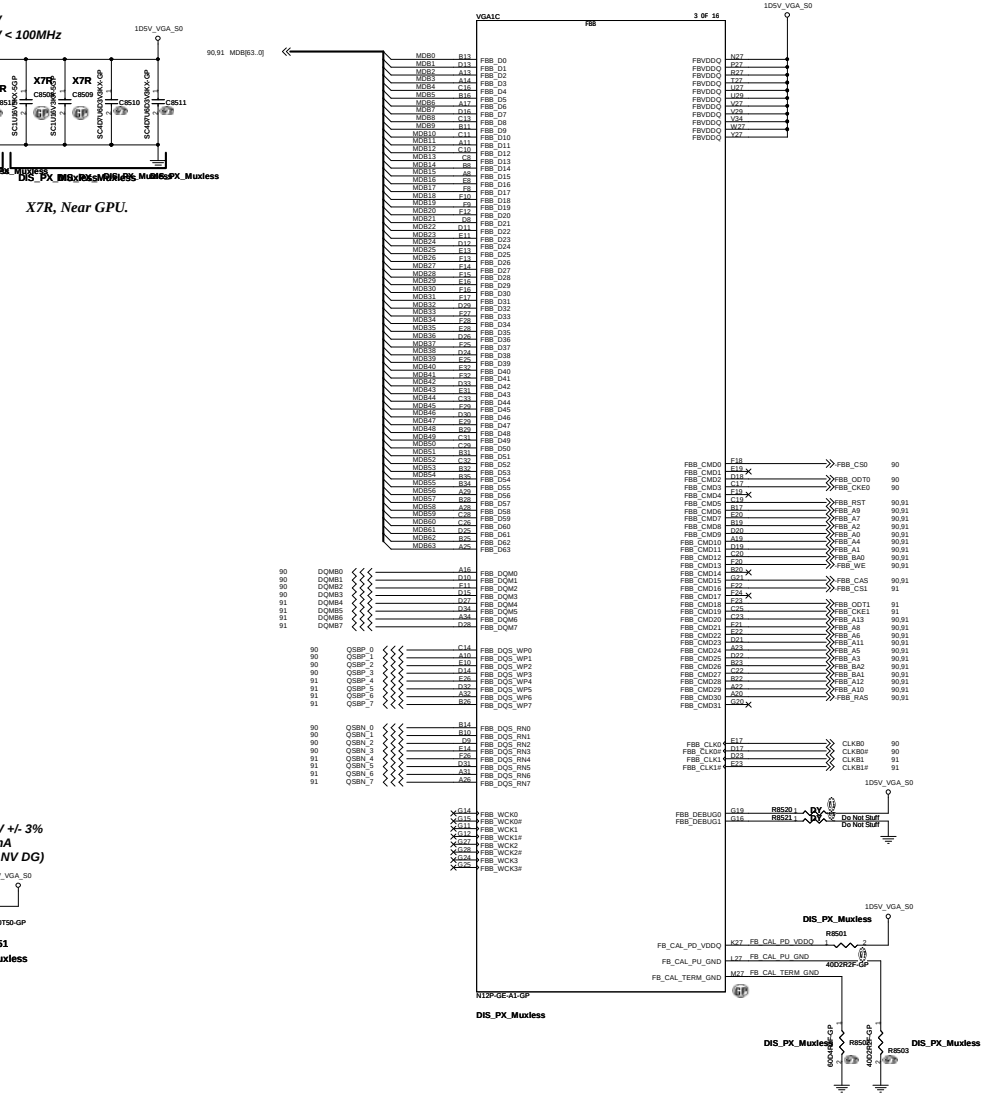
Size: A2 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 84 of 109

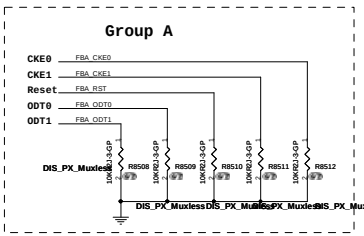
EDP 10A

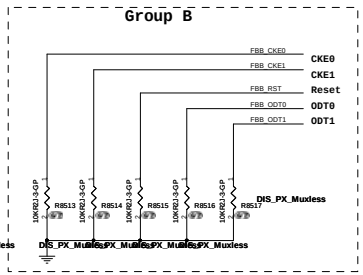
DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz





FBCLK Termination place on VRAM side





FBCLK Termination place on VRAM side

D12G

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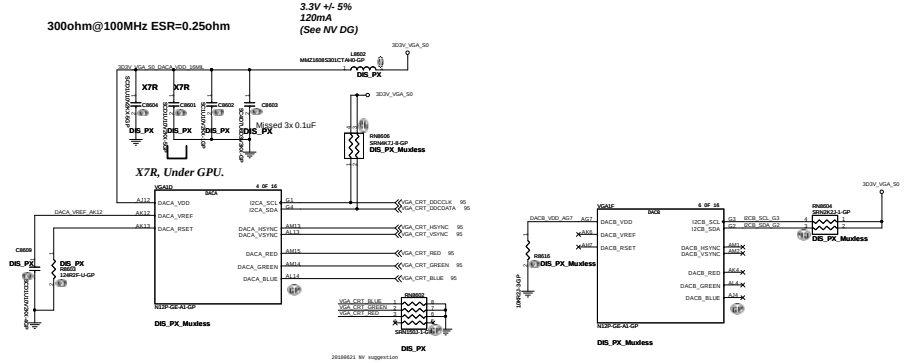
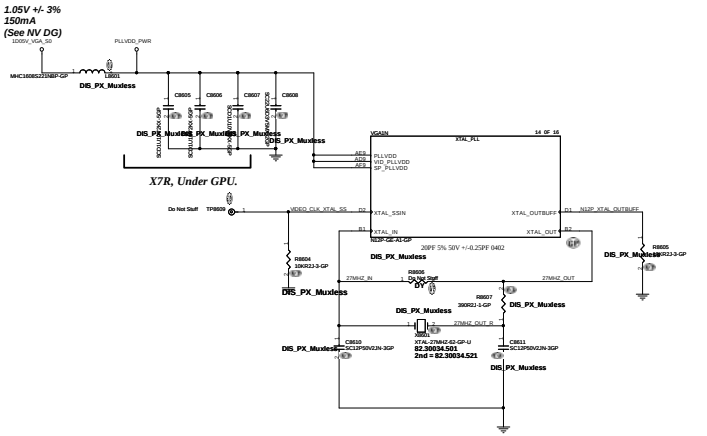
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_DP/LVDS/CRT/GPIO(3/5)**

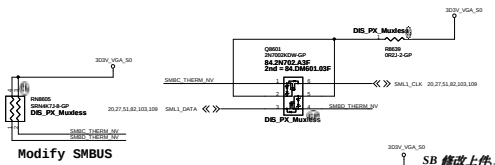
Size	Document Number	Rev
Custom	BA40-HR	SD

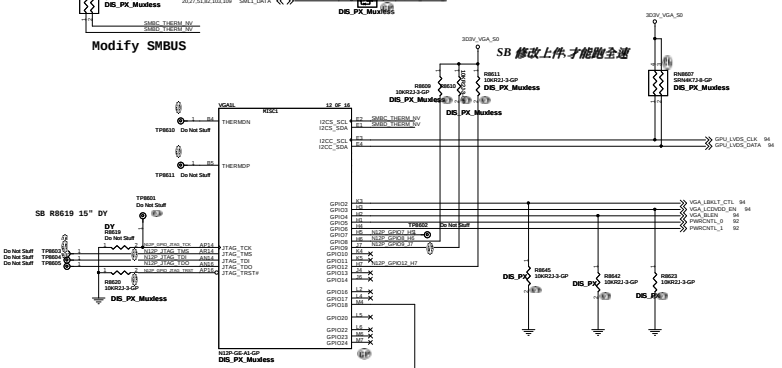
Date: Thursday, April 07, 2011 Sheet 85 of 109

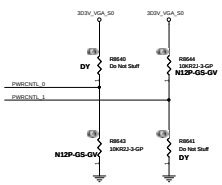




VGA Thermal sensor P2800





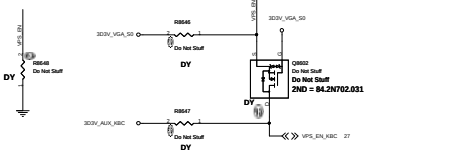


N12P-GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.825V
	H	L	0.9V
	L	H	0.975V
	H	H	1V

← default boot voltage table

Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
64Mx16 DDR3	Hynix	0x2	H5TQ1G63DFR-11C	900/800
	Samsung	0x3	K4W1G1646E-HC11	900
	Samsung	TBD	K4W1G1646G-BC11	900/800
	Hynix		H5TQ1G63BFR-12C	800
	Samsung		K4W1G1646E-HC12	800



NVIDIA TABLE

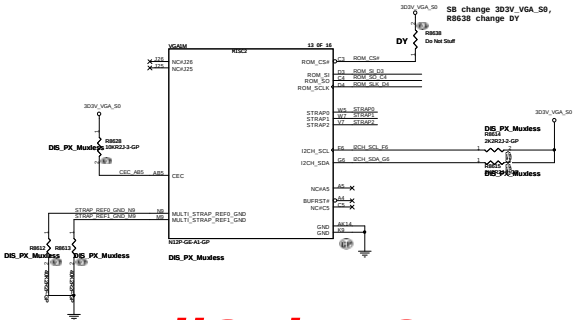
	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

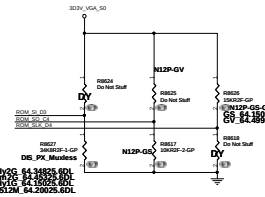
TABLE NVIDIA

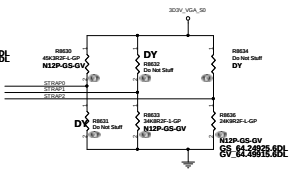
	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

N12P-GS USE 1111 (45K) | N12P-GV | N11P-GE Pull Low | N11P-GS Pull Low | N12P-GE

	ROM_SI	ROM_SO	ROM_CLK	STRAP0	STRAP1	STRAP2
N12P_GS		PL 10K ohm	PH 15K ohm	PH 45K ohm	PL 35K ohm	PL 25K ohm
N12P_GV		PH 10K ohm	PH 5K ohm	PH 45K ohm	PL 35K ohm	PL 5K ohm







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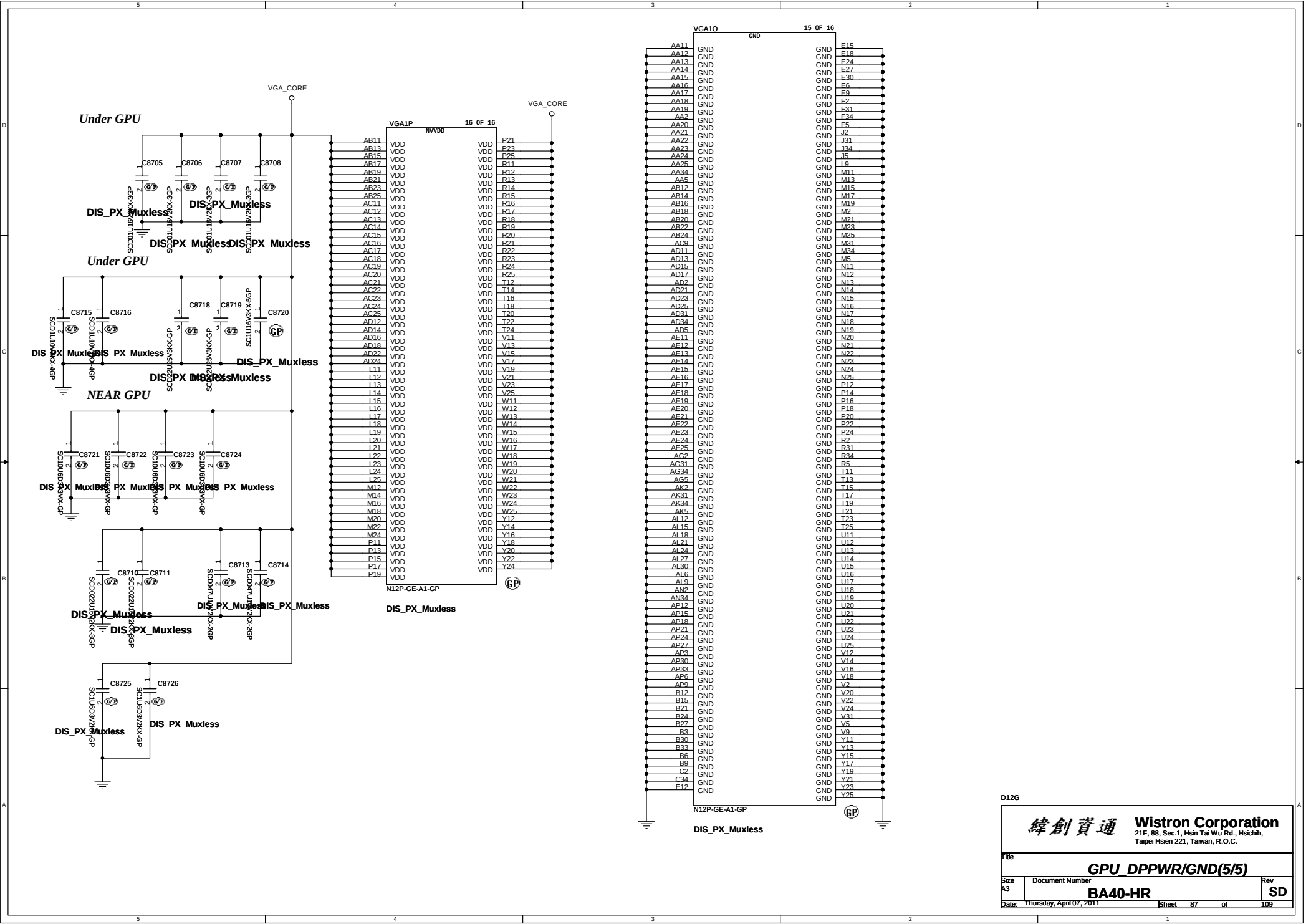
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A1	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 86 of 108



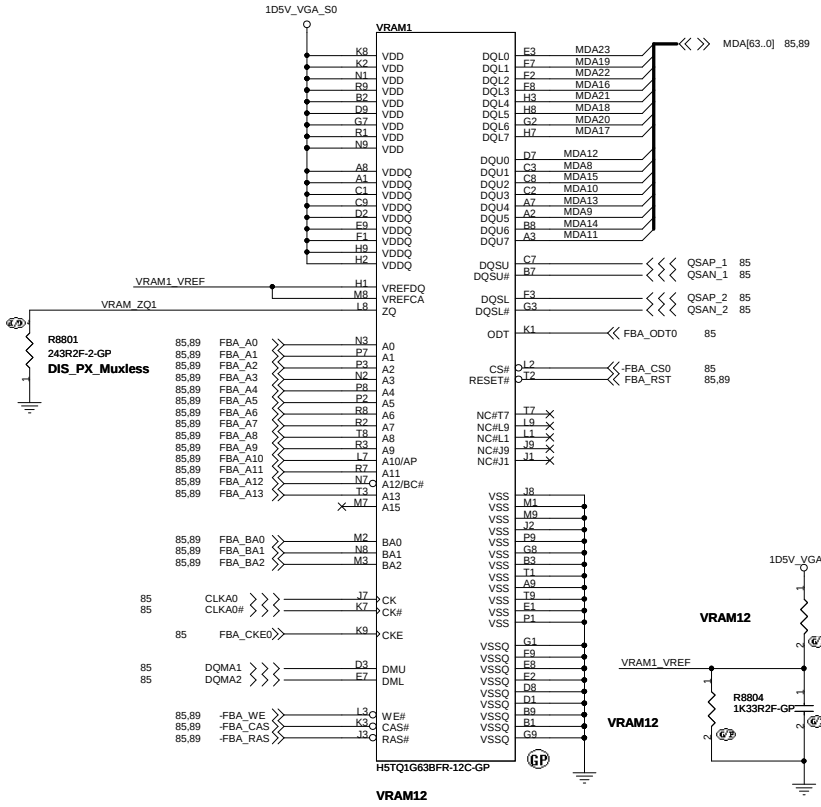
D12G

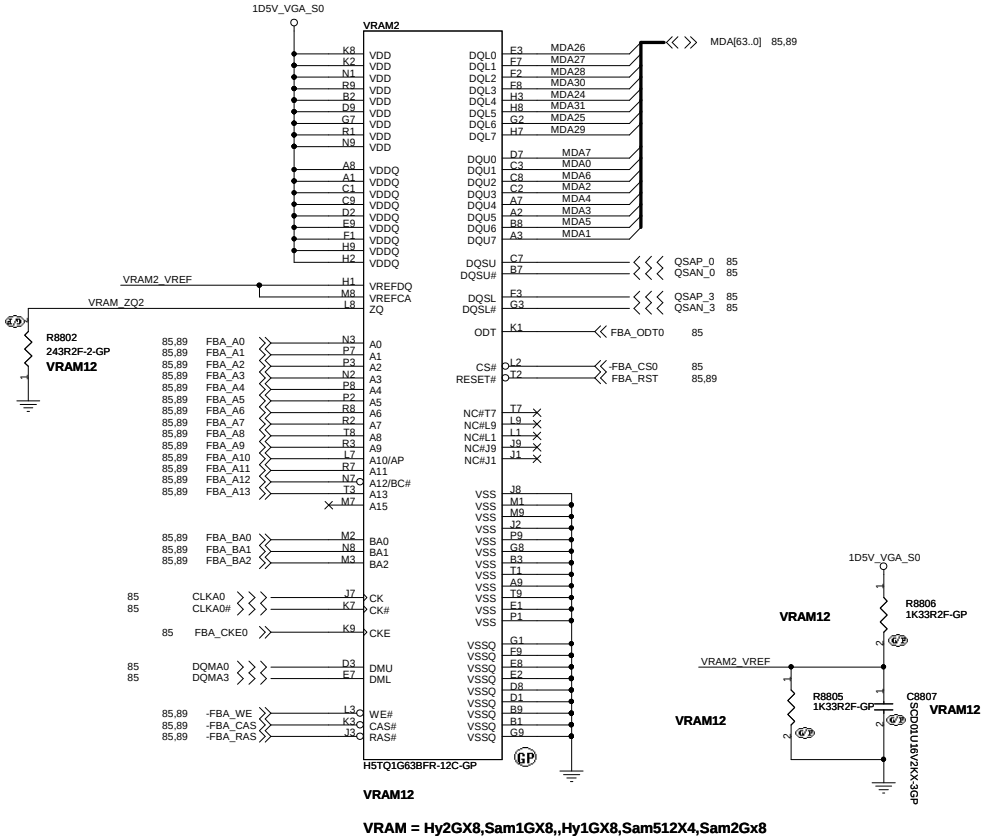
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 87 of 109





Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

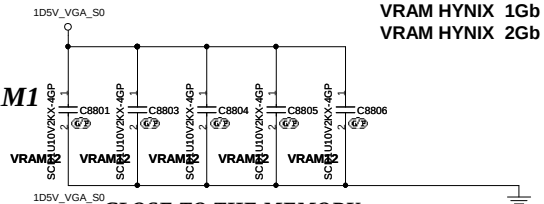
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

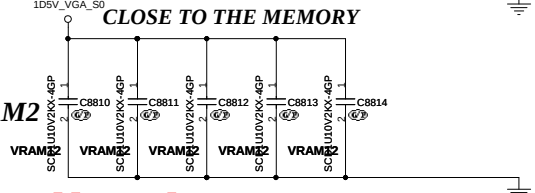
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

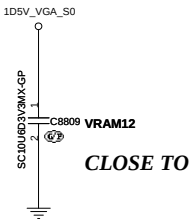
FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2





CLOSE TO THE MEMORY

D12G

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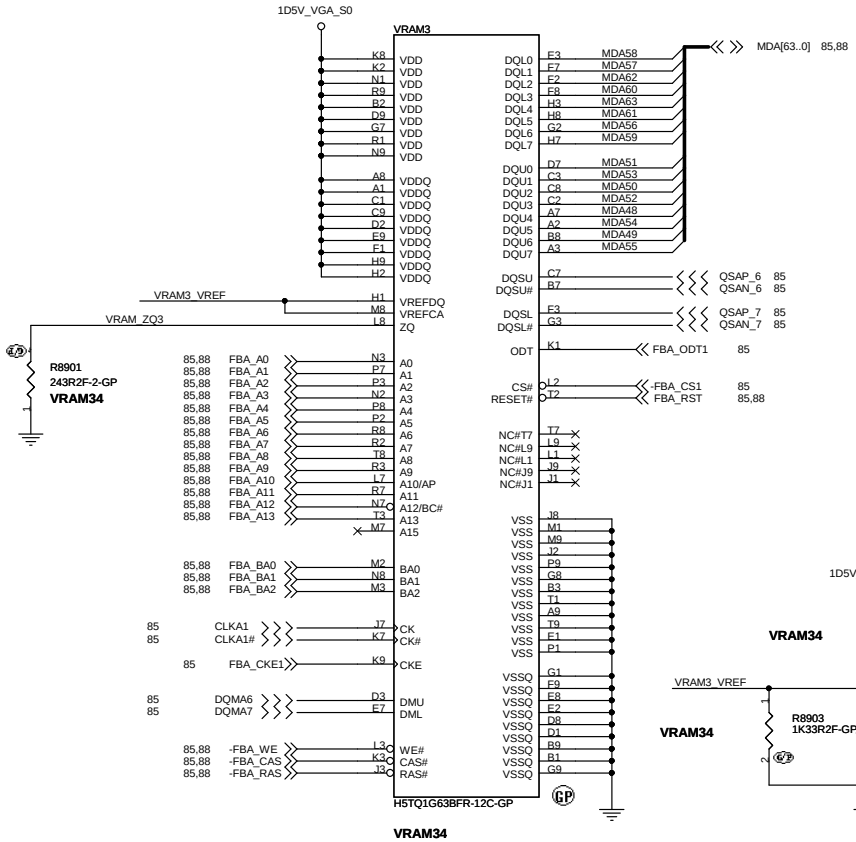
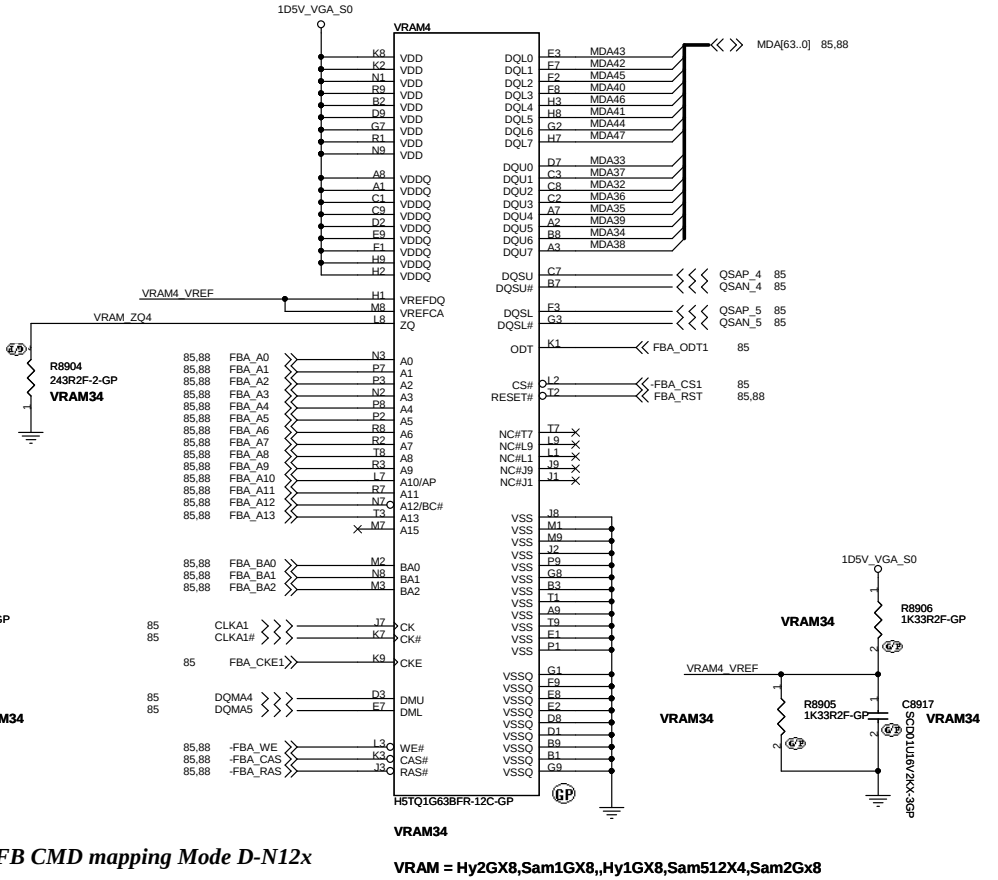
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 88 of 109





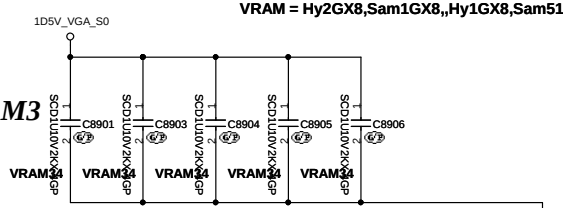
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

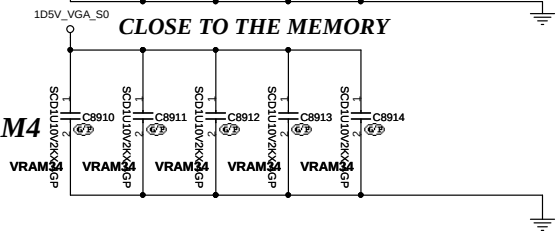
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

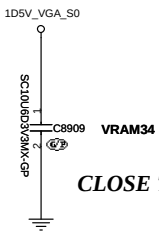
FOR VRAM3



CLOSE TO THE MEMORY

FOR VRAM4





CLOSE TO THE MEMORY

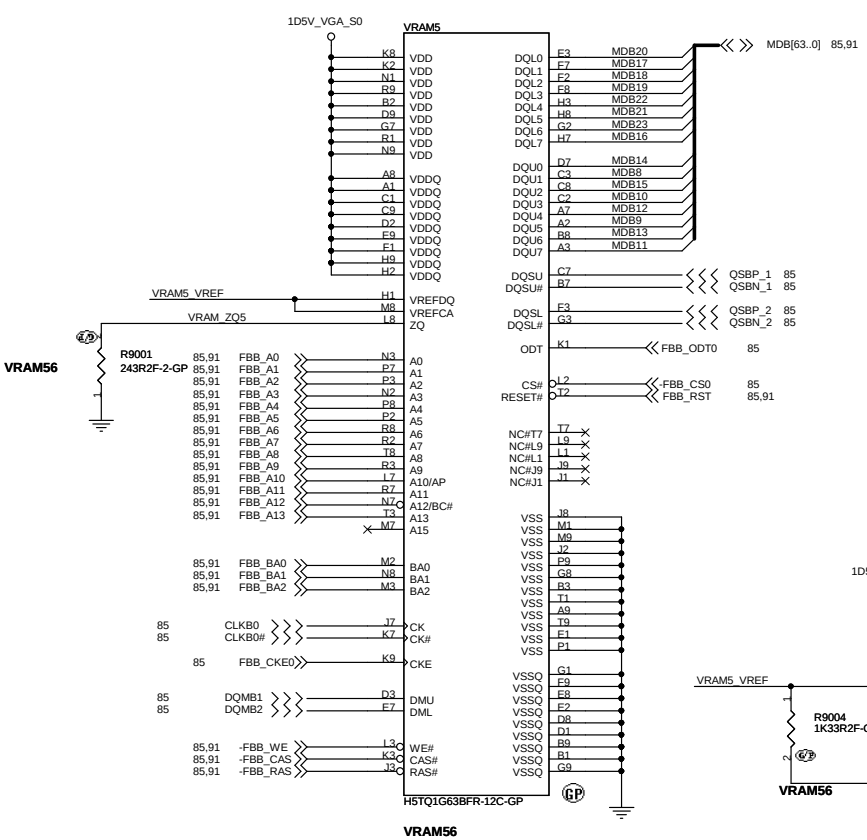
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

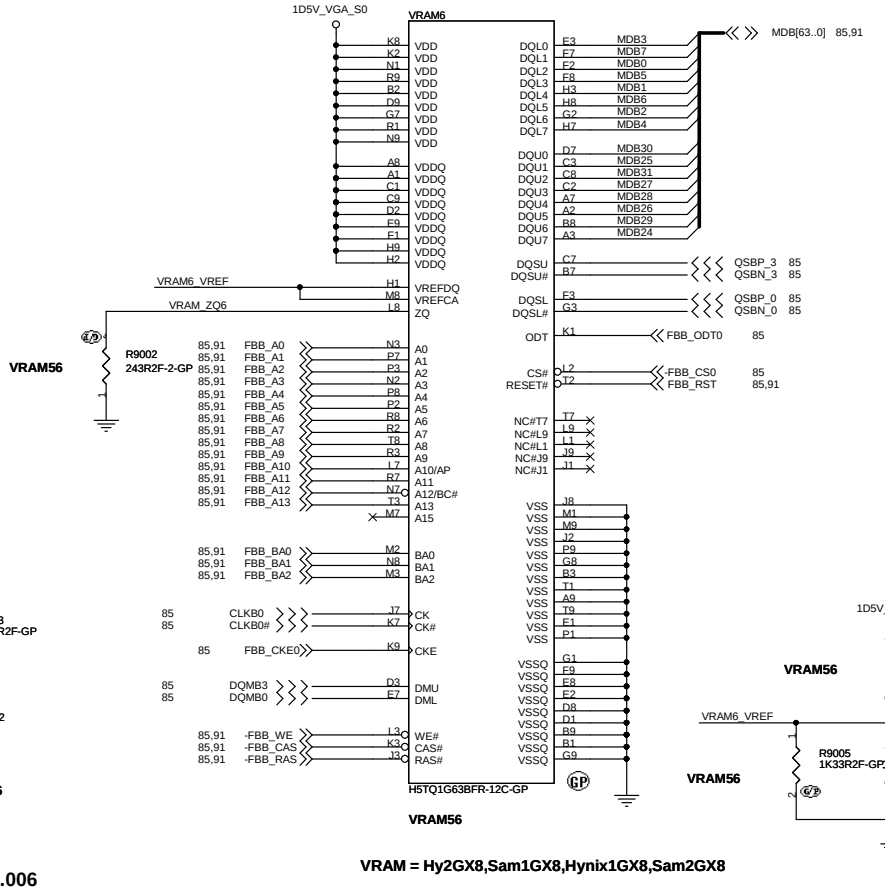
Title: ***GPU-VRAM3,4 (2/4)***

Size	Document Number	Rev
Custom	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 89 of 109

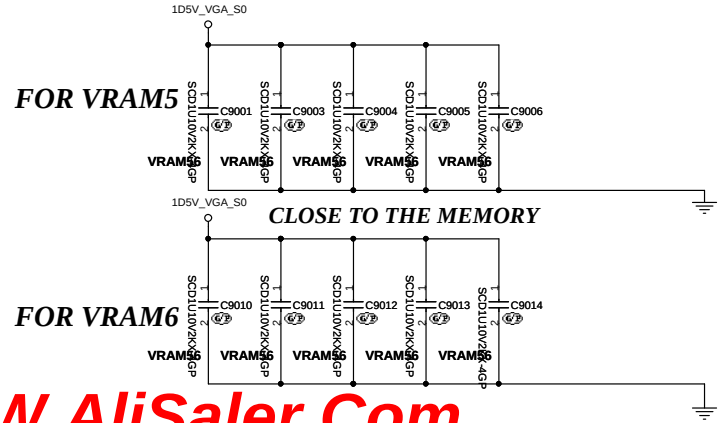


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

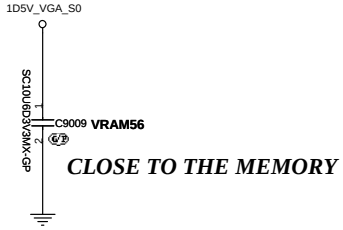


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



D12G

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: Custom | Document Number: BA40-HR | Rev: SD

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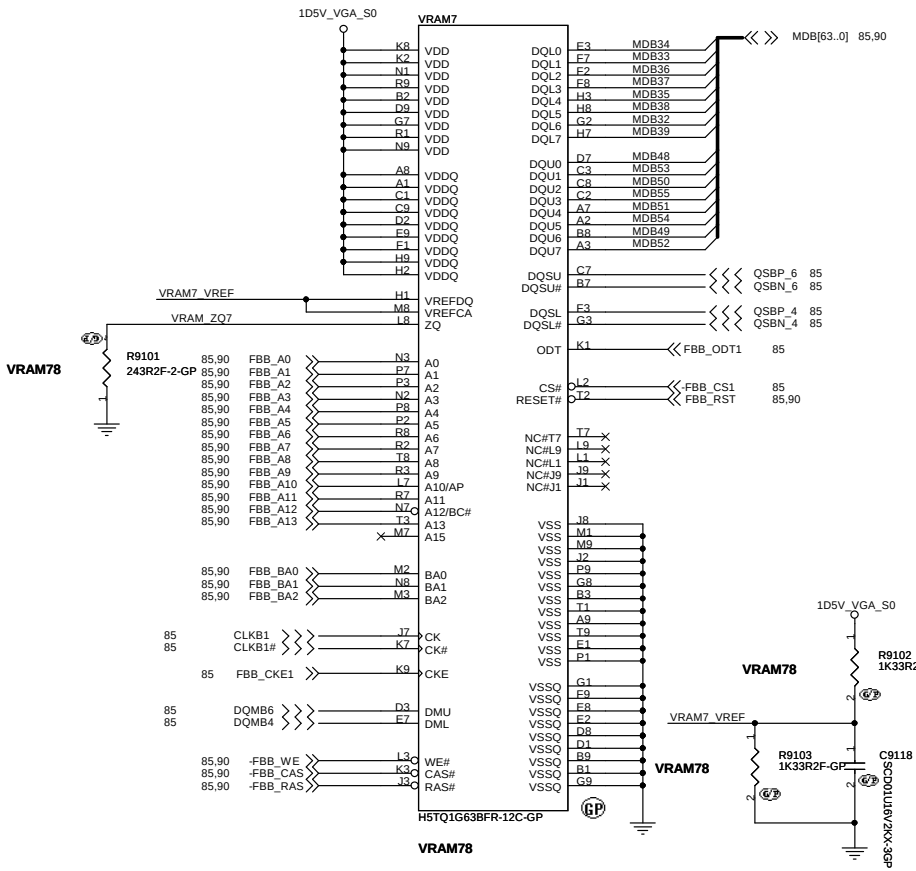
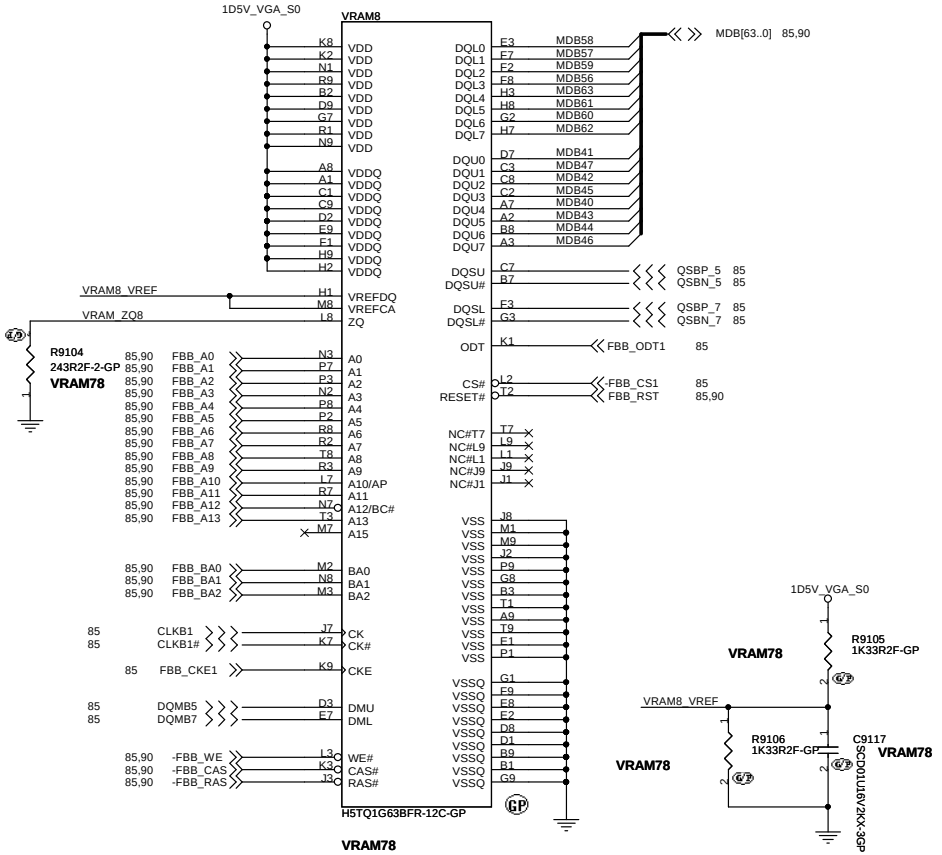




VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

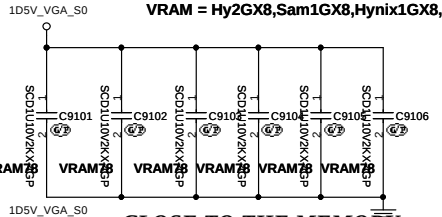
VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006

VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005

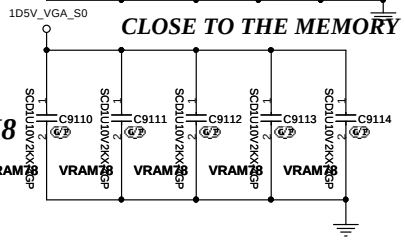
VRAM HYNIX 2Gb VR.2GB0G.001

FOR VRAM7

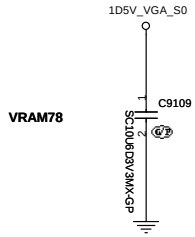


CLOSE TO THE MEMORY

FOR VRAM8



CLOSE TO THE MEMORY



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM7,8 (4/4)***

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Custom	BA40-HR	SD

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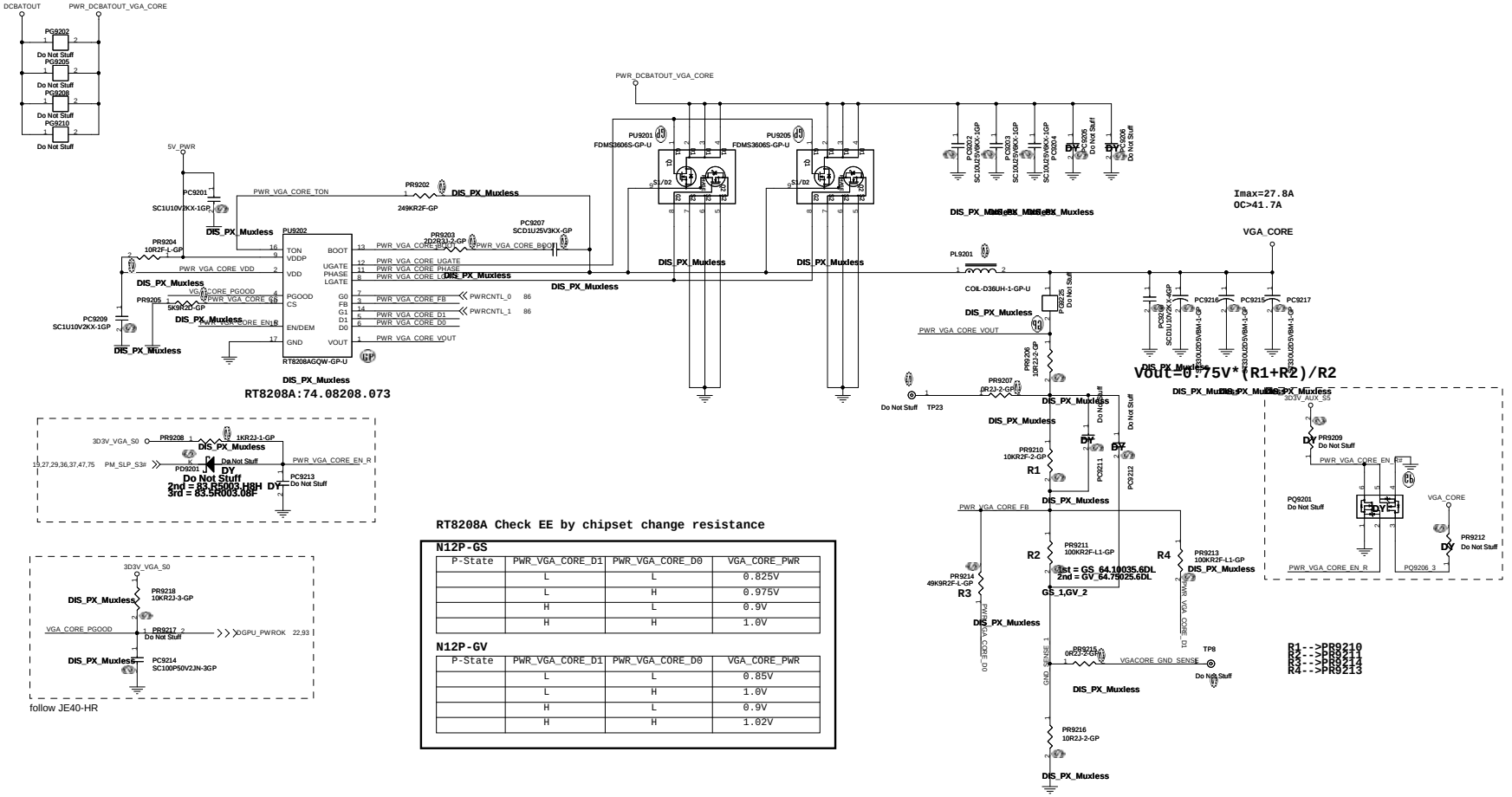

follow JE40-HR

RT8208A:74.08208.073

RT8208A Check EE by chipset change resistance

N12P-GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.825V
	L	H	0.975V
	H	L	0.9V
	H	H	1.0V

N12P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.85V
	L	H	1.0V
	H	L	0.9V
	H	H	1.02V

Frequency setting
470K --->165KHz
200K --->323KHz
100K --->500KHz

D12G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size: A2 | Document Number: BA40/50-HR | Rev: SD

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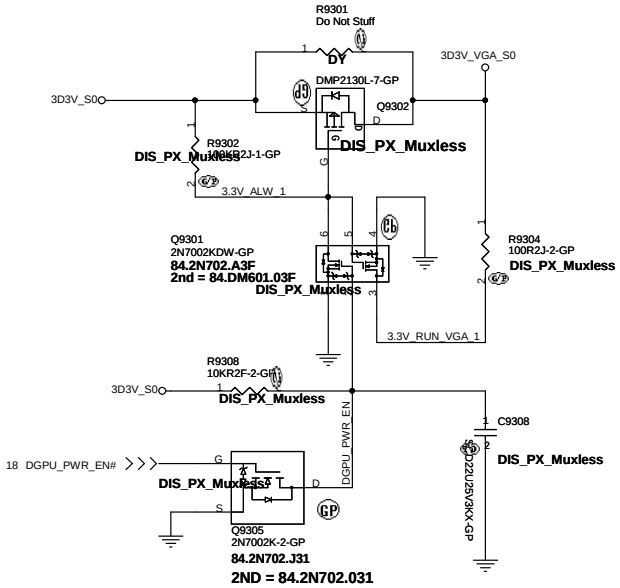
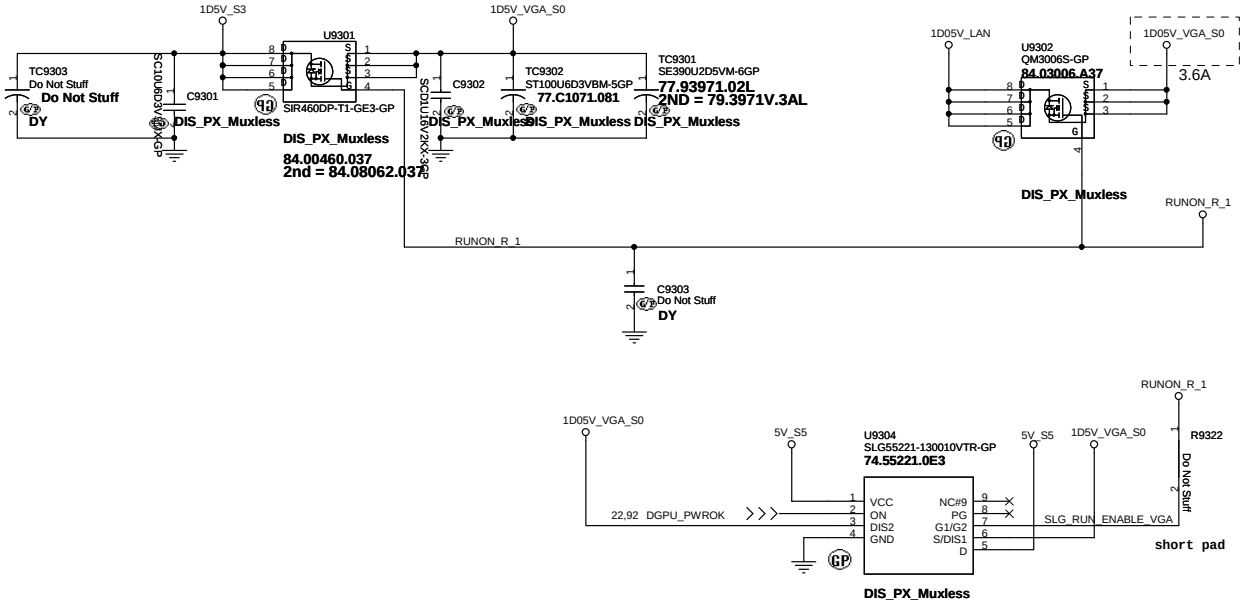
+3VS to 3.3V_DELAY Transfer

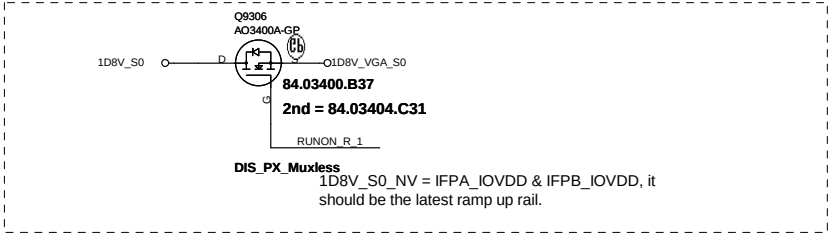


1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

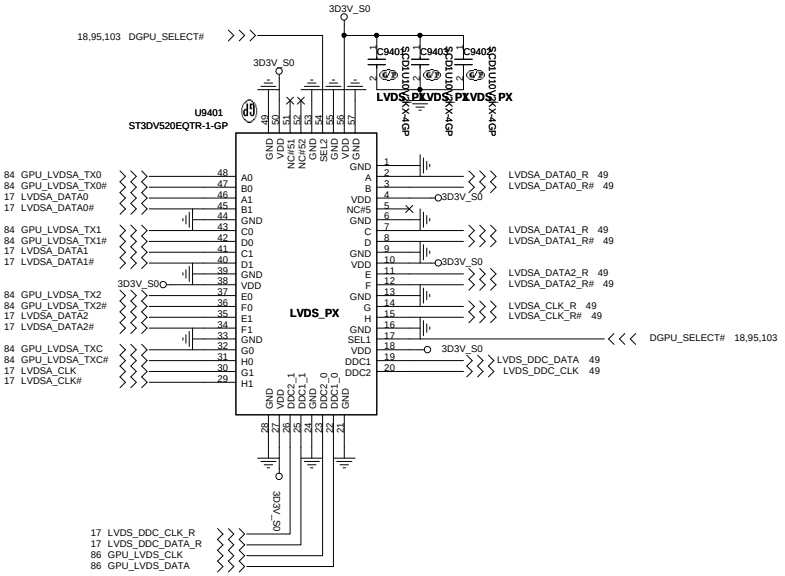


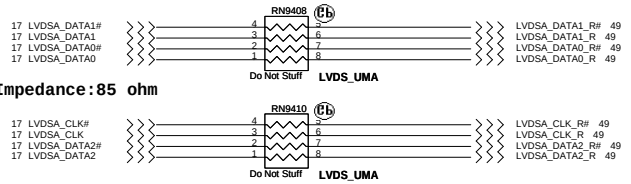


D12G

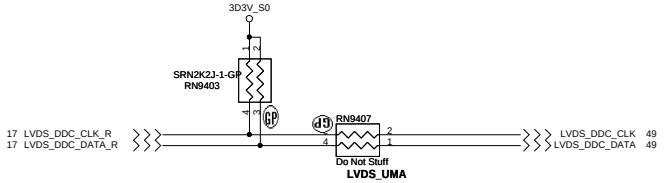
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DISCRETE VGA POWER***
Size: Custom	Document Number: **BA40-HR** Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 93 of 109

LVDS



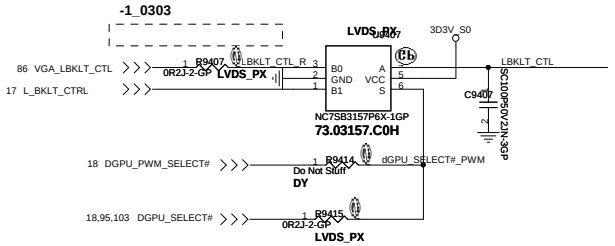


Impedance:85 ohm

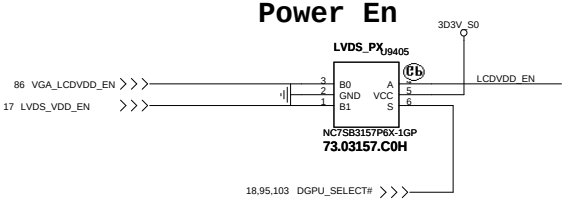


SEL->L(X=nX0),H(X=nX1)
SEL1 Control A~H
SEL2 Control DDC1,DDC2

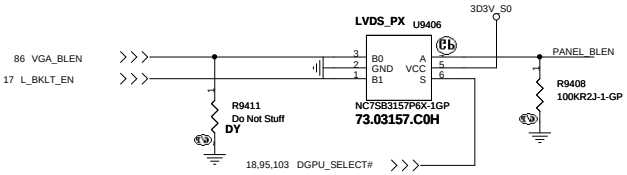
Panel BL brightness



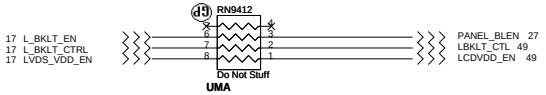
Power En



BL En



Panel BL brightness/Power En/BL En

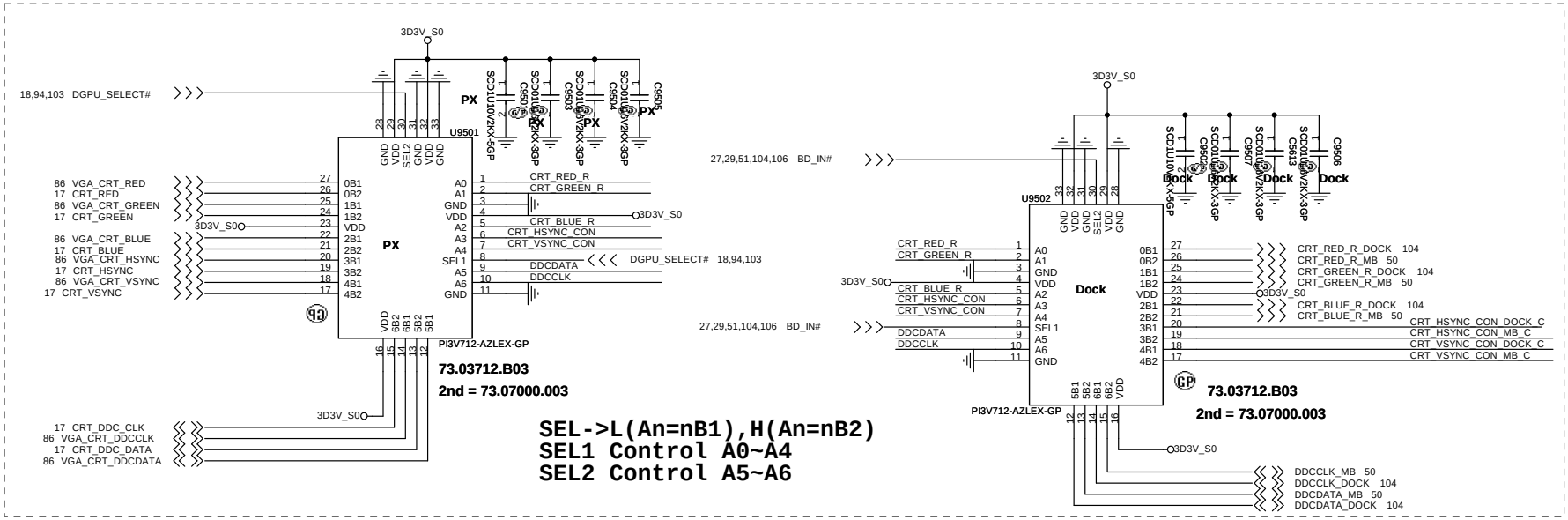


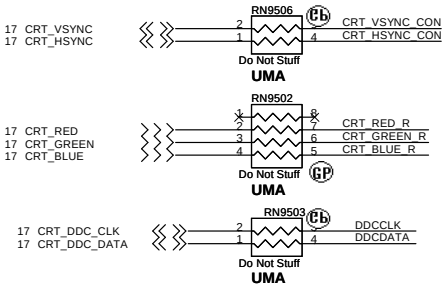
D12G

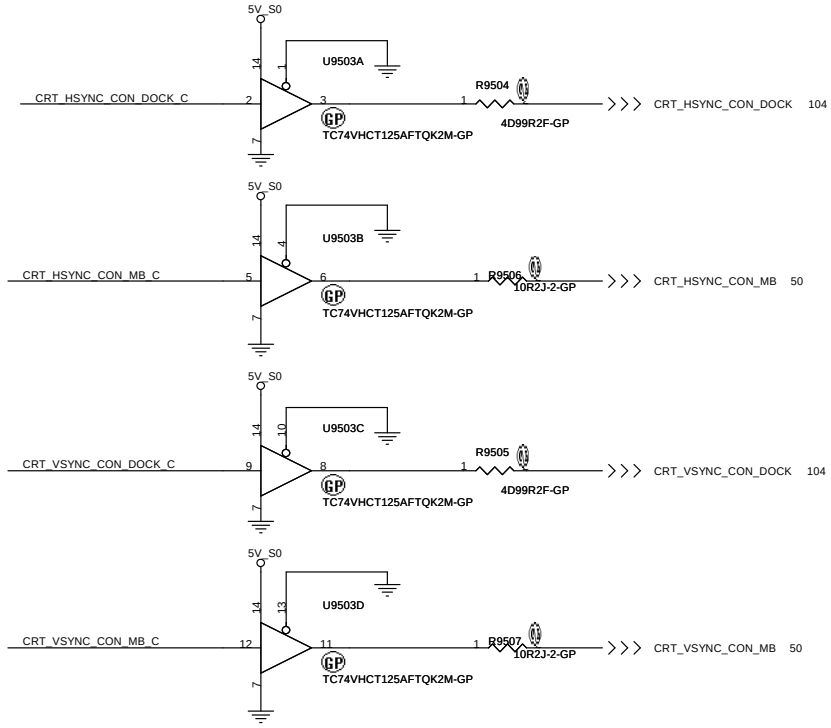
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LVDS_Switch	
Size: Custom	Document Number: BAD50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 94 of 109	

CRT DDCDATA & DDCCLK

VDD :
Recommend to use 6 caps (0.1u + 5*10nF) close to our chips







D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT_Switch***	
Size A3	Document Number **Huron River**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 95 of 109	

SSID = SDIO

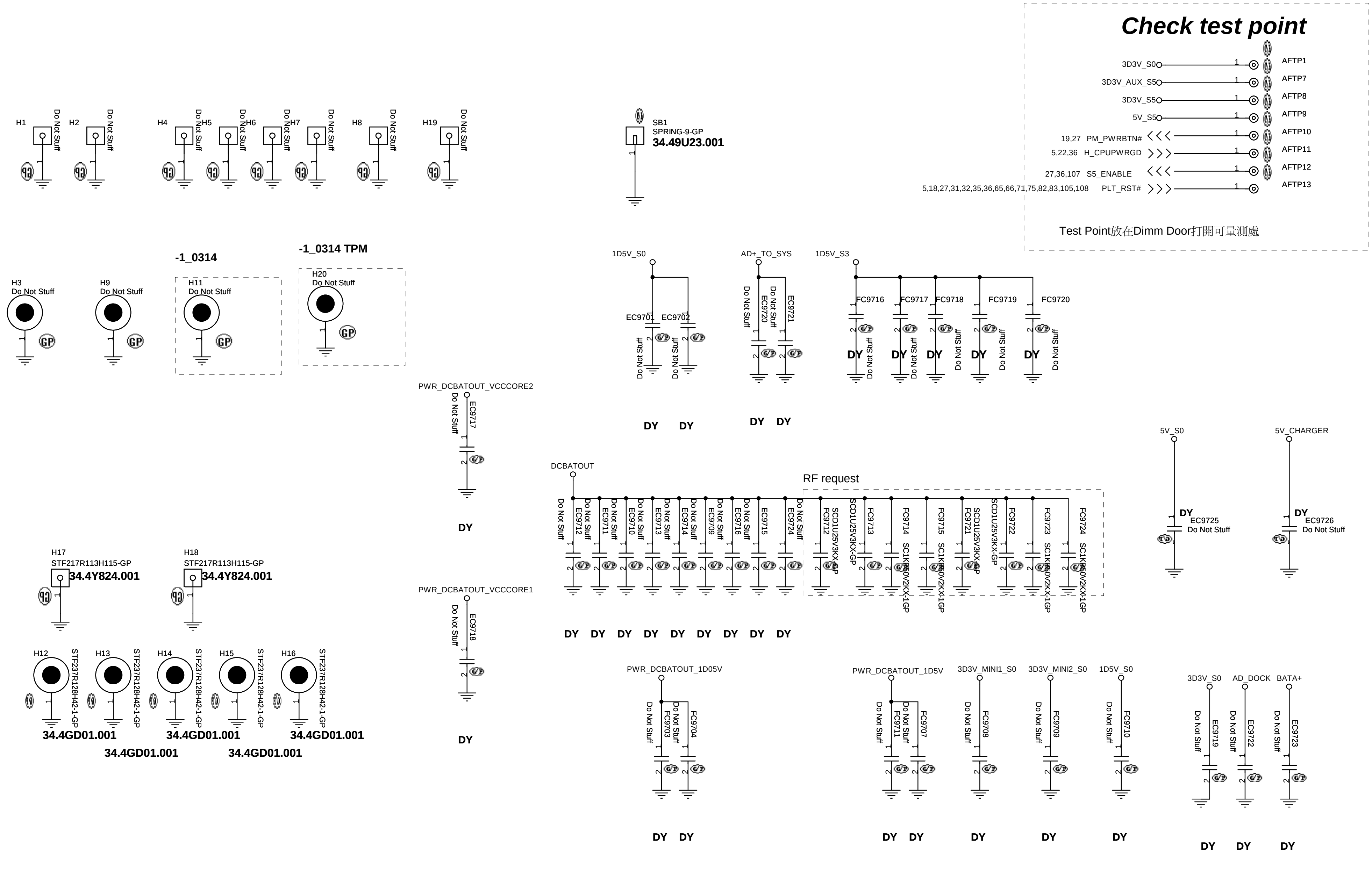
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size	Document Number	Rev
A2	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 96 of 109



Check test point
3D3V_S0
AFTP1
3D3V_AUX_S5
AFTP7
3D3V_S5
AFTP8
5V_S5
AFTP9
19,27 PM_PWRBTN#
AFTP10
5,22,36 H_CPUPWRGD
AFTP11
27,36,107 S5_ENABLE
AFTP12
5,18,27,31,32,35,36,65,66,71,75,82,83,105,108 PLT_RST#
AFTP13
Test Point放在Dimm Door打開可量測處
SB1
SPRING-9-GP
34.49U23.001
H1 Do Not Stuff
H2 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff
H19 Do Not Stuff
-1_0314
-1_0314 TPM
H3 Do Not Stuff
H9 Do Not Stuff
H11 Do Not Stuff
H20 Do Not Stuff
1D5V_S0
AD+_TO_SYS
1D5V_S3
EC9701
EC9702
EC9720
EC9721
FC9716
FC9717
FC9718
FC9719
FC9720
PWR_DCBATOUT_VCCCORE2
EC9717
DCBATOUT
RF request
EC9712
EC9711
EC9710
EC9713
EC9714
EC9709
EC9716
EC9715
EC9724
FC9712
SCD1U25V3KX-GP
FC9713
FC9714
SC1KP50V2KX-1GP
FC9715
FC9721
FC9722
FC9723
FC9724
5V_S0
5V_CHARGER
EC9725 Do Not Stuff
EC9726 Do Not Stuff
H17
STF217R113H115-GP
34.4Y824.001
H18
STF217R113H115-GP
34.4Y824.001
PWR_DCBATOUT_VCCCORE1
EC9718
H12
H13
H14
H15
H16
STF237R128H42-1-GP
34.4GD01.001
PWR_DCBATOUT_1D05V
FC9703
FC9704
PWR_DCBATOUT_1D5V
FC9711
FC9707
3D3V_MINI1_S0
FC9708
3D3V_MINI2_S0
FC9709
1D5V_S0
FC9710
3D3V_S0
EC9719
AD_DOCK
EC9722
BATA+
EC9723
Do Not Stuff
DY

D12G

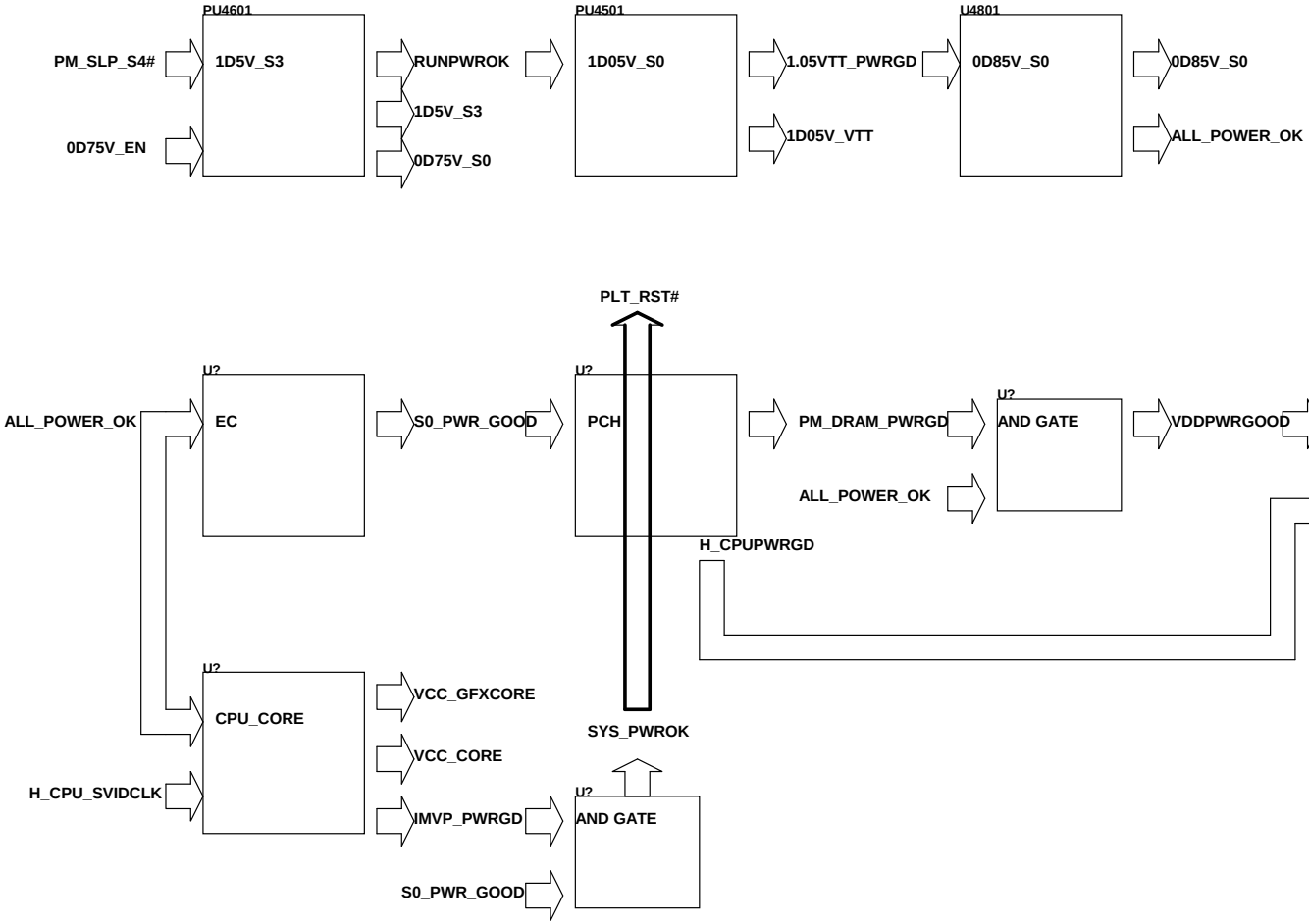
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size: A3 | Document Number: **BA40-HR** | Rev: **SD**

Date: Thursday, April 07, 2011 | Sheet 97 of 109

Power Sequence



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

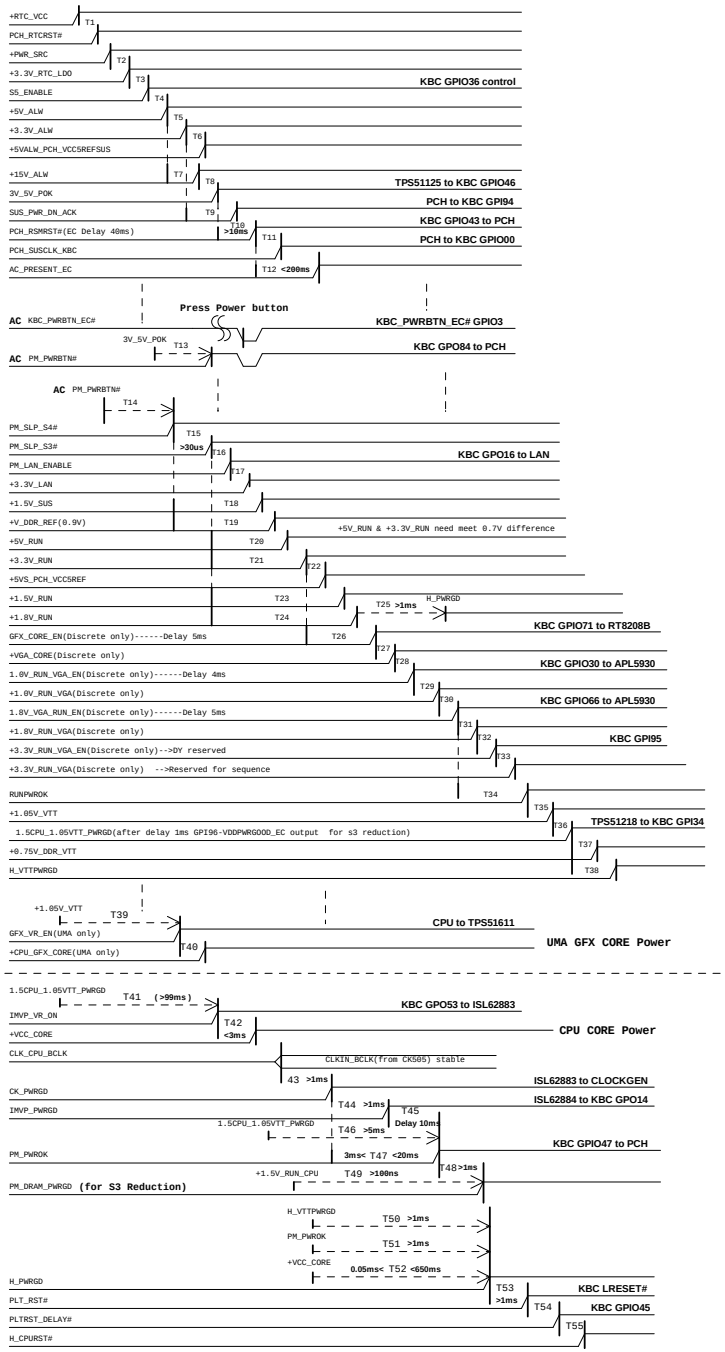
Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 98 of 109

Intel-Power Up Sequence

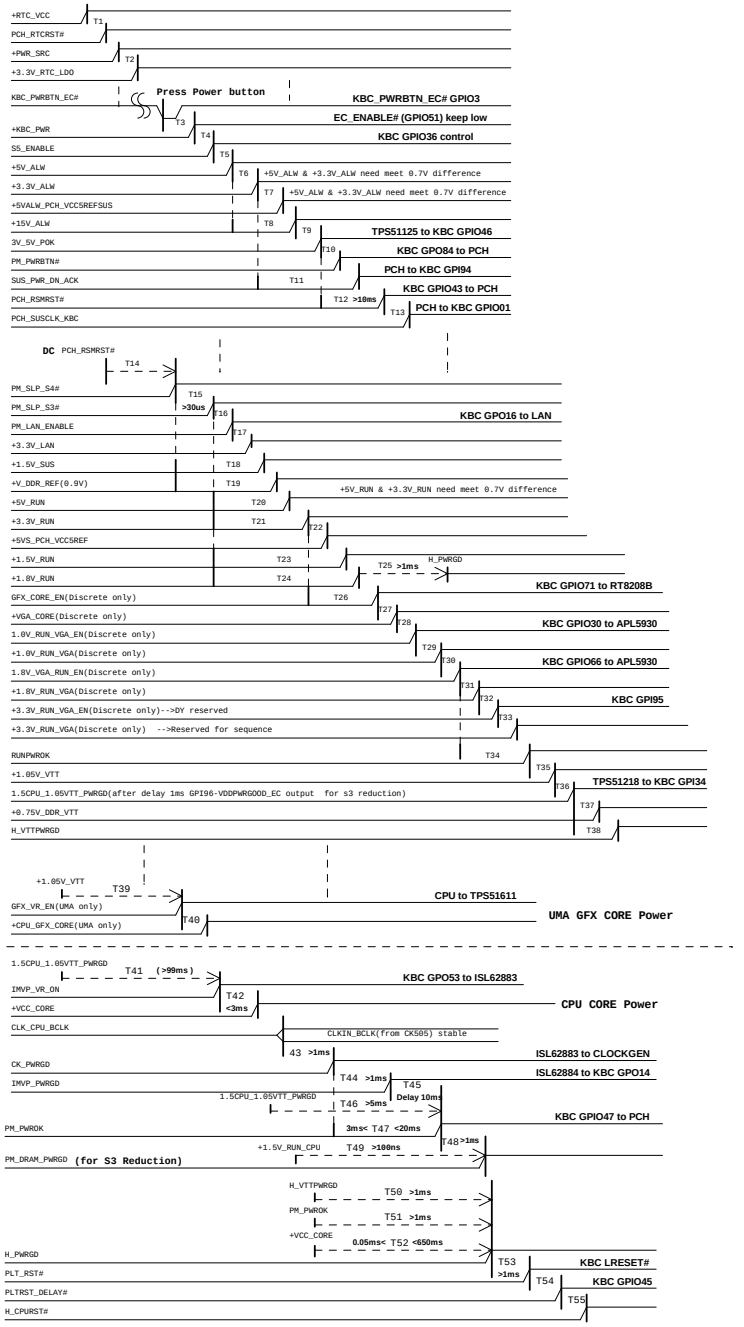
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



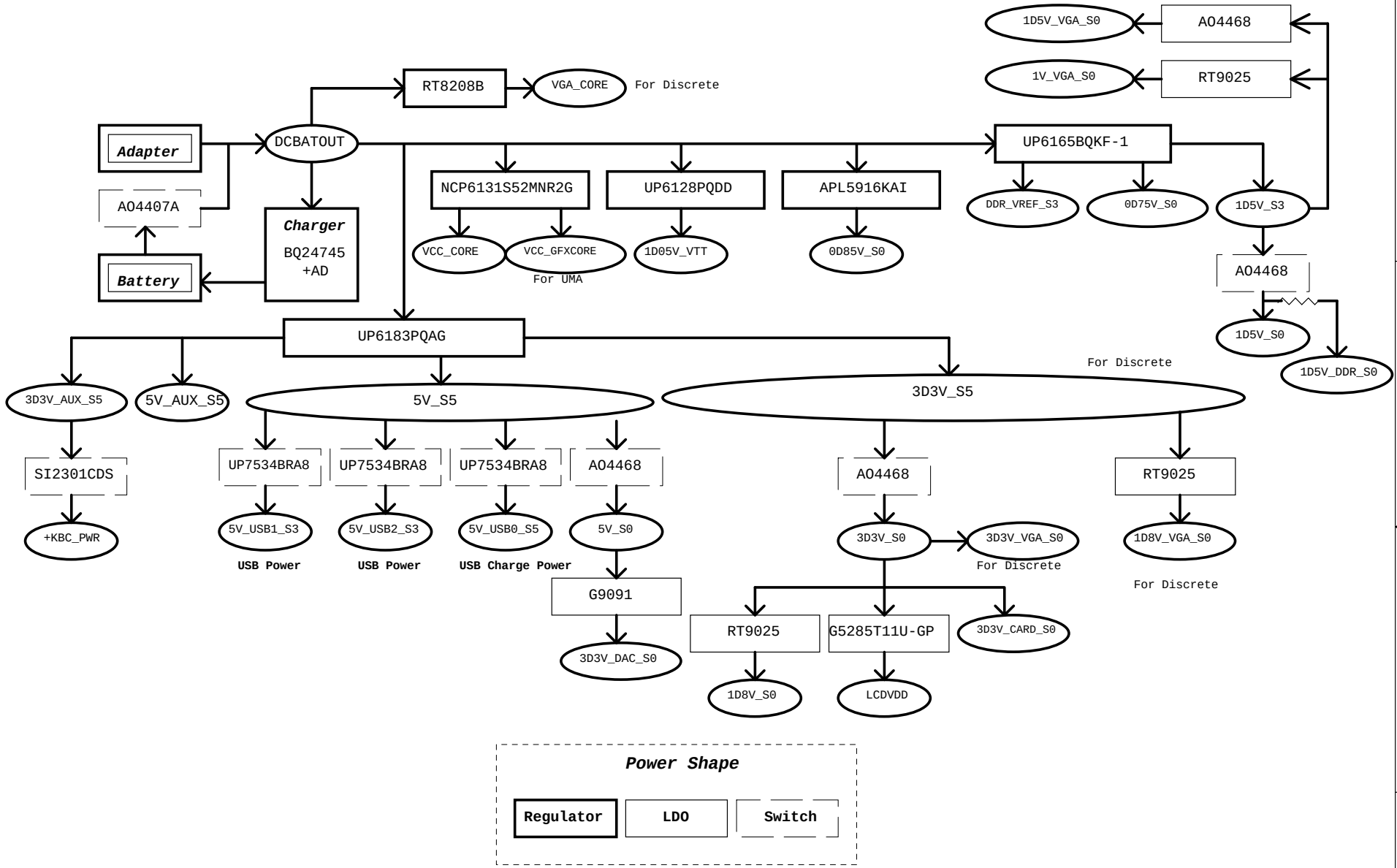
DIGG

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 01, 2010 | Sheet 39 of 50



D12G

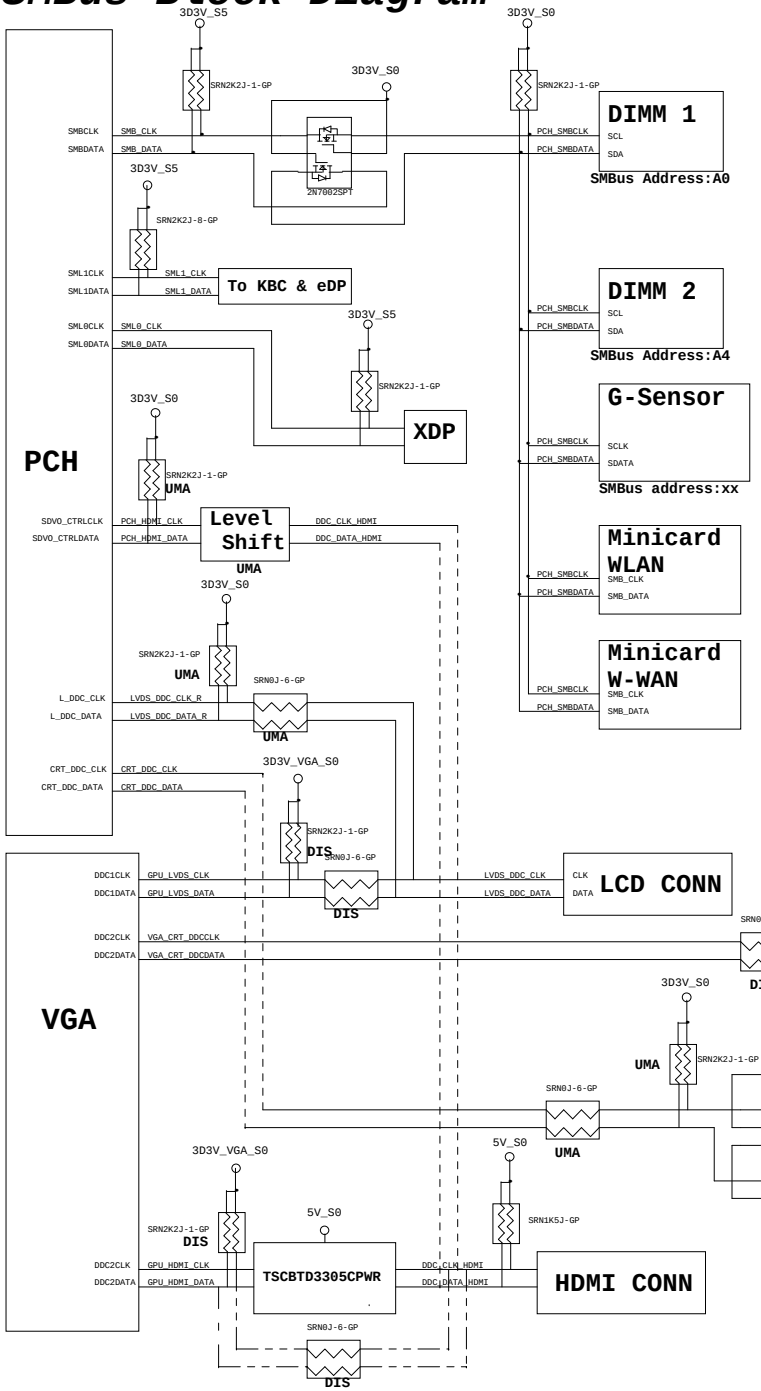
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

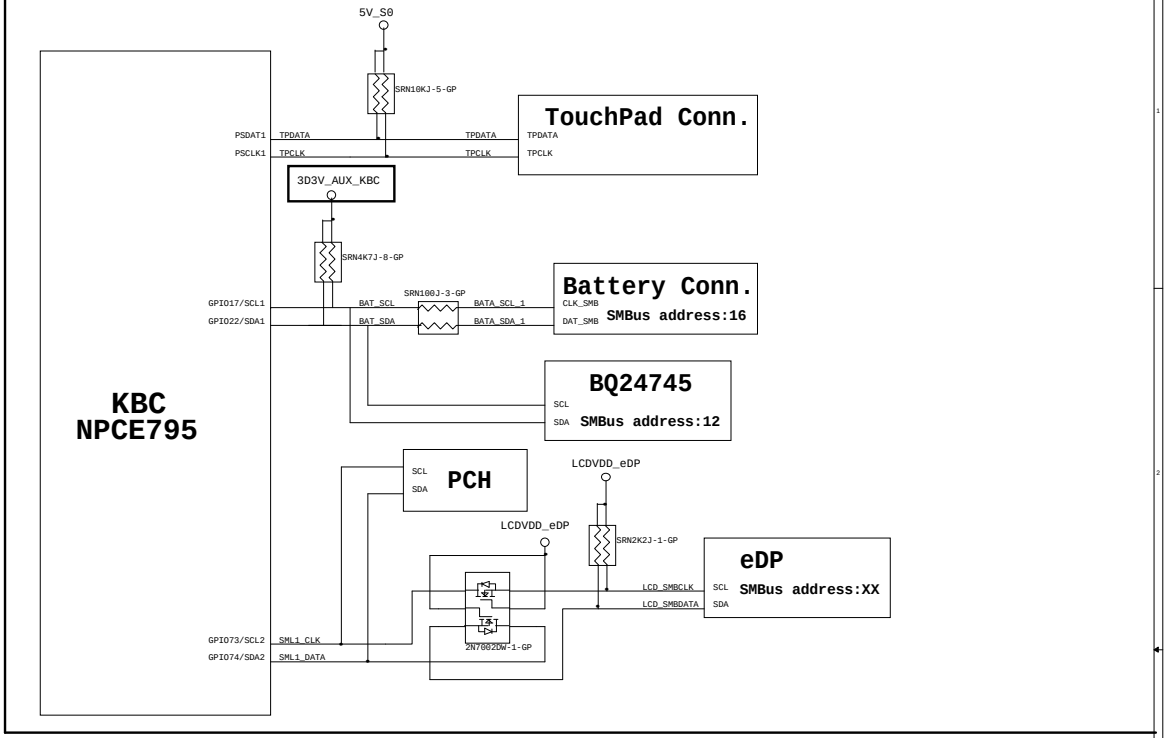
Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 100 of 109

PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA

D12G

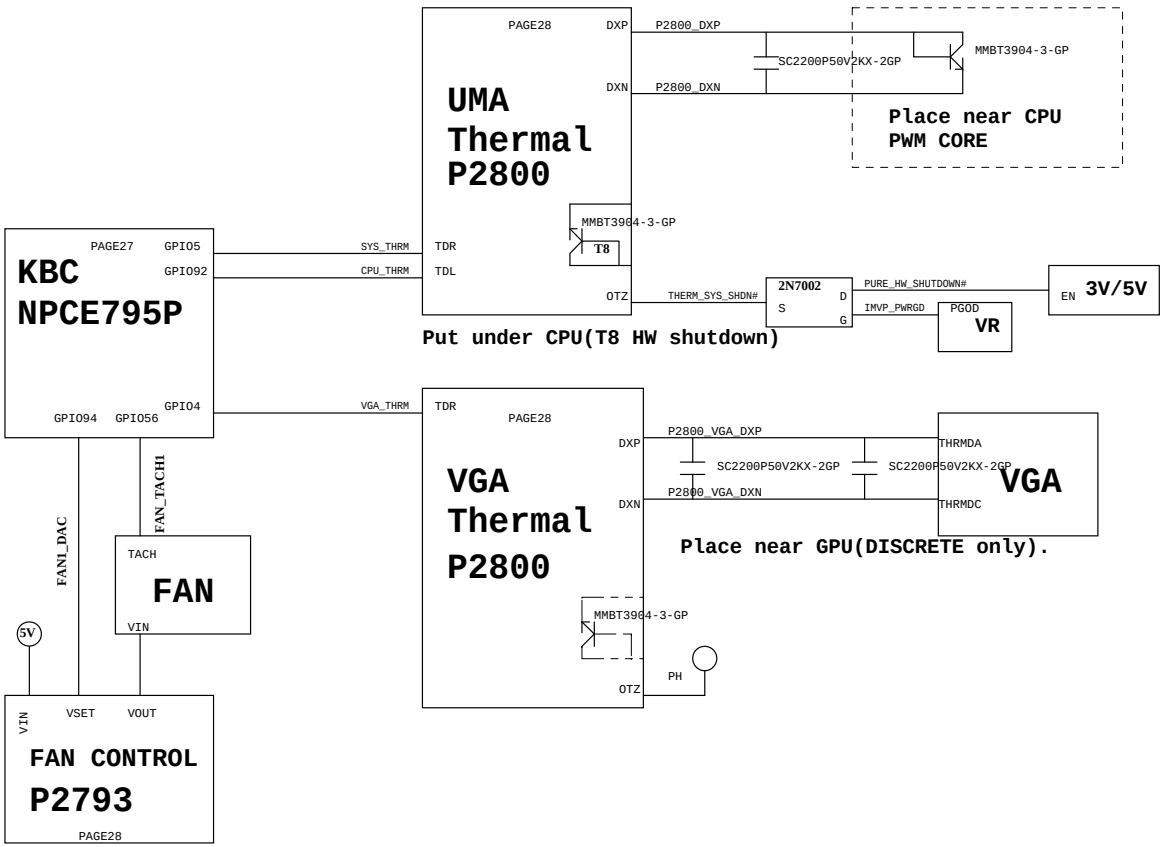
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

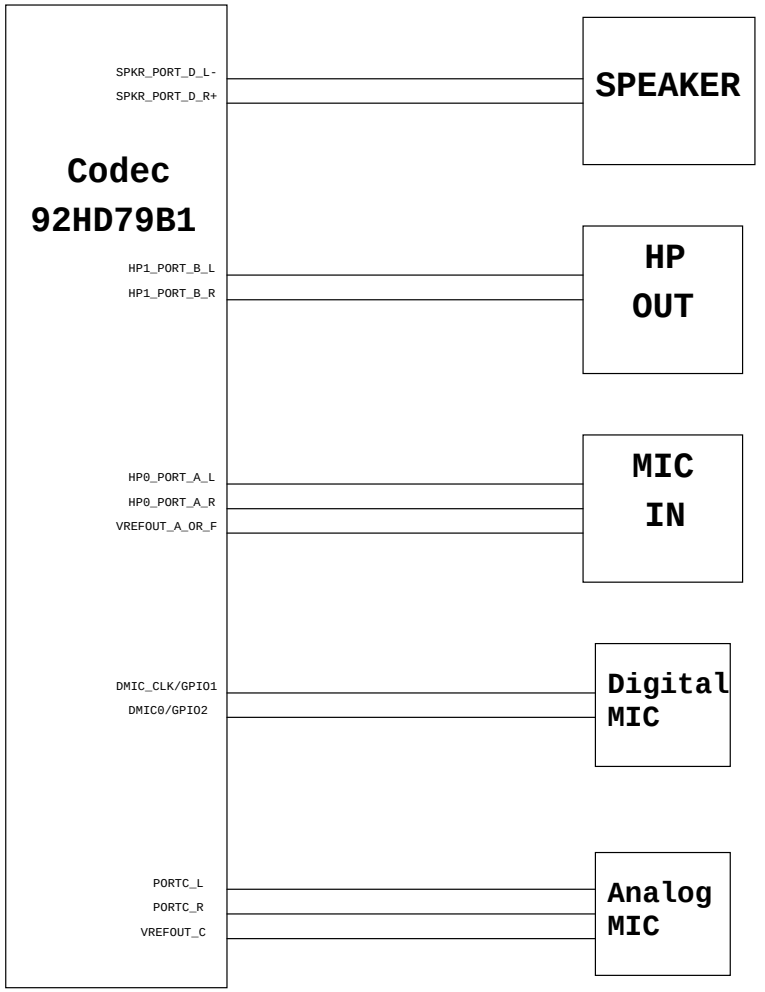
Size	Document Number	Rev
A2	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 101 of 109

Thermal Block Diagram



Audio Block Diagram



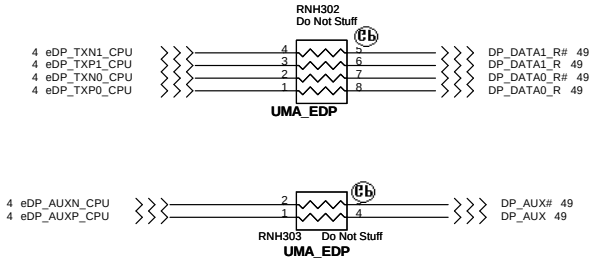
D12G

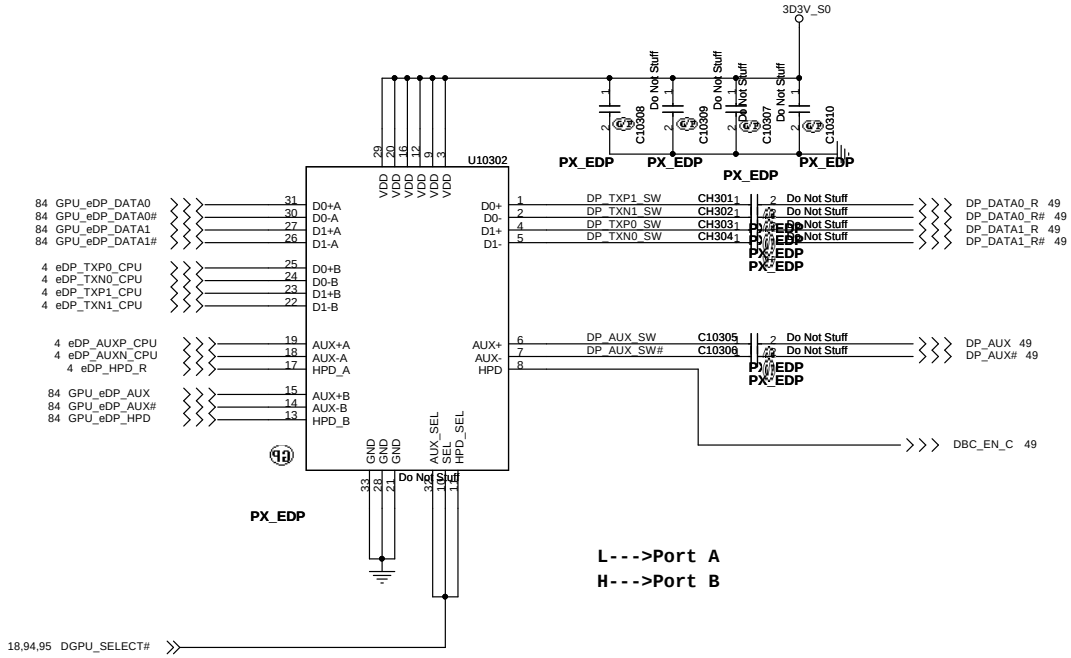
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

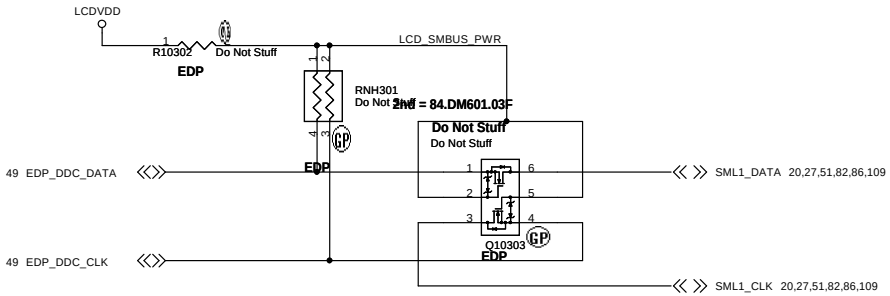
Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 102 of 109







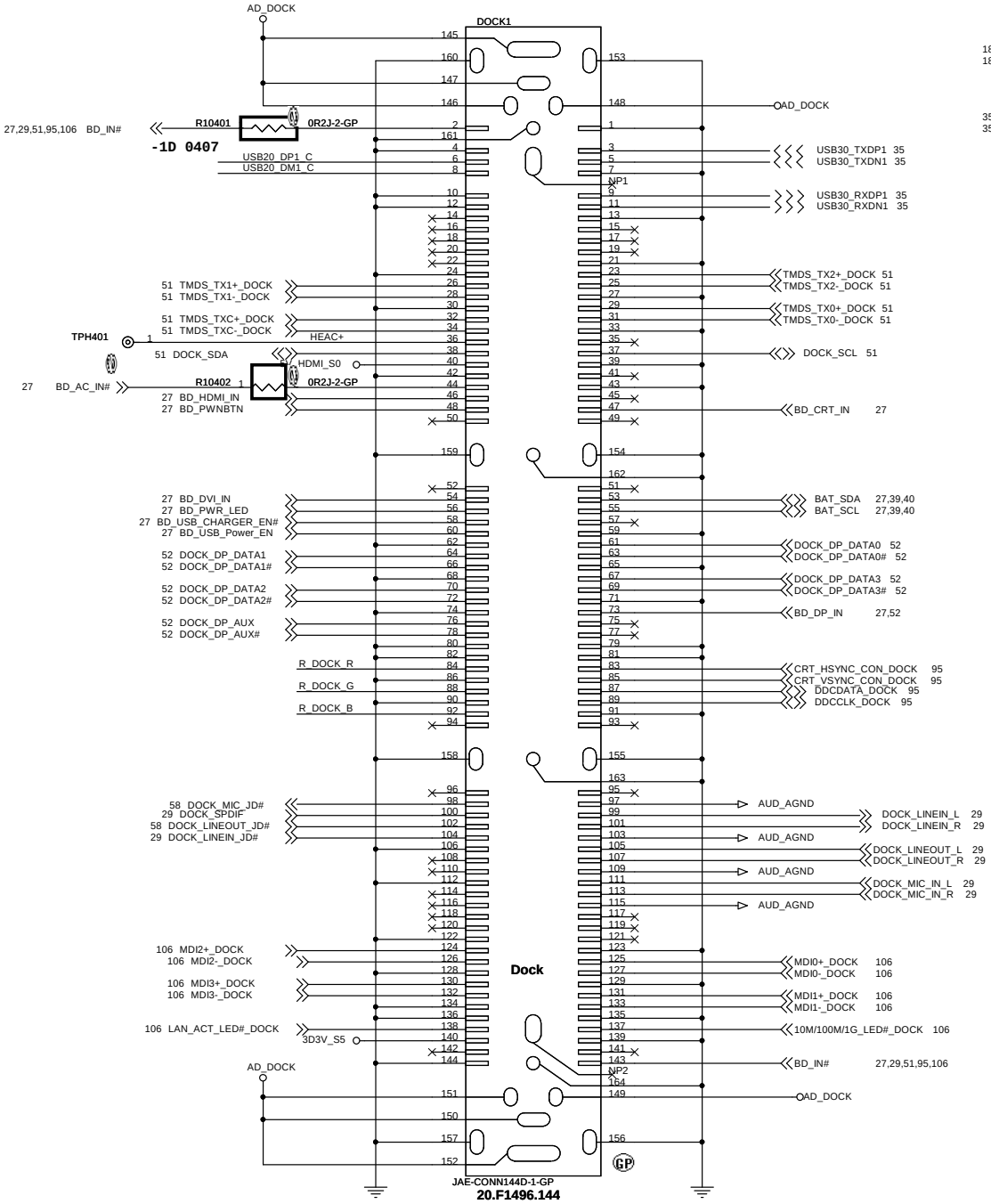
D12G

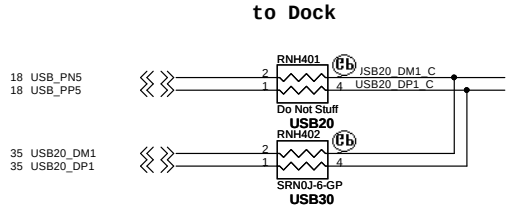
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

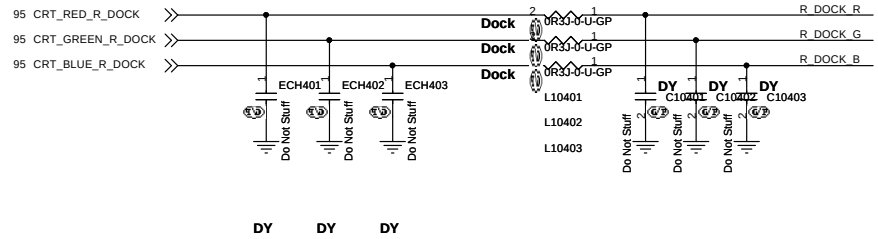
Title: Switch GFX DP

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 103 of 109







D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BOTTOM DOCKING

Size	Document Number	Rev
A3	BA40-HR	SD

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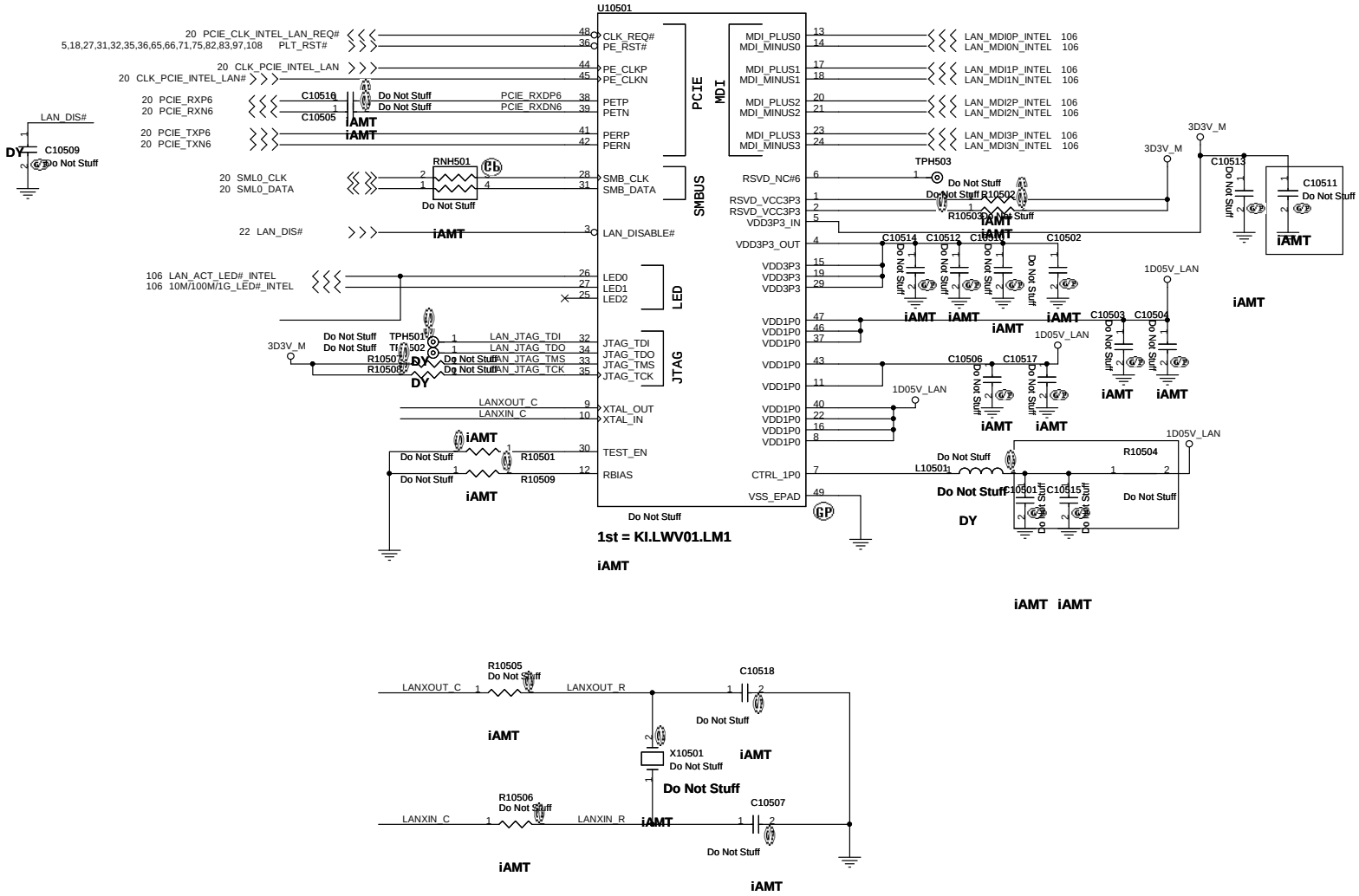
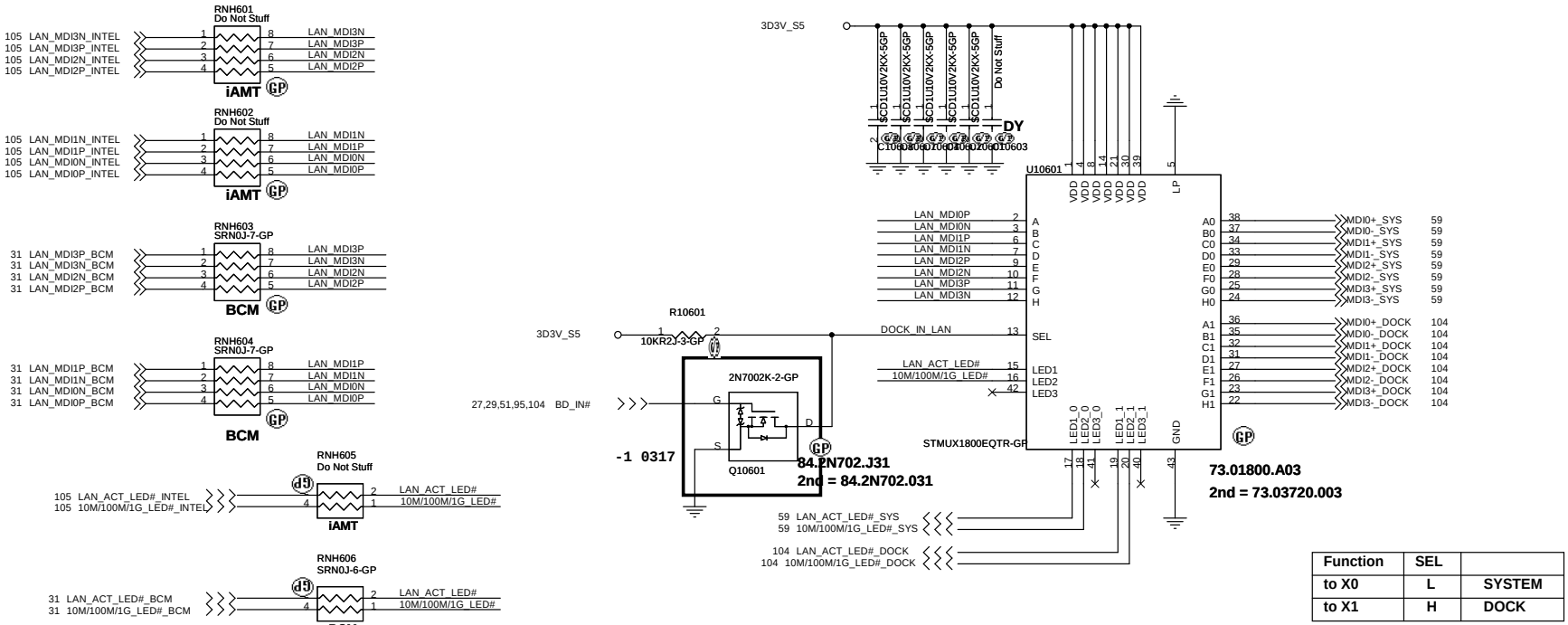


D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN INTEL 82579***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 105 of 109	

LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

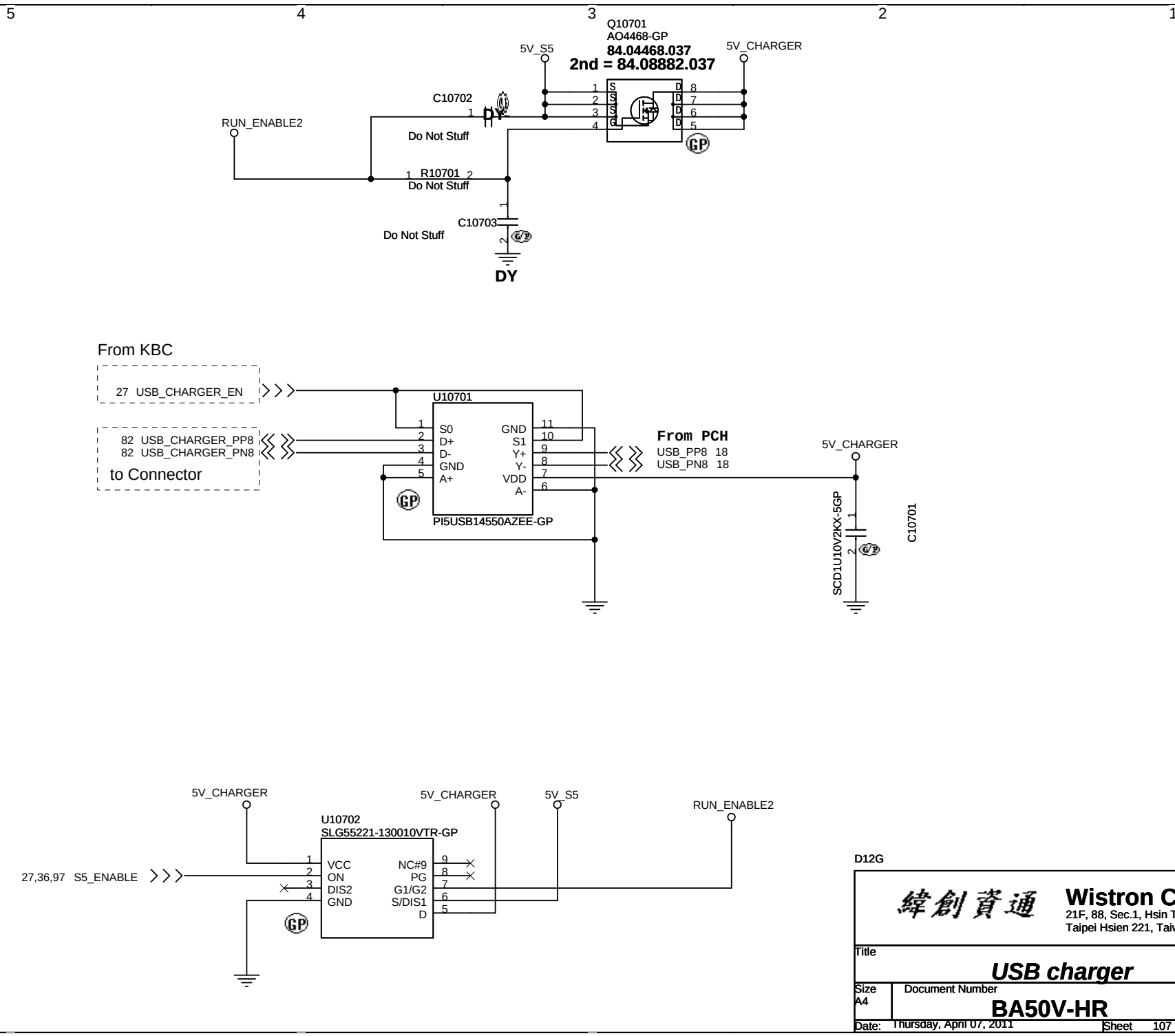
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN SWITCH

Size: A3 | Document Number: BAD50-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 106 of 109



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB charger

Size	Document Number	Rev
A4	**BA50V-HR**	**SD**

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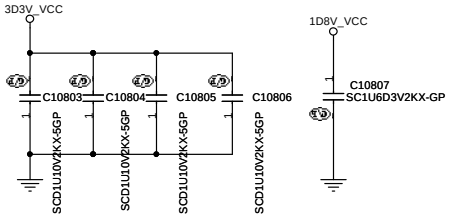
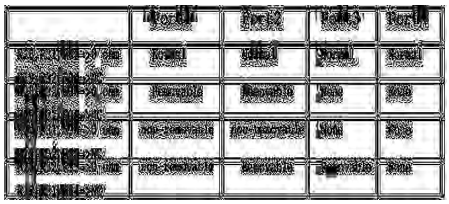
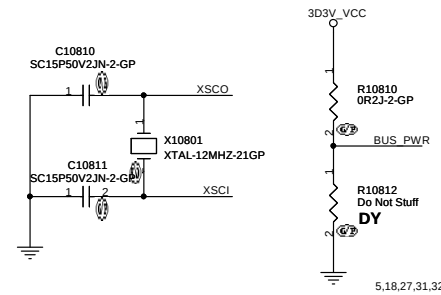
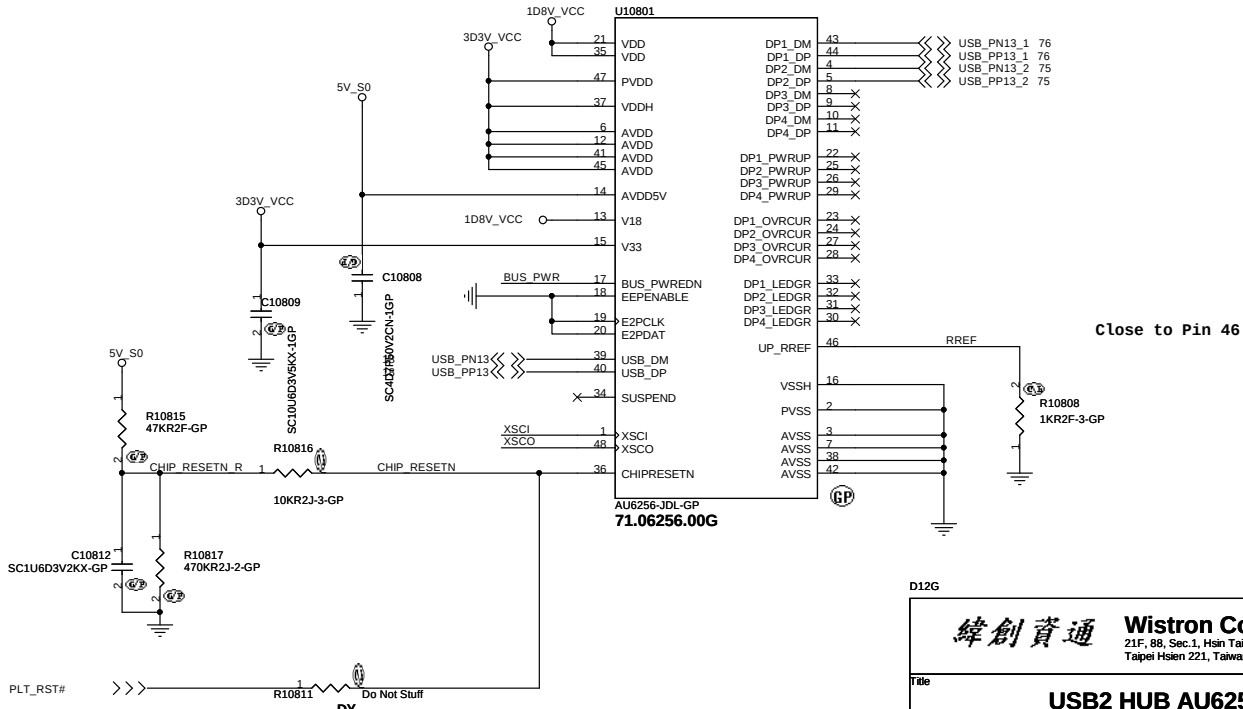




EEPENABLE
0 : Use Internal Rom
1 : Use External Rom





5,18,27,31,32,35,36,65,66,71,75,82,83,97,105 PLT_RST#

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2 HUB AU6256**

Size	Document Number	Rev
	BAD50-HR	SD

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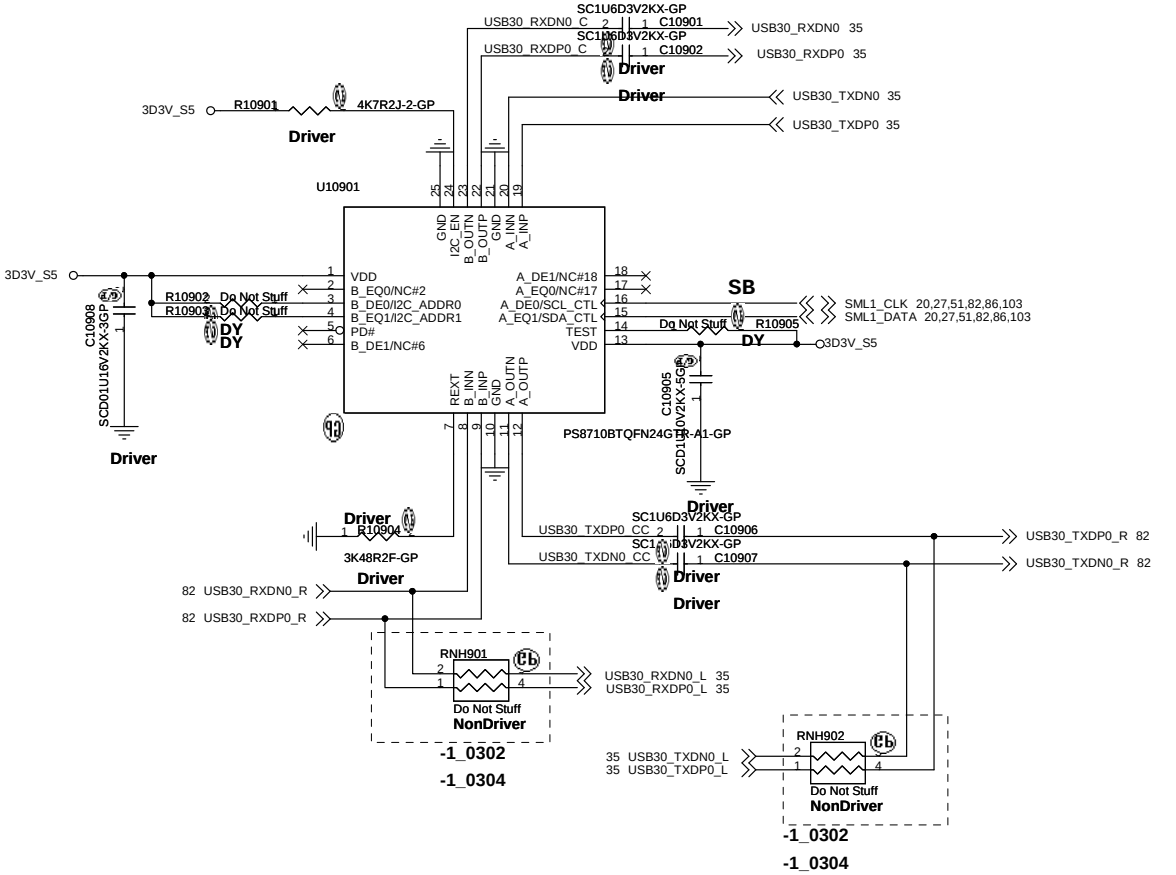
I2C mode
To USB BD



D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB30 re-driver***	
Size B	Document Number **BAD50-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 109 of 109	