Slinky
Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

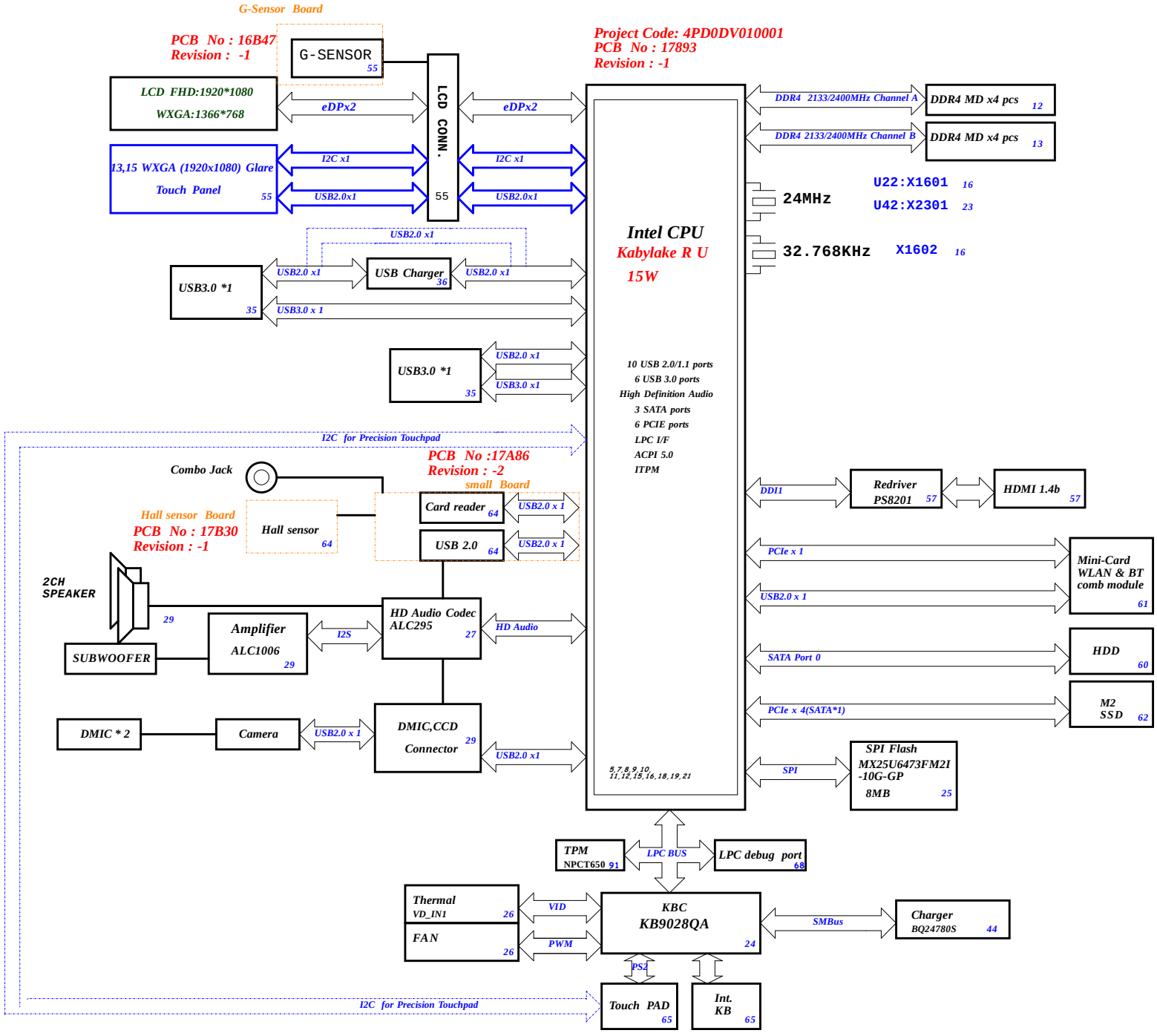
Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size	Document Number	Rev
A3	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 1 of 106



CHARGER BQ24780S	44
INPUTS	OUTPUTS
AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC RT6228	45
INPUTS	OUTPUTS
19V_DCBATOUT	5V_AUX_S5 5V_S5

SYSTEM DC/DC RT6226	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5

CPU DC/DC RT3602	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049	48
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCGT

CPU DC/DC RT9610B	50
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5388K1	51 52
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ
3D3V_S5	PWR_1D0V

SYSTEM DC/DC 9661-25ADJ	53
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM DC/DC S-1339D15	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM Load switch TPS22976	40
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939	40
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, October 19, 2017 Sheet 2 of 106

Main Func = CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU

HDMI

57 HDMI_DATA_CPU_N2
57 HDMI_DATA_CPU_P2
57 HDMI_DATA_CPU_N1
57 HDMI_DATA_CPU_P1
57 HDMI_DATA_CPU_N0
57 HDMI_DATA_CPU_P0
57 HDMI_DATA_CPU_N3
57 HDMI_DATA_CPU_P3

14,57 HDMI_CLK_CPU
14,57 HDMI_DATA_CPU

57 HDMI_DET_CPU

TYPEC

73 DP_DDI_TX_N0
73 DP_DDI_TX_P0
73 DP_DDI_TX_N1
73 DP_DDI_TX_P1
73 DP_DDI_TX_N2
73 DP_DDI_TX_P2
73 DP_DDI_TX_N3
73 DP_DDI_TX_P3

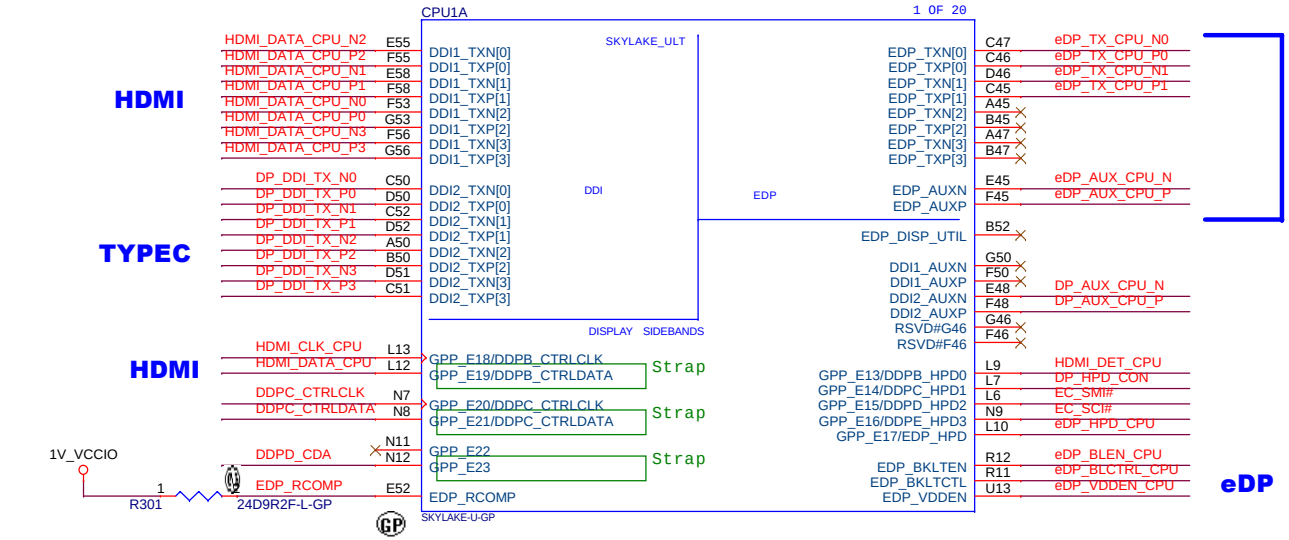
73 DP_AUX_CPU_N
73 DP_AUX_CPU_P

14 DDPC_CTRLDATA
73 DP_HPD_CON

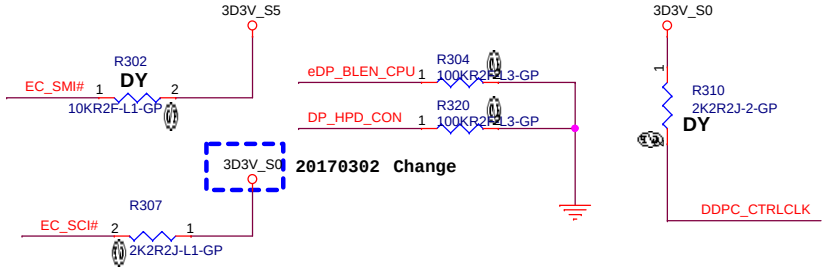
OTHER

14 DDPD_CDA

24 EC_SMI#
24 EC_SCI#



CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DISPLAY)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 3 of 106

Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU1B — 2 OF 20 — SKYLAKE_ULT

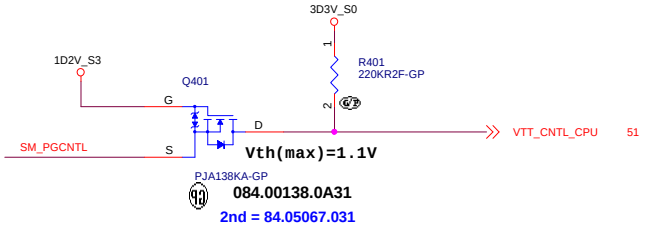
M_A_DQ[0:7]	M_A_DQ0	AL71	DDR0_DQ[0]	DDR0_CKN[0]	AU53	M_A_CLK#0	A-CLK
	M_A_DQ1	AL68	DDR0_DQ[1]	DDR0_CKP[0]	AT53	M_A_CLK0	
	M_A_DQ2	AN68	DDR0_DQ[2]	DDR0_CKN[1]	AU55		
	M_A_DQ3	AN69	DDR0_DQ[3]	DDR0_CKP[1]	AT55		
	M_A_DQ4	AL70	DDR0_DQ[4]				
	M_A_DQ5	AL69	DDR0_DQ[5]	DDR0_CKE[0]	BA56	M_A_CKE0	A-CTRL-CKE
	M_A_DQ6	AN70	DDR0_DQ[6]	DDR0_CKE[1]	BB56		
	M_A_DQ7	AN71	DDR0_DQ[7]	DDR0_CKE[2]	AW56		
M_A_DQ[8:15]	M_A_DQ8	AR70	DDR0_DQ[8]	DDR0_CKE[3]	AY56		
	M_A_DQ9	AR68	DDR0_DQ[9]				
	M_A_DQ10	AU71	DDR0_DQ[10]	DDR0_CS#[0]	AU45	M_A_CS#0	A-CTRL-CS
	M_A_DQ11	AU68	DDR0_DQ[11]	DDR0_CS#[1]	AU43		
	M_A_DQ12	AR71	DDR0_DQ[12]	DDR0_ODT[0]	AT45	M_A_ODT0	A-CTRL-ODT
	M_A_DQ13	AR69	DDR0_DQ[13]	DDR0_ODT[1]	AT43		
	M_A_DQ14	AU70	DDR0_DQ[14]				
	M_A_DQ15	AU69	DDR0_DQ[15]				
M_A_DQ[16:23]	M_A_DQ16	AF65	DDR1_DQ[0]/DDR0_DQ[16]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BA51	M_A_A5	A-CMD-MA
	M_A_DQ17	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BB54	M_A_A9	
	M_A_DQ18	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	BA52	M_A_A6	
	M_A_DQ19	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AY52	M_A_A8	
	M_A_DQ20	AF66	DDR1_DQ[4]/DDR0_DQ[20]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AW52	M_A_A7	
	M_A_DQ21	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AY55	M_A_BG0	
	M_A_DQ22	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AW54	M_A_A12	A-CMD-MA
	M_A_DQ23	AK66	DDR1_DQ[7]/DDR0_DQ[23]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA54	M_A_A11	
M_A_DQ[24:31]	M_A_DQ24	AF70	DDR1_DQ[8]/DDR0_DQ[24]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	BA55	M_A_ACT_N	
	M_A_DQ25	AF68	DDR1_DQ[9]/DDR0_DQ[25]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	AY54	M_A_BG1	
	M_A_DQ26	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU46	M_A_A13	A-CMD-MA
	M_A_DQ27	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_A15	
	M_A_DQ28	AF71	DDR1_DQ[12]/DDR0_DQ[28]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_A14	
	M_A_DQ29	AF69	DDR1_DQ[13]/DDR0_DQ[29]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_A16	
	M_A_DQ30	AH70	DDR1_DQ[14]/DDR0_DQ[30]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52	M_A_BA0	
	M_A_DQ31	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_A2	
M_A_DQ[32:39]	M_A_DQ32	BB65	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48	M_A_BA1	
	M_A_DQ33	AW65	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_A10	
	M_A_DQ34	AW63	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	BB50	M_A_A1	A-CMD-MA
	M_A_DQ35	AY63	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_A0	
	M_A_DQ36	BA65	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_MA[3]	BA50	M_A_A3	
	M_A_DQ37	AY65	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_MA[4]	BB52	M_A_A4	
	M_A_DQ38	BA63	DDR0_DQ[22]/DDR0_DQ[38]				
	M_A_DQ39	BB63	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_DQSN[0]	AM70	M_A_DQS_DN0	M_A_DQS0
M_A_DQ[40:47]	M_A_DQ40	BA61	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_DQSP[0]	AM69	M_A_DQS_DP0	
	M_A_DQ41	AW61	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_DQSN[1]	AT70	M_A_DQS_DN1	M_A_DQS1
	M_A_DQ42	BB59	DDR0_DQ[26]/DDR0_DQ[42]	DDR0_DQSP[1]	AT69	M_A_DQS_DP1	
	M_A_DQ43	AW59	DDR0_DQ[27]/DDR0_DQ[43]	DDR1_DQSN[0]/DDR0_DQSN[2]	AH66	M_A_DQS_DN2	M_A_DQS2
	M_A_DQ44	BB61	DDR0_DQ[28]/DDR0_DQ[44]	DDR1_DQSP[0]/DDR0_DQSP[2]	AH65	M_A_DQS_DP2	
	M_A_DQ45	AY61	DDR0_DQ[29]/DDR0_DQ[45]	DDR1_DQSN[1]/DDR0_DQSN[3]	AG69	M_A_DQS_DN3	M_A_DQS3
	M_A_DQ46	BA59	DDR0_DQ[30]/DDR0_DQ[46]	DDR1_DQSP[1]/DDR0_DQSP[3]	AG70	M_A_DQS_DP3	
	M_A_DQ47	AY59	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_DQSN[2]/DDR0_DQSN[4]	BA64	M_A_DQS_DN4	M_A_DQS4
M_A_DQ[48:55]	M_A_DQ48	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR0_DQSP[2]/DDR0_DQSP[4]	AY64	M_A_DQS_DP4	
	M_A_DQ49	AU66	DDR1_DQ[17]/DDR0_DQ[49]	DDR0_DQSN[3]/DDR0_DQSN[5]	AY60	M_A_DQS_DN5	M_A_DQS5
	M_A_DQ50	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR0_DQSP[3]/DDR0_DQSP[5]	BA60	M_A_DQS_DP5	
	M_A_DQ51	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR66	M_A_DQS_DN6	M_A_DQS6
	M_A_DQ52	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR65	M_A_DQS_DP6	
	M_A_DQ53	AP66	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_DQSN[3]/DDR0_DQSN[7]	AR61	M_A_DQS_DN7	M_A_DQS7
	M_A_DQ54	AT65	DDR1_DQ[22]/DDR0_DQ[54]	DDR1_DQSP[3]/DDR0_DQSP[7]	AR60	M_A_DQS_DP7	
	M_A_DQ55	AU65	DDR1_DQ[23]/DDR0_DQ[55]				
M_A_DQ[56:63]	M_A_DQ56	AT61	DDR1_DQ[24]/DDR0_DQ[56]	DDR0_ALERT#	AW50	M_A_ALERT_N	
	M_A_DQ57	AU61	DDR1_DQ[25]/DDR0_DQ[57]	DDR0_PAR	AT52	M_A_PARITY	
	M_A_DQ58	AP60	DDR1_DQ[26]/DDR0_DQ[58]				
	M_A_DQ59	AN60	DDR1_DQ[27]/DDR0_DQ[59]	DDR_VREF_CA	AY67	V_SMA_VREF_CA	
	M_A_DQ60	AN61	DDR1_DQ[28]/DDR0_DQ[60]	DDR0_VREF_DQ	AY68		
	M_A_DQ61	AP61	DDR1_DQ[29]/DDR0_DQ[61]	DDR1_VREF_DQ	BA67	V_SMB_VREF_CA	
	M_A_DQ62	AT60	DDR1_DQ[30]/DDR0_DQ[62]				
	M_A_DQ63	AU60	DDR1_DQ[31]/DDR0_DQ[63]	DDR_VTT_CNTL	AW67	SM_PGCNTL	

DDR CH - A

SKYLAKE-U-GP

CPU 071.SKYLA.000U

DEL TP406 -1 20170427



VTT_CNTL_CPU 51

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU1C — 3 OF 20 — SKYLAKE_ULT

M_B_DQ[0:7]: M_B_DQ0 AY39, M_B_DQ1 AW39, M_B_DQ2 AY37, M_B_DQ3 AW37, M_B_DQ4 BB39, M_B_DQ5 BA39, M_B_DQ6 BA37, M_B_DQ7 BB37

M_B_DQ[8:15]: M_B_DQ8 AY35, M_B_DQ9 AW35, M_B_DQ10 AY33, M_B_DQ11 AW33, M_B_DQ12 BB35, M_B_DQ13 BA35, M_B_DQ14 BA33, M_B_DQ15 BB33

M_B_DQ[16:23]: M_B_DQ16 AU40, M_B_DQ17 AT40, M_B_DQ18 AT37, M_B_DQ19 AU37, M_B_DQ20 AR40, M_B_DQ21 AP40, M_B_DQ22 AP37, M_B_DQ23 AR37

M_B_DQ[24:31]: M_B_DQ24 AT33, M_B_DQ25 AU33, M_B_DQ26 AU30, M_B_DQ27 AT30, M_B_DQ28 AR33, M_B_DQ29 AP33, M_B_DQ30 AR30, M_B_DQ31 AP30

M_B_DQ[32:39]: M_B_DQ32 AY31, M_B_DQ33 AW31, M_B_DQ34 AY29, M_B_DQ35 AW29, M_B_DQ36 BB31, M_B_DQ37 BA31, M_B_DQ38 BA29, M_B_DQ39 BB29

M_B_DQ[40:47]: M_B_DQ40 AY27, M_B_DQ41 AW27, M_B_DQ42 AY25, M_B_DQ43 AW25, M_B_DQ44 BB27, M_B_DQ45 BA27, M_B_DQ46 BA25, M_B_DQ47 BB25

M_B_DQ[48:55]: M_B_DQ48 AU27, M_B_DQ49 AT27, M_B_DQ50 AT25, M_B_DQ51 AU25, M_B_DQ52 AP27, M_B_DQ53 AN27, M_B_DQ54 AN25, M_B_DQ55 AP25

M_B_DQ[56:63]: M_B_DQ56 AT22, M_B_DQ57 AU22, M_B_DQ58 AU21, M_B_DQ59 AT21, M_B_DQ60 AN22, M_B_DQ61 AP22, M_B_DQ62 AP21, M_B_DQ63 AN21

DDR0_DQ[32]/DDR1_DQ[0] … DDR0_DQ[63]/DDR1_DQ[47] — DDR CH - B

DDR1_CKN[0], DDR1_CKN[1], DDR1_CKP[0], DDR1_CKP[1]

AN45 M_B_CLK#0 → M_B_CLK#0 13
AN46
AP45 M_B_CLK0 → M_B_CLK0 13
AP46

B-CLK

AN56 M_B_CKE0 → M_B_CKE0 13
AP55
AN55
AP53

DDR1_CKE[0], DDR1_CKE[1], DDR1_CKE[2], DDR1_CKE[3]

B-CTRL-CKE

BB42 M_B_CS#0 → M_B_CS#0 13
AY42 M_B_ODT0 → M_B_ODT0 13
BA42
AW42

DDR1_CS#[0], DDR1_CS#[1], DDR1_ODT[0], DDR1_ODT[1]

B-CTRL-CS

B-CTRL-ODT

AY48 M_B_A5 → M_B_A5 13
AP50 M_B_A9 → M_B_A9 13
BA48 M_B_A6 → M_B_A6 13
BB48 M_B_A8 → M_B_A8 13
AP48 M_B_A7 → M_B_A7 13
AP52 M_B_BG0 → M_B_BG0 13
AN50 M_B_A12 → M_B_A12 13
AN48 M_B_A11 → M_B_A11 13
AN53 M_B_ACT_N → M_B_ACT_N 13
AN52 M_B_BG1 → M_B_BG1 13

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] … DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#, DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]

B-CMD-MA

BA43 M_B_A13 → M_B_A13 13
AY43 M_B_A15 → M_B_A15 13
AY44 M_B_A14 → M_B_A14 13
AW44 M_B_A16 → M_B_A16 13
BB44 M_B_BA0 → M_B_BA0 13
AY47 M_B_A2 → M_B_A2 13
BA44 M_B_BA1 → M_B_BA1 13
AW46 M_B_A10 → M_B_A10 13
AY46 M_B_A1 → M_B_A1 13
BA46 M_B_A0 → M_B_A0 13
BB46 M_B_A3 → M_B_A3 13
BA47 M_B_A4 → M_B_A4 13

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] … DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0], DDR1_MA[3], DDR1_MA[4]

B-CMD-MA

BA38 M_B_DQS_DN0
AY38 M_B_DQS_DP0 → M_B_DQS_DN0 — **M_B_DQS0**
AY34 M_B_DQS_DN1 → M_B_DQS_DP0 — **M_B_DQS1**
BA34 M_B_DQS_DP1 → M_B_DQS_DN1
AT38 M_B_DQS_DN2 → M_B_DQS_DP1 — **M_B_DQS2**
AR38 M_B_DQS_DP2 → M_B_DQS_DN2
AT32 M_B_DQS_DN3 → M_B_DQS_DP2 — **M_B_DQS3**
AR32 M_B_DQS_DP3 → M_B_DQS_DN3
BA30 M_B_DQS_DN4 → M_B_DQS_DP3 — **M_B_DQS4**
AY30 M_B_DQS_DP4 → M_B_DQS_DN4
AY26 M_B_DQS_DN5 → M_B_DQS_DP4 — **M_B_DQS5**
BA26 M_B_DQS_DP5 → M_B_DQS_DN5
AR25 M_B_DQS_DN6 → M_B_DQS_DP5 — **M_B_DQS6**
AR27 M_B_DQS_DP6 → M_B_DQS_DN6
AR22 M_B_DQS_DN7 → M_B_DQS_DP6
AR21 M_B_DQS_DP7 → M_B_DQS_DN7 — **M_B_DQS7**
M_B_DQS_DP7

DDR0_DQSN[4]/DDR1_DQSN[0] … DDR0_DQSP[7]/DDR1_DQSP[5], DDR1_DQSN[6], DDR1_DQSP[6], DDR1_DQSN[7], DDR1_DQSP[7]

AN43 M_B_ALERT_N → M_B_ALERT_N 13
AP43 M_B_PARITY → M_B_PARITY 13
AT13 SM_DRAMRST#_CPU
AR18 SM_RCOMP_0
AT18 SM_RCOMP_1
AU18 SM_RCOMP_2

DDR1_ALERT#, DDR1_PAR, DRAM_RESET#, DDR_RCOMP[0], DDR_RCOMP[1], DDR_RCOMP[2]

SKYLAKE-U-GP

1D2V_S3 — R506 470R2F-GP — SM_DRAMRST# 12,13

R501 SDP 200R2F-L-GP
R510 DDP 121R2F-GP
R502 80D6R2F-L-GP
R503 100R2F-L3-GP
R504 0R0402-PAD

C501 SC100P50V2JN-L-GP — Sensitive trace cap

Layout Note:

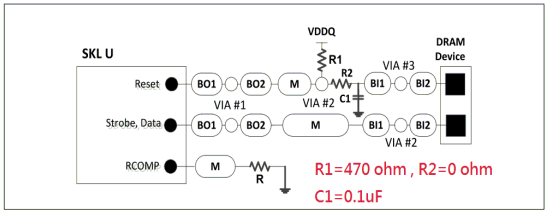
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

	R501
DDP	121ohm(64.12105.6DL)
SDP	200ohm(64.20005.6DL)

close CPU

SM_DRAMRST#_CPU — ED501 AZ5725-01FDR7G-GP DY — ED502 AZ5725-01FDR7G-GP DY

Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



071.SKYLA.000U

#543016

CPU

Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 5 of 106

Main Func = PCH

DETECT&RESET

55 TOUCH_DET#
25 RTC_DET#
55 TOUCH_S_RST#

DEBUG PORT

68 LPSS_UART1_RXD
68 LPSS_UART1_TXD
68 LPSS_UART1_RTS#
68 LPSS_UART1_CTS#
68 LPSS_UART2_RXD
68 LPSS_UART2_TXD
68 LPSS_UART2_RTS#
68 LPSS_UART2_CTS#

I2C

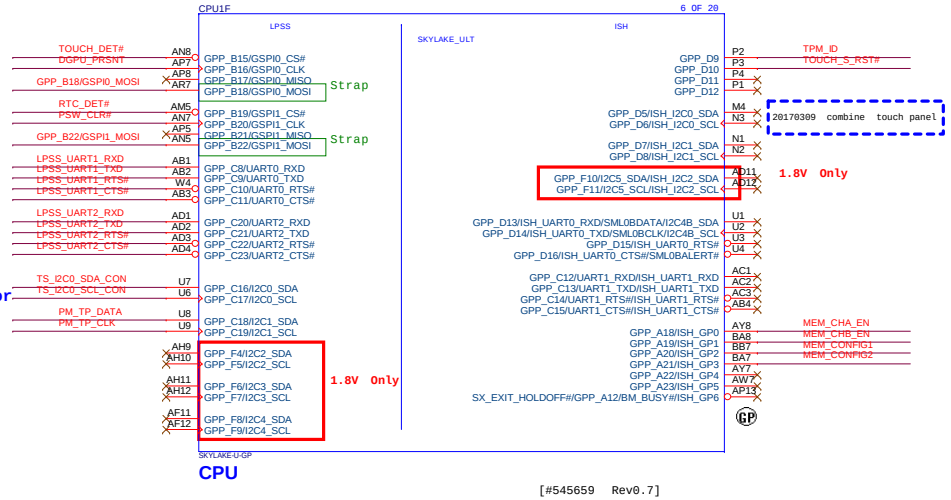
24,55 TS_I2C0_SDA_CON
24,55 TS_I2C0_SCL_CON
65 PM_TP_DATA
65 PM_TP_CLK

OTHER

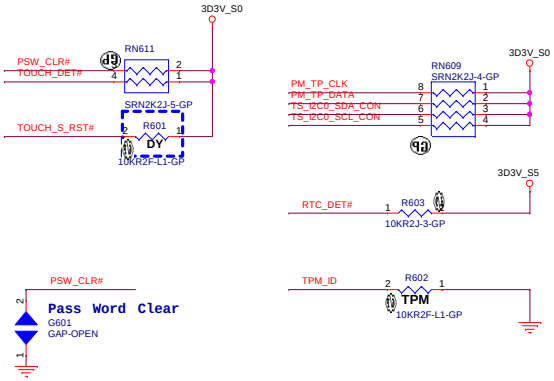
14 GPP_B18/GSPI0_MOSI
14 GPP_B22/GSPI1_MOSI

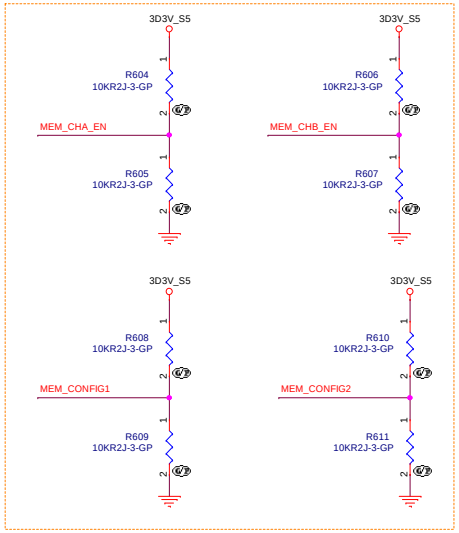
Touch Panel/G-Sensor

Touch Pad



[#545659 Rev0.7]





GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Vendor	GONFIG4 (GPP_A19)	CONFIG3 (GPP_A18)	CONFIG2 (GPP_A21)	CONFIG1 (GPP_A20)	Mfr.PN	Wistron PN	Capacity	DDP/SDP
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	KN.8GB0G.049	8Gb	SDP
MICRON	0	0	0	1	MT40A512M16JY-083E:B	KN.8GB04.013	8Gb	SDP
SAMSUNG	0	0	1	0	K4A8G165WB-BCRC	KN.8GB0B.048	8Gb	SDP
HYNIX	0	0	1	1	H5AN4G6NAFR-TF	KN.0040G.015	4Gb	SDP
HYNIX	0	1	0	0	H5AN4G6NAFR-UHC	KN.0040G.016	4Gb	SDP
MICRON	0	1	0	1	MT40A256M16GE-083E:B	KN.00404.010	4Gb	SDP
SAMSUNG	0	1	1	0	K4A4G165WE-BCRC	KN.0040B.014	4Gb	SDP
HYNIX	0	1	1	1	H5ANAG6NAMR-UHC	KN.0160G.010	16Gb	DDP
MICRON	1	0	0	0	MT40A1G16WBU-083E:B	KN.01604.001	16Gb	DDP

Count

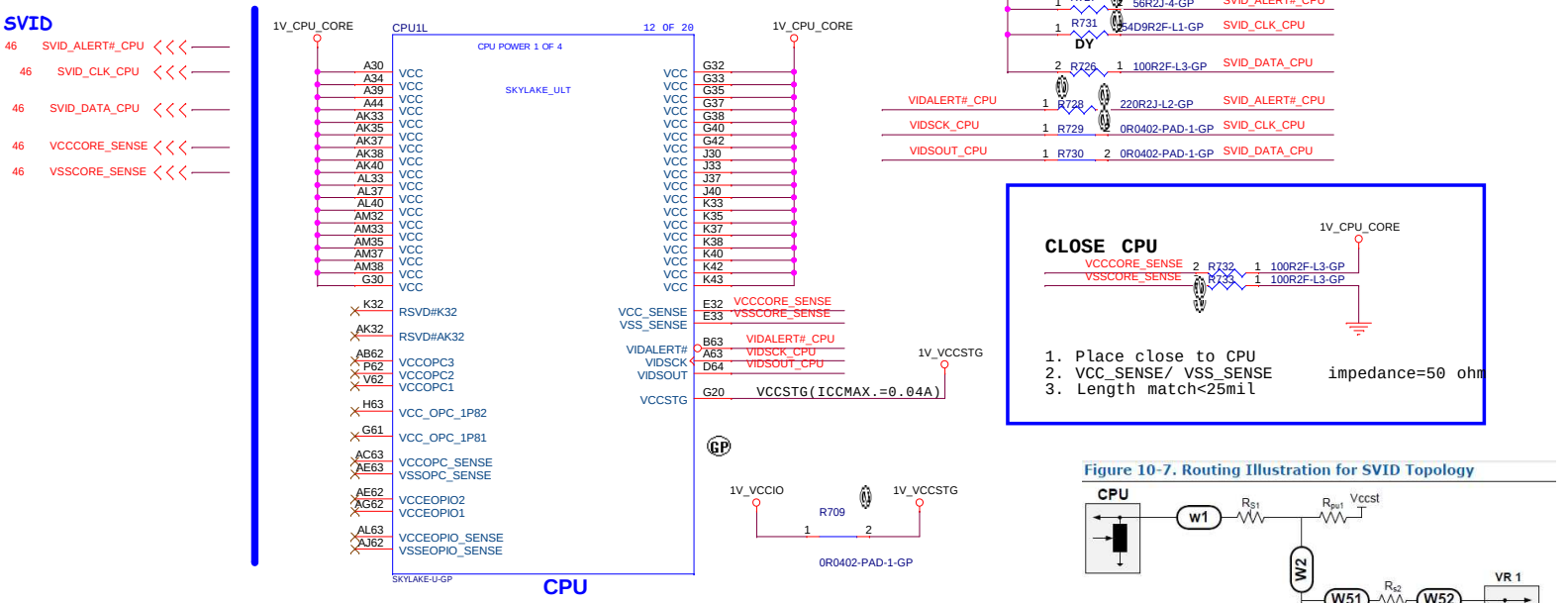
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 6 of 106

Main Func = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

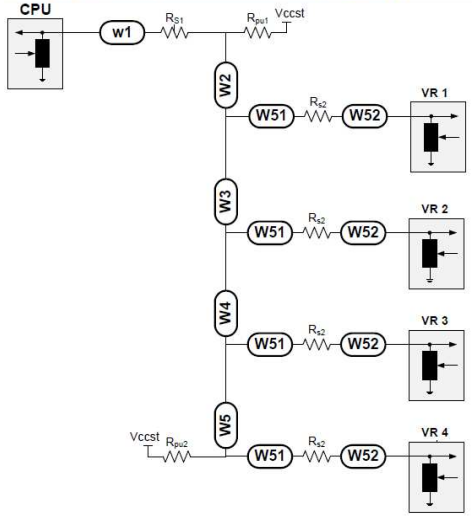


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_POWER1

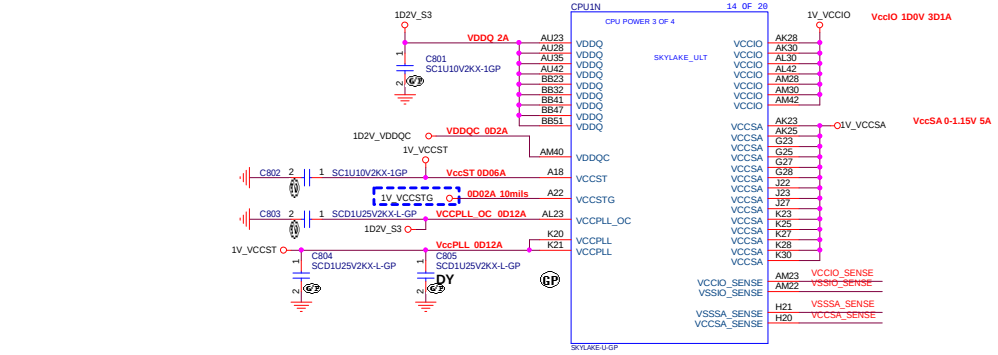
Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 7 of 106

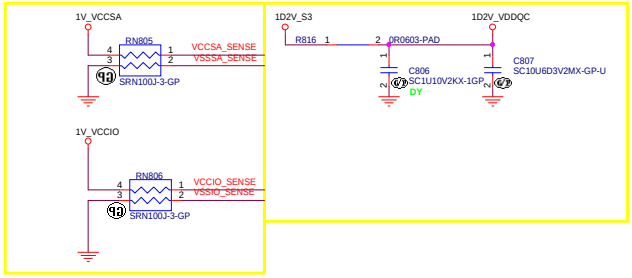
Main Func = CPU

46 VSSSA_SENSE
46 VCCSA_SENSE

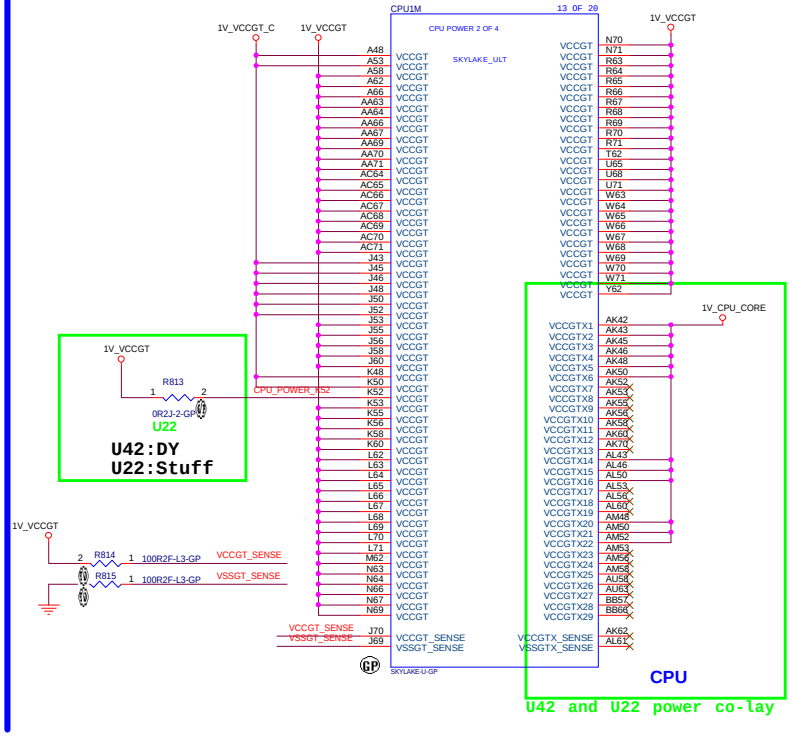
46 VCCGT_SENSE
46 VSSGT_SENSE



CPU

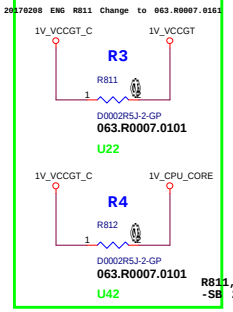


VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



U42 and U22 power co-lay

If no plan to use U 2+3e in the same platform. These balls can be connected to VccCore. No shunting resistor needed.



R811,R812 change PN -SB 20170324

KBL U42 Board Compatibility with KBL U22/23e

- 4 Rshunts Required
  - R1 – between VCCGTU VR and VCCGTU
  - R2 – between VCCGTU and VCCCORE
  - R3 – between VCCGT and VCCGT VR
  - R4 – between VCCGT and VCCCORE
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board

U22	R1	X	R3	X
U42	X	R2	X	R4

Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_POWER1

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 8 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **Slinky**	Rev: **-1**
Date: Thursday, August 24, 2017	Sheet 9 of 106	

Main Func = CPU

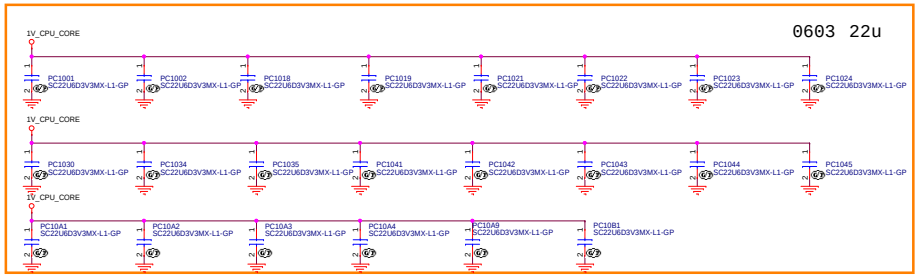
1V_CPU_CORE

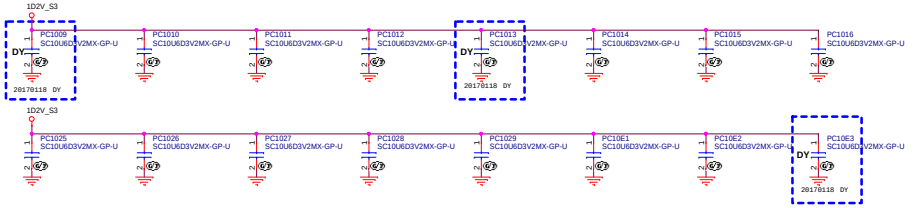
U22 0603 22uF *22 , 0402 10uF*11 , 1uF*1

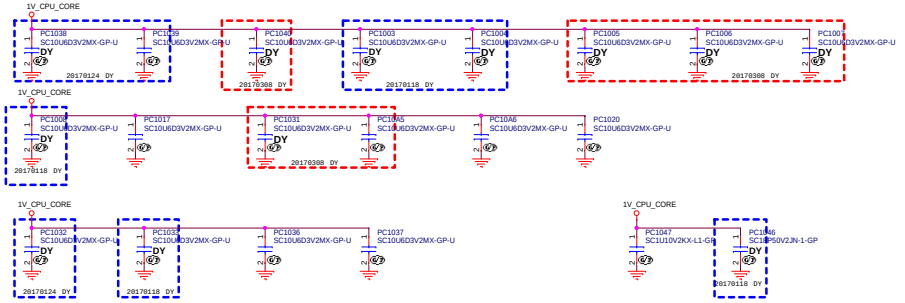
U42 0603 22uF *4 , 0402 10uF*15

1D2V_S3

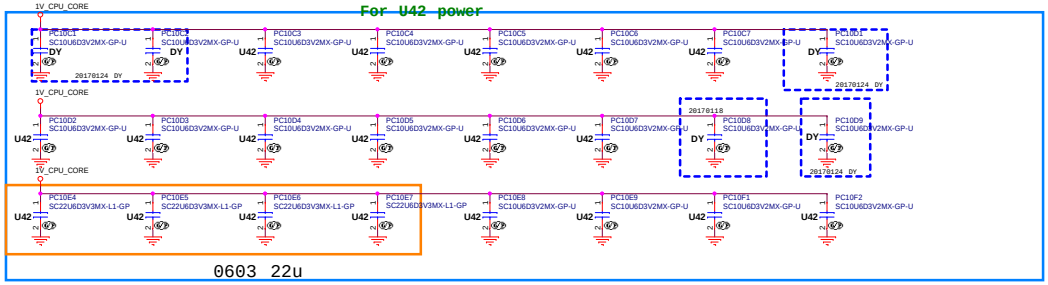
0402 10uF*13





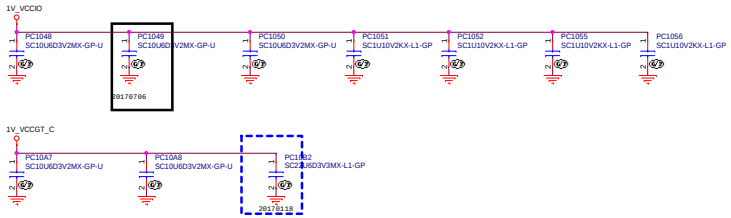


For U42 power



1V_VCCIO

10uF * 2 1uF *4



Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

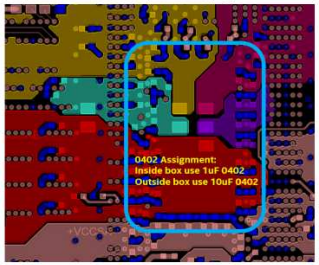
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP1)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 10 of 106

Main Func = CPU

SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

0603 22u

1V_VCCGT
PC1101 SC22U6D3V3MX-L1-GP
PC1102 SC22U6D3V3MX-L1-GP
PC1112 SC22U6D3V3MX-L1-GP
PC1116 SC22U6D3V3MX-L1-GP
PC1134 SC22U6D3V3MX-L1-GP
PC1135 SC22U6D3V3MX-L1-GP
PC1137 SC22U6D3V3MX-L1-GP
PC1138 SC22U6D3V3MX-L1-GP

1V_VCCGT
PC1167 SC22U6D3V3MX-L1-GP
PC10B3 SC22U6D3V3MX-L1-GP
PC10B4 SC22U6D3V3MX-L1-GP
PC10B5 SC22U6D3V3MX-L1-GP
PC10B6 SC22U6D3V3MX-L1-GP
PC10B7 SC22U6D3V3MX-L1-GP

1V_VCCGT
PC1121 SC10U6D3V2MX-GP-U
PC1122 SC10U6D3V2MX-GP-U
PC1123 SC10U6D3V2MX-GP-U
PC1124 SC10U6D3V2MX-GP-U
PC1125 SC10U6D3V2MX-GP-U
PC1126 SC10U6D3V2MX-GP-U
PC1127 SC10U6D3V2MX-GP-U
PC1128 SC10U6D3V2MX-GP-U

1V_VCCGT
PC1133 SC10U6D3V2MX-GP-U DY
PC1107 SC10U6D3V2MX-GP-U
PC1108 SC10U6D3V2MX-GP-U
PC1136 SC10U6D3V2MX-GP-U
PC1103 SC10U6D3V2MX-GP-U
PC1104 SC10U6D3V2MX-GP-U
PC1105 SC10U6D3V2MX-GP-U
PC1168 SC10U6D3V2MX-GP-U DY

1V_VCCGT
PC1109 SC10U6D3V2MX-GP-U
PC1110 SC10U6D3V2MX-GP-U
PC1111 SC10U6D3V2MX-GP-U DY
PC1141 SC10U6D3V2MX-GP-U
PC1113 SC10U6D3V2MX-GP-U
PC1114 SC10U6D3V2MX-GP-U
PC1115 SC10U6D3V2MX-GP-U
PC1171 SC10U6D3V2MX-GP-U

1V_VCCGT
PC1165 SC10U6D3V2MX-GP-U
PC1166 SC10U6D3V2MX-GP-U

1V_VCCGT
1V_VCCSA
0603 10uF *14 , 0402 10uF*26

1V_VCCSA
0402 10uF*12

1V_VCCSA
-1 20170505
PC1117 SC22U6D3V3MX-L1-GP
PC1119 SC22U6D3V3MX-L1-GP
PC1120 SC10U6D3V2MX-GP-U

1V_VCCSA
-1 20170505
PC1129 SC22U6D3V3MX-L1-GP
PC1130 SC22U6D3V3MX-L1-GP
PC1132 SC22U6D3V3MX-L1-GP

1V_VCCSA
20170118
PC1139 SC10U6D3V2MX-GP-U
PC1170 SC10U6D3V2MX-GP-U
PC1152 SC10U6D3V2MX-GP-U
PC1140 SC10U6D3V2MX-GP-U

U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								0r	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								0r	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

1D0V_S5
PC1142 SC1U10V2KX-L1-GP DY
CLOSE CPU AB19

1D0V_S5
PC1143 SC1U10V2KX-L1-GP 20170708
CLOSE CPU AF18

1D0V_S5
PC1144 SC1U10V2KX-L1-GP
CLOSE CPU K17

1D0V_S5
PC1145 SC1U10V2KX-L1-GP
PC1146 SC22U6D3V3MX-L1-GP 20170706
CLOSE CPU N15

1D0V_S5
PC1147 SC1U10V2KX-L1-GP 20170706
CLOSE CPU K15

1D0V_S5
PC1148 SC1U10V2KX-L1-GP 20170706
CLOSE CPU AF20

1D0V_S5
PC1149 SC1U10V2KX-L1-GP
CLOSE CPU N18

1D0V_S5
PC1150 SC1U10V2KX-L1-GP 20170708
CLOSE CPU A10

1D0V_VCCDSW
PC1163 SC1U10V2KX-L1-GP
CLOSE CPU AL1

VCCRTCEXT
PC1164 SCD1U25V2KX-L1-GP
CLOSE CPU BB10

3D3V_S5
PC1153 SC1U10V2KX-L1-GP
CLOSE CPU AJ19

3D3V_S5
PC1154 SC1U10V2KX-L1-GP DY
CLOSE CPU V19

3D3V_S5
PC1155 SC1U10V2KX-L1-GP DY
CLOSE CPU AG15

3D3V_S5
PC1156 SC1U10V2KX-L1-GP DY
CLOSE CPU Y16

3D3V_S5
PC1157 SC1U10V2KX-L1-GP DY
CLOSE CPU T16

3D3V_S5
PC1158 SC1U10V2KX-L1-GP
PC1159 SCD1U25V2KX-L-GP
CLOSE CPU AK17

3D3V_RTC_AUX
PC1160 SC1U10V2KX-L1-GP
PC1161 SCD1U25V2KX-L-GP
CLOSE CPU AK19

1D8V_S5
PC1162 SC1U10V2KX-L1-GP
CLOSE CPU AA1

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

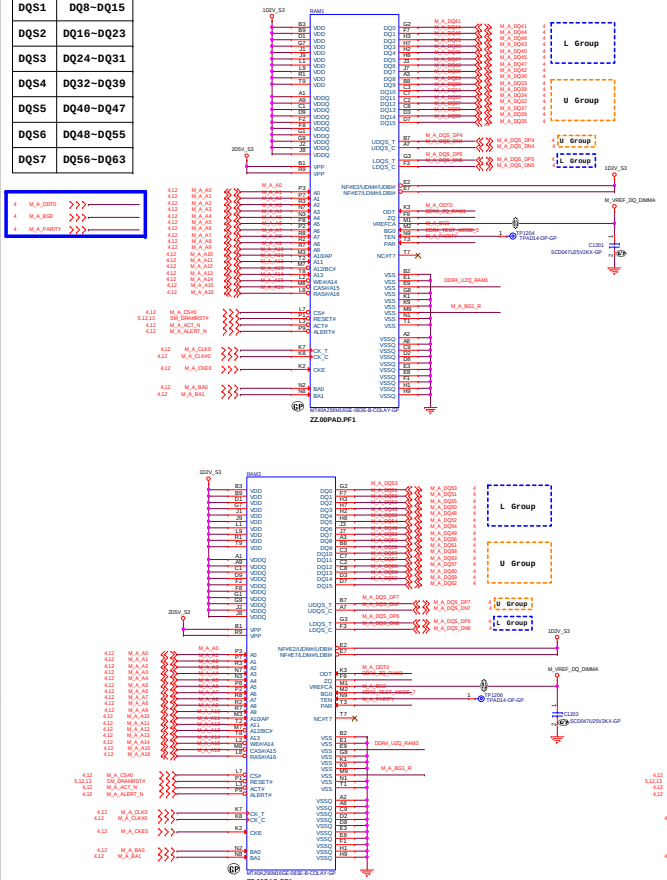
Size: Custom | Document Number: Slinky | Rev: -1

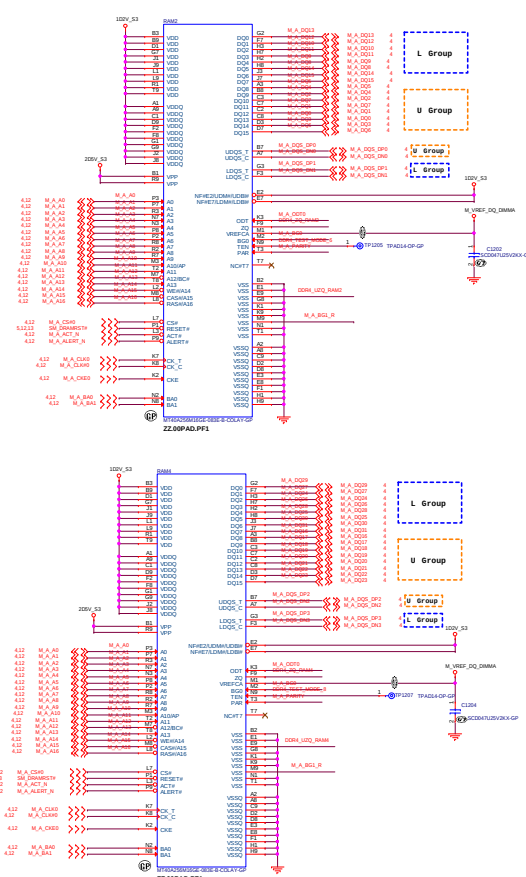
Date: Thursday, August 24, 2017 | Sheet 11 of 106

SSID = LPDDR3 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required





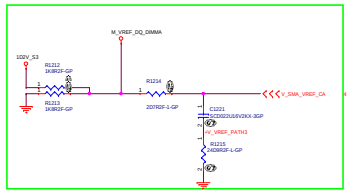
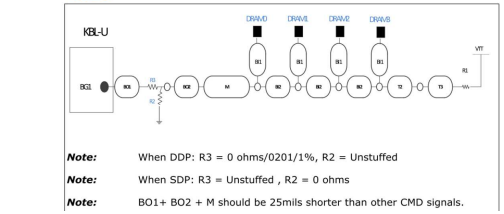


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

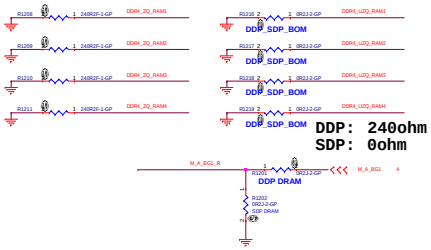


Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

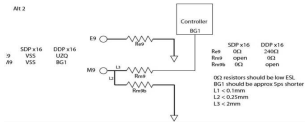
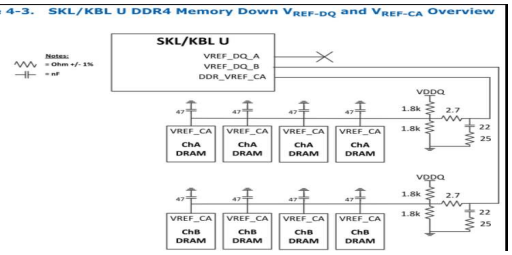
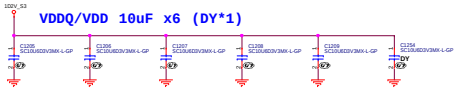
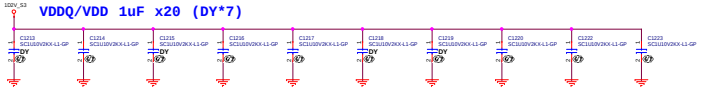


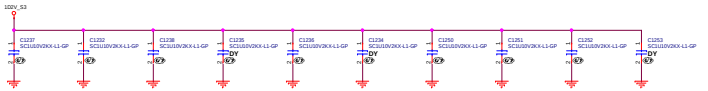
Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview

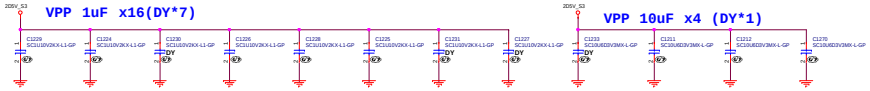


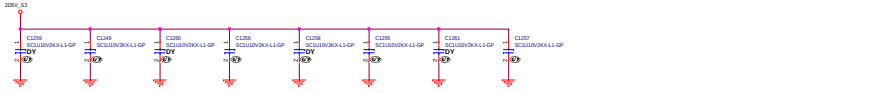
DDR4 On Board RAM Power Decouple Cap

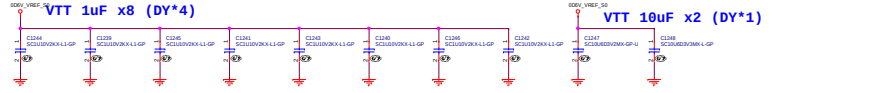


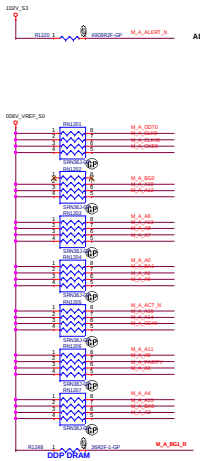












For RAM1, RAM2, RAM3, RAM4

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4 MD_CHA

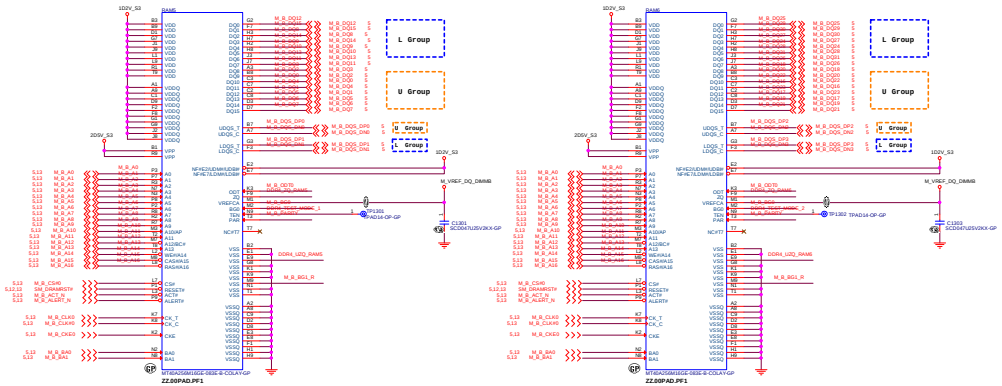
Size: Slinky | Document Number | Rev: -1

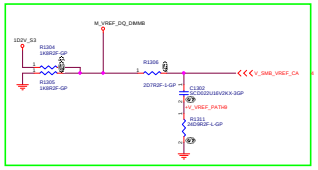
Date: Thursday, August 24, 2017 | Sheet 13 of 108

SSID = LPDDR3 CHB

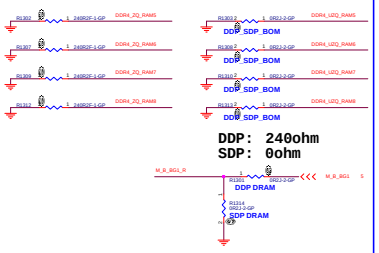
DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required





SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

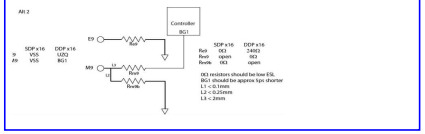
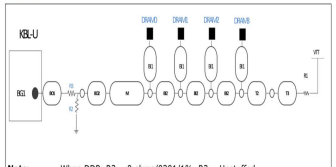


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology



Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

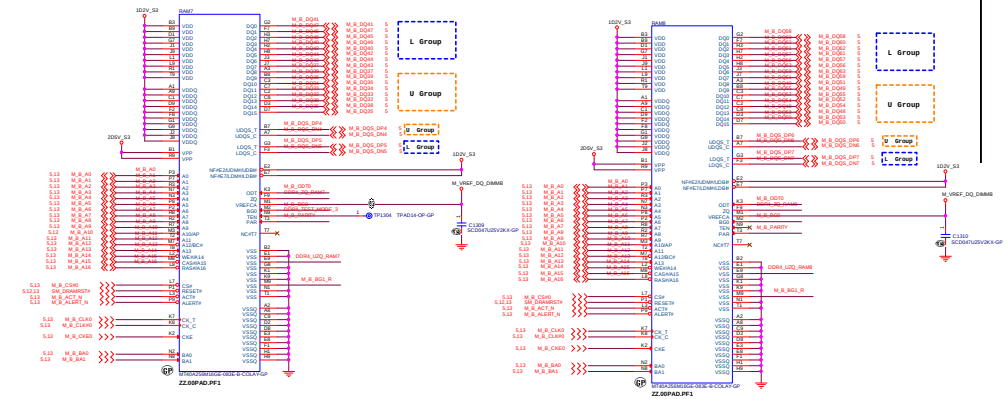
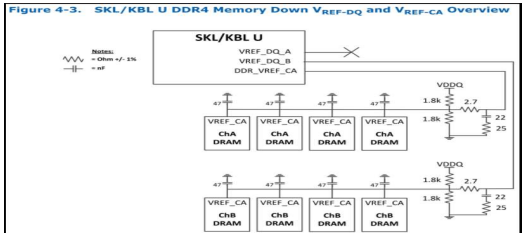
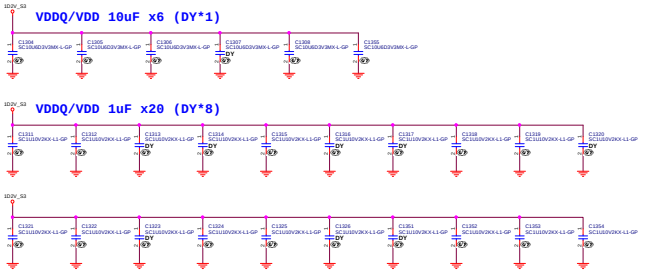


Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



DDR4 On Board RAM Power Decouple Cap

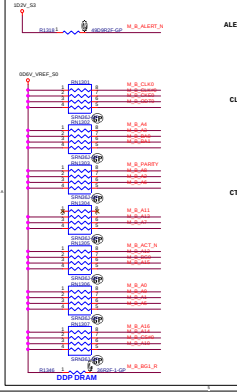


4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

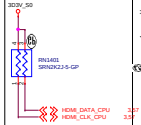
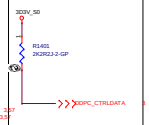
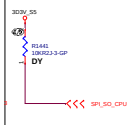
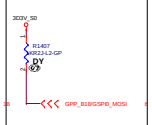
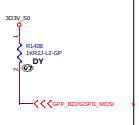
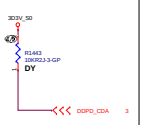
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

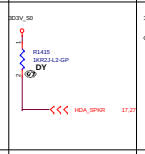
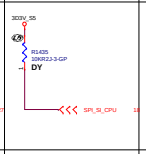
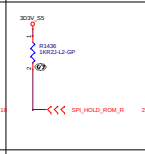
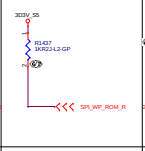
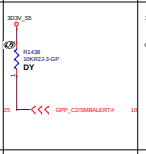
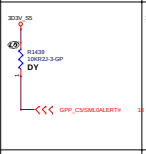
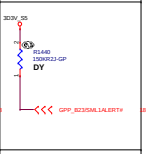


Wistron Corporation	Size: B	Document Number:	Rev: -1	
DDR4MD_CHB	Date: Monday, August 14, 2017	Sheet 12 of 67		
Slinky				

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit 10 — Boot BIOS Destination** 0 — SPI 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	De-Glitch (Note 2) Output	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: (Reserved)_SODIMM_SODIMM4

Size: A1 | Document Number: Slinky | Rev: -1

Date: Thursday, August 04, 2011 | Sheet 14 of 38

Main Func = PCH

USB3 port1

35 USB1_USB30_RX_N
35 USB1_USB30_RX_P
35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB20_N
35 USB1_USB20_P

USB3 port2

35 USB2_USB30_RX_N
35 USB2_USB30_RX_P
35 USB2_USB30_TX_N
35 USB2_USB30_TX_P
36 USB2_USB20_N
36 USB2_USB20_P

USB Type-C

73 USB30_RX_CPU_N3
73 USB30_RX_CPU_P3
73 USB30_TX_CPU_N3
73 USB30_TX_CPU_P3
73 TYPEC_USB20_N
73 TYPEC_USB20_P

USB2.0

64,89 USB3_USB20_N
64,89 USB3_USB20_P
61,89 BT_USB20_N
61,89 BT_USB20_P
55 TS_USB20_N
55 TS_USB20_P
29 CCD_USB20_N
29 CCD_USB20_P
64,89 CR_USB20_N
64,89 CR_USB20_P
92 FP_USB20_N
92 FP_USB20_P

M.2

62 PCIE_RX_CPU_N11
62 PCIE_RX_CPU_P11
62 PCIE_TX_CON_N11
62 PCIE_TX_CON_P11
62 PCIE_RX_CPU_N12
62 PCIE_RX_CPU_P12
62 PCIE_TX_CON_N12
62 PCIE_TX_CON_P12
62 DEVSLP1

HDD

60 HDD_SATA_TX_P
60 HDD_SATA_TX_N
60 HDD_SATA_RX_P
60 HDD_SATA_RX_N

WLAN

61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_PCIE_TX_N
61,89 WLAN_PCIE_TX_P

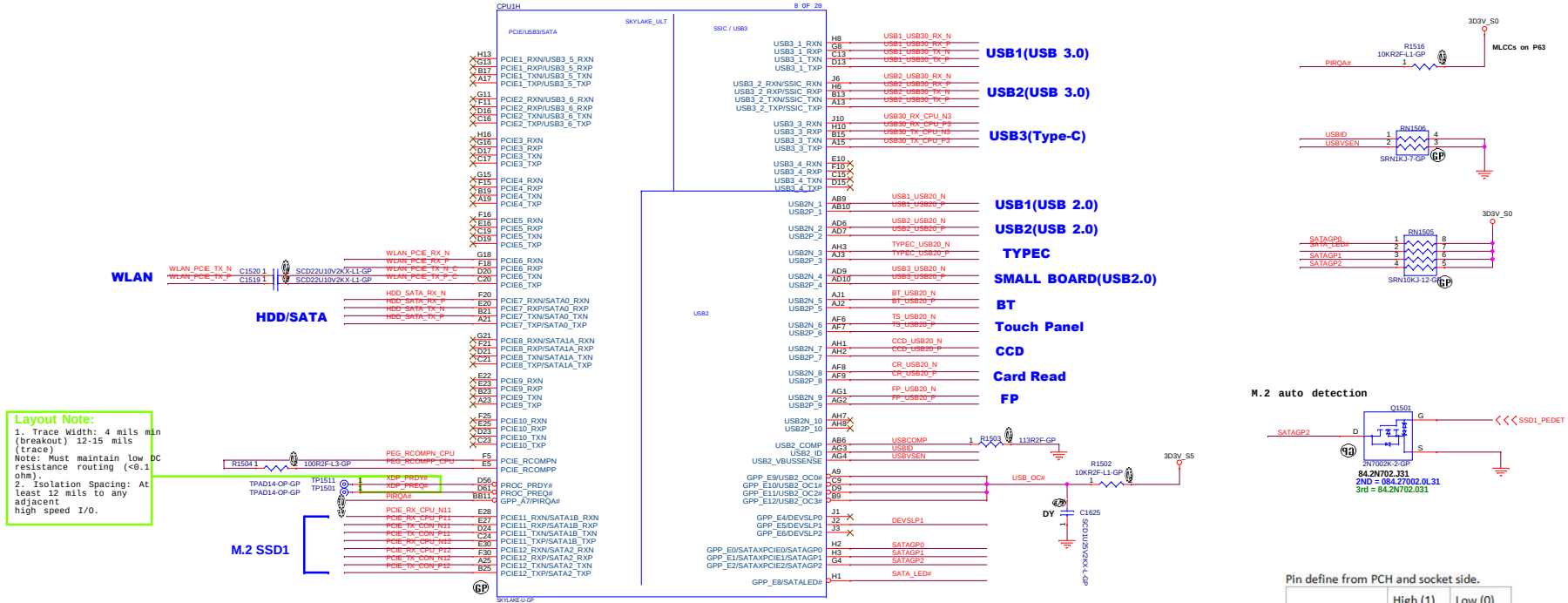


Table 27. Socket 2 Module Configuration

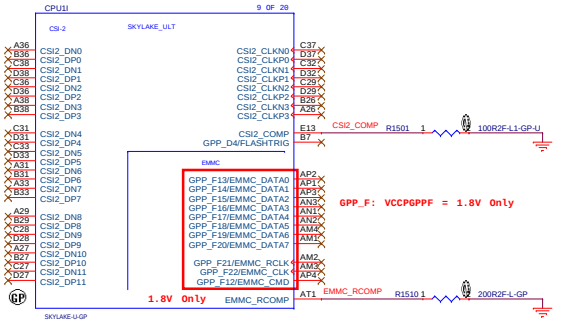
State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

	KBL PremiumU		Acer 2015		2017R15(Premium)		2017R15(base)
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3 Type-C (I/O)		USB 3 Type-C (I/O)
Lane4	USB3 Port4						
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		dGPU		dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2					
Lane7		PCIe Port3					
Lane8		PCIe Port4					
Lane9		PCIe Port5	LAN				
Lane10		PCIe Port6	WIFI		WIFI		WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD		HDD		HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD				
Lane13		PCIe Port9	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal		M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane14		PCIe Port10					
Lane15	SATA1 (Premium)	PCIe Port11					
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)		M.2 SSD SATA		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)		USB 2 Type-C (I/O)		USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / SensorHub		USB 2 (I/O)		USB 2 (I/O)
	USB2 Port5		BT		BT		BT
	USB2 Port6		TS		TS		TS
	USB2 Port7		CCD		CCD		CCD
	USB2 Port8		CR (USB) / FP		CR		CR
	USB2 Port9		3G		FP		FP
	USB2 Port10						



Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 15 of 106

Main Func = PCH

WLAN
61,89 WLAN_CLK_CPU#
61,89 WLAN_CLK_CPU
61,89 WLAN_CLKREQ_CPU#

NGFF1
62 SSD1_CLK_CPU_N
62 SSD1_CLK_CPU
62 SSD1_CLKREQ_CPU_N

KBC
24 RTCRST_ON

WLAN
61 SUS_CLK_CPU

CPU

CPU1J
10 OF 20
CLOCK SIGNALS
SKYLAKE_ULT
SKYLAKE-U-GP

WLAN
NGFF1

PEG_CLKREQ_CPU# D42 C42 AR10 CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
LAN_CLKREQ_CPU# B42 A42 AT7 CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
WLAN_CLK_CPU# WLAN_CLK_CPU WLAN_CLKREQ_CPU# D41 C41 AT8 CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
SSD1_CLK_CPU_N SSD1_CLK_CPU SSD1_CLKREQ_CPU_N D40 C40 AT10 CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
SRCCLKREQ4# B40 A40 AU8 CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
SRCCLKREQ5# E40 E38 AU7 CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 SUS_CLK_CPU
XTAL24_IN E37 XTL_24M_X1_CPU
XTAL24_OUT E35 XTL_24M_X2_CPU
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 XTL_32K_X1_CPU
RTCX2 AM20 XTL_32K_X2_CPU
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#

1D0V_S5
R1603 2K7R2F-GP

RTC Reset

For AFR
RTCRST_ON
Q1603 2N7002K-2-GP
RTC_RST#_R
RTC_RST#
R1618 100KR2F-L3-GP
R1621 2K2R2J-L1-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1615 10MR2J-L-GP
20170210 change
X1602 XTAL-32D768KHZ-91-GP
082.30003.0221
2ND = 082.30003.0301
3RD = 082.30003.0191
C1603 SC15P50V2JN-L-GP
C1604 SC15P50V2JN-L-GP
-SB 20170314 VENDOR SUGGEST

3D3V_RTC_AUX
RN1601 SRN20KJ-1-GP
SRTC_RST#
RTC_RST#
C1606 SC1U50V3KX-GP
G1601 GAP-OPEN
C1605 SC1U50V3KX-GP

XTL_24M_X1_CPU
U22 C1601 SC15P50V2JN-L-GP
R1602 1MR2F-L-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
X1601 XTAL-24MHZ-135-GP
082.30006.0041
2nd = 82.30004.A01
XTL_24M_X2_CPU
U22 C1602 SC15P50V2JN-L-GP

X1601 P/N:082.30006.0041

close to CPU
3D3V_S0
RN1608
SSD1_CLKREQ_CPU_N
PEG_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
LAN_CLKREQ_CPU#
SRN10KJ-12-GP
RN1609
SRCCLKREQ4#
SRCCLKREQ5#
SRN10KJ-L-GP

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP_CLOCK
Size: Custom
Document Number: Slinky
Rev: -1
Date: Thursday, August 24, 2017
Sheet 16 of 106

Main Func = PCH

Audio Code

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
14,27 HDA_SPKR

24 ME_UNLOCK

3D3V_S5
R1702
150KR2J-GP
DY
HDA_SDOUT_CPU

RN1701
SRN33J-7-GP
HDA_BITCLK_CODEC — HDA_BITCLK_CPU
HDA_SYNC_CODEC — HDA_SYNC_CPU
HDA_SDOUT_CODEC — HDA_SDOUT_CPU
HDA_RST#_CPU

CPU1G
7 OF 20
AUDIO
SKYLAKE_ULT
SKYLAKE-U-GP

1KR2F-L1-GP
R1709
ME_UNLOCK

HDA_SYNC_CPU — BA22 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU — AY22 HDA_BLK/I2S0_SCLK
HDA_SDOUT_CPU — BB22 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU — BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
HDA_RST#_CPU — AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD

Strap

AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD

1.8V Only

H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1

HDA_SPKR — AW5 GPP_B14/SPKR

Strap

SDIO/SDXC

GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7

GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9

SD_RCOMP AB7
SD_RCOMP — R1701 1 DY 200R2F-L-GP

1.8V Only
GPP_F23 AF13

RESET# in not required for ALC295

CPU

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 17 of 106

Main Func = PCH

LPC

24,68,91 LPC_AD_CPU_P0
24,68,91 LPC_AD_CPU_P1
24,68,91 LPC_AD_CPU_P2
24,68,91 LPC_AD_CPU_P3
24,68,91 LPC_FRAME#_CPU
18,24 LPC_CLK_KBC
18,68 LPC_CLK_DBG

SPI

24,25 SPI_CS_CPU_N0
24,25 SPI_CLK_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24,25 SPI_SO_ROM
24,25 SPI_SI_ROM
14 SPI_SO_CPU
14 SPI_SI_CPU

SMBUS

69 SMB_CLK_CPU
69 SMB_DATA_CPU
24,55,70,73 SML1_CLK
24,55,70,73 SML1_DATA
27,29 SML0_CLK_CPU
27,29 SML0_DATA_CPU

KBC

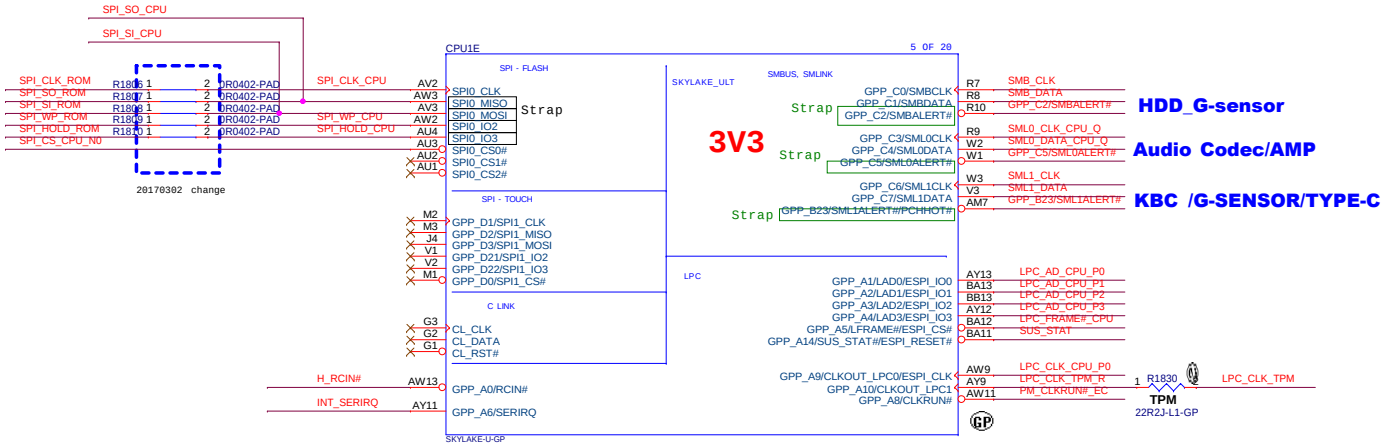
24 H_RCIN#
24,68,91 INT_SERIRQ

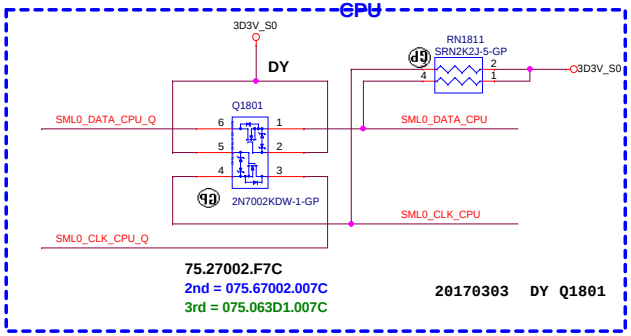
TPM

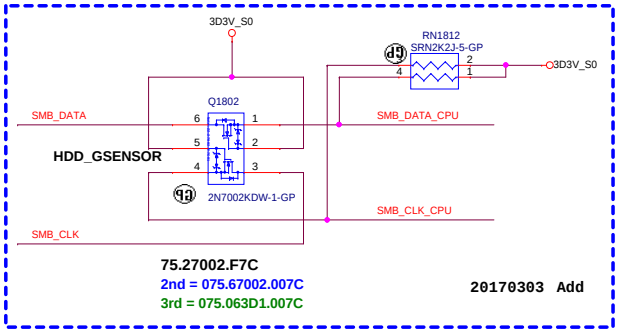
91 LPC_CLK_TPM
91 SUS_STAT
24,91 PM_CLKRUN#_EC

OTHER

14 GPP_C2/SMBALERT#
14 GPP_C5/SML0ALERT#
14 GPP_B23/SML1ALERT#







Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

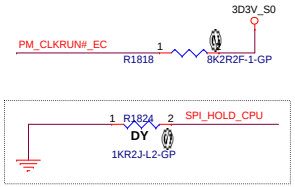
20.9 Serial Interrupt

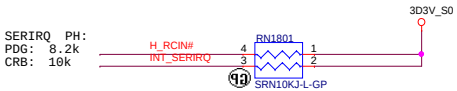
The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

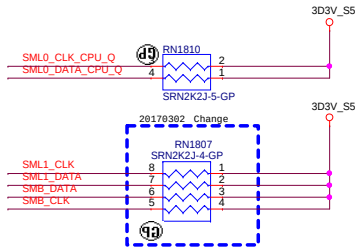
- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

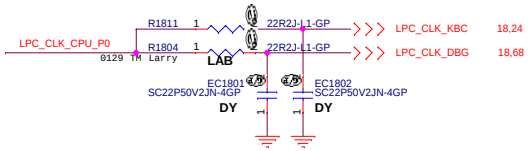
The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.









Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LPC,SPI,SMBUS,CLINK***
Size: Custom	Document Number: **Slinky** Rev: **-1**
Date: Thursday, August 24, 2017	Sheet 18 of 106

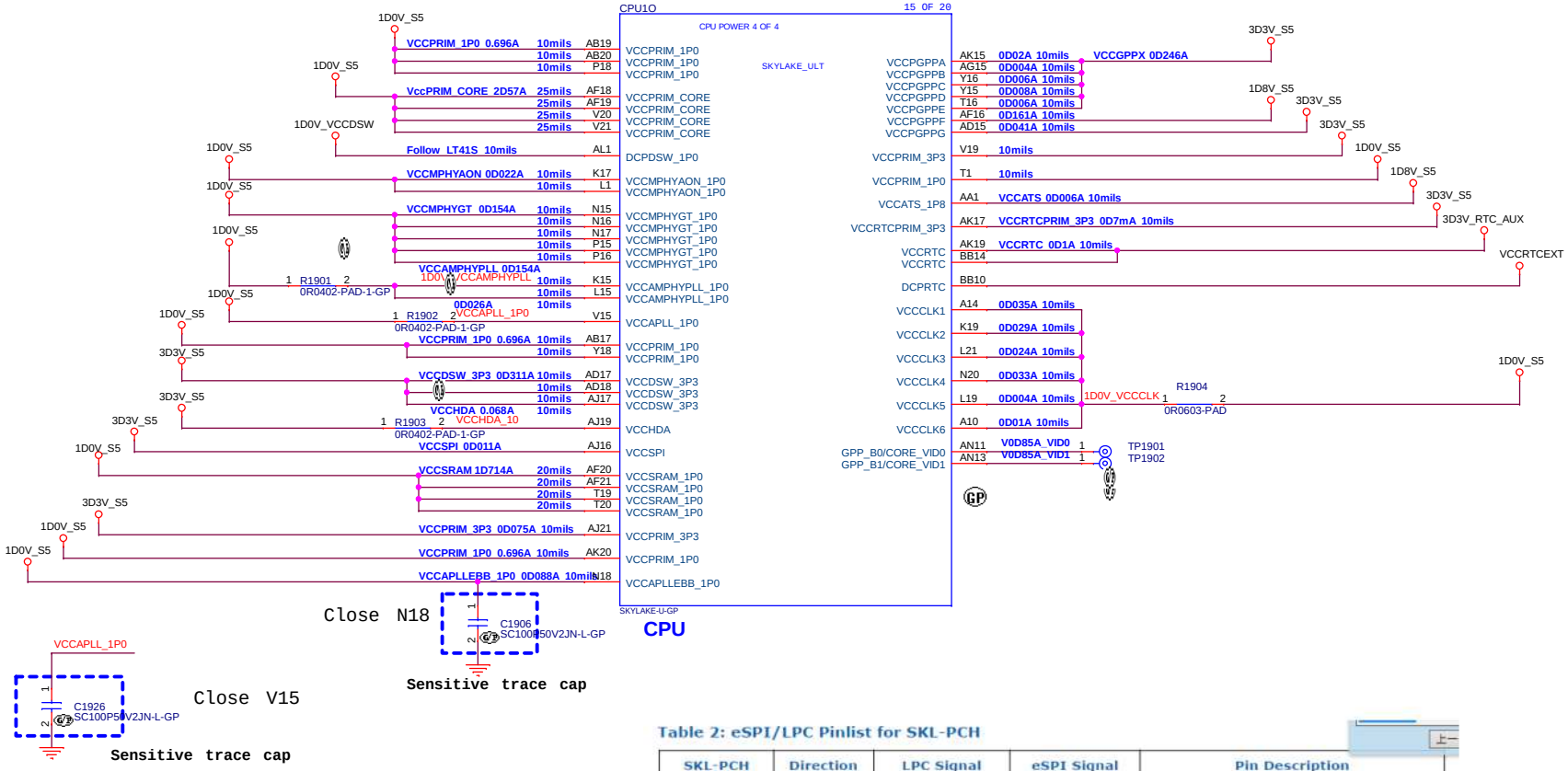


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(CS-2/EMMC)***

Size: Custom | Document Number: **Slinky** | Rev: **-1**

Date: Thursday, August 24, 2017 | Sheet 19 of 106

Main Func = PCH

24 SYS_PWROK
40 PCH_PWROK
24,61,62 PCIE_WAKE#
24,40 ALL_SYS_PWRGD
24,61,62,68,89,91 PLT_RST#
24 RSMRST#_KBC
45,53,73 3V_5V_POK
24,40,45,53,60 PM_SLP_S3#
24,40,51 PM_SLP_S4#
24 PM_PWRBTN#
24 AC_PRESENT

CPU1K — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT — 11 OF 20

PLT_RST# / XDP_DBRESET# / PM_RSMRST# → GPP_B13/PLTRST# / SYS_RESET# / RSMRST# (AN10, B5, AY17)
VCCST_PWRGD → PROCPWRGD / VCCST_PWRGD (A68, B65)
SYS_PWROK / PM_PCH_PWROK / PCH_DPWROK → SYS_PWROK / PCH_PWROK / DSW_PWROK (B6, BA20, BB20)
PM_SUSWARN# / PM_SUSACK# → GPP_A13/SUSWARN#/SUSPWRDNACK / GPP_A15/SUSACK# (AR13, AP11)
PCIE_WAKE# / GPD2/LAN_WAKE# → WAKE# / GPD2/LAN_WAKE# / GPD11/LANPHYPC / GPD7/RSVD#AT15 (BB15, AM15, AW17, AT15)

GPP_B12/SLP_S0# / GPD4/SLP_S3# / GPD5/SLP_S4# / GPD10/SLP_S5# → PM_SLP_S3# / PM_SLP_S4# (AT11, AP15, BA16, AY16)
SLP_SUS# / SLP_LAN# / GPD9/SLP_WLAN# / GPD6/SLP_A# (AN15, AW15, BB17, AN16)
GPD3/PWRBTN# / GPD1/ACPRESENT / GPD0/BATLOW# → PM_PWRBTN# / AC_PRESENT / BATLOW# (BA15, AY15, AU13)
GPP_A11/PME# / INTRUDER# → SM_INTRUDER# (AU11, AP16)
GPP_B11/EXT_PWR_GATE# / GPP_B2/VRALERT# → EXT_PWR_GATE# (AM10, AM11)

SKYLAKE-U-GP

PCH_PWROK / PM_RSMRST# — R2008 0R0402-PAD-1-GP — R2006 0R0402-PAD-1-GP

BATLOW#: Pull-up required even if not implemented.

3D3V_S5
BATLOW# / GPD2/LAN_WAKE# — RN2005 SRN10KJ-L-GP
PCIE_WAKE# / AC_PRESENT — RN2006 SRN10KJ-L-GP
PM_PWRBTN# — R2009 10KR2F-L1-GP

CPU

PM_SUSACK# — R2017 DY 0R2J-2-GP — PM_SUSWARN#

3D3V_S0
R2024 1KR2F-L1-GP
分 壓
ALL_SYS_PWRGD — R2020 10KR2F-L1-GP — VCCST_PWRGD
R2021 4K7R2J-L-GP
C2001 SC100P50V2JN-L-GP
Sensitive trace

-SB 20170316

3D3V_S5
RSMRST#_KBC / 3V_5V_POK → U2001 (A, B, VCC, GND, Y) → PM_RSMRST#
U74LVC1G08GW-R-GP-U
73.01G08.EHG
2nd = 73.7SZ08.DAH
C2002 SCD1U25V2KX-L-GP

3D3V_AUX_S5
R2004 100KR2J-3-GP
DY
R2005 10KR2F-L1-GP
3V_5V_POK_# — Q2001 (2N7002KDW-1-GP) — PM_RSMRST# / 3V_5V_POK_C
R2001 1KR2F-L-GP
R2002 0R0402-PAD-1-GP
RSMRST#_KBC / 3V_5V_POK
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

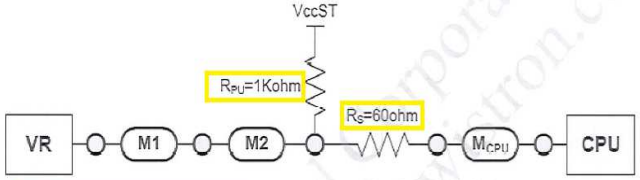
3D3V_S5
PM_SUSWARN# — R2030 DY 10KR2F-L1-GP
EXT_PWR_GATE# — R2031 DY 20KR2F-L3-GP
20170217 Change 20k
3D3V_RTC_AUX
SM_INTRUDER# — R2019 1MR2F-L-GP
PM_RSMRST# — R2010 10KR2F-L1-GP
PM_PCH_PWROK — R2011 DY 10KR2J-L-GP

3D3V_S0
R2014 10KR2F-L1-GP
XDP_DBRESET#
PLT_RST# — EC2020 DY SC22P50V2JN-L-GP
PM_PCH_PWROK — EC2002 DY SC10P50V2JN-L1-GP

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

VCCST_PWRGD / HWM201:

VCCST_PWRGOOD



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

GPP_A13-15 pin(LPC/eSPI):

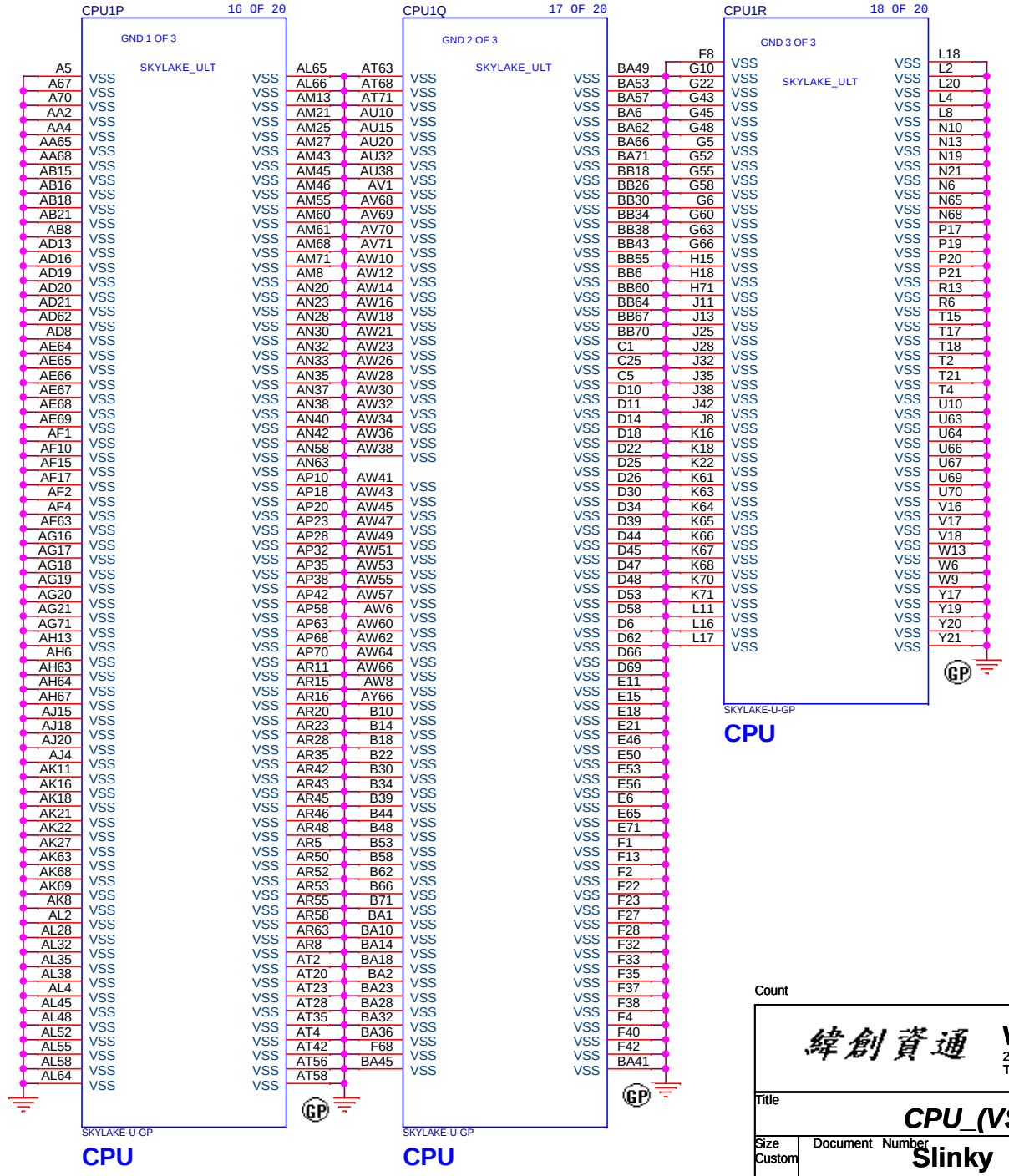
Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: Custom | Document Number: Slinky | Rev: -1
Date: Thursday, August 24, 2017 | Sheet 20 of 106

Main Func = PCH

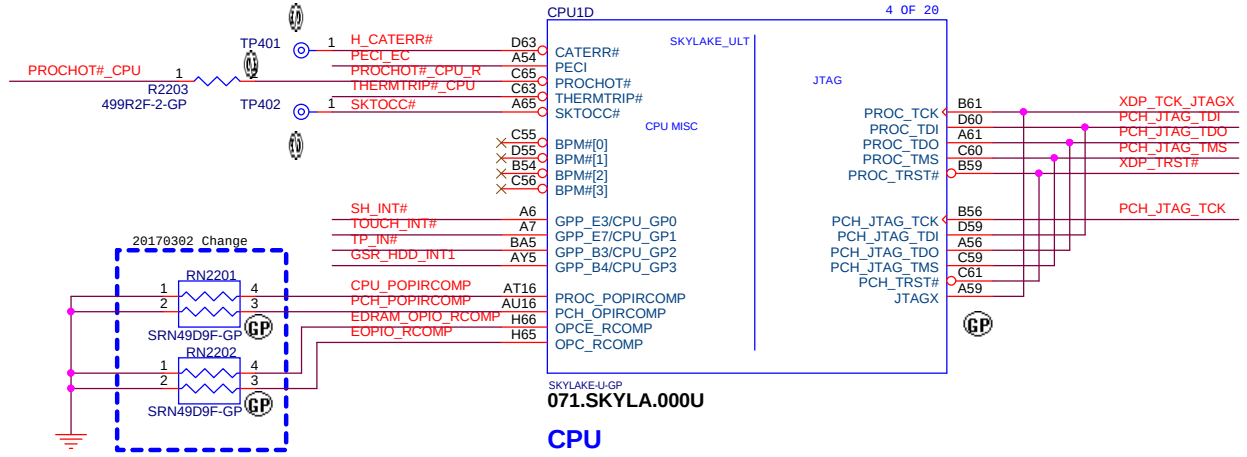


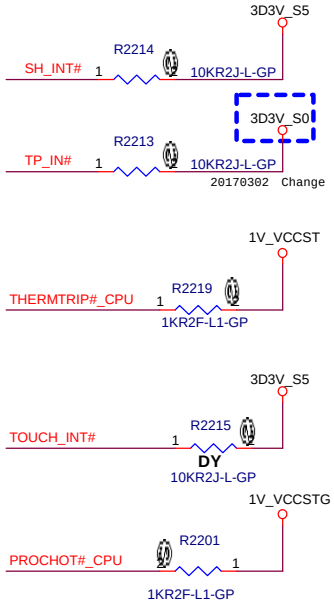
Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_(VSS)***	
Size Custom	Document Number **Slinky**	Rev -1
Date: Thursday, August 24, 2017	Sheet 21 of 106	

Main Func = CPU

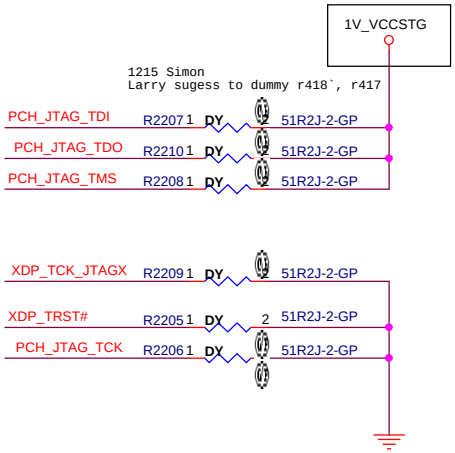
24 PECI_EC
24,44,46 PROCHOT#_CPU
24 SH_INT#
55 TOUCH_INT#
65 TP_IN#
69 GSR_HDD_INT1





PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

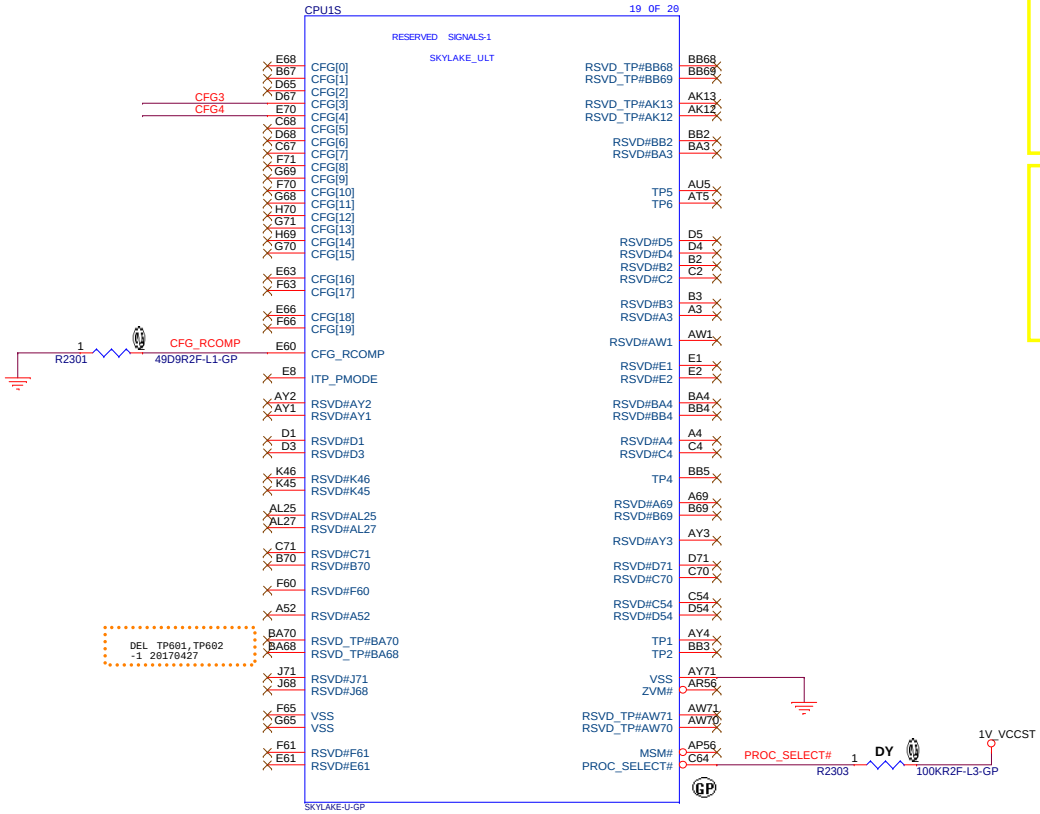
+VCCSTG = 1.0 V



Count

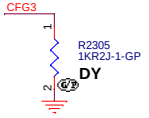
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_(JTAG/CPU SIDE BAND)***	
Size: Custom	Document Number: **Slinky**	Rev: **-1**
Date: Thursday, August 24, 2017	Sheet 22 of 106	

Main Func = CPU



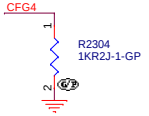
CPU

PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

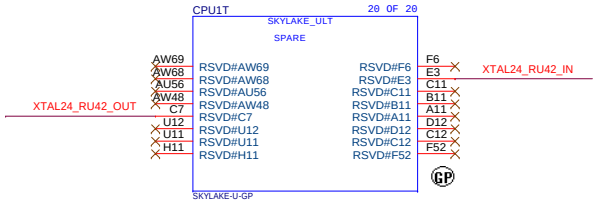
PCH strap pin:



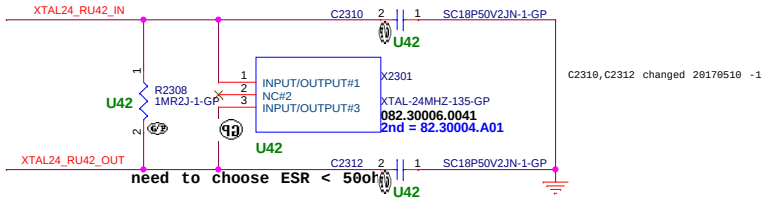
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines



CPU



P/N: 082.30006.0041

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_RESERVED,CFG**

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 23 of 106

SSID = KBC

Power

- 3D3V_AUX_S5
- 3D3V_S0
- 3D3V_RTC_AUX

Signal

- H_RCIN# 18
- FUN_OFF# 65,89
- LPC_FRAME#_CPU 18,68,91
- LPC_AD_CPU_P3 18,68,91
- LPC_AD_CPU_P2 18,68,91
- LPC_AD_CPU_P1 18,68,91
- LPC_AD_CPU_P0 18,68,91
- LPC_CLK_KBC 18
- PLT_RST# 20,61,62,68,89,91
- WLAN_PCIE_WAKE# 24,61
- LID_CLOSE# 64
- LID_CLOSE2# 64
- PTP_PWR_EN# 65
- PURE_HW_SHUTDOWN# 26,40
- PM_CLKRUN#_EC 18,91
- ES1_TXD 61,68
- SH_INT# 22
- EC_TP_INI# 24,65
- KBC_BEEP 27
- KB_BL_DET 65
- FAN1_PWM 26,89
- FAN_TACH1 26,89
- Value+ 64
- Value- 64
- KSI0 65,89
- KSI1 65,89
- KSI2 65,89
- KSI3 65,89
- KSI4 65,89
- KSI5 65,89
- KSI6 65,89
- KSI7 65,89
- KSO0 65,89
- KSO1 65,89
- KSO2 65,89
- KSO3 65,89
- KSO4 65,89
- KSO5 65,89
- KSO6 65,89
- KSO7 65,89
- KSO8 65,89
- KSO9 65,89
- KSO10 65,89
- KSO11 65,89
- KSO12 65,89
- KSO13 65,89
- KSO14 65,89
- KSO15 65,89
- KSO16 65,89
- KSO17 65,89
- AC_IN# 44,74
- DC_Protect_EC 44
- KBC_PWRBTN# 64,89
- BAT_IN# 43,44
- DC_IN_OK 44,73,74
- AD_IA 44
- BT_IA 44
- ALL_SYS_PWRGD 20,40
- MODEL_ID_AD 55
- STDBY_LED 64,89
- POWER_LED 64,89
- CHARGE_LED 64,89
- DC_BATFULL 64,89
- SML1_CLK 18,55,70,73
- SML1_DATA 18,55,70,73
- BAT_SCL 43,44
- BAT_SDA 43,44
- SPI_WP_ROM 18,25
- EC_TPCLK 65
- EC_TPDATA 65
- ME_UNLOCK 17
- EC_TP_INI 24,65
- RTCRST_ON 16
- BLON_OUT 55
- AD_OFF 43
- VD_IN1 26
- VD_OUT1 26
- PROCHOT#_CPU 22,44,46
- RSMRST#_KBC 20
- AMP_MUTE# 27
- 5V_EN 40,45
- KB_BL_PWM 65
- TOUCH_EN 55
- 3V_5S_ENABLE 40

- AC_PRESENT 20
- eDP_BLEN_CPU 3
- PM_PWRBTN# 20
- PCIE_WAKE# 20,61,62
- INT_SERIRQ 18,68,91
- EC_SMI# 3
- EC_SCI# 3

3.3V

- PM_SLP_S3# 20,40,45,53,60
- PM_SLP_S4# 20,40,51

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

- PD_INT# 73

Type_C

- USB_CHARGER_EN 36
- USB_CHAR_SEL 36
- USB_CHAR_CT1 36

Charger

- WIFI_RF_EN 61
- BLUETOOTH_EN 61,89
- USB_PWR_EN# 35,64
- WLAN_PCIE_WAKE# 24,61
- CHG_ON# 44
- PECI_EC 22
- WLAN_PERST# 61
- WLAN_PWR_EN# 61

- TS_I2C0_SCL_CON 6,55
- TS_I2C0_SDA_CON 6,55
- SYS_PWROK 20
- SPI_SO_ROM 18,25
- SPI_SI_ROM 18,25
- SPI_CLK_ROM 18,25
- SPI_CS_CPU_N0 18,25

Close to the EC

VCC_LPC(Pin9)

For EC power consumption reserver

68.00084.921
2nd = 68.00217.401

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

CPU/G-sensor/Type C --->
BATTER /CHARGER --->
CPU<---
Touch Pad--->

071.09028.000G

KB9028Q-C-GP

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Woody 13"	/	10.0K	
Buzz UMA 15"	0K	/	
Slinky 14"	100.0K	64.9K	2.001V
Reserved for project use	100.0K	76.8K	1.867V
Reserved for project use	100.0K	100.0K	1.650V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0K	10.0K	3.000V	3.005V	>=2.875V	
SB	100.0K	20.0K	2.750V	2.759V	>=2.616V	<2.875V
SC	100.0K	33.0K	2.481V	2.493V	>=2.363V	<2.616V
-1	100.0K	47.0K	2.245V	2.259V	>=2.123V	<2.363V
-2	100.0K	64.9K	2.001V	2.017V	>=1.934V	<2.123V
-3	100.0K	76.8K	1.867V	1.883V	>=1.758V	<1.934V
-4	100.0K	100.0K	1.650V	1.667V	>=1.504V	<1.758V
-5	100.0K	143.0K	1.358V	1.374V	>=1.281V	<1.504V
Reserved fot project use	100.0K	174.0K	1.204V	1.220V	>=1.126V	<1.281V
Reserved fot project use	100.0K	215.0K	1.048V	1.062V	>=0.524V	<1.126V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	78.8 K	100.0 K	1.453 V	1.469 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

close RN2407

GPIO0 High Active

Sensitive trace cap

Woody/Slinky 45W,Buzz UMA 65W Setting

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

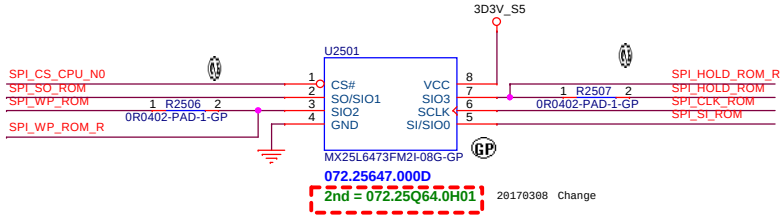
Title: KBC_KB9028
Size: Slinky
Document Number
Rev: -1
Date: Thursday, August 24, 2017
Sheet 24 of 106

18,24 SPI_CS_CPU_N0
18,24 SPI_SO_ROM
18 SPI_WP_ROM
14 SPI_WP_ROM_R
14 SPI_HOLD_ROM_R
18 SPI_HOLD_ROM
18,24 SPI_CLK_ROM
18,24 SPI_SI_ROM
6 RTC_DET#

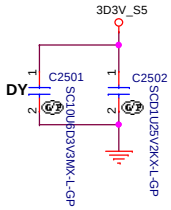
Main Func = SPI Flash

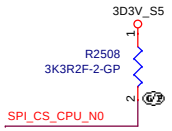
SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



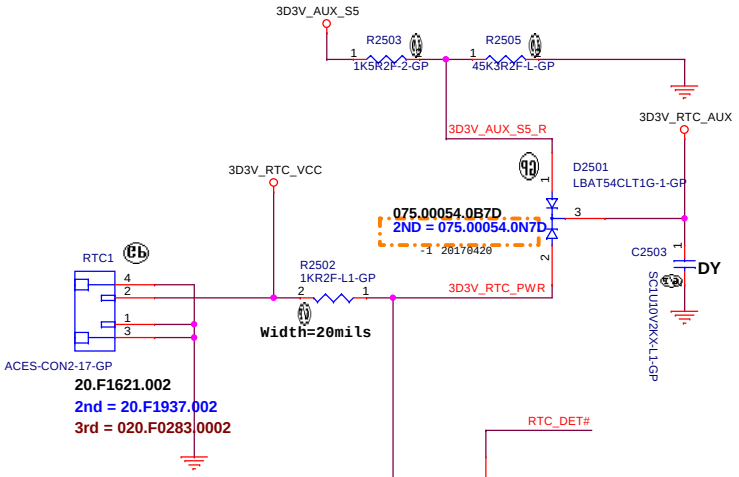
072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND





20170215 Delete U2504 For ENG

Main Func = RTC



RTC BATTERY
1st= 023.21212.0001
2nd= 023.22032.0621

Count

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Flash(KBC+PCH)/RTC*
Size: Custom	Document Number: Slinky
Rev	-1
Date: Thursday, August 24, 2017	Sheet 25 of 106

24 VD_IN1

24,26,89 FAN1_PWM

24,89 FAN_TACH1

24,40 PURE_HW_SHUTDOWN#

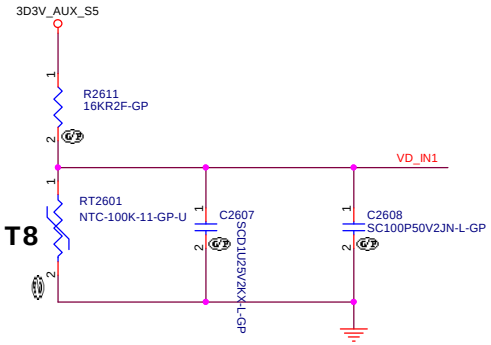
24 VD_OUT1

40,46 VR_RDY

89 FAN_TACH1_C

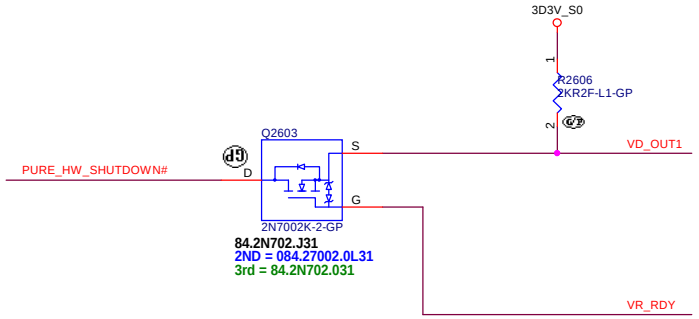
24,26,89 FAN1_PWM

SSID = Thermal

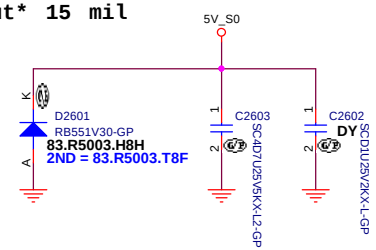


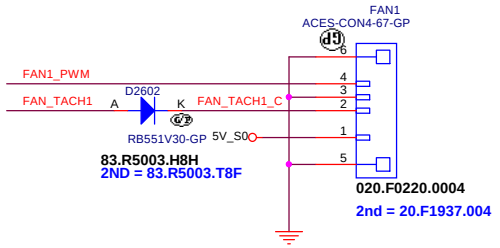
RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli



***Layout* 15 mil**





Count

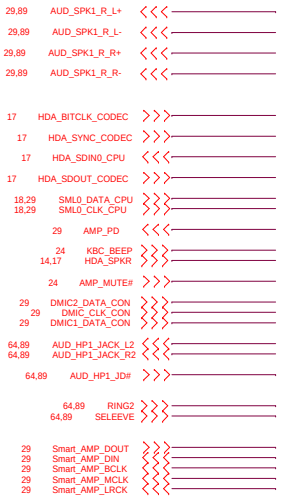
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

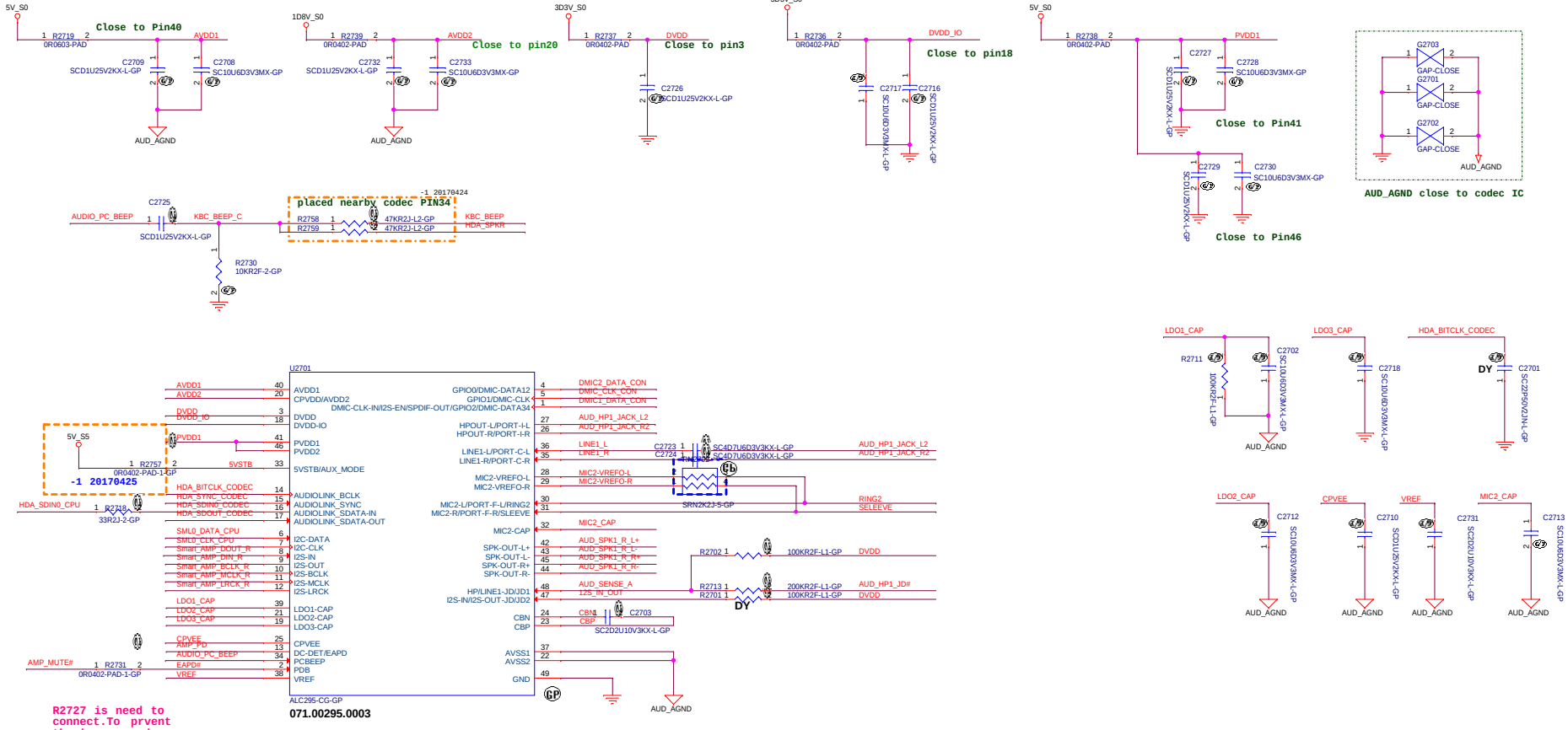
Title: ***Thermal 7718/Fan Controllor P2793***

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 26 of 106

SSID = AUDIO





Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Audio Codec ALC295		
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 27 of 106	

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 28 of 106

SSID = AUDIO

Amplifiers

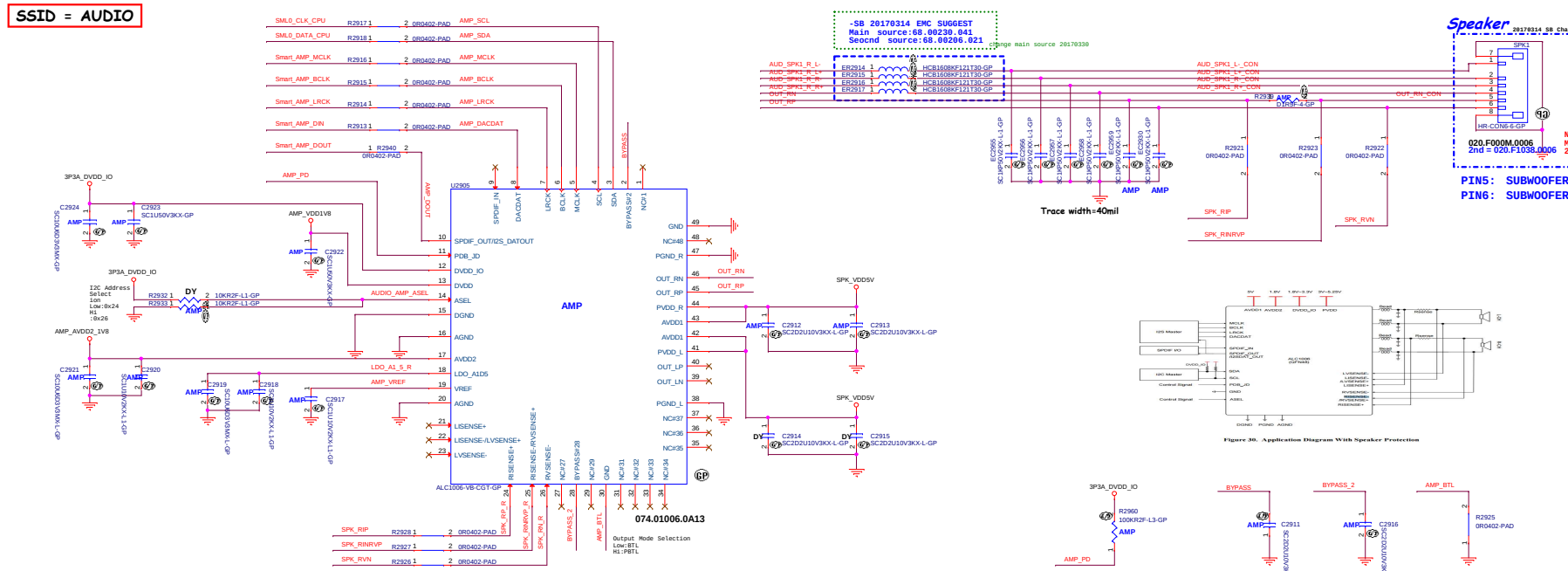
18,27 SML0_CLK_CPU
18,27 SML0_DATA_CPU
27 Smart_AMP_MCLK
27 Smart_AMP_BCLK
27 Smart_AMP_LRCK
27 Smart_AMP_DIN
27 Smart_AMP_DOUT
27 AMP_PD
27,89 AUD_SPK1_R_L-
27,89 AUD_SPK1_R_L+
27,89 AUD_SPK1_R_R-
27,89 AUD_SPK1_R_R+
89 OUT_RN_CON
89 OUT_RP
89 SPK_RINRVP

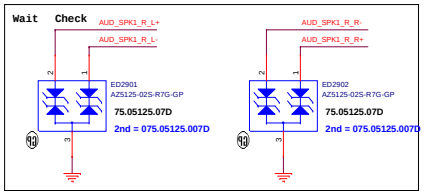
CCD

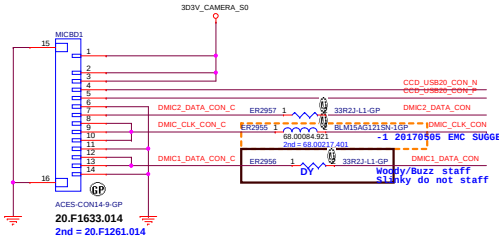
15 CCD_USB20_P
15 CCD_USB20_N
89 CCD_USB20_CON_P
89 CCD_USB20_CON_N

DMIC

27 DMIC_CLK_CON
27 DMIC1_DATA_CON
27 DMIC2_DATA_CON
89 DMIC_CLK_CON_C
89 DMIC1_DATA_CON_C
89 DMIC2_DATA_CON_C







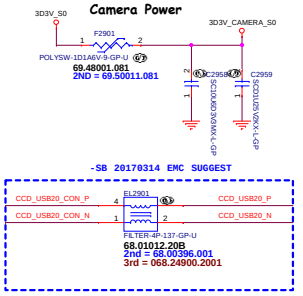
A. Pin define

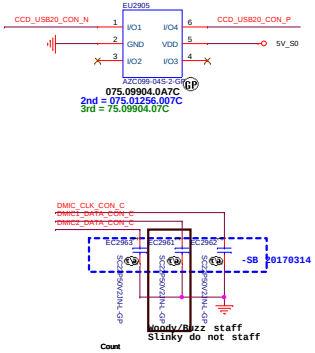
Note

CCD Module

MB Connecter		CCD connector pin	MIC-R PCB	MIC-L PCB
Pin 1	3D3V_CAMERA_S0	1		
Pin 2	3D3V_CAMERA_S0		1	
Pin 3	3D3V_CAMERA_S0			1
Pin 4	CCD_USB20_CON_N	2		
Pin 5	CCD_USB20_CON_P	3		
Pin 6	GND	4		
Pin 7	DMIC2_DATA_CON	6		
Pin 8	DMIC_CLK_CON	5		
Pin 9	DMIC_CLK_CON		3	
Pin 10	DMIC_CLK_CON			3
Pin 11	GND		4	
Pin 12	DMIC1_DATA_CON		2	
Pin 13	DMIC1_DATA_CON			2
Pin 14	GND			4

MB Connecter	CCD Connecter





Count

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Speaker/AMP/DMIC	
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 29 of 106	

Blanking

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **Slinky**	Rev: **-1**
Date: Thursday, August 24, 2017	Sheet 30 of 106	

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 31 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 32 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 33 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 34 of 106

USB1

15 USB1_USB20_N
15 USB1_USB20_P

15 USB1_USB30_RX_N
15 USB1_USB30_RX_P

15 USB1_USB30_TX_N
15 USB1_USB30_TX_P

89 USB1_CON_USB20_N
89 USB1_CON_USB20_P

USB2

36 USB2_CHAR_N
36 USB2_CHAR_P

15 USB2_USB30_RX_N
15 USB2_USB30_RX_P

15 USB2_USB30_TX_N
15 USB2_USB30_TX_P

89 USB2_CON_USB20_N
89 USB2_CON_USB20_P

USB Power enable

24,64 USB_PWR_EN#

Low Active 2A

5V_S5 — C3501 SC1U10V2KX-L1-GP — USB_PWR_EN# — U3501 SY6288DAAC-GP (IN, EN#, OUT, GND, OC#)

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

5V_USB30 — 0R3F-1-GP-U 1 — R3501 — 5V_USB30_CHARGER

NON USB CHARGE

C3502 SCD1U25V2KX-L-GP

5V_USB30 — C3504 SC100U6D3V6MX-GP

5V_USB30_CHARGER — C3516 SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

EU3501 — L05ESDL5V0NA-4-GP

USB1_USB30_RX_N / USB1_USB30_RX_P / USB1_USB30_TX_N / USB1_USB30_TX_P — SCD1U25V2KX-L-GP — C3508 / C3509

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30 — USB1 (SKT-USB13-348-GP-U)

20170309 Change
20170324 Change symbol

VBUS, D-, D+, GND-DRAIN, CHASSIS#12, CHASSIS#13, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND, USB3.0

022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

EL3501 — FILTER-4P-137-GP-U

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

EU3503 — AZC099-04S-2-GP

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

EU3502 — L05ESDL5V0NA-4-GP

USB2_USB30_RX_N / USB2_USB30_RX_P / USB2_USB30_TX_N / USB2_USB30_TX_P — SCD1U25V2KX-L-GP — C3510 / C3511

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30_CHARGER — USB2 (SKT-USB13-348-GP-U)

20170309 Change
20170324 Change symbol

022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

EL3502 — FILTER-4P-137-GP-U

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

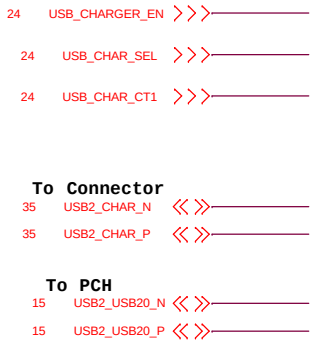
Count

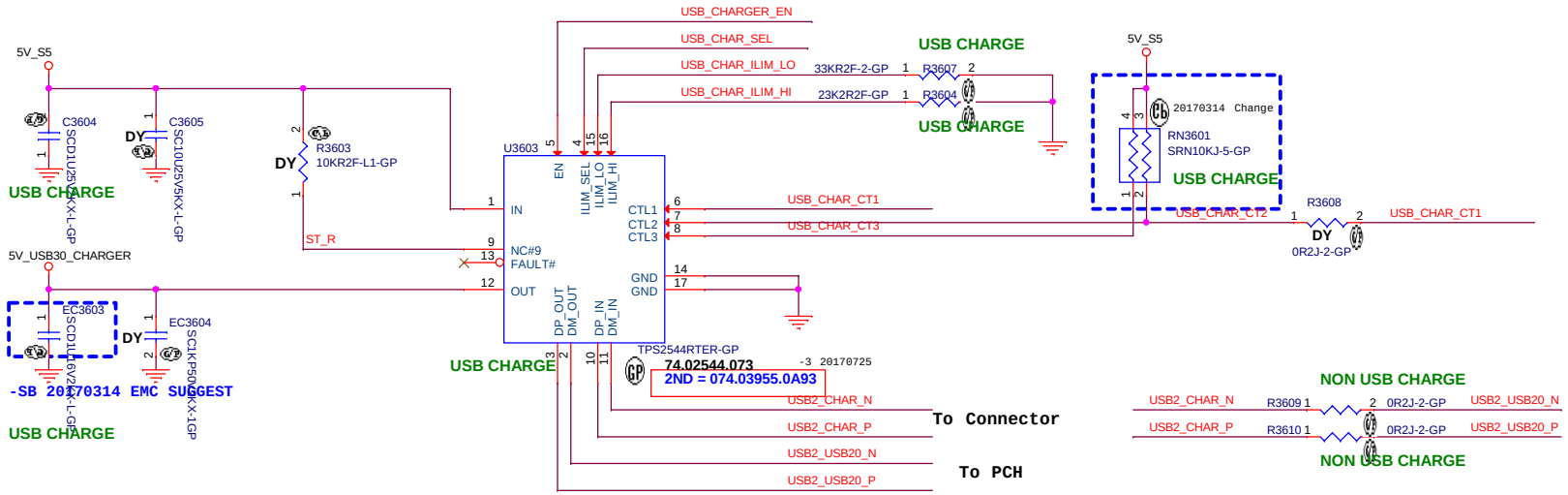
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 35 of 106





CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB CHARGER***

Size: Custom | Document Number: **Slinky** | Rev: **-1**

Date: Thursday, August 24, 2017 | Sheet 36 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 37 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 38 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 39 of 106

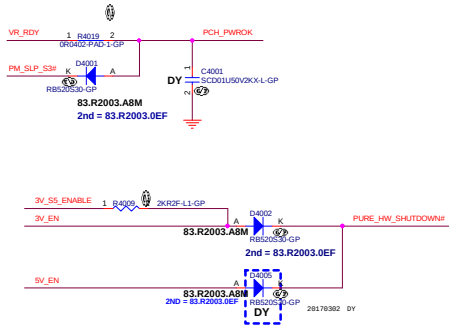
Power Sequence

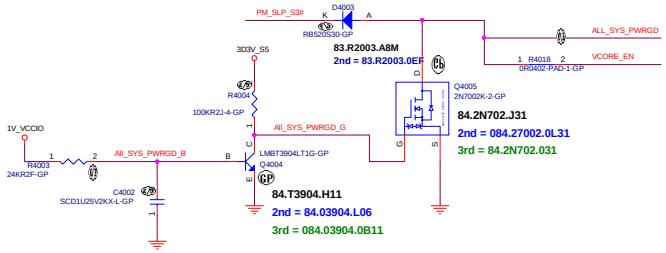
26,46 VR_RDY
20 PCH_PWROK
20,24,40,45,53,60 PM_SLP_S3#
24 3V_S5_ENABLE
45 3V_EN
24,45 5V_EN
34,26 PURE_HW_SHUTDOWN#
20,24 ALL_SYS_PWRGD
46 VCORE_EN

Run Power

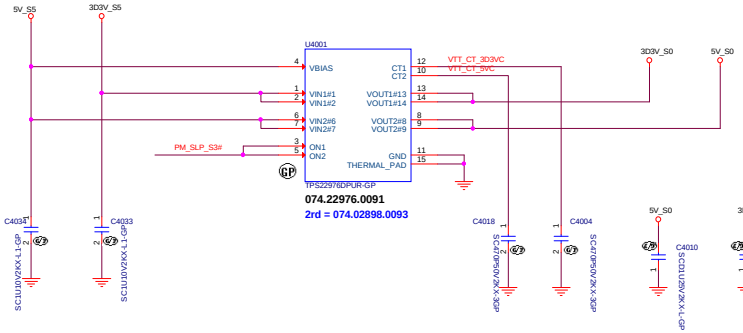
20,24,51 PM_SLP_S4#
20,24,40,45,53,60 PM_SLP_S3#

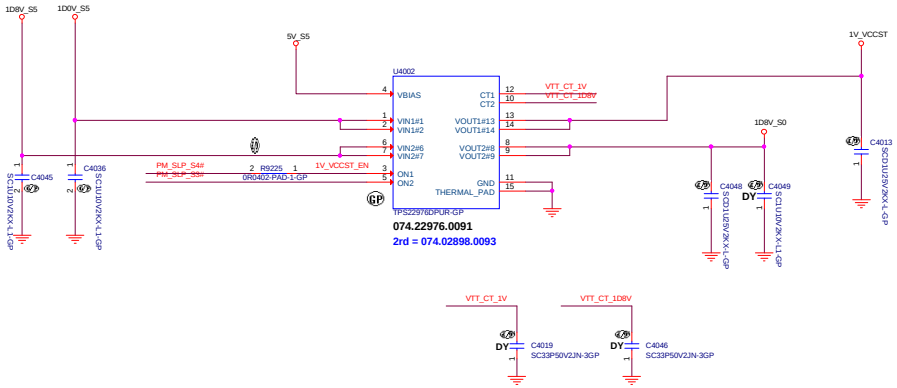
Power Sequence

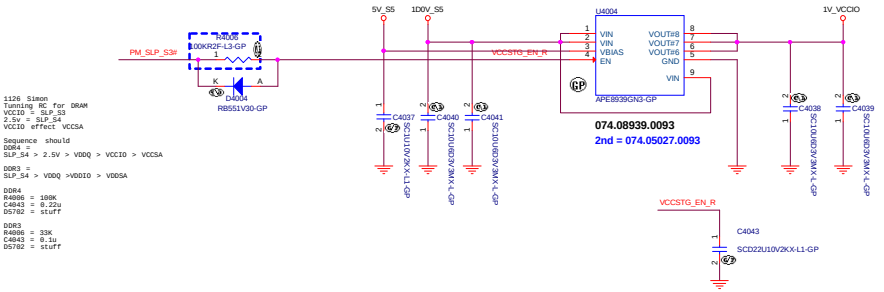




ANNIE Run Power







Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 40 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 41 of 106

Blanking

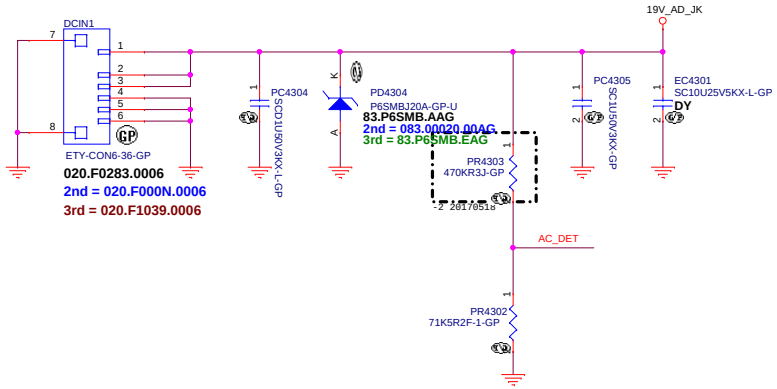
Count

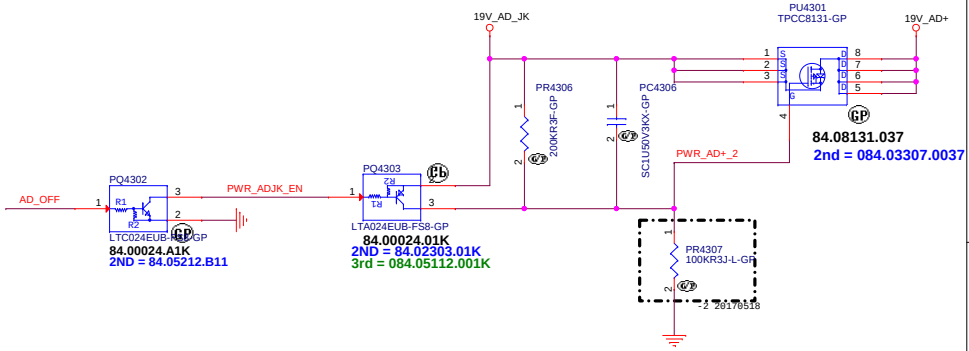
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Slinky**
Rev	**-1**
Date: Thursday, August 24, 2017	Sheet 42 of 106

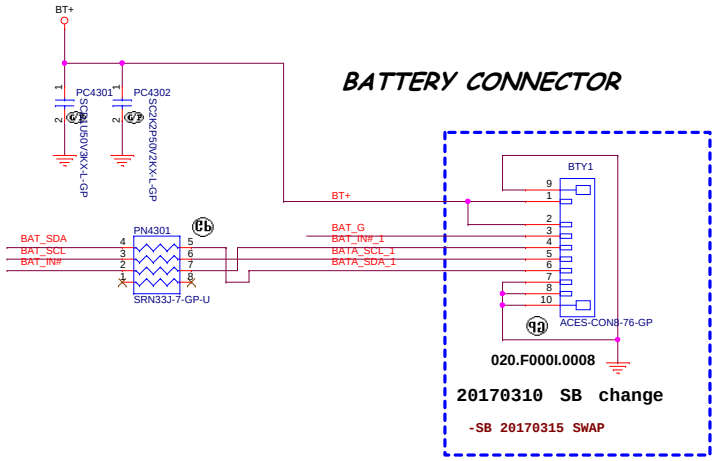
24 AD_OFF
24,44 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA
89 BAT_G
89 BAT_IN#_1
89 BATA_SCL_1
89 BATA_SDA_1
64 BAT_RST
74 AC_DET

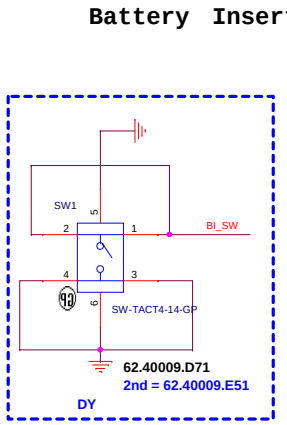
ANNIE solution

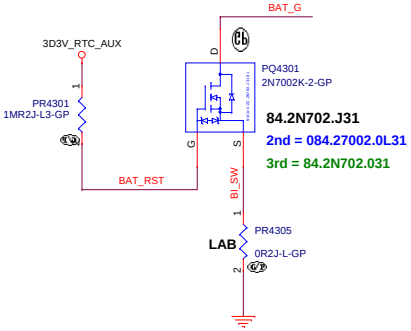
Adaptor in to generate DCBATOUT







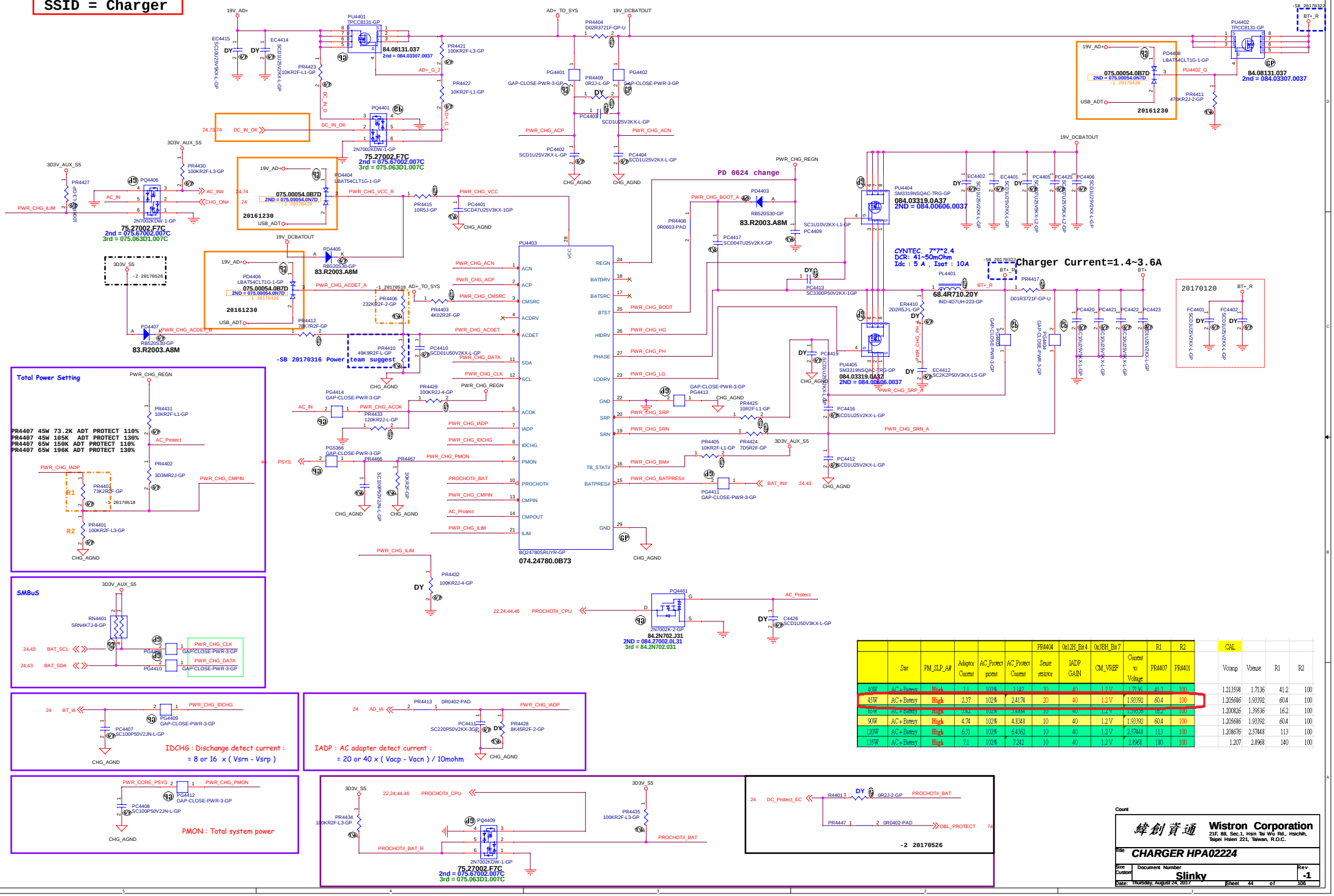




Count

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT CONN	
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 43 of 106	

SSID = Charger



	Stat	PM_SLP_A#	Adaptor Current	AC_Protect protect	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit 4 IADP GAIN	0x3BH_Bit 7 CM_VREF	Current to Voltage	R1 PR4407	R2 PR4401	CAL Vcomp	Vsense	R1	R2
40W	AC + Battery	High	2.1	102%	2.142	20	40	1.2 V	1.71396	41.2	100	1.213598	1.7136	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.395576	16.2	100	1.200826	1.39536	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100	1.208676	2.57448	113	100
135W	AC + Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	180	100	1.207	2.8968	140	100

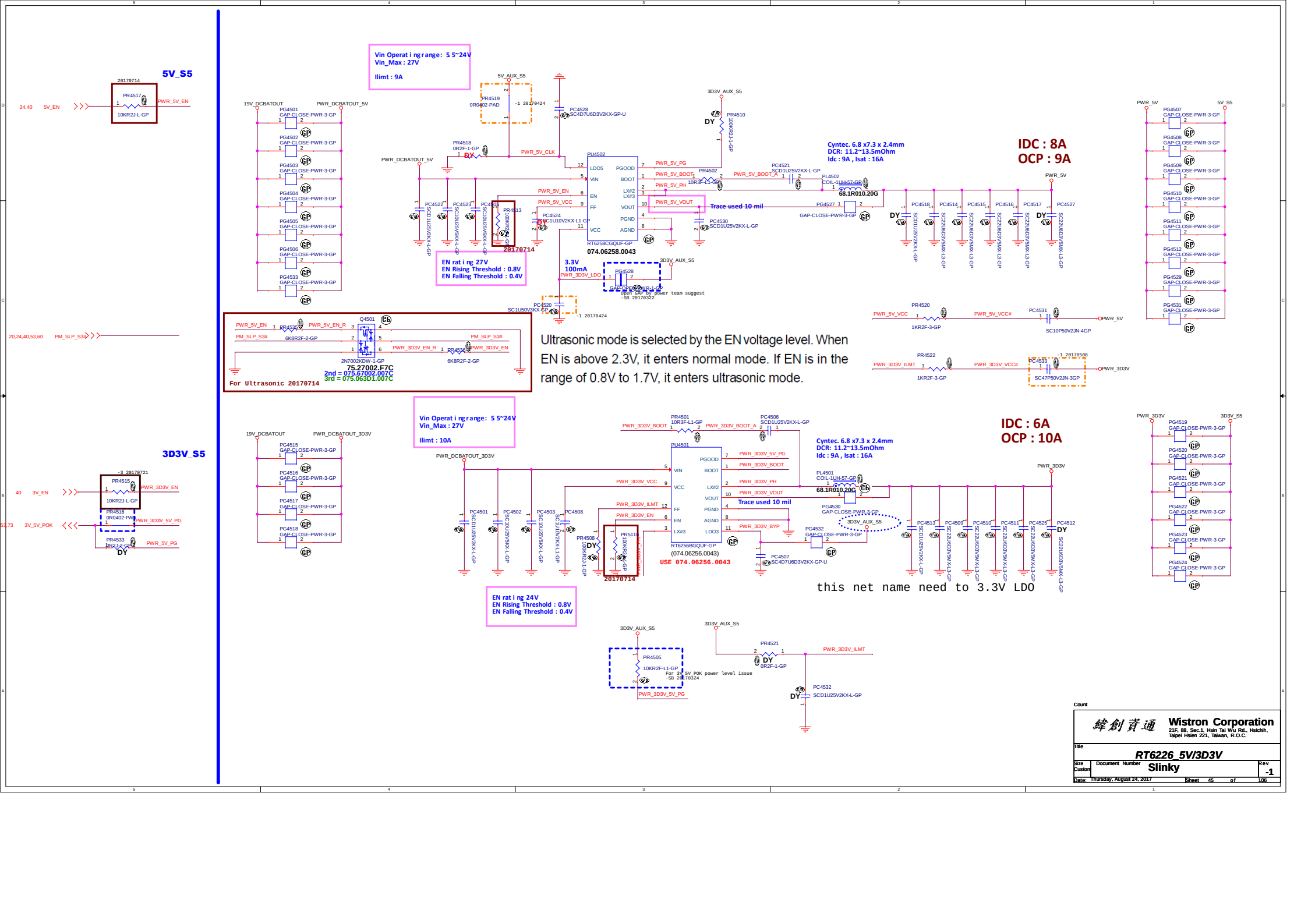
Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 44 of 106


5V_S5
3D3V_S5
Vin Operating range: 5.5~24V
Vin_Max : 27V
Ilimt : 9A
IDC : 8A
OCP : 9A
Cyntec. 6.8 x7.3 x 2.4mm
DCR: 11.2~13.5mOhm
Idc : 9A , Isat : 16A
Trace used 10 mil
EN rating 27V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
3.3V
100mA
Ultrasonic mode is selected by the EN voltage level. When EN is above 2.3V, it enters normal mode. If EN is in the range of 0.8V to 1.7V, it enters ultrasonic mode.
For Ultrasonic 20170714
Vin Operating range: 5.5~24V
Vin_Max : 27V
Ilimt : 10A
IDC : 6A
OCP : 10A
EN rating 24V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
this net name need to 3.3V LDO
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
RT6226_5V/3D3V
Slinky
Thursday, August 24, 2017

Main Func = CPU_CORE

OFFPAGE

22,24,44 PROCHOT#_CPU
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
26,40 VR_RDY
40 VCORE_EN
7 VSSCORE_SENSE
7 VCCCORE_SENSE
8 VCCGT_SENSE
8 VSSGT_SENSE
8 VSSSA_SENSE
8 VCCSA_SENSE
44 PSYS

50 PWR_VCCSA_ISUMP
50 PWR_VCCSA_ISUMN
48 PWR_VCCGT_ISUMP
48 PWR_VCCGT_ISUMN
47 PWR_VCORE_ISUMP_A
47 PWR_VCORE_ISUMN_A
47 PWR_VCORE_ISUMP_B
47 PWR_VCORE_ISUMN_B

50 PWR_VCCSA_PWM
48 PWR_VCCGT_PWM
47 PWR_VCORE_PWMA
46,47 PWR_VCORE_PWMB
46,47 PWR_VCORE_PWMB
47,48,50 PWR_VCORE_FCCM#

Location	U22		U42	
PR4640	28K	64.28025.6DL	31.6K	64.31625.6DL
PR4659	47.5k	64.47525.6DL	52.3K	64.52325.6DL

BOM CONTROL U22 28K U42 31.6K

BOM CONTROL U22 47.5K U42 52.3K

	PR4652	PR4682
U22	0	0
U42	DY	DY

	PR4684
U22	DY
U42	1R

Jason 0104

RT3602AEGQW-GP
074.03602.0073

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)

Size: Custom | Document Number: Slinky | Rev: -1

Date: Friday, September 29, 2017 | Sheet 46 of 106

Main Func = CPU_CORE

46 PWR_VCORE_ISUMP_A
46 PWR_VCORE_ISUMN_A
46 PWR_VCORE_PWMA
46,48,50 PWR_VCORE_FCCM#
46 PWR_VCORE_ISUMP_B
46 PWR_VCORE_ISUMN_B
46 PWR_VCORE_PWMB

19V_DCBATOUT PWR_DCBATOUT_VCOREA
PG4702 PG4703 PG4704 PG4705 PG4706 PG4707 PG4708 PG4709
GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCOREA
PC4702 PC4703 PC4704 PC4705
SC1U25V5KX-L-GP

PU4702
AOZ5049QI-1-GP
PWR_VCORE_BOOTA
PWR_VCORE_VCCDA
PWR_DCBATOUT_VCOREA
PWR_VCORE_PHASEDA
PWR_VCORE_SWA
PWR_VCORE_BOOTA_RC
PWR_VCORE_PWM_RA
PWR_VCORE_FCCMA
PWR_VCORE_PWMA
PWR_VCORE_FCCMB
5V_S5
PR4702 2D2R2F-GP
PC4706 SC1U10V2KX-L1-GP
PC4707 SCD22U25V3KX-GP
PR4703 2D2R3-1-U-GP
PR4704 0R0402-PAD-1-GP
PR4705 0R0402-PAD-1-GP

074.05049.0A73

SKL_U42
Icc(max)=64A
TDC=42A
Confirm with EE
22uF/0805 total 32pcs
(78.22610.L2L)

Cyntec 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A
PL4702
COIL-D15UH-8-GP
068.R1510.2091
2nd = 068.R1510.2111
PG4706 PG4707
GAP-CLOSE-PWR-3-GP

1V_CPU_CORE
PT4702
SE330U2VDM-4-GP
79.33719.20C
2nd = 077.53371.0081
PANASONIC
ESR: 9 mohm

PWR_VCORE_ISEN1P_GA
PR4708 360R2F-GP
PC4708 SCD47U25V3KX-1GP
PR4709 10KR2F-L1-GP
PWR_VCORE_ISUMP_A
PWR_VCORE_ISUMN_A
CLOSE to IC

PWR_VCORE_SWA
PR4707 2D2R6J-3-GP
PWR_VCORE_SNB
PC4709 SC1KP50V2KX-L-1-GP

PWR_DCBATOUT_VCOREB
PC4701 PC4711 PC4712 PC4710
SC1U25V5KX-L-GP

PU4701
AOZ5049QI-1-GP
PWR_VCORE_BOOTB
PWR_VCORE_VCCDB
PWR_DCBATOUT_VCOREB
PWR_VCORE_PHASEDB
PWR_VCORE_SWB
PWR_VCORE_BOOTB_RC
PWR_VCORE_PWM_RB
PWR_VCORE_FCCMB
PWR_VCORE_PWMB
PWR_VCORE_FCCMB
5V_S5
PR4710 2D2R2F-GP
PC4713 SC1U10V2KX-L1-GP
PC4714 SCD22U25V3KX-GP
PR4711 2D2R3-1-U-GP
PR4701 0R0402-PAD-1-GP
PR4712 0R0402-PAD-1-GP

074.05049.0A73

SKL_U42
Icc(max)=64A
TDC=42A
Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A
PL4701
COIL-D15UH-8-GP
068.R1510.2091
2nd = 068.R1510.2111
PG4713 PG4714
GAP-CLOSE-PWR-3-GP

1V_CPU_CORE
PT4701
SE330U2VDM-4-GP
79.33719.20C
2nd = 077.53371.0081
PANASONIC
ESR: 9 mohm

PWR_VCORE_ISENP_GA
PR4715 360R2F-GP
PC4715 SCD47U25V3KX-1GP
PR4716 10KR2F-L1-GP
PWR_VCORE_ISUMP_B
PWR_VCORE_ISUMN_B
CLOSE to IC

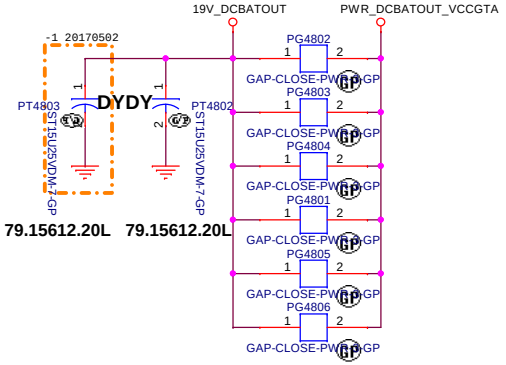
PWR_VCORE_SWB
PR4714 2D2R6J-3-GP
PWR_VCORE_SNB_B
PC4716 SC1KP50V2KX-L-1-GP

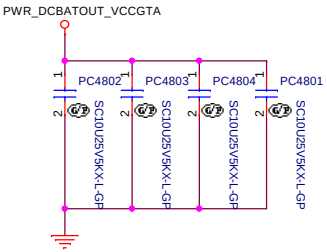
Count

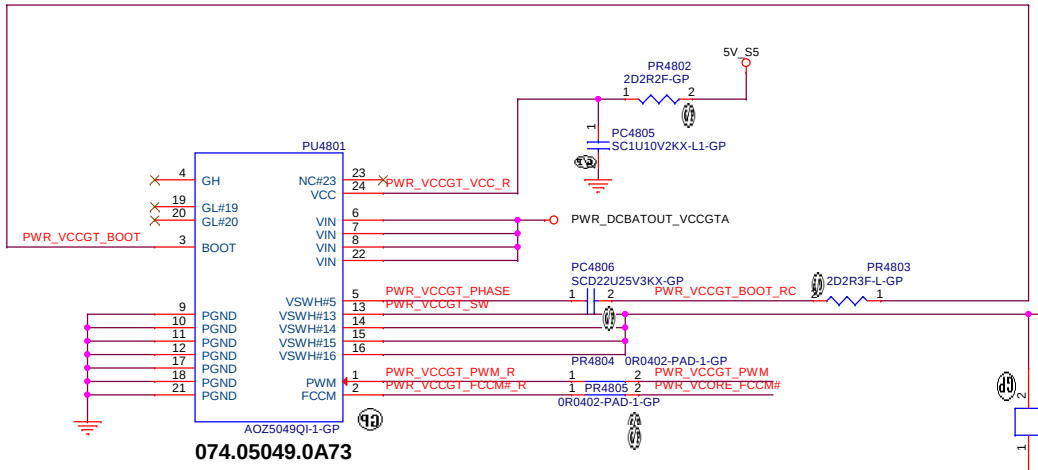
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_VCORE(2/3)
Size: Custom	Document Number: Slinky
Rev	-1
Date: Thursday, August 24, 2017	Sheet 47 of 106

Main Func = CPU_CORE

46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN
46 PWR_VCCGT_PWM
46,47,50 PWR_VCORE_FCCM#



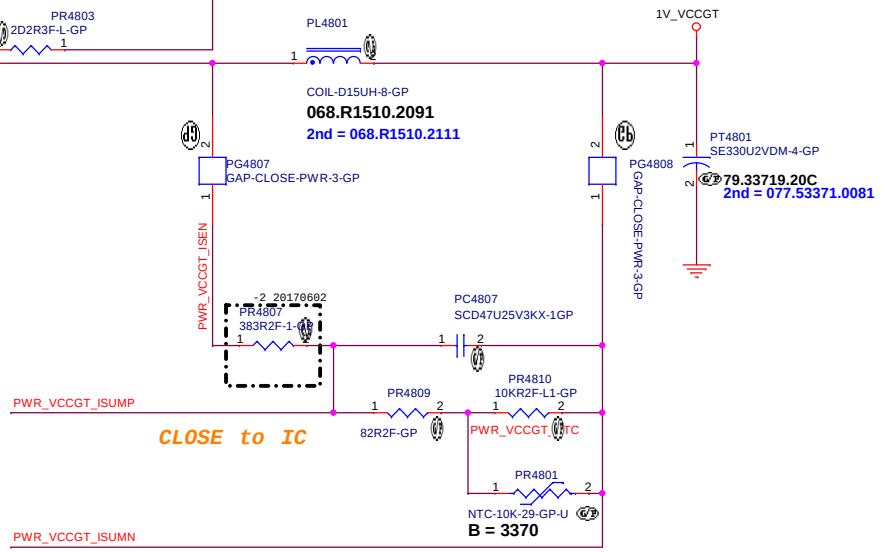


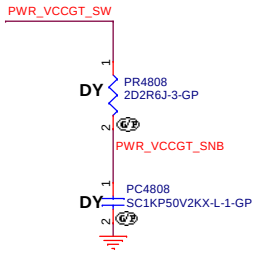


SKL_U42
Icc(max)=28A
TDC=12A

Confir mwith EE
22uF/0805 total 26pcs
(78.22610.L2L)

Cyntec 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A





Location	U22		U42	
PR4807	430ohm	64.43005.6DL	324ohm	64.32405.6DL

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_VCCGT(3/3)**

Size	Document Number	Rev
A3	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 48 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 49 of 106

Main Func = CPU_CORE

46,47,48 PWR_VCORE_FCCM#
46 PWR_VCCSA_PWM
46 PWR_VCCSA_ISUMP
46 PWR_VCCSA_ISUMN

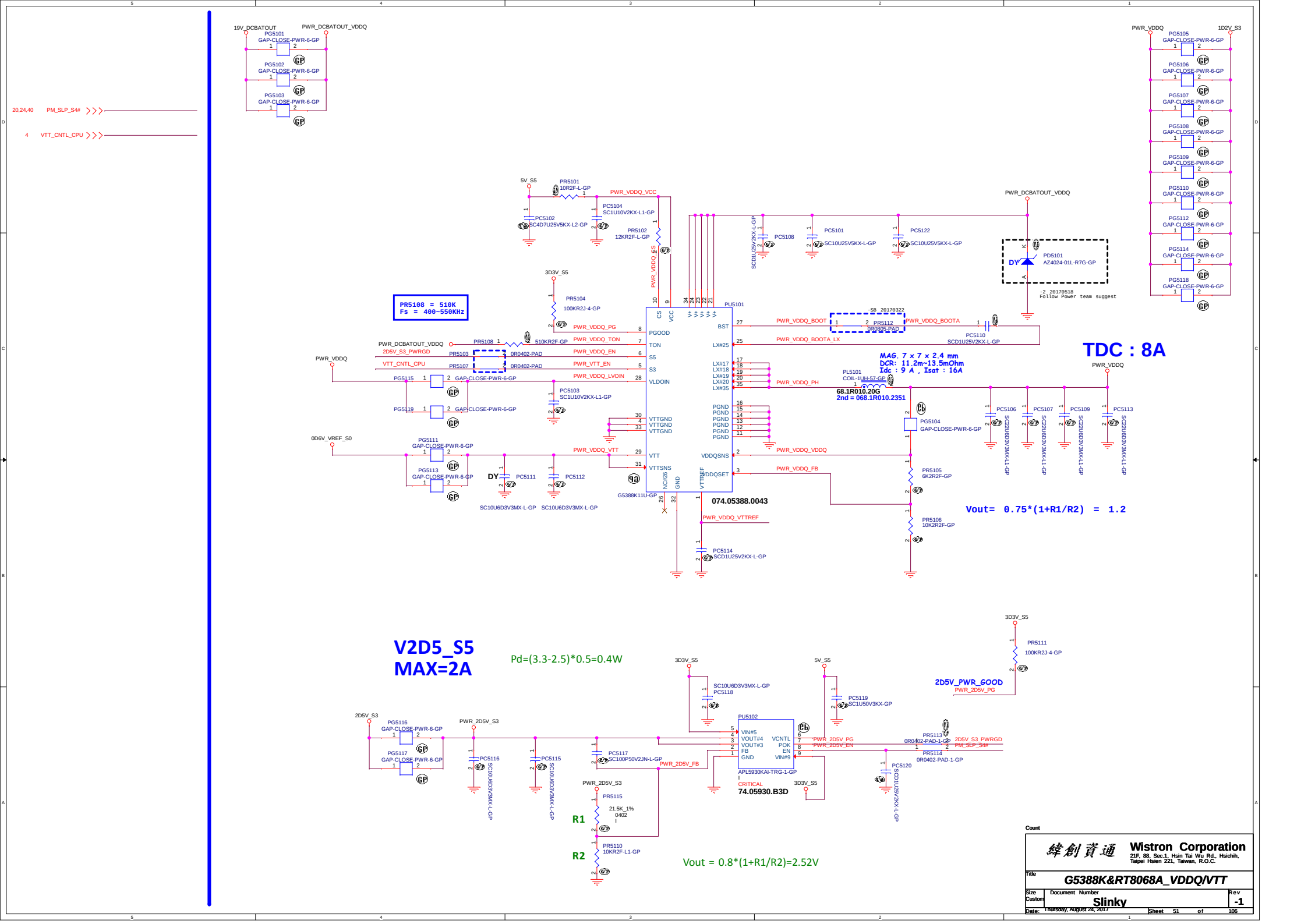
19V_DCBATOUT
PWR_DCBATOUT_VCCSA
PG5002 GAP-CLOSE-PWR-3-GP
PG5003 GAP-CLOSE-PWR-3-GP

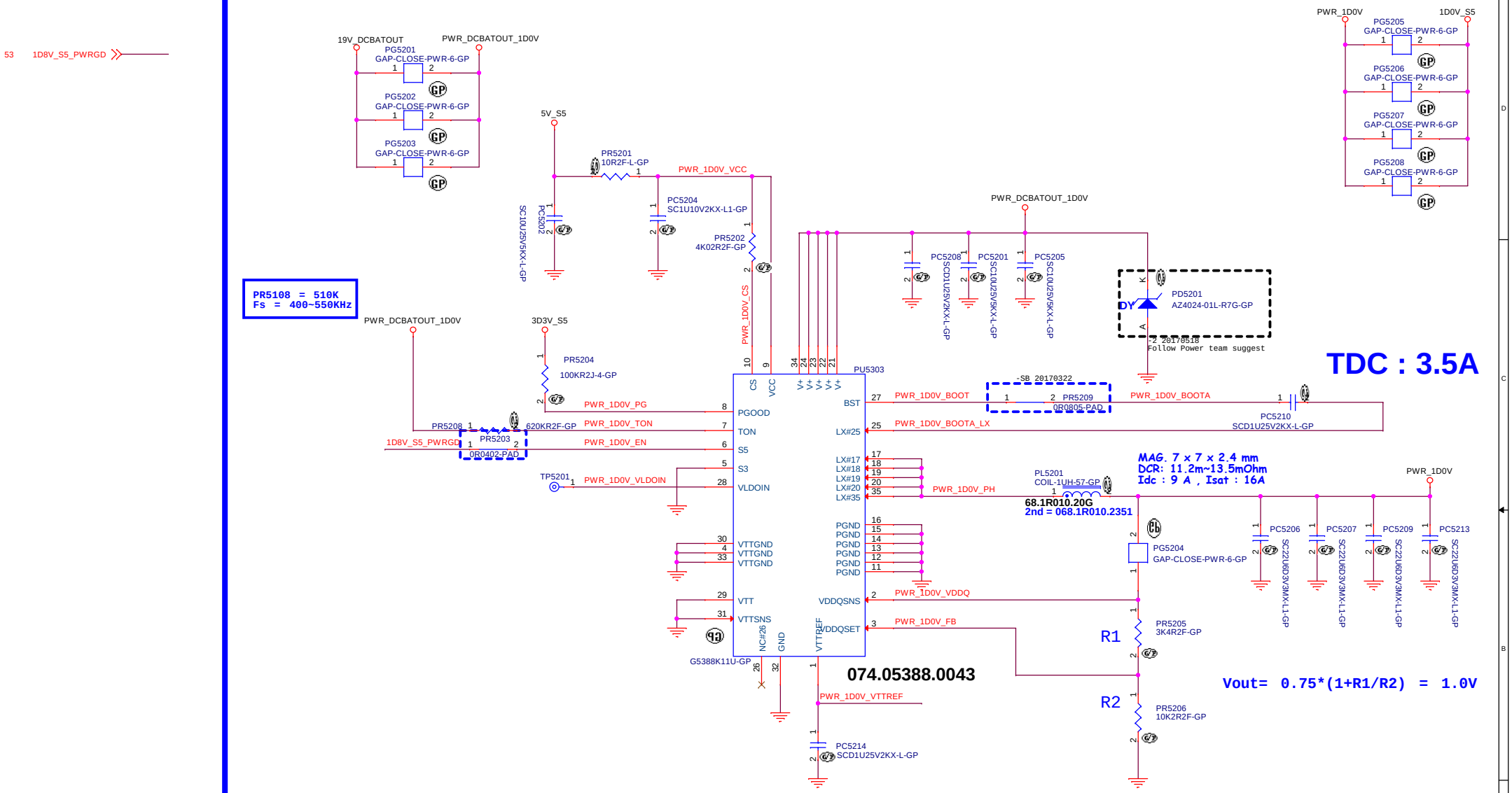
SKL_U42/U22/U23e
Icc(max)=5.1A
TDC=5A
Confirm with EE
22uF/0805 total 5pcs
(78.22610.L2L)

5V_S5
5V_S0
-1 20170502
PR5003 0R0402-PAD
PR5002 0R2J-2-GP
DY
VCCSA_POWER
PC5001 SCD22U10V3KX-L-GP
PR5001 2D2R3F-L-GP
PWR_VCCSA_BST
PWR_VCCSA_BST_RC
PC5005 SCD22U25V3KX-GP
PU5004
VCC BOOT
EN UGATE
PWM PHASE
GND LGATE
GND
RT9610BZQW-GP
74.09610.0E3
PR5010 0R0402-PAD
PR5011 0R0402-PAD
PWR_VCORE_FCCM#
PWR_VCCSA_FCCM#
PWR_VCCSA_PWM
PWR_VCCSA_PWM_A
PR5008 100KR2F-L3-GP
PWR_VCCSA_DRVH
PWR_VCCSA_SW
PWR_VCCSA_DRVL
PU5001 SM3319NSQAC-TRG-GP
084.03319.0A37
2nd = 084.00606.0037
PU5003 SM3319NSQAC-TRG-GP
084.03319.0A37
2nd = 084.00606.0037
PWR_DCBATOUT_VCCSA
PC5002 SC10U25V5KX-L-GP
PC5003 SC10U25V5KX-L-GP
PC5004 SCD1U25V2KX-L-GP
MAG. 7 x 7 x 2.4 mm
DCR: 4.5m~5.1 mOhm
Idc : 15 A , Isat : 22A
PL5001 COIL-D47UH-20-GP
068.R4710.2011
068.R4710.2201
1V_VCCSA
PG5011 GAP-CLOSE-PWR-3-GP
PG5001 GAP-CLOSE-PWR-3-GP
PWR_VCCSA_ISEN1P_GB
-1 20170508
PR5005 309R2F-GP
PC5006 SCD47U25V3KX-1GP
PR5007 1R2F-L-GP
PR5006 3KR2F-GP
PWR_VCCSA_ISUMP
PWR_VCCSA_ISEN1P_GB
CLOSE to IC
PR5004 NTC-10K-29-GP-U
B = 3370
PWR_VCCSA_ISUMN
PR5009 2D2R6J-3-GP
PWR_VCCSA_SNB
PC5007 SC1KP50V2KX-L-1-GP

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VCCSA		
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 50 of 106	


20,24,40 PM_SLP_S4#
4 VTT_CNTL_CPU
19V_DCBATOUT
PWR_DCBATOUT_VDDQ
PG5101 GAP-CLOSE-PWR-6-GP
PG5102 GAP-CLOSE-PWR-6-GP
PG5103 GAP-CLOSE-PWR-6-GP
PWR_VDDQ
1D2V_S3
PG5105 GAP-CLOSE-PWR-6-GP
PG5106 GAP-CLOSE-PWR-6-GP
PG5107 GAP-CLOSE-PWR-6-GP
PG5108 GAP-CLOSE-PWR-6-GP
PG5109 GAP-CLOSE-PWR-6-GP
PG5110 GAP-CLOSE-PWR-6-GP
PG5112 GAP-CLOSE-PWR-6-GP
PG5114 GAP-CLOSE-PWR-6-GP
PG5118 GAP-CLOSE-PWR-6-GP
5V_S5
PR5101 10R2F-L-GP
PWR_VDDQ_VCC
PC5102 SC4D7U25V5KX-L2-GP
PC5104 SC1U10V2KX-L1-GP
PR5102 12KR2F-L-GP
PWR_VDDQ_SS
PC5108 SCD1U25V2KX-L-GP
PC5101 SC10U25V5KX-L-GP
PC5122 SC10U25V5KX-L-GP
PD5101 AZ4024-01L-R7G-GP
-2 20170518
Follow Power team suggest
3D3V_S5
PR5104 100KR2J-4-GP
PR5108 = 510K
Fs = 400~550KHz
PR5108 510KR2F-GP
PWR_VDDQ_PG
PWR_VDDQ_TON
PWR_VDDQ_EN
PWR_VDDQ_VTT_EN
PWR_VDDQ_LVOIN
PU5101
CS
VCC
PGOOD
TON
S5
S3
VLDOIN
VTTGND
VTTSNS
VTTREF
VDDQSNS
VDDQSET
GND
NC#26
G5388K11U-GP
BST
LX#25
PWR_VDDQ_BOOT
PWR_VDDQ_BOOTA
PR5112 0R0805-PAD
PWR_VDDQ_BOOTA_LX
PC5110 SCD1U25V2KX-L-GP
PWR_VDDQ_PH
PL5101 COIL-1UH-57-GP
68.1R010.20G
2nd = 068.1R010.2351
MAG. 7 x 7 x 2.4 mm
DCR: 11.2m~13.5mOhm
Idc : 9 A , Isat : 16A
TDC : 8A
PWR_DCBATOUT_VDDQ
2D5V_S3_PWRGD
PR5103 0R0402-PAD
VTT_CNTL_CPU
PR5107 0R0402-PAD
PG5115 GAP-CLOSE-PWR-6-GP
PG5119 GAP-CLOSE-PWR-6-GP
PC5103 SC1U10V2KX-L1-GP
0D6V_VREF_S0
PG5111 GAP-CLOSE-PWR-6-GP
PG5113 GAP-CLOSE-PWR-6-GP
PWR_VDDQ_VTT
DY
PC5111
PC5112
SC10U6D3V3MX-L-GP
074.05388.0043
PWR_VDDQ_VTTREF
PC5114 SCD1U25V2KX-L-GP
PG5104 GAP-CLOSE-PWR-6-GP
PC5106 SC22U6D3V3MX-L1-GP
PC5107 SC22U6D3V3MX-L1-GP
PC5109 SC22U6D3V3MX-L1-GP
PC5113 SC22U6D3V3MX-L1-GP
PWR_VDDQ_VDDQ
PWR_VDDQ_FB
PR5105 6K2R2F-GP
PR5106 10K2R2F-GP
Vout= 0.75*(1+R1/R2) = 1.2
V2D5_S5
MAX=2A
Pd=(3.3-2.5)*0.5=0.4W
3D3V_S5
PR5111 100KR2J-4-GP
2D5V_PWR_GOOD
PWR_2D5V_PG
SC10U6D3V3MX-L-GP
PC5118
5V_S5
PC5119 SC1U50V3KX-GP
2D5V_S3
PG5116 GAP-CLOSE-PWR-6-GP
PG5117 GAP-CLOSE-PWR-6-GP
PWR_2D5V_S3
PC5116 SC10U6D3V3MX-L-GP
PC5115 SC10U6D3V3MX-L-GP
PC5117 SC100P50V2JN-L-GP
PWR_2D5V_FB
PU5102
VIN#5
VOUT#4
VOUT#3
FB
GND
VCNTL
POK
EN
VIN#9
APL5930KAI-TRG-1-GP
CRITICAL
74.05930.B3D
PWR_2D5V_PG
PWR_2D5V_EN
PR5113 0R0402-PAD-1-GP
2D5V_S3_PWRGD
PM_SLP_S4#
PR5114 0R0402-PAD-1-GP
PC5120 SCD1U25V2KX-L-GP
R1
PR5115 21.5K_1% 0402
R2
PR5110 10KR2F-L1-GP
Vout = 0.8*(1+R1/R2)=2.52V
Count
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
G5388K&RT8068A_VDDQ/VTT
Size Custom
Document Number
Slinky
Rev -1
Date: Thursday, August 24, 2017
Sheet 51 of 106

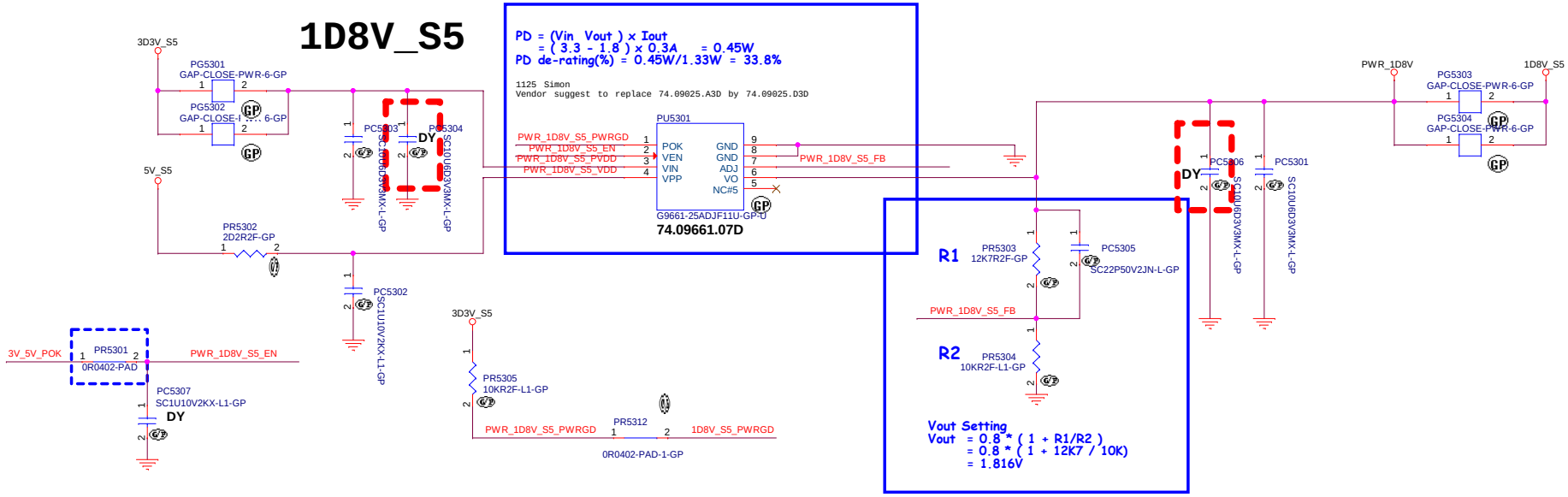


Count

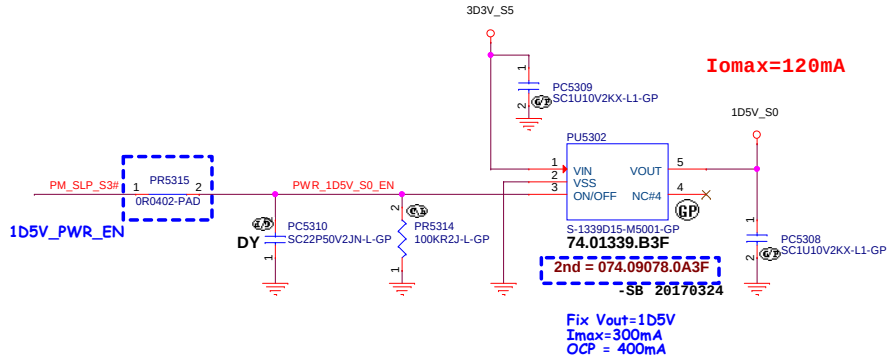
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***G5388K_1D0V***	
Size A3	Document Number **Slinky**	Rev -1
Date: Thursday, August 24, 2017	Sheet 52 of 106	

20160608 -1M

1D8V_S5



TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



Count	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8068_1D8V
Size: Custom	Document Number: Slinky
Rev	
Date: Thursday, August 24, 2017	Sheet 53 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Reserved**
Size A4	Document Number **Slinky**
Rev	**-1**
Date:	Thursday, August 24, 2017
Sheet	54 of 106

Main Func = LCD

24 MODEL_ID_AD
3 eDP_AUX_CPU_P
3 eDP_AUX_CPU_N
3 eDP_TX_CPU_P0
3 eDP_TX_CPU_N0
3 eDP_TX_CPU_P1
3 eDP_TX_CPU_N1
18,24,70,73 SML1_DATA
18,24,70,73 SML1_CLK
22 TOUCH_INT#
24 TOUCH_EN
6 TOUCH_DET#
3 eDP_VDDEN_CPU
24 BLON_OUT
3 eDP_HPD_CPU
3 eDP_BLCTRL_CPU
15 TS_USB20_P
15 TS_USB20_N
6,24 TS_I2C0_SDA_CON
6,24 TS_I2C0_SCL_CON
6 TOUCH_S_RST#
89 eDP_HPD_CON
89 eDP_BLEN_CON
89 eDP_BLCTRL_CON
89 TOUCH_DET#_R
89 TS_S0
89 eDP_TX_CON_P0
89 eDP_TX_CON_N0
89 eDP_TX_CON_P1
89 eDP_TX_CON_N1
89 eDP_AUX_CON_P
89 eDP_AUX_CON_N
89 TOUCH_INTR#

EDP1
STAR-CON40-1-GP

MODEL_ID_AD
eDP_AUX_CON_P C5511 SCD1U25V2KX-L-GP eDP_AUX_CPU_P
eDP_AUX_CON_N C5512 SCD1U25V2KX-L-GP eDP_AUX_CPU_N
eDP_TX_CON_P0 C5513 SCD1U25V2KX-L-GP eDP_TX_CPU_P0
eDP_TX_CON_N0 C5514 SCD1U25V2KX-L-GP eDP_TX_CPU_N0
eDP_TX_CON_P1 C5515 SCD1U25V2KX-L-GP eDP_TX_CPU_P1
eDP_TX_CON_N1 C5516 SCD1U25V2KX-L-GP eDP_TX_CPU_N1
SML1_DATA
SML1_CLK
TOUCH_INTR# R5508 TS_I2C 33R2J-L1-GP TOUCH_INT#
R5509 0R0402-PAD TOUCH_EN
eDP_HPD_CON
3D3V_S5 FOR G-SENSOR
3D3V_LCDVDD_S0
TOUCH_DET#_R R5505 DY 33R2J-L1-GP TOUCH_DET#
TOUCH_S_RST#_R
TS_S0
TS_USB20_CON_N
TS_USB20_CON_P
eDP_BLCTRL_CON R5502 33R2J-L1-GP eDP_BLEN_CON
eDP_BLCTRL_CPU
19V_DCBATOUT_LCD

To PCH
To EC

20.K0809.040
2nd = 20.K0678.040
3rd = 020.K0160.0040

FOR G-SENSOR
SML1_DATA
SML1_CLK
ED5501 AZ5125-02S-R7G-GP
GSENSOR_1
75.05125.07D
2nd = 075.05125.007D

EU5501
TS_USB20_CON_N I/O1 I/O4 TS_USB20_CON_P
GND VDD 5V_S0
I/O2 I/O3
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

Inverter Power
19V_DCBATOUT_LCD
19V_DCBATOUT
F5501 POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 069.41101.0001
C5501 SC4D7U25V5KX-L2-GP
C5502 SCD1U50V3KX-L-GP

TOUCH_S_RST#_R DY C5518 SC10P50V2JN-L1-GP
TOUCH_INT# DY C5517 SC10P50V2JN-L1-GP
eDP_BLEN_CON eDP_HPD_CON RN5501 SRN1KJ-7-GP BLON_OUT eDP_HPD_CPU
eDP_HPD_CON eDP_BLEN_CON RN5502 SRN100KJ-6-GP

3D3V_S5
20170302 Change
U5501
eDP_VDDEN_CPU IN OUT GND EN OC#
G524B1T11U-GP
074.00524.0B9F
2ND = 074.06288.007B
C5506 SC1U10V2KX-L1-GP
R5503 100KR2F-L3-GP
3D3V_LCDVDD_S0
C5505 DY SC4D7U6D3V3KX-L-GP
C5503 DY SCD1U25V2KX-L-GP
C5504 SCD1U25V2KX-L-GP
20170303 change 1uF

Touch panel Power

TS_I2C
R5506 0R2J-L-GP TS_I2C0_SDA_CON
R5507 0R2J-L-GP TS_I2C0_SCL_CON
TS_I2C
TS_USB20_CON_P R5512 0R0402-PAD TS_USB20_P
TS_USB20_CON_N R5513 0R0402-PAD TS_USB20_N
TS_USB
TS_I2C
TOUCH_S_RST#_R R5515 33R2J-L1-GP TOUCH_S_RST#
R5514 0R0402-PAD
TS_USB

5V_S0 3D3V_S0
TS_I2C
TS_S0
R5510 0R3J-L1-GP
R5511 0R0402-PAD
TS_USB
C5509 SC10U25V5KX-L-GP
C5510 SCD1U25V2KX-L-GP

Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN
Size: Custom
Document Number: Slinky
Rev: -1
Date: Thursday, August 24, 2017
Sheet 55 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **Slinky**
Rev	**-1**
Date: Thursday, August 24, 2017	Sheet 56 of 106

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

3 HDMI_DATA_CPU_P0
3 HDMI_DATA_CPU_N0
3 HDMI_DATA_CPU_P1
3 HDMI_DATA_CPU_N1
3 HDMI_DATA_CPU_P2
3 HDMI_DATA_CPU_N2

3 HDMI_DATA_CPU_P3
3 HDMI_DATA_CPU_N3

3,14 HDMI_CLK_CPU
3,14 HDMI_DATA_CPU
3 HDMI_DET_CPU

89 HDMI_CLK_CON_N3
89 HDMI_CLK_CON_P3

89 HDMI_DATA_CON_P0
89 HDMI_DATA_CON_N0
89 HDMI_DATA_CON_P1
89 HDMI_DATA_CON_N1
89 HDMI_DATA_CON_P2
89 HDMI_DATA_CON_N2

89 HDMI_CLK_CON
89 HDMI_DATA_CON
89 HDMI_DET_CON

3D3V_S0 — 4K7R2J-L-GP DY — R5727 — PS8201_EN
3D3V_S0 — 4K7R2J-L-GP LS — R5728 — PS8201_DDCBUF
4K7R2J-L-GP DY — R5731
-SB DY
3D3V_S0 — 4K7R2J-L-GP DY — R5713 — PS8201_PRE
4K7R2J-L-GP DY — R5714
3D3V_S0 — 4K7R2J-L-GP LS — R5724 — PS8201_CFG
3D3V_S0 — 4K7R2J-L-GP LS — R5726 — PS8201_EQ
4K7R2J-L-GP DY — R5709
3D3V_S0 — 4K7R2J-L-GP DY — R5730 — PS8201_ISET
4K7R2J-L-GP DY — R5712

HDMI1 — SKT-HDMI23-92-GP-U
20170302 Change
HDMI_DATA_CON_P2
HDMI_DATA_CON_N2
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
HDMI_DATA_CON_P0
HDMI_DATA_CON_N0
HDMI_CLK_CON_P3
HDMI_CLK_CON_N3
HDMI_CLK_CON
HDMI_DATA_CON
5V_HDMI_S0
HDMI_DET_CON
22.10296.981
2nd = 022.10025.00S1

ER5701 ER5702 ER5703 ER5704 — 150R2J-L1-GP-U
HDMI_CLK_CON_N3
HDMI_CLK_CON_P3
HDMI_DATA_CON_N0
HDMI_DATA_CON_P0
HDMI_DATA_CON_N1
HDMI_DATA_CON_P1
HDMI_DATA_CON_N2
HDMI_DATA_CON_P2

5V_HDMI_S0 — D5701 BAW56H-1-GP — 75.00056.D7D
5V_DDC_HDMI1
5V_DDC_HDMI2
RN5701 SRN2K2J-5-GP
HDMI_CLK_CON
HDMI_DATA_CON

5V_HDMI_S0 — C5733 SCD1U25V2KX-L-GP — F5701 POLYSW-1[illegible]6V-9-GP-U
69.48001.081
2ND = 69.50011.081

EMI Request:
ED5701 DY — L05ESDL5V0NA-4-GP
HDMI_DATA_CON_P2
HDMI_DATA_CON_N2
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

ED5702 DY — L05ESDL5V0NA-4-GP
HDMI_DATA_CON_P0
HDMI_DATA_CON_N0
HDMI_CLK_CON_N3
HDMI_CLK_CON_P3
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

ED5703 DY — AZC099-04S-2-GP
HDMI_CLK_CON
HDMI_DATA_CON
HDMI_DET_CON
5V_HDMI_S0
20170208 ENG change to 5V_HDMI_S0
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

1D5V_S0 — C5713 LS — C5712 LS — C5714 DY — SCD01U50V2KX-L-GP

U5701 — PS8201ATQFN40GTR2-A0-GP
3D3V_S0 → VDD33
1D5V_S0 → VDD15 ×3
OUT_CKN / OUT_CKP → HDMI_CLK_CON_N3 / HDMI_CLK_CON_P3
OUT_D0P / OUT_D0N / OUT_D1P / OUT_D1N / OUT_D2P / OUT_D2N → HDMI_DATA_CON_P0 / N0 / P1 / N1 / P2 / N2
SCL_SNK / SDA_SNK / HPD_SNK → HDMI_CLK_CON / HDMI_DATA_CON / HDMI_DET_CON
SCL_SRC / SDA_SRC / HPD_SRC → HDMI_CLK_CPU / HDMI_DATA_CPU / HDMI_DET_CPU
HDMI_HPD_E — R5722 0R0402-PAD-1-GP
I2C_CTL_EN — R5723 4K7R2J-L-GP DY
PS8201_PRE
PS8201_PD# — R5725 4K7R2J-L-GP DY
IN_D0P / IN_D0N / IN_D1P / IN_D1N / IN_D2P / IN_D2N
IN_CKP / IN_CKN
DCIN_EN/SCL_CTL
DDCBUF/SDA_CTL
EQ/I2C_ADDR
CFG
REXT — R5721 4K02R2F-GP LS
NC#12 / NC#15 / NC#37 / NC#34
GND ×3

HDMI_DATA_CPU_P0 LS C5724 — SCD1U25V2KX-L-GP — HDMI_DATA_CPU_P0_C
HDMI_DATA_CPU_N0 LS C5723 — HDMI_DATA_CPU_N0_C
HDMI_DATA_CPU_P1 LS C5726 — HDMI_DATA_CPU_P1_C
HDMI_DATA_CPU_N1 LS C5725 — HDMI_DATA_CPU_N1_C
HDMI_DATA_CPU_P2 LS C5728 — HDMI_DATA_CPU_P2_C
HDMI_DATA_CPU_N2 LS C5727 — HDMI_DATA_CPU_N2_C
HDMI_DATA_CPU_P3 LS C5722 — HDMI_CLK_CPU_P3_C
HDMI_DATA_CPU_N3 LS C5721 — HDMI_CLK_CPU_N3_C

1D5V_S0 — C5710 LS — C5709 DY — C5711 LS — SCD01U25V2KX-L-GP

3D3V_S0 — C5716 LS — SCD01U50V2KX-L-GP
3D3V_S0 — C5715 LS — SCD01U50V2KX-L-GP

PS8201_EN
PS8201_DDCBUF
PS8201_EQ
PS8201_CFG
PS8201_REXT
PS8201_ISET

Count

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI Level Shifter/Connector		
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 57 of 106	

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 58 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DVI(Reserved)***	
Size A4	Document Number **Slinky**	Rev **-1**
Date: Thursday, August 24, 2017	Sheet 59 of 106	

SSID = SATA SATA HDD Connector

HDD_SATA_RX_P 15
HDD_SATA_RX_N 15
HDD_SATA_TX_N 15
HDD_SATA_TX_P 15
HDD_UNLOAD 69
PM_SLP_S3# 20,24,40,45,53

5V_S0
C6005 HDD C10U25V5KX-L-GP
C6006 HDD SCD1U25V2KX-L-GP
HDD_UNLOAD
HDD_SATA_RX_C_P
HDD_SATA_RX_C_N
HDD_SATA_TX_C_N
HDD_SATA_TX_C_P
HDD1 HDD HRS-CON12-8-GP

20170210 change

20.K0824.012
2ND = 020.K0125.0012
3RD = 020.K0190.0012

3D3V_S5 R6025 1 DY 2 0R2J-L-GP 3D3V_HDD_S0
3D3V_S0 R6026 1 2 0R0402-PAD

3D3V_HDD_S0
U6001 HDD
VCC 10 20
TX1P 15
TX1N 14
TX2P 5
TX2N 4
RX1P
RX1N
RX2P
RX2N
EN 7
DE1 9 8
DE2
DEW1 16
DEW2 6
GND 3 13 18 21
SN75LVCP601RTJR-GP
71.75601.003

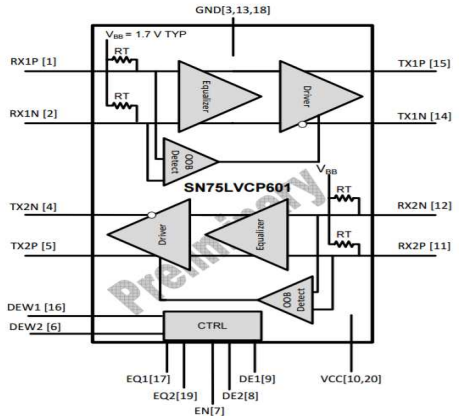
HDD_SATA_TX_P HDD SCD01U50V2KX-L-GP 1 C6018 HDD_SATA_TX_RE_P 1
HDD_SATA_TX_N HDD SCD01U50V2KX-L-GP 1 C6019 HDD_SATA_TX_RE_N 2
HDD_SATA_RX_C_P HDD SCD01U50V2KX-L-GP 1 C6020 SATA_RX_REO_P0 11
HDD_SATA_RX_C_N HDD SCD01U50V2KX-L-GP 1 C6021 SATA_RX_REO_N0 12

SATA_TX_REO_P0 C6022 1 SCD01U50V2KX-L-GP HDD HDD_SATA_TX_C_P
SATA_TX_REO_N0 C6023 1 SCD01U50V2KX-L-GP HDD HDD_SATA_TX_C_N
HDD_SATA_RX_RE_P C6024 1 SCD01U50V2KX-L-GP HDD HDD_SATA_RX_P
HDD_SATA_RX_RE_N C6025 1 SCD01U50V2KX-L-GP HDD HDD_SATA_RX_N

EQ1 17
EQ2 19
3D3V_HDD_S0
HDD_EN 7 R6033 1 2 10KR2J-3-GP HDD
PM_SLP_S3# R6035 1 2 0R2J-L-GP DY

EU6001 DY
HDD_SATA_RX_C_P 1 10
HDD_SATA_RX_C_N 2 3 9 8
HDD_SATA_TX_C_N 4 7
HDD_SATA_TX_C_P 5 6
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

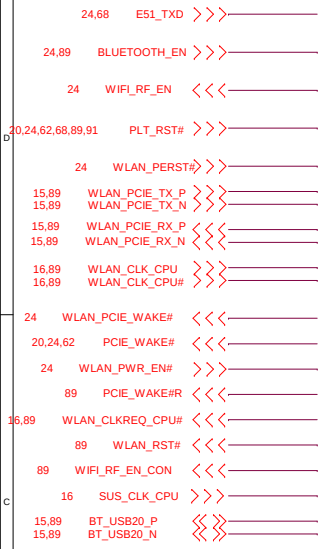
3D3V_HDD_S0
R60101 DY 10KR2J-3-GP EQ1 R60161 DY 10KR2J-3-GP
R60111 DY 10KR2J-3-GP EQ2 R60171 DY 10KR2J-3-GP
R60121 DY 10KR2J-3-GP DE1 R60181 DY 10KR2J-3-GP
R60131 DY 10KR2J-3-GP DE2 R60191 DY 10KR2J-3-GP
R60141 DY 10KR2J-3-GP DEW1 R60201 HDD 10KR2J-3-GP
R60151 DY 10KR2J-3-GP DEW2 R60211 HDD 10KR2J-3-GP

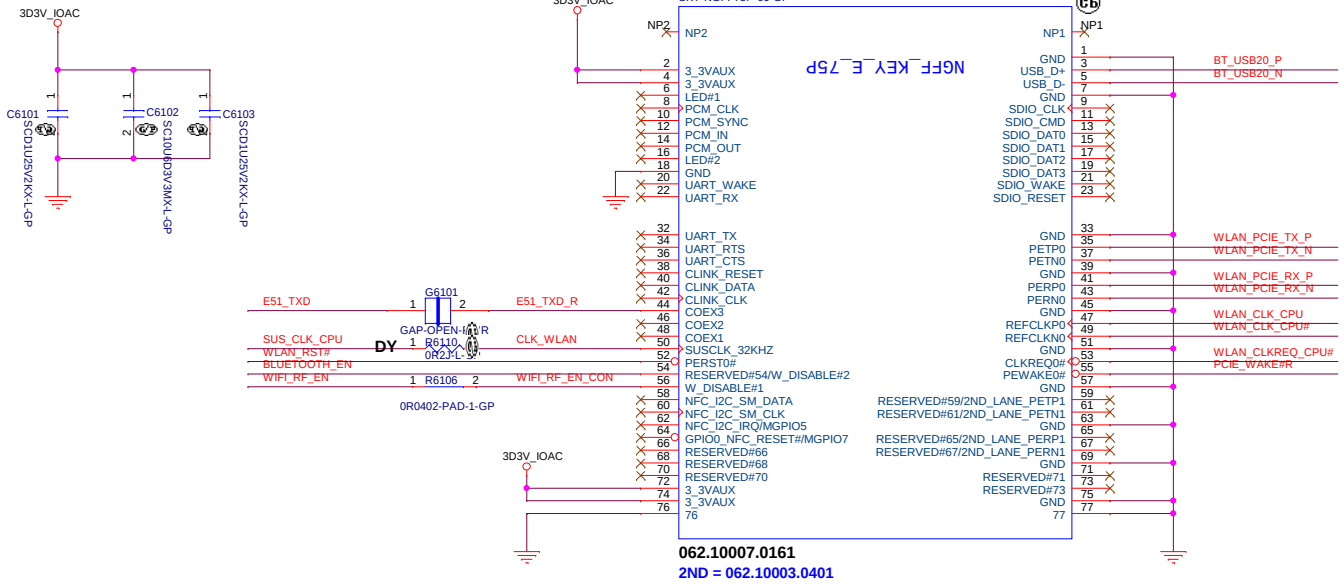


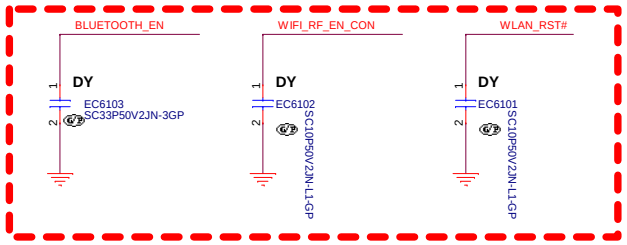
Count

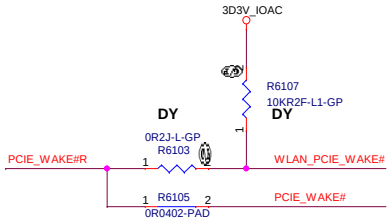
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDD_GSENSOR
Size: Custom	Document Number: Slinky
Rev	-1
Date: Thursday, August 24, 2017	Sheet 60 of 106

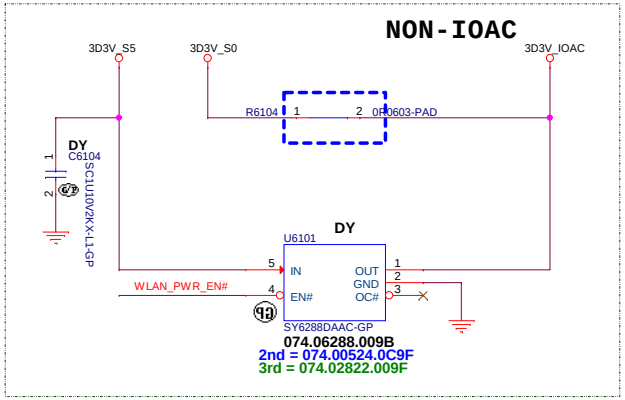
SSID = Wireless Mini Card Connector(802.11a/b/g/n)

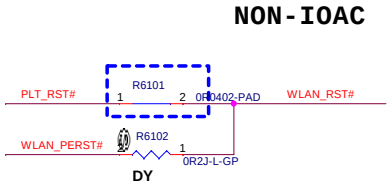










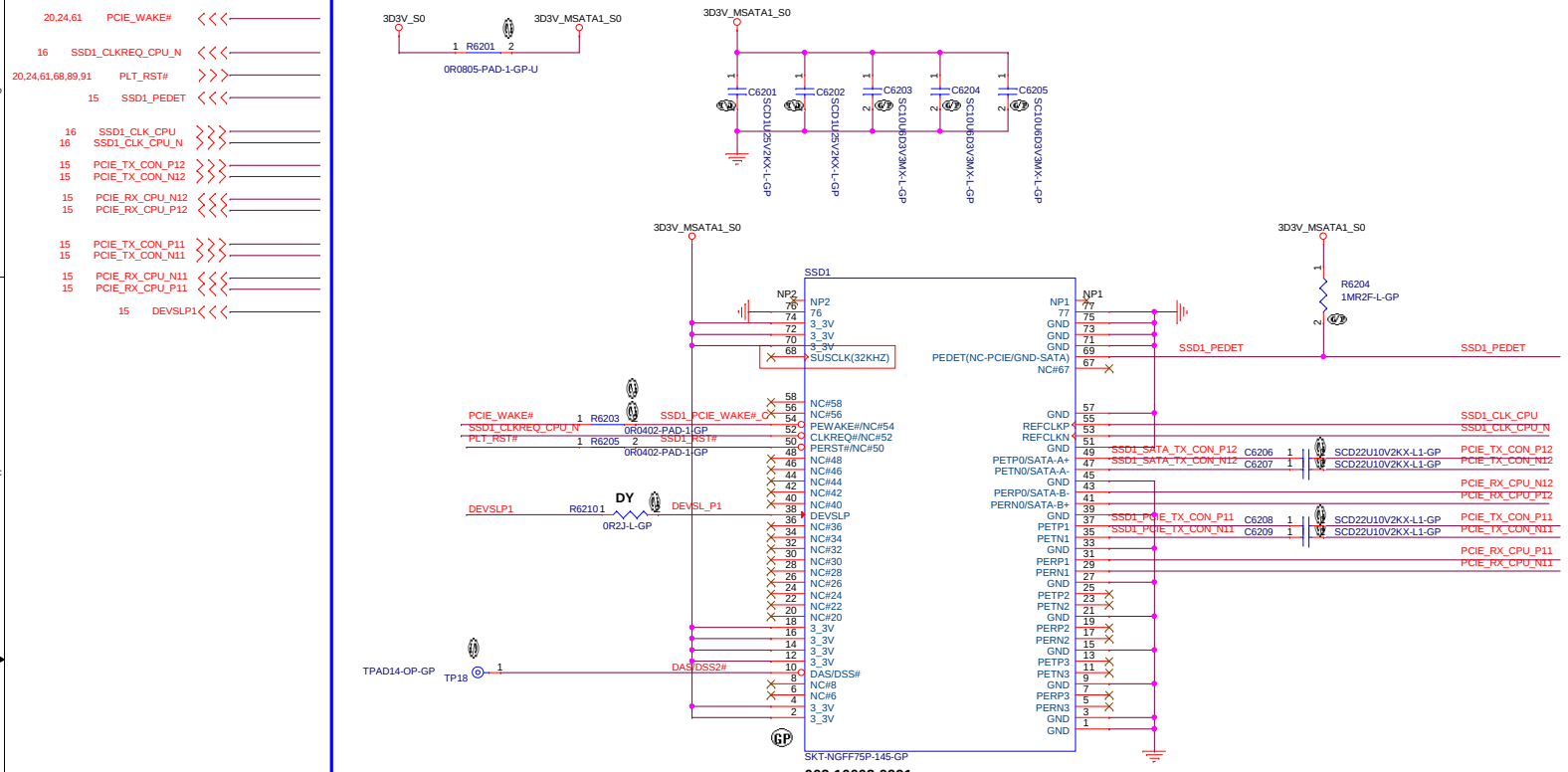


Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Mini Card-WLAN		
Size: Custom	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 61 of 106	

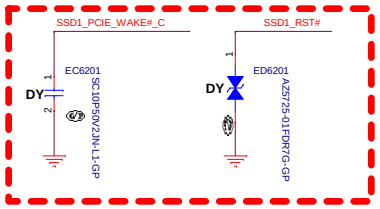
SSID = mSATA

Mini Card Connector(mSATA)



062.10003.0991

2ND = 062.10003.00A1



Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1				RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-Y	1x4	RP 1				RP 5							
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9			
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9			
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5				RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10		

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **mSTATA**

Size: Custom | Document Number: **Slinky** | Rev: **-1**

Date: Thursday, August 24, 2017 | Sheet 62 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 63 of 106

24,89 STDBY_LED
24,89 POWER_LED
24,89 CHARGE_LED
24,89 DC_BATFULL
24 Value+
24 Value-
24 LID_CLOSE#
24 LID_CLOSE2#
15,89 USB3_USB20_N
15,89 USB3_USB20_P
15,89 CR_USB20_N
15,89 CR_USB20_P
43 BAT_RST
24,89 KBC_PWRBTN#
24,35 USB_PWR_EN#
27,64,89 RING2
27,64,89 RING2
27,64,89 SELEEVE
27,64,89 SELEEVE
27,89 AUD_HP1_JACK_R2
27,89 AUD_HP1_JACK_L2
27,89 AUD_HP1_JD#

SSID = User.Interface

Low Active 2A

5V_S5
C6408 SC1U10V2KX-L1-GP
U6401
USB_PWR_EN#
IN
EN#
OUT
GND
OC#
SY6288DAAC-GP
5V_USB20
C6409 SCD1U25V2KX-L-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

Close connector

EU6402
USB3_USB20_N
CR_USB20_N
I/O1
GND
I/O2
I/O4
VDD
I/O3
USB3_USB20_P
5V_USB20
CR_USB20_P
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

20170309 change
PWRBT1
KBC_PWRBTN#
SW-TACT-124-GP
62.40078.001
LAB

Close SMB1

SMB1
STAR-CON40-1-GP
USB3_USB20_N
USB3_USB20_P
CR_USB20_N
CR_USB20_P
Value+_R
Value-_R
BAT_RST
KBC_PWRBTN#
LID_CLOSE#
LID_CLOSE2#
RING2
RING2
SELEEVE
SELEEVE
AUD_HP1_JACK_R2
AUD_HP1_JACK_L2
AUD_HP1_JD#
STDBY_LED
POWER_LED
DC_BATFULL
LED_POWER
CHARGE_LED
3D3V_S0
RN6427
Value+
Value-
SRN2K2J-5-GP
5V_USB20
3D3V_AUX_S5
5V_S5
AUD_AGND
PIN1,PIN5 SWAP
-SB 20170324
20.K0809.040
2ND = 20.K0678.040
3rd = 020.K0160.0040

3D3V_S5
RN6401
Value-
Value+
SRN100KJ-6-GP
KBC_PWRBTN#
ED6401
DY
AZ5725-01FDR7G-GP

5V_AUX_S5
-1 20170424
Del R6401 LED_POWER OPTION(3D3V_AUX_S5)
R6402 0R0402-PAD
LED_POWER

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 64 of 106

24,89 KSI[0..7]
24,89 KSO[0..17]
24 EC_TPCLK
24 EC_TPDATA
24,89 FUN_OFF#
24 PTP_PWR_EN#
22 TP_IN#
24 EC_TP_IN#
6 PM_TP_CLK
6 PM_TP_DATA
24 KB_BL_PWM
24 KB_BL_DET
89 EC_TP_CLK_C
89 EC_TP_DATA_C
89 I2C1_DATA_TP
89 I2C1_CLK_TP
89 TP_IN#_R

SSID = KBC

3D3V_S0 3D3V_TP_S3 Q6502 R6506 100KR2F-L-3-GP TP_IN# TP_IN#_R EC_TP_IN# R6512 0R0402-PAD-1-GP 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031

3D3V_TP_S3 RN6503 SRN4K7J-8-GP RN6502 SRN33J-5-GP-U EC_TPCLK EC_TPDATA FUN_OFF# EC6502 SC22P50V2JN-L-GP EC_TP_CLK_C EC_TP_DATA_C I2C1_DATA_TP I2C1_CLK_TP TP_IN#_R TP1 STM-CON8-3-GP EC6501 EC6503 SC22P50V2JN-3GP

TOUCH PAD

020.K0277.0008
2ND = 020.K0235.0008

3D3V_S0 3D3V_TP_S3 RN6505 SRN2K2J-5-GP Q6503 2N7002KDW-1-GP PM_TP_CLK PM_TP_DATA I2C1_CLK_TP I2C1_DATA_TP EC6504 EC6505 SCD1U16V2KX-L-GP

75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

3D3V_S5 U6502 SY6288DAAC-GP PTP_PWR_EN# C6509 SC4D7U6D3V3KX-L-GP 3D3V_TP_S3 C6504 SC4D7U6D3V3KX-L-GP

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

TP_IN#_R EC6507 SCD1U16V2KX-L-GP

Internal KeyBoard Connector

KBBL1 PTWO-CON4-16-GP KB_BL_DET_R KB_LED_PWM_R R6504 100KR2F-L-3-GP KB_BL_DET KB_BL R6502 200KR2F-L-3-GP KB_BL R6521 0R0402-PAD KB_LED_PWM_D 5V_S0 C6501 SCD1U16V2KX-L-GP

20.K0397.004
2nd = 020.K0262.0004

20170210 Change

20170208 ENG R6521 chage short PAD

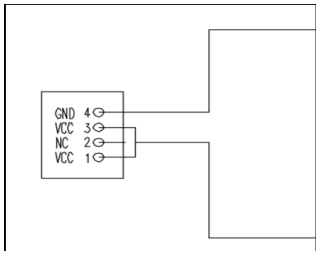
Q6501 2N7002K-2-GP KB_BL KB_BL_PWM C6502 SCD1U16V2KX-L-GP

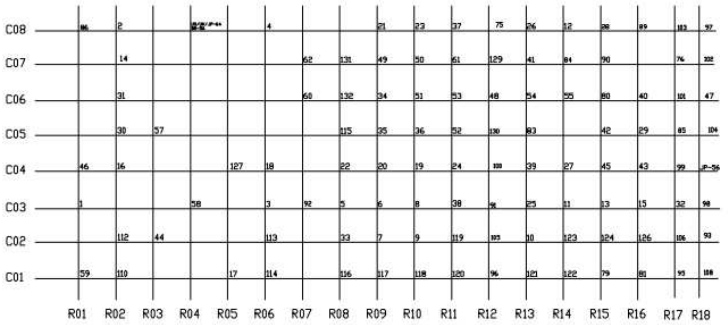
84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031

KB1 ACES-CON28-10-GP

020.K0173.0028
2ND = 020.K0266.0028

KSO16 KSO17 KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7





Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size: Custom | Document Number: **Slinky** | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 65 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 66 of 106

Blanking

Count

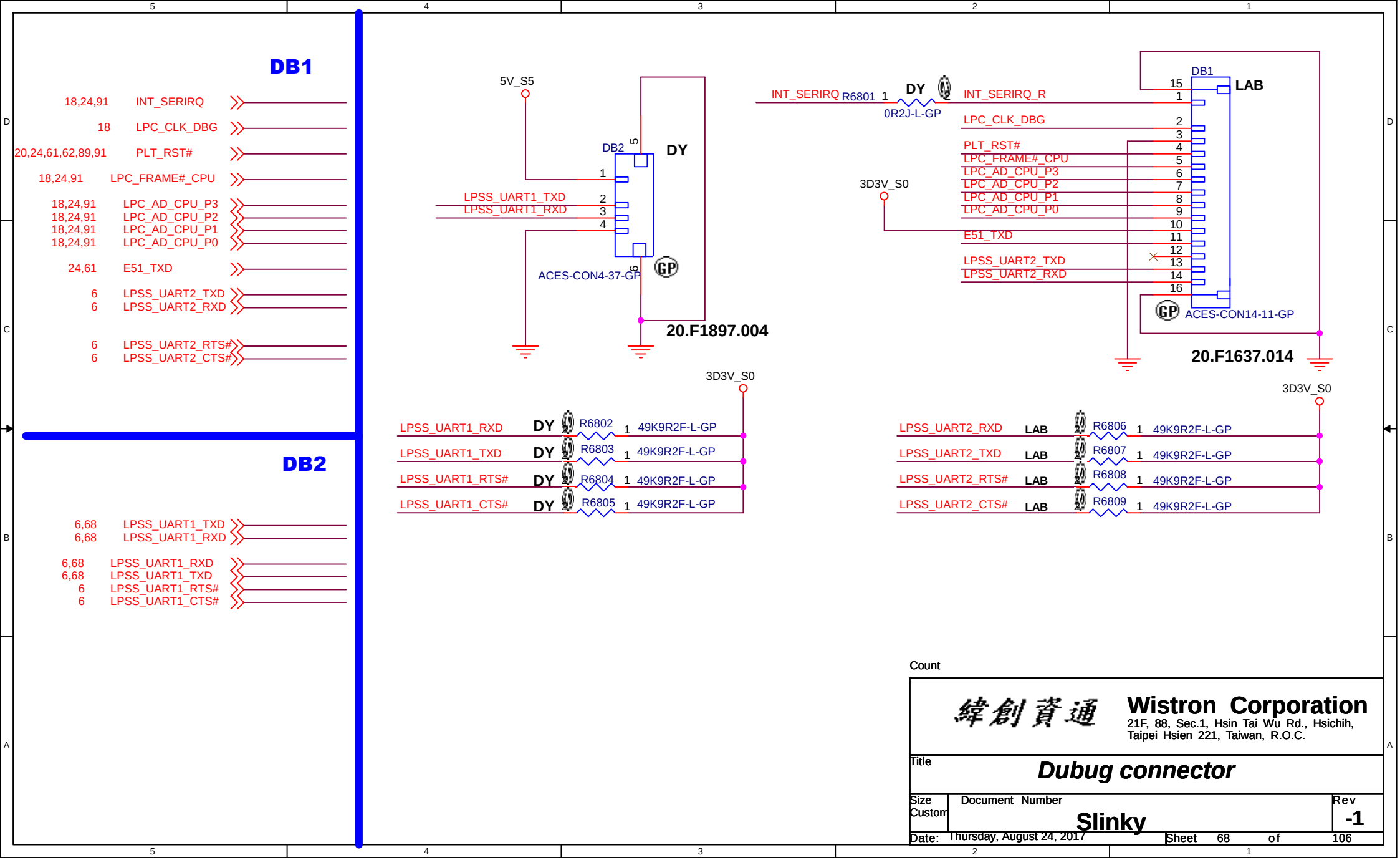
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

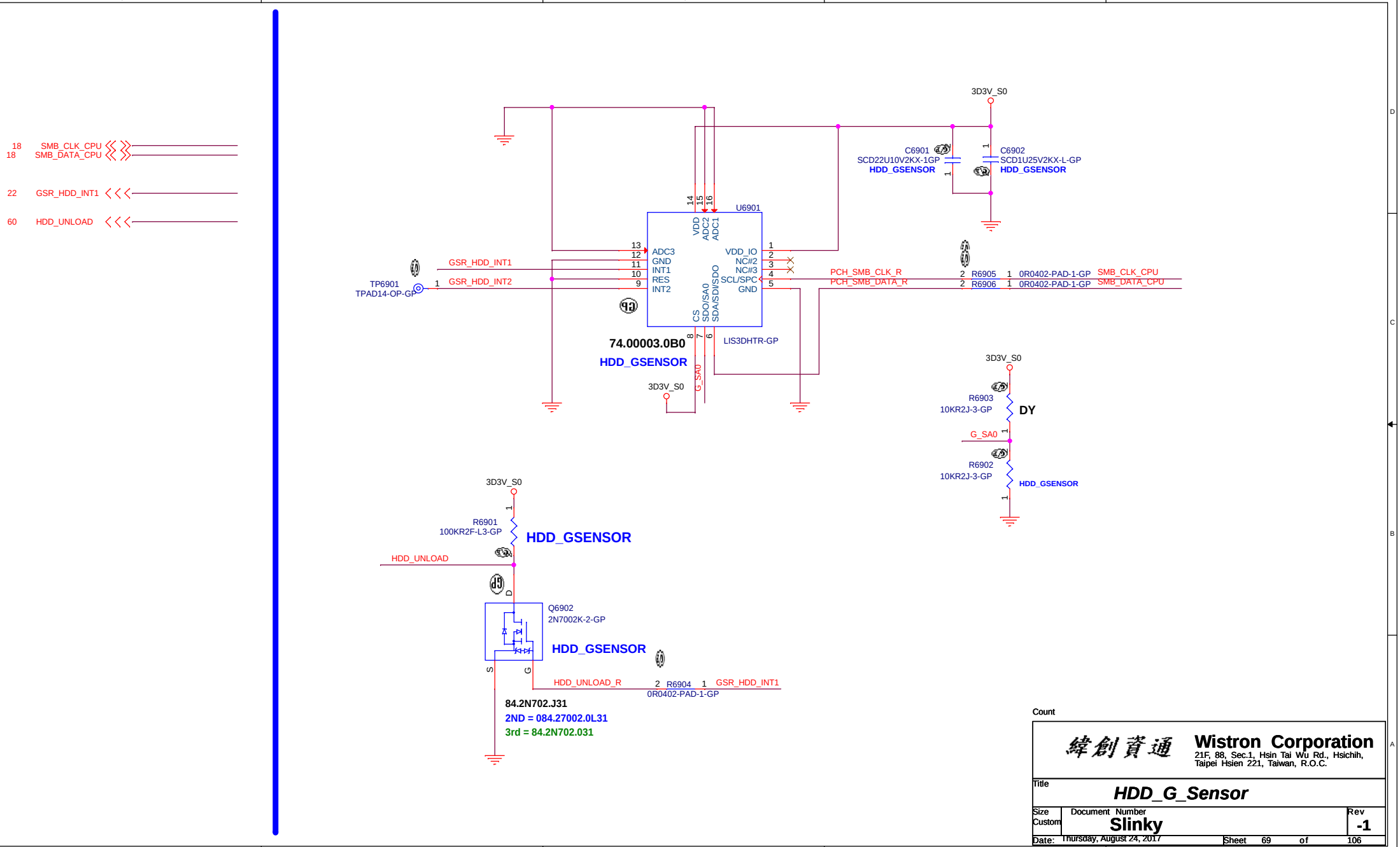
Title

Reserved

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 67 of 106


DB1
18,24,91 INT_SERIRQ
18 LPC_CLK_DBG
20,24,61,62,89,91 PLT_RST#
18,24,91 LPC_FRAME#_CPU
18,24,91 LPC_AD_CPU_P3
18,24,91 LPC_AD_CPU_P2
18,24,91 LPC_AD_CPU_P1
18,24,91 LPC_AD_CPU_P0
24,61 E51_TXD
6 LPSS_UART2_TXD
6 LPSS_UART2_RXD
6 LPSS_UART2_RTS#
6 LPSS_UART2_CTS#
DB2
6,68 LPSS_UART1_TXD
6,68 LPSS_UART1_RXD
6,68 LPSS_UART1_RXD
6,68 LPSS_UART1_TXD
6 LPSS_UART1_RTS#
6 LPSS_UART1_CTS#
5V_S5
DB2
DY
LPSS_UART1_TXD
LPSS_UART1_RXD
ACES-CON4-37-GP
20.F1897.004
3D3V_S0
LPSS_UART1_RXD DY R6802 1 49K9R2F-L-GP
LPSS_UART1_TXD DY R6803 1 49K9R2F-L-GP
LPSS_UART1_RTS# DY R6804 1 49K9R2F-L-GP
LPSS_UART1_CTS# DY R6805 1 49K9R2F-L-GP
INT_SERIRQ R6801 1 DY 2 INT_SERIRQ_R
0R2J-L-GP
DB1
LAB
LPC_CLK_DBG
PLT_RST#
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
3D3V_S0
E51_TXD
LPSS_UART2_TXD
LPSS_UART2_RXD
ACES-CON14-11-GP
20.F1637.014
3D3V_S0
LPSS_UART2_RXD LAB R6806 1 49K9R2F-L-GP
LPSS_UART2_TXD LAB R6807 1 49K9R2F-L-GP
LPSS_UART2_RTS# LAB R6808 1 49K9R2F-L-GP
LPSS_UART2_CTS# LAB R6809 1 49K9R2F-L-GP
Count
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Dubug connector
Size Custom
Document Number
Slinky
Rev
-1
Date: Thursday, August 24, 2017
Sheet 68 of 106



Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD_G_Sensor***

Size	Document Number	Rev
Custom	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 69 of 106

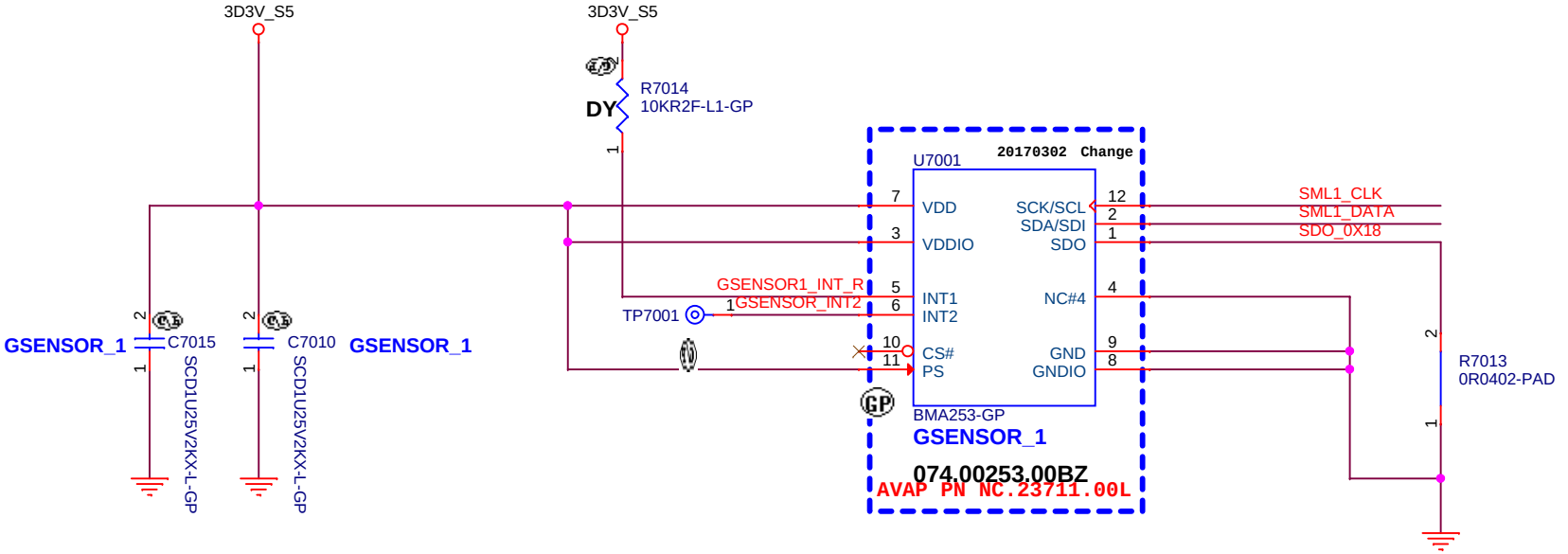
18,24,55,73 SML1_CLK
18,24,55,73 SML1_DATA

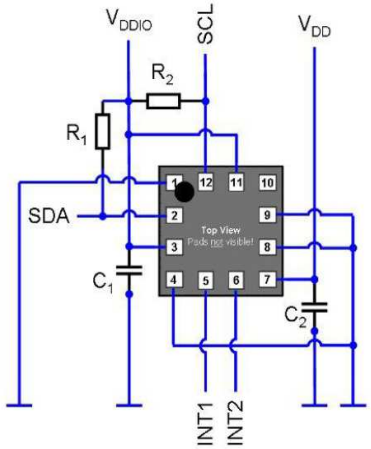
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SSID = User.Interface

G Sensor

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.





Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *G SENSOR*	
Size: Custom	Document Number: Slinky — Rev: -1
Date: Thursday, August 24, 2017	Sheet 70 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 71 of 106

Blanking

Count

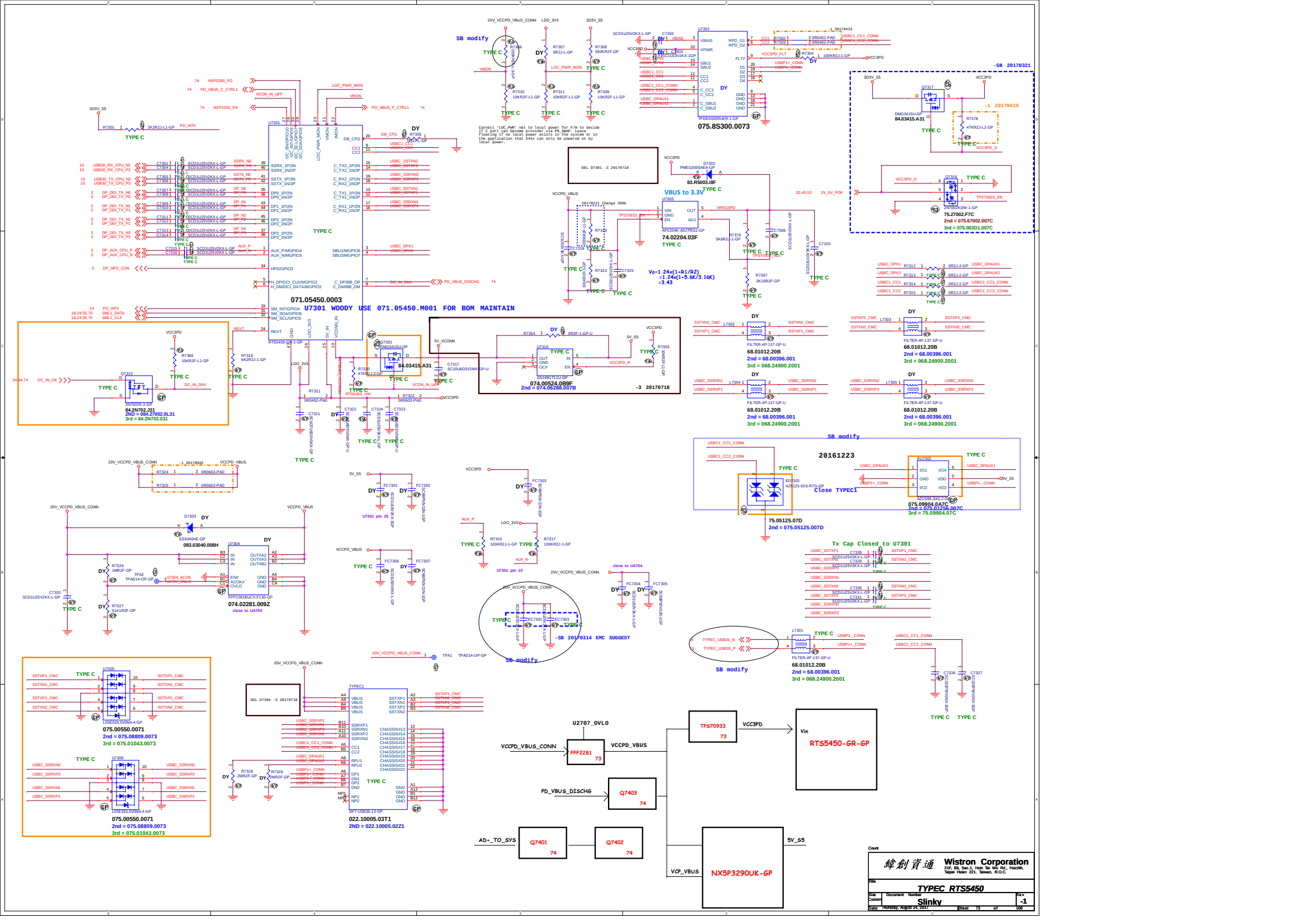
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

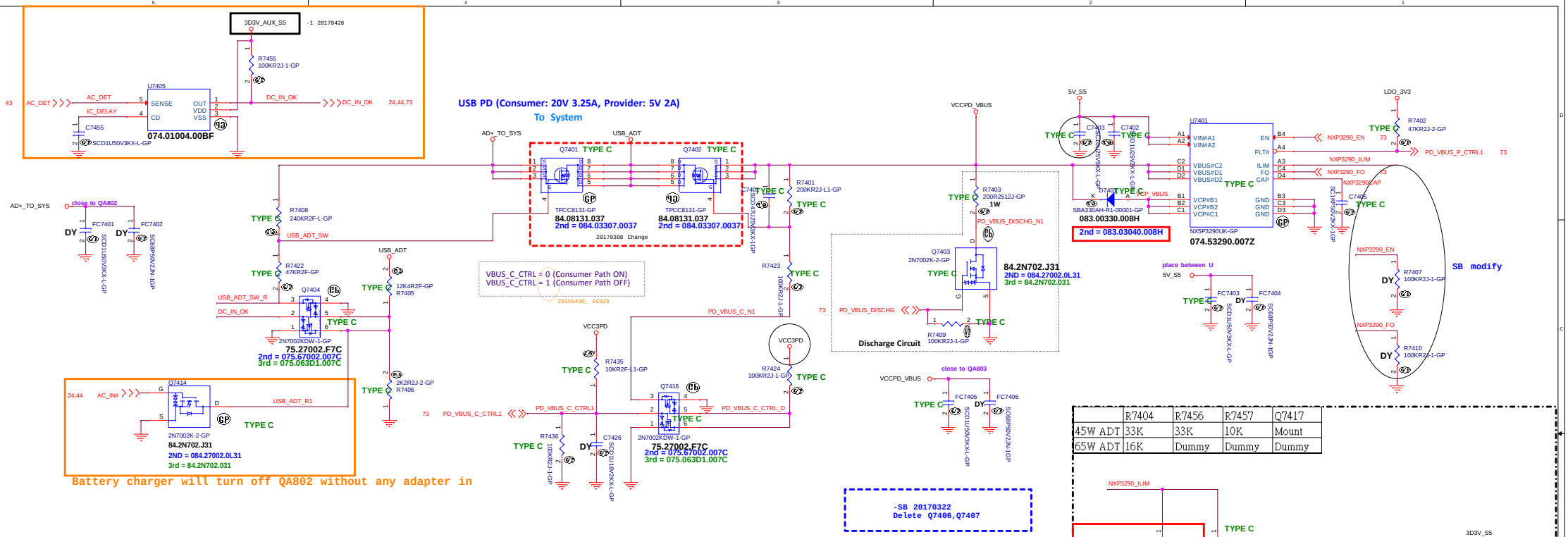
Title

Reserved

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 72 of 106


SB modify
TYPE C
DY
071.05450.0003
U7301 WOODY USE 071.05450.M001 FOR BOM MAINTAIN
RTS5450-GR-GP
84.03415.A31
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
074.00524.0B9F
2nd = 074.06288.007B
-3 20170718
-SB 20170321
-1 20170419
83.R5003.J8F
74.02204.03F
VBUS to 3.3V
Vo=1.24x(1+R1/R2)
=1.24x(1+5.6K/3.16K)
=3.43
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.083D1.007C
68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001
20161223
Close TYPEC1
75.05125.07D
2nd = 075.05125.007D
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C
Tx Cap Closed to U7301
-SB 20170314 EMC SUGGEST
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
022.10005.03T1
2ND = 022.10005.02Z1
U2707_OVLO
VCCPD_VBUS_CONN
VCCPD_VBUS
PD_VBUS_DISCHG
AD+_TO_SYS
VCP_VBUS
TPS70933
FPF2281
Q7403
Q7401
Q7402
NX5P3290UK-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TYPEC RTS5450
Slinky
Thursday, August 24, 2017



	R7404	R7456	R7457	Q7417
45W ADT	33K	33K	10K	Mount
65W ADT	16K	Dummy	Dummy	Dummy

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

Count

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TYPEC_Control

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 74 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 75 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_PEG(Reserved)***

Size	Project Name	Rev
	Slinky	*-1*

Date: Thursday, August 24, 2017 Sheet 76 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DIGITALOUT(Reserved)***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 77 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size | Project Name: **Slinky** | Rev: *-1*

Date: Thursday, August 24, 2017 | Sheet 78 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_GPIO/STRAP(Reserved)***

Size	Project Name	Rev
	Slinky	*-1*

Date: Thursday, August 24, 2017 Sheet 79 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER/GND(Reserved)

Size | Project Name: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 80 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 81 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM3,4(Reserved)***

Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 82 of 106

Blanking

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU-VRAM5,6(Reserved)*		
Size: A4	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 83 of 106	

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM7,8(Reserved)***	
Size A4	Document Number **Slinky**	Rev **-1**
Date: Thursday, August 24, 2017	Sheet 84 of 106	

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VGA_CORE(Reserved)***
Size A4	Document Number **Slinky**
Rev	
Date: Thursday, August 24, 2017	Sheet 85 of 106

Blanking

Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DIS VGA POWER(Reserved)*		
Size: A4	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 86 of 106	

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GFX_LCD(1/2)(Reserved)***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 87 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GFX_LCD(2/2)(Reserved)***

Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 88 of 106

DCIN

19V_AD_JK
19V_AD_JK
AFTP2
AFTP3
AFTP4
AFTP5

Battery

BT+
BT+
43 BAT_G
43 BAT_INF_1
43 BATA_SCL_1
43 BATA_SDA_1
AFTP6
AFTP11
AFTP13
AFTP14
AFTP21
AFTP22
AFTP23
AFTP36

EDP

55 eDP_TX_CON_P0
55 eDP_TX_CON_N0
55 eDP_TX_CON_P1
55 eDP_TX_CON_N1
55 eDP_AUX_CON_P
55 eDP_AUX_CON_N
55 eDP_BLCTRL_CON
55 eDP_HPD_CON
55 eDP_BLEN_CON
3D3V_CAMERA_S0
3D3V_LCDVDD_S0
19V_DCBATOUT_LCD
3D3V_S0
29 CCD_USB20_CON_P
29 CCD_USB20_CON_N
29 DMIC_CLK_CON_C
29 DMIC1_DATA_CON_C
29 DMIC2_DATA_CON_C
55 TOUCH_INT#
55 TOUCH_DETI_R
55 TS_S0
AFTP37
AFTP38
AFTP73
AFTP74
AFTP86
AFTP87
AFTP89
AFTP83
AFTP92
AFTP93
AFTP81
AFTP15
AFTP17
AFTP88
AFTP69
AFTP70
AFTP95
AFTP110
AFTP152
AFTP153
AFTP154
AFTP155

Touch PAD

65 EC_TP_CLK_C
65 EC_TP_DATA_C
65 I2C1_DATA_TP
65 I2C1_CLK_TP
65 TP_INT_R
3D3V_TP_S3
24,65 FUN_OFF#
AFTP148
AFTP56
AFTP57
AFTP58
AFTP59
AFTP90
AFTP91
AFTP85

FAN

24,26 FAN_TACH1
5V_S0
26 FAN_TACH1_C
24,26 FAN1_PWM
AFTP147
AFTP61
AFTP1
AFTP2
AFTP3

Daughter BD

15,64 CR_USB20_P
15,64 CR_USB20_N
24,64 POWER_LED
24,64 STDBY_LED
3D3V_S0
24,64 CHARGE_LED
24,64 DC_BATFULL
5V_S5
5V_USB20
15,64 USB3_USB20_N
15,64 USB3_USB20_P
AFTP1
AFTP2
TP151
TP135
AFTP46
AFTP47
AFTP67
AFTP97
AFTP98
TP133
TP108
AFTP109

10,24,61,62,68,91 PLT_RST#
AFTP86

WLAN

61,89 PCIE_WAKE#R
15,61 BT_USB20_P
15,61 BT_USB20_N
61 WLAN_RST#
16,61 WLAN_CLKREQ_CPU#
16,61 WLAN_CLK_CPU#
16,61 WLAN_CLK_CPU
15,61 WLAN_PCIE_TX_P
15,61 WLAN_PCIE_TX_N
15,61 WLAN_PCIE_RX_P
15,61 WLAN_PCIE_RX_N
24,61 BLUETOOTH_EN
61,89 PCIE_WAKE#R
61 WIFI_RF_EN_CON
3D3V_IOAC
AFTP76
AFTP77
AFTP78
AFTP80
AFTP4
AFTP5
AFTP6
AFTP7
AFTP8
AFTP9
AFTP1
AFTP3
AFTP4
AFTP5
AFTP82
AFTP84

LOUT

27,64 SELEEVE
27,64 AUD_HP1_JACK_R2
27,64 AUD_HP1_JD#
27,64 AUD_HP1_JACK_L2
27,64 RING2
AFTP62
AFTP63
AFTP64
AFTP65
AFTP66

FP

FP_3D3V_S0
92 FP_USB20_CON_N
92 FP_USB20_CON_P
TP141
TP142
TP140
AFTP143

USB3.0

5V_USB30_CHARGER
5V_USB30
35 USB1_CON_USB20_N
35 USB1_CON_USB20_P
36 USB2_CON_USB20_N
36 USB2_CON_USB20_P
TP150
TP118
TP119
AFTP120
TP106
TP107
AFTP144

Check test point

3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
AFTP1
AFTP7
AFTP8
AFTP9

Top side

KB

KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
KBC_PWRBTN#
KSI[0..7] 24,65
KSO[0..17] 24,65
AFTP24
AFTP25
AFTP26
AFTP27
AFTP28
AFTP29
AFTP30
AFTP32
AFTP33
AFTP39
AFTP40
AFTP41
AFTP42
AFTP43
AFTP44
AFTP45
AFTP156
AFTP157
AFTP48
AFTP50
AFTP49
AFTP51
AFTP53
AFTP52
AFTP54
AFTP55
AFTP140
AFTP145

HDMI

S7 HDMI_CLK_CON_N3
S7 HDMI_CLK_CON_P3
S7 HDMI_DATA_CON_P0
S7 HDMI_DATA_CON_N0
S7 HDMI_DATA_CON_P1
S7 HDMI_DATA_CON_N1
S7 HDMI_DATA_CON_P2
S7 HDMI_DATA_CON_N2
S7 HDMI_CLK_CON
S7 HDMI_DATA_CON
S7 HDMI_DET_CON
5V_HDMI_S0
AFTP121
AFTP122
AFTP124
AFTP123
AFTP126
AFTP125
AFTP128
AFTP127
AFTP130
AFTP129
AFTP132
AFTP131
AFTP146

Speaker

29 OUT_RP
29 OUT_RN_CON
29 SPK_RINRVP
27,29 AUD_SPK1_R_L-
27,29 AUD_SPK1_R_L+
27,29 AUD_SPK1_R_R-
27,29 AUD_SPK1_R_R+
AFTP160
AFTP159
AFTP158
AFTP16
AFTP18
AFTP19
AFTP20

CLIP1 SUL-0815A1-GP
CLIP2 SUL-0815A1-GP
CLIP3 SUL-0815A1-GP
34.4L601.001
34.4L601.001
34.4L601.001
-2 20170519

H1 HT85B95X975R29-S-GP
H2 HOLE335R115-GP
H3 HT85B95X975R29-S-GP
H4 HOLE276R150-GP
H5 HOLE276R150-GP
ZZ.00PAD.D71
ZZ.00PAD.D01
ZZ.00PAD.D71
ZZ.00PAD.H91
ZZ.00PAD.H91

HS1 STF237R128H34-4-GP
HS2 STF237R128H34-4-GP
HS3 STF237R128H34-4-GP
34.4YP25.001
34.4YP25.001
34.4YP25.001
-3 20170717

For CPU Bracket

PTH2 HOLE170X130R138X99-GP
PTH3 HOLE170X130R138X99-GP
ZZ.SCREW.S91
ZZ.SCREW.S91

P T H 橢圓短 位孔

Top side

SPR1 SPRING-98-GP
SPR2 SPRING-98-GP
SPR3 SPRING-98-GP
DY
34.34S02.002
34.34S02.002
34.34S02.002

EMI Soluation

19V_DCBATOUT
-SB 20170314 EMC SUGGEST
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910 EC8911
PWR_DCBATOUT_1D0V
PWR_DCBATOUT_VCOREB
PWR_DCBATOUT_VCOREA
PWR_DCBATOUT_VCCGTA
5V_S5
-SB 20170314 EMC SUGGEST
EC8912 EC8913 EC8914 EC8915
EC8916

RF Soluation

5V_S5
5V_S0
5V_S5
PWR_3D3V
BT+
PWR_DCBATOUT_5V
1V_CPU_CORE
1V_CPU_CORE
FC8901 FC8902 FC8903 FC8904 FC8905 FC8906 FC8907 FC8908 FC8909 FC8910 FC8911 FC8912 FC8913 FC8914 FC8915 FC8916 FC8917 FC8918 FC8919

20170120
19V_AD+
-SB 20170314 EMC SUGGEST
19V_DCBATOUT
FC8932 FC8933 FC8934 FC8935

1V_VCCGT
BT+
3D3V_IOAC
PWR_5V
1V_VCCGT
3D3V_MSATA1_S0
AD+_TO_SYS
PWR_DCBATOUT_3D3V
1V_VCCSA
FC8920 FC8921 FC8922 FC8923 FC8924 FC8925 FC8926 FC8927 FC8928 FC8929 FC8930 FC8931

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 89 of 106

Blanking

Count

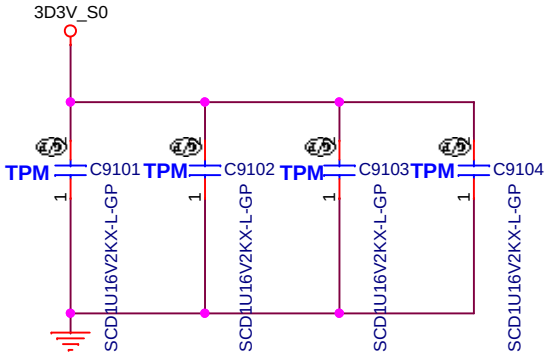
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

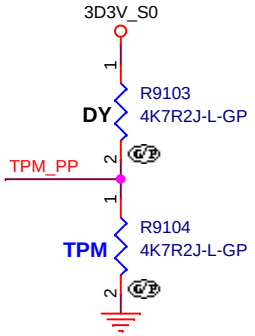
Title: ***NFC(Reserved)***

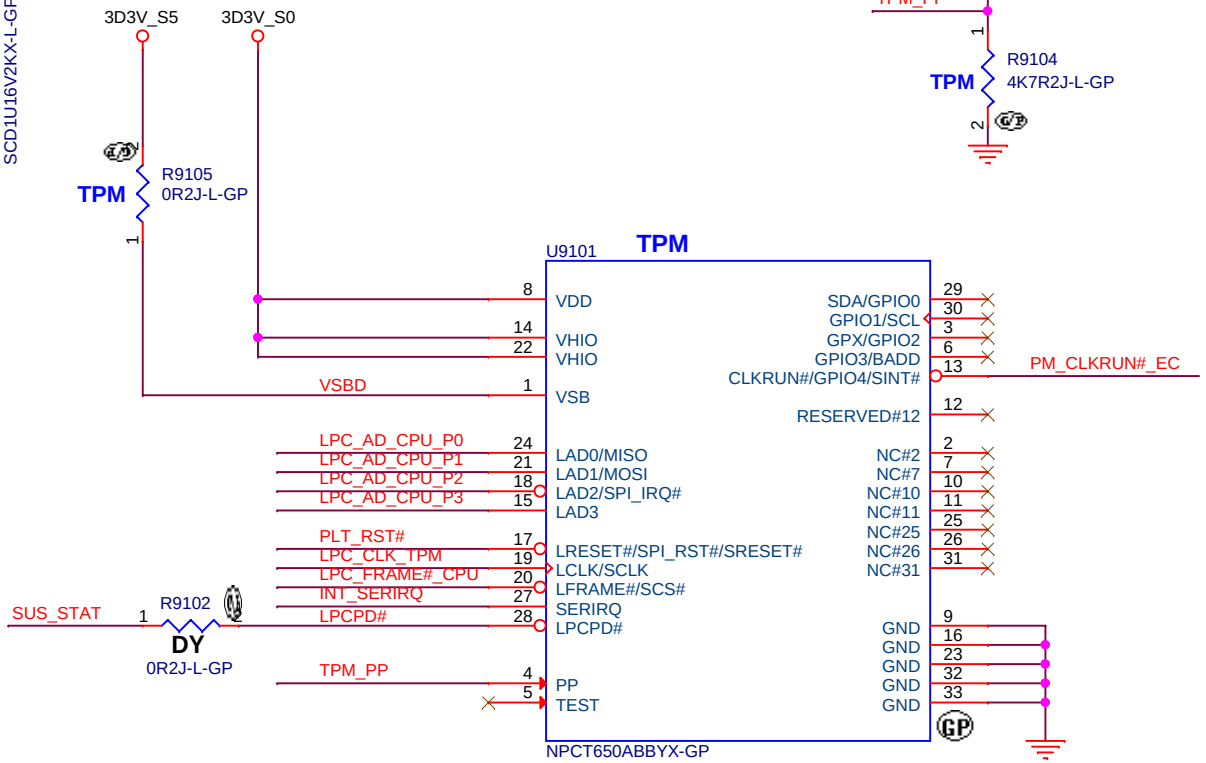
Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 90 of 106

18,24,68 LPC_AD_CPU_P0
18,24,68 LPC_AD_CPU_P1
18,24,68 LPC_AD_CPU_P2
18,24,68 LPC_AD_CPU_P3
18 LPC_CLK_TPM
18,24,68 LPC_FRAME#_CPU
20,24,61,62,68,89 PLT_RST#
18,24,68 INT_SERIRQ
18,24 PM_CLKRUN#_EC
18 SUS_STAT







071.00650.0N03

P/N: 071.00650.0N03

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TPM***	
Size A4	Document Number **Slinky**	Rev **-1**
Date: Thursday, August 24, 2017	Sheet 91 of 106	

15 FP_USB20_N

15 FP_USB20_P

89 FP_USB20_CON_N

89 FP_USB20_CON_P

3D3V_S0 — 1 R9201 2 — FP_3D3V_S0
0R0603-PAD

20170329 change

FP_3D3V_S0

FP_USB20_CON_P
FP_USB20_CON_N

FP1
10
8
7
6
5
4
3
2
1
9
FP

PTWO-CON8-17-GP

020.K0312.0008
2nd = 20.K0481.008

FP

EU9201

FP_USB20_CON_P — 1 I/O1 — I/O4 6 — FP_USB20_CON_N
2 GND — VDD 5 — 5V_S0
3 I/O2 — I/O3 4

AZC099-04S-2-GP

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

FP_USB20_P — R9202 1 — 2 0R0402-PAD — FP_USB20_CON_P

FP_USB20_N — R9203 1 — 2 0R0402-PAD — FP_USB20_CON_N

Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Print

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 92 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Express_Card(Reserved)***

Size	Document Number	Rev
A	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 93 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Smart Card scoket(Reserved)***

Size	Document Number	Rev
A	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 94 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GFX eDP(Reserved)***

Size	Document Number	Rev
A	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 95 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bottom Docking(Reserved)***

Size	Document Number	Rev
A	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 96 of 106

Blanking

Count

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Inter LAN WG1217LM(Reservrd)***	
Size A4	Document Number **Slinky**	Rev **-1**
Date: Thursday, August 24, 2017	Sheet 97 of 106	

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_CFG STRAP(Reserved)***

Size	Document Number	Rev
A	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 98 of 106

Blanking

Count

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_XDP(Reserved)***

Size	Document Number	Rev
A4	**Slinky**	**-1**

Date: Thursday, August 24, 2017 Sheet 99 of 106

Blanking

Count

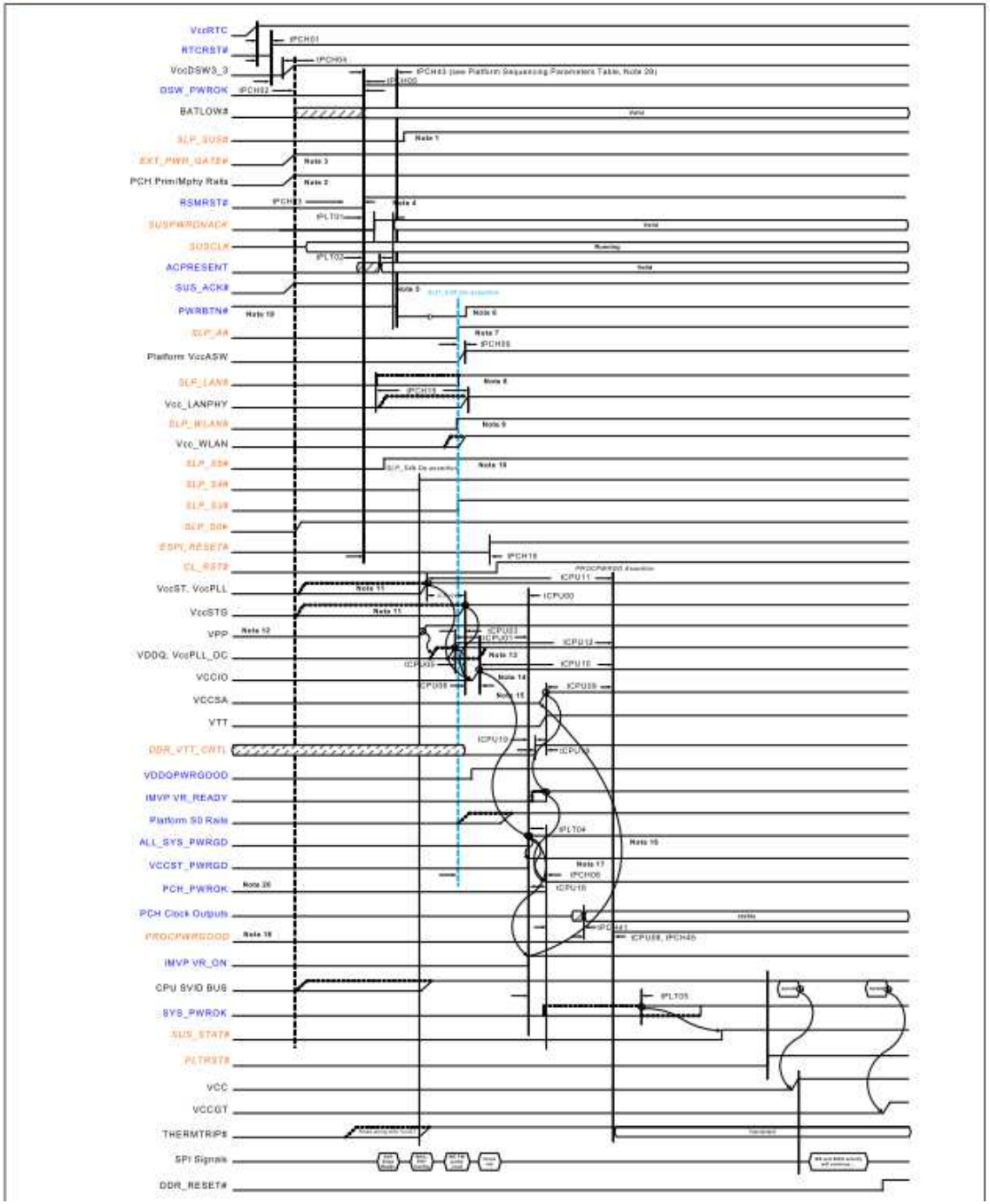
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***table of content***

Size	Document Number	Rev
A4	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 100 of 106

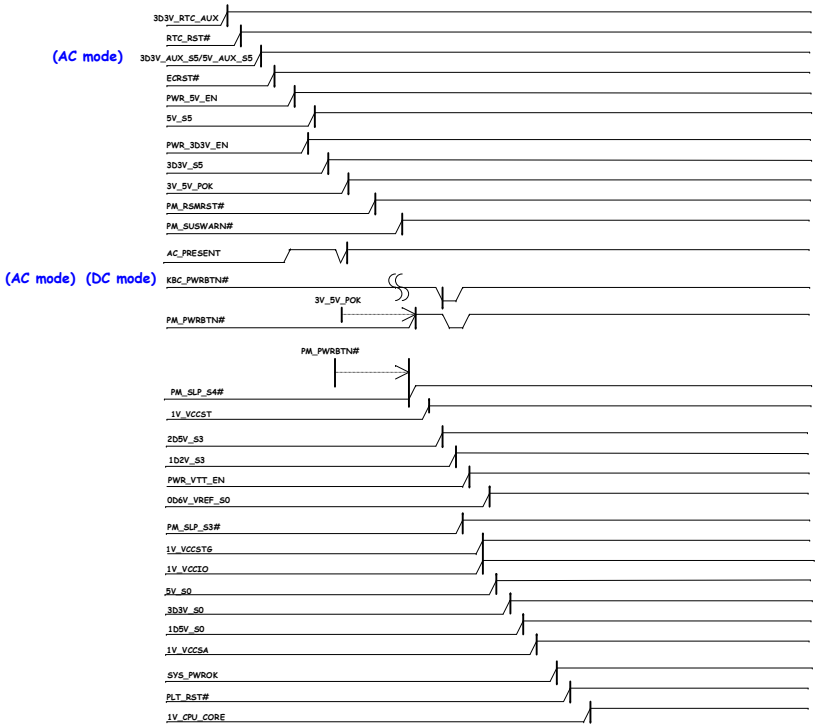
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

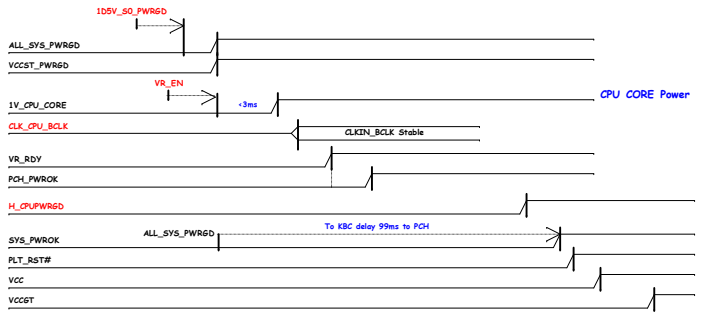


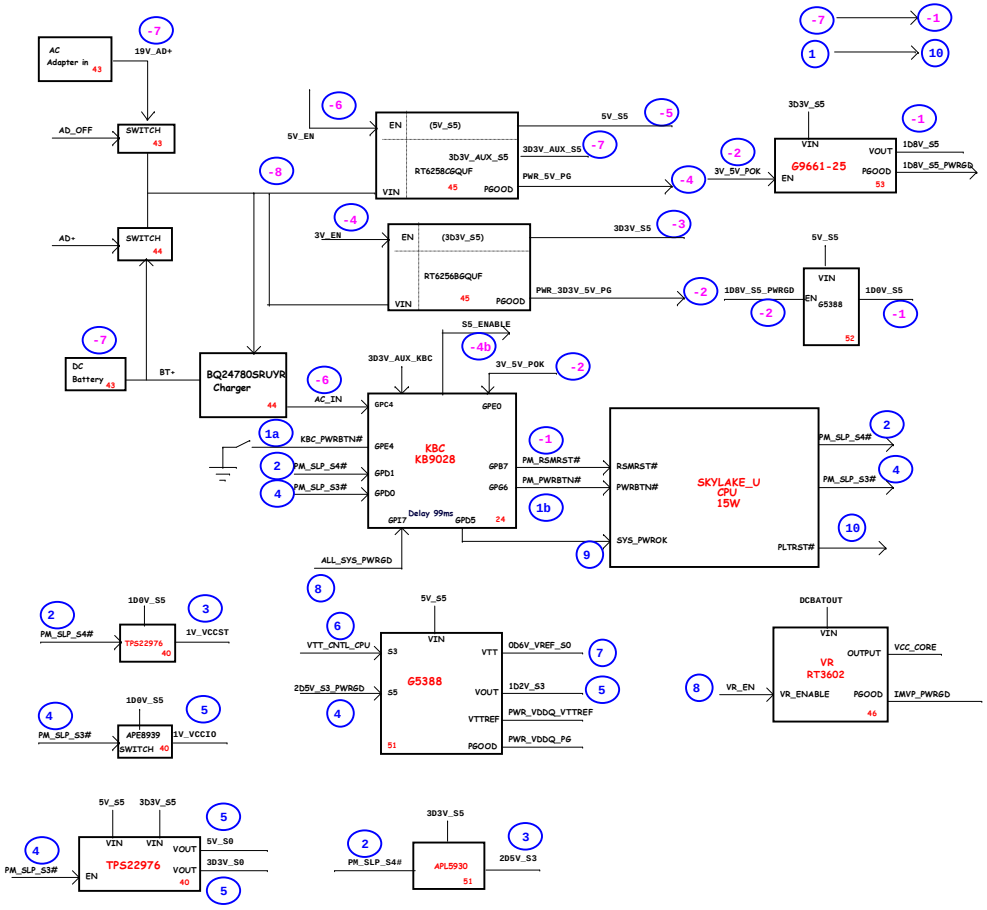
Count

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Change History***		
Size: A4	Document Number: **Slinky**	Rev: **-1**
Date: Thursday, August 24, 2017	Sheet 101 of 106	

Intel-Power Up Sequence

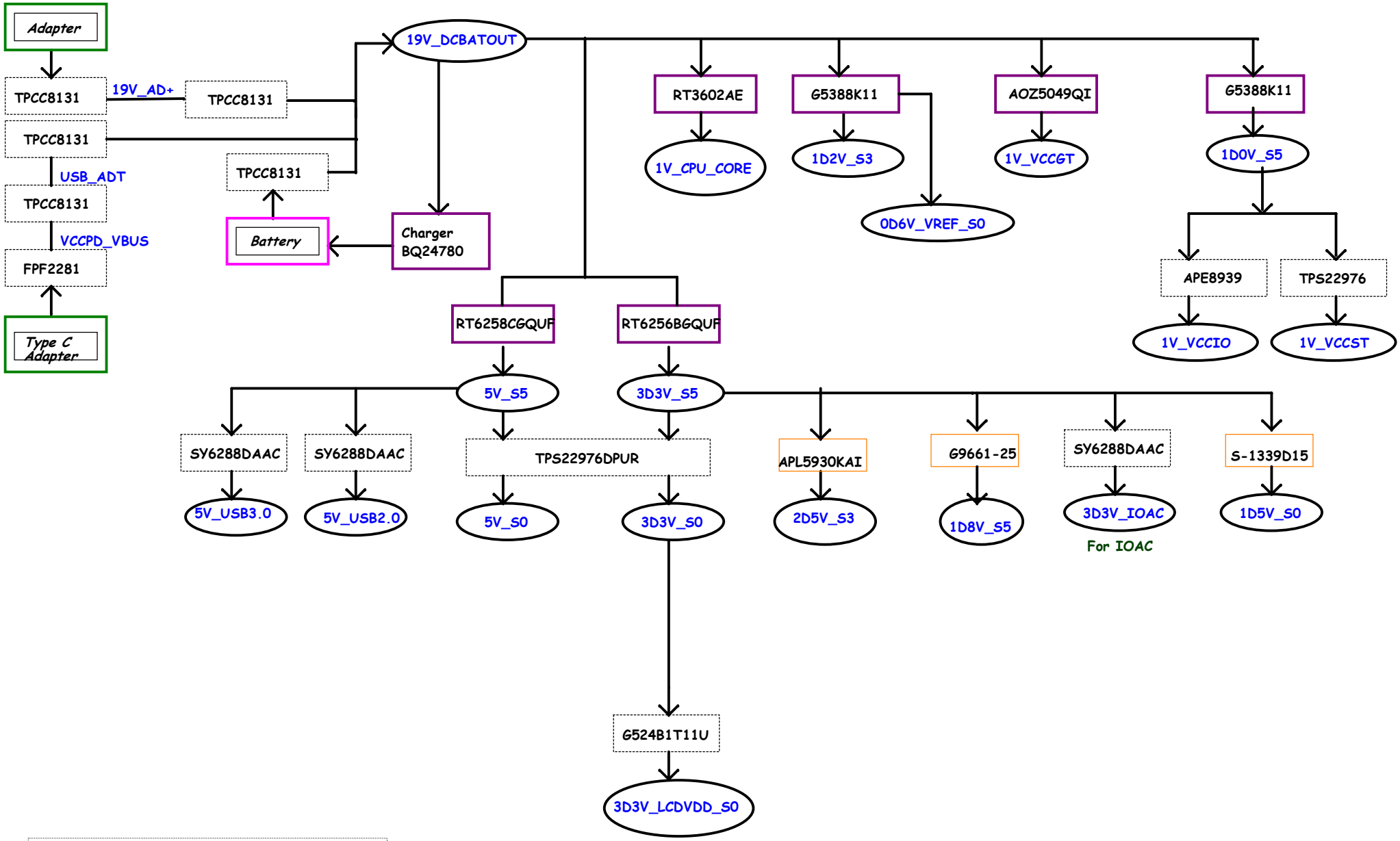






Count

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Power Sequence		
Size: A1	Document Number: Slinky	Rev: -1
Date: Thursday, August 24, 2017	Sheet 102 of 106	



Power Shape

Regulator | LDO | Switch

Count

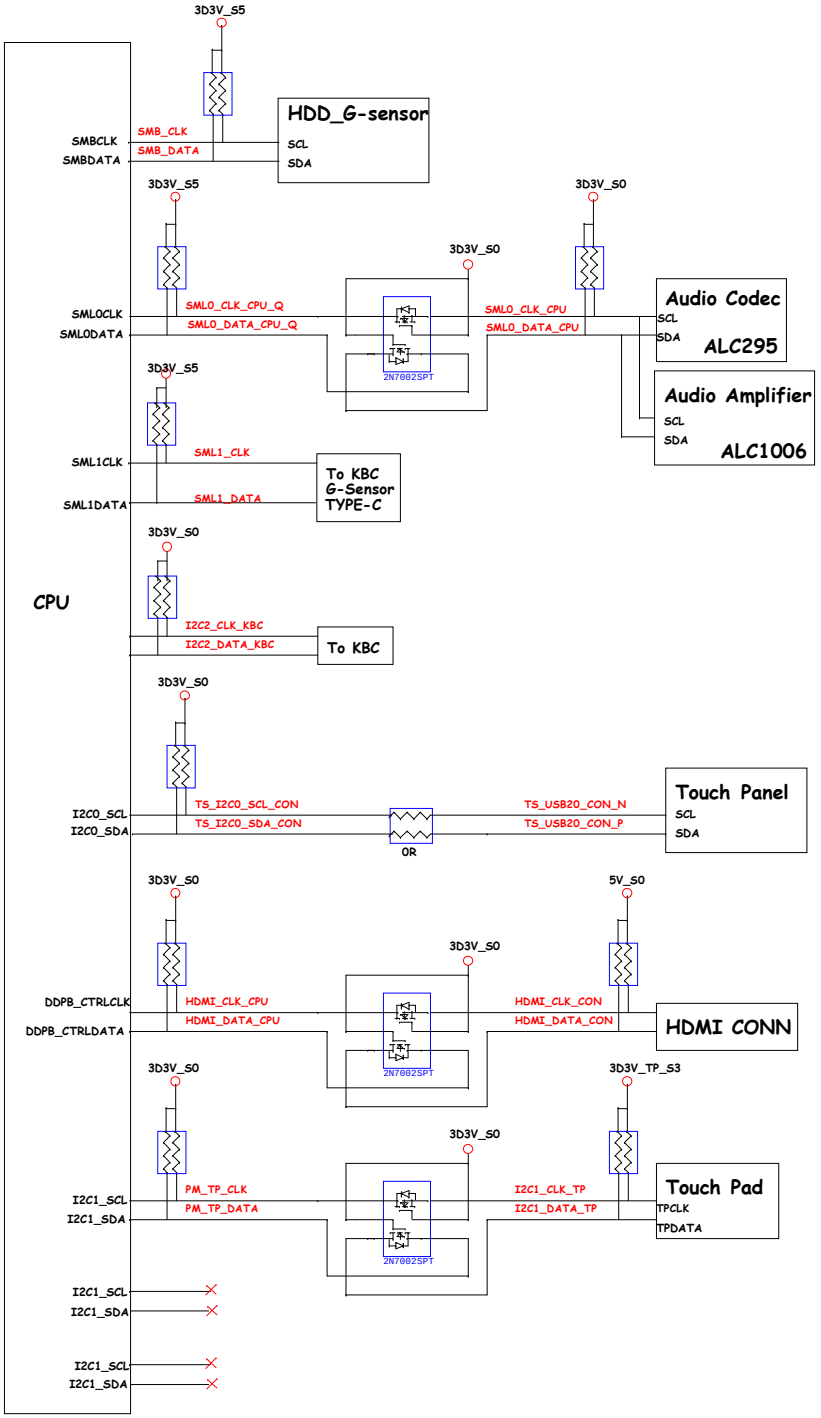
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

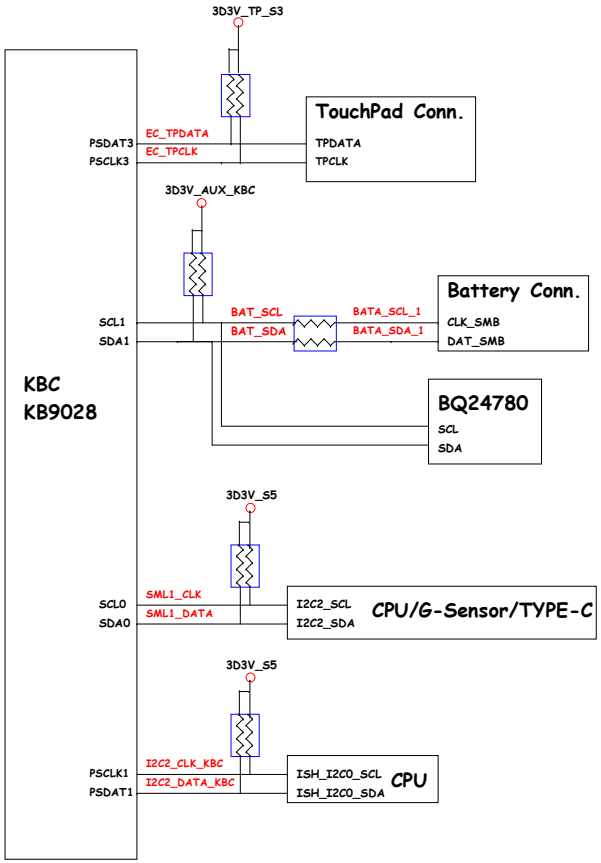
Size: A3 | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 103 of 106

PCH SMBus/I2C Block Diagram



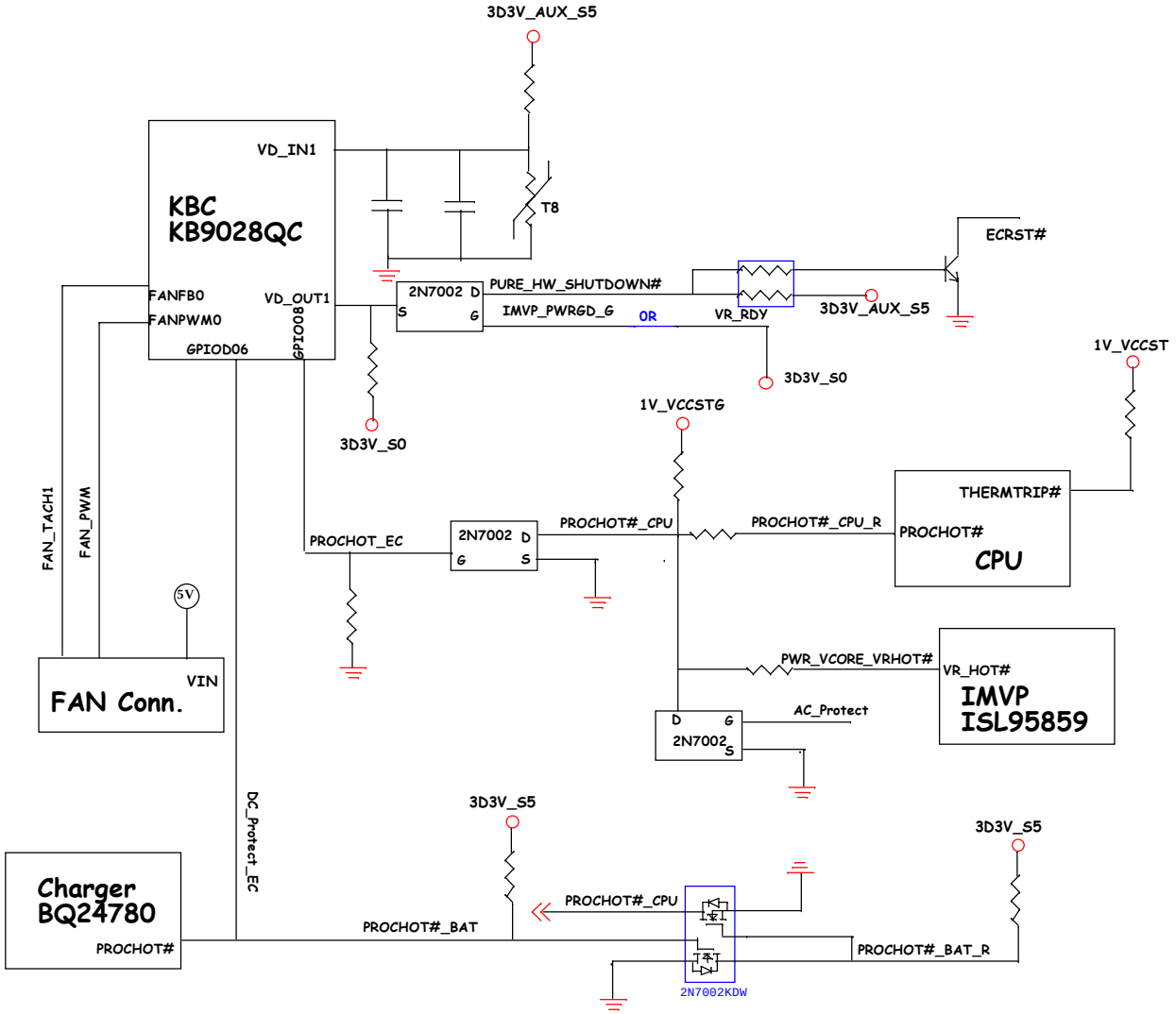
KBC SMBus/I2C Block Diagram



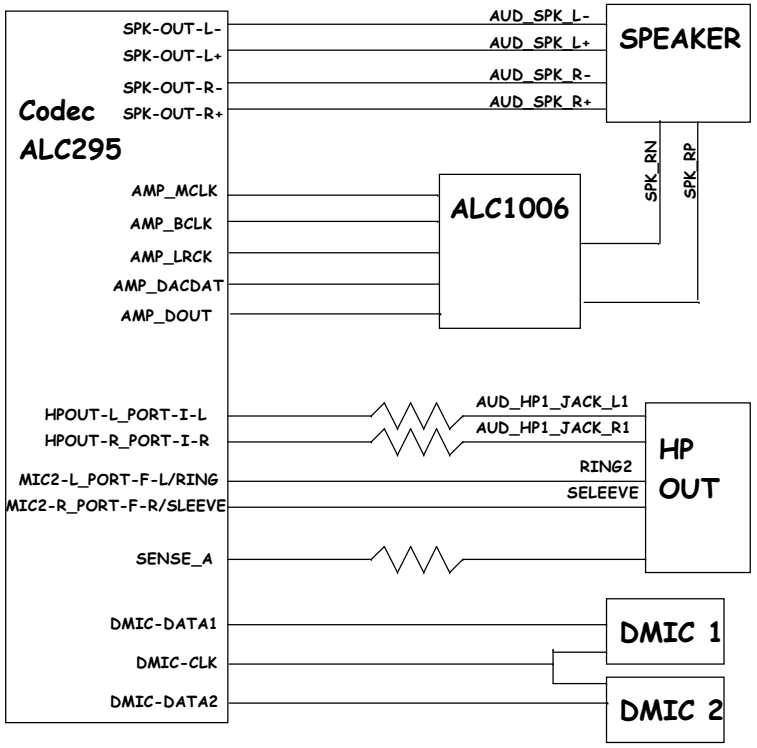
Count

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SMBUS BLOCK DIAGRAM	
Size A2	Document Number Slinky	Rev -1
Date: Thursday, August 24, 2017	Sheet 104 of 106	

Thermal Block Diagram



Audio Block Diagram



Count

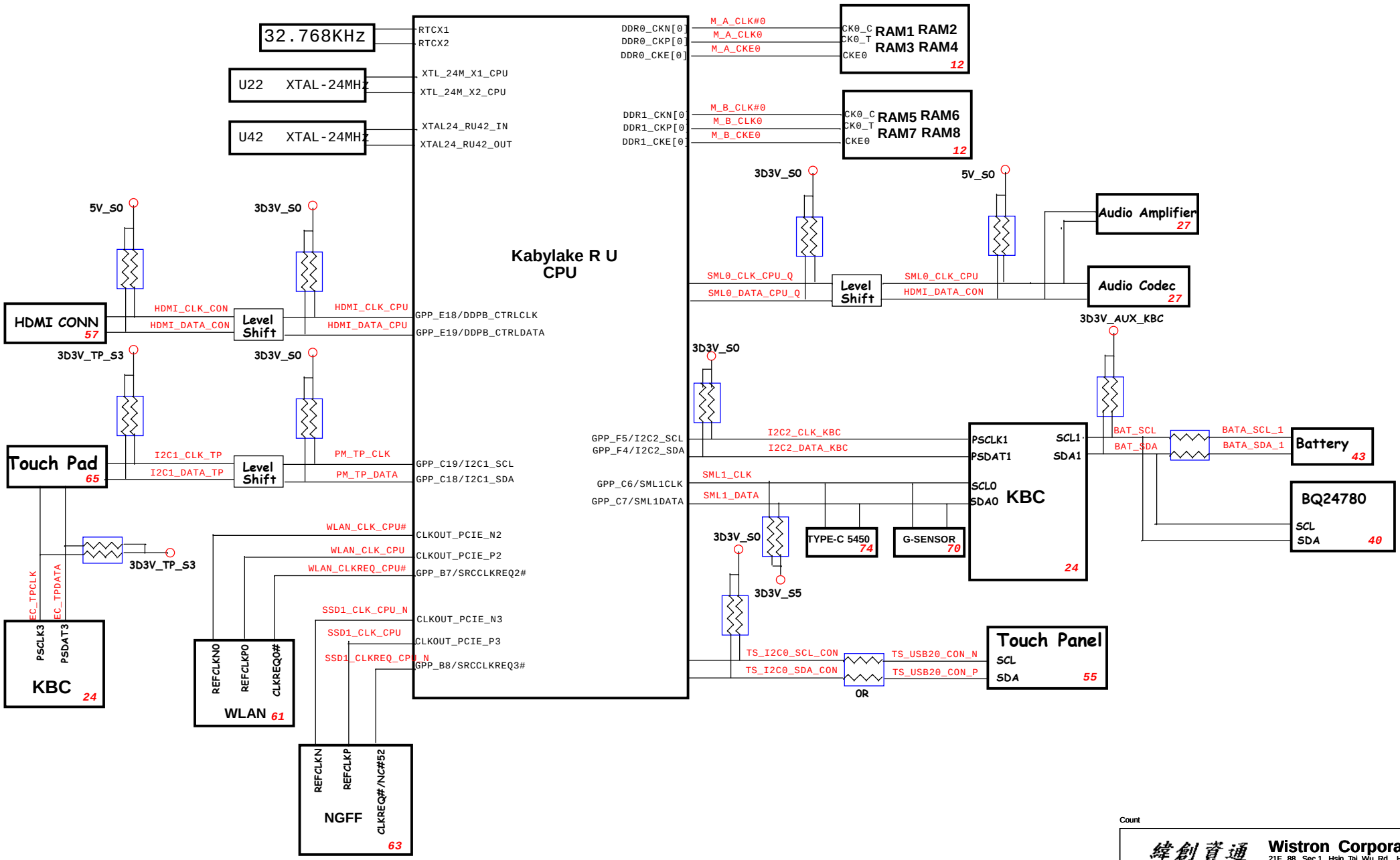
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL/AUDIO BLOCK DIAGRAM**

Size	Document Number	Rev
Custom	Slinky	-1

Date: Thursday, August 24, 2017 Sheet 105 of 106

CLOCK BLOCK DIAGRAM



Count

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLK Block

Size: Custom | Document Number: Slinky | Rev: -1

Date: Thursday, August 24, 2017 | Sheet 106 of 106