Project code:
LV115SK:4PD08B010001
LV114SK:4PD08A010001
PCB P/N: 15277/15309
Revision: SA
IO Board:

LV115/LV114 SKL-U
Block Diagram

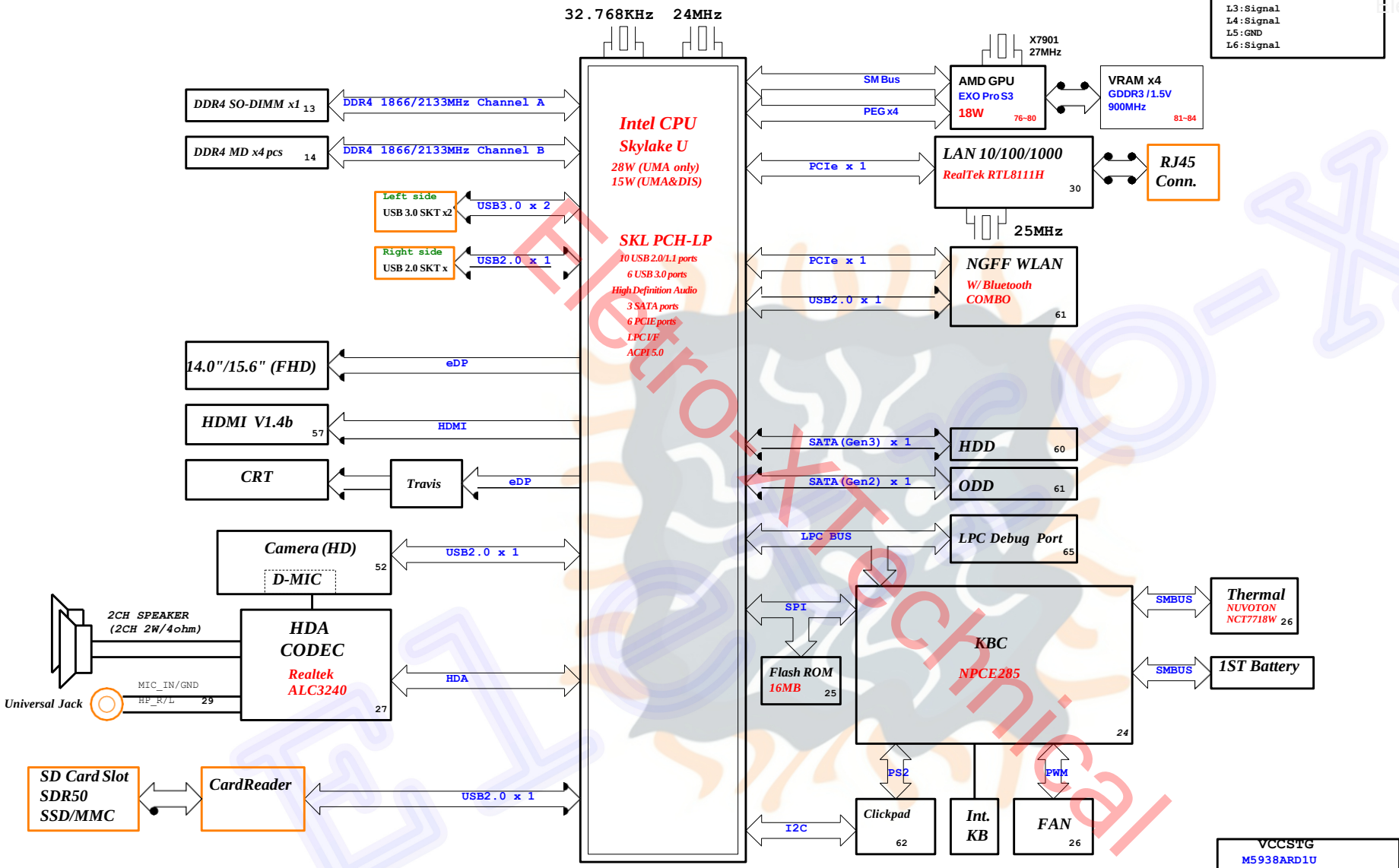
PCB	Halogen PN	No Halogen PN
LV115SK MB	15277	15309
LV115SK BTN BD	15902	15939
LV115SK AUDIO IO BD	15903	15940
LV115SK ODD BD	15904	15941

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page
Size: A3
Document Number: LV115 SKL-U
Rev: 1
Date: Monday, April 25, 2016
Sheet 1 of 1

LV115/LV114 SKL-U Block Diagram



PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

CHARGER BQ24780RUYR 44

INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	

SYSTEM DC/DC TPS51275CRUKR 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power
NCP81208MNTXG 46~50
NCP81382MNTXG x 2
NCP81382MNTXG (23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+V_VCCGTUS_VR (23e only)
DCBATOUT	+VCCSA_VR

DDR3L SUS TPS51716RUKR 51

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU VCCIO 0.975V RT8068AZQWID 52

INPUTS	OUTPUTS
3D3V_S5	+VCCIO_VR

CPU VCCPRIM_CORE 0.95V TPS22961DNYT 52

INPUTS	OUTPUTS
3D3V_S5	VCCPRIM_CORE

CPU DCDC-V1D00A AOZ1268QI 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V TLV70215DBVR 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V RT9025-25ZSP 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G5016KD1U 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00DX 40

VCCST M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU 40

EOPIO/EDRAM (23e) TPS22961DNYT 52

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA G5016KD1U 86

INPUTS	OUTPUTS
3D3V_S0 3D3V_S0	+V_EDRAM_VR +V_EOPIO_VR

<Core Design>

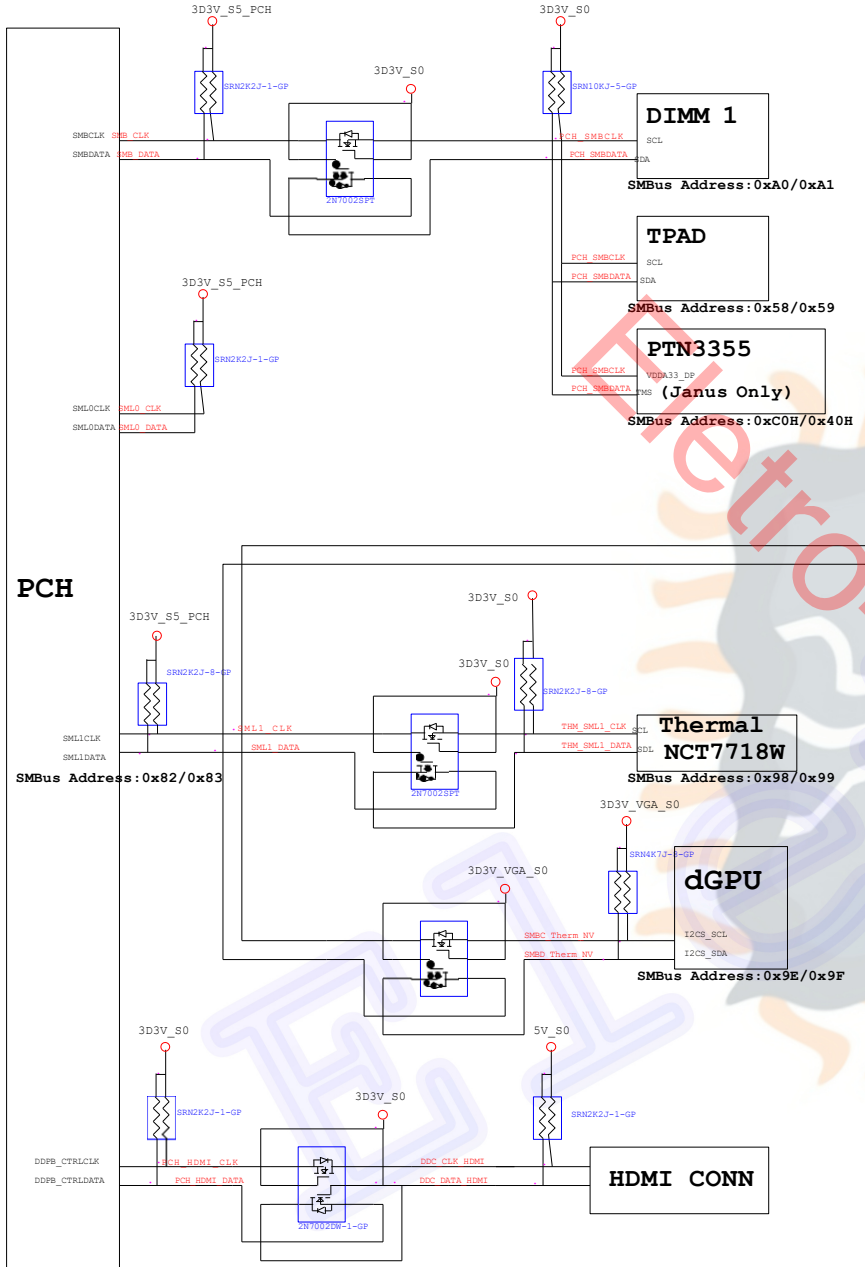
緯創資通 Wistron Corporation

Title: Block Diagram

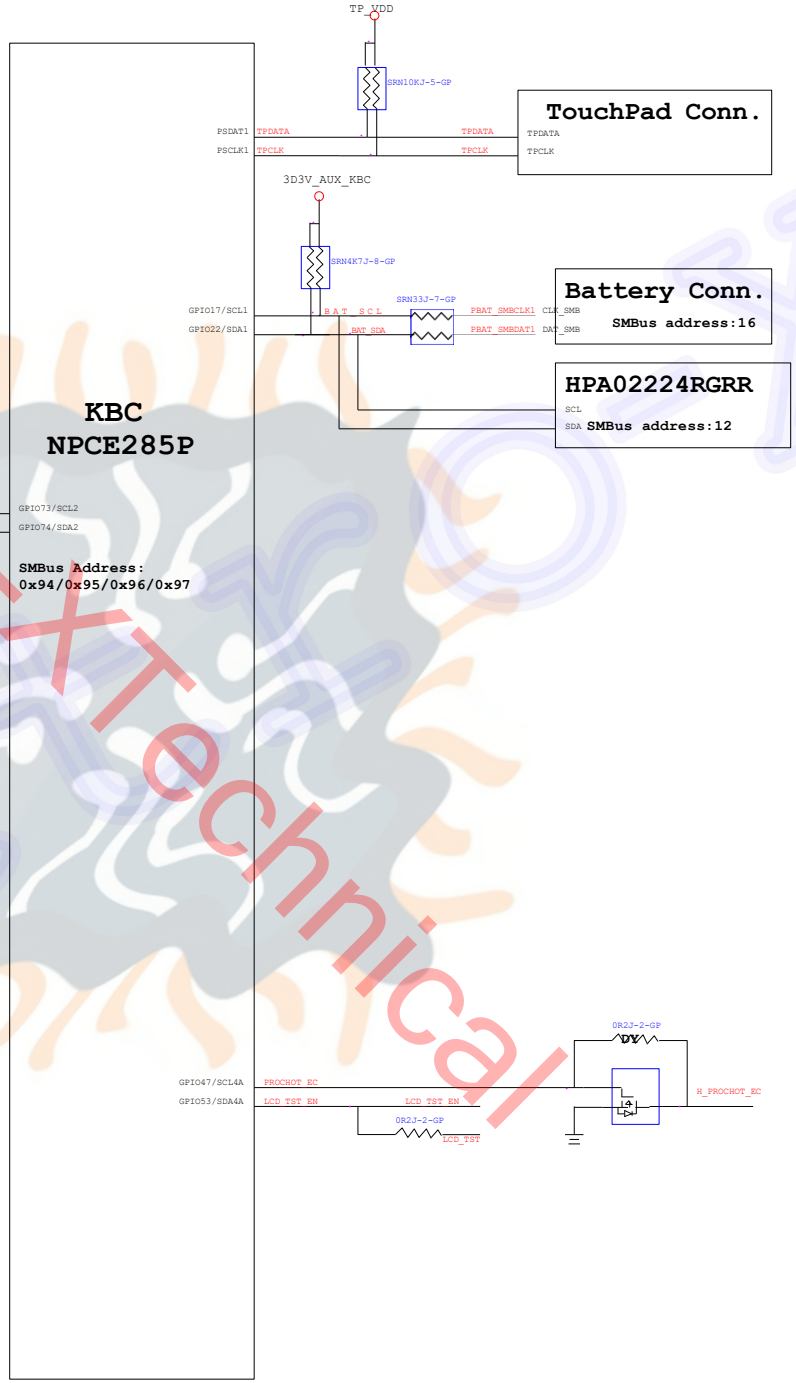
Size: C | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 2 of 102

PCH SMBus Block Diagram

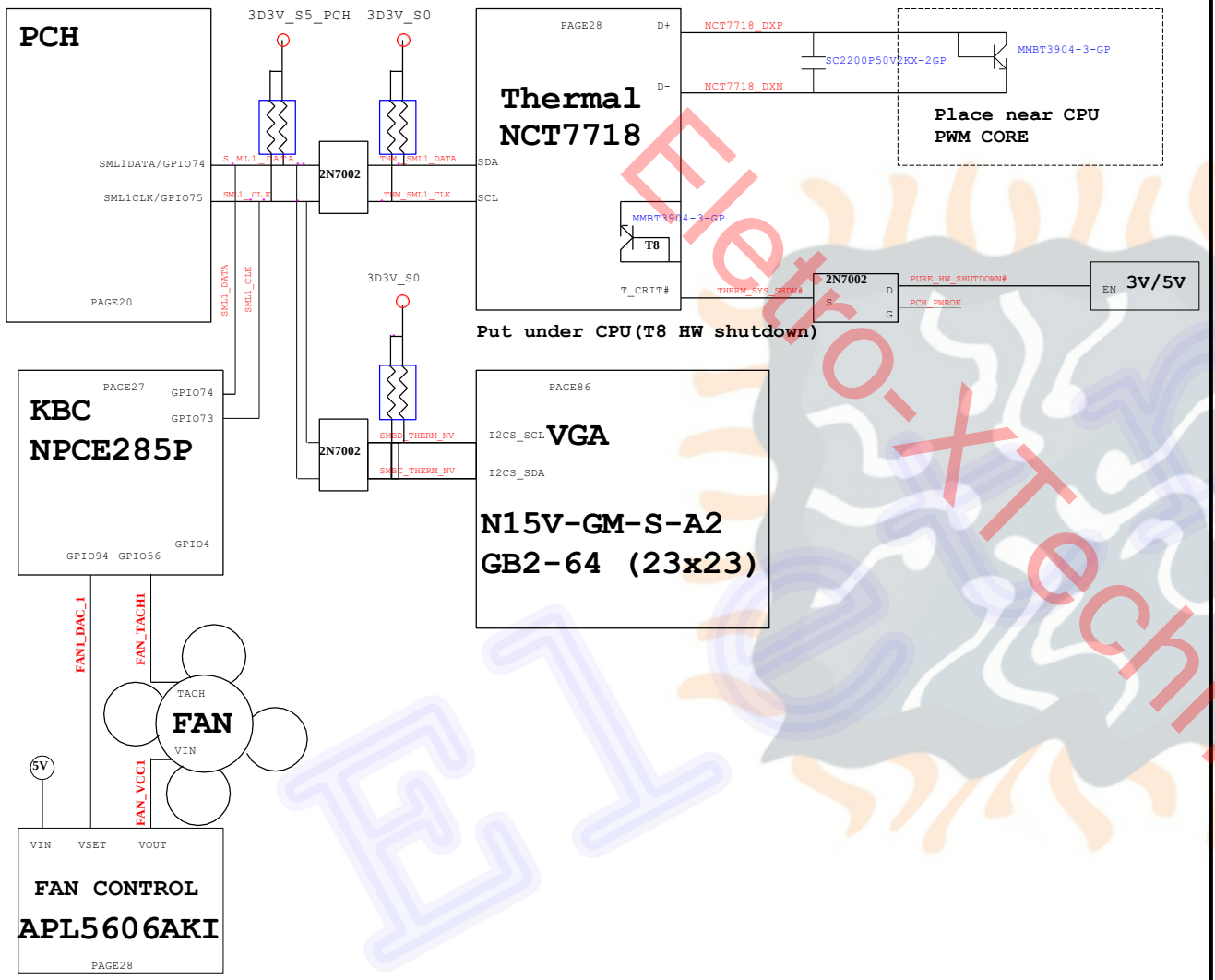


KBC SMBus Block Diagram

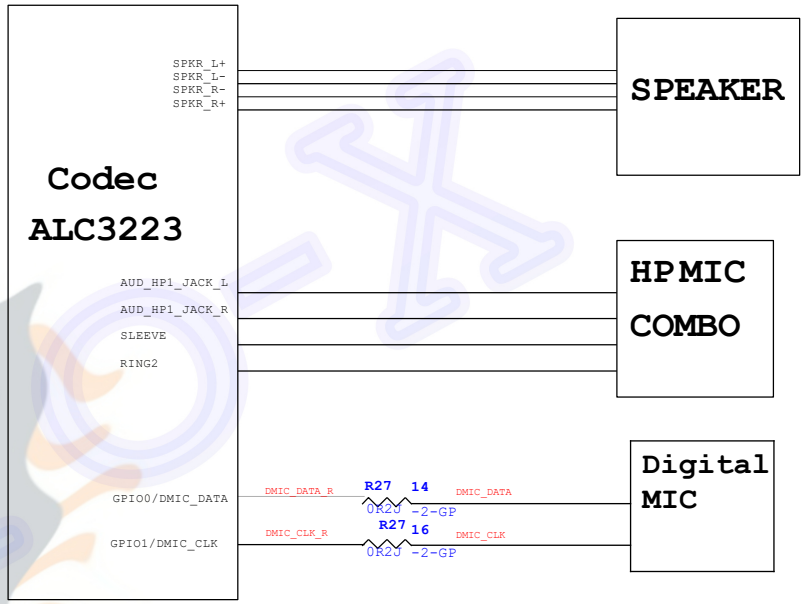


<Core Design>
緯創資通 Wistron Corporation
21F., 88, Sec.1, HsinTai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: SMBUS BLOCK DIAGRAM
Size: A2
Document Number: LV115 SKL-U
Date: Monday, April 25, 2016
Sheet 104 of

Thermal Block Diagram

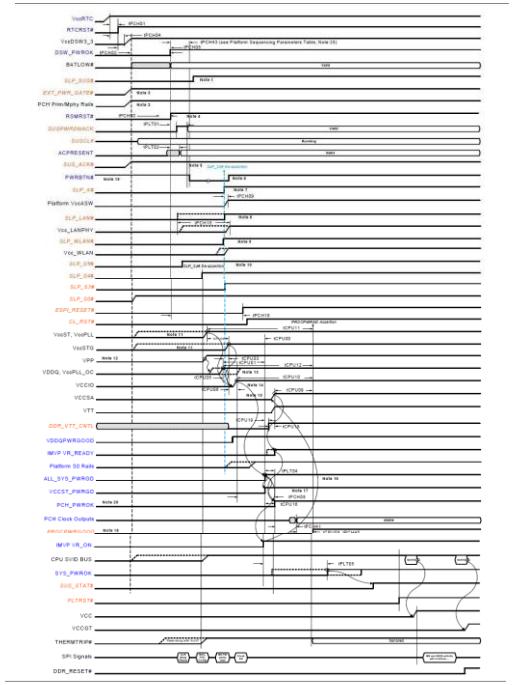


Audio Block Diagram



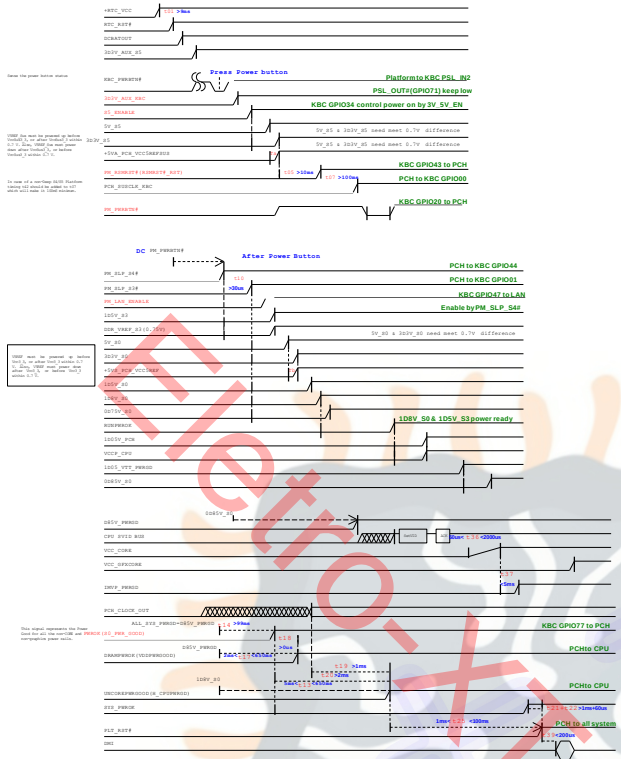
<core_design>
<Core Desiign>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: THERMAL/AUDIO BLOCK DIAGRAM
Size: Custom
Document Number: ODYSSEY SKL-U
Rev: 1
Date: Monday, April 25, 2016
Sheet 105 of 102
</core_design>

SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

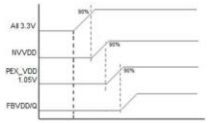


(DC mode)

Red Words: Controlled by EC GPIO



[dGPU] N16x Power-Up/Down Sequence



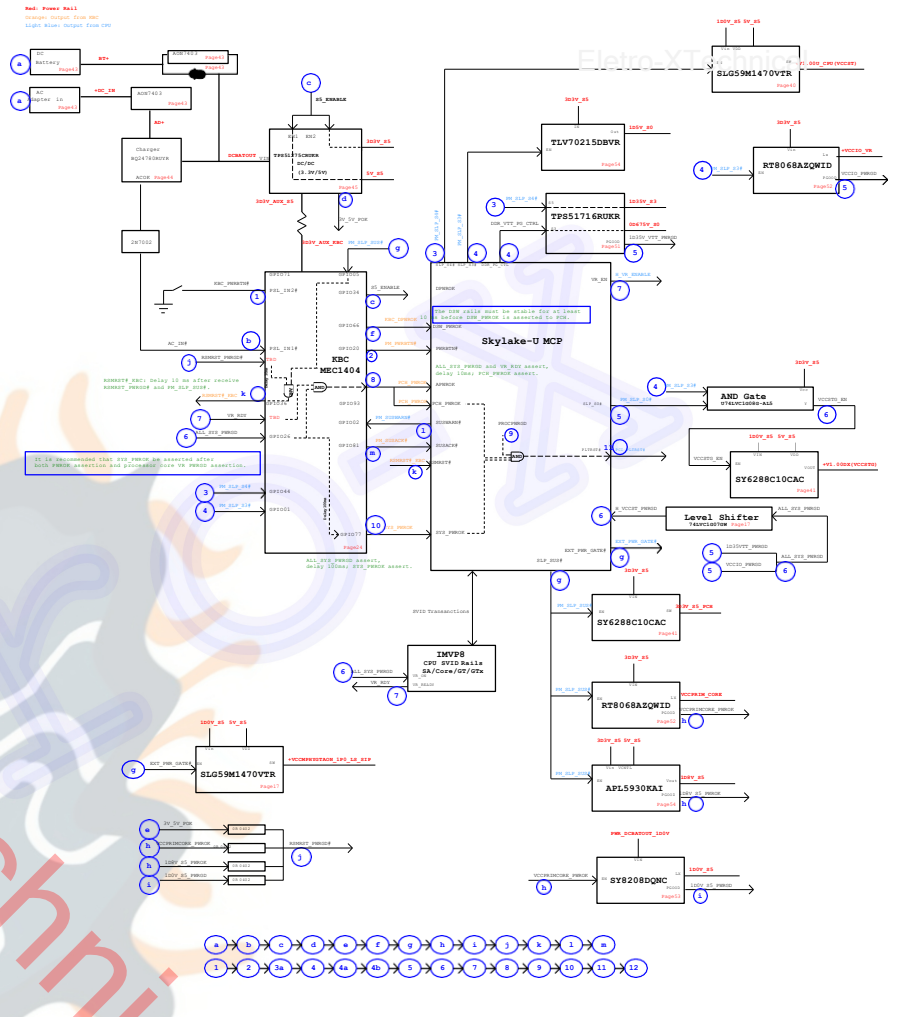
Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

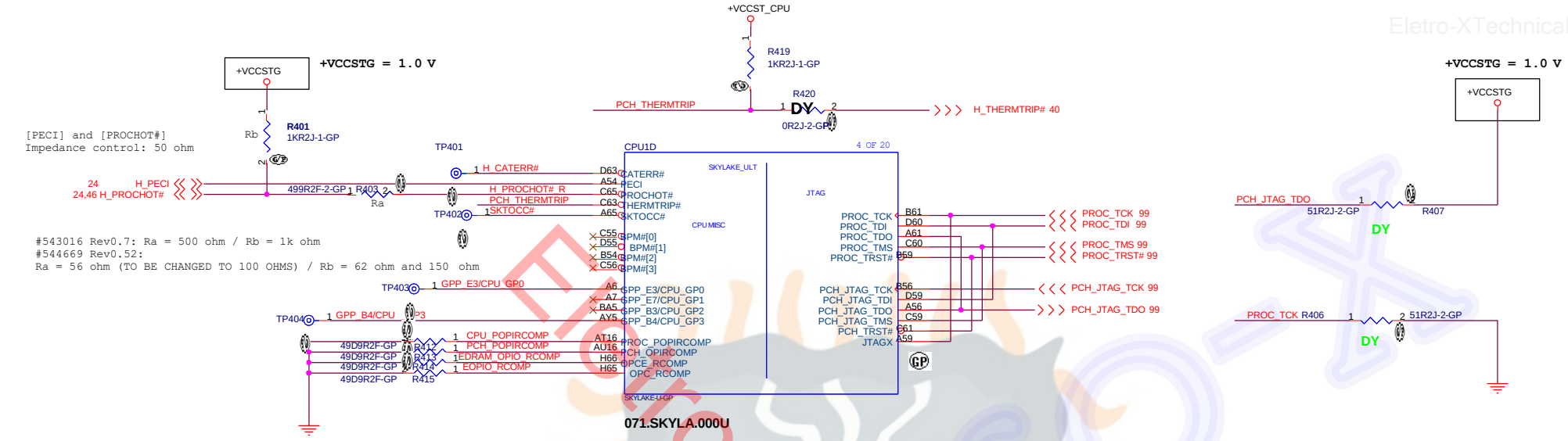
3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

Skylake POWER UP SEQUENCE DIAGRAM

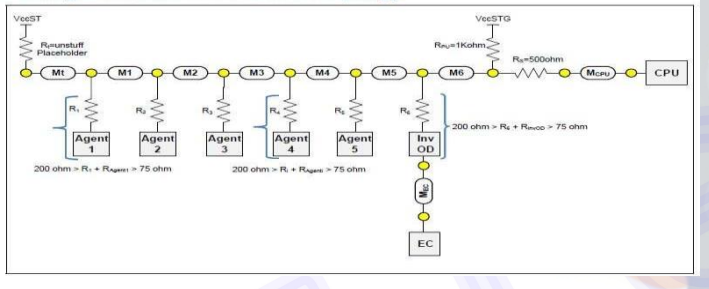


Main Func = CPU



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1~11 inches
MCPU: 0.3~1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1~12 inches

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (JTAG/CPU SIDE BAND)

Size: A3 | Document Number: LV115 SKL-U | Rev: 1

Date: Monday, April 25, 2016 | Sheet 4 of

Main Func = CPU

DDR4 ball type: Interleaved Type

M_A_BG1
M_VREF_DQ_DIMM0
Reserve Testpoint only

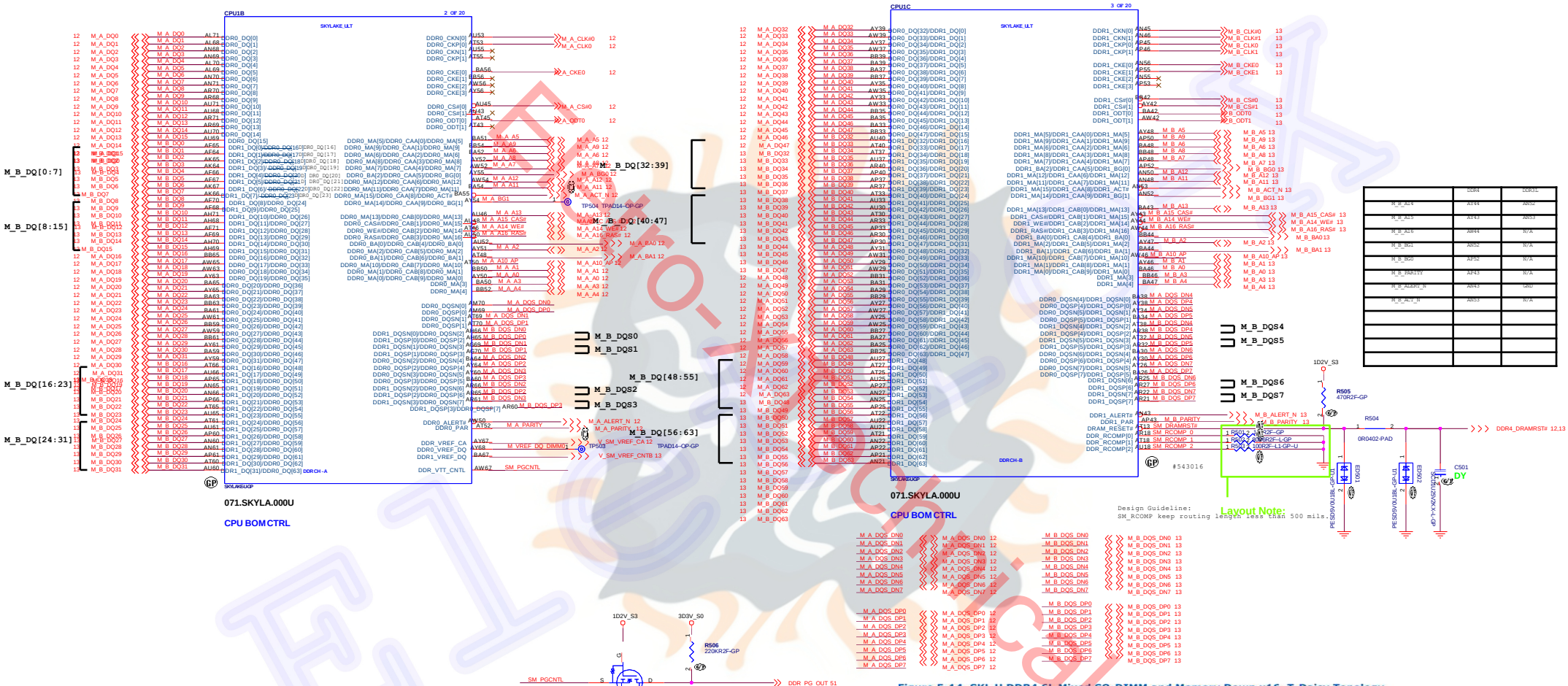
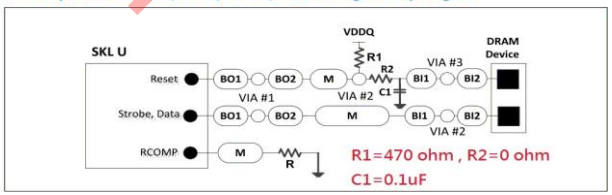


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



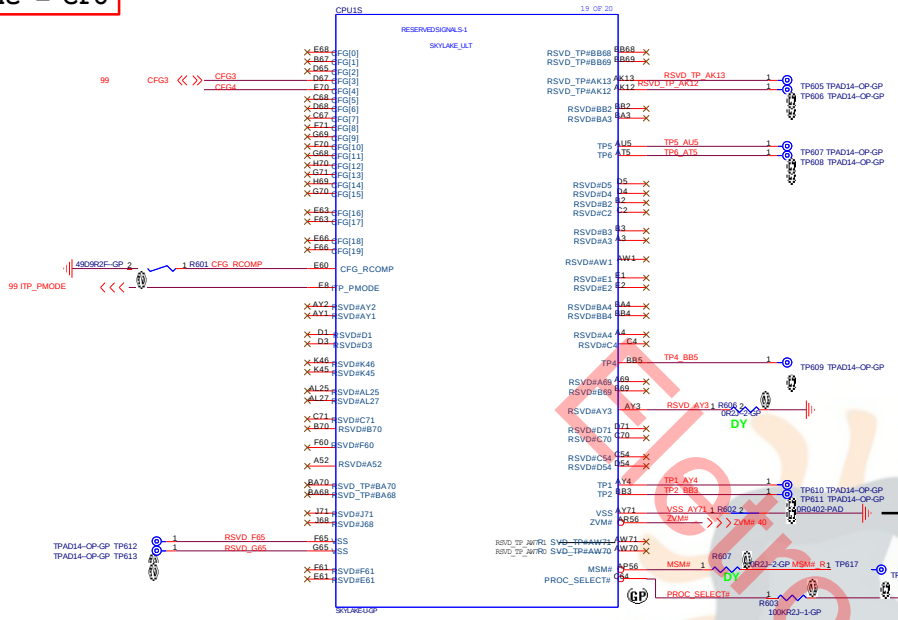
<Core Design>

Wistron Corporation
2F, 88, Sec. 1, HsinTai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)
Size: A2
Document Number: LV115 SKL-U
Date: Monday, April 25, 2016
Sheet 5

Eletro-XTechnical

Main Func = CPU



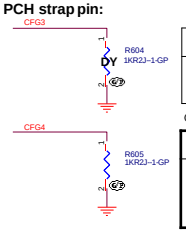
[#543016 Rev0.9]

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

PCH strap pin:

071.SKYLA.000U CPU BOM CTRL



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	1 : ENABLED An external Display Port device is connected to the Embedded Display Port. 0 : DISABLED (DEFAULT) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Desiign>

Wistron Corporation

CPU (RESERVED)

LV115 SKL-U

Monday, April 25, 2016

Sheet 6

Main Func = CPU

140mA

3A

3A

071.SKYLA..000U

CPU BOM CTRL

071.SKYLA..000U

CPU BOM CTRL

071.SKYLA..000U

CPU BOM CTRL

SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID CLOCK

Layout Note:
1. Place close to CPU
2. VCC_SENSE/VSS_SENSE impedance=50 ohm
3. Length match<25mil

SVID_543016:

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{Pull} [Ω]	R_{Pull2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{SF} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology

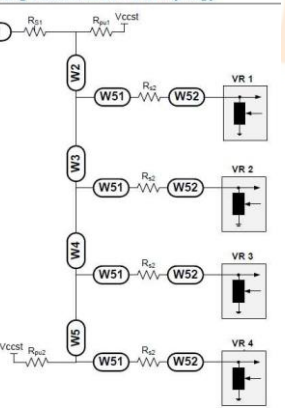


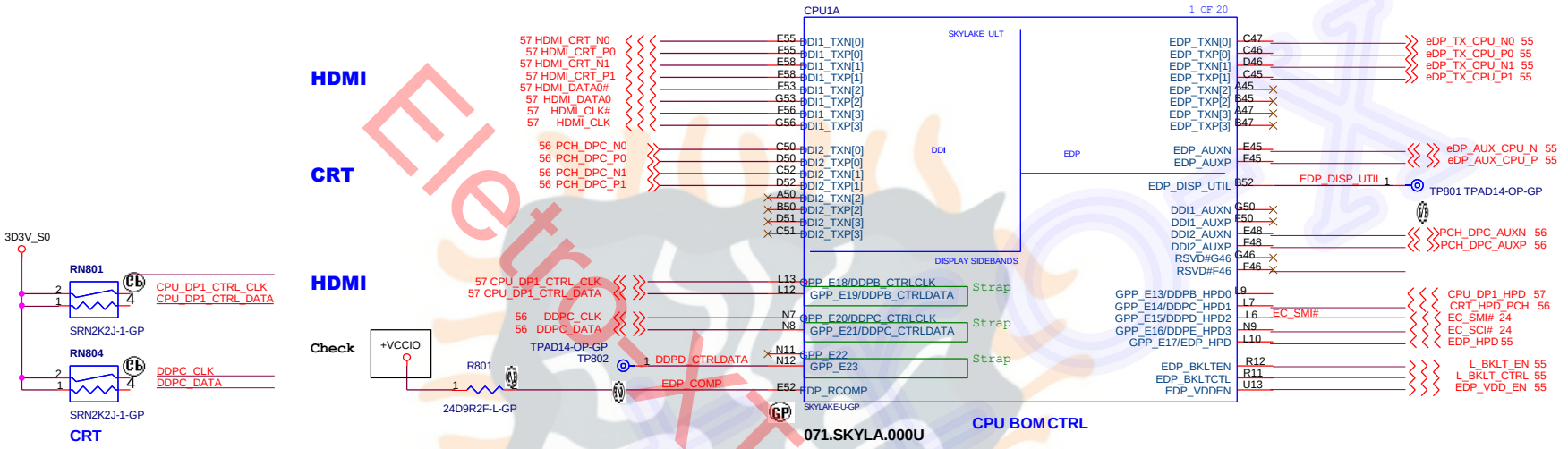
Table 55-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
V_{CCIO}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 1uF 0402	Place as close to the package as possible
V_{DDQ}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 10uF 0402	Place as close to the package as possible
		3 x 22uF 0603	Place as close to the package as possible
V_{DDQC}	1x 1uF 0201 (Placeholder)		Place on secondary side, underneath the package
		1 x 10uF 0402	Place as close to the package as possible
V_{CCPLL}		1x 1uF 0402	Place as close to the package as possible
V_{CCPLL_OC}		1x 1uF 0201	Place as close to the package as possible
V_{CCST}		1x 1uF 0402	Place as close to the package as possible
V_{CCSTG}	1x 1uF 0402 (Placeholder)		Place on secondary side, underneath the package Placeholder only
$V_{CCEOPIO}$	2x 10uF 0402		Place on secondary side, underneath the package
V_{CCOPC}	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

CPU/VCC_CORE

LV115 SKL

Main Func = CPU



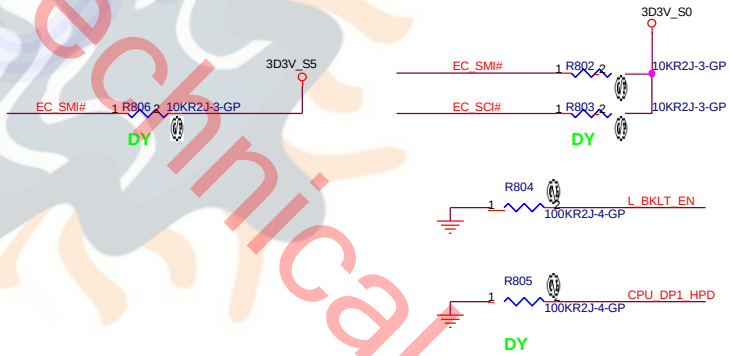
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien221, Taiwan, R.O.C.

Title: CPU_(DISPLAY)
Size: A3
Document Number: LV115 SKL-U
Rev: 1
Date: Monday, April 25, 2016
Sheet 8 of

Main Func = DDR4 On Board with Single Rank

C1201 close to ODIMM1.M1

C1202 close to ODIMM2.M1

C1203 close to ODIMM3.M1

C1204 close to ODIMM4.M1

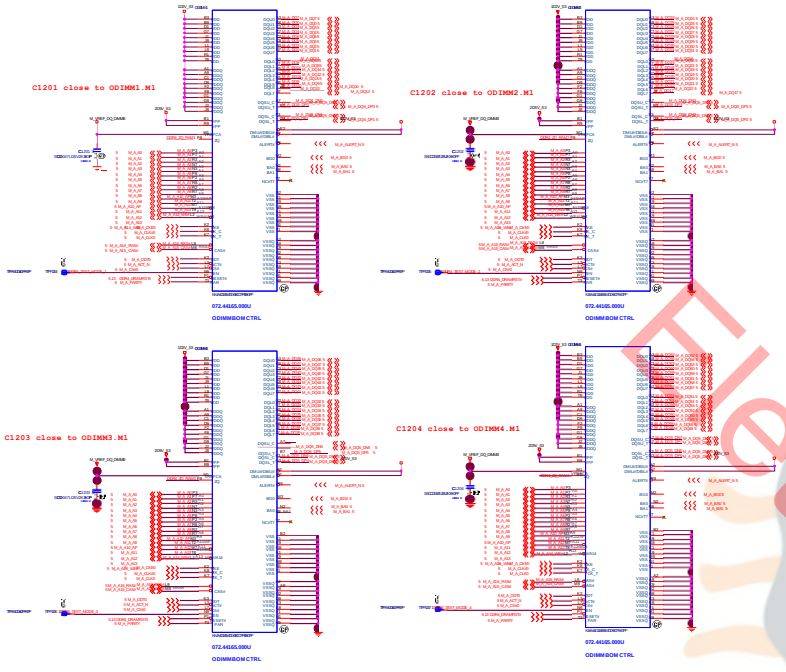


Figure 5-15. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down CLK/CTRL/CKE/CMD Signals Double-T Topology

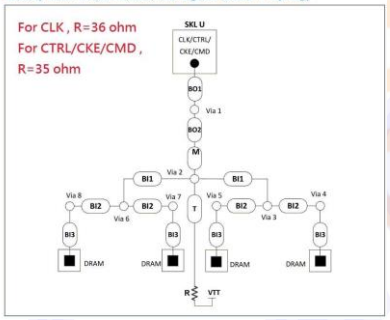
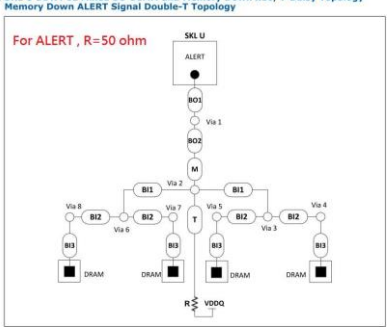
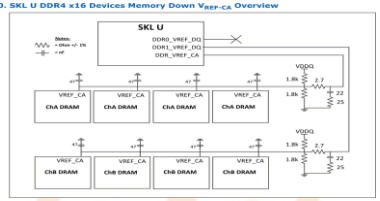


Figure 5-16. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down ALERT Signal Double-T Topology



Ref. 549360_SKL_U_6L_WP_P47

Figure 5-20. SKL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



DDR4 On Board RAM Power Decouple Cap

VDDQ/VDD 10uF x10

VDDQ/VDD 1uF x32

VPP 1uF x16

VTT 1uF x16

VPP 10uF x5

VTT 10uF x4

For ODIMM1,ODIMM2,ODIMM3,ODIMM4

LV115 use 1ch memory down , only need half of Caps

4.23.5 SKL-U DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

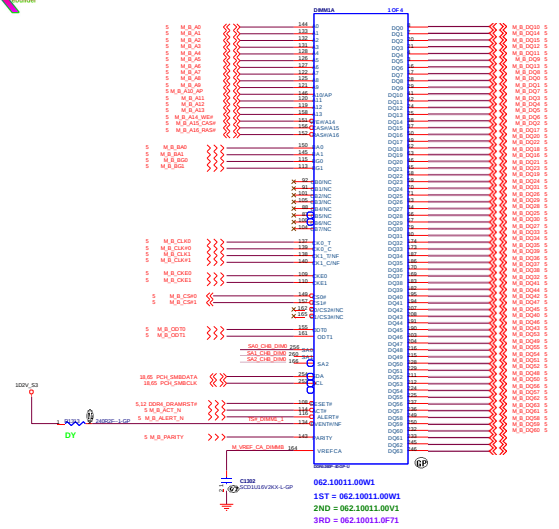
Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

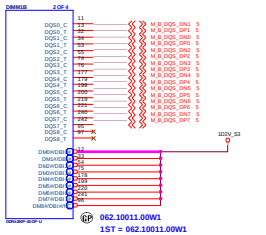
Memory Configuration	Power Domain	Decoupling Location	Qty × µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

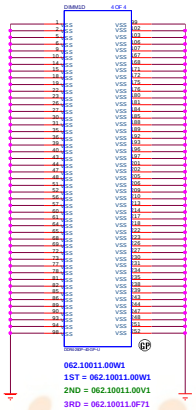
Wistron Corporation

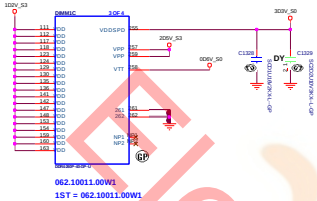
DDR4-SODIMM1

LV115 SKL-U









20151007 Change DIMM1 SKT PN

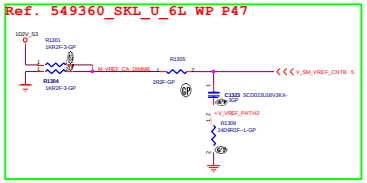
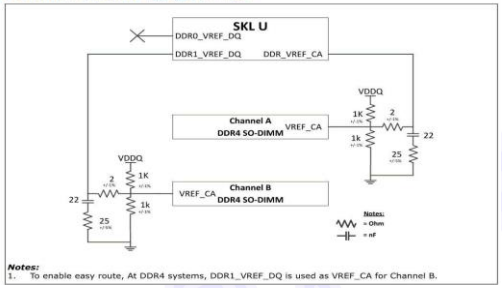
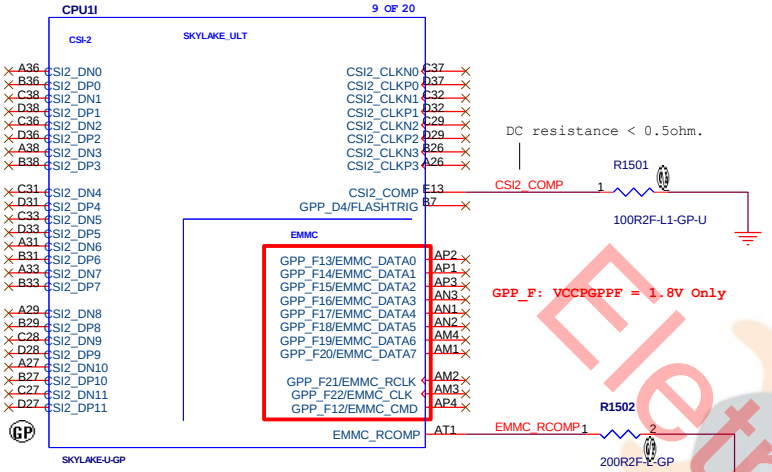


Figure 5-19. SKL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Main Func = PCH



071.SKYLA.000U

CPU BOMCTRL

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

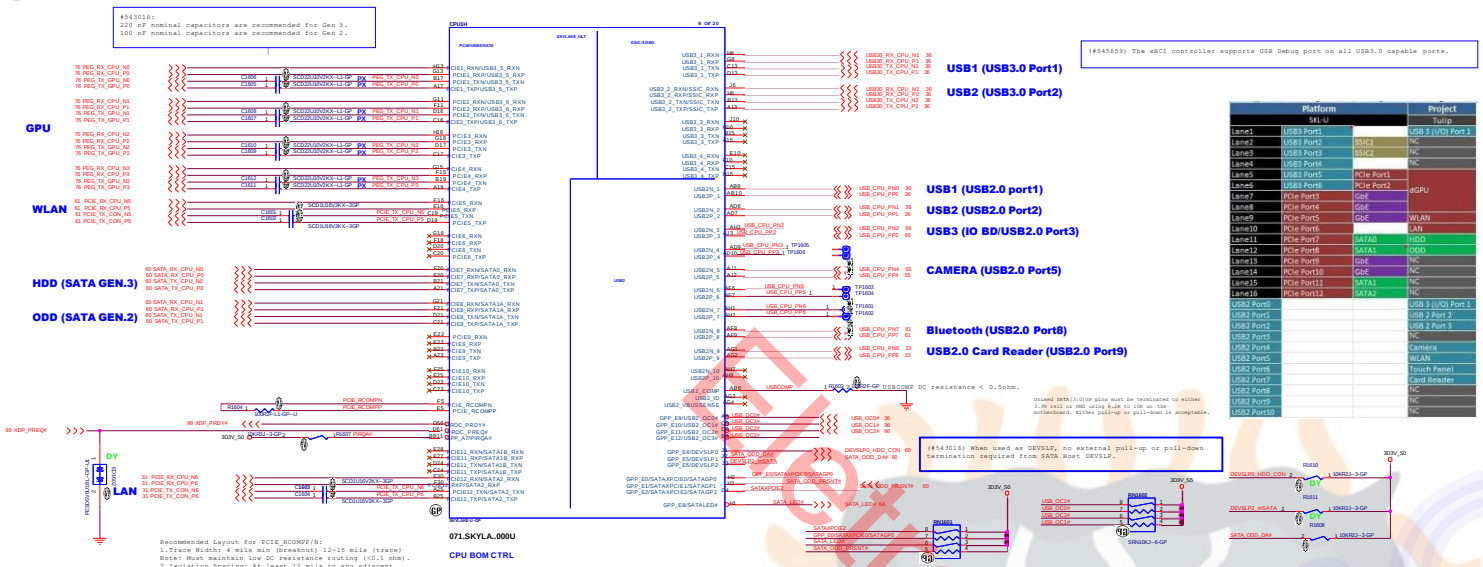
GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
Taiipeiii-Hsiien221, Taiiwan, R.O.C.

Title: CPU (CS-2/EMMC)
Size: A3
Document Number: LV115 SKL-U
Rev: 1
Date: Monday, April 25, 2016
Sheet 15 of

Main Func = PCH



PCIE Table

Port	Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	WLAN	
6	N/A	
7	N/A	SATA0 (HDD)
8	N/A	SATA1 (ODD)
9	N/A	
10	N/A	
11	N/A	
12	LAN	

USB 2.0 Table

Pair	Device
0	USB3.0 port1 (Debug Port)
1	USB2.0 Port2
2	USB2.0 Port3 (IOBD)
3	
4	CAMERA
5	
6	
7	Bluetooth
8	USB2.0 Card Reader
9	

20151024 Modify PCIE/USB2.0 Mapping Table

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

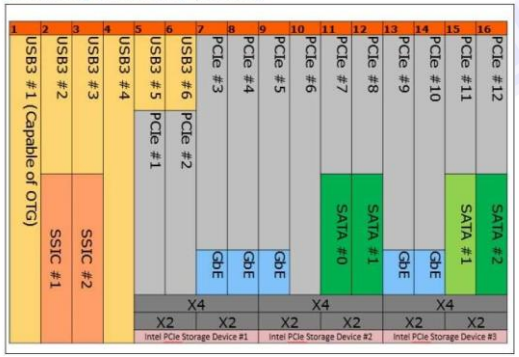


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s) x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes 1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH

3D3V_S5
R1709 10KR2J-3-GP AC_PRESENT
RN1701 SRN10KJ-5-GP SIO_PWRBTN# PCH_WAKE#
R1723 10KR2J-3-GP PCH_BATLOW#
RTC_AUX_S5
R1730 1MR2J-1-GP SM_INTRUDER#
R1733 10KR2J-3-GP PM_RSMRST#
ED1701 PESD5V0U1BL-GP-U1
R1732 8K2R2F-1-GP PM_PCH_PWROK
R1717 10KR2J-3-GP SYS_PWROK

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.
H_CPUPWRGD
AFTP1702
ED1702 PESD5V0U1BL-GP-U1
R1735 10KR2J-3-GP 24,31,79 PCH_WAKE#

3D3V_S0 3D3V_S5
R1711 10KR2J-3-GP
R1701 3KR2J-2-GP DY
ED1704 PESD5V0U1BL-GP-U1
40 H_THERMTRIP_EN
H_VCCST_PWRGD_R 0R2J-2-GP R1733
H_VCCST_PWRGD 60D4R2F-GP R1734
24 SYS_PWROK
40 PCH_PWROK
PM_RSMRST# R1706 0R0402-PAD R1704 0R0402-PAD
20,24 ME_SUS_PWR_ACK_R
3D3V_S5 R1707 10KR2J-3-GP

24,31,40,61,68,76 PLT_RST#
R1713 33R2J-2-GP PCH_PLTRST#
R1715 47KR2J-2-GP
C1701 SC100P50V2JN-3GP DY

CPU1K
SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
11 OF 20
PCH_PLTRST# GPP_B13/PLTRST#
XDP_DBRESET# SYS_RESET#
PM_RSMRST# RSMRST#
H_CPUPWRGD PROCPWRGD
H_VCCST_PWRGD DCCST_PWRGD
SYS_PWROK
PM_PCH_PWROK PCH_PWROK
PCH_DPWROK DSW_PWROK
ME_SUS_PWR_ACK_R GPP_A13/SUSWARN#/SUSPWRDNACK
SUSACK# R GPP_A15/SUSACK#
PCH_WAKE# GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD#AT15
SKYLAKE_ULP

GPP_B12/SLP_S0# SIO_SLP_S0#
GPD4/SLP_S3# SIO_SLP_S3#
GPD5/SLP_S4# SIO_SLP_S4#
GPD10/SLP_S5# SIO_SLP_S5#
SLP_SUS# SIO_SLP_SUS#
SLP_LAN# SLP_LAN#
GPD9/SLP_WLAN# GPD9/SLP_WLAN#
GPD6/SLP_A# SIO_SLP_A#
GPD3/PWRBTN# SIO_PWRBTN#
GPD1/ACPRESENT AC_PRESENT
GPD0/BATLOW# PCH_BATLOW#
GPP_A11/PME# PME#
INTRUDER# SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# EXT_PWR_GATE#
GPP_B2/VRALERT# GPP_B2/VRALERT#

SIO_SLP_S3# TP1701
TP1709 SIO_SLP_S3# 24,40,51,52,54
TP1703 SIO_SLP_S4# 24,40,51
TP1710
TP1704
TP1705
TP1706
SIO_PWRBTN# 24
AC_PRESENT 24
TP1707
TP1708

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

3D3V_S5
R1731 20KR2J-L2-GP EXT_PWR_GATE# 2

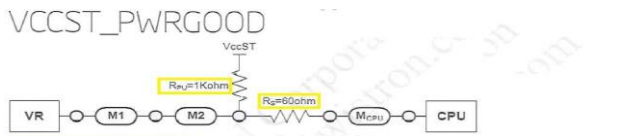
BATLOW#:
Pull-up required even if not implemented.

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

071.SKYLA.000U CPU BOM CTRL

3D3V_S5
C1702 SCD1U16V2KX-3GP
+VCCST_CPU
Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
U1701 74LVC1G07GW-GP 73.01G07.0HG
24,40 ALL_SYS_PWRGD
R1722 1KR2J-1-GP
H_VCCST_PWRGD_R
EC1708 SCD1U16V2KX-3GP
R1718 100KR2F-L1-GP
R1719 47KR2F-GP
EC1709 SCD1U16V2KX-3GP

VCCST_PWRGD / HWM201:



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

XDP_DBRESET#
SYS_PWROK
PLT_RST#
PCH_PWROK
EC1706 EC1702 EC1703 EC1705 SC1KP50V2KX-1GP
ED1702 PESD5V0U1BL-GP-U1

DY
R1708 ME_SUS_PWR_ACK_R SUSACK# R
3D3V_AUX_KBC
R1727 100KR2J-1-GP
R1726 10KR2J-3-GP
Q1701 2N7002KDW-GP
3V_5V_POK#
PM_RSMRST# 1KR2J-1-GP R1702
3V_5V_POK_C R1728 0R0402-PAD
PCH_RSMRST# 24
3V_5V_POK 45,54
EC1711 EC1712 SCD1U16V2KX-3GP
84.2N702.A3F
2nd = 075.063D1.007C

<Core Design>
Wistron Corporation
2F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU_(POWER MANAGEMENT)
Size: A2 Document Number: LV115 SKL-U
Date: Monday, April 25, 2016 Sheet 17

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SMLALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PLACE WITHIN 1.1 INCH OF PCH

(#5430316)Optional, can be left as OPEN/No-Connect.

add Circuit for NFC

Memory Down Strap

0=L,1=H

RAMID	MD_ID3	MD_ID2	MD_ID1	MD_ID0	LENOVO PN	VENDOR PN	WISTRON PN	VENDOR	Density
0	0	0	0	0				SAMSUNG	1GB
1	0	0	0	1				MICRON	1GB
2	0	0	1	0				HYNIX	1GB
3	0	0	1	1				SAMSUNG	2GB
4	0	1	0	0				MICRON	2GB
5	0	1	0	1				HYNIX	2GB
6	0	1	1	0	SM30K11219	K4A8G165WB-BCPB	072.48165.0000	SAMSUNG	4GB
7	0	1	1	1	SM30K59902	MT40A512M16HA-083E:A	072.40512.0A00	MICRON	4GB
8	1	0	0	0	SM30K59899	H5AN8G6NAFR-VFC	N/A	HYNIX	4GB
9	1	0	0	1					
10	1	0	1	0					
11	1	0	1	1					
12	1	1	0	0					
13	1	1	0	1					
14	1	1	1	0					
15	1	1	1	1					

Check Clock Mapping

GPU

WLAN

LAN

071.SKYLA..000U

CPU BOM CTRL

84.2N702.A3F

2nd=075.06301.007C

82.30004.841

82.30001.G11

84.2N702.J31

2ND=84.2N702.031

3rd=84.2N702.W31

Layout: Place at the open door area.

Wistron Corporation

CPU_(LPC/SPI/SMBUS/CL/CLK)

LV115 SKL-U

-1

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	* 0 = Port C is not detected. 1 = Port C is detected.

These two signals have weak internal pull-down.

PCH strap pin:

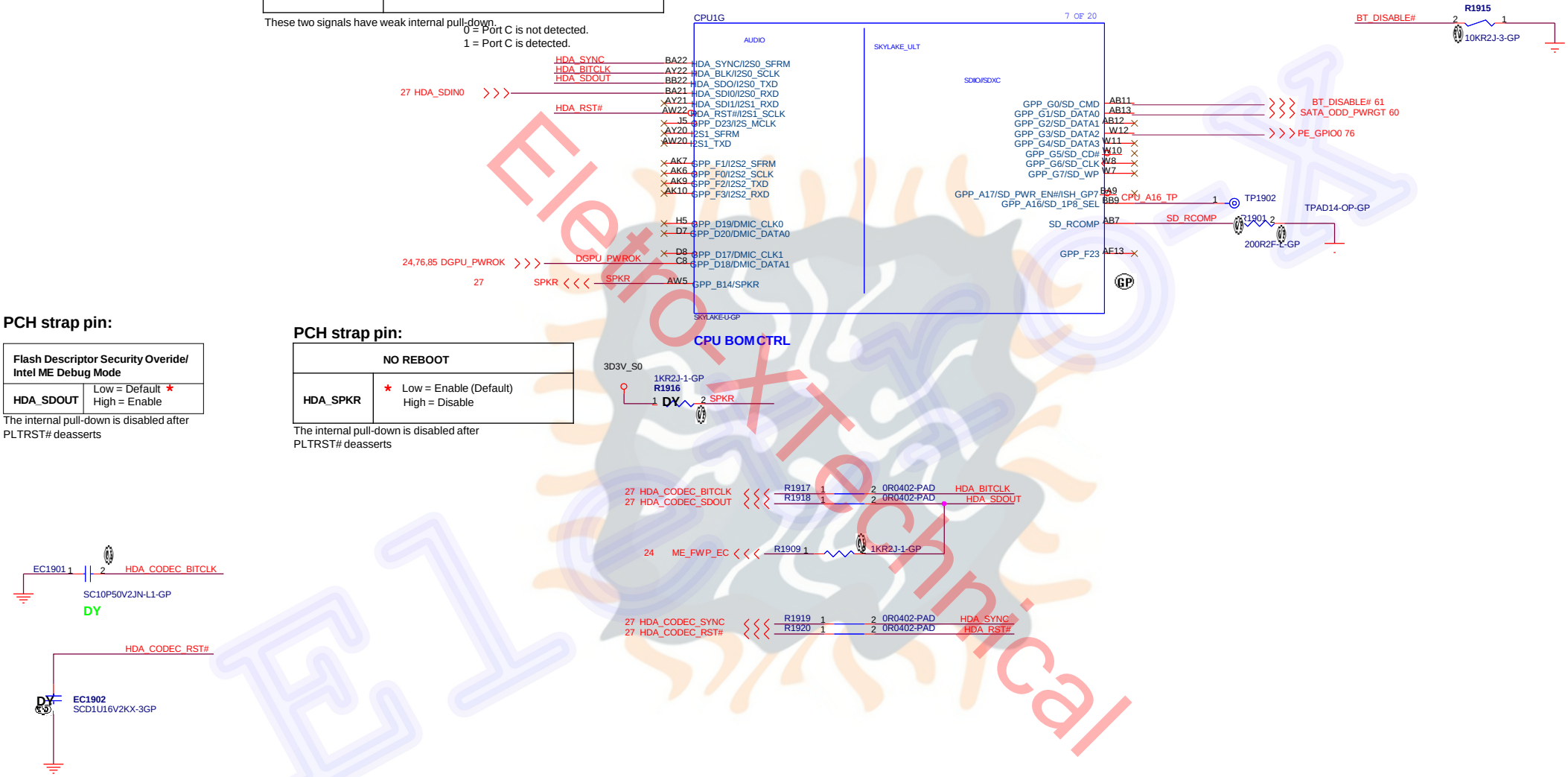
Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AUDIO/SDIO/SDXC)

Size: A3 | Document Number: LV115 SKL-U | Rev: 1

Date: Monday, April 25, 2016 | Sheet 19 of

Main Func = PCH

20151013 Change VIDEO_THERM_ALERT# PIN to GPP_B20

20151013 ADD R2041 to Connect DGPU_PWR_EN and PE_GPIO1

PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination ★	Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

CPU1F — LPSS / SKYLAKE_ULT / ISH — 6 OF 20

071.SKYLA.000U

CPU BOM CTRL

PCH Prim

UMA / PX

ON BOARD RAM STUFF / ON BOARD RAM DY

DIMM SKT STUFF / DIMM SKT DY

CPU_28W / CPU_15W

<Core Design>

Wistron Corporation

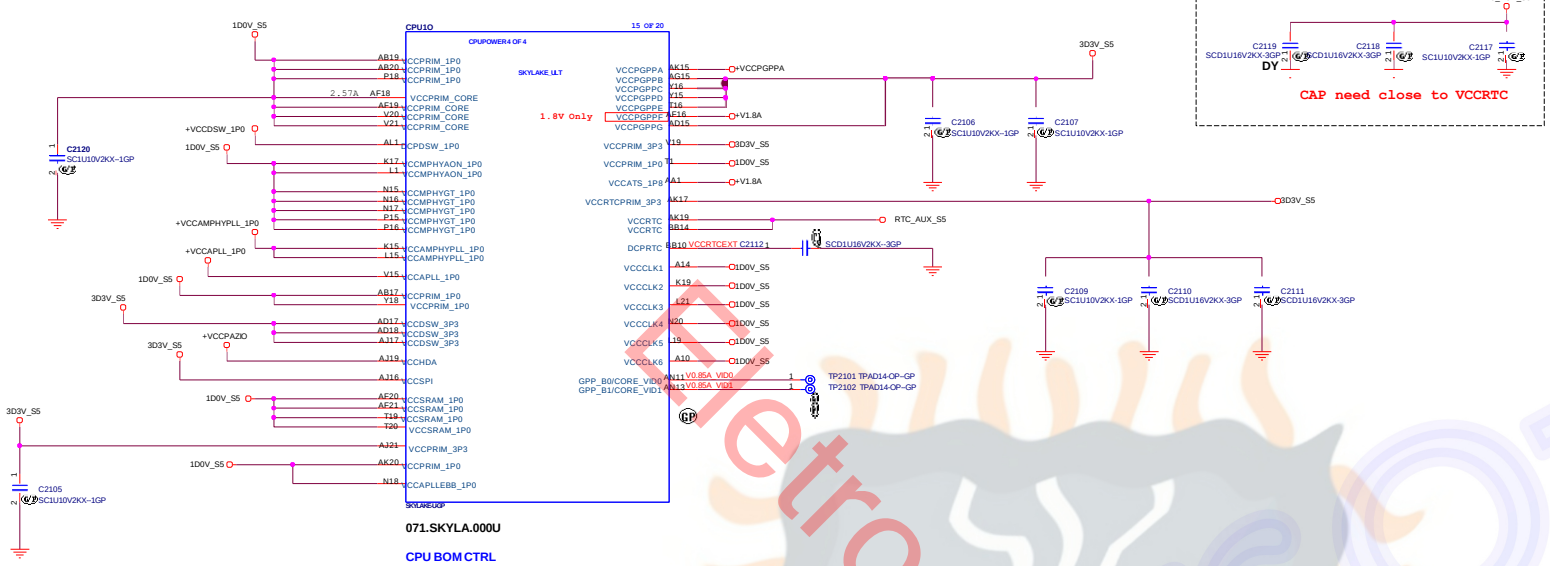
2F., 88, Sec. 1, HsinTai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

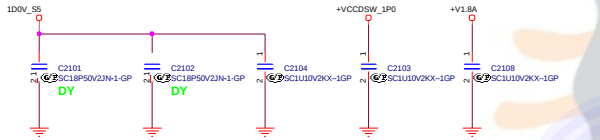
Title: CPU (LPSS/ISH)

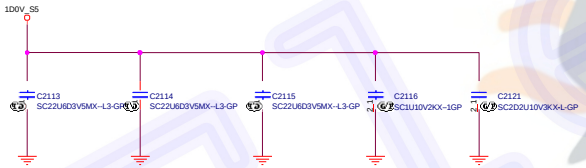
Size: A2 | Document Number: LV115 SKL-U | Rev: 1.0

Date: Monday, April 25, 2016 | Sheet: 20

Main Func = PCH







Wistron Corporation
2F, 88, Sec.1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A2 | Document Number: LV115 SKL-U | Rev: 1.0

Date: Monday, April 25, 2016 | Sheet 21

Main Func = PCH

CPU1T 20 OF 20

SKYLAKE_ULT

SPARE

AW69	RSVD#AW69	RSVD#F6	F6
AW68	RSVD#AW68	RSVD#E3	E3
AU56	RSVD#AU56	RSVD#C11	C11
AW48	RSVD#AW48	RSVD#B11	B11
C7	RSVD#C7	RSVD#A11	A11
U12	RSVD#U12	RSVD#D12	D12
U11	RSVD#U11	RSVD#C12	C12
H11	RSVD#H11	RSVD#F52	F52

GP

SKYLAKE-U-GP

071.SKYLA.000U

CPU BOM CTRL

<Core Design>

緯創資通 **Wistron Corporation**

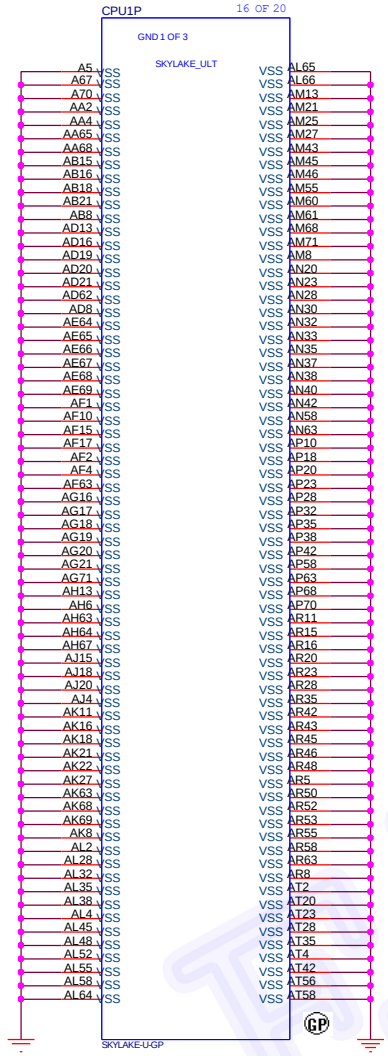
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(RSVD)***

Size	Document Number	Rev
A4	**LV115 SKL-U**	-1

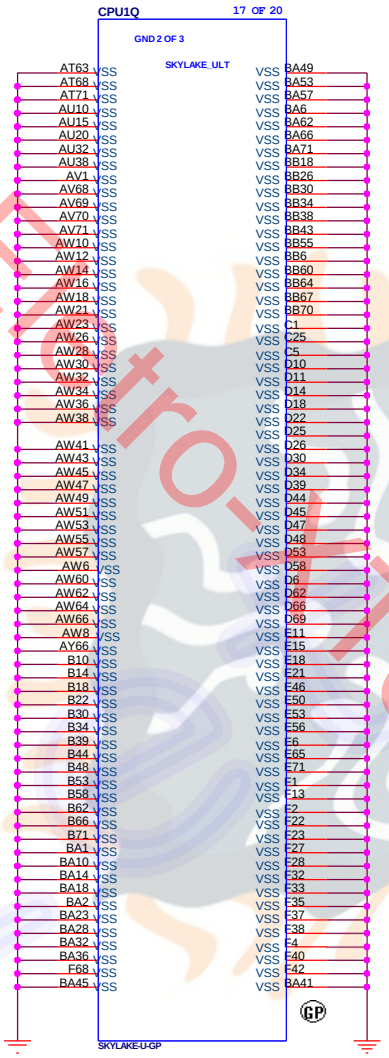
Date: Monday, April 25, 2016 Sheet 22 of 102

Main Func = PCH



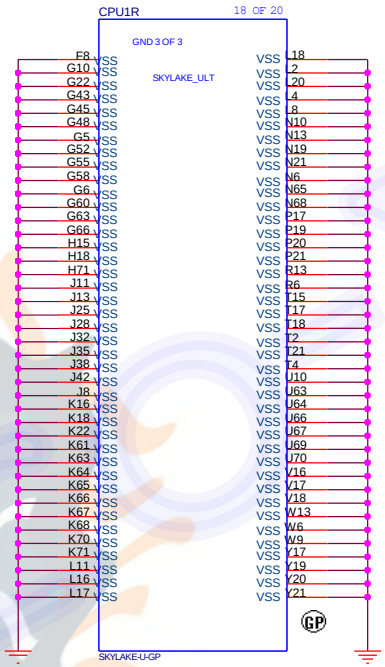
071.SKYLA.000U

CPU BOM CTRL



071.SKYLA.000U

CPU BOM CTRL



071.SKYLA.000U

CPU BOM CTRL

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(VSS)	
Size A3	Document Number LV115 SKL-U	Rev 1
Date: Monday, April 25, 2016	Sheet 23 of 60	

SSID = KBC

Model_ID_BOM Ctrl

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LV115 Intel skylake	100.0K	10.0K 64.10025.6DL	3.0V
LV114 Intel skylake	100.0K	20.0K 64.20025.1.DL	2.75V
N A	4% 0 K	33.0K ex 3 025.1.DL	2.48V
NA	100.0K	47.5K 64.4/025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
SE	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

SPEC: ADT PWR Detection Function V1 3

DELTA Model:ADP65FD BB-PD03 ADP

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.100V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

SA

Prevent BIOS data loss solution

84.T3906.A11
1ST = 84.T3906.A11
2nd = 84.T3906.E11
74.03809.07B

NPCE285G

Thermal VD

BATTERY / CHARGER ---->

TP----> 65

20150724 Need check DGPUHOT

Modified 20151007
Delete D53 Relative Components

06/16 MAX R1717 DY

Reserved AOAC

071.00285.0A0G

6/18 U2403 Change Part Number to 71.00285.0A0G (285P)

KBC PWR supply at PSL mode.

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

2013/9/12
GPIO83/SOUT_CR & GPIO87/SIN_CR
Need reserved TP for Debug

R2472 close to Pin103

NOTE: Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE: PWM Signal: 1.If unused, select alternative GPIO function and enable internal pull-down. 2.Please measure and make sure that the rise time of VCC_POR is less than 10us.

NOTE: Please be aware that the SPI interface trace length between PCH and EC should not exceed 6500mils. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE: Locate resistors R2415 and R2417 close to the U2401.

<----06/26 LY41 USB_CHAR_SEL

<----06/24 AOU_IFLG#

<----08/19 AD_OFF

Viber Del TPM

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) : 3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC) :		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC) :		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.02130.031
2nd = 84.00102.031
84.2N702.331
2ND = 84.2N702.031
3rd = 84.2N702.W31

EC_GPIO47 High Active
84.2N702.331
2ND = 84.2N702.031
3rd =84.2N702.W31

EC GPIO PH

EC GPIO PL

(Debug Card Side) (Main Board Side)

3.3V_S5

KBC

LF15V Note:
(1) R21= DY R2458(ES1_TXD)
(2) R13= DY R2451(ES1_RXD)

Nuvoton KBC PSL Logic

KBB_DEFINE1_R use MODEL_ID to Define Lenovo Key:
LV115: "Fast Forward" Key
LV114: "Delete" Key

Table 11. PSL Operation States

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

Micrel P/N: 74.02782.072

Wistron Corporation

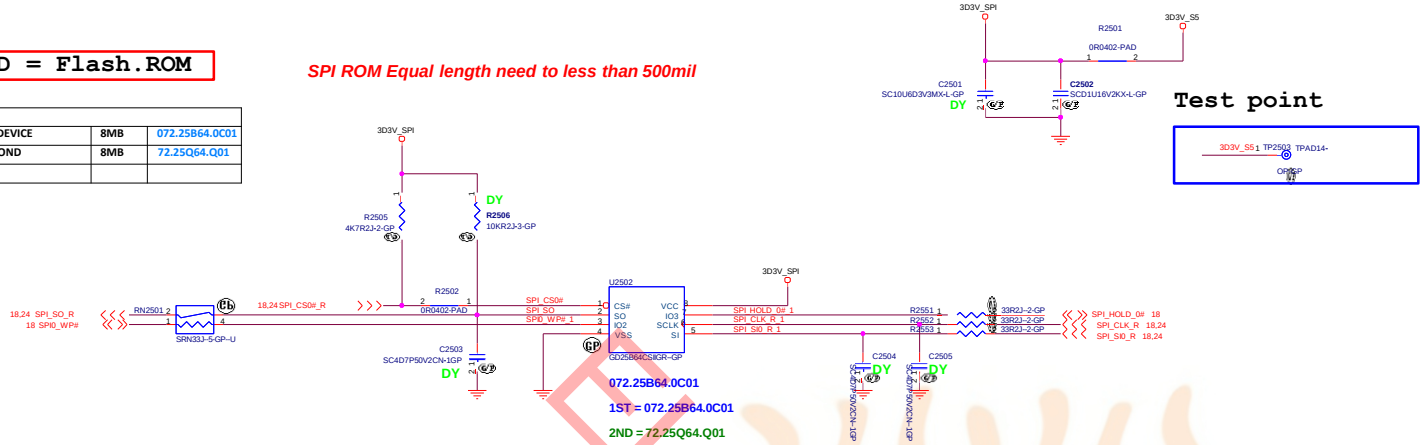
NPCE285

LV115 SKL

SSID = Flash.ROM

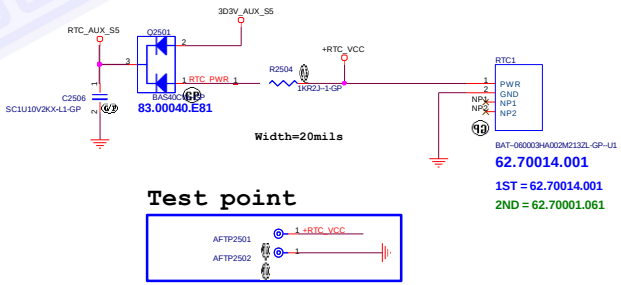
SPI ROM Equal length need to less than 500mil

U2502			
1ST	GIGA DEVICE	8MB	072.25B64.0C01
2ND	WINBOND	8MB	72.25Q64.Q01
3RD			

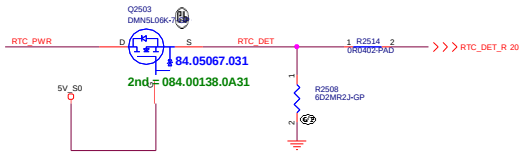


SSID = RBATT

SSID = RBATT

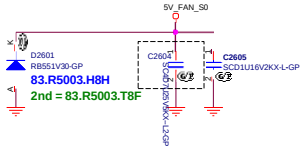


High Detect
Need to Check whether to PD in PCH Side



Main Func = Thermal Sensor

Layout 15 mil

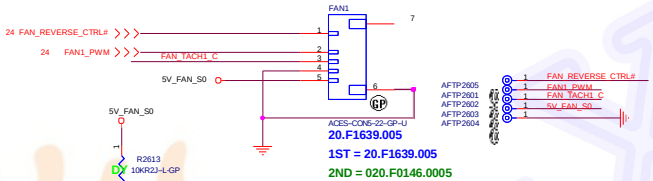


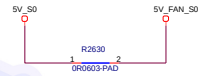
07/31 C2604 Change part number 78.47523.5BL to 78.47522.L4L, 4.7uF, 0805, 25V

ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

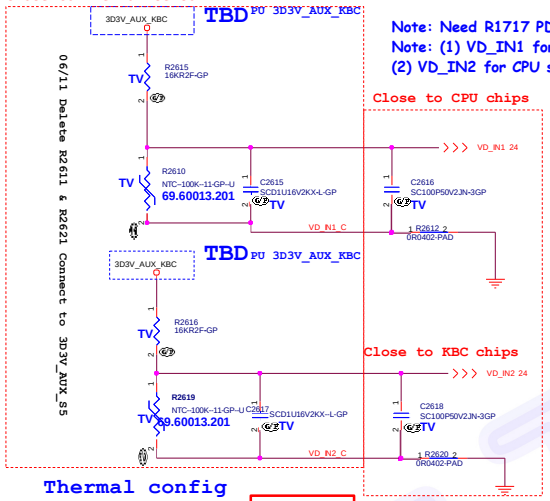
T_CRIT temperature strapping point





2.System Sensor, Put on palm rest

Close to Thermal sensor

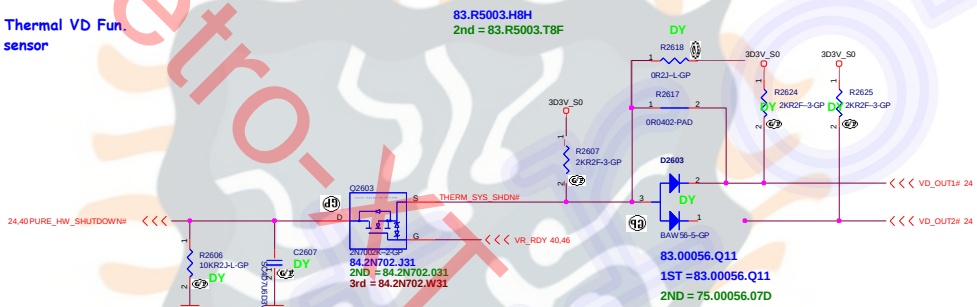


Close to CPU chips

Close to KBC chips

Note: Need R1717 PD: Enable Thermal VD Fun.
Note: (1) VD_IN1 for System sensor
(2) VD_IN2 for CPU sensor

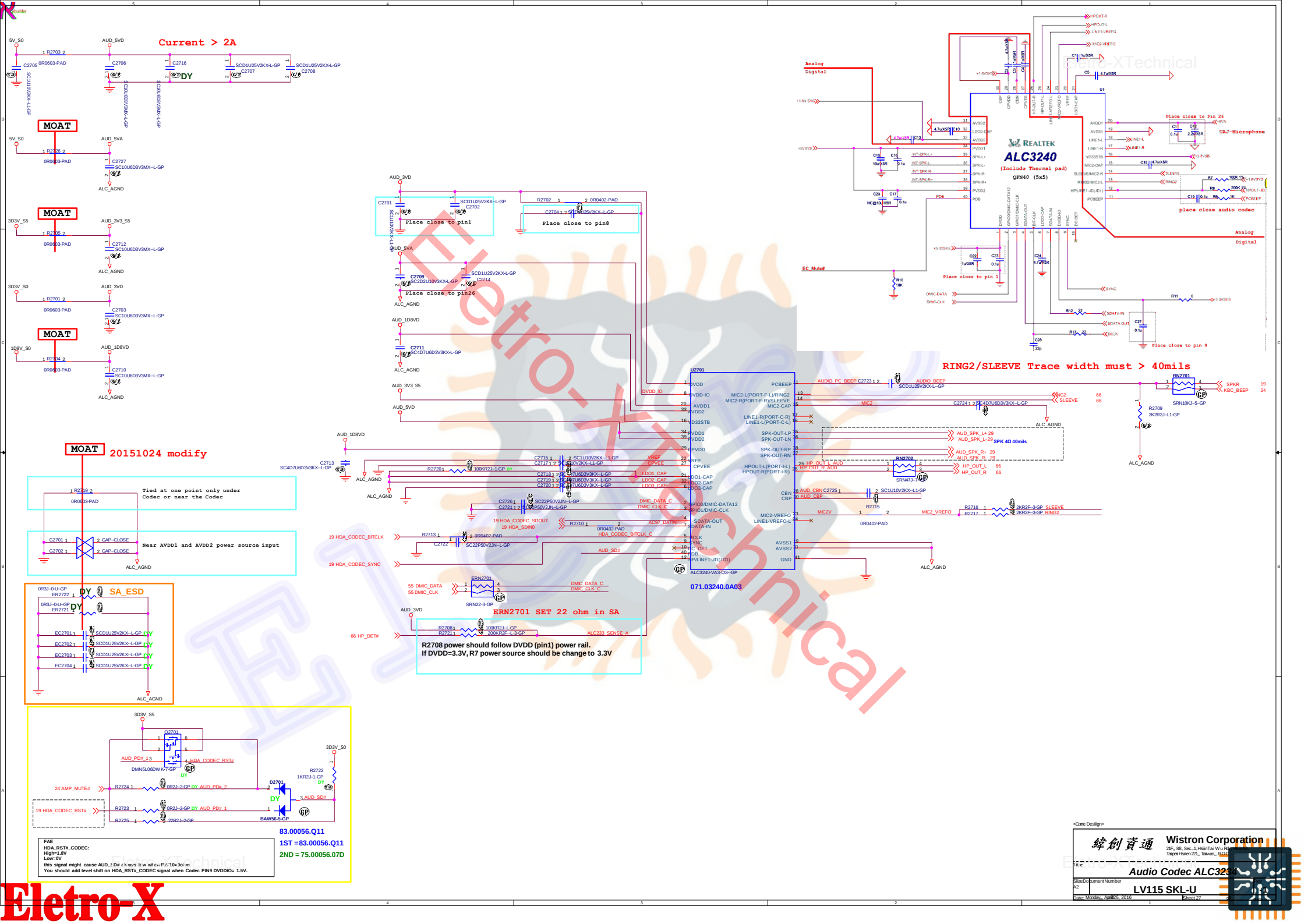
T8=85 degree



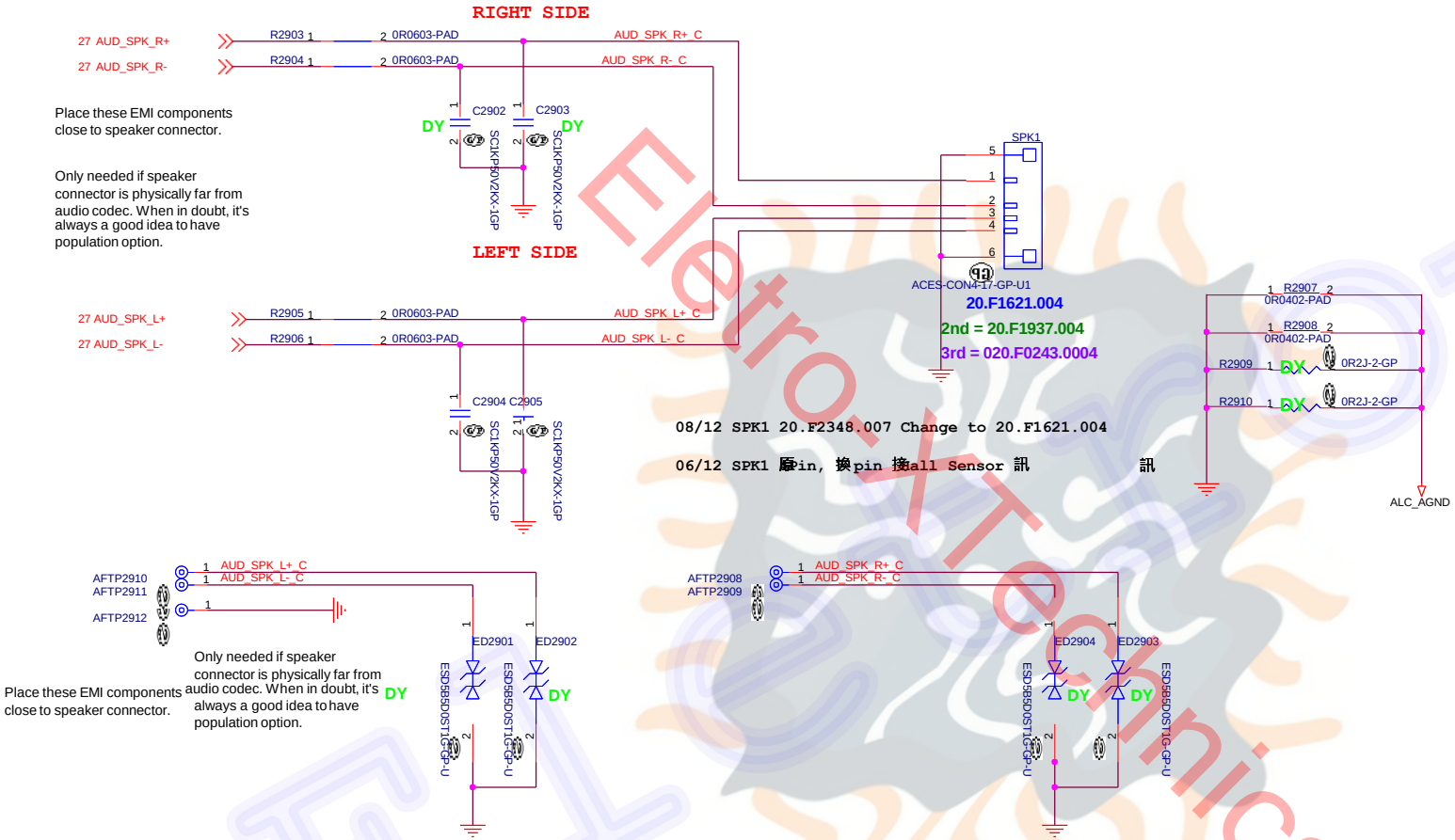
Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
R1717	ASM	DY

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.
Title
THERMAL NCT7718W/Fa
Size A2
Document Number
LV115 SKL-U
Date: Monday, April 25, 2016
Sheet 28


Current > 2A
MOAT
MOAT
MOAT
MOAT
MOAT 20151024 modify
Tied at one point only under Codec or near the Codec
Near AVDD1 and AVDD2 power source input
SA_ESD
Place close to pin1
Place close to pin8
Place close to pin26
Place close to pin 1
Place close to pin 9
Place close to Pin 26
UAJ-Microphone
place close audio codec
Analog
Digital
REALTEK
ALC3240
(Include Thermal pad)
QFN40 (5x5)
RING2/SLEEVE Trace width must > 40mils
SPK 4Ω 40mils
071.03240.0A03
ERN2701 SET 22 ohm in SA
R2708 power should follow DVDD (pin1) power rail.
If DVDD=3.3V, R7 power source should be change to 3.3V
83.00056.Q11
1ST =83.00056.Q11
2ND = 75.00056.07D
FAE
HDA_RST#_CODEC:
High=1.8V
Low=0V
this signal might cause AUD_SDI# always low when P2.10=3.3V
You should add level shift on HDA_RST#_CODEC signal when Codec PIN9 DVDDIO= 1.5V.
Wistron Corporation
Audio Codec ALC3234
LV115 SKL-U
Eletro-X

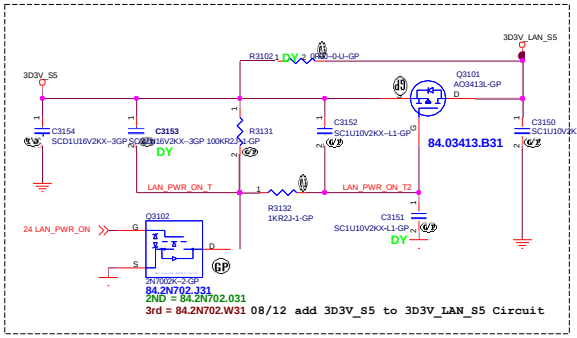
INTERNAL STEREO SPEAKERS

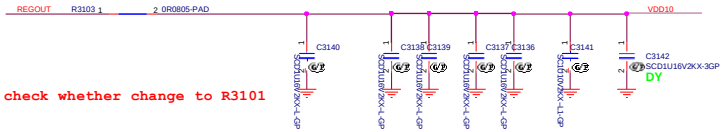


<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio IC	
Size A3	Document Number LV115 SKL-U	Rev 1
Date: Monday, April 25, 2016	Sheet 29	of 60





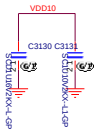
Need check whether change to R3101

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3138 to C3141 close to each VDD10 pin-- 3, 8, 22, 30

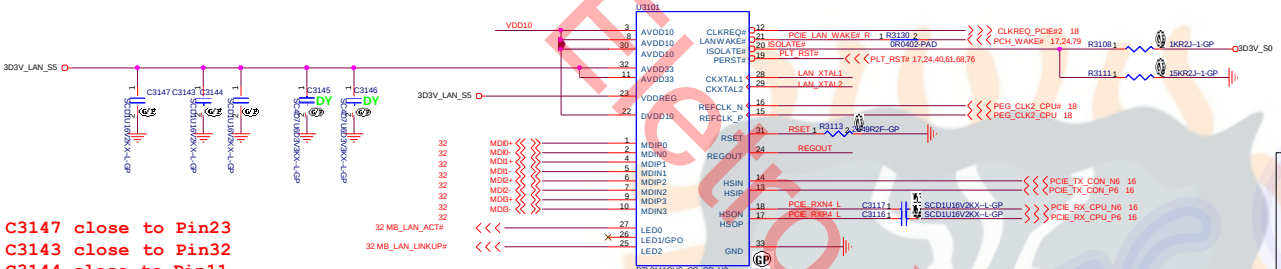
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)

C3138 close to Pin3 , C3139 close to Pin8
C3140 close to Pin30,C3136 close to Pin22

For RTL8111G(S) Series/ RTL8111GUS Series/ RTL8111H(S) Series/ RTL8106EUS Series/ RTL8107E(S) Series/ RTL8118AS Series
C3132,C3133 close to Pin22



For RTL8106E Series
C3130,C3131 close to Pin30



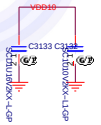
C3147 close to Pin23
C3143 close to Pin32
C3144 close to Pin11

71.08111.W03

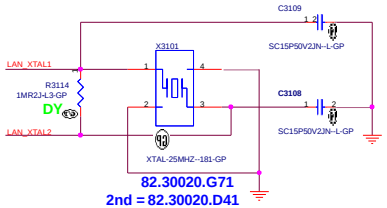
BOM CHANGE TO RTL8111H:SC50H01259

LAN_BOM_CTRL

For RTL8111G(S) Series/ RTL8111GUS Series/ RTL8111H(S) Series/ RTL8106EUS Series/ RTL8107E(S) Series/ RTL8118AS Series
C3132,C3133 close to Pin22



25MHz XTAL



Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

LAN and Transformer Config:

LAN/Transformer	

<Core Design>

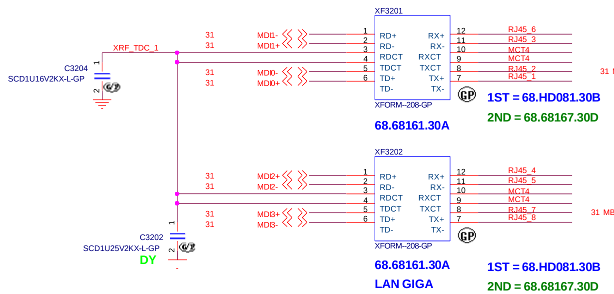
Wistron Corporation
21F., 88, Sec. 1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111

Size: A2 | Document Number: LV115 SKL-U

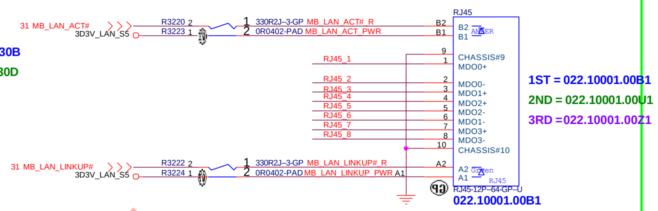
Date: Monday, April 25, 2016 | Sheet 31

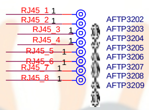
10/100M/1000M Lan Transformer



Change LAN CONN 20151007

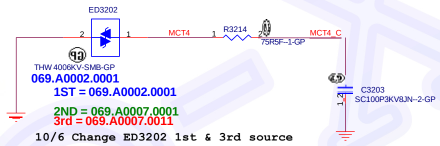
LAN Connector



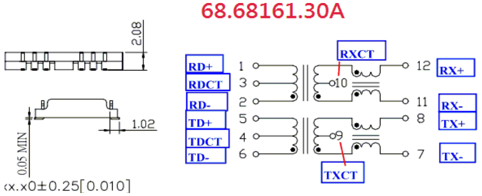


10/100/1000 LAN surge circuit

For test stuff



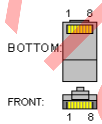
68.68161.30A



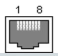
RJ45 Pin define

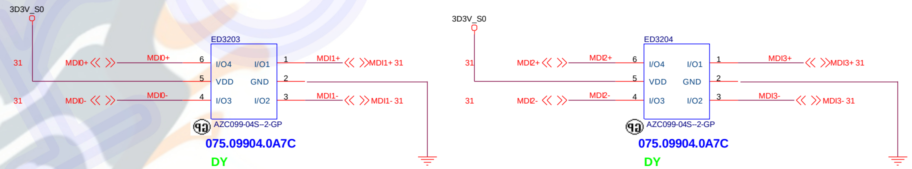
Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

The connector is 8 pin RJ45 (8P8C) male



The associated connector is 8 pin RJ45 (8P8C) female





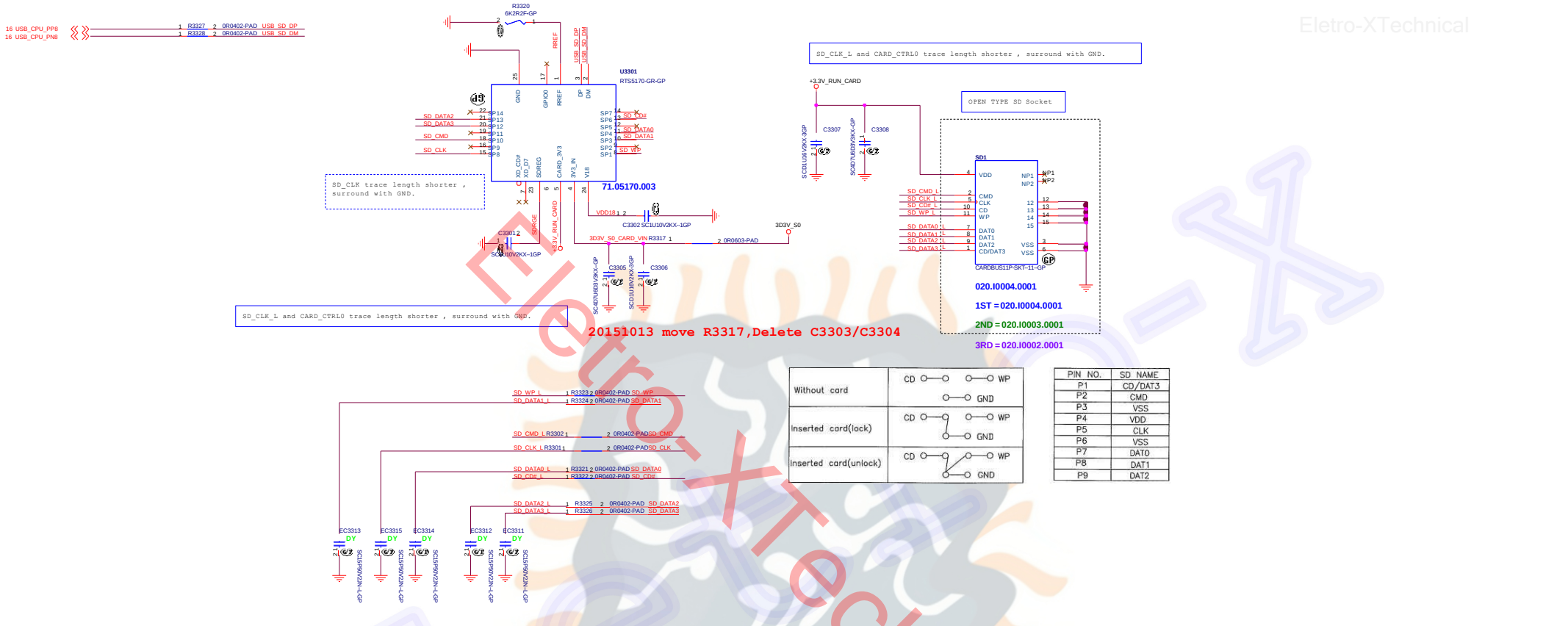
8/25 將ED3203,ED3204 改ESD STUFF OPTION 改, Wake on Lan

10/13 ED3203,ED3204 改3501一樣source

10/23 第2nd Source將5.09904.07C, 更換Part number至3501,BOM別

10/23 ED3203, ED3204 ESD STUFF OPTION改DY,丟

Card Reader RTS5170



PIN_NO.	SD_NAME
P1	CD/DAT3
P2	CMD
P3	VSS
P4	VDD
P5	CLK
P6	VSS
P7	DAT0
P8	DAT1
P9	DAT2

<Core Design>

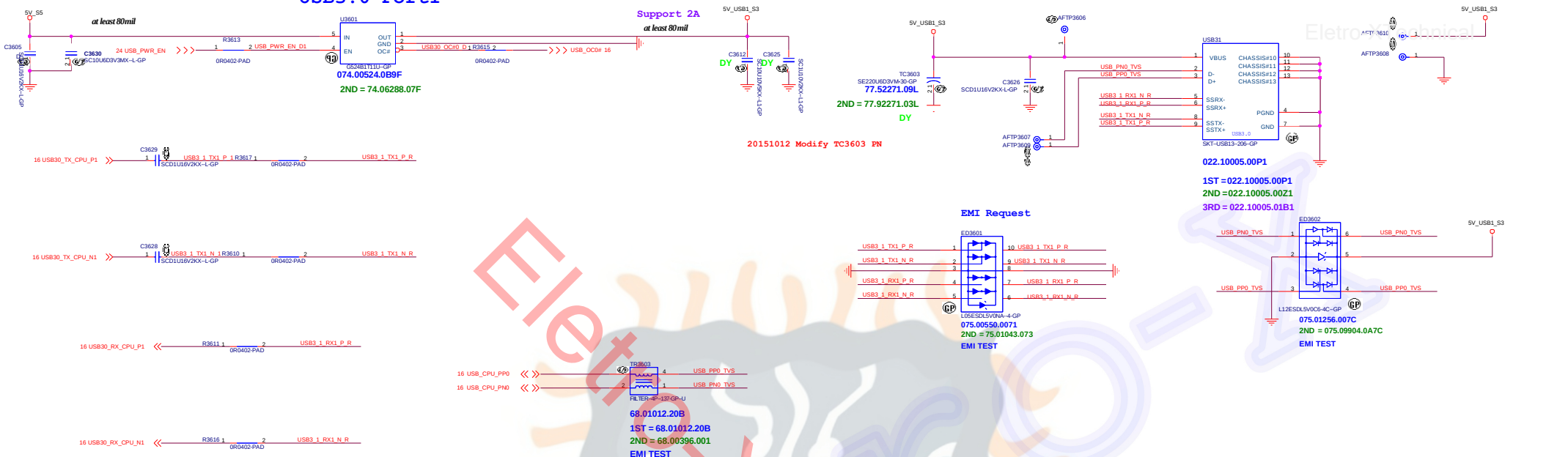
緯創資通 Wistron Corporation
2F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A2 | Document Number: LV115 SKL-U

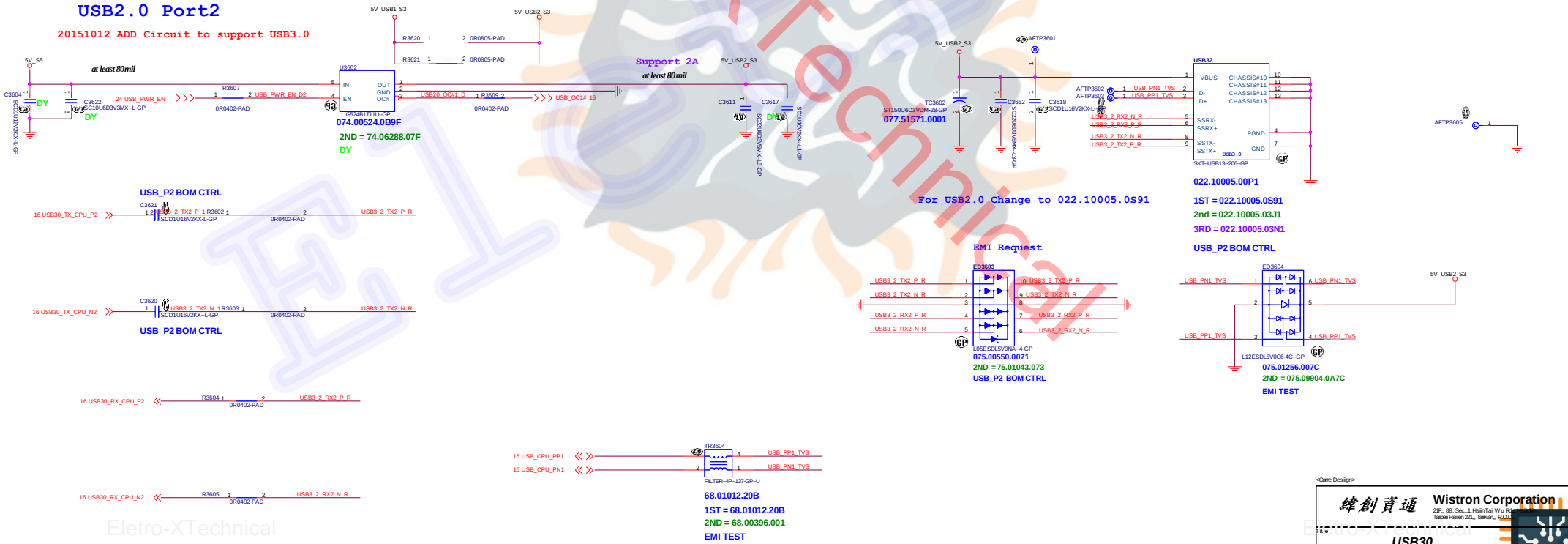
Date: Monday, April 25, 2016 | Sheet 33

USB3.0 Port1



USB2.0 Port2

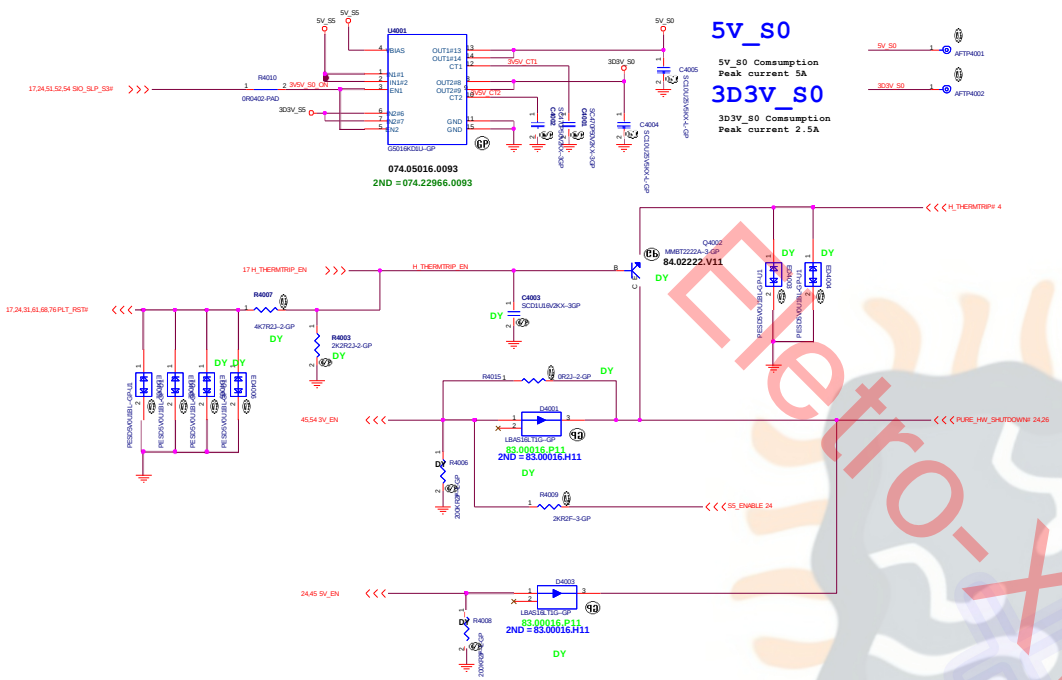
20151012 ADD Circuit to support USB3.0



<Core Design>
Wistron Corporation
USB30
LV115 SKL-U
Size: A2
Document Number
Date: Monday, April 25, 2016
Sheet 36

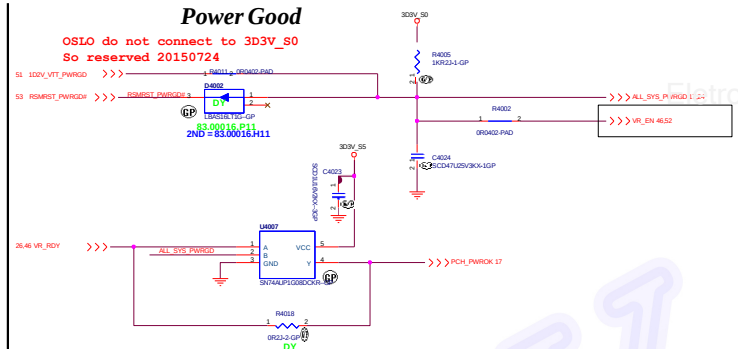
Main Func = Power Plane & Sequence

ROSA Run Power



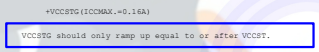
Power Good

OSLO do not connect to 3D3V_S0
So reserved 20150724



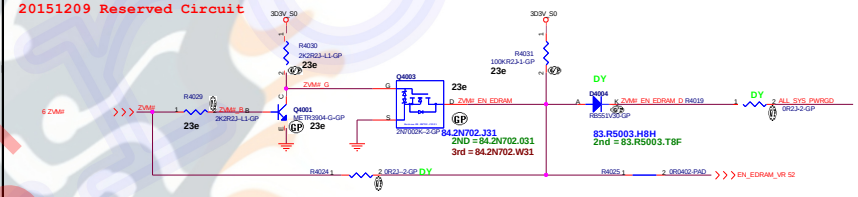
VCCSTG

20151007 Delete Reserved Circuit
Power Source Keep VCCIO (R710)

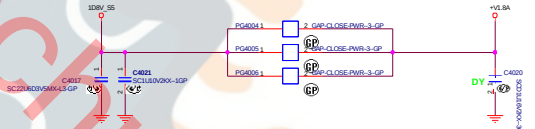


GT3 Low Power Circuit (ZVM)

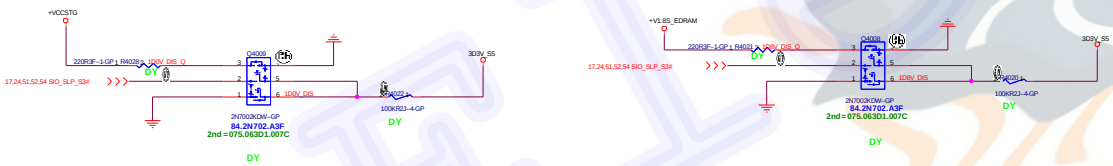
20151209 Reserved Circuit



V1.8A



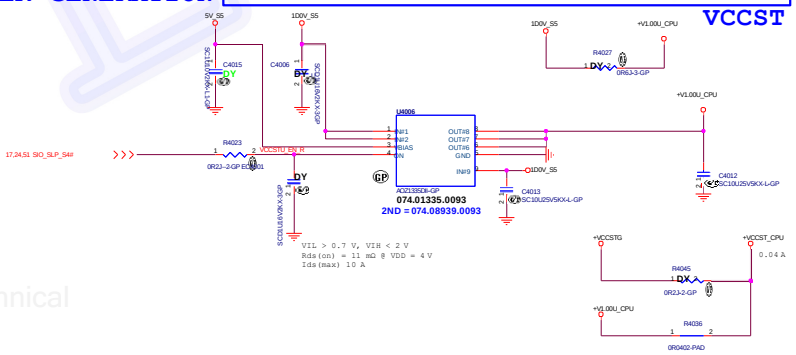
Discharge circuit



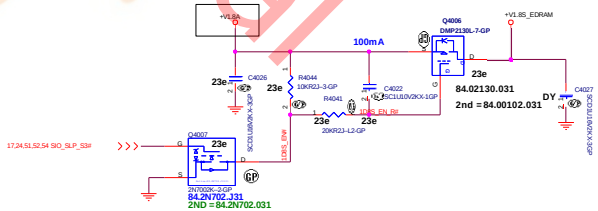
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

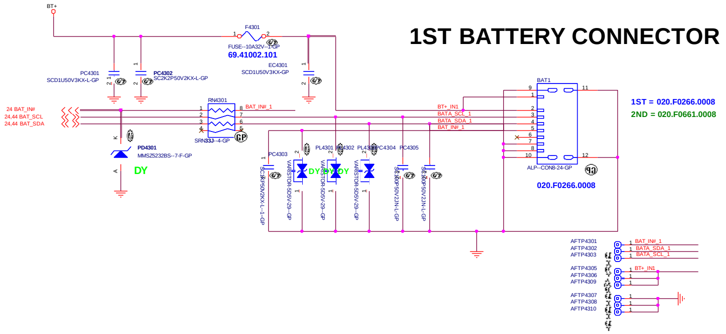
VCCST



V1.8S



1ST BATTERY CONNECTOR



Connector Pin Alignment(Vendor: Suyin,Aces)

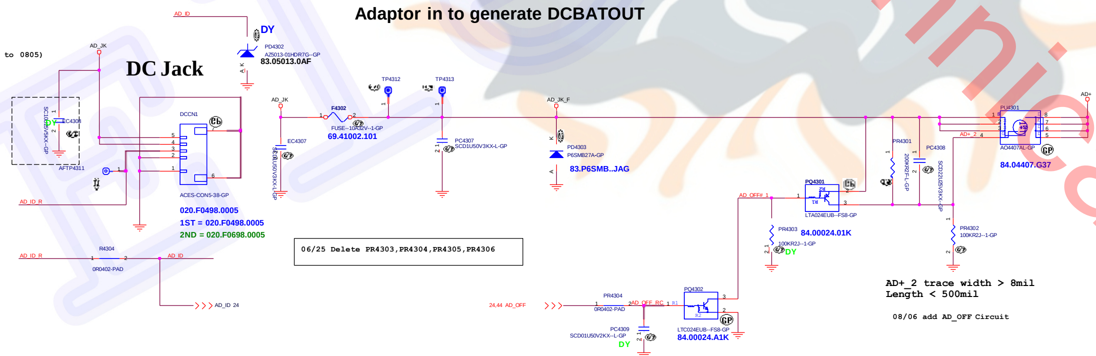
Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

Adaptor in to generate DCBATOUT

08/01 EC4308 Change part number 78.10622.L5L to 78.10622.51L(1206 to 0805)

DC Jack

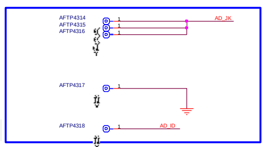


06/25 Delete PR4303,PR4304,PR4305,PR4306

AD+_2 trace width > 8mil
Length < 500mil

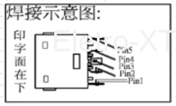
08/06 add AD_OFF Circuit

Test point



MB_Side		Cable Max. Current
Pin 1	AD_JK_F	UL10064AWG28# (3A)
Pin 2	AD_JK_F	UL10064AWG28# (3A)
Pin 3	AD_ID	UL10064AWG28# (3A)
Pin 4	GND	UL10064AWG26# (3.8A)
Pin 5	GND	UL10064AWG26# (3.8A)

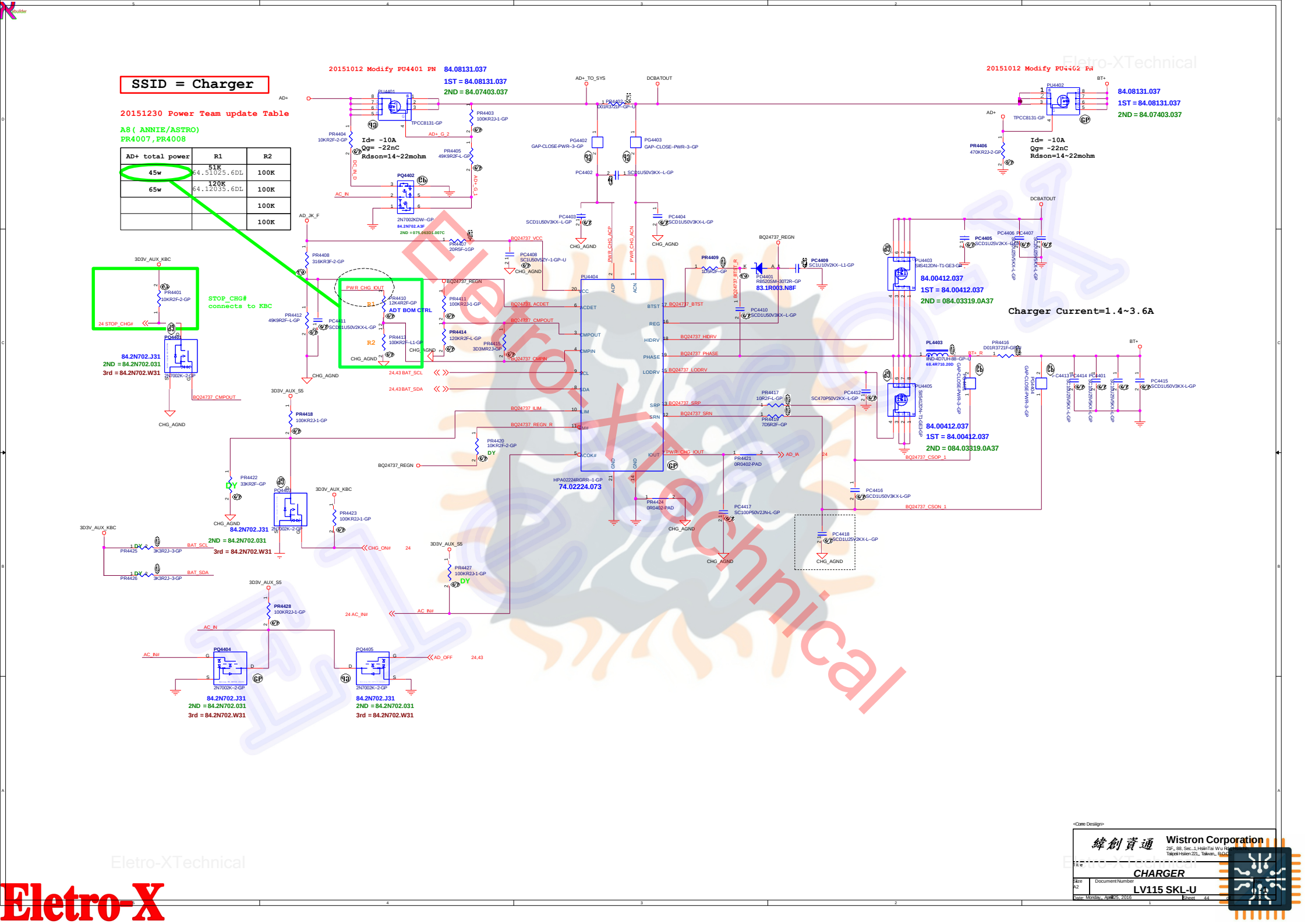
焊接示意图:



Wistron Corporation

DCIN & BATT Conn

LV115 SKL-U


SSID = Charger
20151230 Power Team update Table
A8 (ANNIE/ASTRO)
PR4007,PR4008
AD+ total power | R1 | R2
45w | 51K 64.51025.6DL | 100K
65w | 120K 64.12035.6DL | 100K
100K
100K
20151012 Modify PU4401 PN 84.08131.037
1ST = 84.08131.037
2ND = 84.07403.037
20151012 Modify PU4402 PN
84.08131.037
1ST = 84.08131.037
2ND = 84.07403.037
Id= -10A
Qg= -22nC
Rdson=14~22mohm
STOP_CHG# connects to KBC
ADT BOM CTRL
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
84.00412.037
1ST = 84.00412.037
2ND = 084.03319.0A37
Charger Current=1.4~3.6A
74.02224.073
Wistron Corporation
CHARGER
LV115 SKL-U
Size A2
Document Number
Date: Monday, April 25, 2016
Sheet 44

08/20 add 5V_EN

12/18 PR4501,PR4502 Change to Short PAD

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(止

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(止

Design Current=3.1A
OCP <6.2A

Design Current=6.4A
OCP < 12.8A

84.07410.A37
2nd = 84.01528.037

68.3R310.20V
2nd = 68.3R31A.10V

68.2R21A.20B
2nd = 68.2R21B.10J

77.52271.09L
2ND = 77.92271.03L

20151012 Modify TC4501 PN

20151012 Modify TC4503 PN

074.06575.0A43

ASM_RES_PAD_DY

ZZ.00RES.021

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

<Core Design>

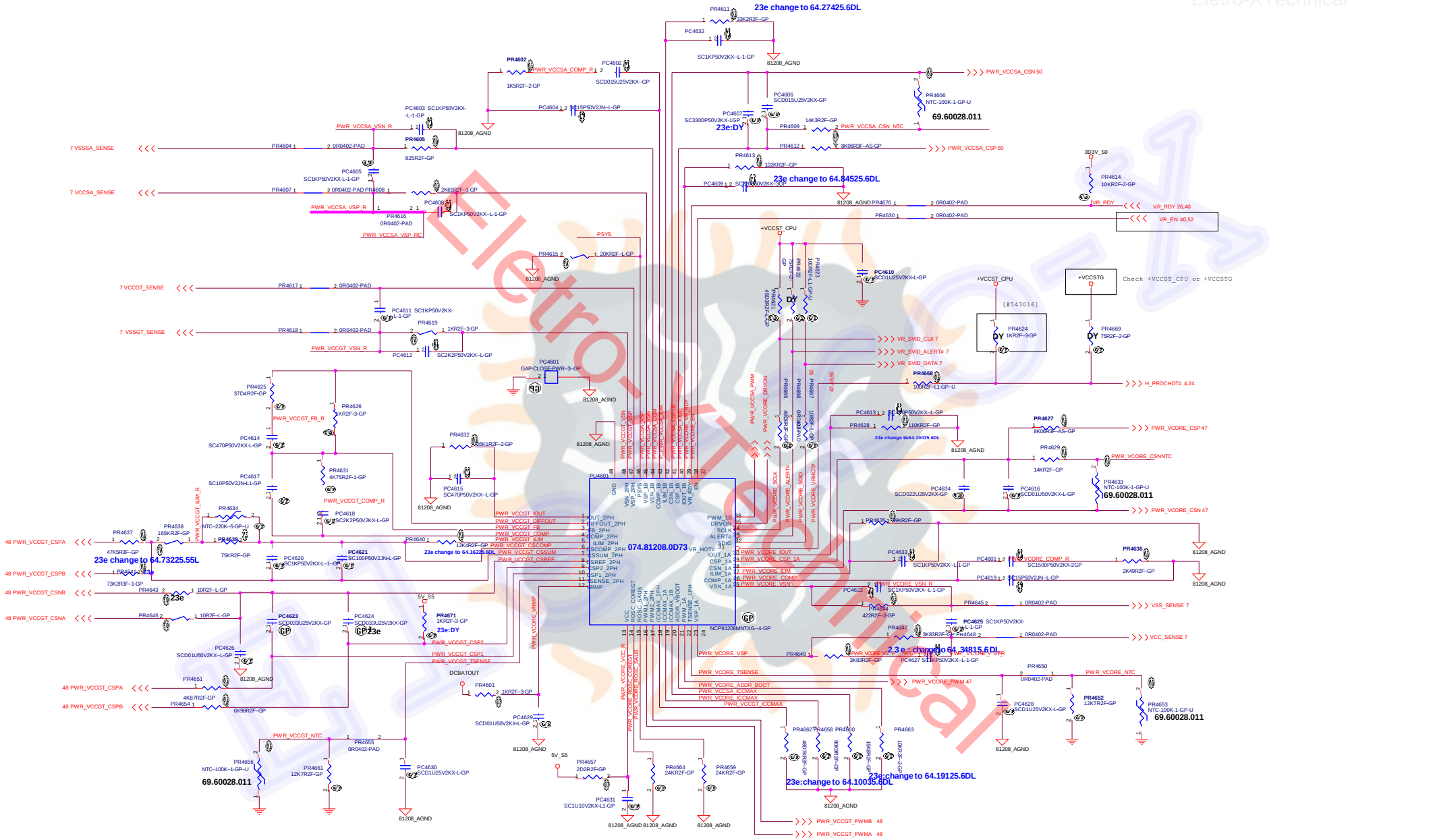
Wistron Corporation

SYN256 5V/3D3V

LV115 SKL-U

Eletro-X

Main Func = CPU_CORE



<Core Design>

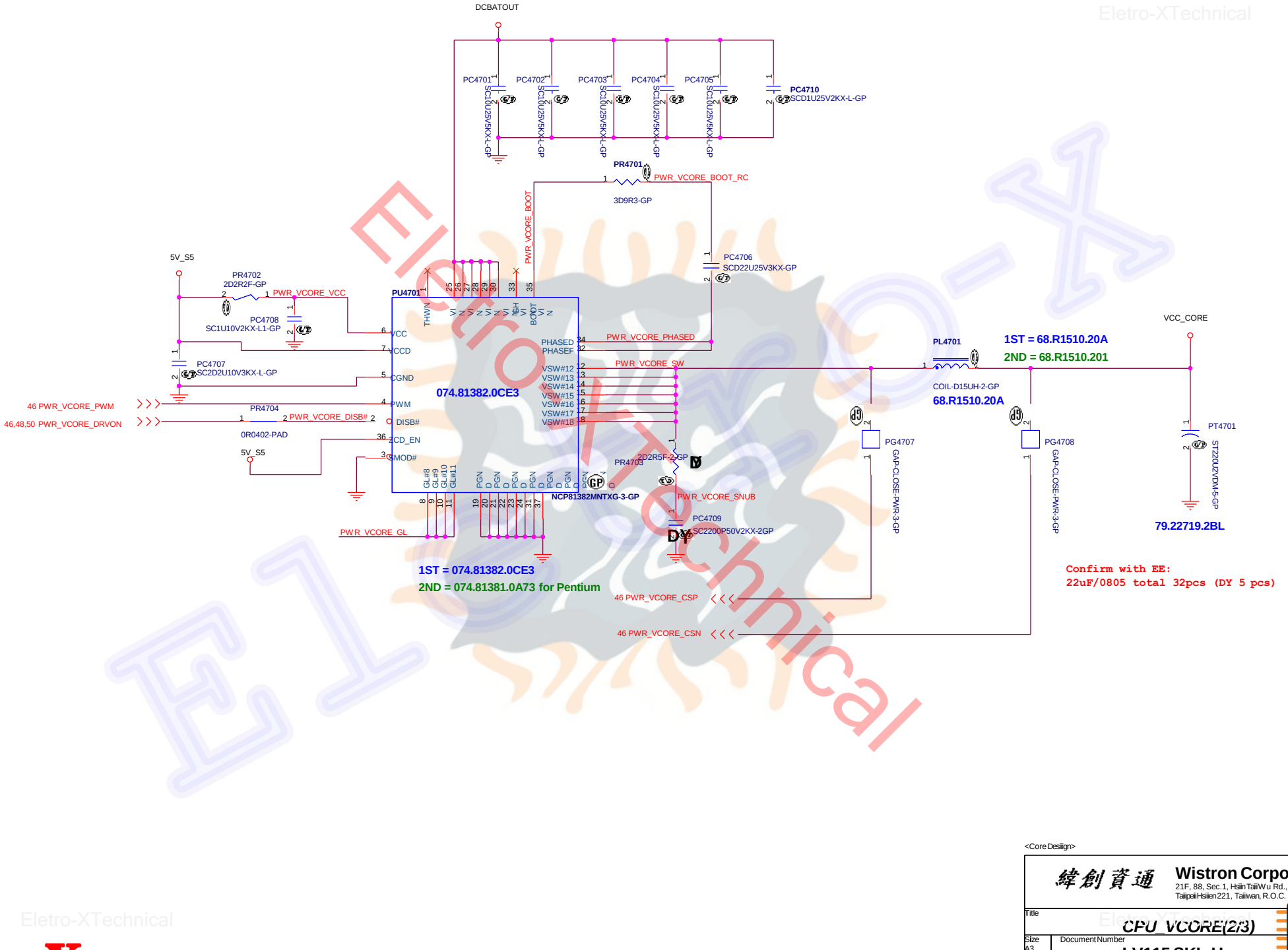
Wistron Corporation
2F., 88, Sec. 1, HsinTai Wu Rd., Hsichih
Taipei Hsien221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)

Size: A2 | Document Number: LV115 SKL-U | Rev:

Date: Monday, April 25, 2016 | Sheet 46 of

Main Func = CPU_CORE

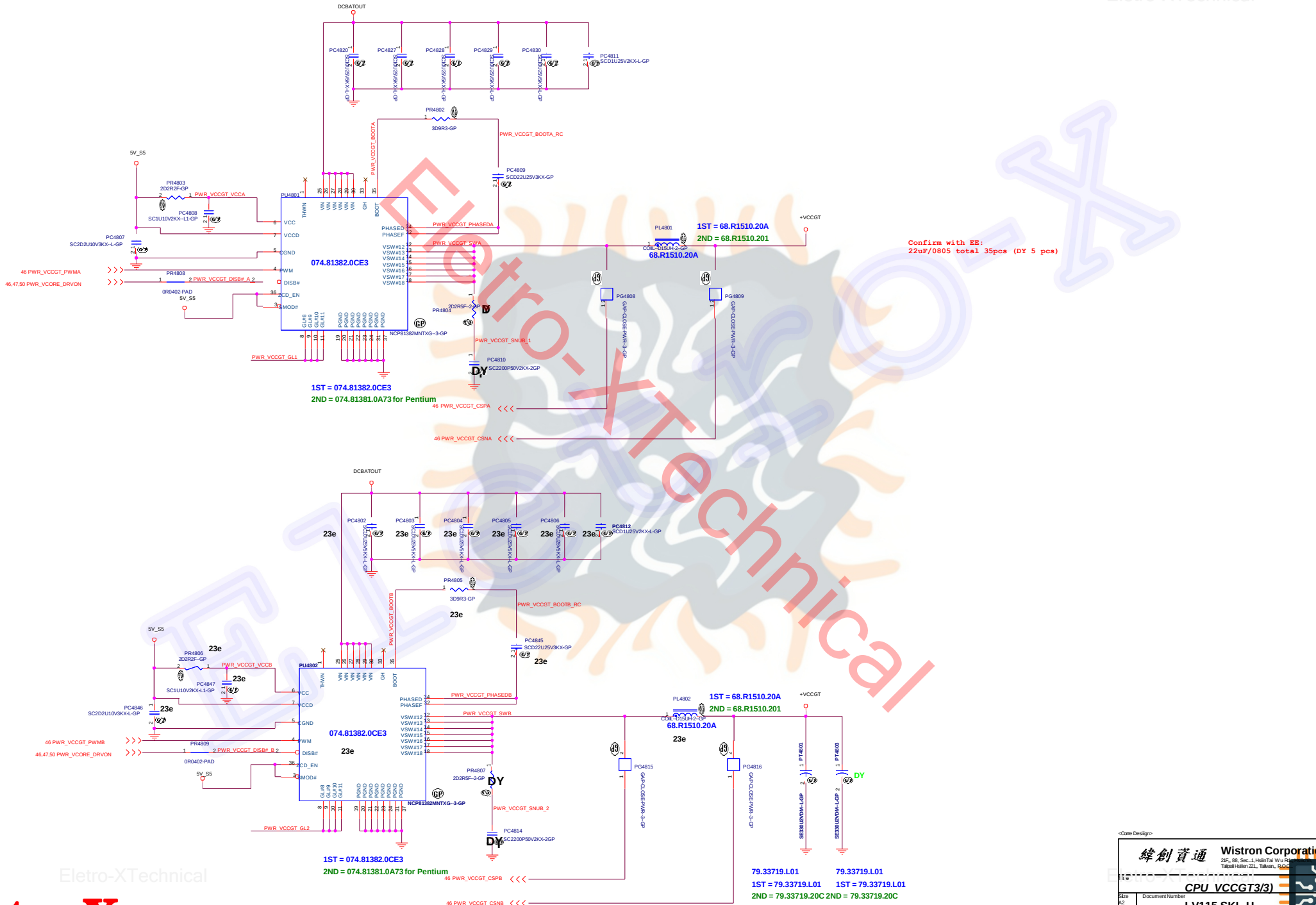


<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

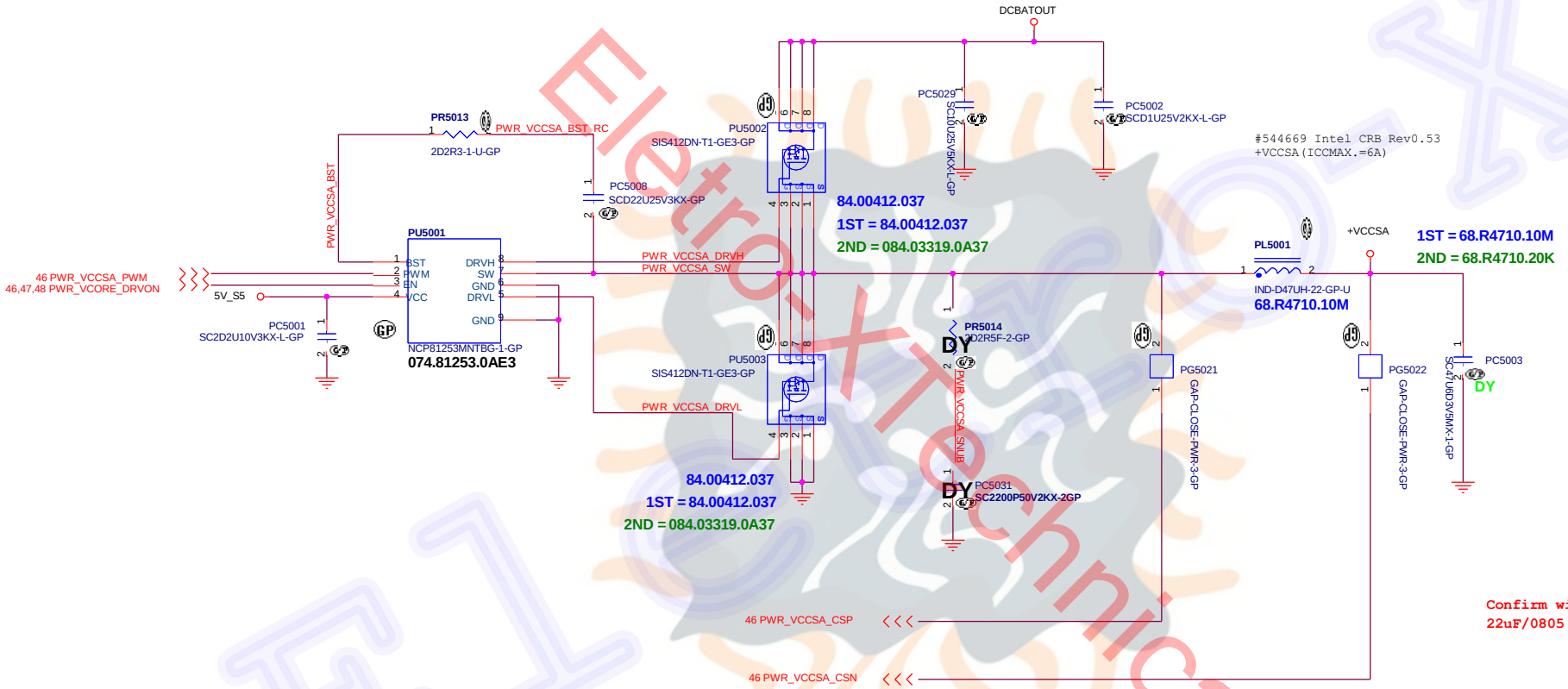
Title	CPU_VCORE(2/3)	
Size A3	Document Number LV115 SKL-U	Rev 1
Date: Monday, April 25, 2016	Sheet 47	of

Main Func = CPU_CORE



<Core Design>
Wistron Corporation
21F, 88, Sec.1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_VCCGT3/3)
Size A2
Document Number
LV115 SKL-U
Date: Monday, April 25, 2016
Sheet 48

Main Func = CPU_CORE



<Core Desiign>

緯創資通 Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiichih,
Taiipeiii-Hsiien221, Taiiwan, R.O.C.

Title	CPU_VCCSA	
Size A3	Document Number LV115 SKL-U	Rev 1
Date: Monday, Aprill25, 2016	Sheet 50	of

Main Func = VDDQ

VID
Logic-High = 0.75V
Logic-Low = 0.3V

OCP setting

Freq. setting
750K -> 350K Hz

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Vout = 0.6V
Iomax = 1.2A

RF RESERVED

Design Current :15.6A
OCP : 21.84A

Close to output cap pin1, not inside of the output cap

R1
R2
Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 15.8K / 20K)
= 1.2V

VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on

2D5V_LDO

PD = (Vin Vout) x Iout
= (3.3 - 2.5) x 0.3A = 0.24W
PD de-rating(%) = 0.24W/1.33W = 18.0%

Enable
EN_Logic-High = 1.4V
EN_Logic-Low = 0.8V

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 24.3 / 11.3K)
= 2.5204V

SY8288 For DDR4
Vout = 2.5V

Reference OSLO & LT41S 20150724

Enable

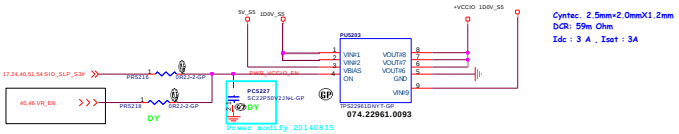
Design Current :4A
OCP : 7 A

20150604 power modify

Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.6 * (1 + 63.4K / 20K)
= 2.502 V

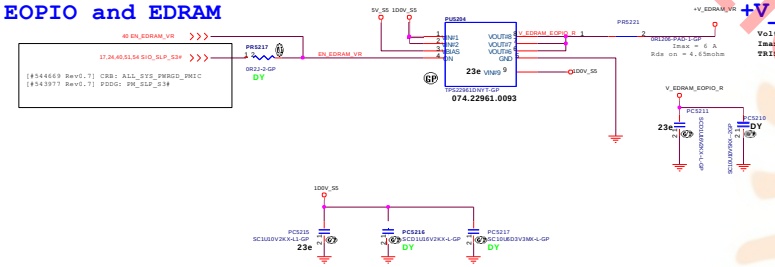
Current Limit
Low : OCP8A
Floating : OCP10A

VCCIO



Cyntec_2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A

EOPIO and EDRAM



+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

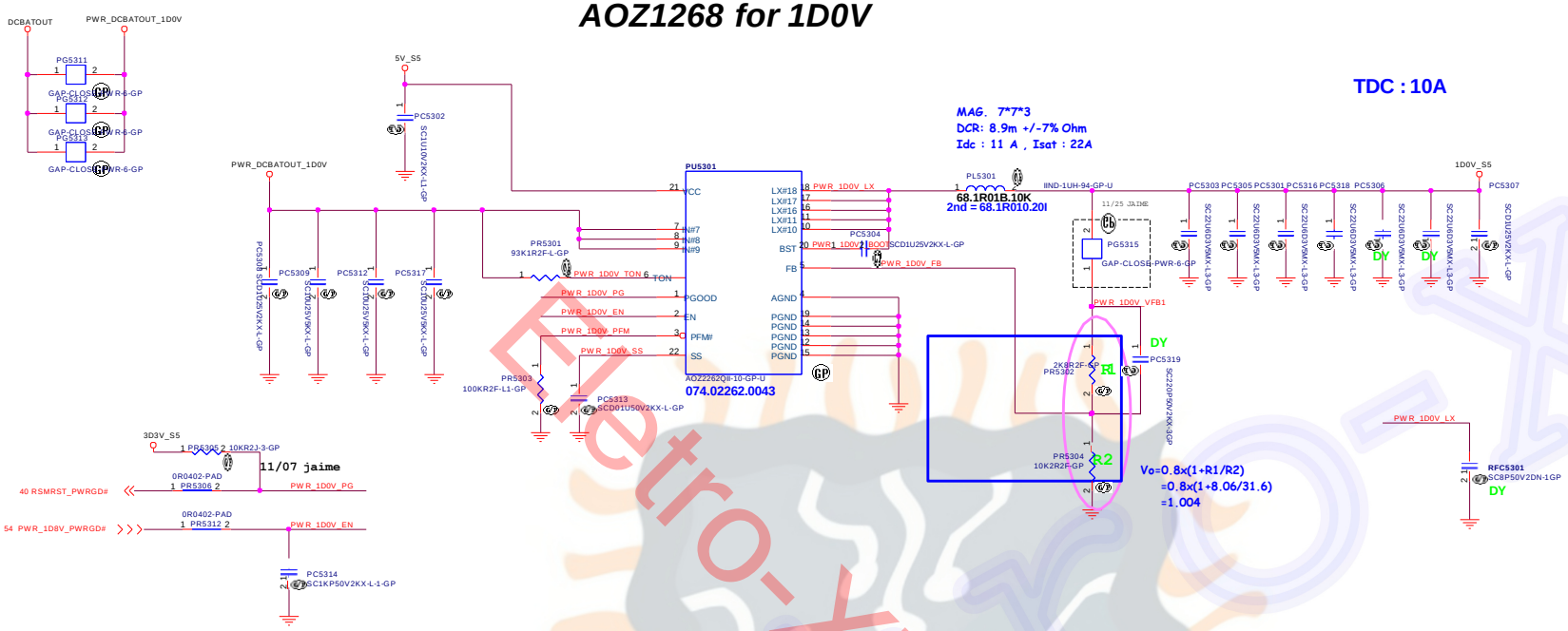
+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

<Core Design>
緯創資通 Wistron Corporation
DCDC-0D975V_VCCIO
LV115SKL-U
-1

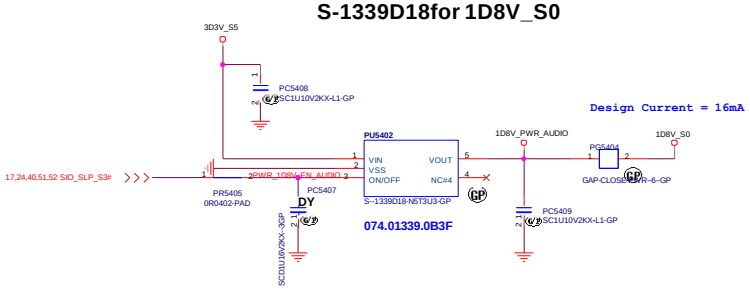
Main Func = 1D0V

AOZ1268 for 1D0V

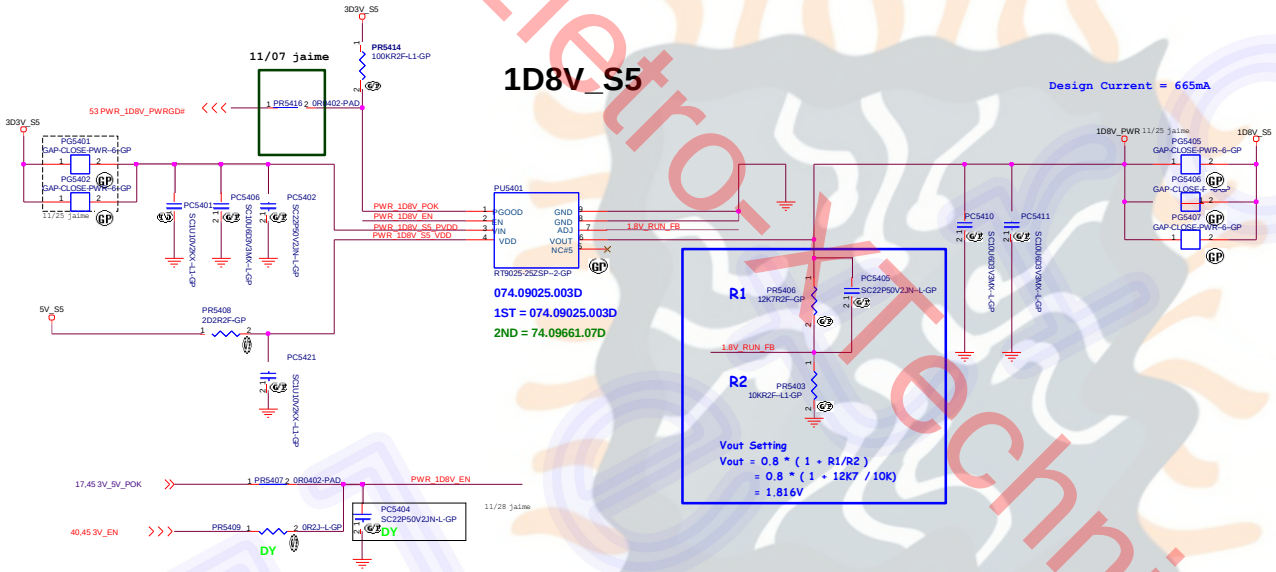


Main Func = 1D5V

S-1339D18for 1D8V_S0



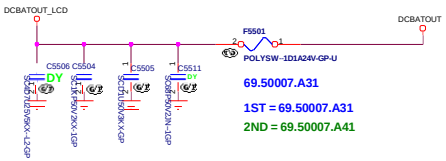
1D8V_S5



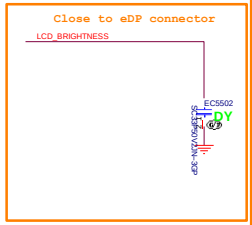
Wistron Corporation	緯創資通
DCDC V1D8V	
LV115 SKL-U	
Size: A2	Document Number
Date: Monday, April 25, 2016	Sheet 54

SSID = VIDEO

INVERTER POWER



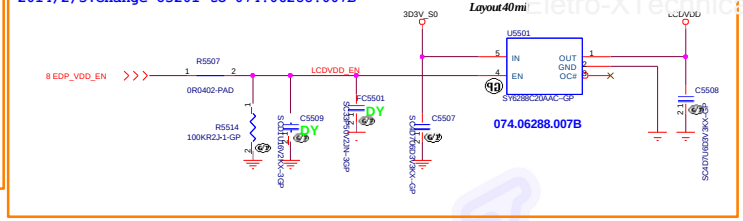
Close to eDP connector



SSID = VIDEO

LCD POWER (Do Not use SW 74.09724.09F)

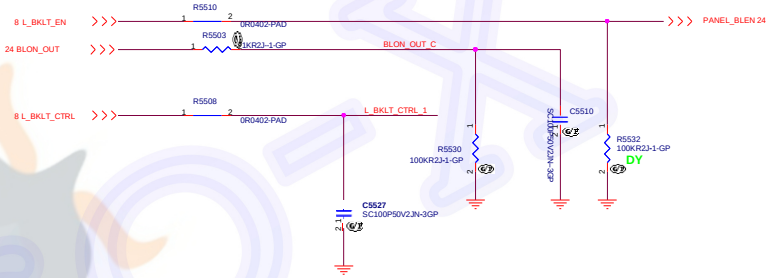
2014/2/5:Change U5201 to 074.06288.007B



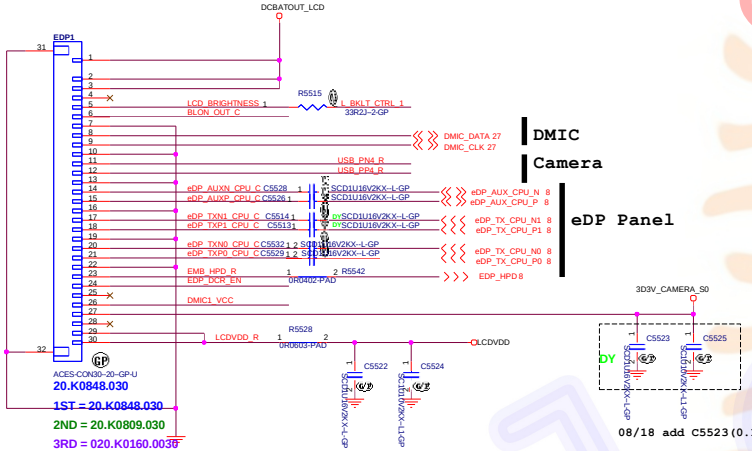
eDP Device

Item	Device
1	eDP Panel
2	Camera
3	DMIC
4	
5	
6	

Panel BL brightness/Power En/BL En



eDP connector



DMIC

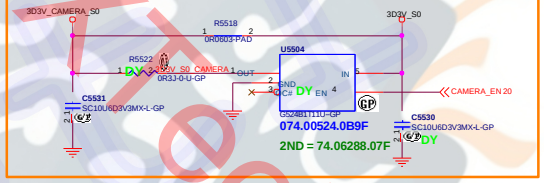
Camera

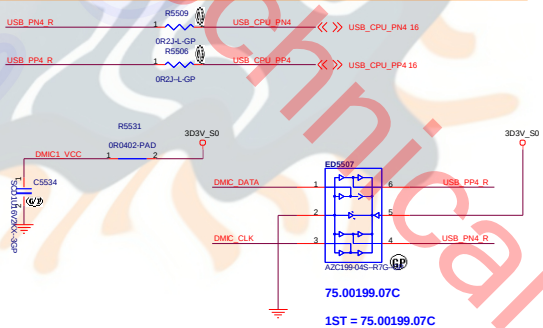
eDP Panel

08/18 add C5523(0.1uF), C5525(1uF)

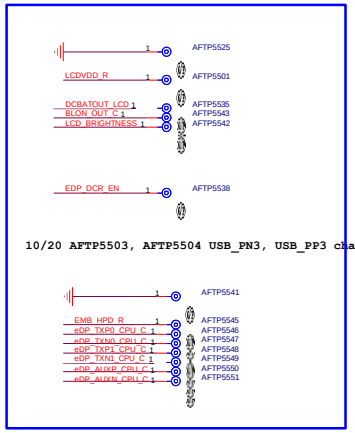
Layout 40 mil

CAMERA POWER





Test point



10/20 AFTP5503, AFTP5504 USB_PN3, USB_PP3 change to USB_PN3_R, USB_PP3_R

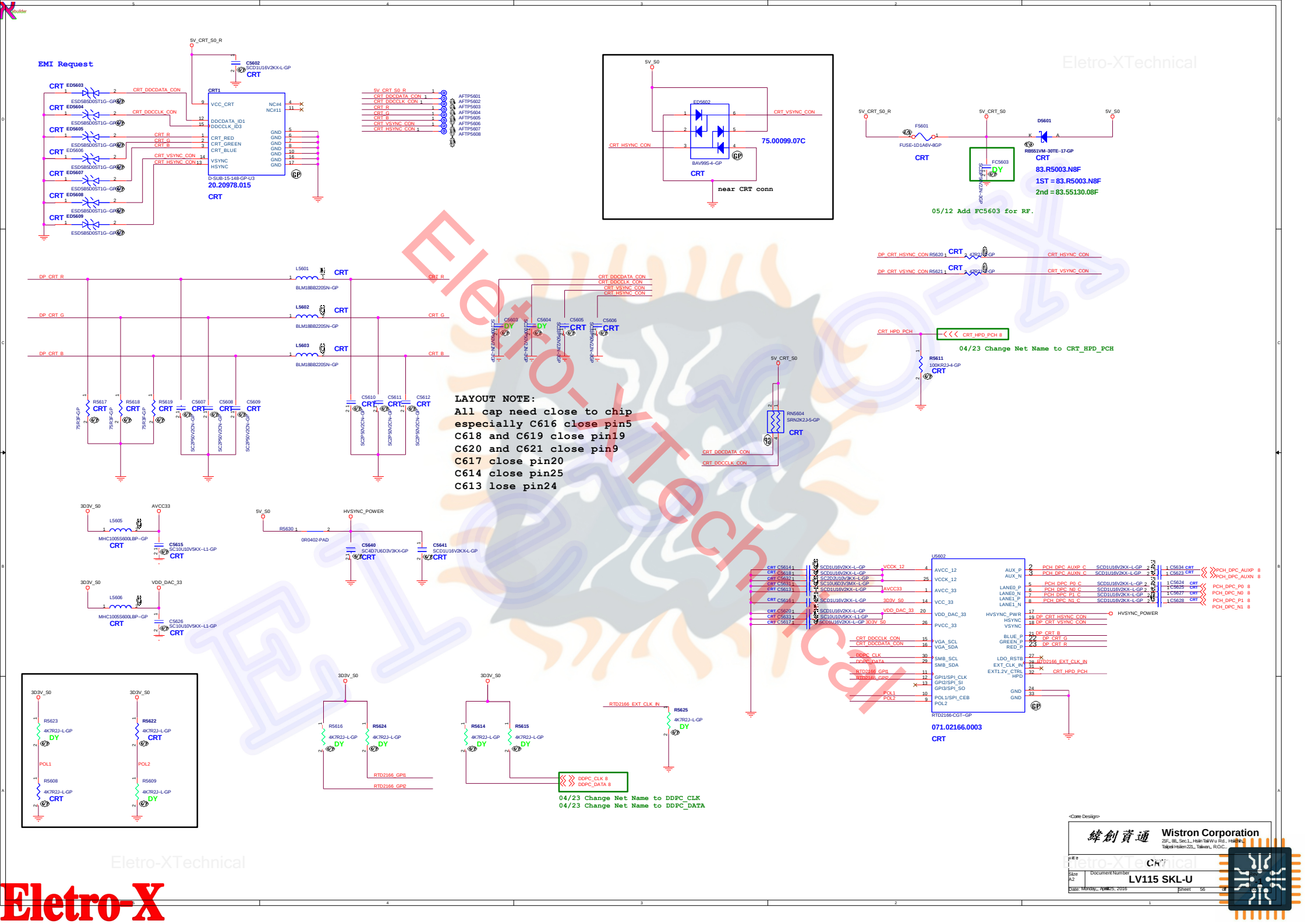
<Core Design>

Wistron Corporation

LCD&CAM&DMC&Touch

LV115 SKL-U

Monday, April 25, 2016

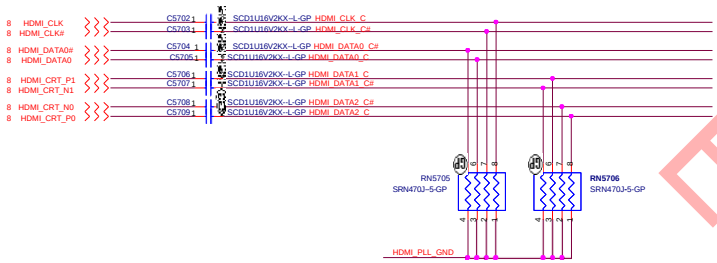


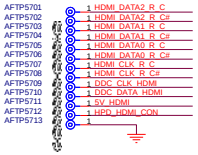
SSID = VIDEO

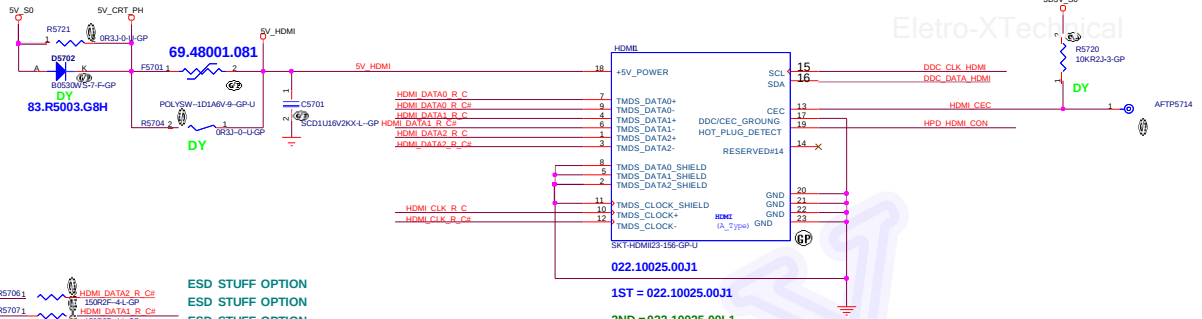
HDMI CONNECTOR

HDMI Passive Level Shifter

Close to HDMI Connector

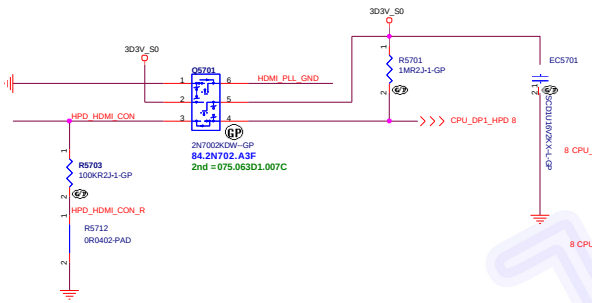


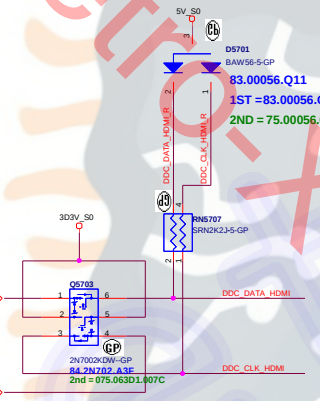


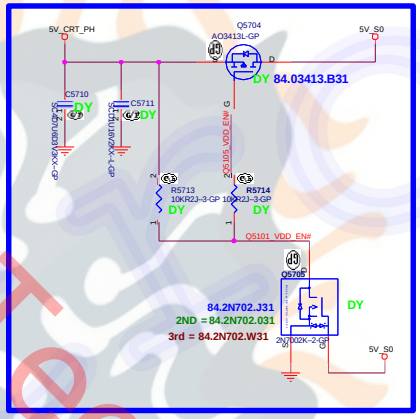


ESD STUFF OPTION
ESD STUFF OPTION
ESD STUFF OPTION
ESD STUFF OPTION

HDMI DDC Passive Level Shifter



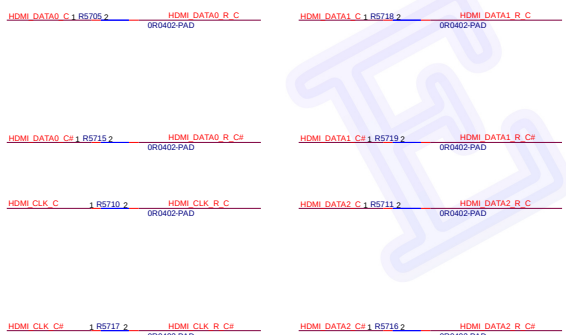


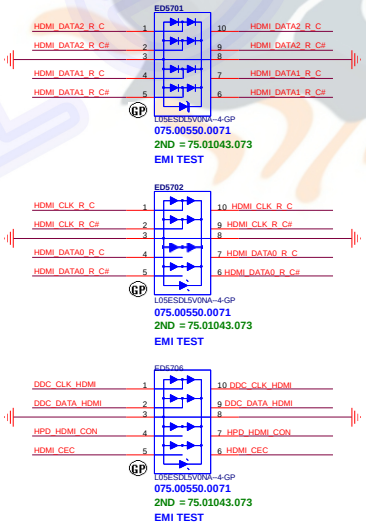


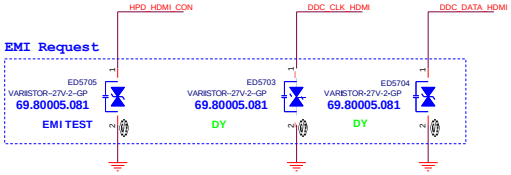
07/02 Change Part Number 84.07002.I31(轉 to 84.2N702.J31

HDMI A type pin define
(Total: 19pin)

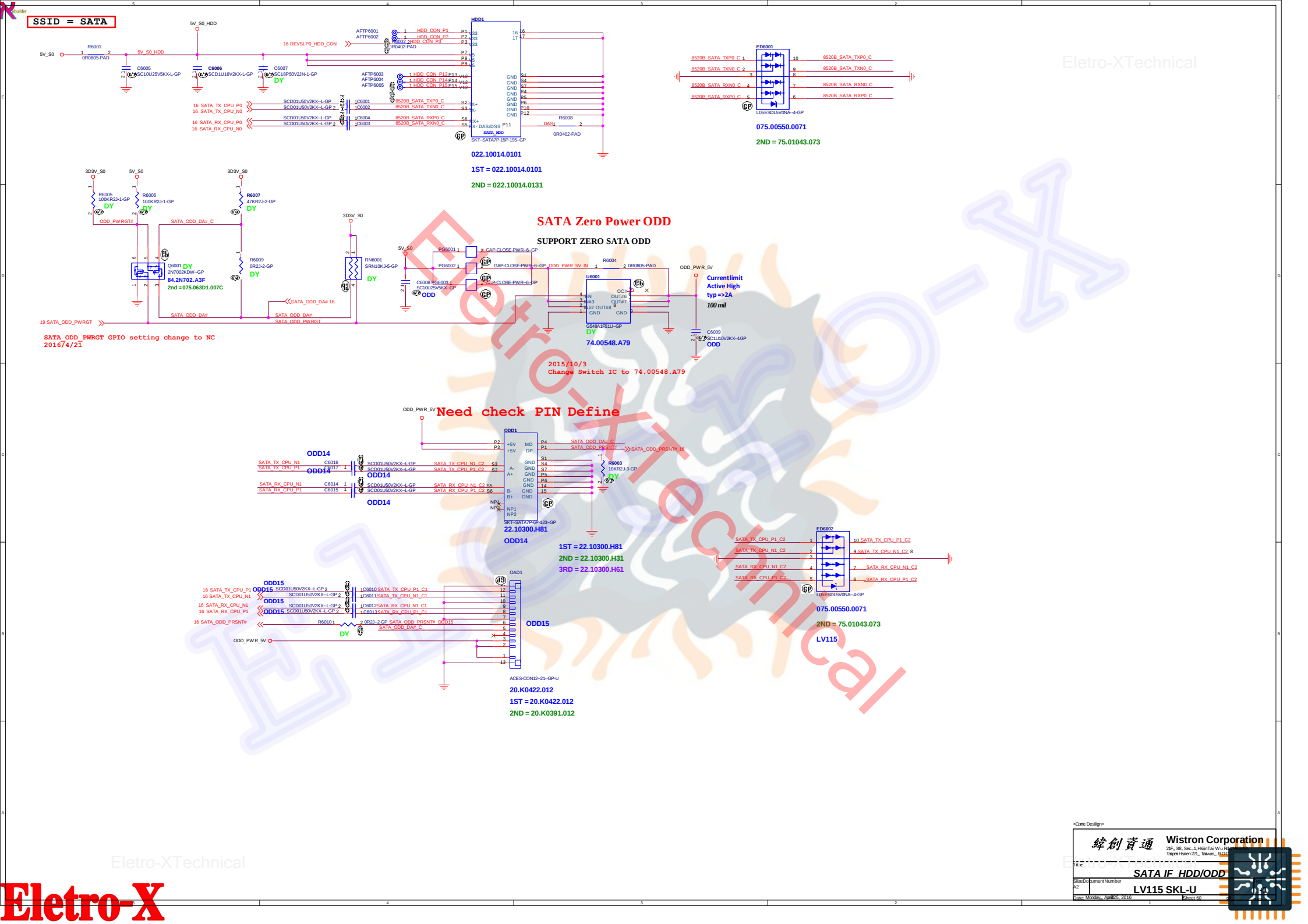
Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

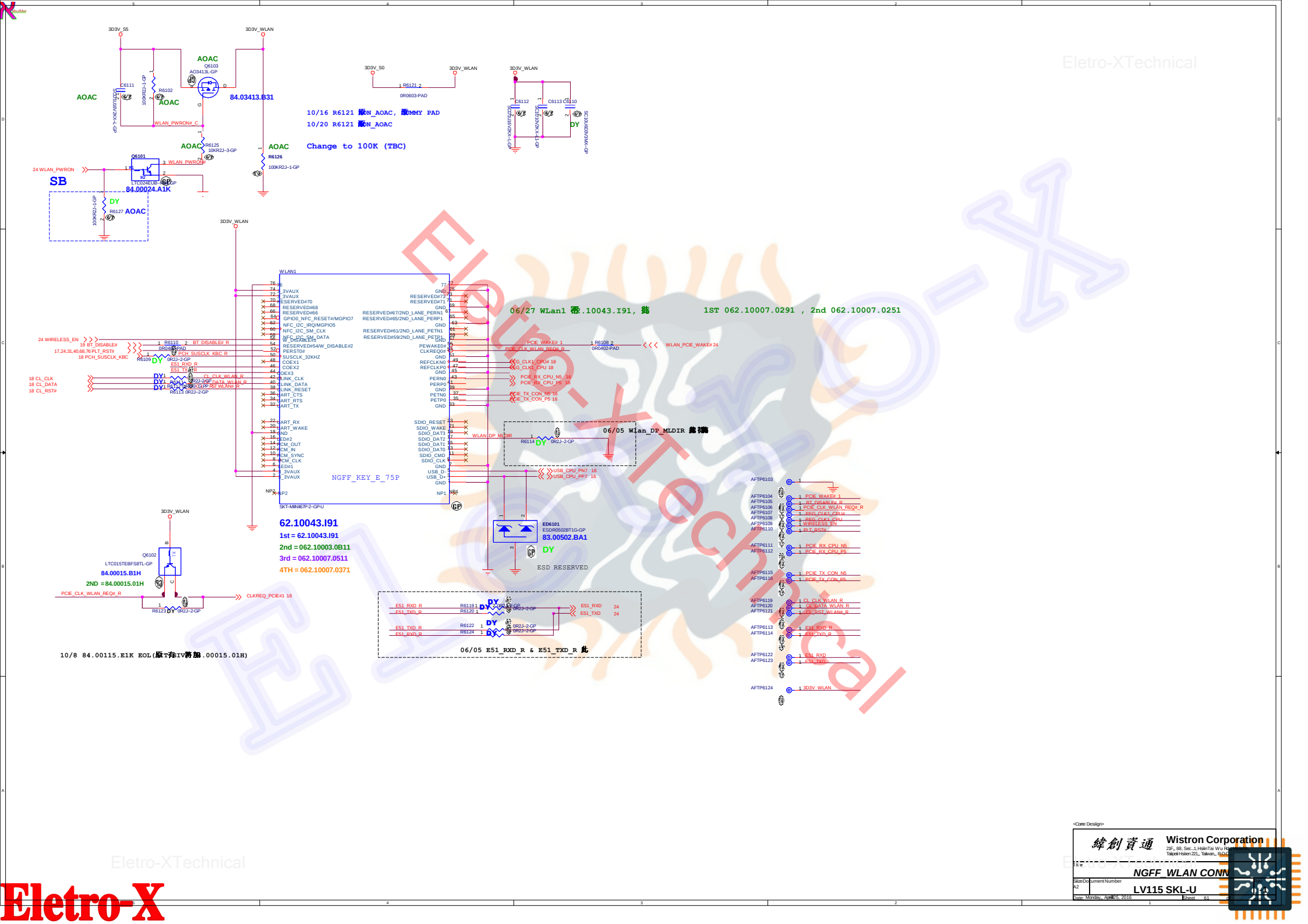






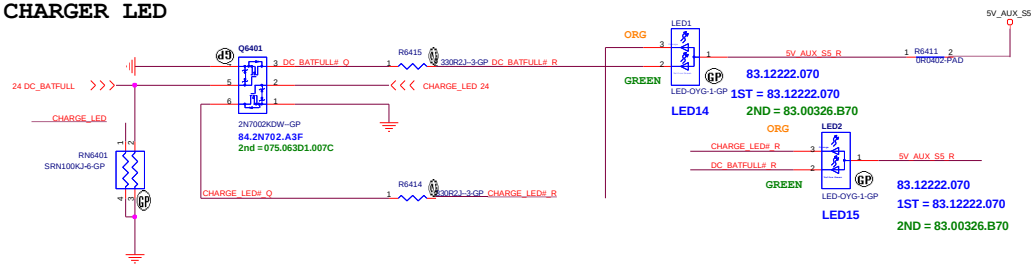
<Core Design>
緯創資通 Wistron Corporation
2F., 88, Sec.1, HsinTai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: HDMI
Size: A2
Document Number: LV115 SKL-U
Date: Monday, April 25, 2016
Sheet: 57


SSID = SATA
HDD1
SKT-SATA7P-15P-195-GP
022.10014.0101
1ST = 022.10014.0101
2ND = 022.10014.0131
ED6001
L05ESDL5V0NA-4-GP
075.00550.0071
2ND = 75.01043.073
SATA Zero Power ODD
SUPPORT ZERO SATA ODD
SATA_ODD_PWRGT GPIO setting change to NC
2016/4/21
Currentlimit
Active High
typ =>2A
100 mil
74.00548.A79
2015/10/3
Change Switch IC to 74.00548.A79
Need check PIN Define
ODD1
SKT-SATA7P-SP-123-GP
22.10300.H81
ODD14
1ST = 22.10300.H81
2ND = 22.10300.H31
3RD = 22.10300.H61
OAD1
ACES-CON12-21-GP-U
20.K0422.012
1ST = 20.K0422.012
2ND = 20.K0391.012
ED6002
L05ESDL5V0NA-4-GP
075.00550.0071
2ND = 75.01043.073
LV115
Wistron Corporation
SATA IF HDD/ODD
LV115 SKL-U
Eletro-XTechnical



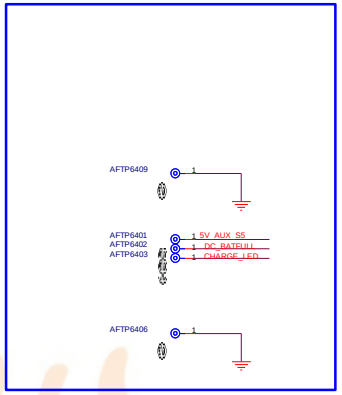
Test point

CHARGER LED

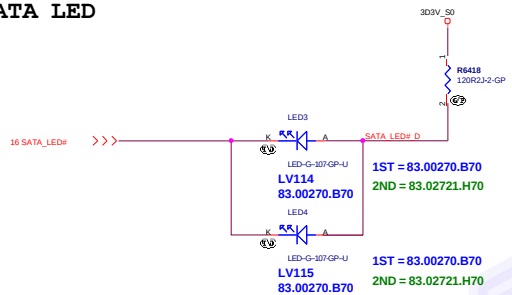


Forward Current	I_F	S2:25 G6:25	mA

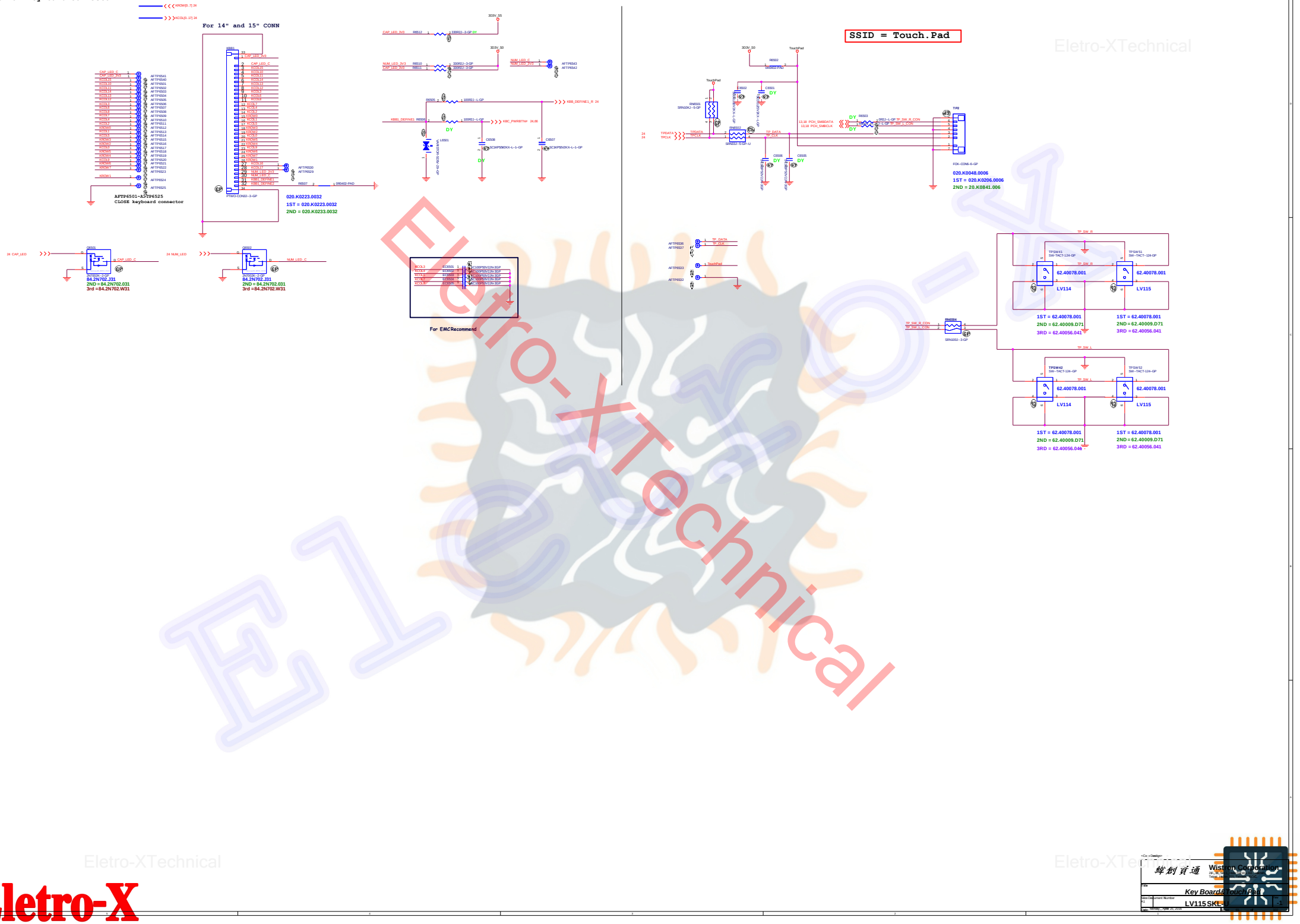
Chip		Emitted Color	Resin Color
Type	Material		
S2	AlGaInP	Brilliant Orange	Water Clear
G6	AlGaInP	Brilliant Yellow Green	



SATA LED



Internal KeyBoard Connector



Wistron Corporation

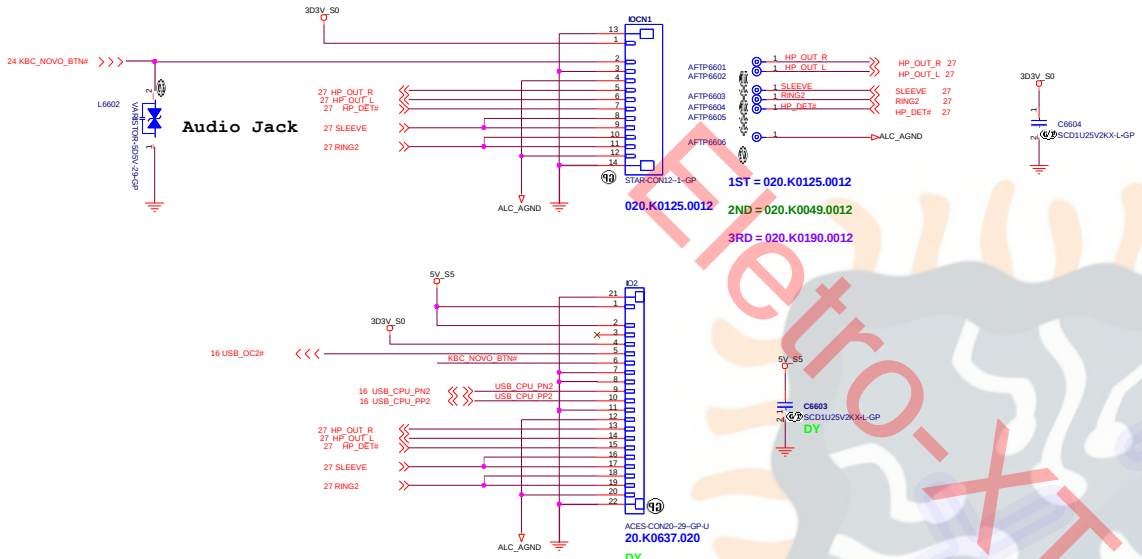
Key Board&Touch Pad

LV115 SKL

IO BD Device

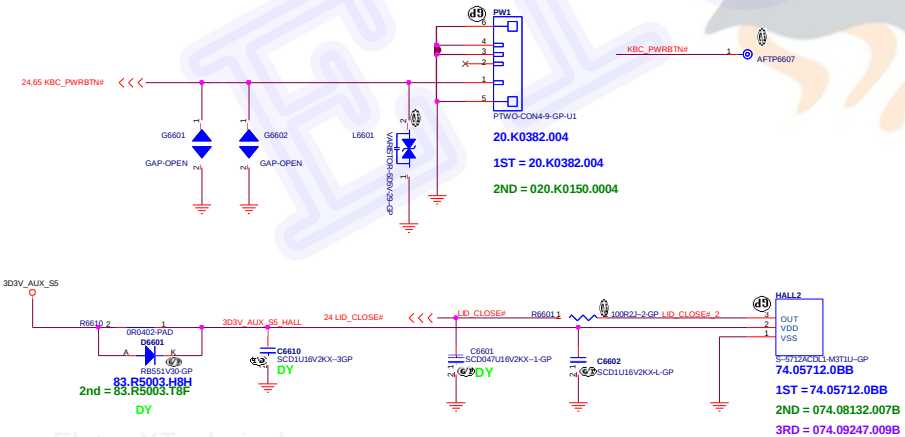
Item	Device
1	
2	
3	
4	

IO BD connector



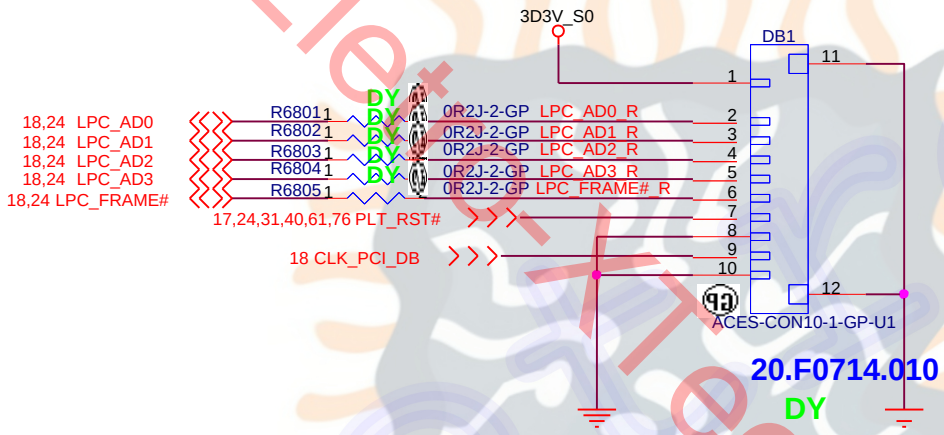
PWR BTN BD connector

Modified Pin Define and PN 20151208



Main Func = Debug

Debug Connector



20.F0714.010

DY

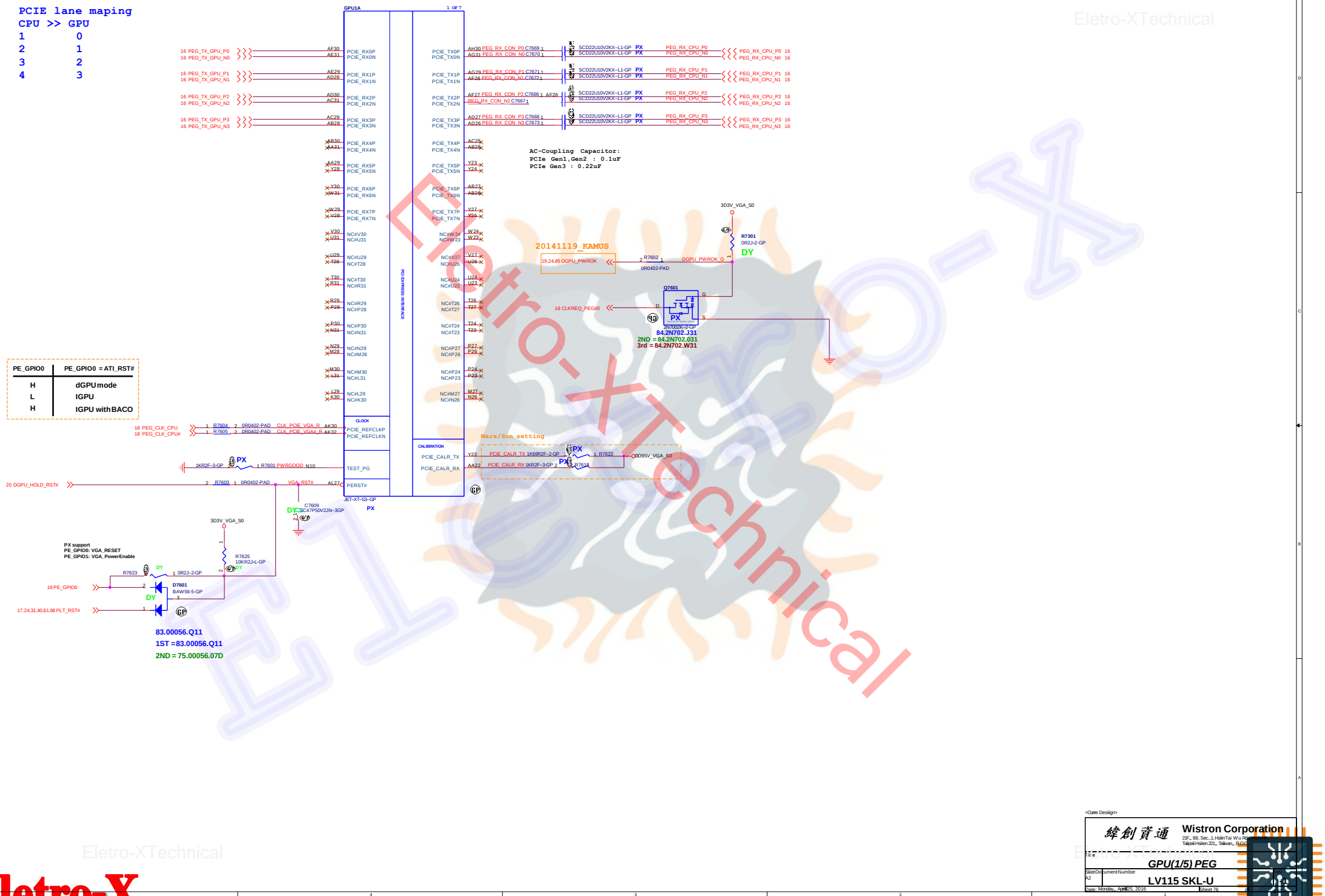
<Core Design>

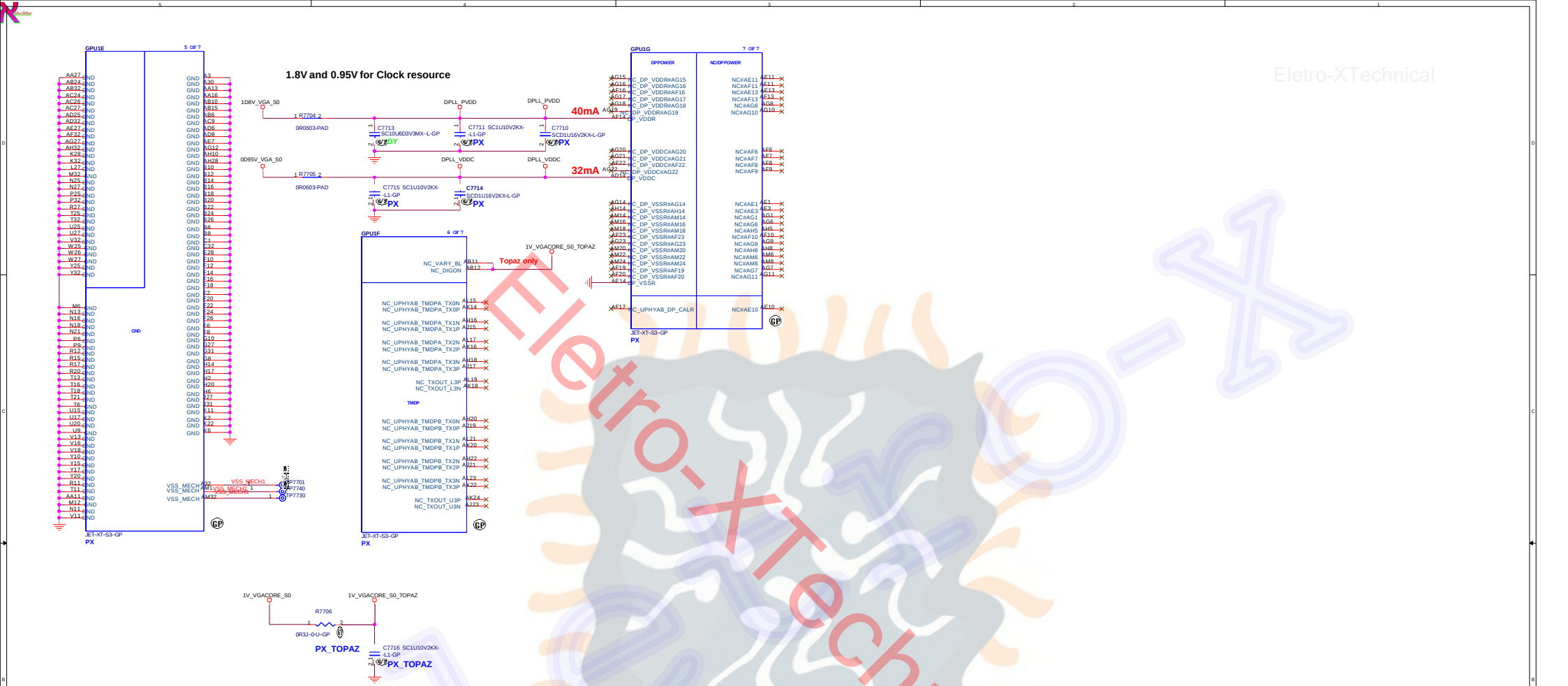
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug connector***

Size	Document Number	Rev
A4	**LV115 SKL-U**	-1

Date: Monday, April 25, 2016 Sheet 68 of 102


PCIE lane maping
CPU >> GPU
1 0
2 1
3 2
4 3
GPU1A
1 OF 7
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCI EXPRESS INTERFACE
CLOCK
PCIE_REFCLKP
PCIE_REFCLKN
TEST_PG
PERST#
CALIBRATION
PCIE_CALR_TX
PCIE_CALR_RX
JET-XT-S3-GP
AC-Coupling Capacitor:
PCIe Gen1,Gen2 : 0.1uF
PCIe Gen3 : 0.22uF
20141119_KAMUS
19,24,85 DGPU_PWROK
R7602
0R0402-PAD
DGPU_PWROK_G
3D3V_VGA_S0
R7301
0R2J-2-GP
DY
Q7601
2N7002K-2-GP
18 CLKREQ_PEG#0
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
PE_GPIO0 | PE_GPIO0 = ATI_RST#
H | dGPU mode
L | IGPU
H | IGPU with BACO
18 PEG_CLK_CPU
18 PEG_CLK_CPU#
R7604
R7605
0R0402-PAD
CLK_PCIE_VGA_R
CLK_PCIE_VGA#_R
1KR2F-3-GP
R7601 PWRGOOD
20 DGPU_HOLD_RST#
R7603
VGA_RST#
C7609
SC47P50V2JN-3GP
Mars/Sun setting
PCIE_CALR_TX 1K69R2F-2-GP
PCIE_CALR_RX 1KR2F-3-GP
R7622
R7618
C0D95V_VGA_S0
PX support
PE_GPIO0: VGA_RESET
PE_GPIO1: VGA_PowerEnable
R7625
10KR2J-L-GP
R7623
0R2J-2-GP
19 PE_GPIO0
D7601
BAW56-5-GP
17,24,31,40,61,68 PLT_RST#
83.00056.Q11
1ST =83.00056.Q11
2ND = 75.00056.07D
Wistron Corporation
GPU(1/5) PEG
LV115 SKL-U
Eletro-XTechnical

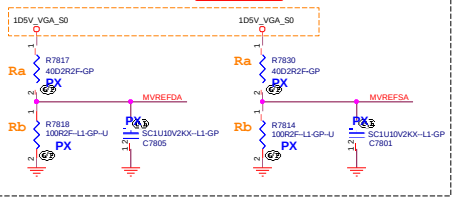


<Core Design>
緯創資通 Wistron Corporation
21F., 88, Sec. 1, HsinTai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU (2/5) DIGITAL OUT
Size: A2 | Document Number: LV115 SKL-U
Date: Monday, April 25, 2016 | Sheet 77

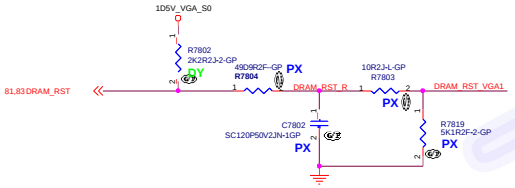
Please MVREF drivers and Caps close to ASIC

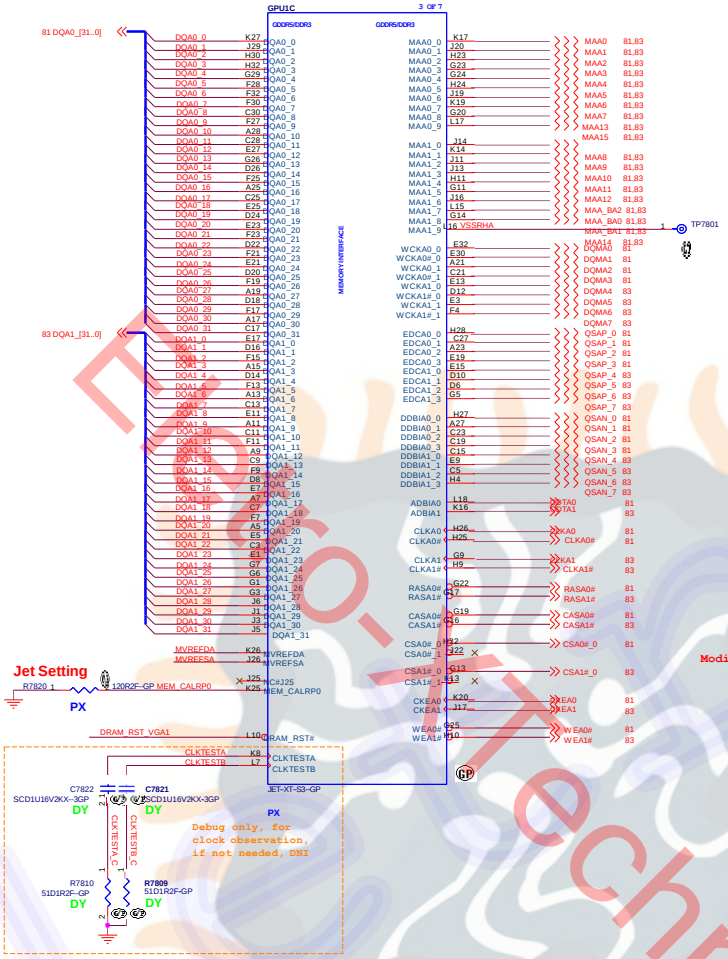
DDR3/GDDR3 Memory Stuff Option(JET/TOPAZ)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





Modify 20151007

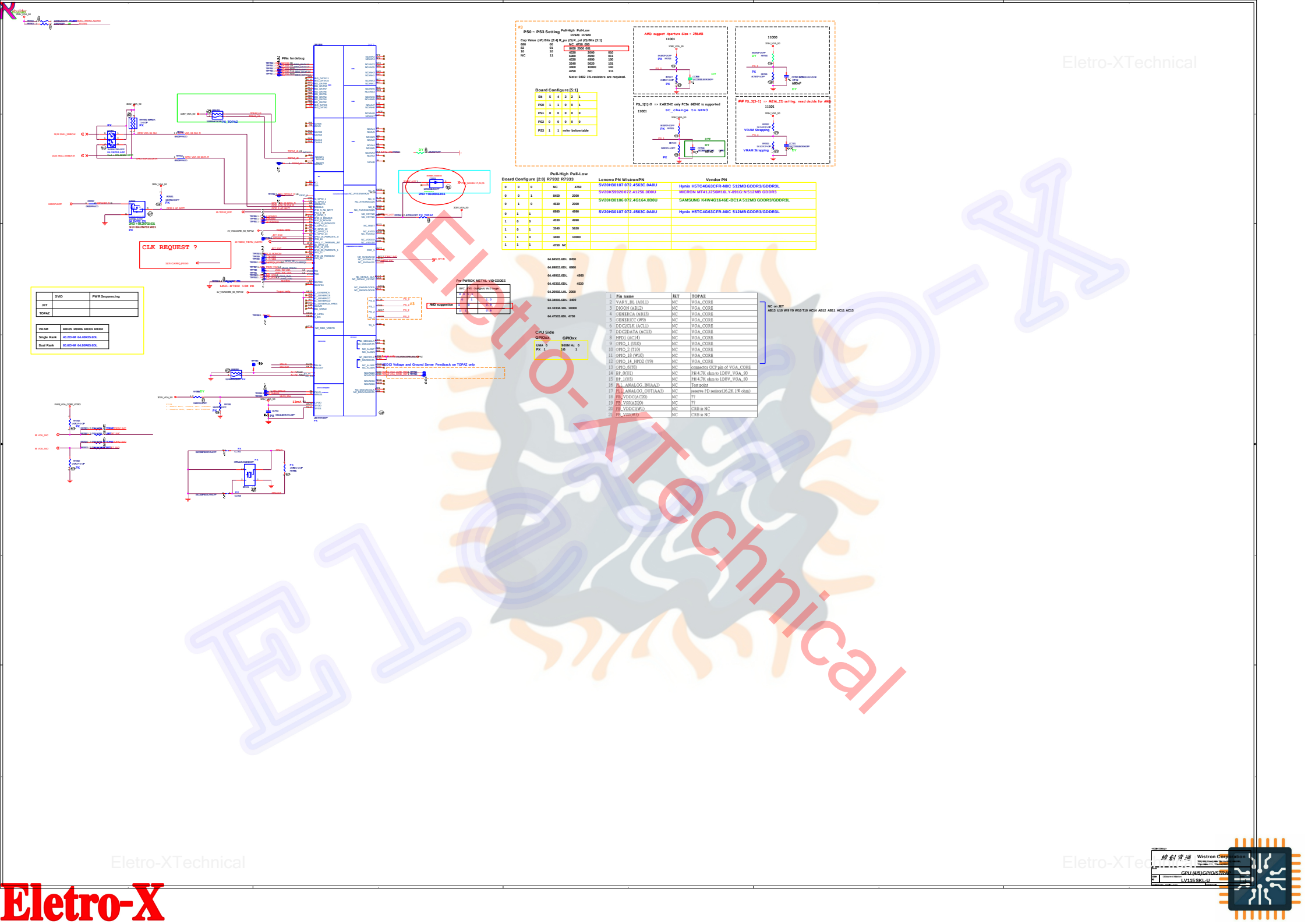
Wistron Corporation
21F., 88, Sec.1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

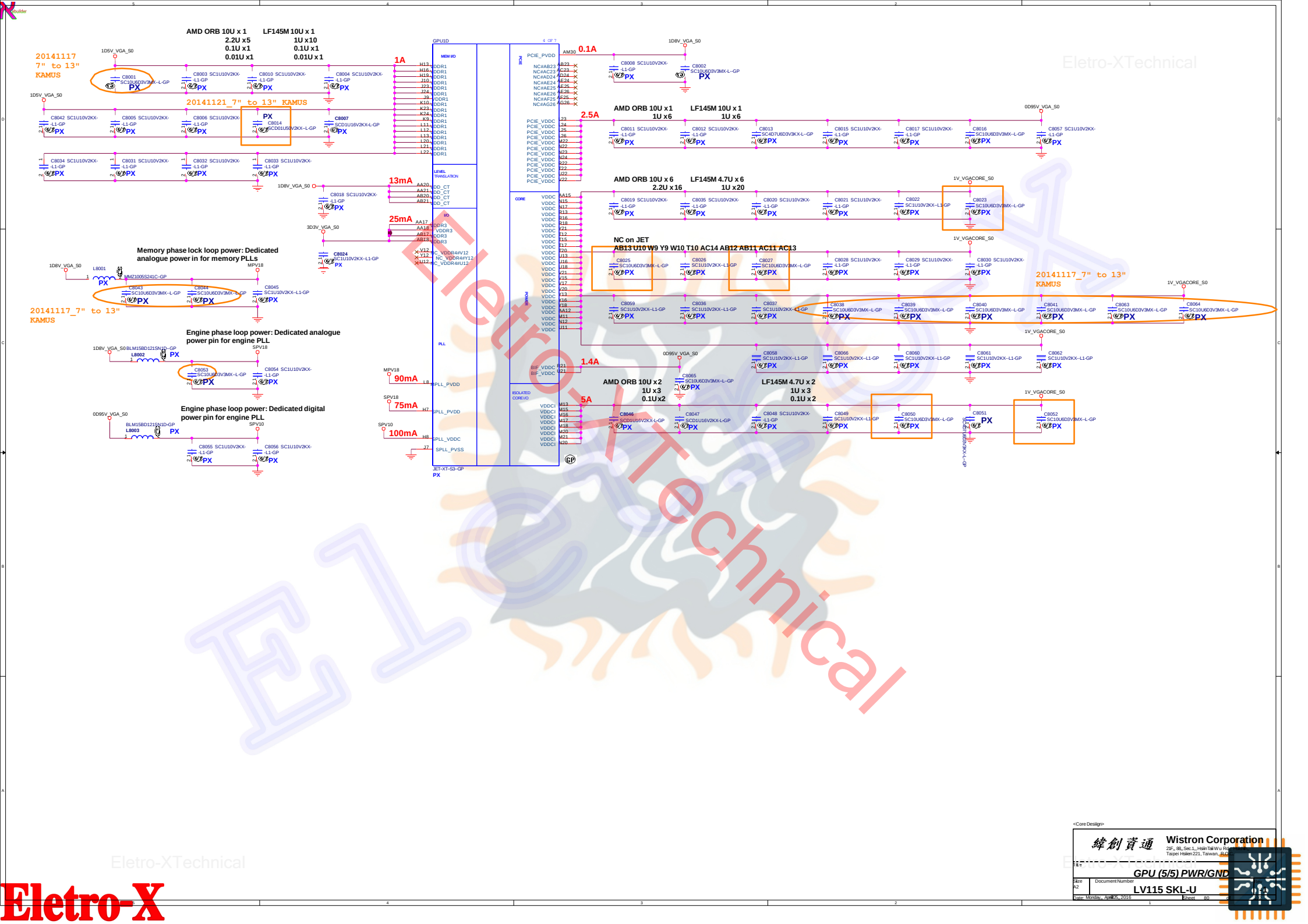
GPU (3/5) VRAM I/F

LV115 SKL-U

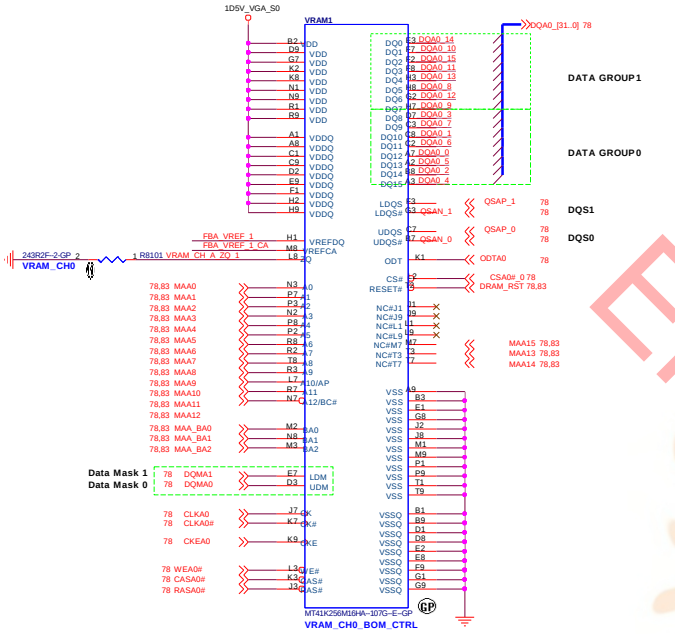
Size: A2 | Document Number | Rev

Date: Monday, April 25, 2016 | Sheet 78

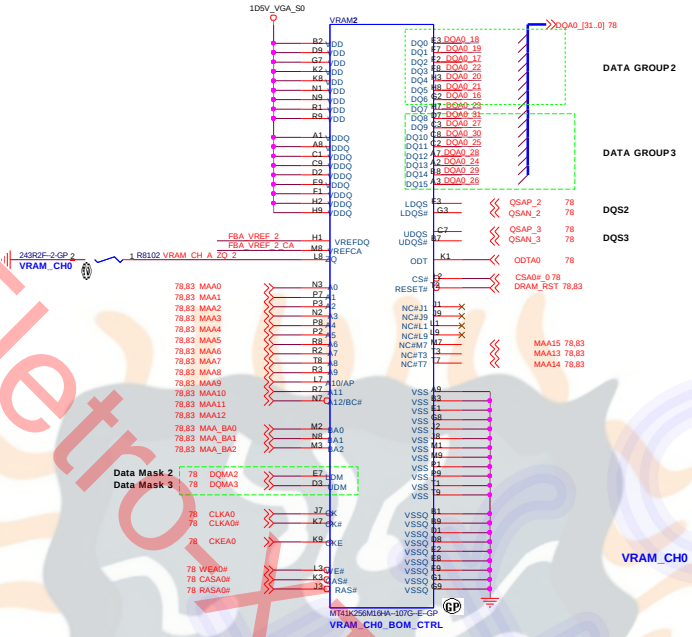


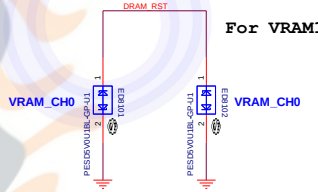

AMD ORB 10U x 1
2.2U x5
0.1U x1
0.01U x1
LF145M 10U x 1
1U x10
0.1U x1
0.01U x1
20141117
7" to 13"
KAMUS
1A
20141121_7" to 13" KAMUS
13mA
25mA
Memory phase lock loop power: Dedicated analogue power in for memory PLLs
20141117_7" to 13"
KAMUS
Engine phase loop power: Dedicated analogue power pin for engine PLL
90mA
Engine phase loop power: Dedicated digital power pin for engine PLL
75mA
100mA
0.1A
2.5A
AMD ORB 10U x1
1U x6
LF145M 10U x 1
1U x6
AMD ORB 10U x 6
2.2U x 16
LF145M 4.7U x 6
1U x20
NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
20141117_7" to 13"
KAMUS
1.4A
AMD ORB 10U x2
1U x3
0.1U x2
5A
LF145M 4.7U x 2
1U x 3
0.1U x 2
Wistron Corporation
GPU (5/5) PWR/GND
LV115 SKL-U
Eletro-XTechnical

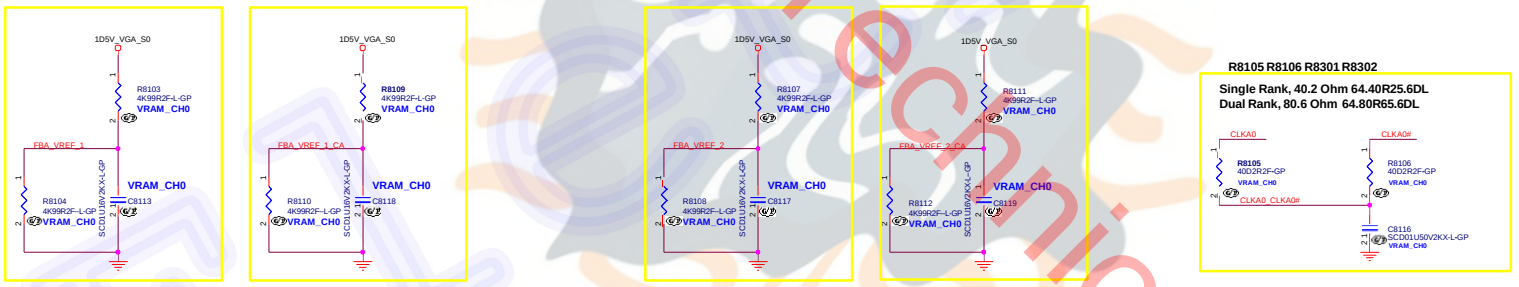
Channel 0 DATA0:15

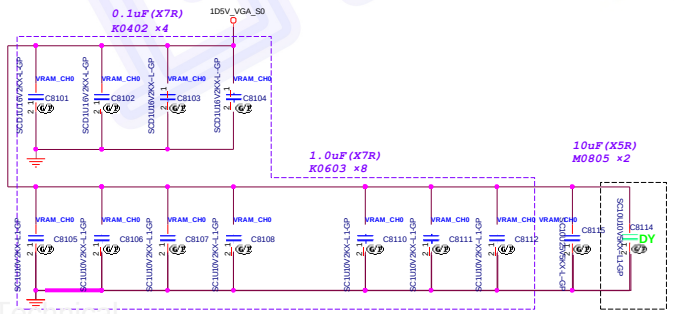


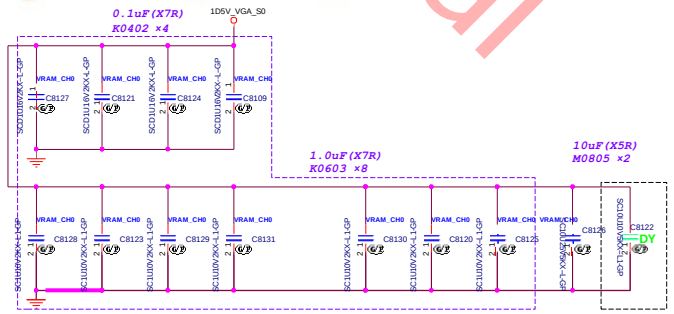
Channel 0 DATA16:31





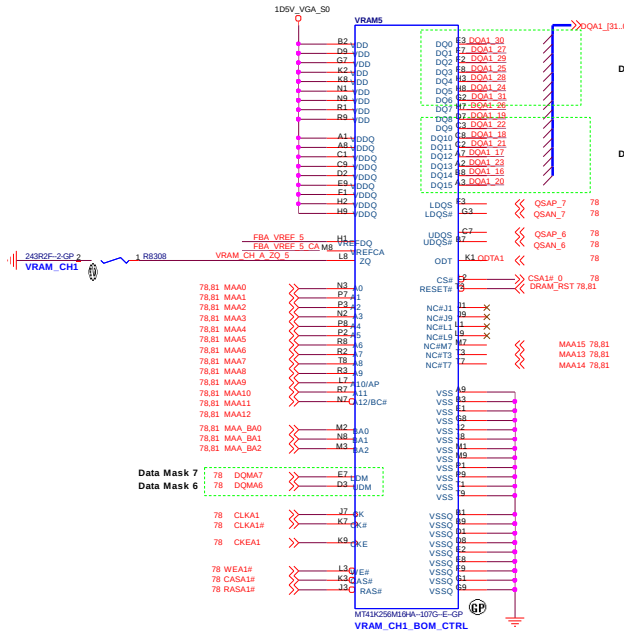




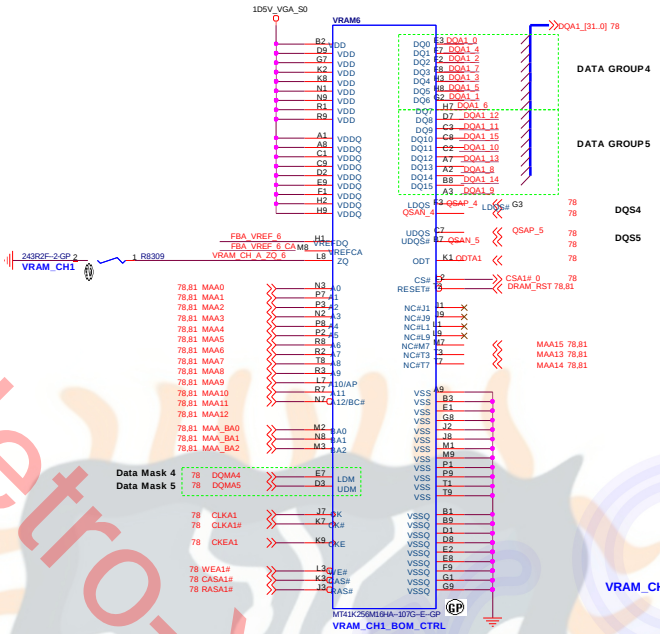


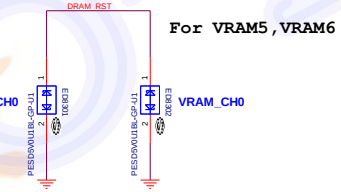
<Core Design>
緯創資通 Wistron Corporation
2F., 88, Sec.1, HsinTai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM1,2 (1/4)
Size A2
Document Number
LV115 SKL-U
Date: Monday, April 25, 2016
Sheet 81

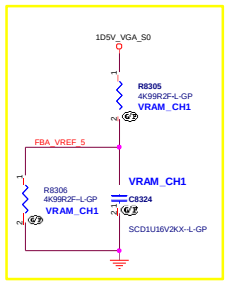
Channel 1 DATA16:31

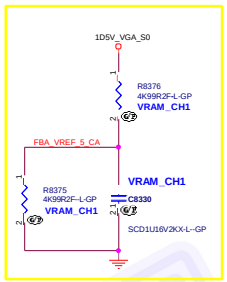


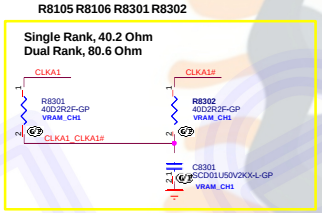
Channel 1 DATA0:15

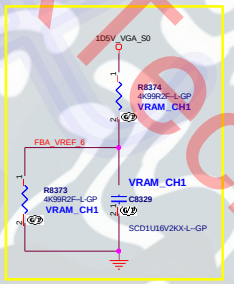


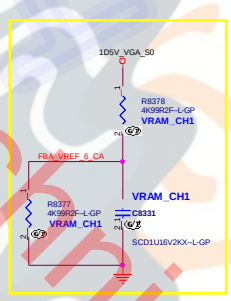


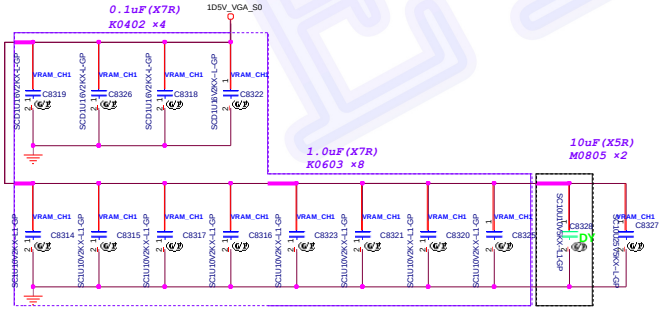


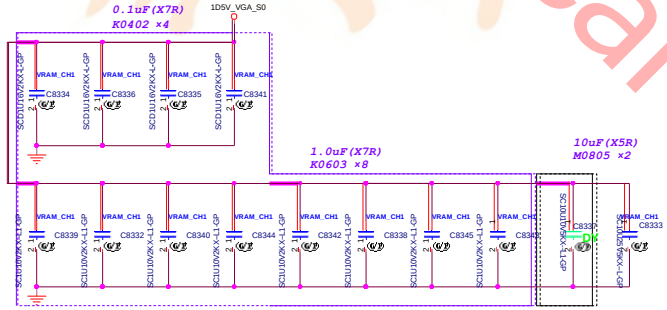






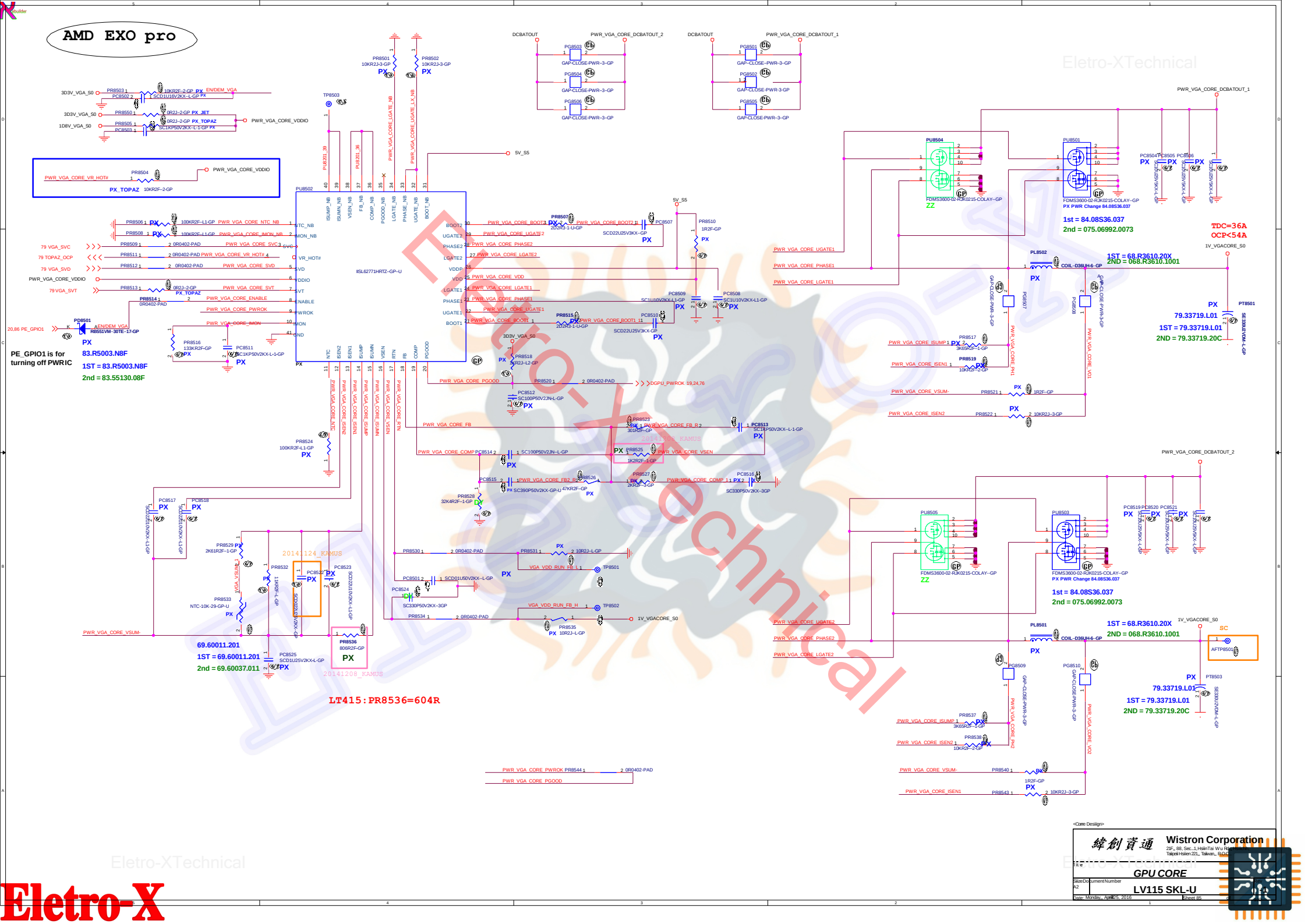






<Core Design>
緯創資通 Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM5,6 (3/4)
Size Document Number
A2 LV115 SKL-U
Date: Monday, April 25, 2016 Sheet 83

AMD EXO pro


PE_GPIO1 is for turning off PWRIC
83.R5003.N8F
1ST = 83.R5003.N8F
2nd = 83.55130.08F
69.60011.201
1ST = 69.60011.201
2nd = 69.60037.011
LT415:PR8536=604R
1st = 84.08S36.037
2nd = 075.06992.0073
TDC=36A
OCP<54A
1ST = 68.R3610.20X
2ND = 068.R3610.1001
79.33719.L01
1ST = 79.33719.L01
2ND = 79.33719.20C
Wistron Corporation
GPU CORE
LV115 SKL-U

20151106 need Add MOS to Control 1D35V_EN# IN SB version

3D3V_S0 to 3D3V_VGA_S0 Transfer

Peak current: 25mA

Discharge circuit

GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D35V_VGA_S0

=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

1D8V_S5 to 1D8V_VGA_S0 Transfer

1D0V_S5 to 0D95V_VGA_S0 Transfer

Peak current: 311mA

Peak current: 2A

NN30331A for VGA_1D5V(For VRAM DDR3)

Reference OSLO 1D5V_VGA_S0

MAG. 7 x 7 x 3.0mm

DCR: 9m~10mOhm

Idc : 10 A , Isat : 22A

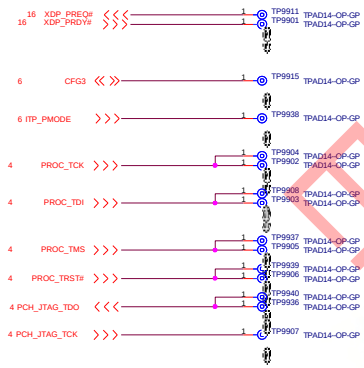
TDC : 6A

Add For Discharge Circuit 20151123

Vo=0.8x(1+R1/R2)

=0.8x(66.5+75/75)

=1.509



<Core Design>

緯創資通 Wistron Corporation

21F., 88, Sec. 1, HsinTai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

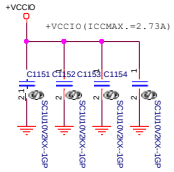
Size: A2 | Document Number: LV115 SKL-U | Rev:

Date: Monday, April 25, 2016 | Sheet 99

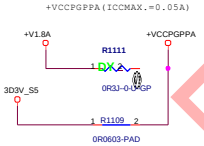
Main Func = CPU

UNSLICED GT

VCCIO



PCH DERIVED RAILS



GTUS

20141114 Alden

+V_VCCGTUS_VR can merge to +VCCGT

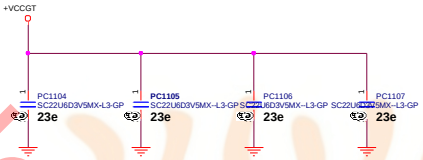
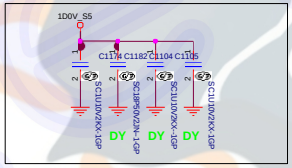
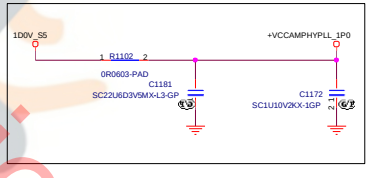
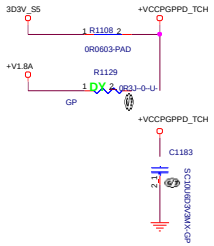


Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		
		(6.3V)*	
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible





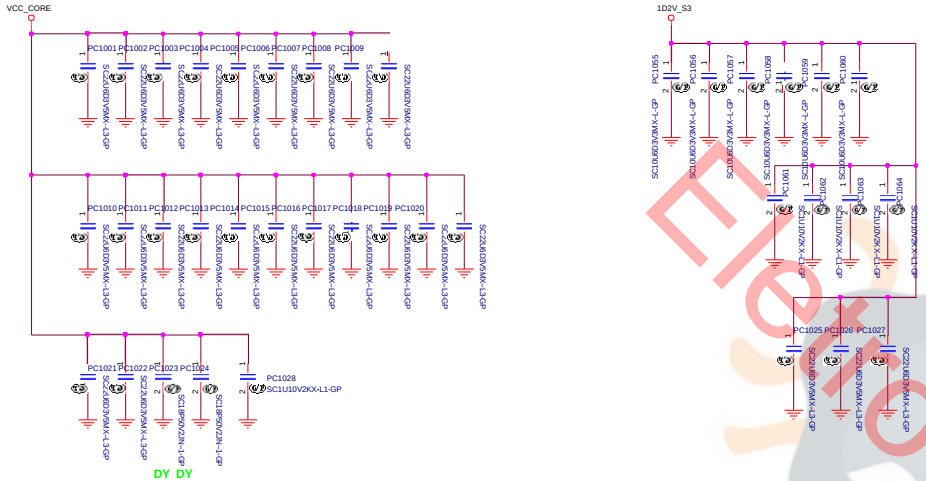


Wistron Corporation
CPU (Power CAP2)
LV115 SKL-U

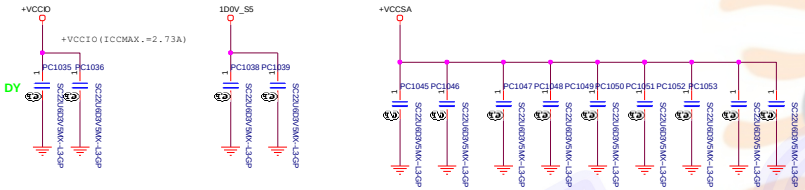
Main Func = CPU

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

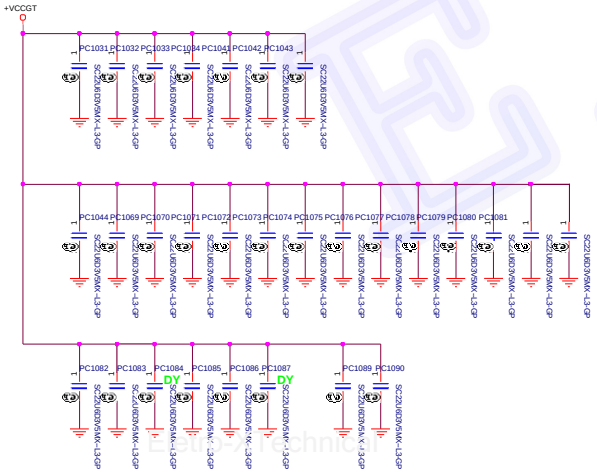


VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A



(#543016 PDG)

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

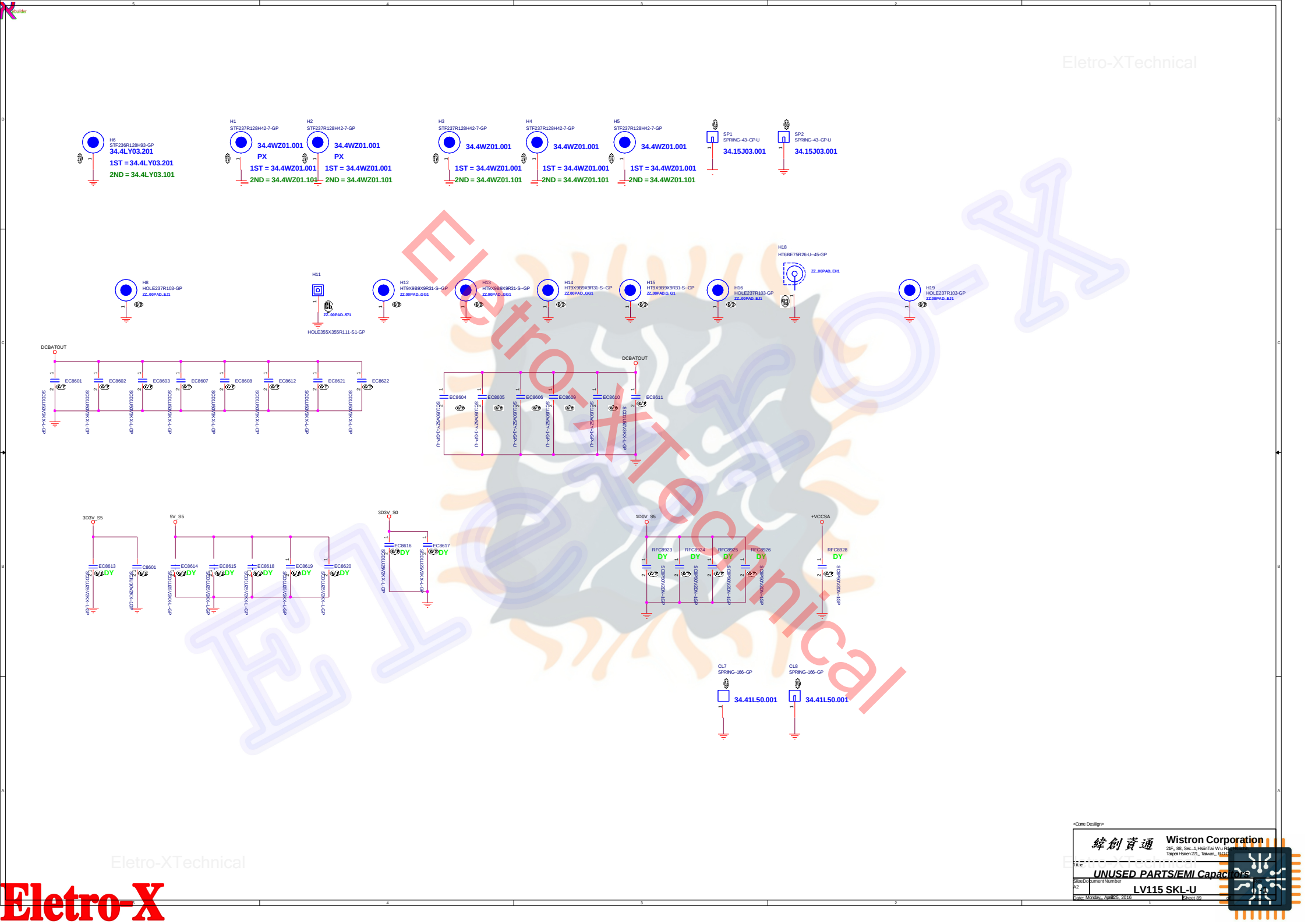
<Core Design>

Wistron Corporation
2F, 88, Sec.1, HsinTai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)

Size: A2 | Document Number: LV115 SKL-U | Rev:

Date: Monday, April 25, 2016 | Sheet 10



<Core Design>

Wistron Corporation

Title: UNUSED PARTS/EMI Capacitors

Size: A2 | Document Number: LV115 SKL-U

Date: Monday, April 25, 2016 | Sheet 89