

# NBWAA

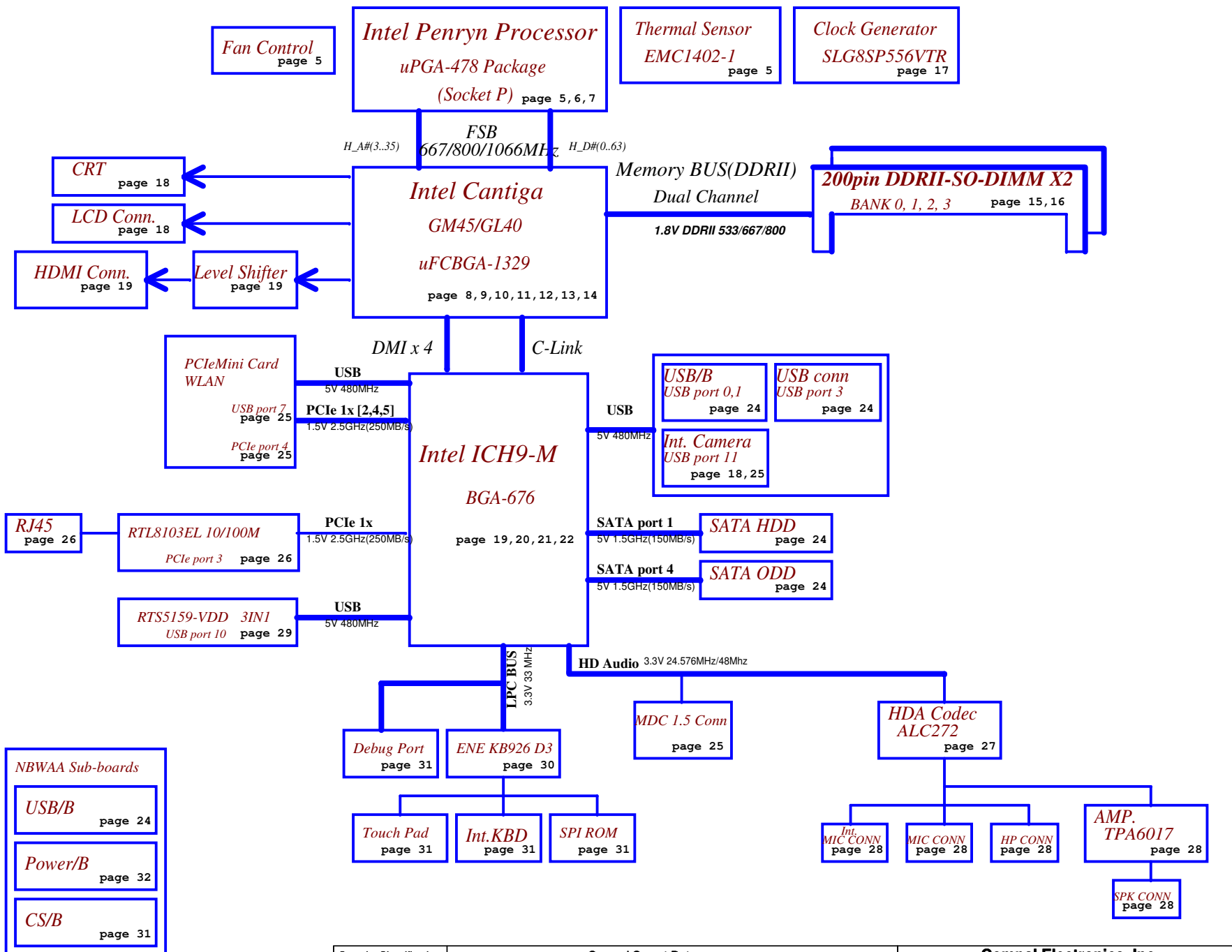
*Low Cost Los Angeles 10L*

*LA-5821P REV 1.0 Schematics*

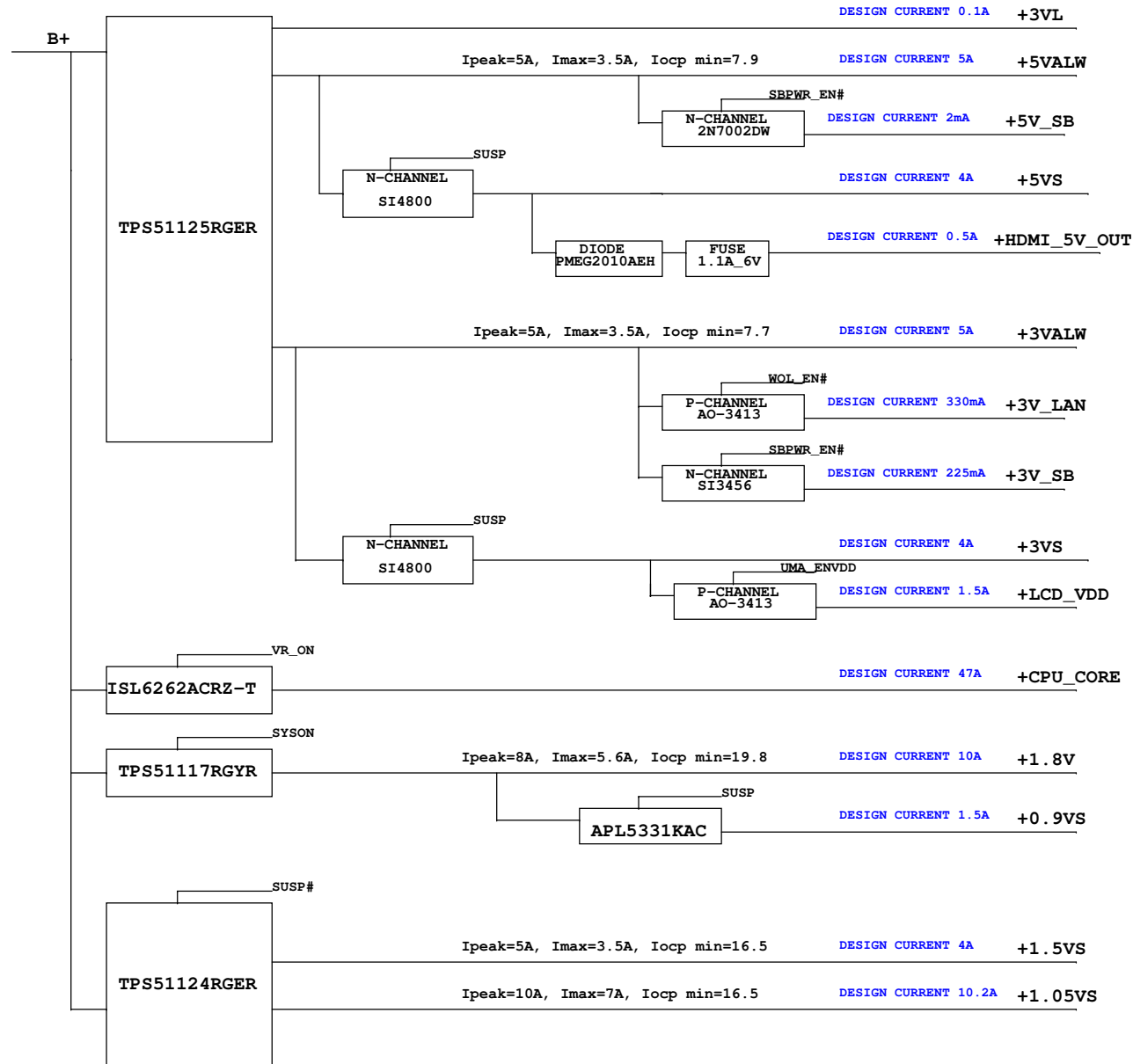
Intel Penryn/ Cantiga/ ICH9M  
2008-08-10 Rev. 1.0

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**Model Name : NBWAA**  
**File Name : LA-5821P**



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## Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

## BTO Option Table

Function	North Bridge		RJ11	CAMERA	MIC	HDMI	
description	GM	GL				Y	
explain	GM45	GL40	MODEM	CAMERA	MIC	HDMI	Non-HDMI
BTO	GM45R3@ GM45R1@	GL40R3@ GL40R1@	MDC@	CAM@	MIC@	IHDMI@	NIHDMI@

## External PCI Devices

### EC SM Bus1 address

### EC SM Bus2 address

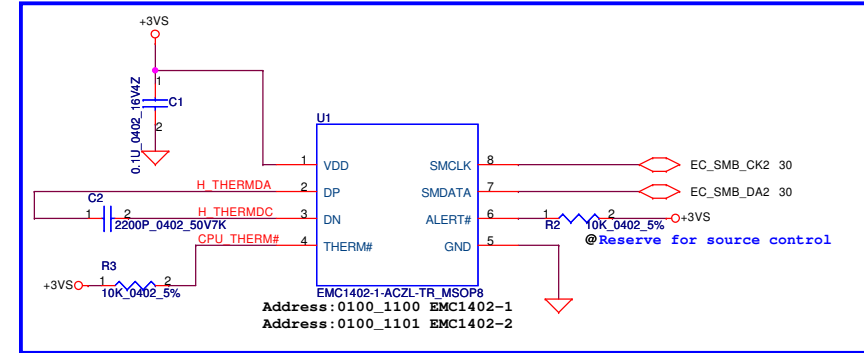
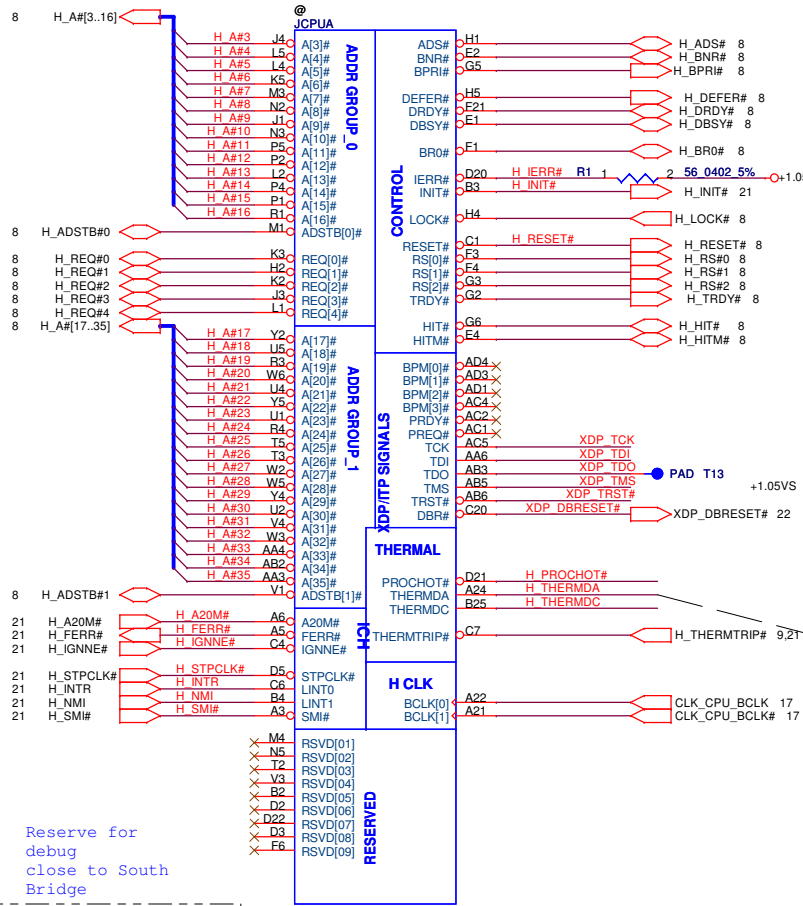
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011X b			
+3VL	FUN/B (CAP Sensor)		+3VS	CPU THM Sen	0100 110x b
				SMSC SMC1402	

### ICH9M SM Bus address

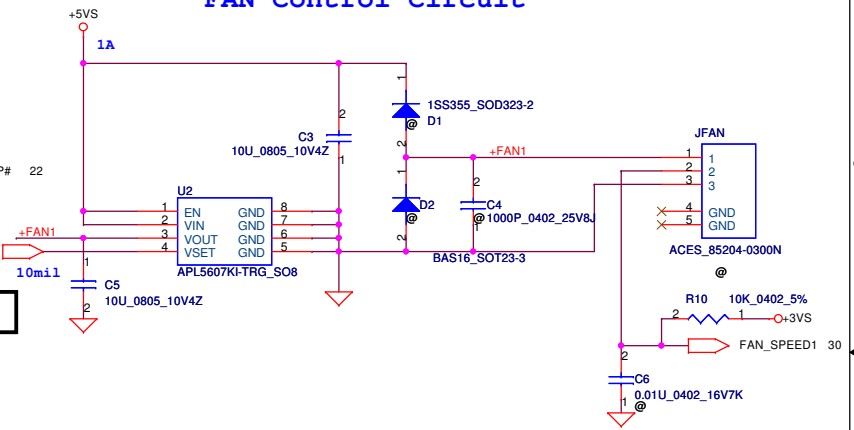
Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS		

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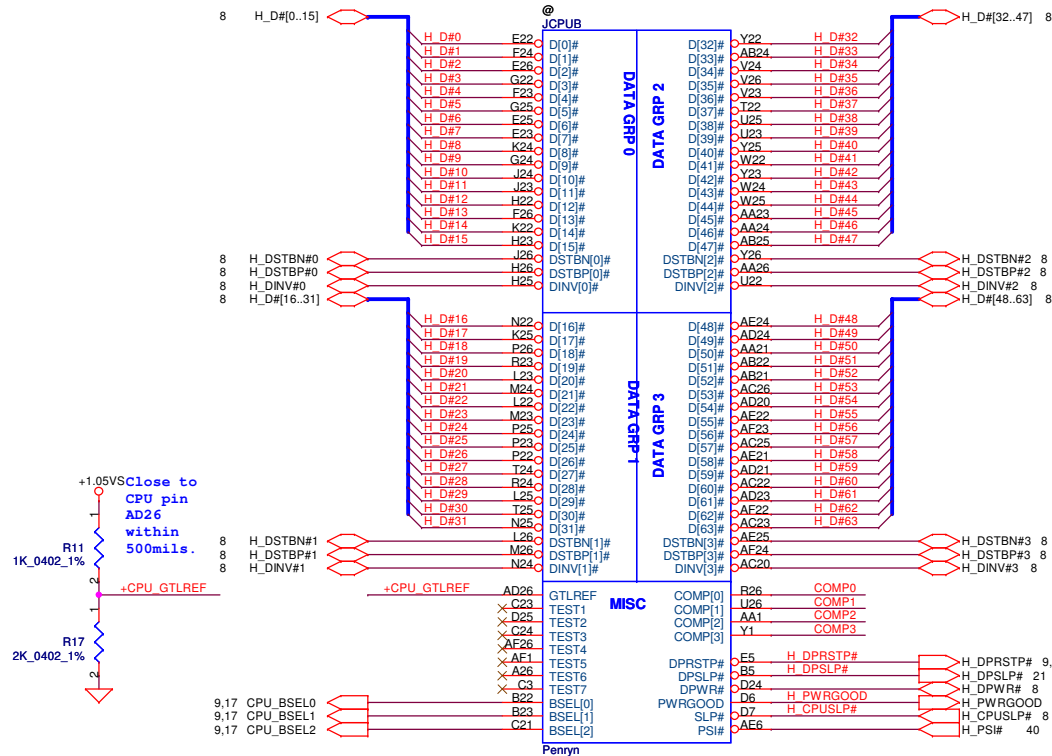


## FAN Control Circuit



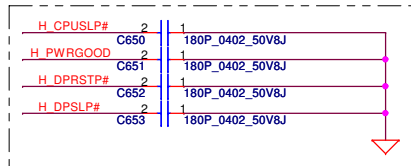
**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

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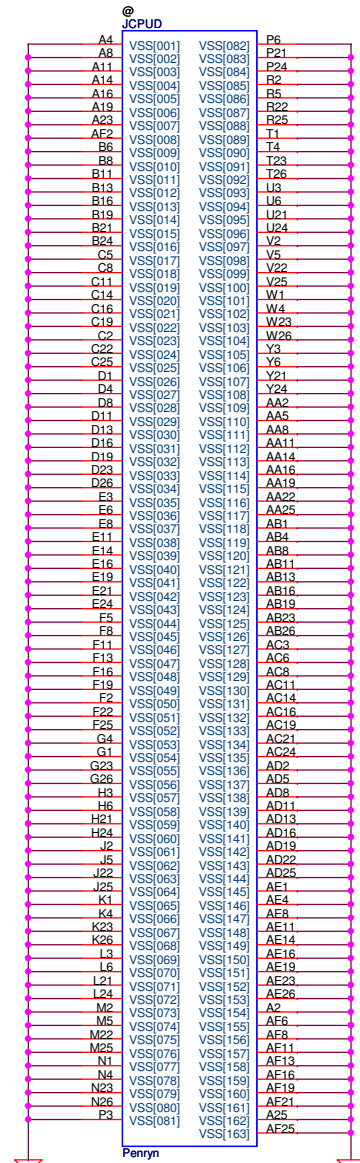


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

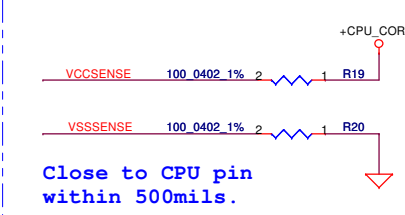
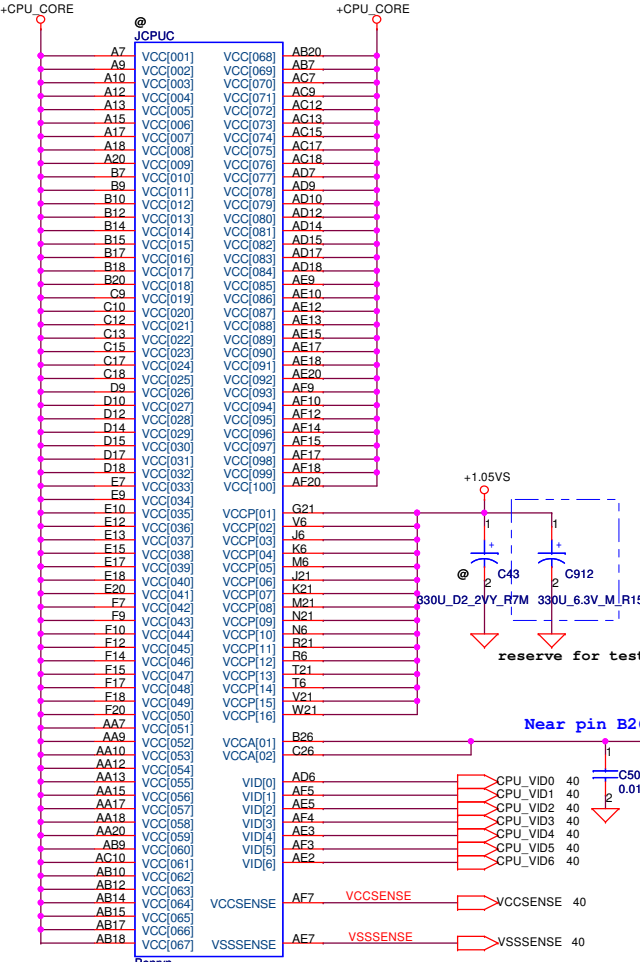
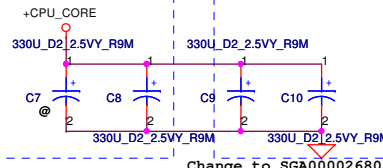


Reserve for debug close to CPU

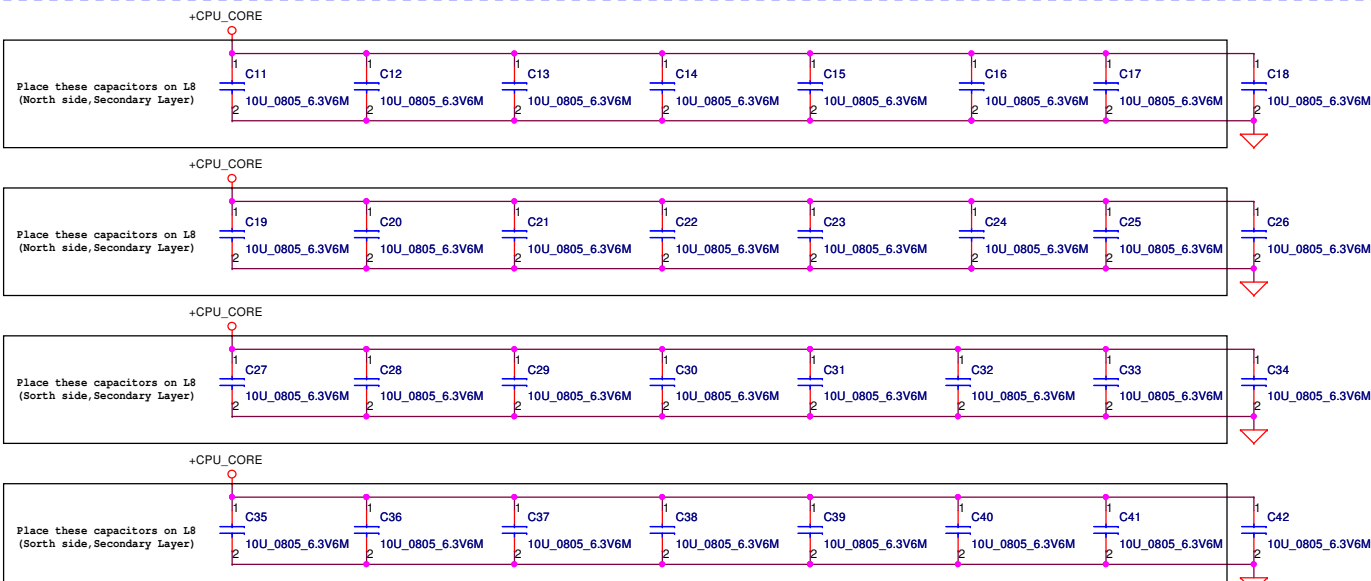


### Near CPU CORE regulator

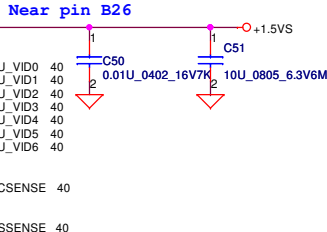
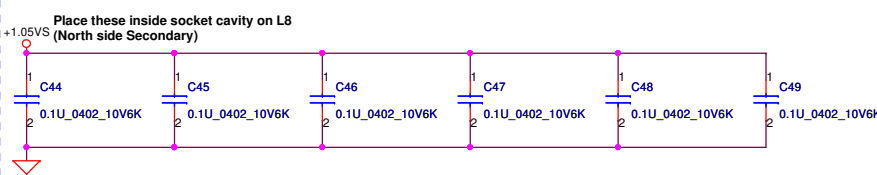
**ESR <= 1.5m ohm**  
**Capacitor > 1980uF**



Length match within 25 mils.  
The trace width/space/other is  
14/7/25.



## Mid Frequency Decoupling

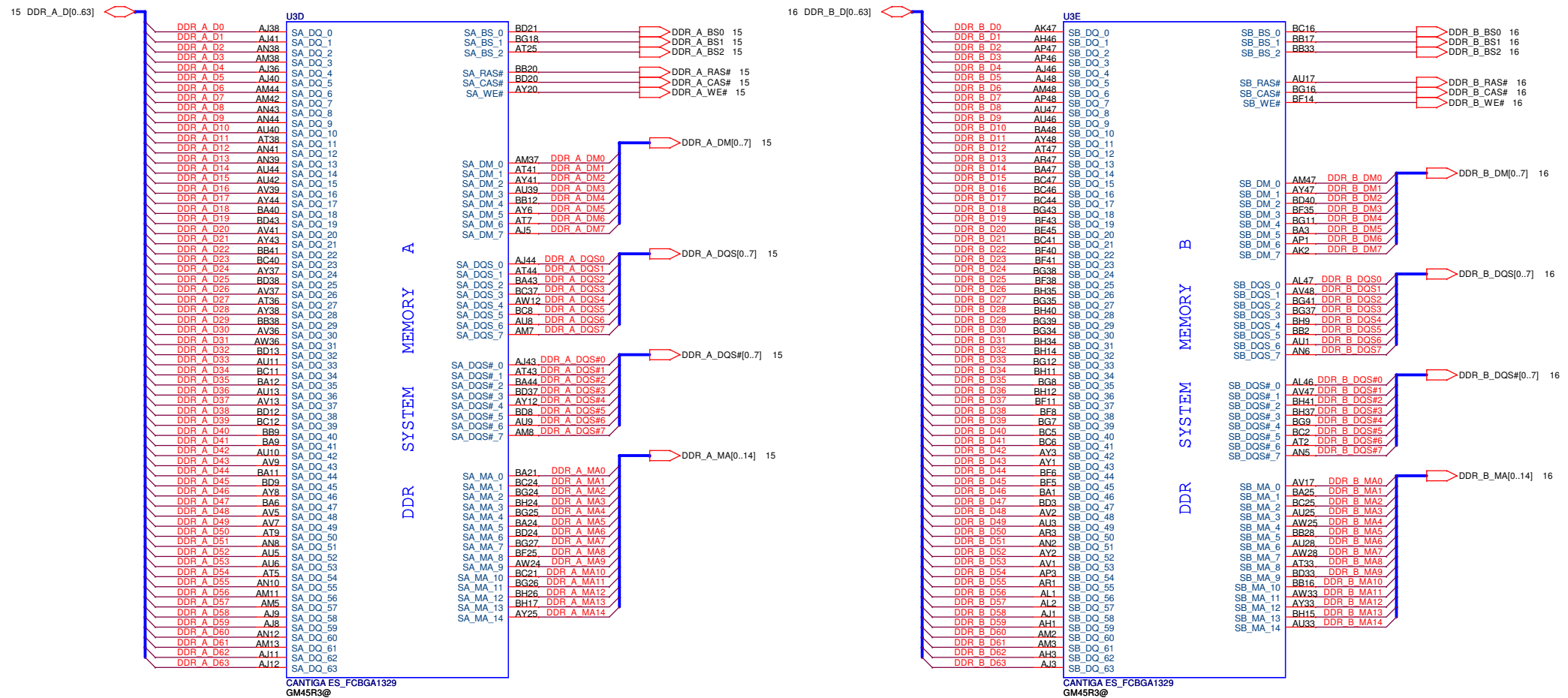


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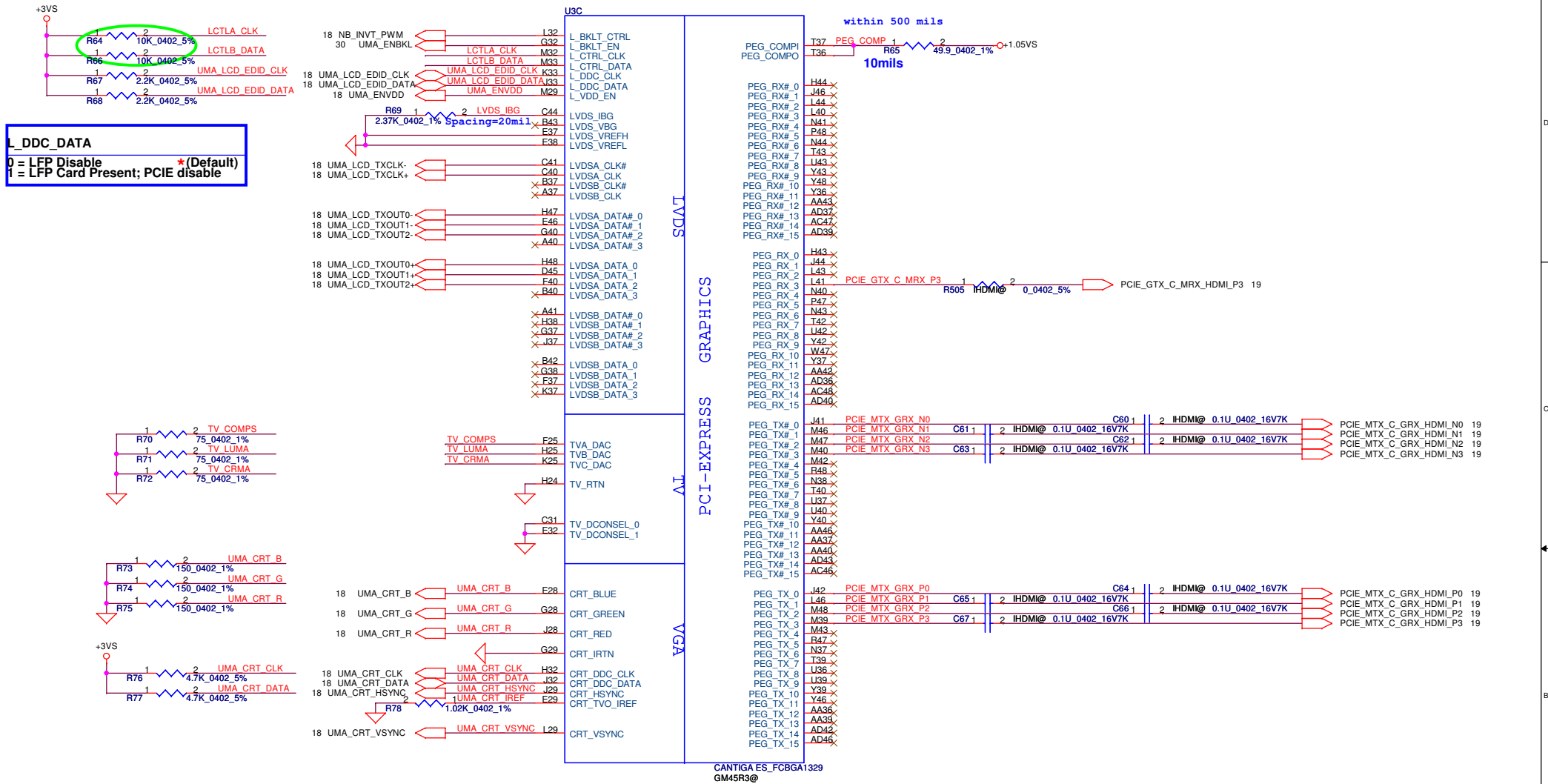




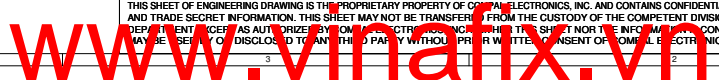


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**L\_DDC\_DATA**  
0 = LFP Disable  
1 = LFP Card Present; PCIE disable



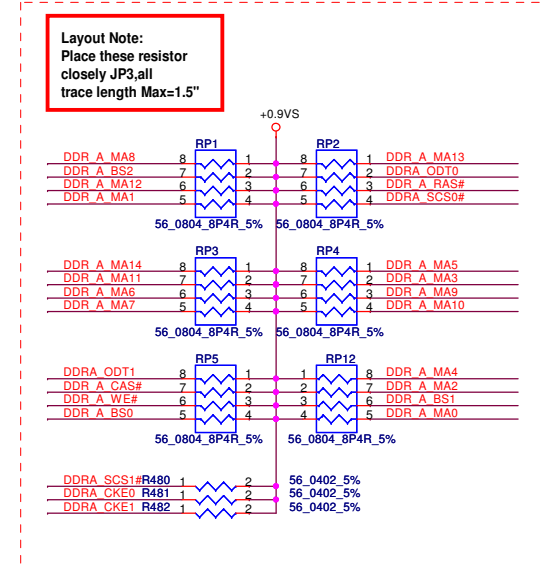
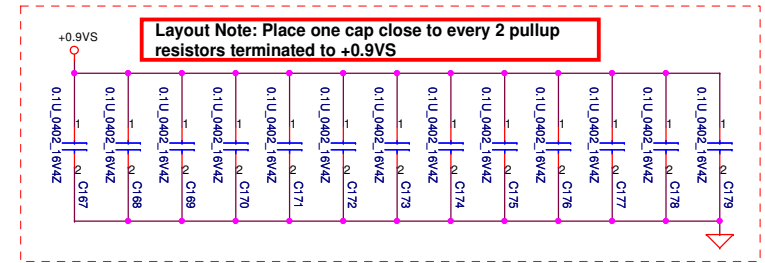
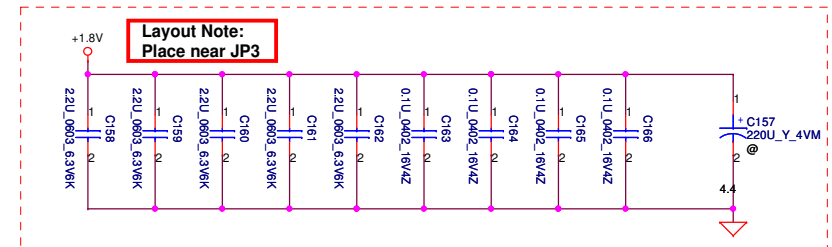
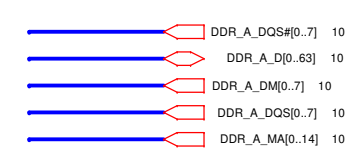
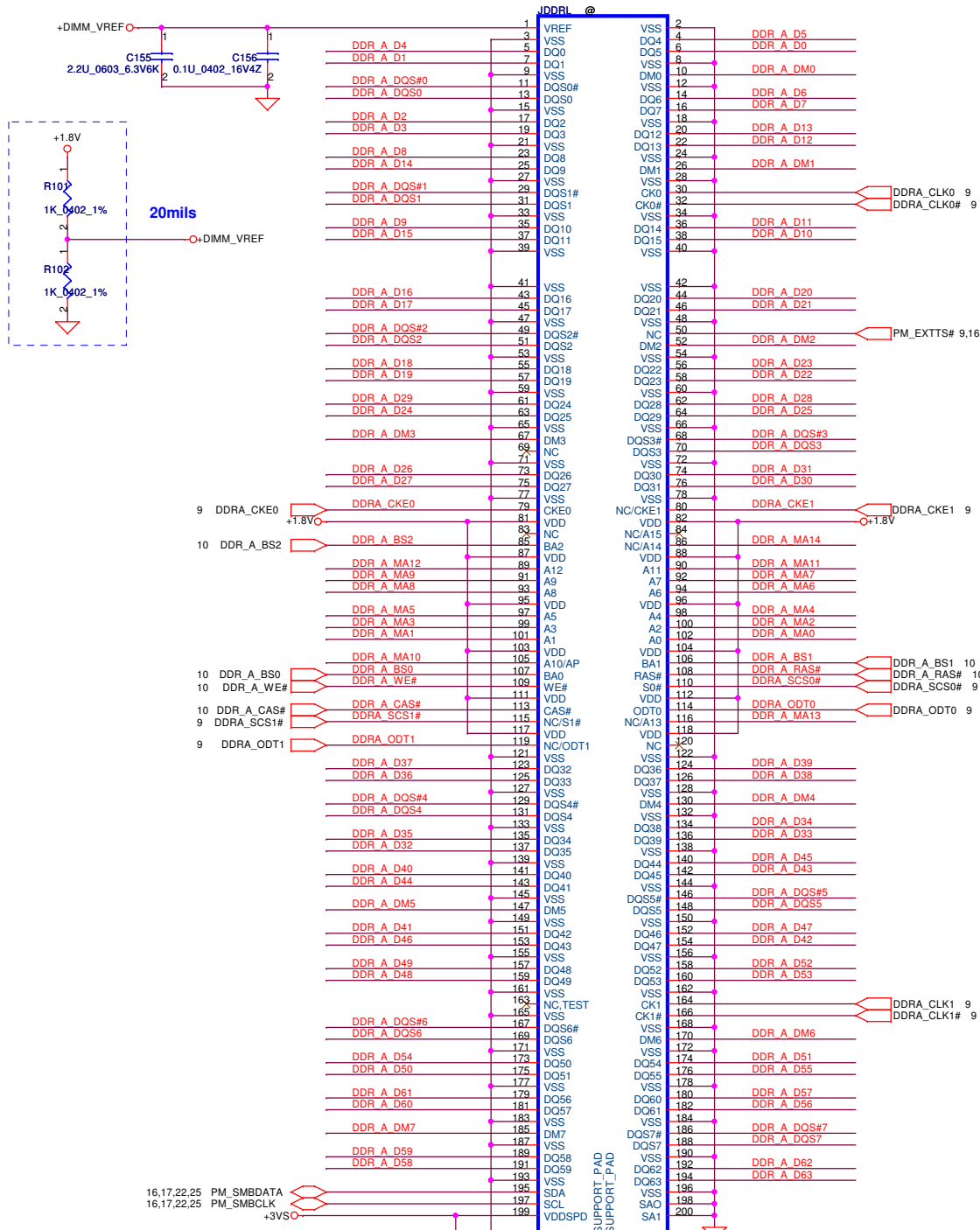






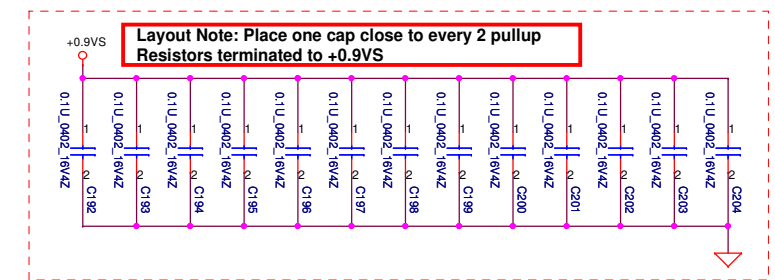
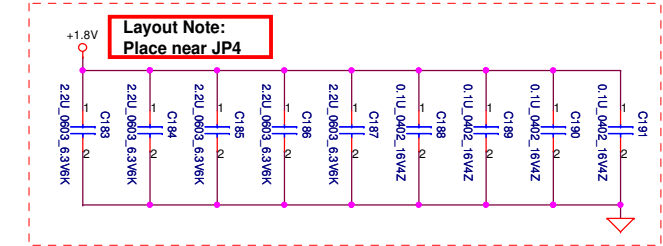
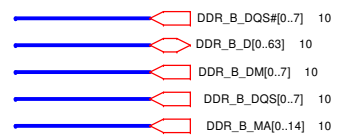
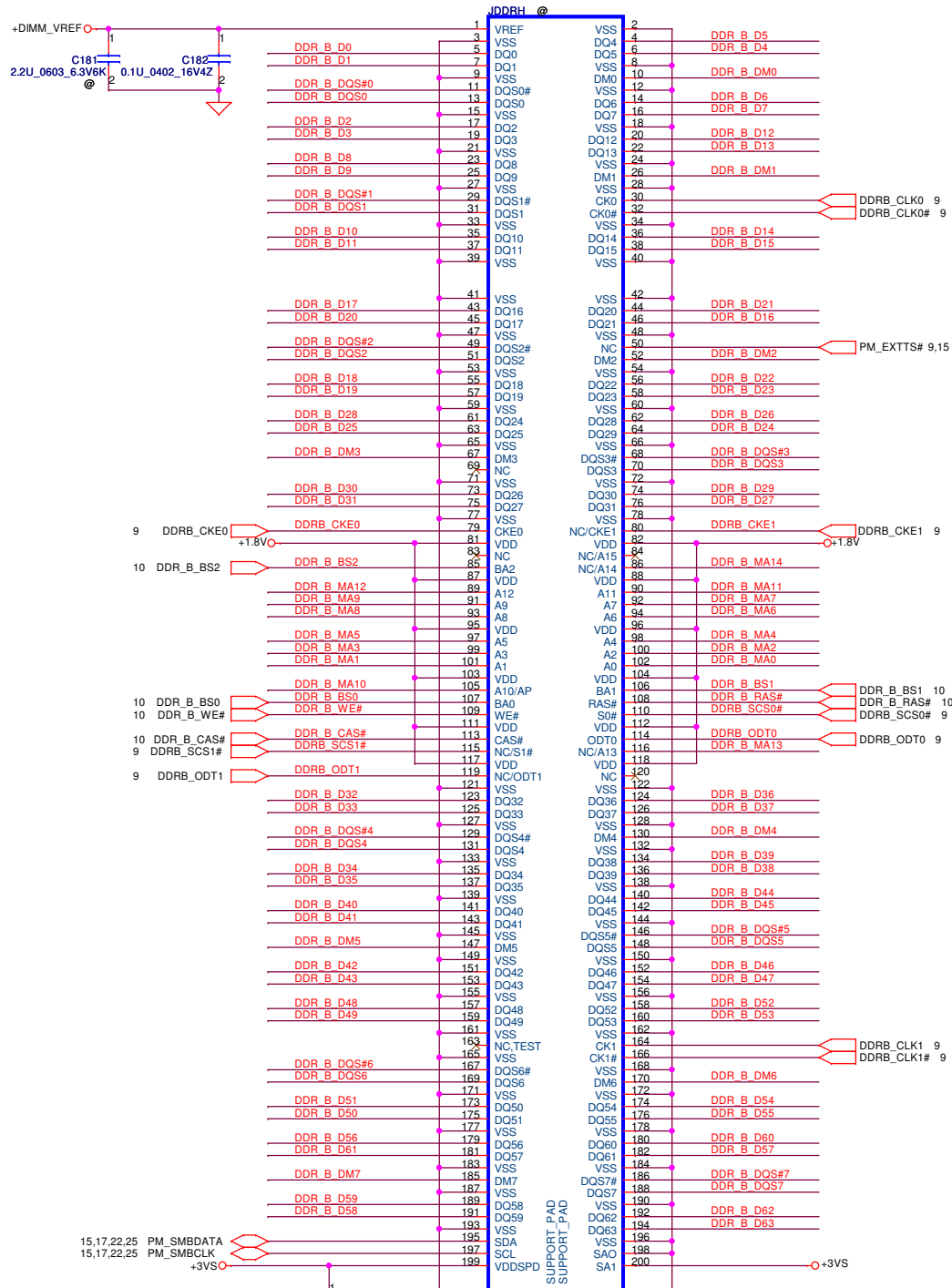


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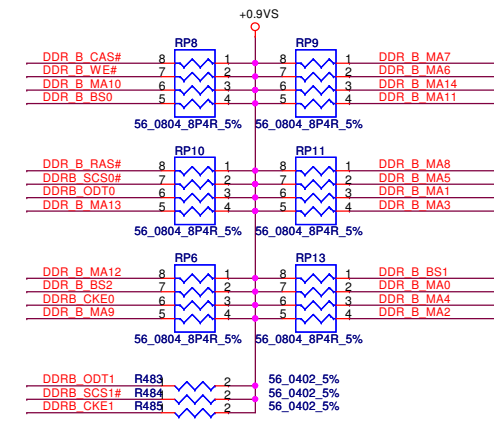


SO-DIMM A  
REVERSE  
Top side

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								DDRII-SODIMMO	
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Layout Note:  
Place these resistor  
closely JP4, all  
trace length Max=1.5"

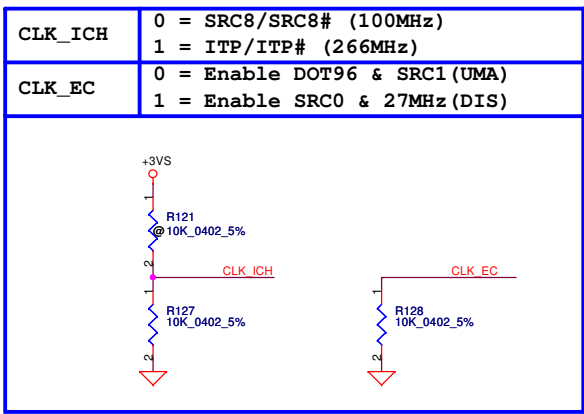
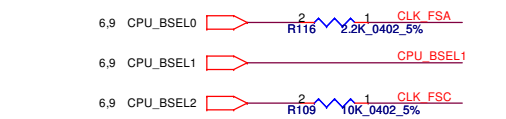
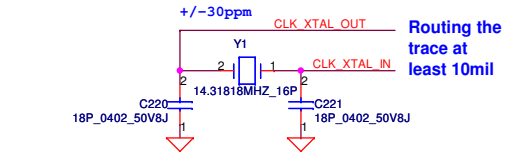
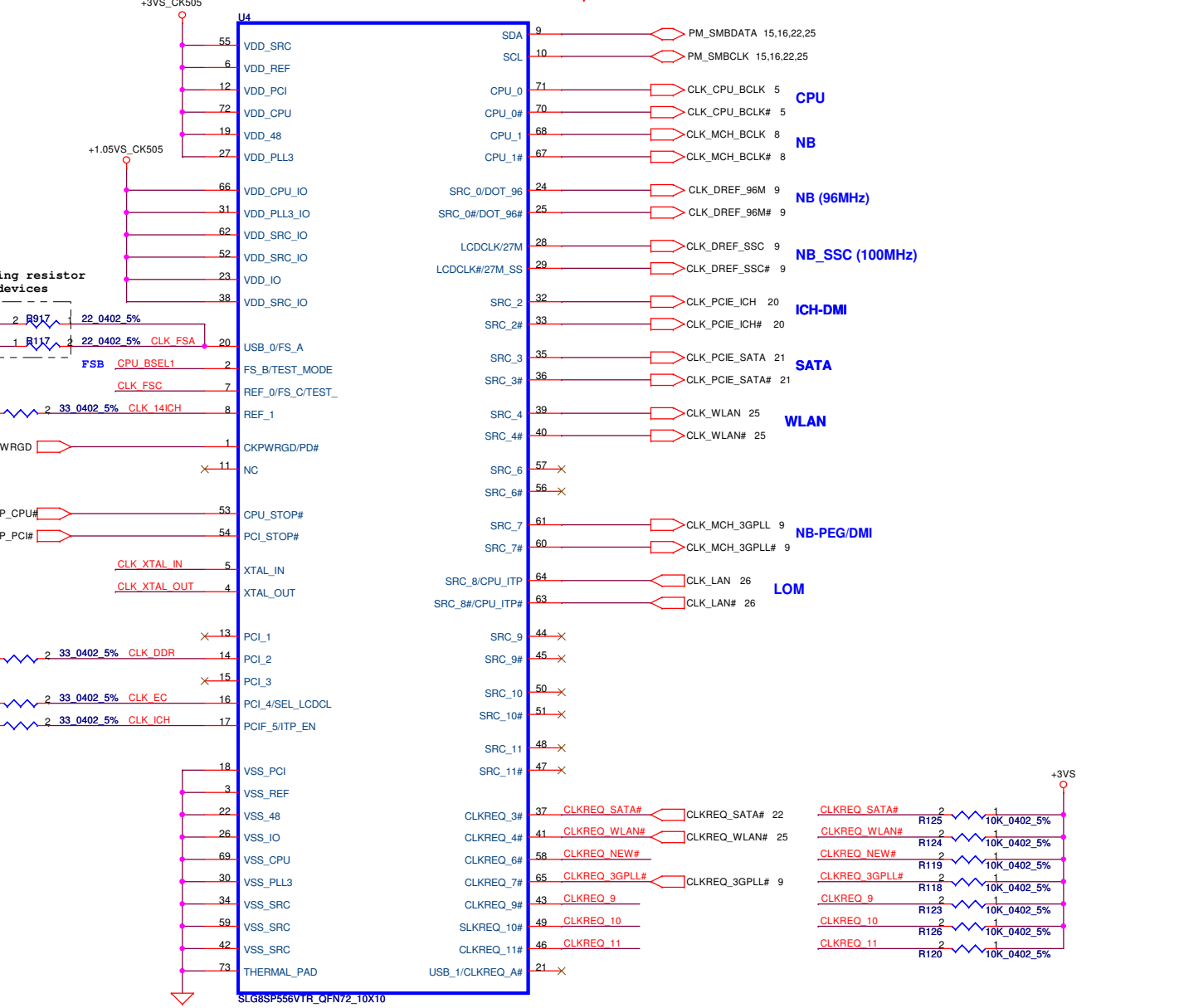
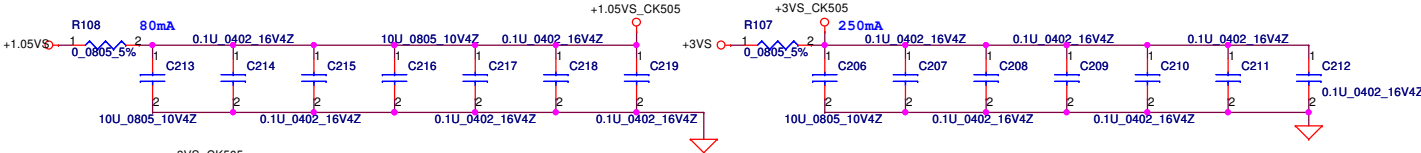


SO-DIMM B  
STANDARD  
Bottom side

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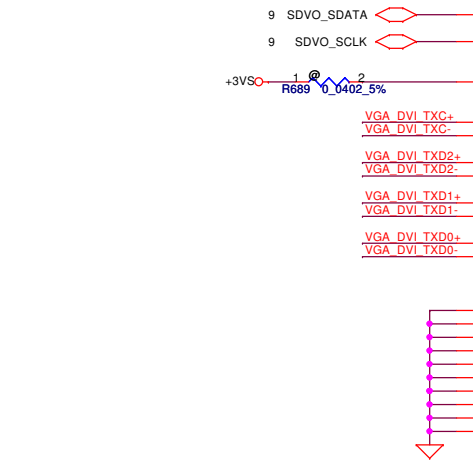
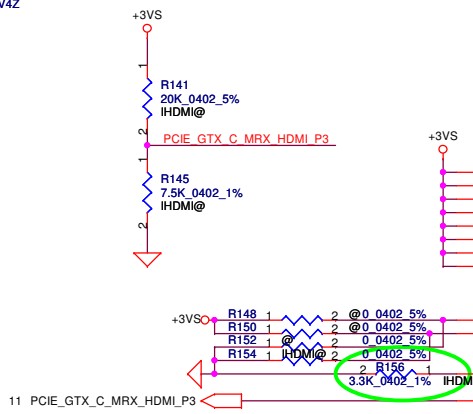
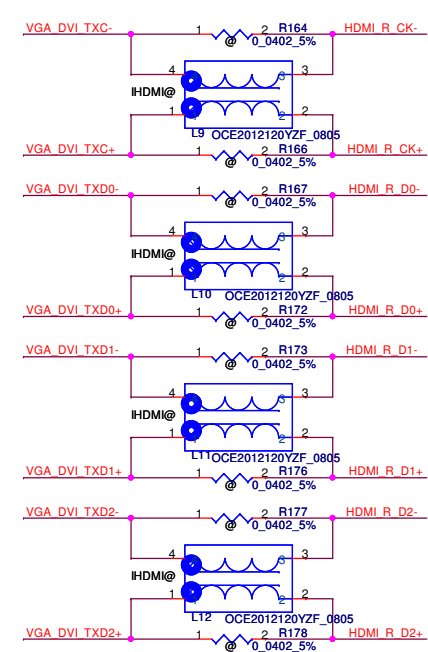
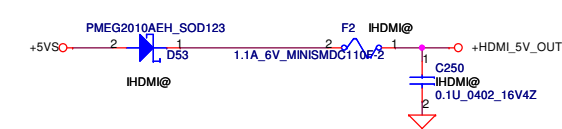
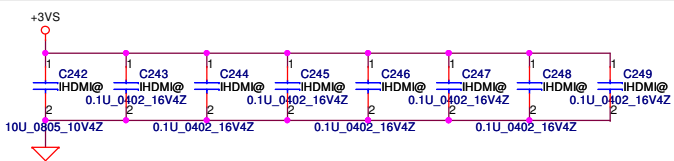


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

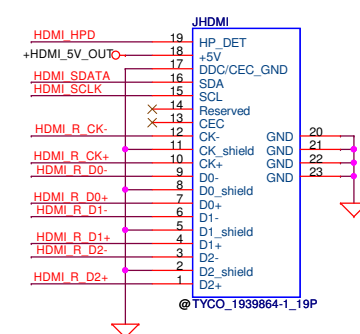


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## HDMI Connector



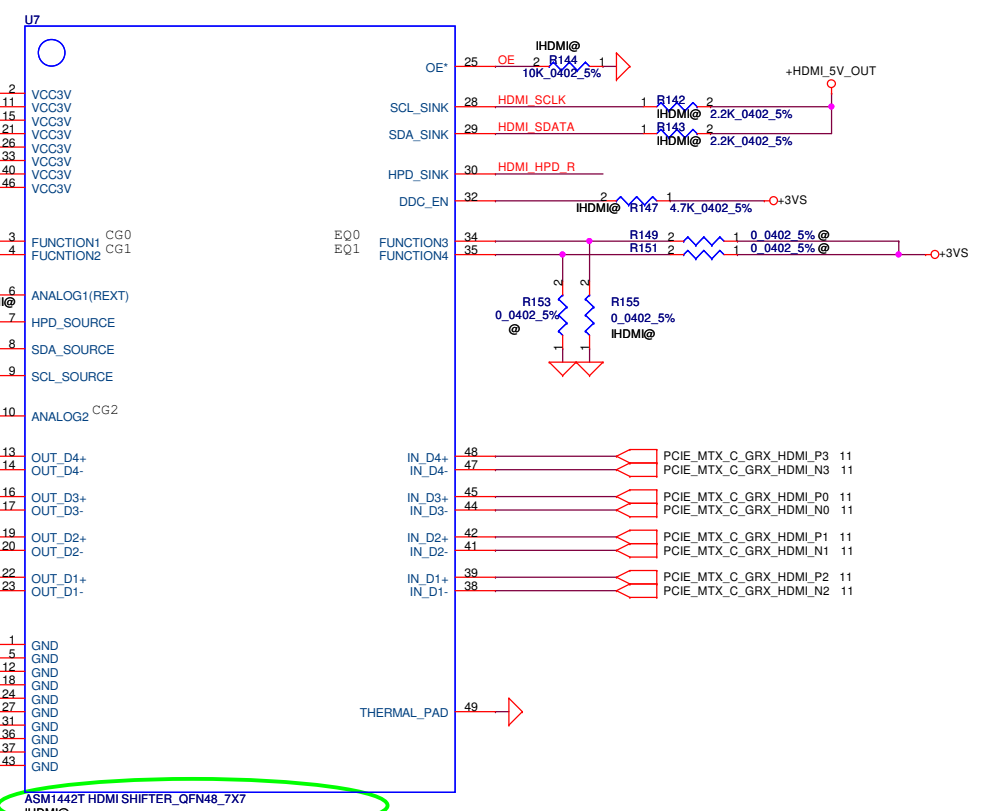
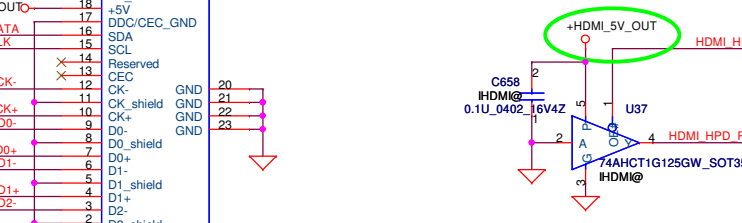
Vendor suggest un-mount for these.

VGA DVI TXC- R159 1 @ 2 1 2 VGA DVI TXC+ 68\_0402\_5% C251 0.5P\_0402\_50V8B

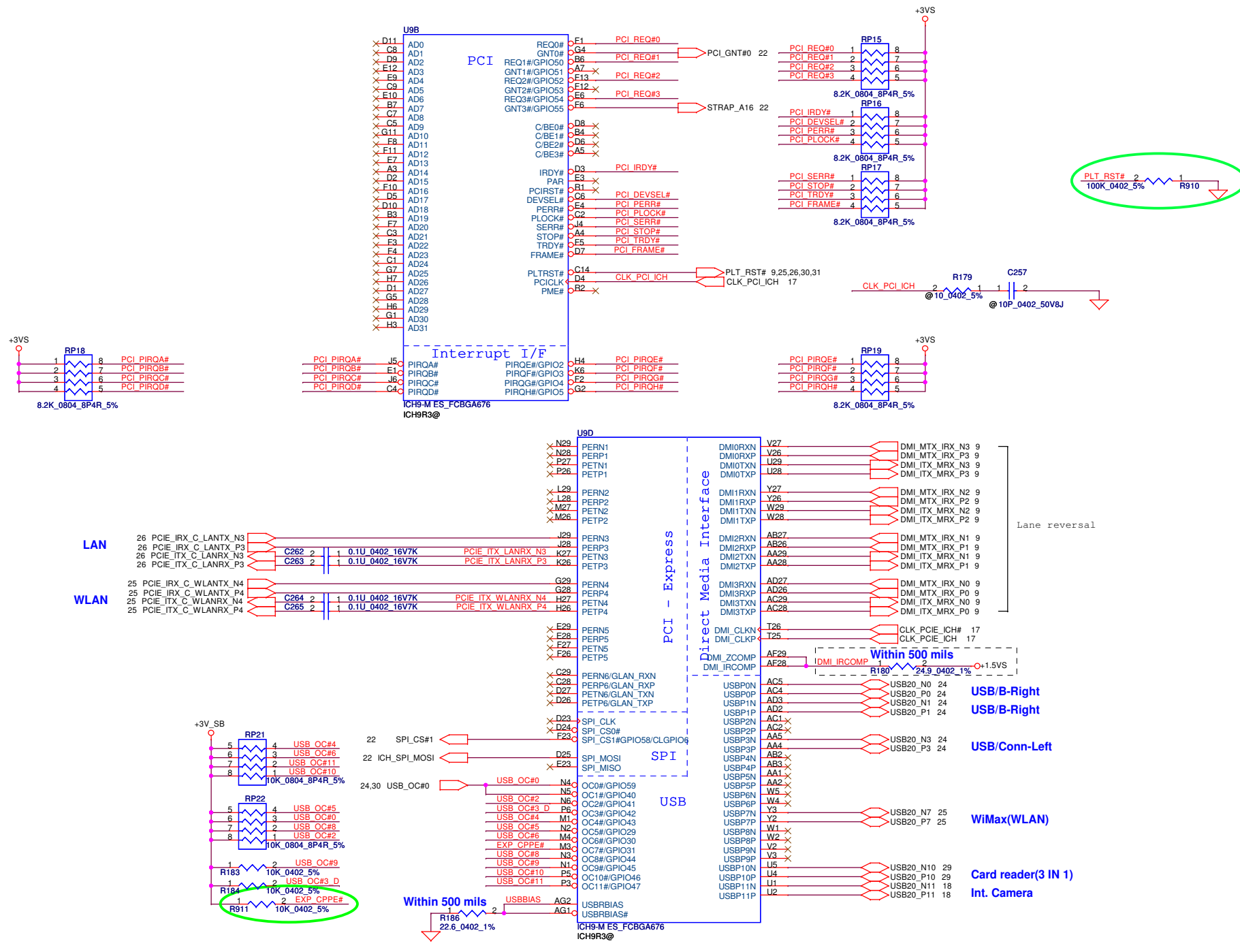
VGA DVI TXD2- R160 1 @ 2 1 2 VGA DVI TXD2+ 68\_0402\_5% C252 0.5P\_0402\_50V8B

VGA DVI TXD1- R161 1 @ 2 1 2 VGA DVI TXD1+ 68\_0402\_5% C253 0.5P\_0402\_50V8B

VGA DVI TXD0- R162 1 @ 2 1 2 VGA DVI TXD0+ 68\_0402\_5% C254 0.5P\_0402\_50V8B



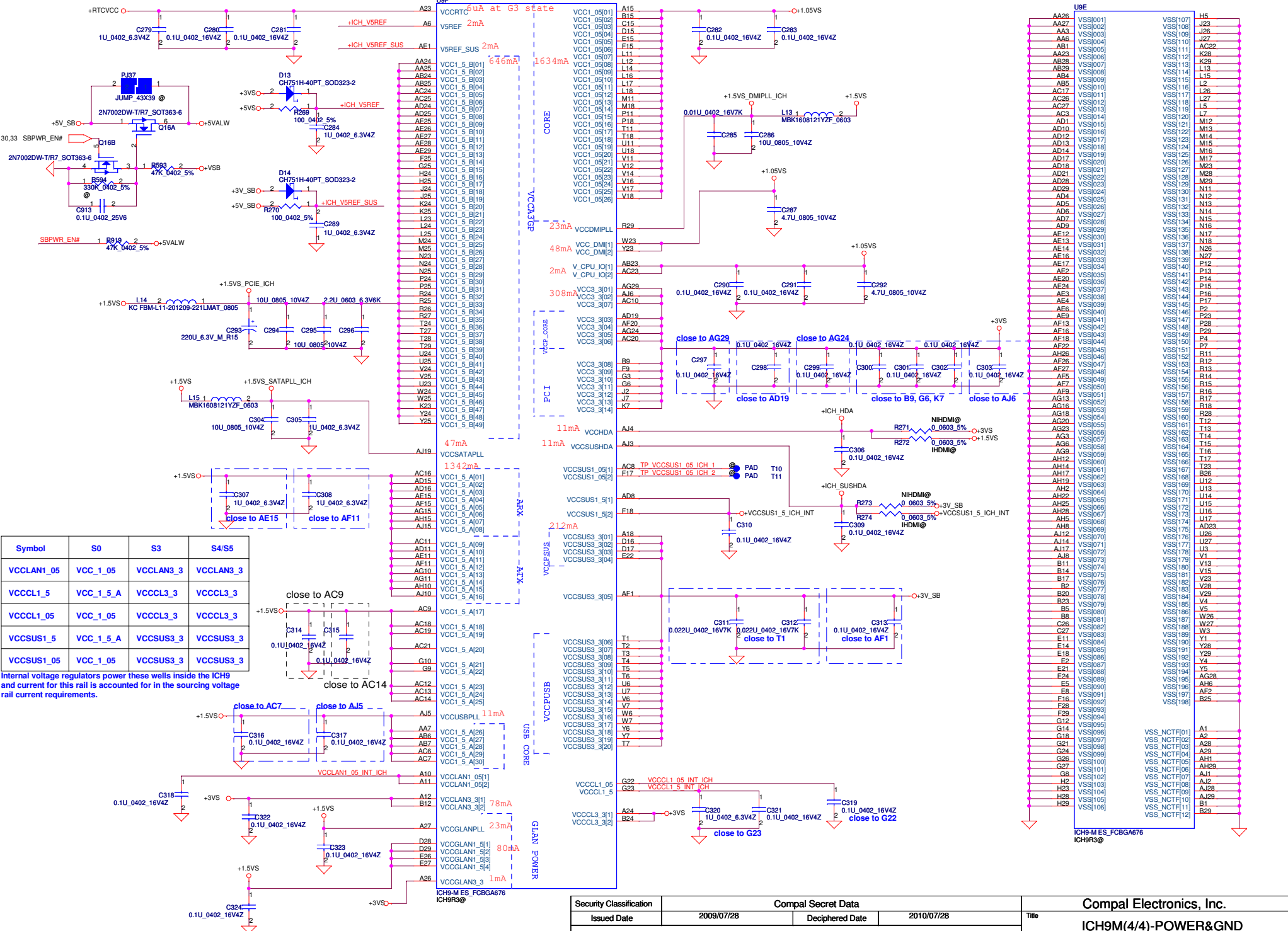
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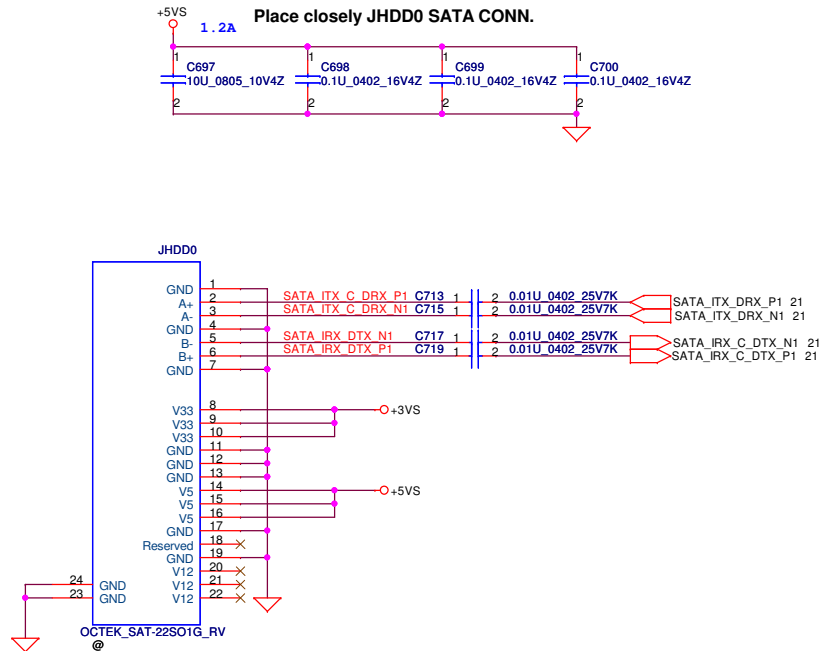




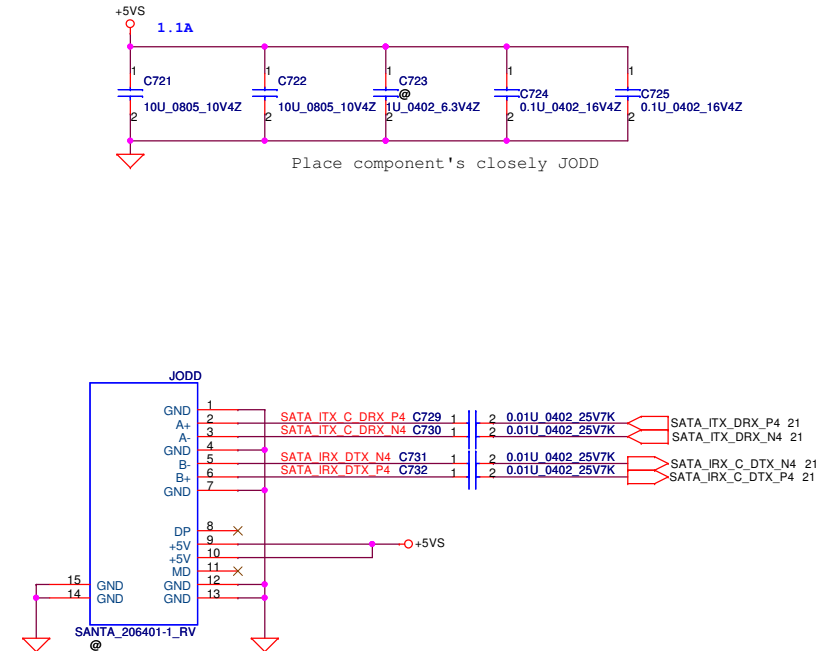
Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

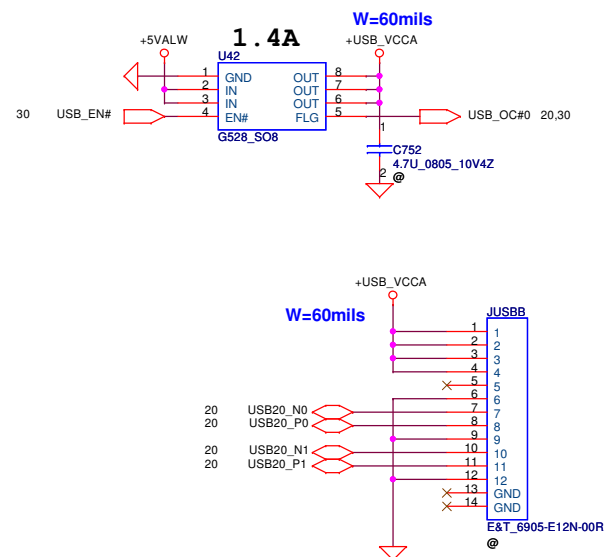
## SATA HDD Conn.



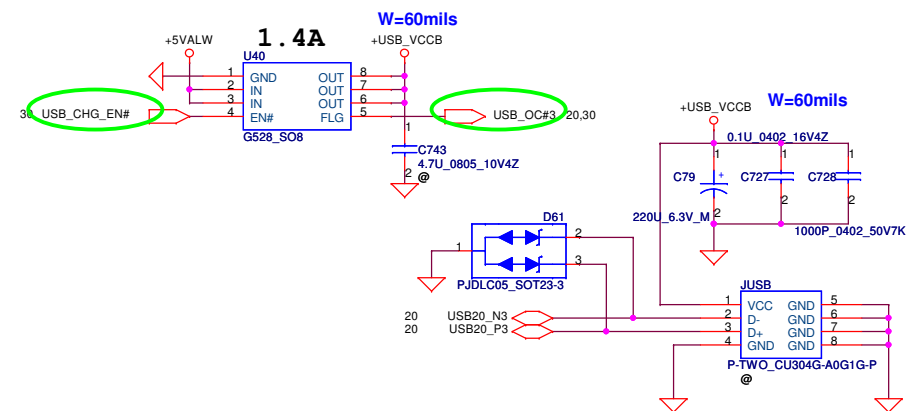
## SATA ODD Conn



## USB Board Conn



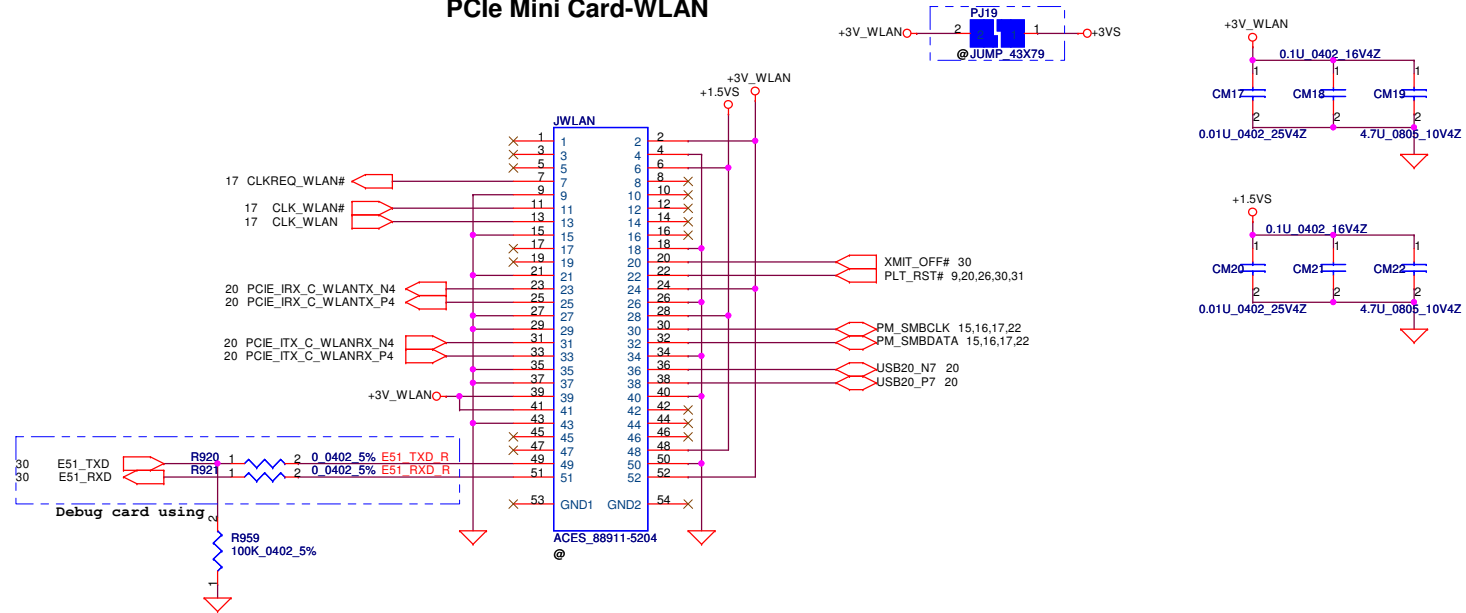
## USB Left Conn



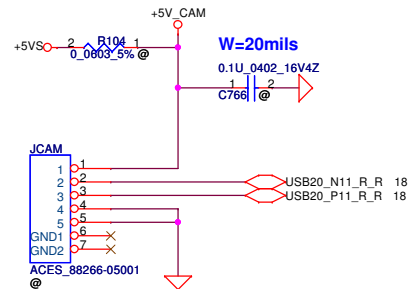
Security Classification				Compal Secret Data				Title	
Issued Date				2009/07/28		Deciphered Date		2010/07/28	
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						NBWAA LA5821P M/B		1.0	
				Date		Thursday, August 06, 2009		Sheet 24 of 41	



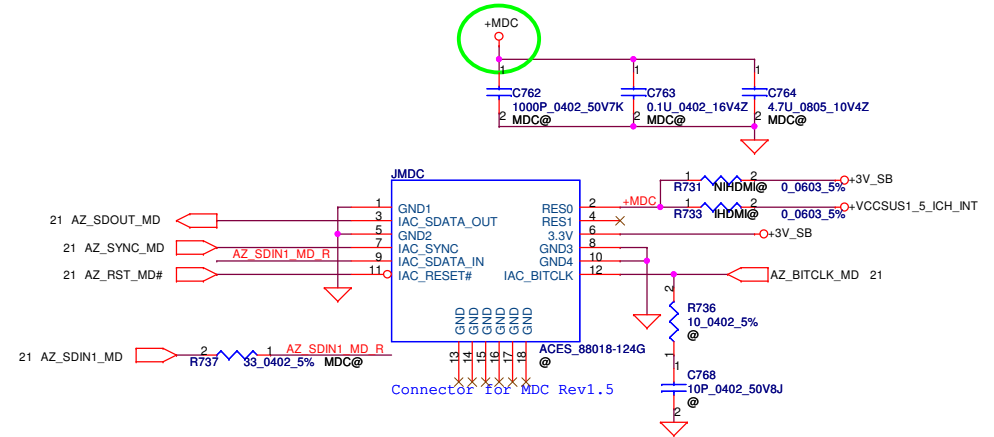
## PCIe Mini Card-WLAN



## Int. Camera



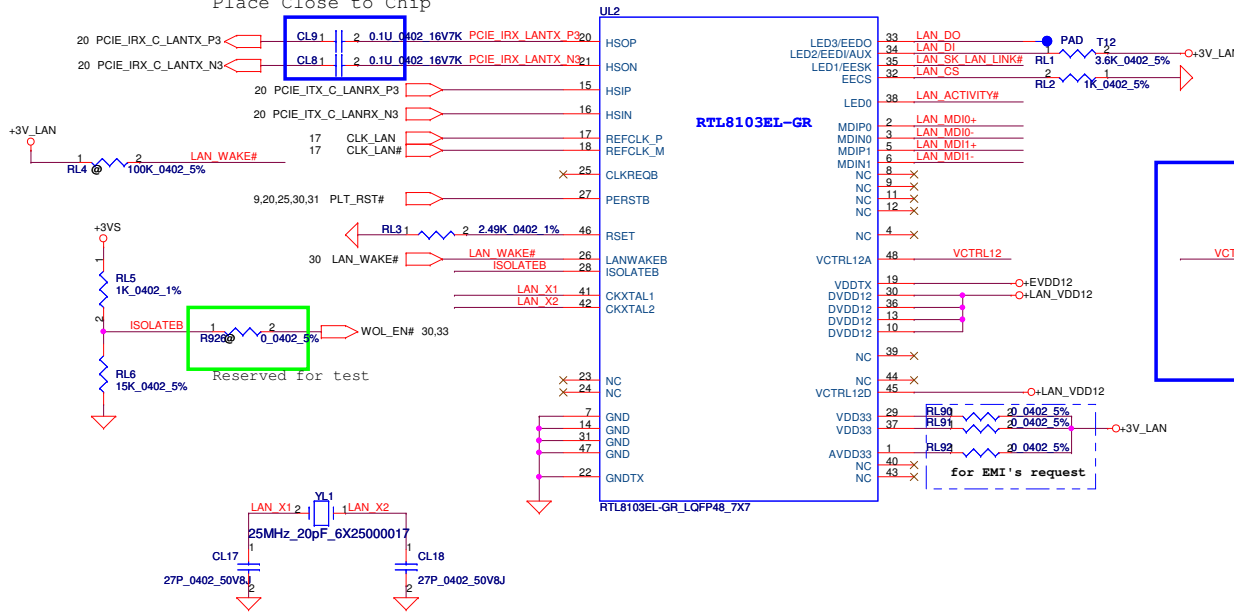
## MDC 1.5 Conn.



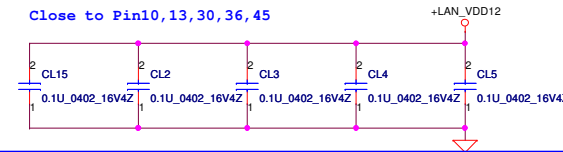
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2009/07/28		Deciphered Date	2010/07/28		Title
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				Size	Document Number	Rev
					<b>NBWAA LA5821P M/B</b>	<b>1.0</b>
				Date: <b>Monday, August 10, 2009</b>		
				Sheet <b>25</b> of <b>41</b>		

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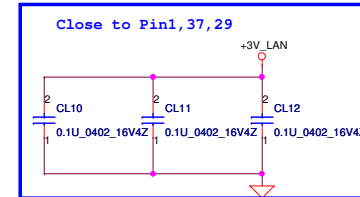
Place Close to Chip



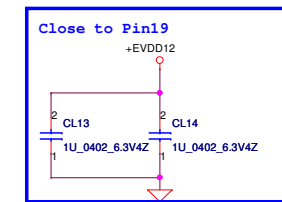
Close to Pin10,13,30,36,45



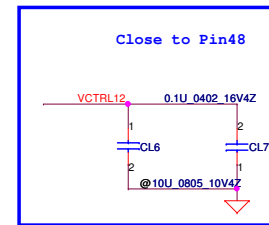
Close to Pin1,37,29



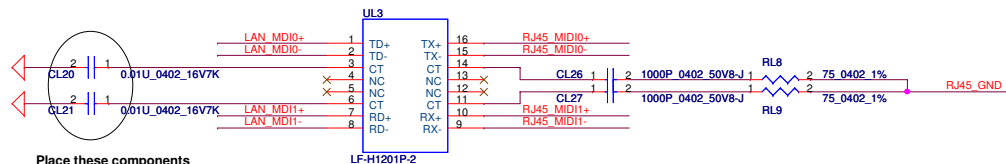
Close to Pin19



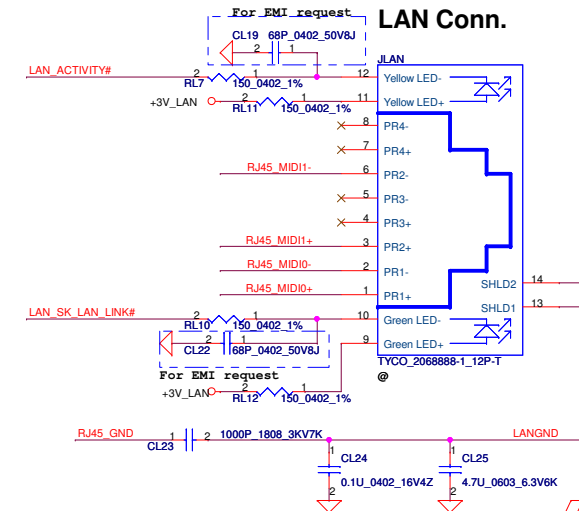
Close to Pin48



Place these components  
close to UL3

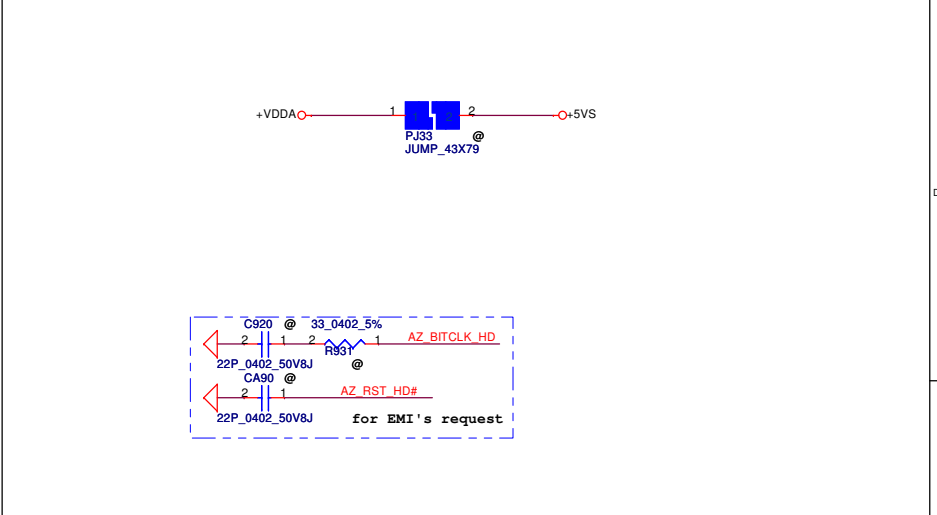
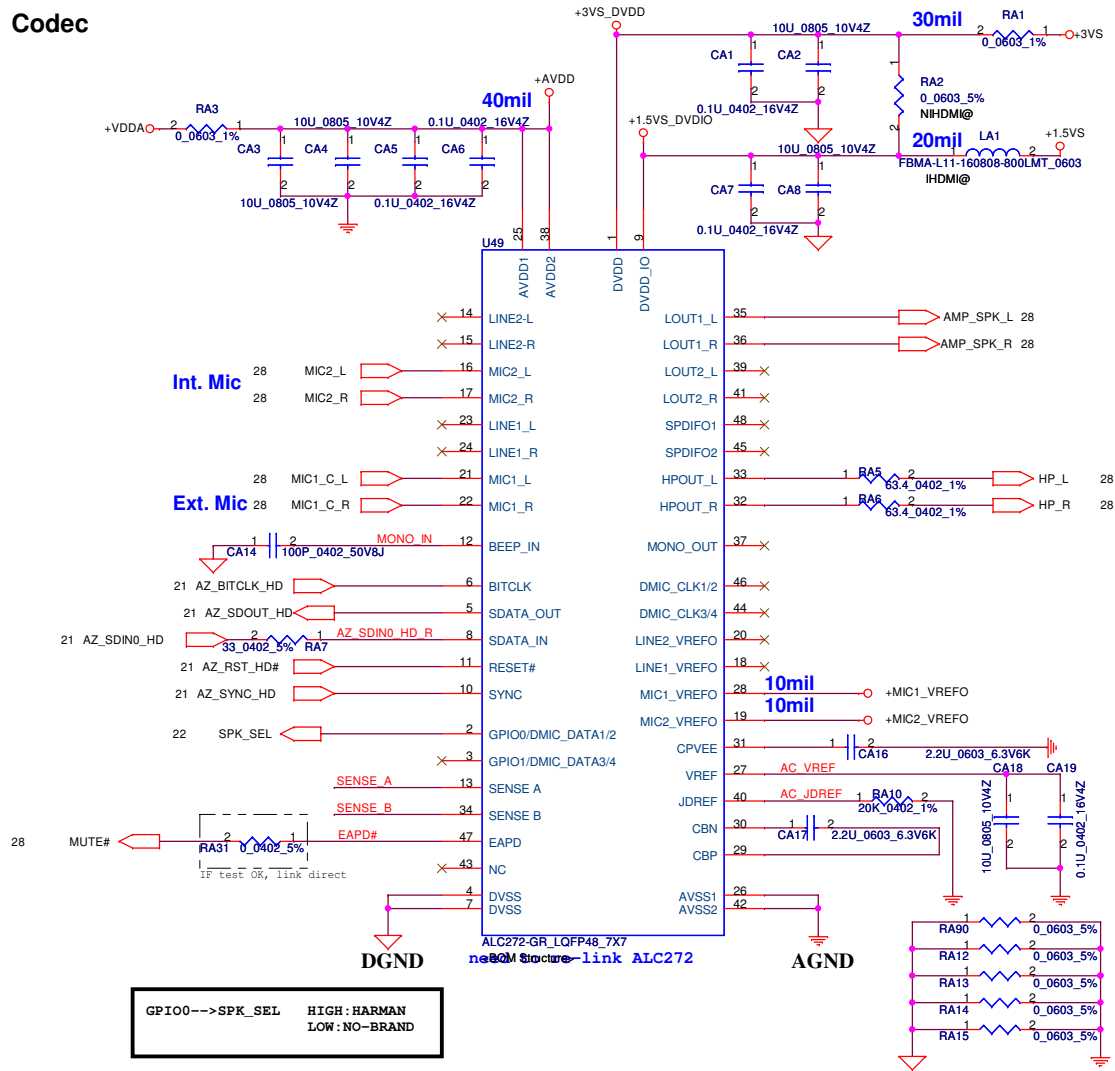


LAN Conn.

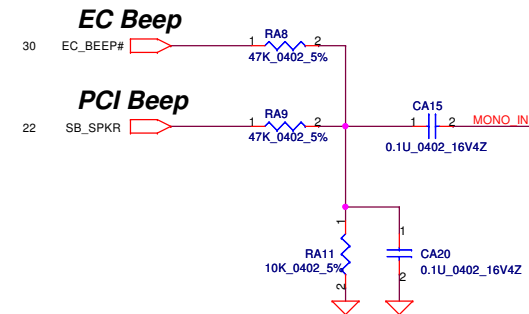


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Title				RTL8103EL 10/100 LAN				Rev			
Size				Document Number				1.0			
Customer				NBWAA LAS821P M/B							
Date				Thursday, August 06, 2009				Sheet 26 of 41			

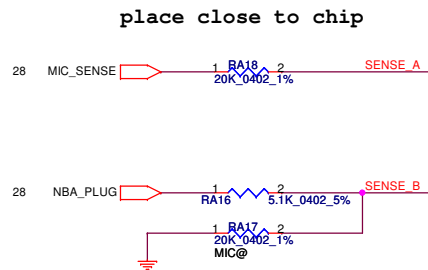
# Codec



## Beep sound



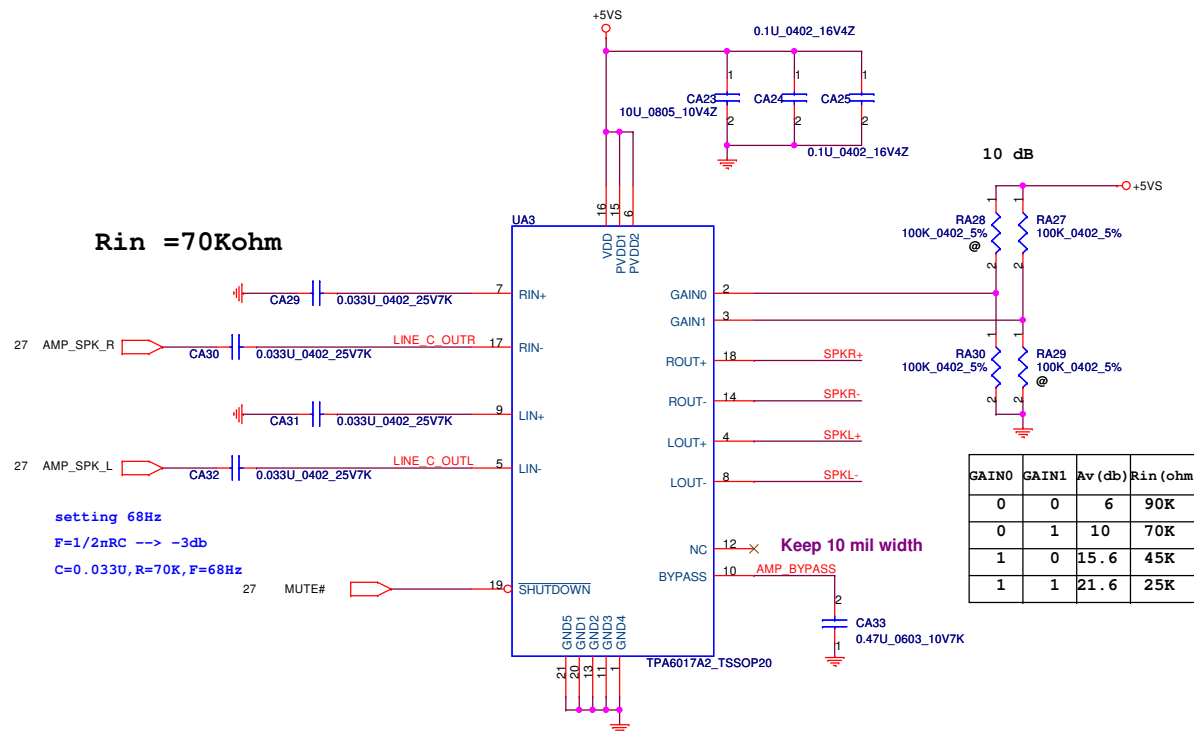
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



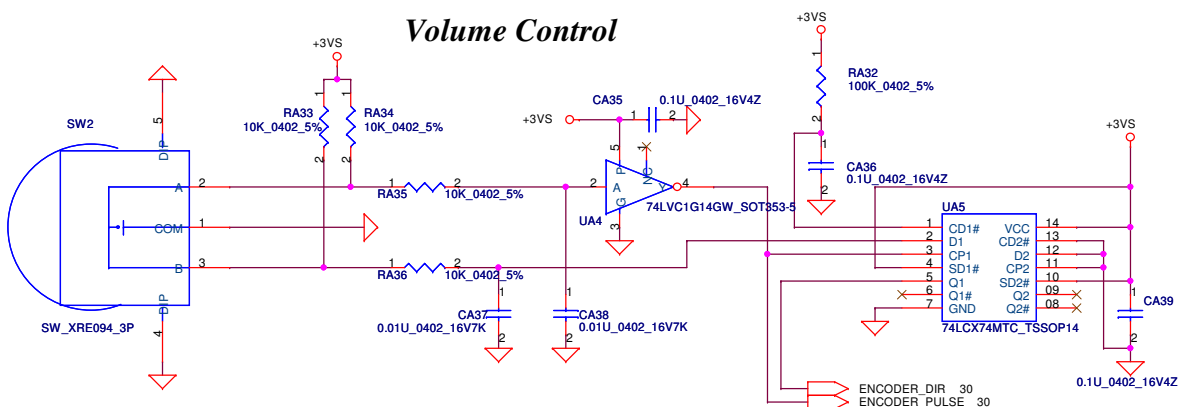
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/07/28				Title			
Deciphered Date				2010/07/28				HD CODEC ALC272			
Size				Document Number				NBWAA LA5821P M/B			
Date				Monday, August 10, 2009				Sheet 27 of 41			

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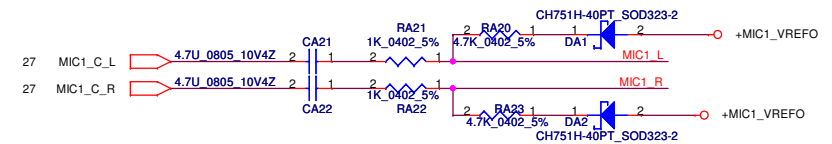
## TPA6017 Medium Range Amplifier



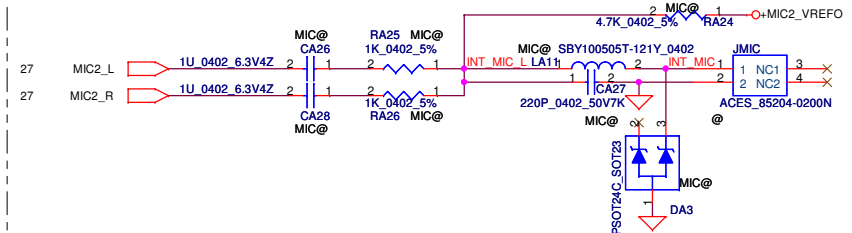
## Volume Control



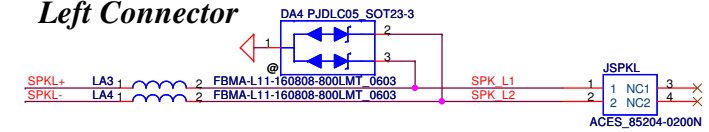
## Ext. Mic



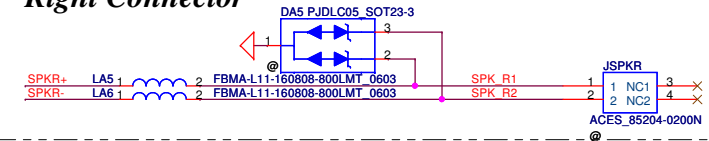
## Int. Mic



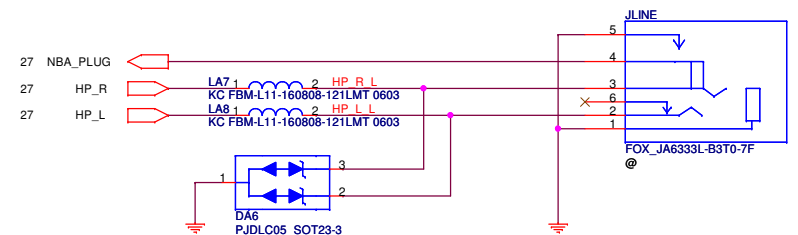
## Left Connector



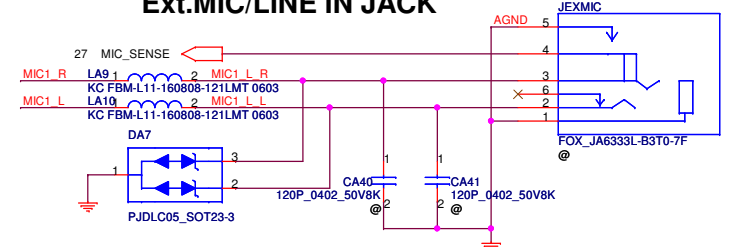
## Right Connector



## HeadPhone/LINE Out JACK

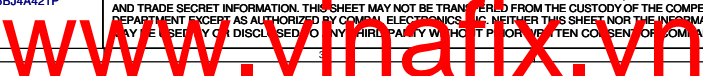


## Ext.MIC/LINE IN JACK



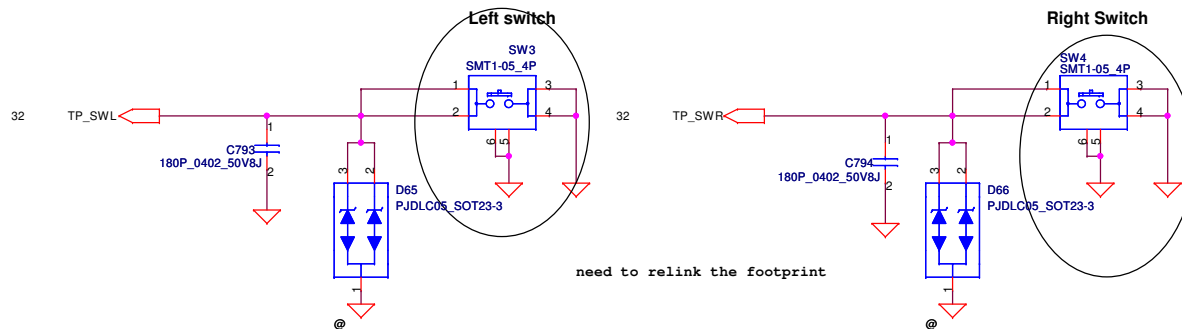
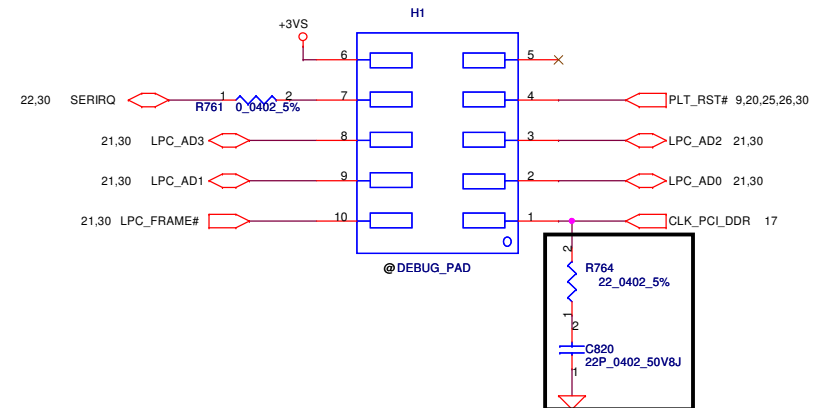
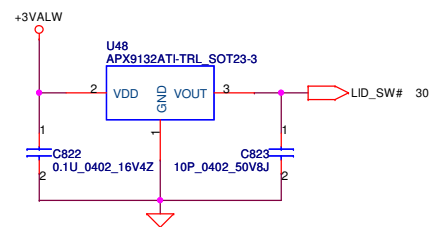
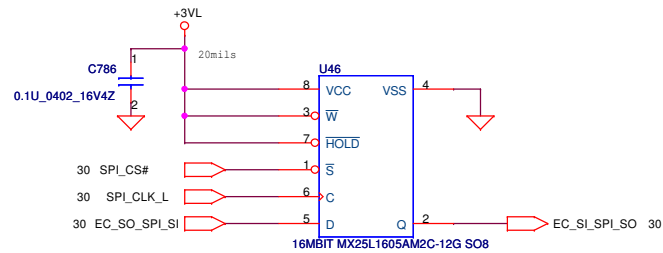
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				Date	Thursday, August 06, 2009
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				Rev	1.0



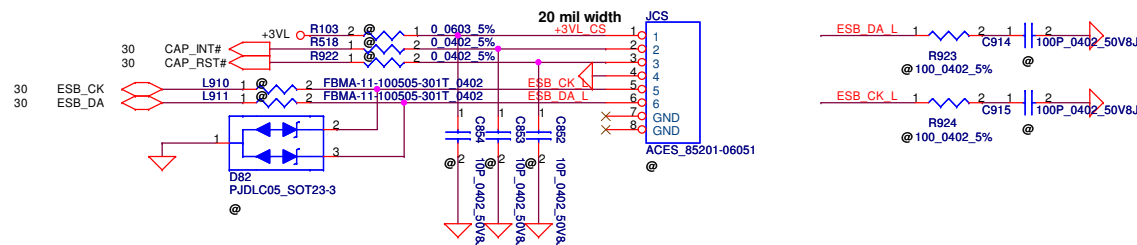


## LPC Debug Port

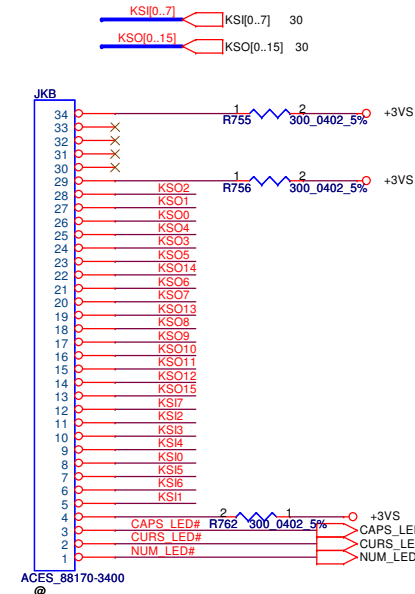
Please place the PAD under DDR DIMM.



## CS/B Connector



KEYBOARD  
CONN.



please close to JKB

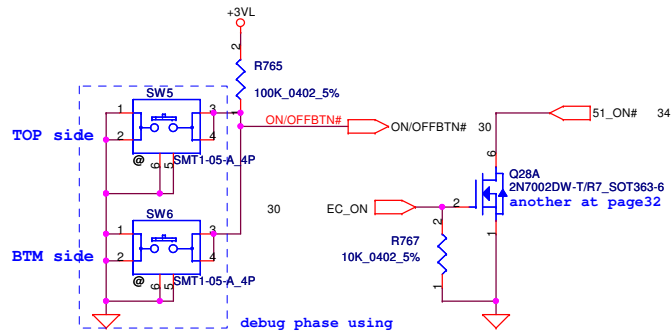
KSO2	1	2	
KSO1	1	2	100P_0402_50V8J
KSO0	1	2	
KSO4	1	2	100P_0402_50V8J
KSO3	1	2	
KSO5	1	2	100P_0402_50V8J
KSO6	1	2	
KSO7	1	2	100P_0402_50V8J
KSO13	1	2	
KSO8	1	2	100P_0402_50V8J
KSO9	1	2	
KSO10	1	2	100P_0402_50V8J
KSO11	1	2	
KSO12	1	2	100P_0402_50V8J
KSO15	1	2	
KS17	1	2	100P_0402_50V8J
KS12	1	2	
KS13	1	2	100P_0402_50V8J
KS14	1	2	
KS10	1	2	100P_0402_50V8J
KS15	1	2	
KS16	1	2	100P_0402_50V8J
KS11	1	2	
CAPS_LED#	1	2	100P_0402_50V8J
CURS_LED#	1	2	
NUM_LED#	1	2	100P_0402_50V8J
	1	2	

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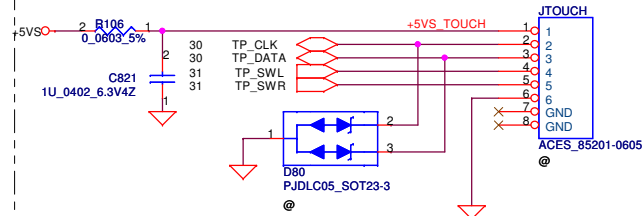
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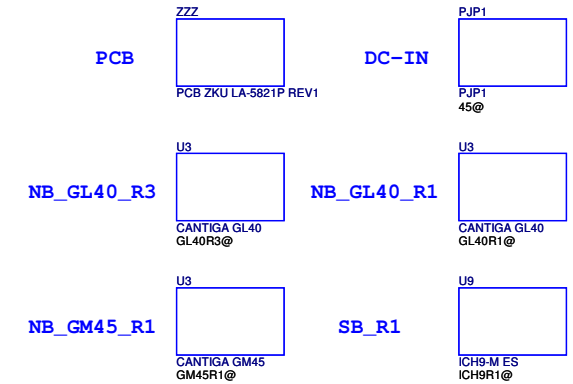
## Power Button



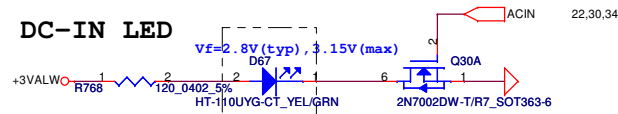
## Touch Pad Connector



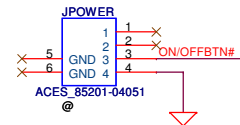
## ISPD



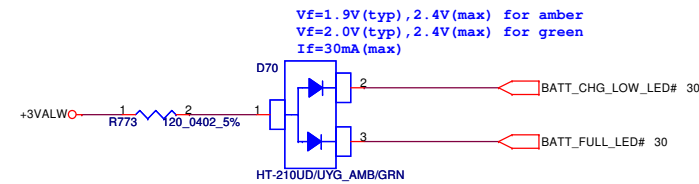
## DC-IN LED



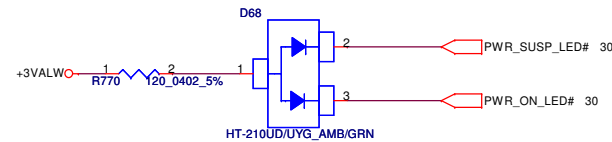
## PWR/B



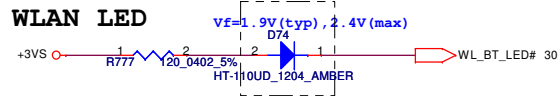
## BATT CHARGE/FULL LED



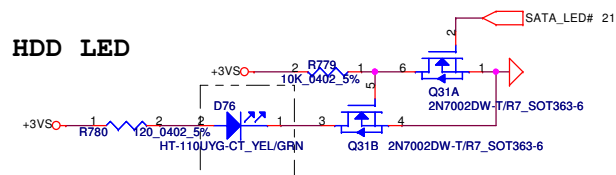
## POWER/SUSPEND LED



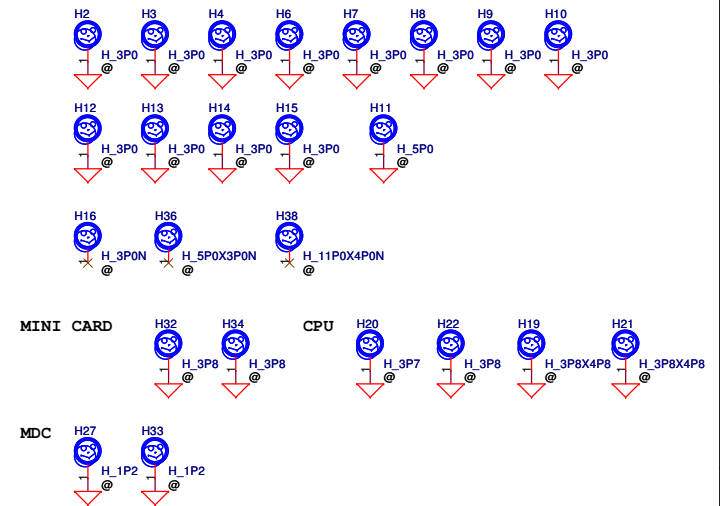
## WLAN LED



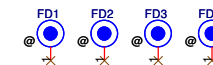
## HDD LED



## Screw Hole

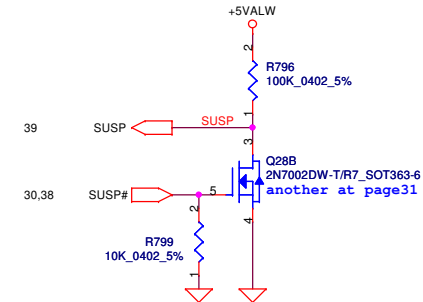
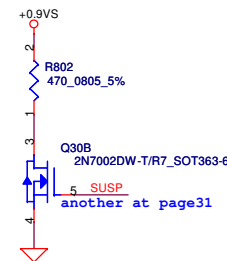
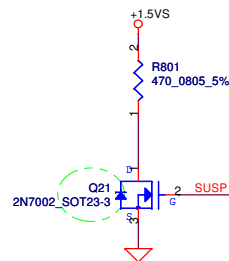
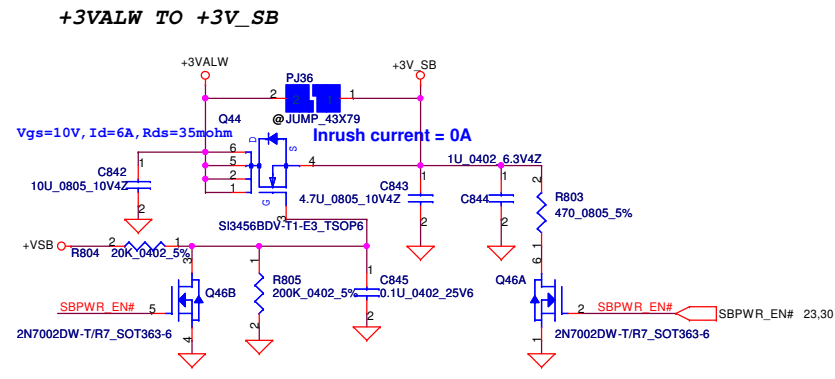
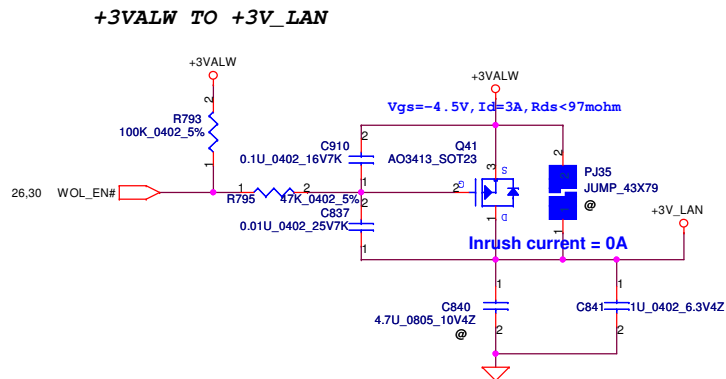
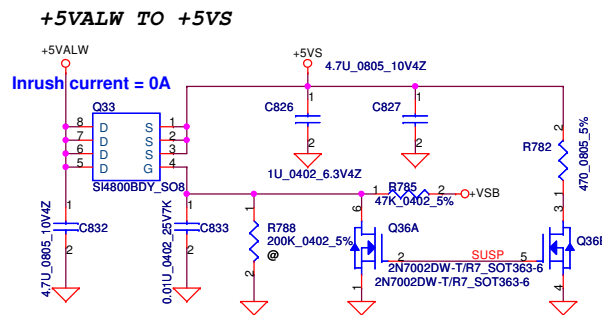
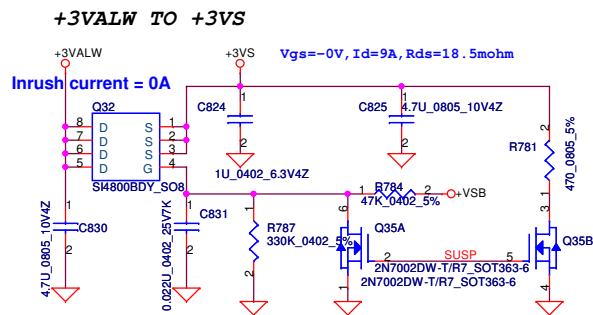


## PCB Federal Mark PAD



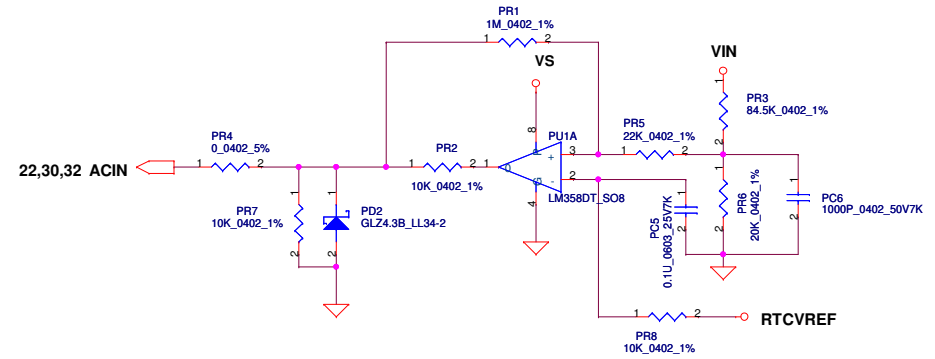
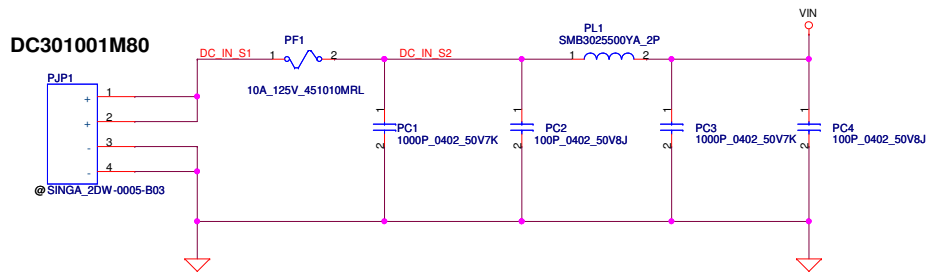
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Size	Document Number	NBWAA LA5821P M/B		Rev	1.0
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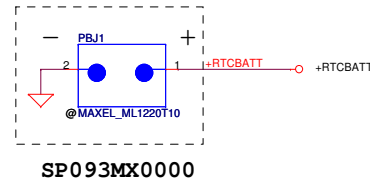
# DC301001M80



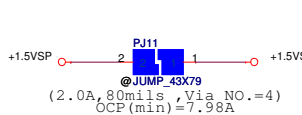
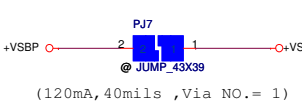
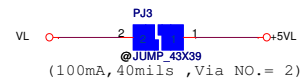
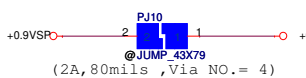
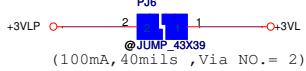
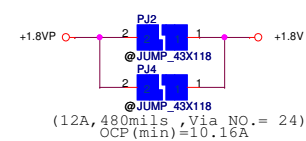
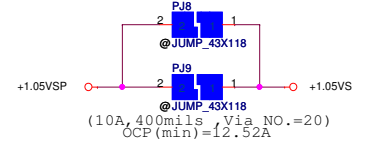
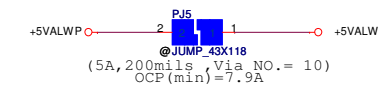
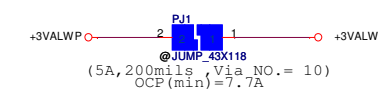
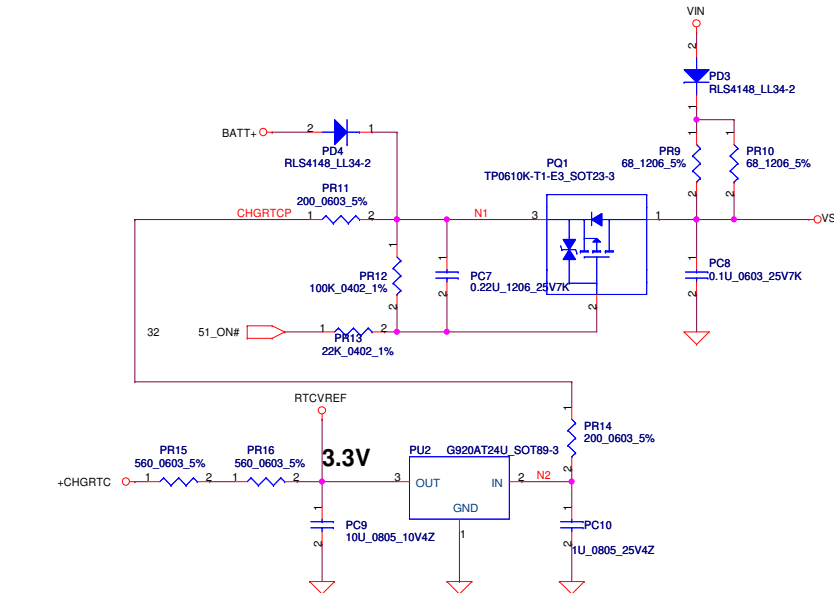
## Vin Detector

High	18.384	17.901	17.430
Low	17.728	17.257	16.976

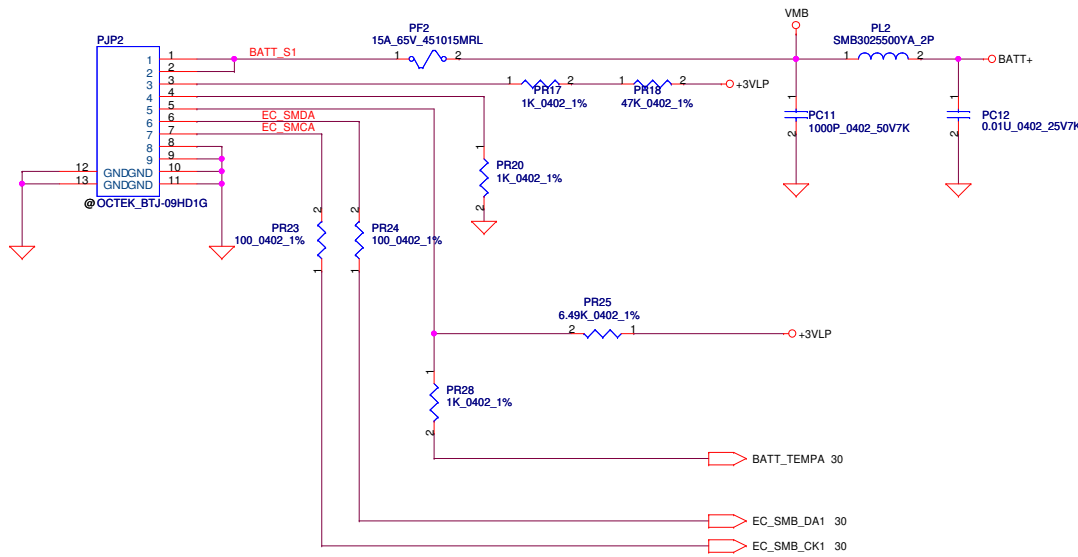
## RTC Battery



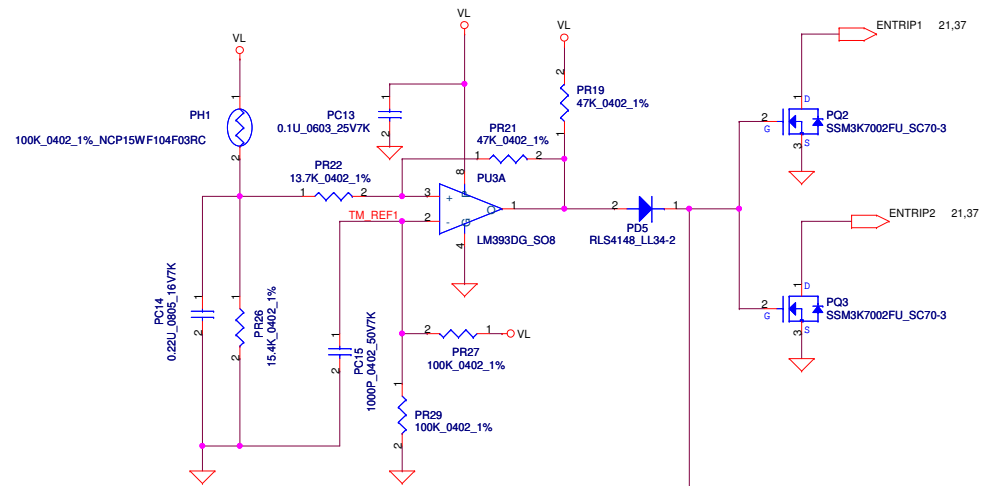
SP093MX0000



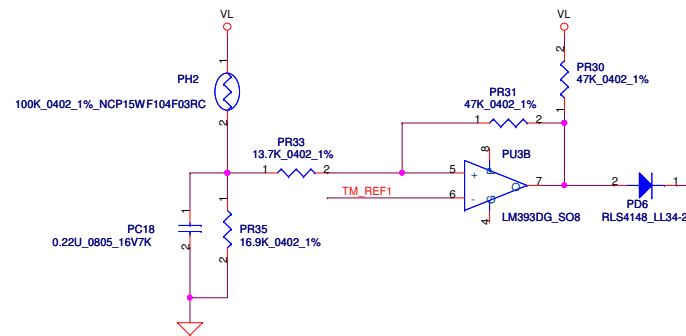
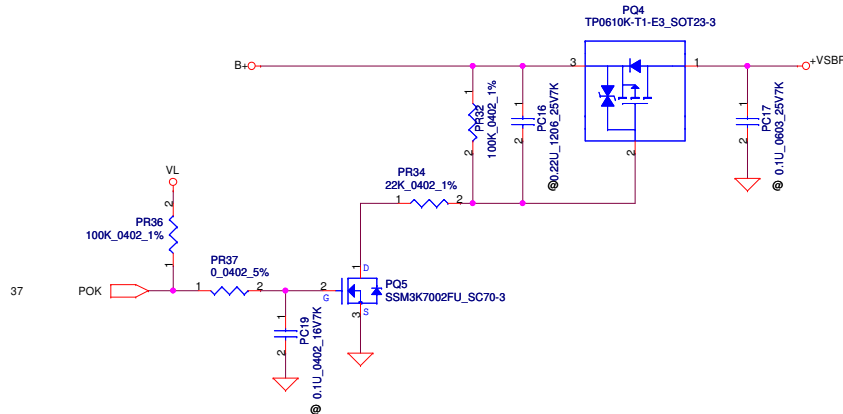
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/07/28	Deciphered Date	2010/07/28	Title	
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Date: Monday, August 10, 2009		Sheet 34 of 41		1.0	

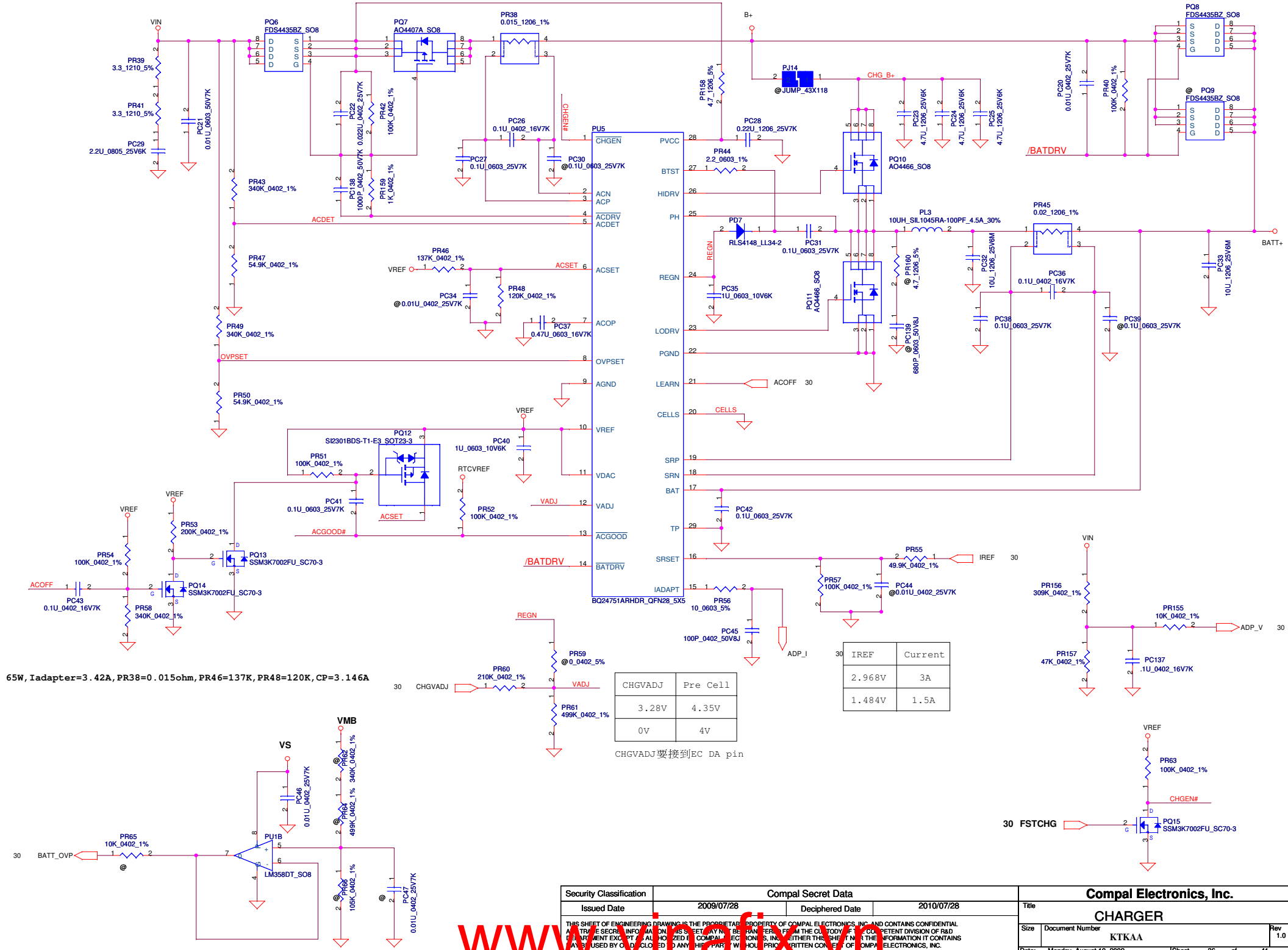


**PH1 under CPU bottom side :**  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 90 degree C  
 Recovery at 53 degree C





65W, Iadapter=3.42A, PR38=0.015ohm, PR46=137K, PR48=120K, CP=3.146A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

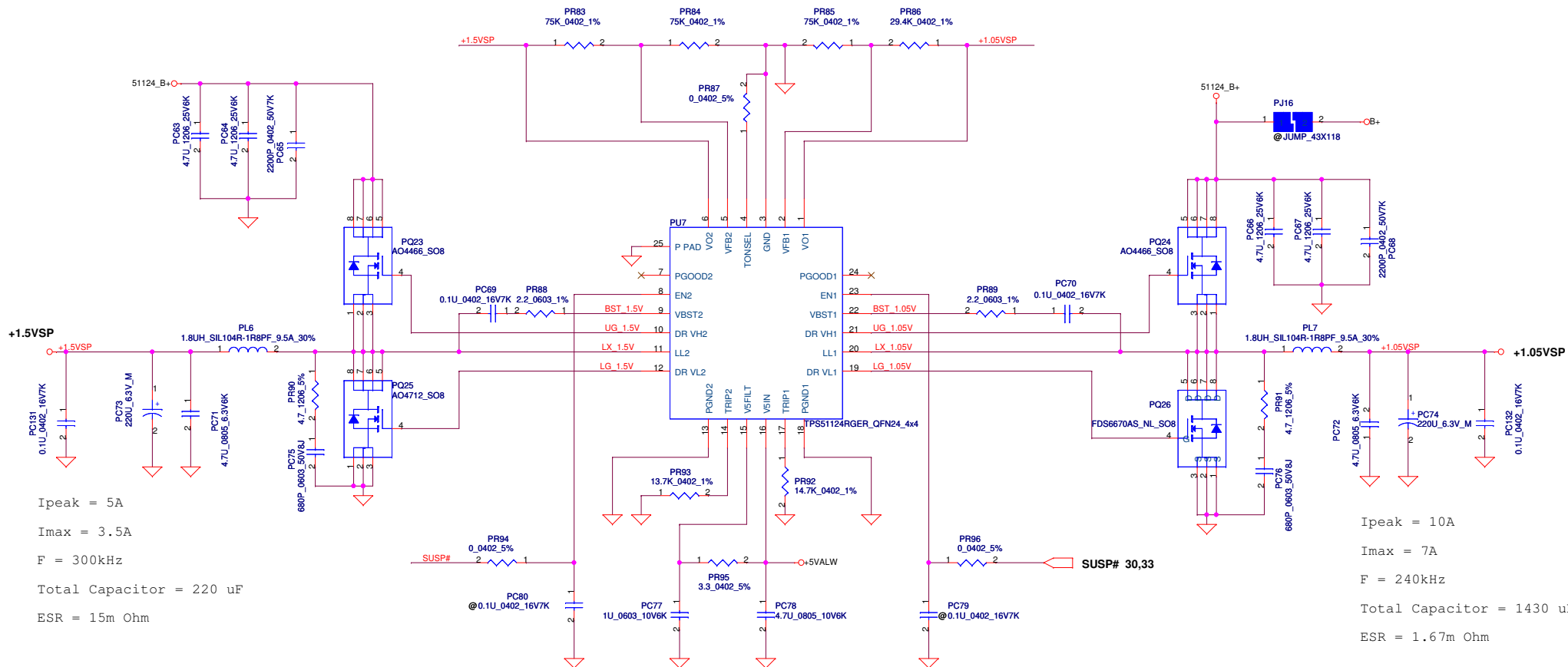
CHGVADJ要接到EC DA pin

Security Classification	Compal Secret Data	
Issued Date	2009/07/28	Deciphered Date
		2010/07/28

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Compal Electronics, Inc.			
CHARGER			
Size	Document Number	Rev	
	KTCAA	1.0	
Date:	Monday, August 10, 2009	Sheet	36 of 41

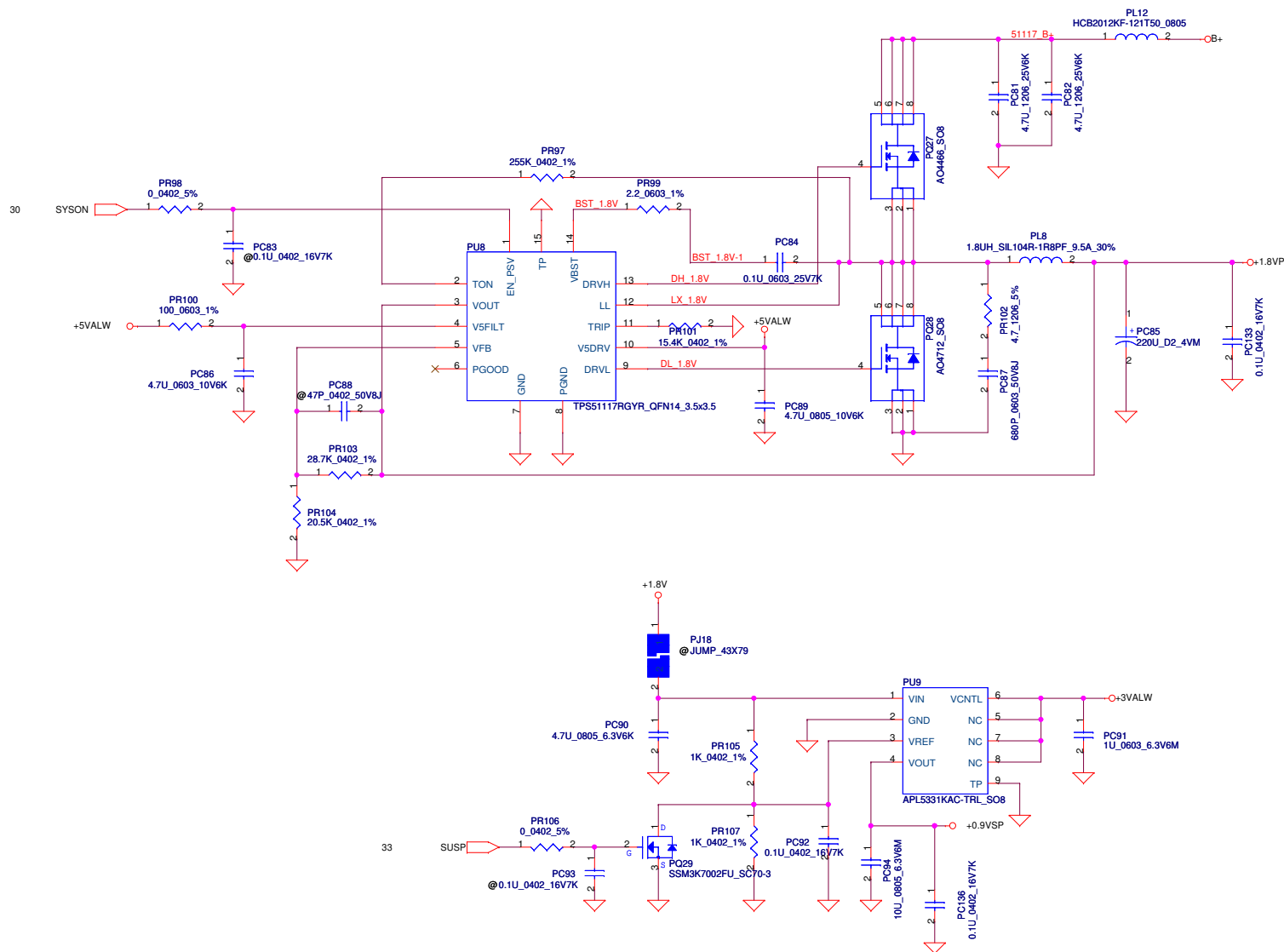




Security Classification		Compal Secret Data	
Issued Date	2009/07/28	Deciphered Date	2010/07/28

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Compal Electronics, Inc.			
Title 1.05V / 1.5V			
Size	Document Number	Rev 1.0	
Date:	Monday, August 10, 2009	Sheet	38 of 41



$I_{peak} = 8A$   
 $I_{max} = 5.6A$   
 $F = 312kHz$   
 Total Capacitor = 440  $\mu F$   
 $ESR = 7.5m \Omega$

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/07/28		Deciphered Date		2010/07/28		Title	
										1.8V / 0.9V	
										Size	Document Number
										Rev	1.0
										Date: Thursday, August 06, 2009	
										Sheet 39 of 41	

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PIR (Product Improve Record)

NBWAA LA-5821P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/06	18	Add R936 on BKOFF#; R937 on INVT_PWM	To prevent EC pin damage
2.	08/06	26	Add RL90, RL91, RL91 on +3V_LAN	For EMI's request
3.	08/06	18	Add C922, C923, C924 220pF on DAC_BRIG, INVT_PWM_R, BKOFF#_R	For EMI's request
4.	08/06	31	Delete R752, C787 on SPI_CLK; Add L912, C925 on SPI_CLK_L	For EMI's request
5.	08/06	28	Add LA11 on INT_MIC_L	For EMI's request
6.	08/06	28	Mount D61, DA3, DA6, DA7	For ESD's request
7.	08/06	32	Un-mount SW5, SW6	Power button, no need after pre-MP