

Ares-1 (LAR-1)

Cometlake-U Schematics

Project Code: 4PD0HK010001
PCB(Raw Card): 18834-1M

2020-03-19

DY	DUMMY
PCBID	PCB NO. control for SW
SKUID	CPU Type change for SW
MEM_ID	Memory ID for SW
DDR4_CTRL	SDP DDP setting
SDP/DDP	Select single DIE (SDP) Dual DIE(DDP)
APS/ISH/LPC/XDP	Debug Connectors
EMC	For EMC test request
NON_PSL/PSL	KBC PSL model control
CHARGER_HS/CHARGER_LS	Charger High/Low side MOSFET
VCCSA_HS/VCCSA_LS	VCCSA High/Low Side MOSFET
YOGA	YOGA model setting
ZZ	For Test Piont /Hole /ShortPad

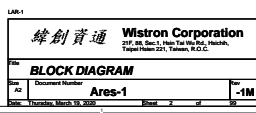
LAR-1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title COVER PAGE			
Size A4	Document Number Ares-1		Rev -1M
Date: Thursday, March 19, 2020		Sheet 1 of	99

Project Code: 4PD0HK010001
PCB(Raw Card): 18834-SB

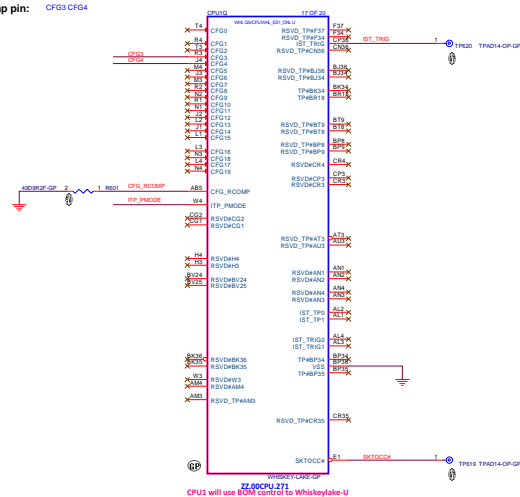
The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2->0402, R3->0603, R5->0805.

Battery Charger/Selector			44
RQ257/04ANSR			
IPV.DCATOUT	IPV.DCATOUT		
REF			
System DC/DC 5V			45
TPS31303RUEJ			
IPV.DCATOUT	IPV.5V		
System DC/DC 3.3V			45
TPS31303RUEJ			
IPV.DCATOUT	IPV.3V3		
DC/DC DMV#8			46
NCF81218MNTXG			
DC/DC VCCCP/CORE			47
NCF3020453LMTG			
IPV.DCATOUT	IPV.CPU_CORE		
DC/DC VCCGT			48
NCF3020453LMTG			
IPV.DCATOUT	IPV.VCCGT		
DC/DC VCCSA			50
NCF81251MNTBGT			
IPV.DCATOUT	IPV.VCCSA		
DC/DC DDR4 VDDQ			51
TPS31460RUEJ			
IPV.DCATOUT	IPV.5V3		
DC/DC DDR4 VTT			51
TPS31460RUEJ			
IPV.5V3	IPV.DDR4_VREF_50		
DC/DC DDR4 VREF			51
TPS31460RUEJ			
IPV.5V3	IPV.5V3		
DC/DC ID05V_SUS			52
TPS31350RUEJ			
IPV.DCATOUT	IPV.ID05V_SUS		
DC/DC IDB0V_SUS			53
TPS312ALGQJ			
IPV.5V3	IPV.IDB0V_SUS		

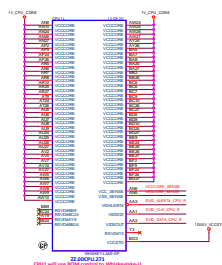


PCH strap pin: [CFG3](#) [CFG4](#)

15,99 CFG3  CFG3
15 CFG4 CFG4



ZZ00CPU.271
CPU1 will use BOM control to Whiskeylake-L



CPU1 will use BOM control to Whiskeylake-U

Layout Note:
The total length of Data and Clock (from CPU to each YE) must be equal (±0.1 inch). Route the Signal along between the Clock and the Data signals.

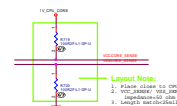
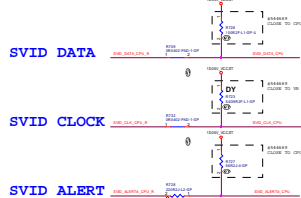


Figure 10-7. Routing Illustration for SVID Topology

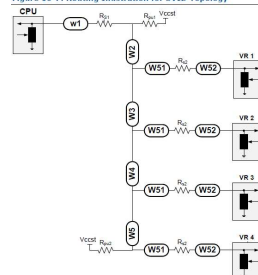
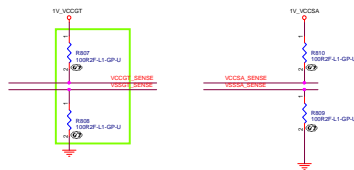
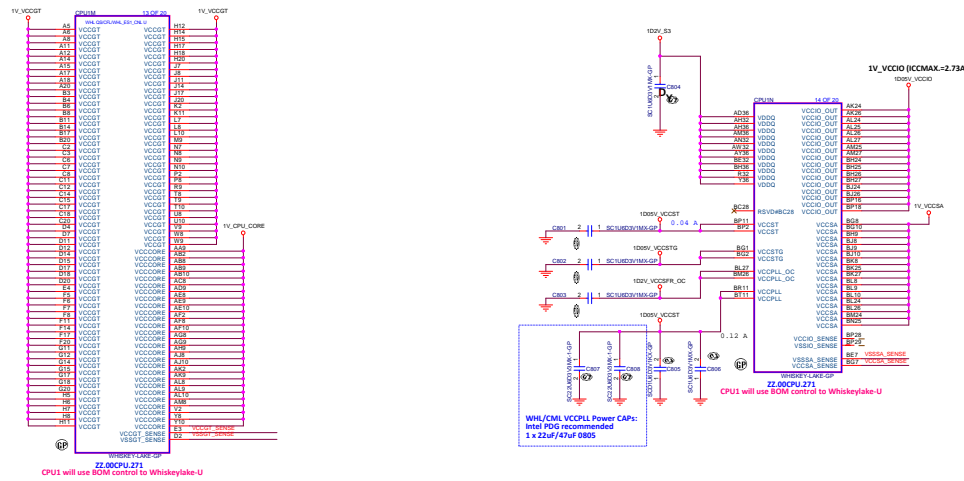


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R ₅₀₁ [°]	R ₅₀₂ [°]	R ₅₁ [°]	R ₅₂ [°]	W ₅₃ [°]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.4
VIDSCK							Empty	45	0	50	
VIDALERT d							56	Empty V	220	0	



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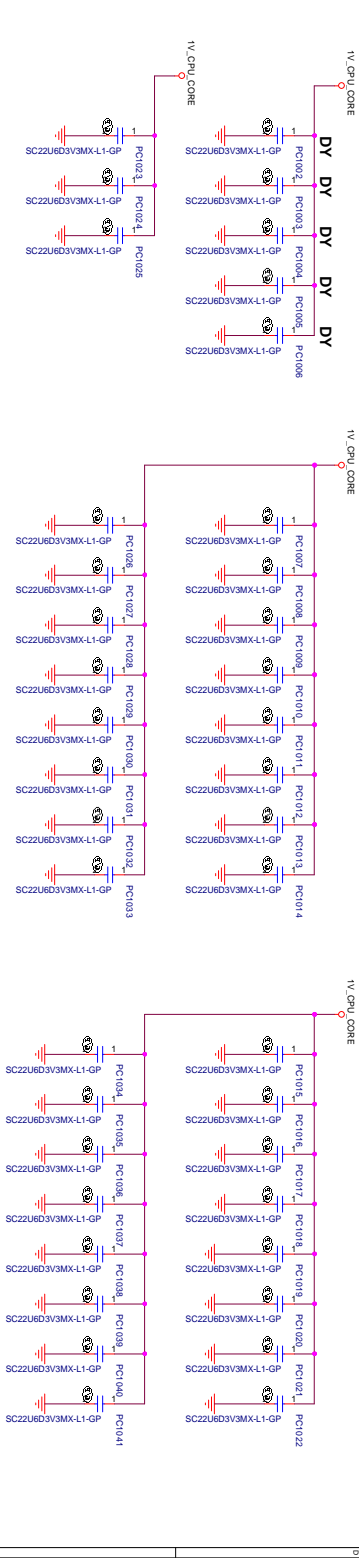
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Title			
CPU (RSVD)			
Size	Document Number		Rev
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2		1	

VCORE

CML_U42

U42
IcchMax current-10ms max = 70 A

22uF	PCS	Cap
U42	35	330uF*2
U22	22	330uF*1

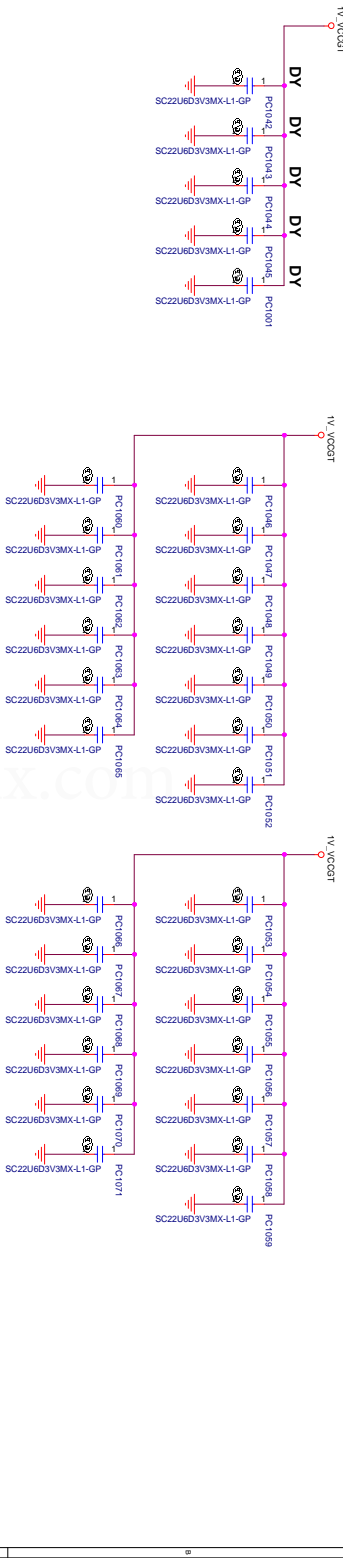


VCCGT

CML_U42

U42
IcchMax current-10ms max = 31 A

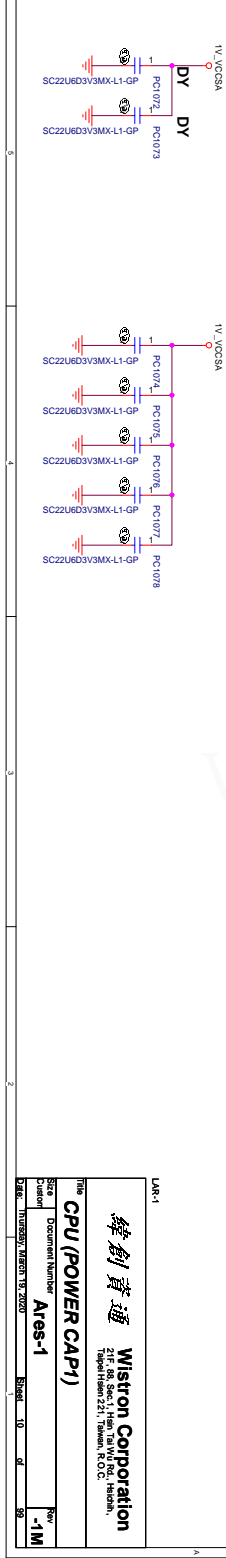
22uF	PCS	Cap
CML	26	330uF*1



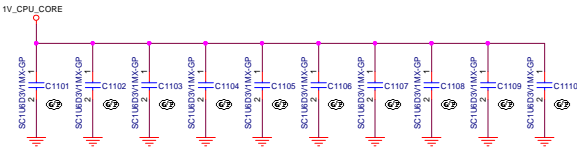
VCCSA

CML_U42

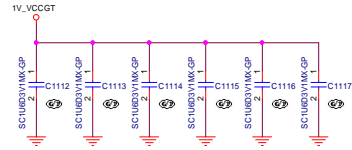
U42
IcchMax current-10ms max = 5 A



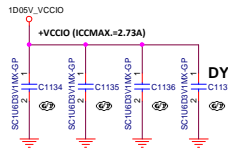
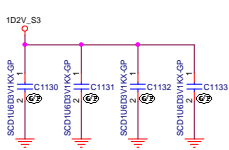
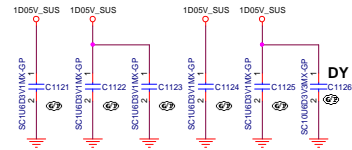
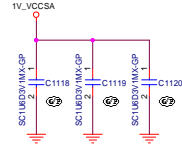
VCORE WHL U42



VCCGT WHL U42



VCCSA WHL U42



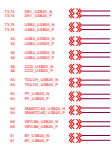
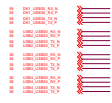
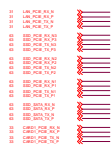
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File CPU (POWER CAP2)	
Size A3	Document Number Ares-1 Rev -1M
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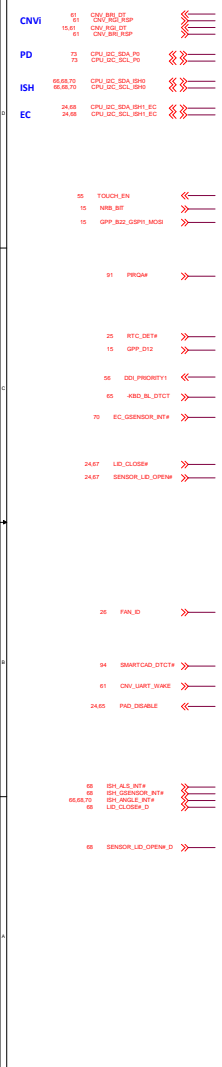
GBE PHY
M.2 PCIe SSD
Media Card Reader



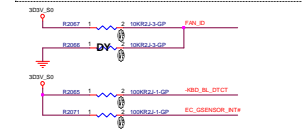
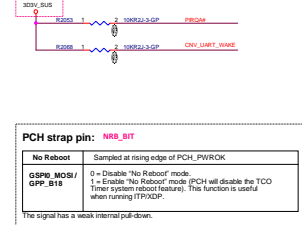
Legend Note:
1. Please refer to the pin definition of the component.
2. Please refer to the pin definition of the component.
3. Please refer to the pin definition of the component.

SATA Configuration	PCIe Configuration	USB1 Configuration	USB2 Configuration
Pin Device	Pin Device	Pin Device	Pin Device
1 NC	1 NC	1 USB1 Type-C Port (USB3 Docking)	1 USB1 Type-C Port (USB3 Docking)
2 M.2 SATA SSD	2 NC	2 USB1 Type-A Port (ADU)	2 USB1 Type-A Port (ADU)
3 NC	3 NC	3 USB1 Type-A Port (ADU)	3 USB1 Type-A Port (ADU)
4 NC	4 NC	4 USB1 Type-A Port (ADU)	4 USB1 Type-A Port (ADU)
5 NC	5 NC	5 NC	5 NC
6 NC	6 GBE PHY	6 NC	6 NC
7 NC	7 M.2 PCIe SSD	7 NC	7 NC
8 NC	8 M.2 PCIe SSD	8 NC	8 NC
9 NC	9 M.2 PCIe SSD	9 NC	9 NC
10 NC	10 M.2 PCIe SSD	10 NC	10 NC
11 NC	11 M.2 PCIe SSD	11 NC	11 NC
12 NC	12 M.2 PCIe SSD	12 NC	12 NC
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22 NC	22 M.2 PCIe SSD	22 NC	22 NC
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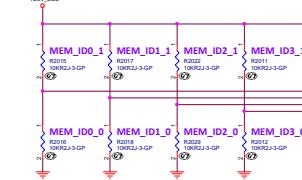
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PDG 4575412 p128



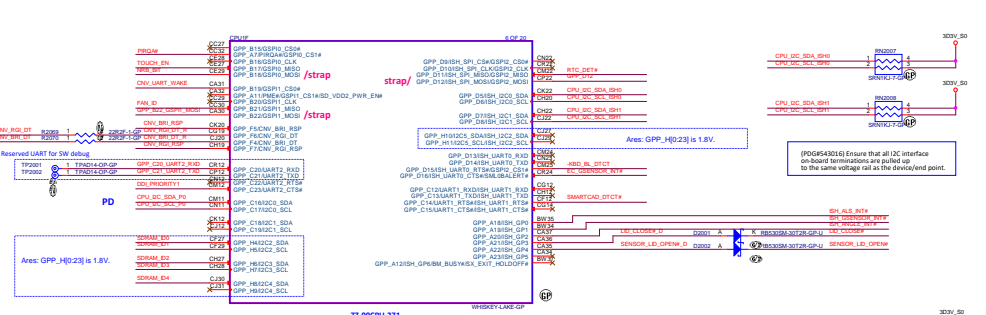
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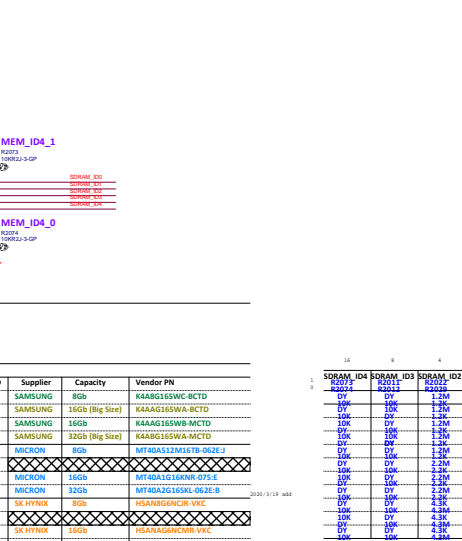
Memory Configuration

00: 8Gb 01: 16Gb (Big Size) 10: 16Gb 11: 32Gb (Big Size)		00: Samsung 01: Micron 10: SK Hynix 11: (Reserved)			
GPP_H0		GPP_H1		GPP_H4	
SRDRAM_ID4	SRDRAM_ID3	SRDRAM_ID2	SRDRAM_ID1	SRDRAM_ID0	Memory ID
0	0	0	0	0	0
0	1	0	0	0	8
1	0	0	0	0	16
1	1	0	0	0	24
0	0	0	1	0	2
0	1	0	1	0	10
1	0	0	1	0	18
1	1	0	1	0	26
0	0	1	0	0	4
0	1	1	0	0	12
1	0	1	0	0	20
1	1	1	0	0	28
0	0	0	0	1	1
0	0	0	1	1	3
0	0	1	1	1	5
0	0	1	1	0	6
0	1	1	1	0	14
1	0	1	1	0	22
1	1	1	1	0	30

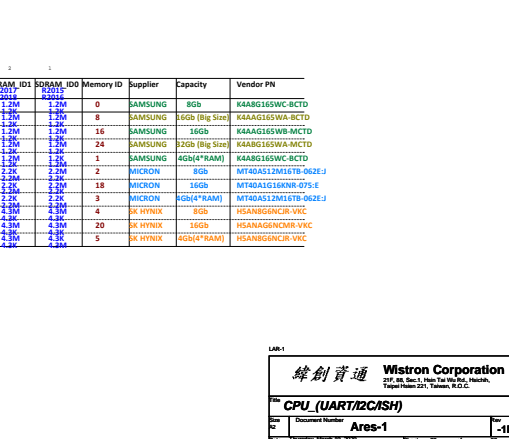
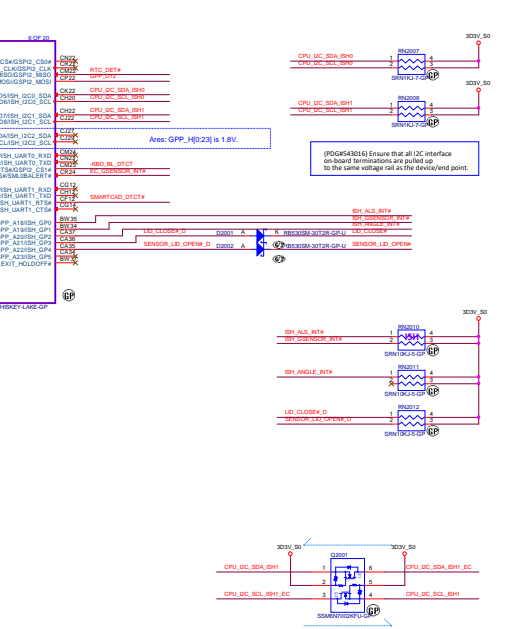
0x1, 1=H



22.00CPU.271 CPU1 will use BOM control to Whiskeylake-U

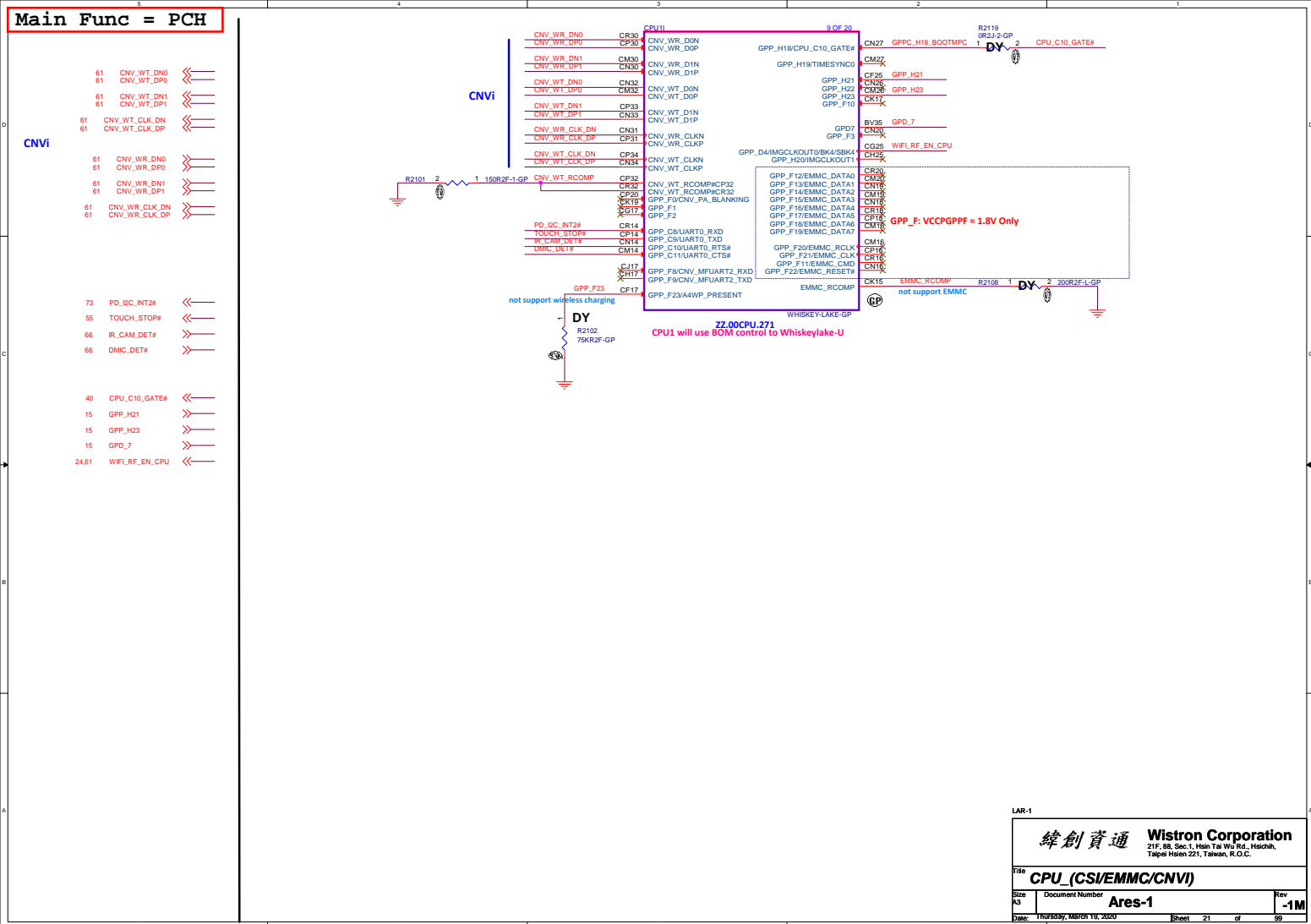


3/29 add 800-4u-8GB Configuration



Wistron Corporation
CPU (UART/IO/USB)
Ares-1
1M

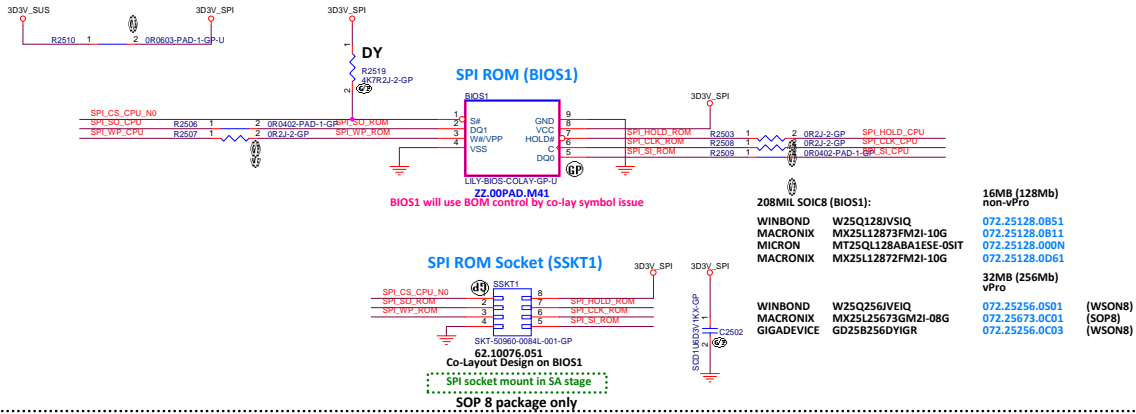
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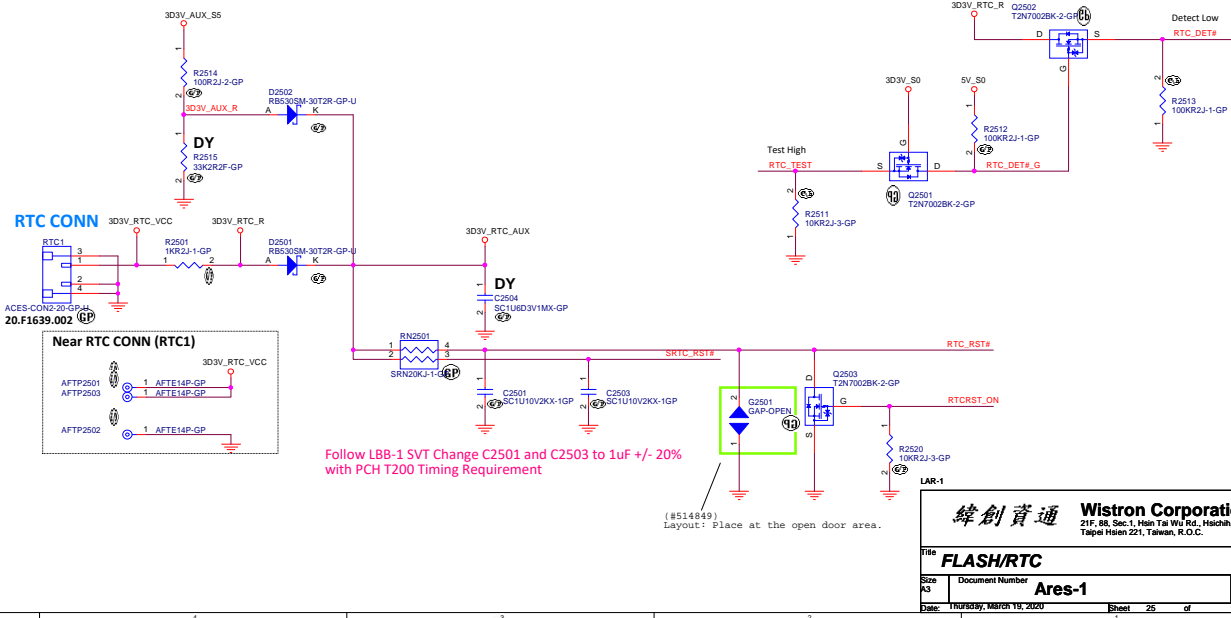
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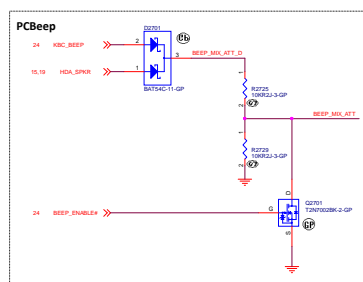
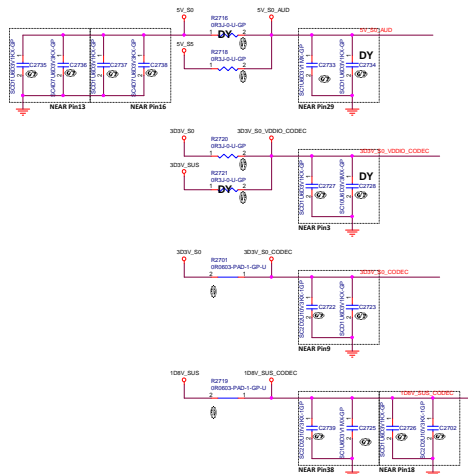
18,24 SPI_CS_CPU_N0
18,24,91 SPI_CLK_CPU
15,18,24,91 SPI_SI_CPU
18,24,91 SPI_SD_CPU
15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU



Main Func = RTC

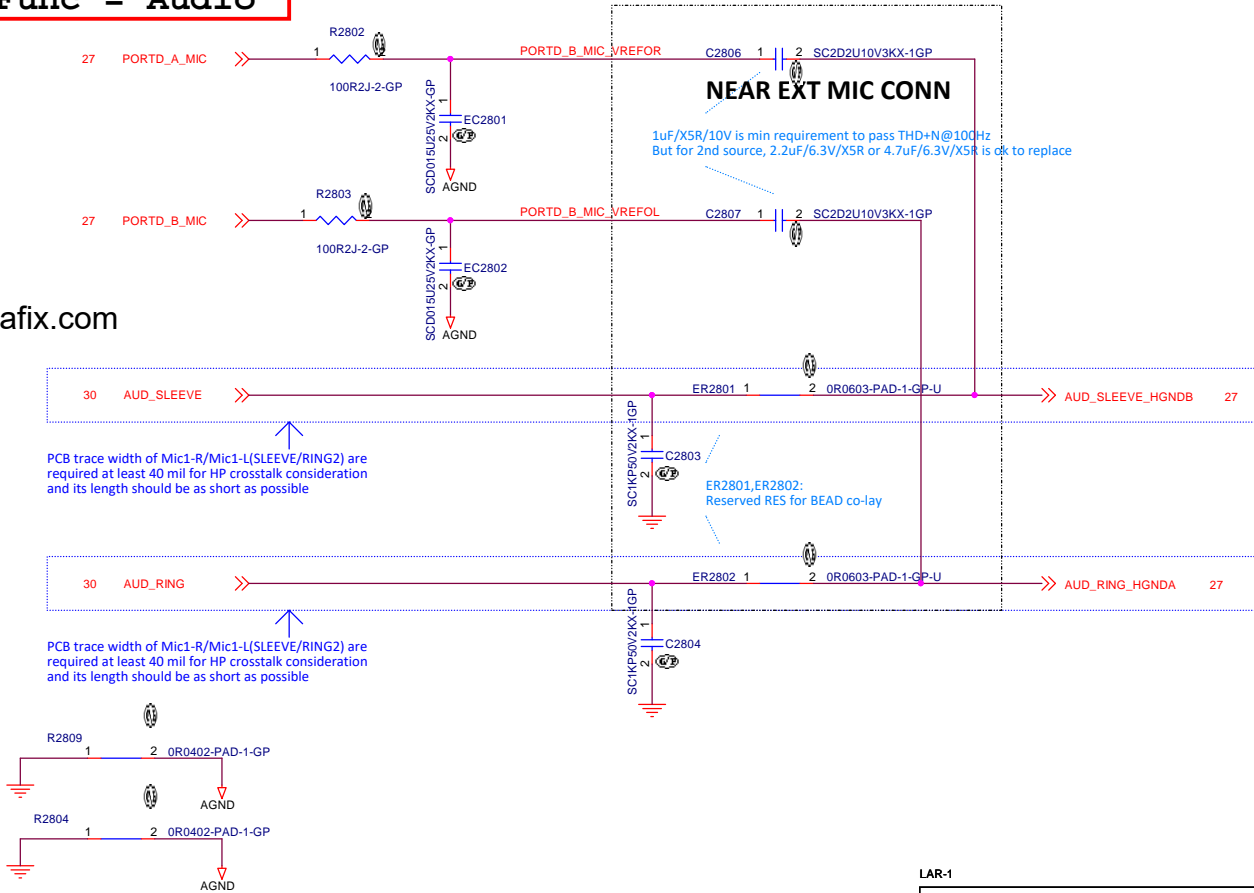
18,99 RTC_RST#
18 SRTC_RST#
20 RTC_DET#
18 RTC_TEST
24 RTCRST_ON





Main Func = Audio

Vinafix.com

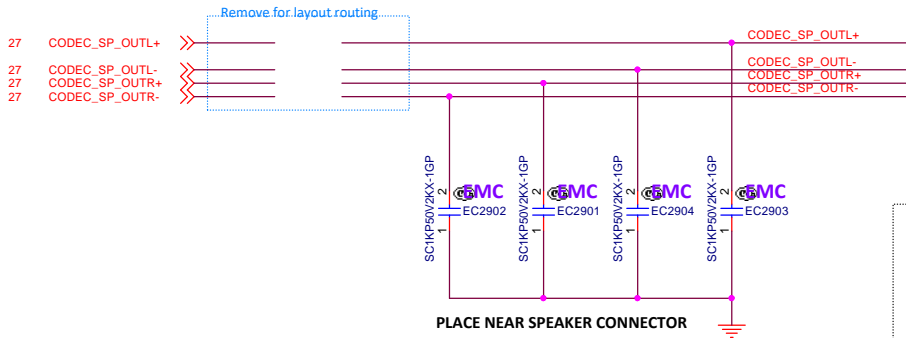


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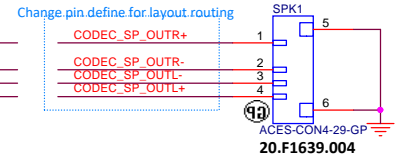
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Taipei Hsien 221, Taiwan, R.O.C.

Title
AUDIO (MIC I/F)

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SPEAKER CONN

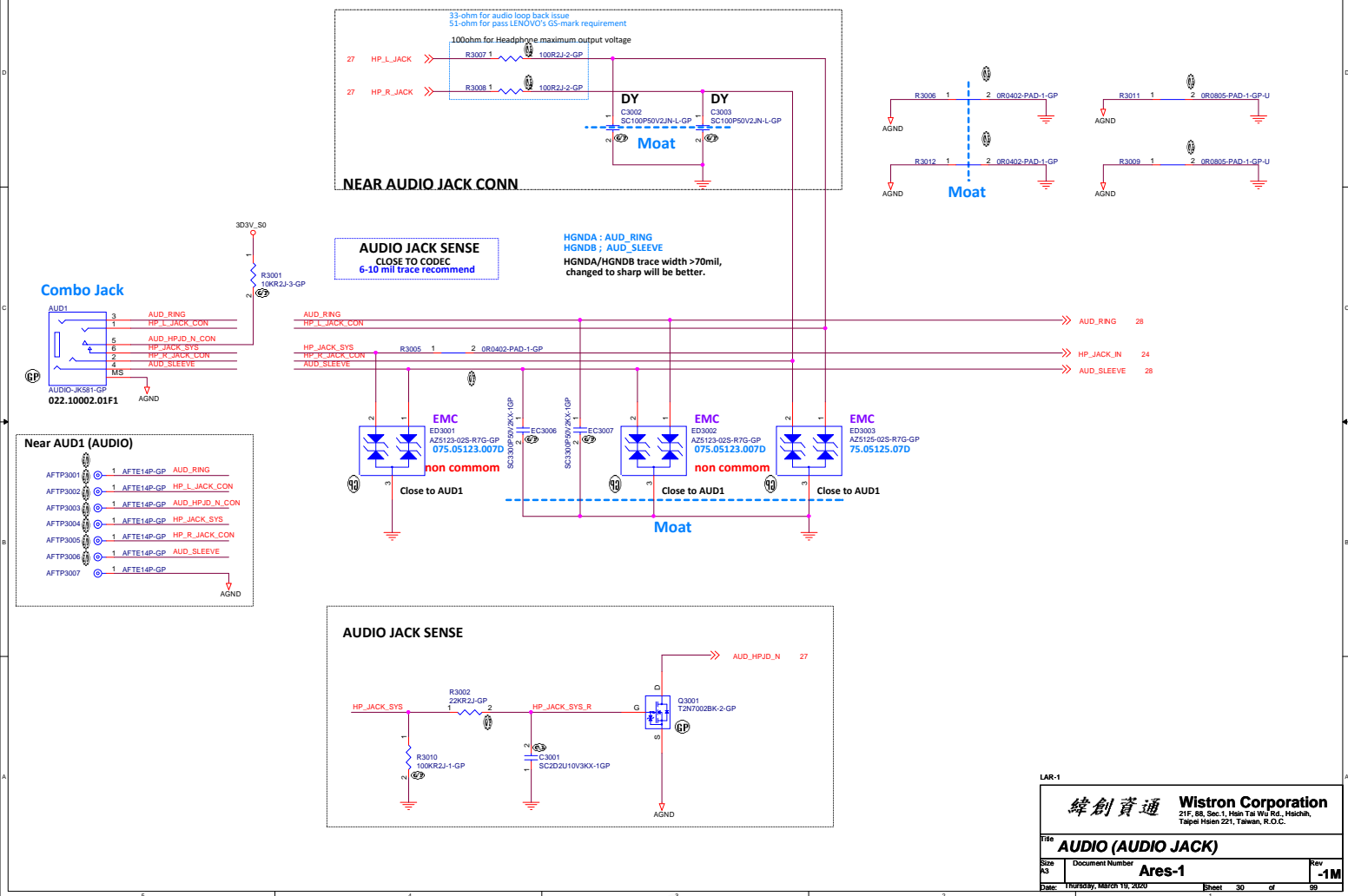


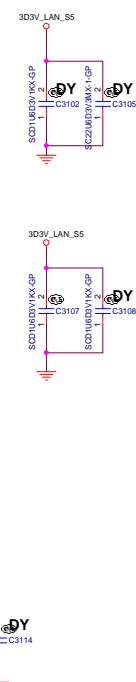
Near SPK1 (SPEAKER)



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Title AUDIO (SPEAKER)			
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25MHz (X3101)
TXC 7R25000008 082.30005.0931
HARMONY X2V025000DC1H-HU 082.30005.0A81

LAR-1

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Taipei Hsien 221, Taiwan, R.O.C.

Title **LAN (GIGA_WGI219LM)**

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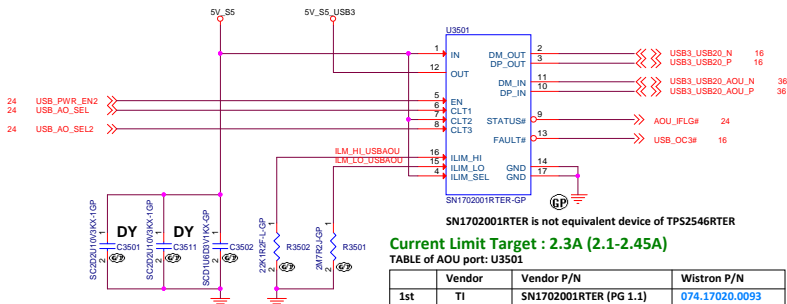
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Title LAN (RSVD)			
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Title USB (RSVD)	
Size A4	Document Number Ares-1
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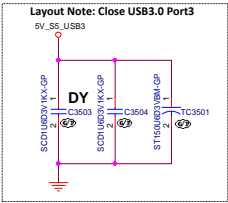
For USB3.0 System Port3 (For AOU)



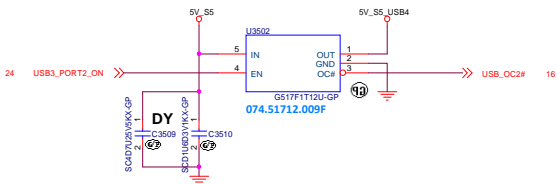
Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PISUSB2546H2HEX	074.52546.0073



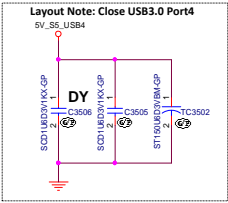
For USB3.0 System Port4

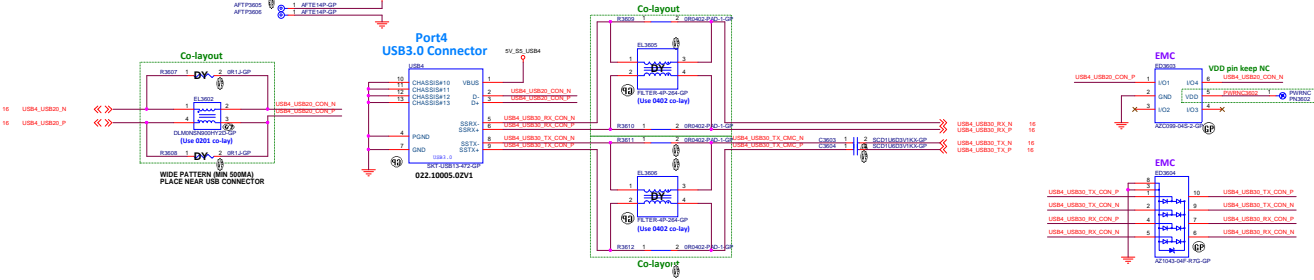
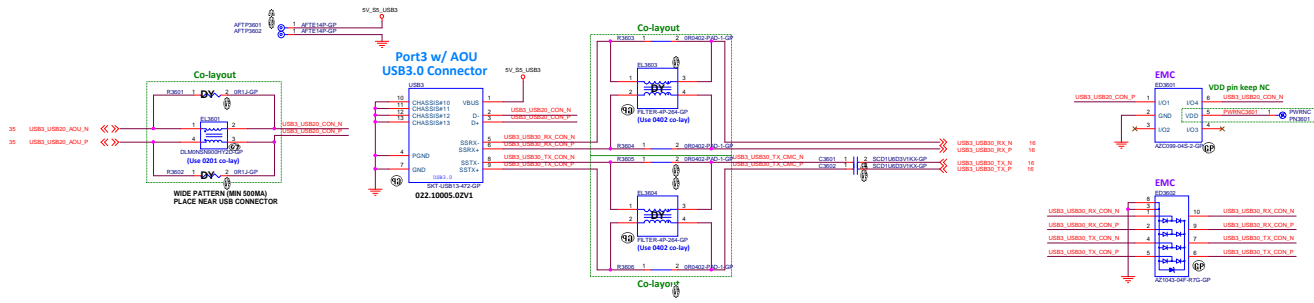


Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	GMT	G517F1T12U	074.51712.009F
2nd	SILERGY	SY6288C20AAC	074.06288.007B





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Title USB (RSVD)	
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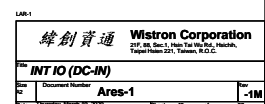
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Title SEQUENCE (RSVD)	
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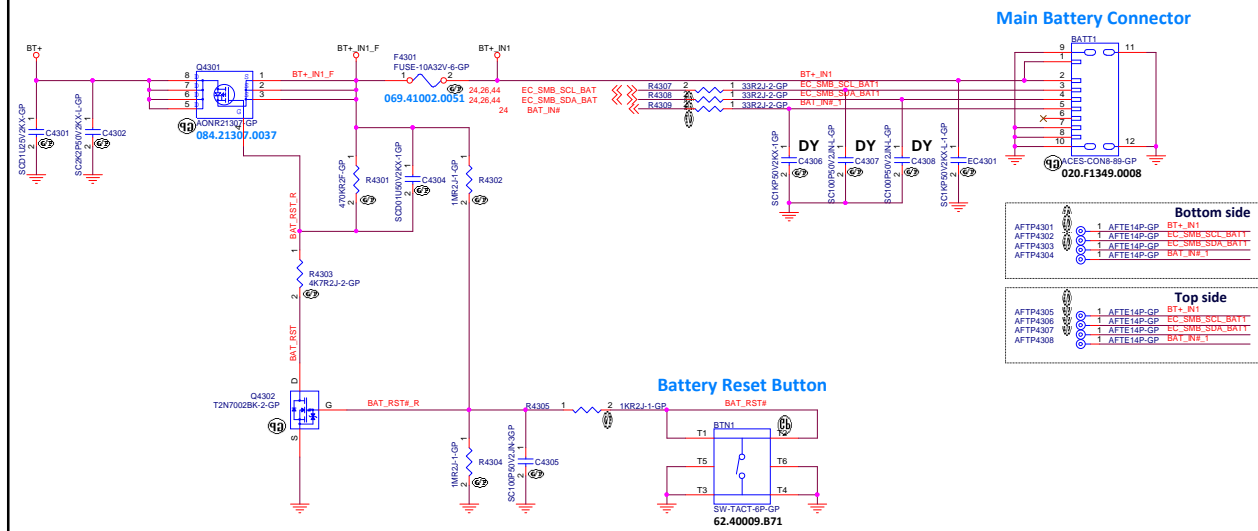
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Main Func = M-BAT Input
Main Func = BAT Reset



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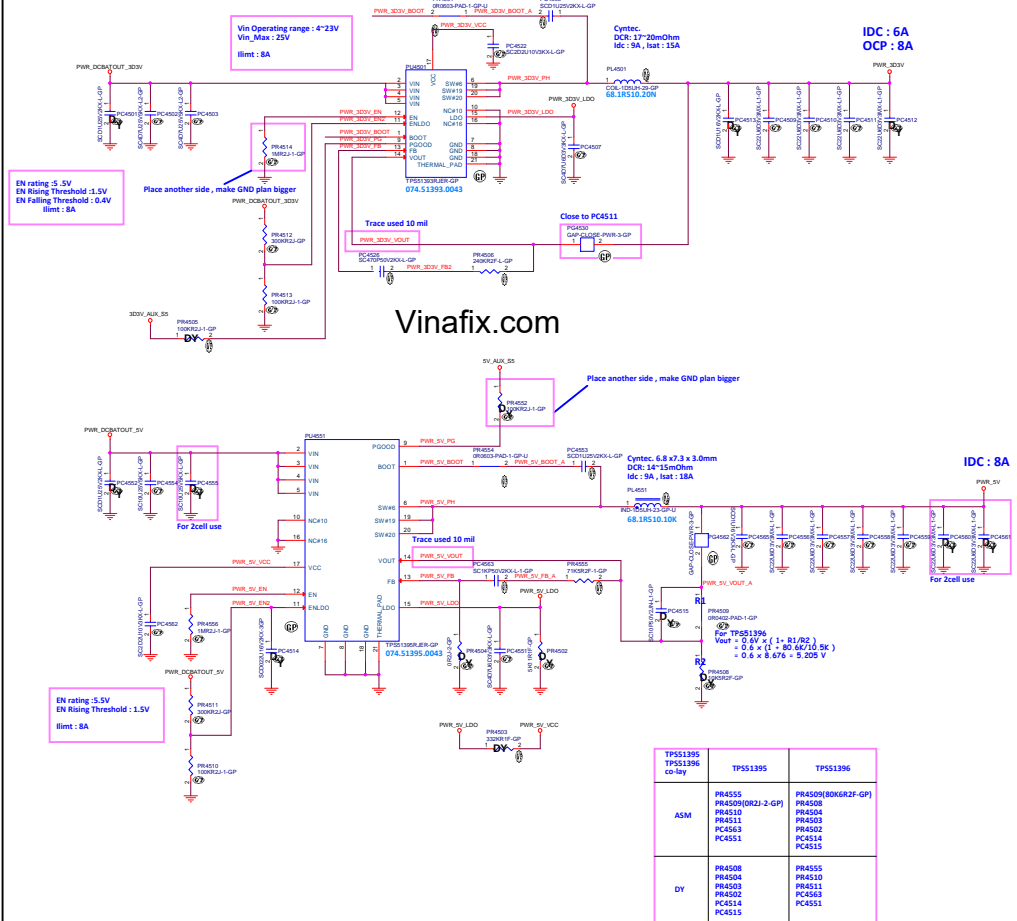
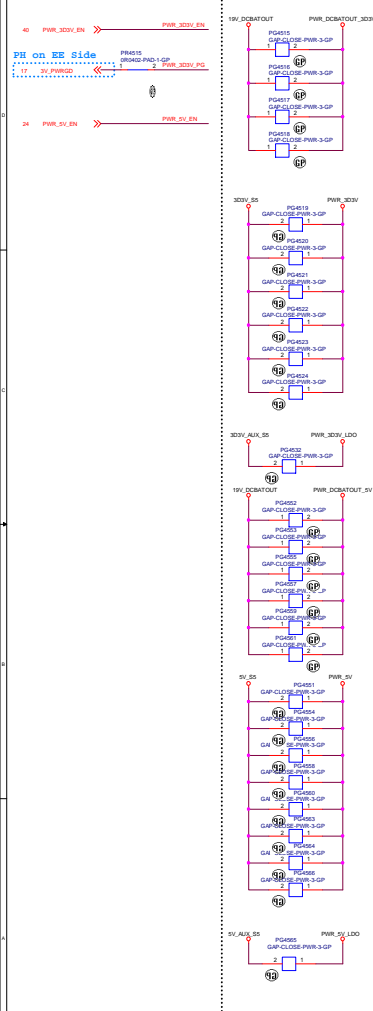
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

INT IO (BATT CONN)

Size A3 Document Number Ares-1 Rev -1M

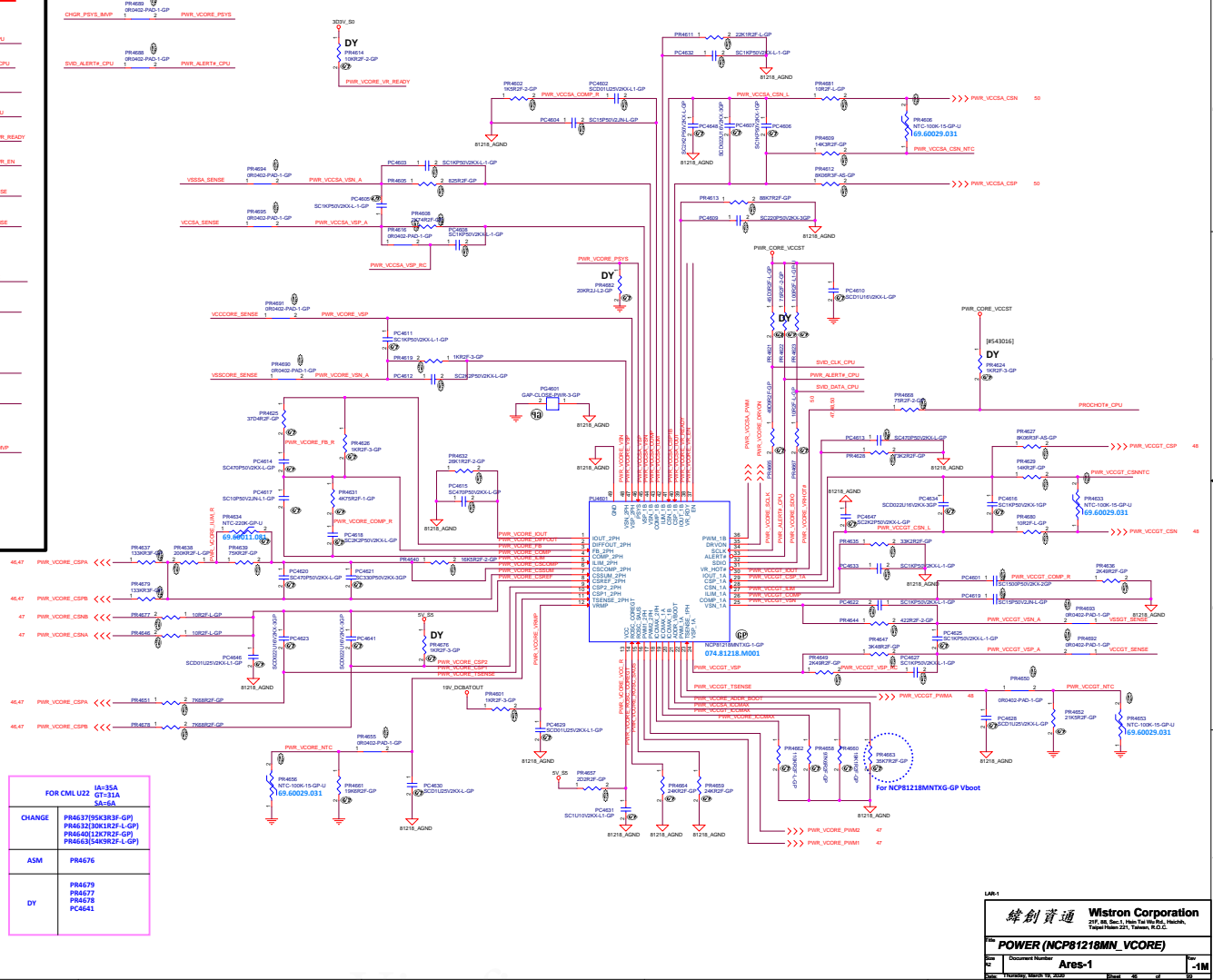
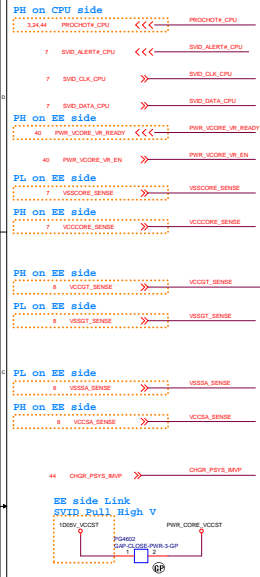
Date: Thursday, March 19, 2020 Sheet 43 of 59

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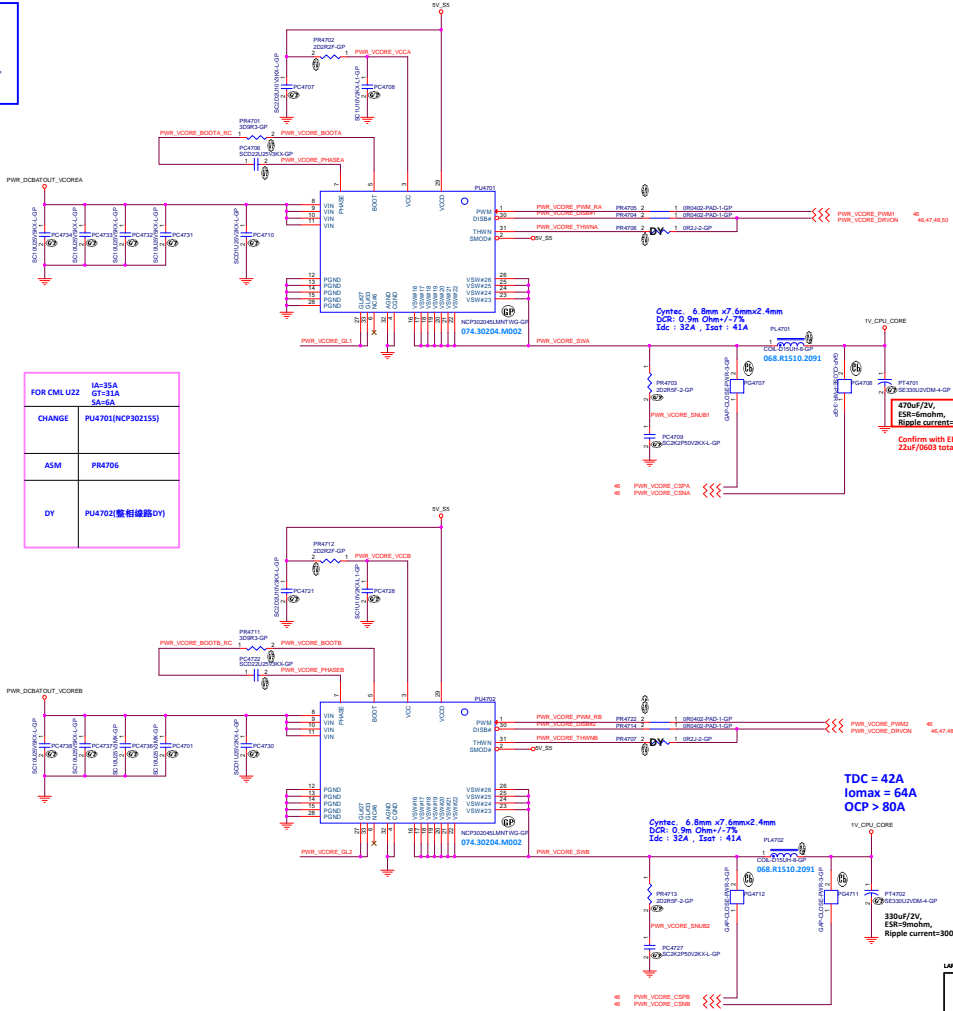
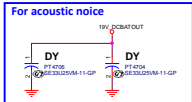
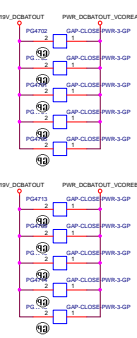
TP551395 TP551396 co-lay	TP551395	TP551396
ASM	PR4555 PR4509(ORJ2-2-GP) PR4510 PR4511 PC4563 PC4551	PR4508(80K6R2F-G) PR4508 PR4504 PR4503 PR4502 PC4514 PC4515
DY	PR4508 PR4504 PR45031 PR4502 PC4514 PC4515	PR4555 PR4510 PR4511 PC4563 PC4551

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FOR CML U22		IA=35A GT=31A SA=6A
CHANGE	PR4637(95K3R3F-GP) PR4632(30K1R2F-L-GP) PR4640(12K7R2F-GP) PR4663(54K9R2F-L-GP)	
ASM	PR4676	
DY	PR4679 PR4677 PR4678 PC4641	

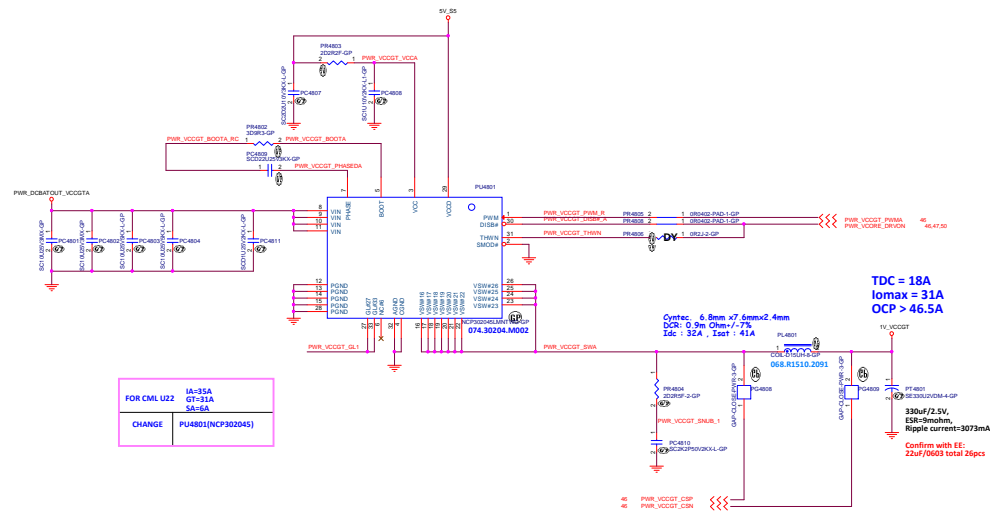
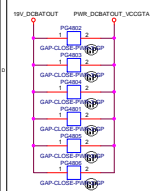
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FOR CML U22	IA=35A GT=91A SA=5A
CHANGE	PU4701(NCP302155)
ASM	PR4706
DY	PU4702(雙相線路DY)

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POWER (NCP30204SLM_VCORE)
Ares-1
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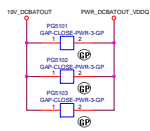
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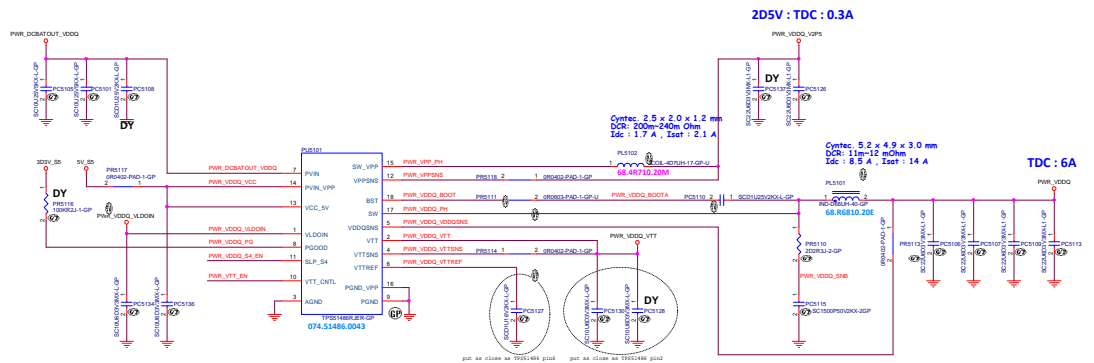
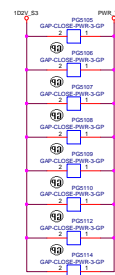
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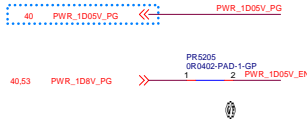


STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

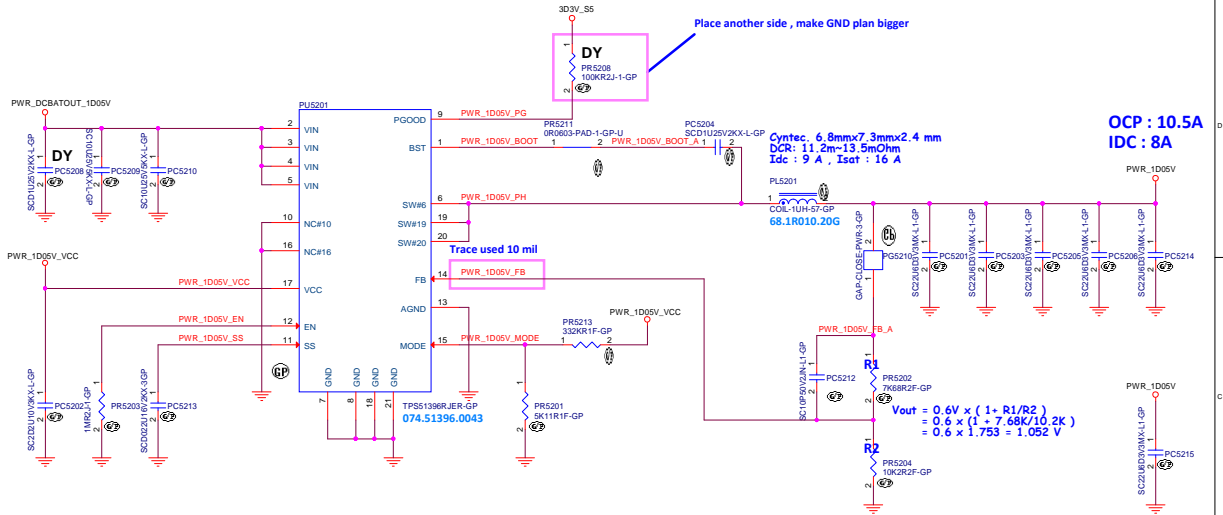
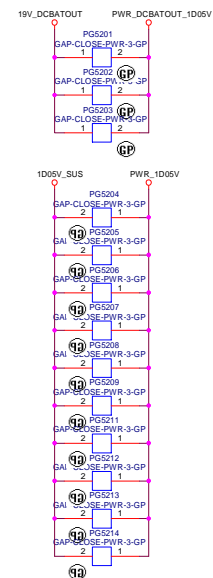


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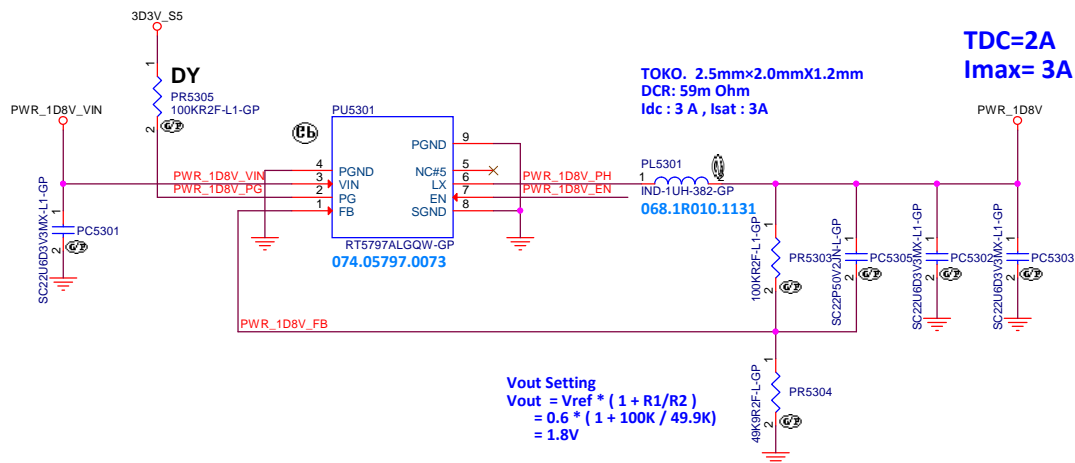
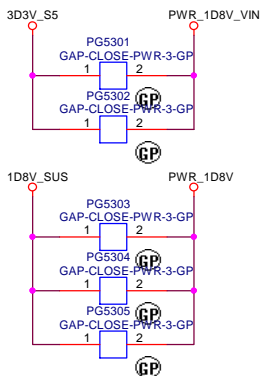


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Title	POWER (RT5797_1D8V)
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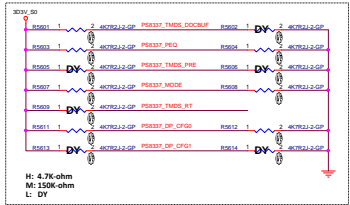
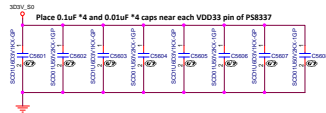
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TABLE 1: Automatic Switching Mode (CFG0 = H)
SW (DDI_PRIORITY)
L: USB Type-C has higher priority when both ports are plugged
H: HDMI Port has higher priority when both ports are plugged
Note: SW is pulled down with 150K-ohm internally



WHL DDI

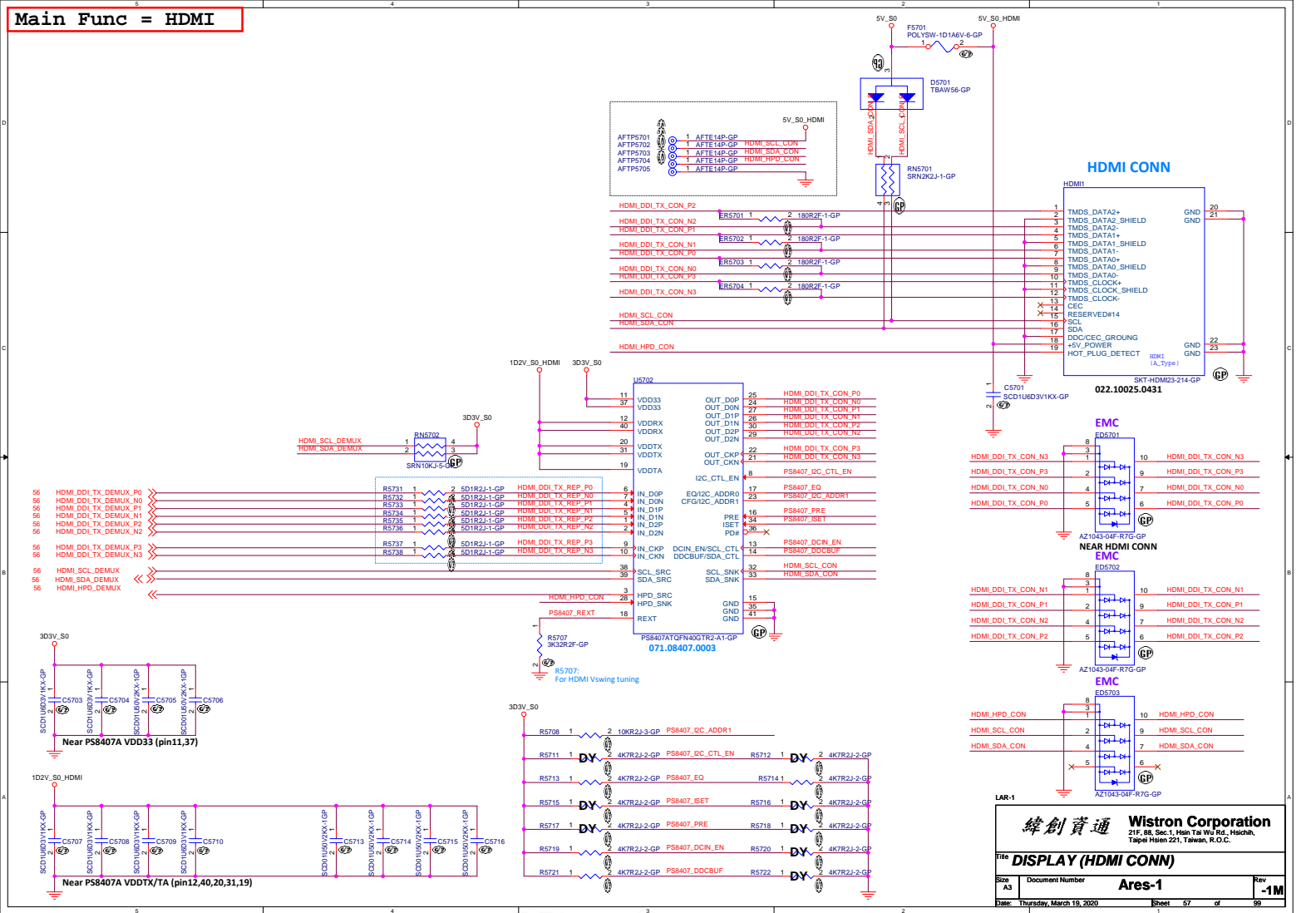
WHL DDI

24.26.70 CPU_SMB_SCL_THERM PS8337_DP_CFG0
24.26.70 CPU_SMB_SDA_THERM PS8337_DP_CFG0

TO PS8747B
TO HDMI

TO PS8747B
Priority first

TO HDMI

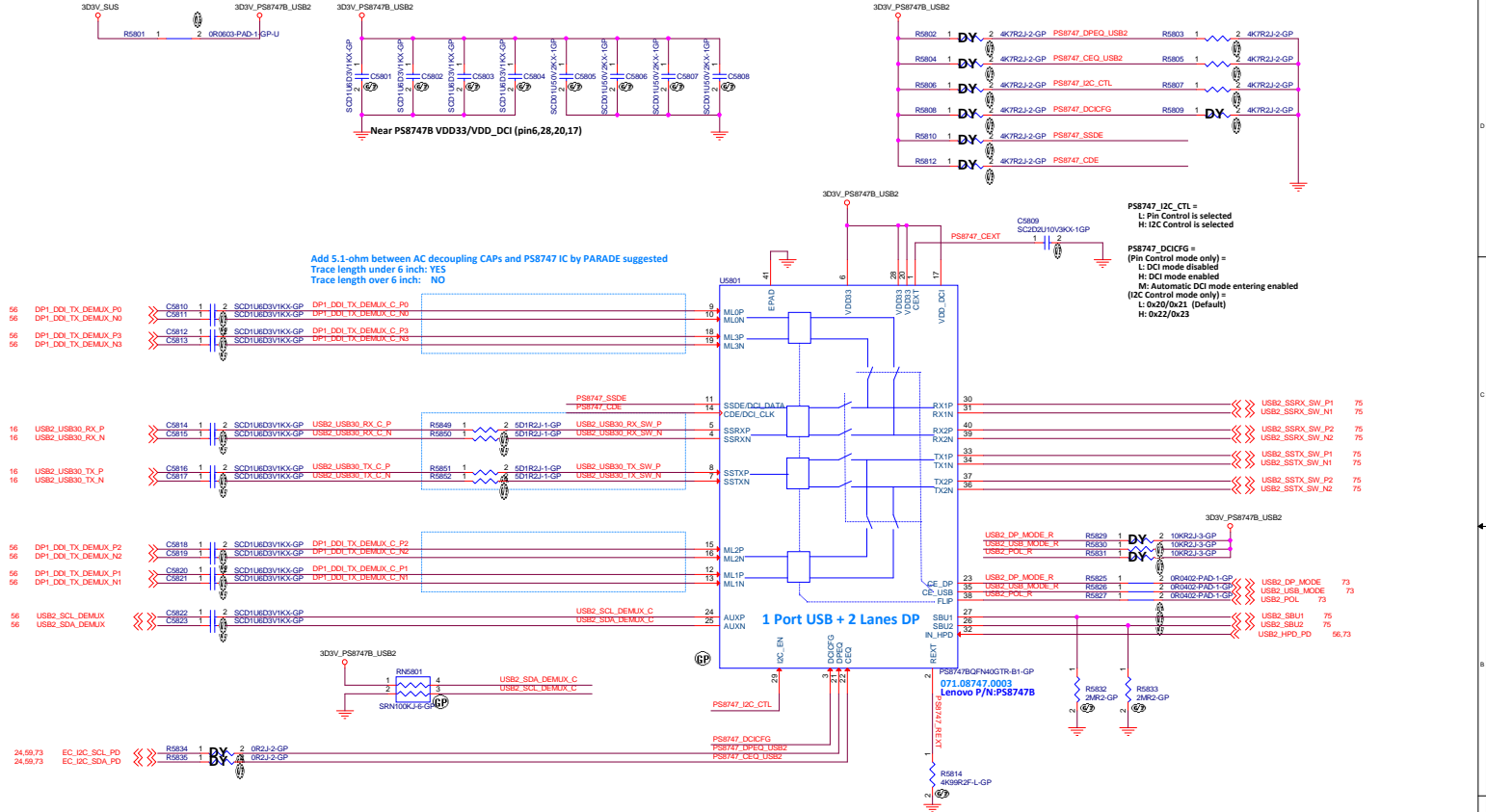


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File: **DISPLAY (HDMI CONN)**

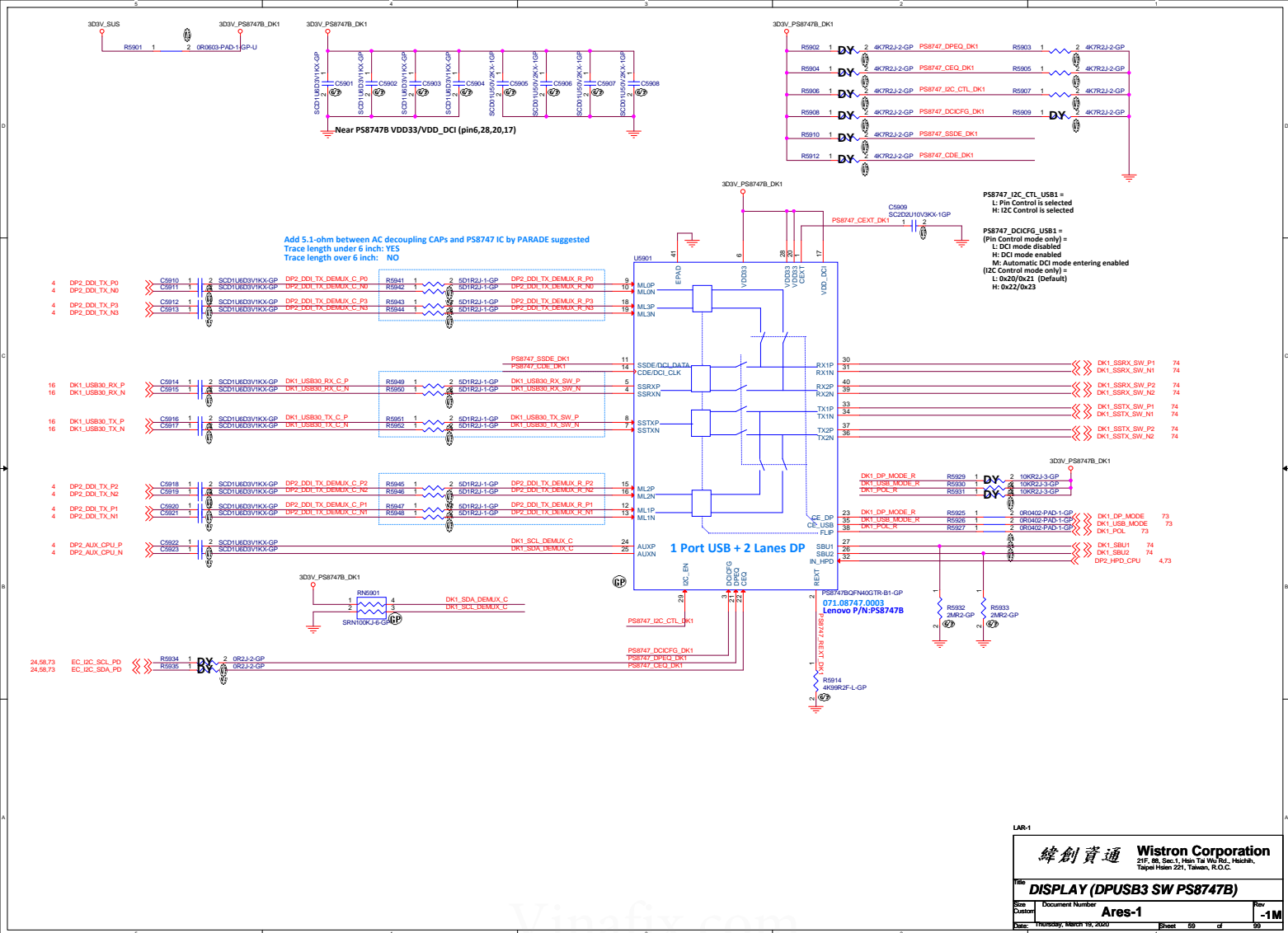
Size: A3 Document Number: **Ares-1** Rev: **-1M**

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PS8747_I2C_CTL =
L: Pin Control is selected
H: I2C Control is selected

PS8747_DCICFG =
(Pin Control mode only) =
L: DCI mode disabled
H: DCI mode enabled
(Automatic DCI mode entering enabled
(I2C Control mode only) =
L: 0x20/0x21 (Default)
H: 0x22/0x23



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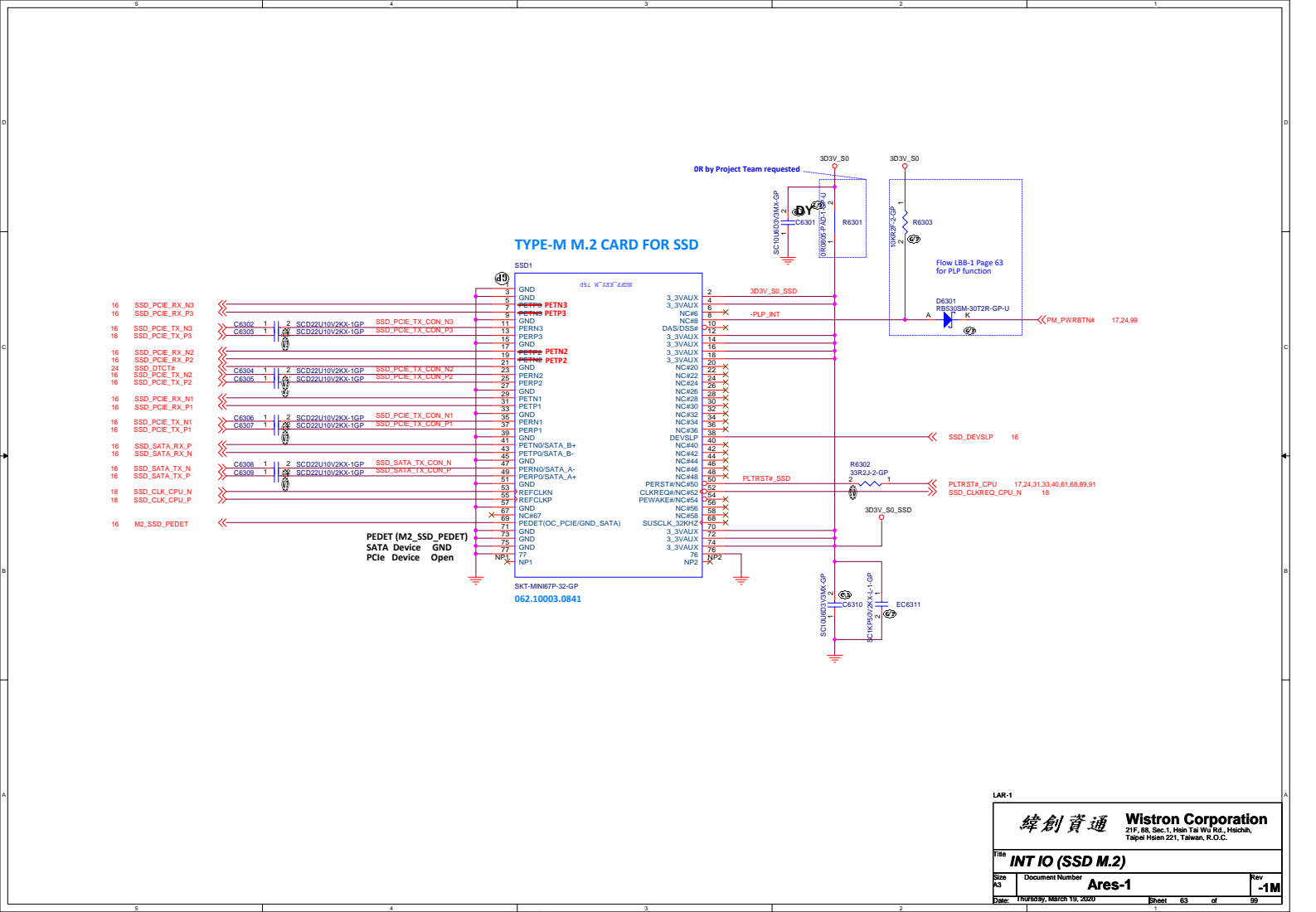
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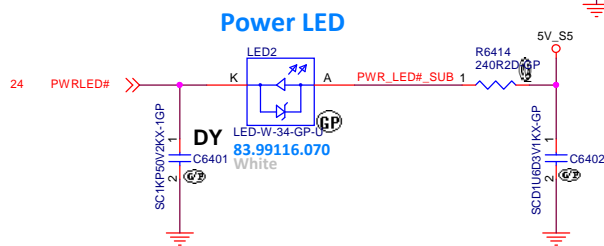
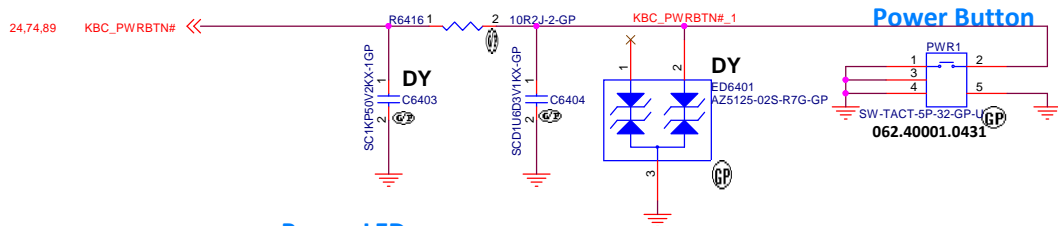
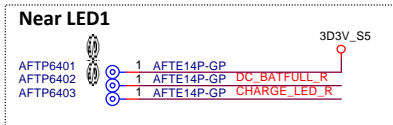
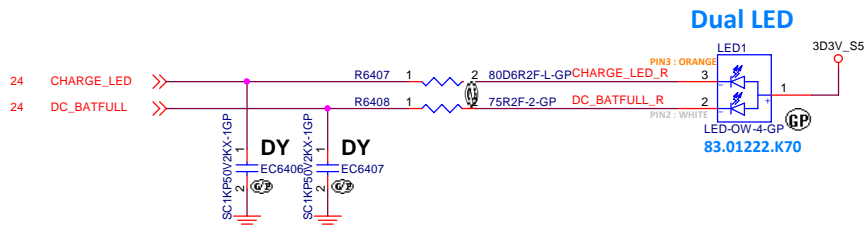
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Title INT IO (RSVD)			
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Title **LED/BTN/POWER BTN**

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LID_CLOSE#: NB Lid function
SENSOR_LID_OPEN#: Tablet detect function



TOP VIEW (pads not visible)

TOP VIEW (pads not visible)

GND			OUT2 (Detect the north pole)
-----	-------------------------------------------------------------------------------------	-------------------------------------------------------------------------------------	------------------------------

VDD		OUT1 (Detect the south pole)
-----	-------------------------------------------------------------------------------------	------------------------------

B1 B2

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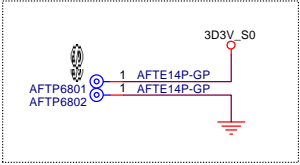
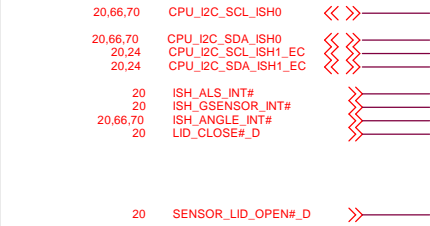
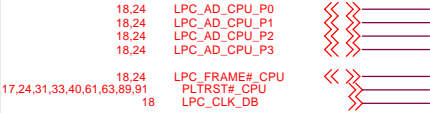
Title **SENSOR (HALL-SENSOR)**

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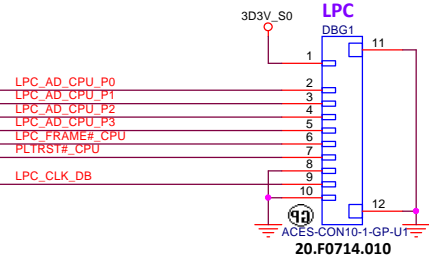
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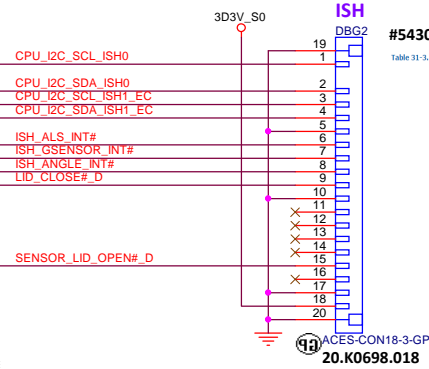
Main Func = Debug



LPC Connector



Sensors Debug Hooks



#543016

Table 31-3. 18-pin ZIF Connector Pinout

Pin	Pin Function	Description
1	SPW_I2C0_SCL	Click line for the I2C0
2	SPW_I2C0_SDA	Click line for the I2C0
3	SPW_I2C1_SCL	Click line for the I2C1
4	SPW_I2C1_SDA	Click line for the I2C1
5	GND	System Ground
6	GPIOA[10]	Connect here one of the GPIOs in use
7	GPIOA[11]	Connect here one of the GPIOs in use
8	GPIOA[12]	Connect here one of the GPIOs in use
9	GPIOA[13]	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vcc	Sensors Reference Voltage

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Title

DEBUG (LPC DEBUG)

Size

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Document Number

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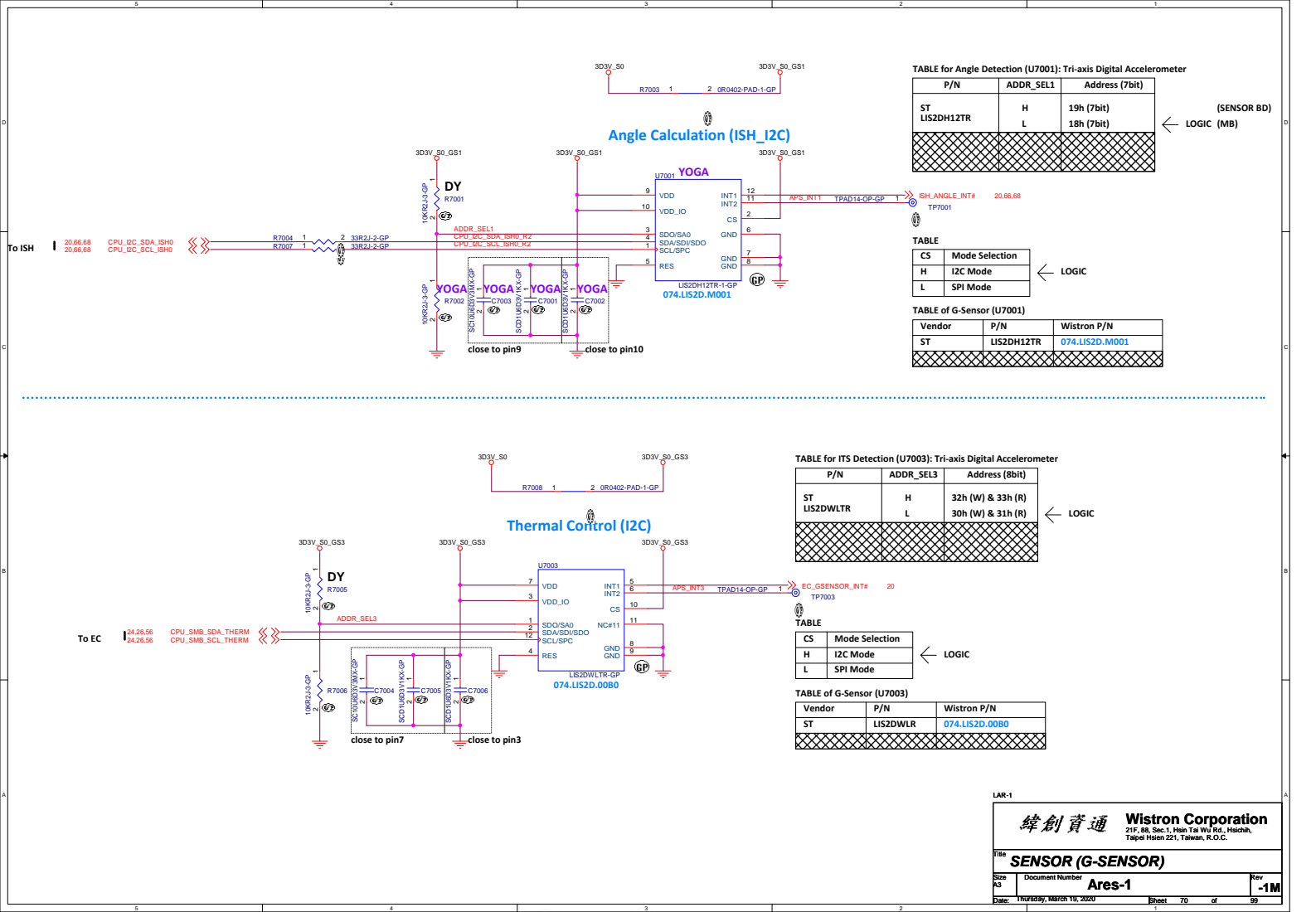
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Title EXT IO (RSVD)			
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Title EXT IO (RSVD)			
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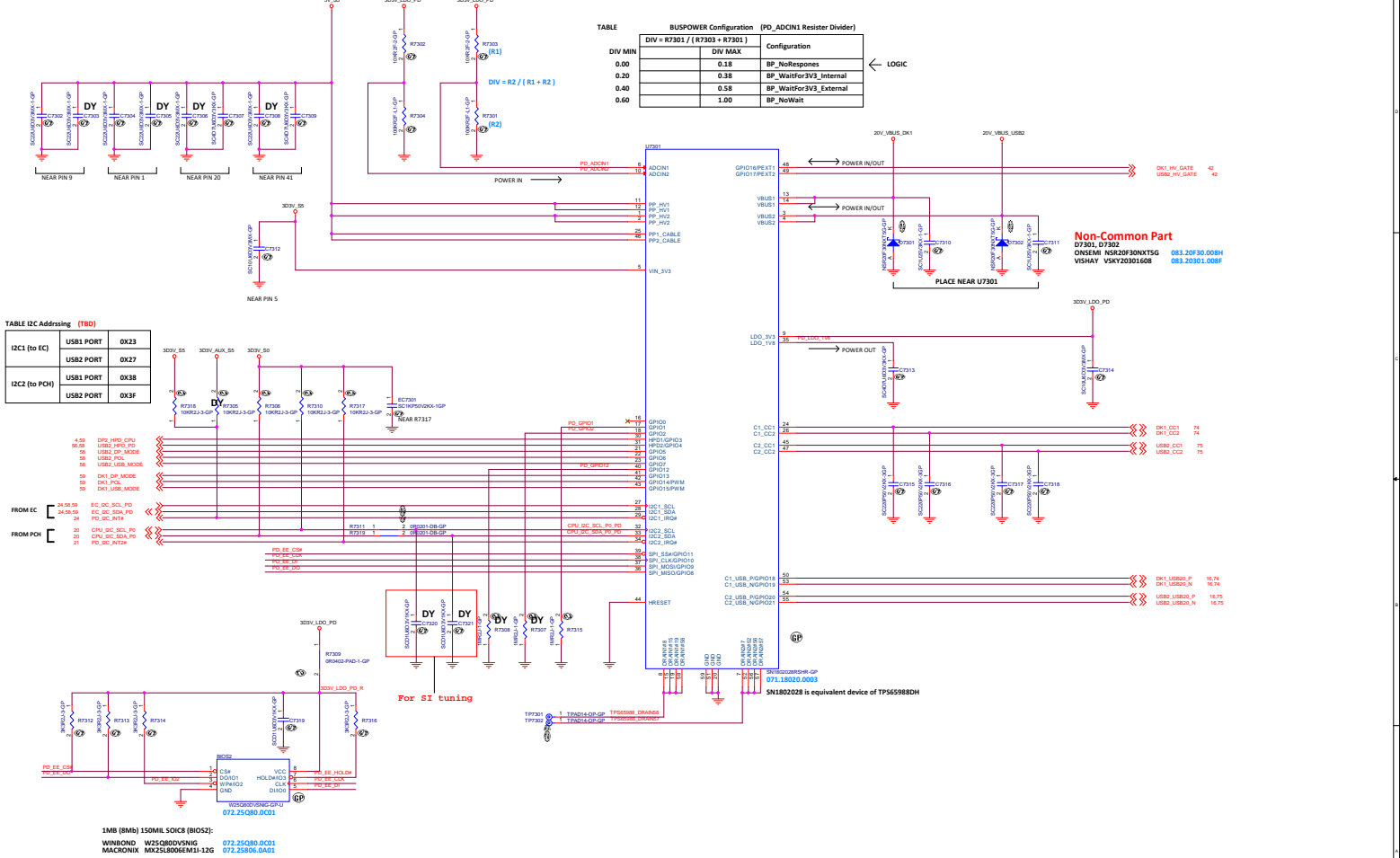


TABLE I2C Addressing (TBD)

IZC1 (to EC)	USB1 PORT	0X23
IZC1 (to EC)	USB2 PORT	0X27
IZC2 (to PCH)	USB1 PORT	0X38
IZC2 (to PCH)	USB2 PORT	0X3F

TABLE BUSPOWER Configuration (PD_ADCIN1 Resistor Divider)

DIV MIN	DIV MAX	Configuration
0.00	0.18	BP_NoResponses
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

Non-Common Part
D7301, D7302
ONSEMI NOK20F30NXTSG 083.20F30.008H
VISHAY VSKY20301608 083.20301.008F

1MB (BMA) 150MBL SOC8 (BIOS2):
WINBOND W25Q80DV5NIG 072.25Q80.DC01
MACRONIX MX25L8006EM1-12G 072.25806.0A01

Wistron Corporation
EXT IO (TYPEC PD TPS65988)

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Title GPU (RSVD)	
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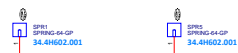
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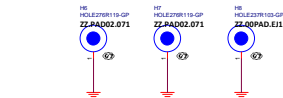
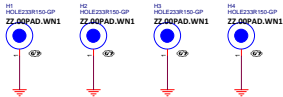
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EMI Spring

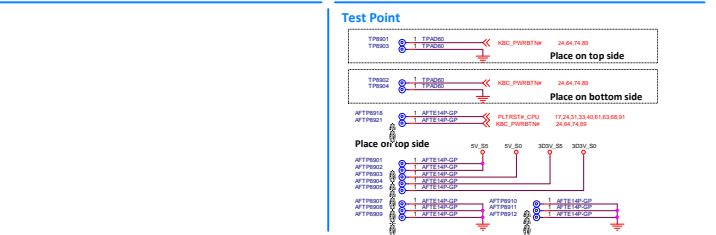
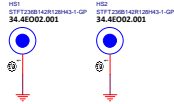


Screw Pad

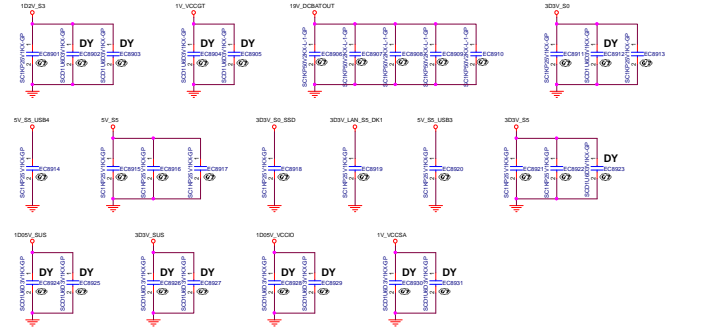


RF CAPS

Stand Off



EMI CAPS



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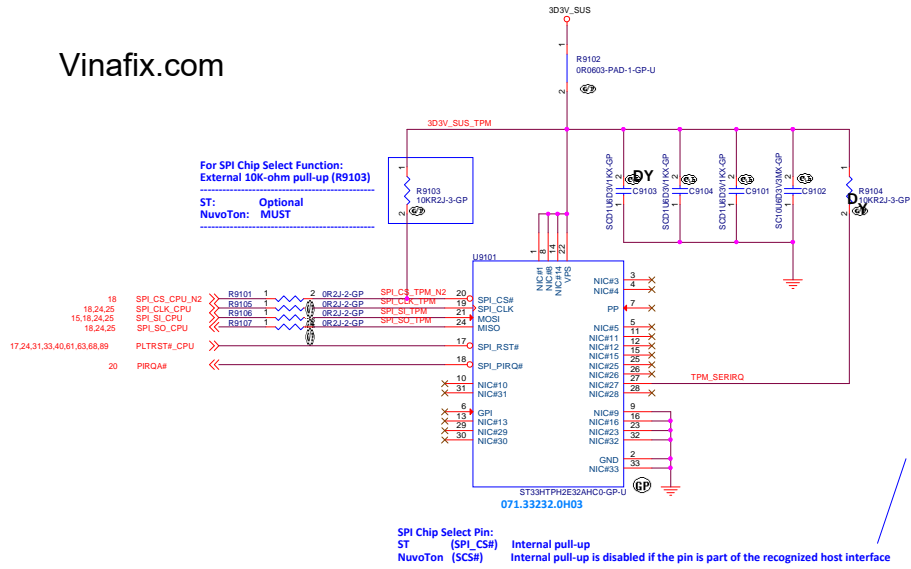
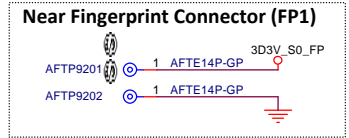
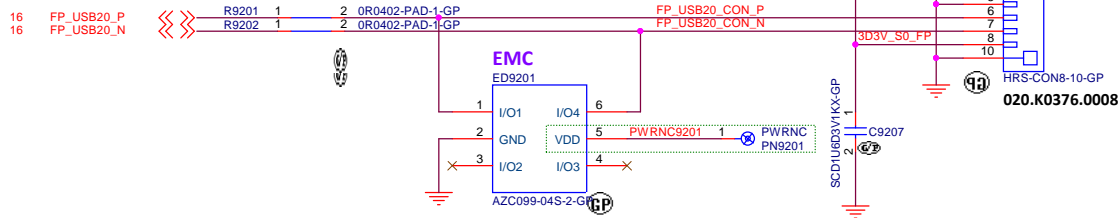
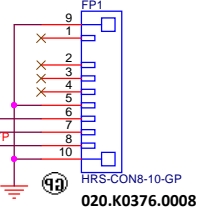


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1st	ST33HTPH2E32AHCO	071.33232.0H03
2nd	NPCT750LABYX	071.00750.0D03

TABLE				
		071.33232.0H03	071.00750.0D03	071.00750.0D03
Pin No	TCG PTP Spec(V38)	ST Micro ST33HTPH2E32AHCO	NuvoTon NPCT750LABYX	Indefinite
1	VDD	NC	VSB	VDD
2	GND	NC	NC	GND
3	NC	NC	NC	NC
4	GPIO	NC	GPIO/PP	GPIO
5	NC	NC	NC	NC
6	GPIO	NC	GPIO3	GPIO
7	GPIO	NC	NC	GPIO
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	NC
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	GPIO
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	GND
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CSH	SPI_CSH	SCSH/GPIO5	SCSH
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	SDA
30	SDA/GPIO0	NC	SCL/GPIO1	SCL
31	NC	NC	NC	NC
32	NC	NC	NC	NC



Fingerprint Connector



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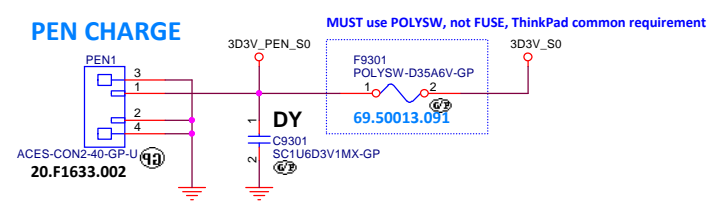
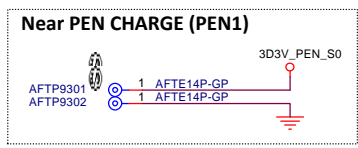
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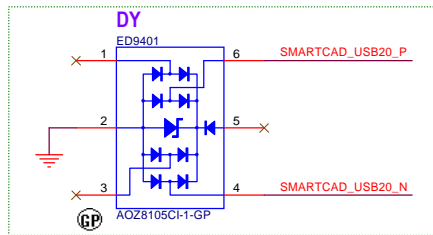
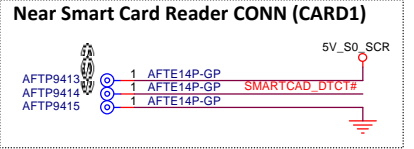
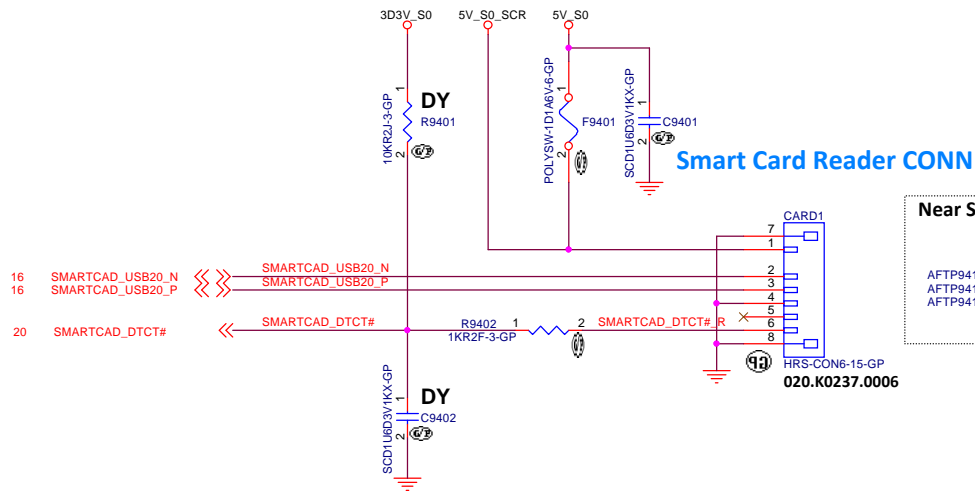
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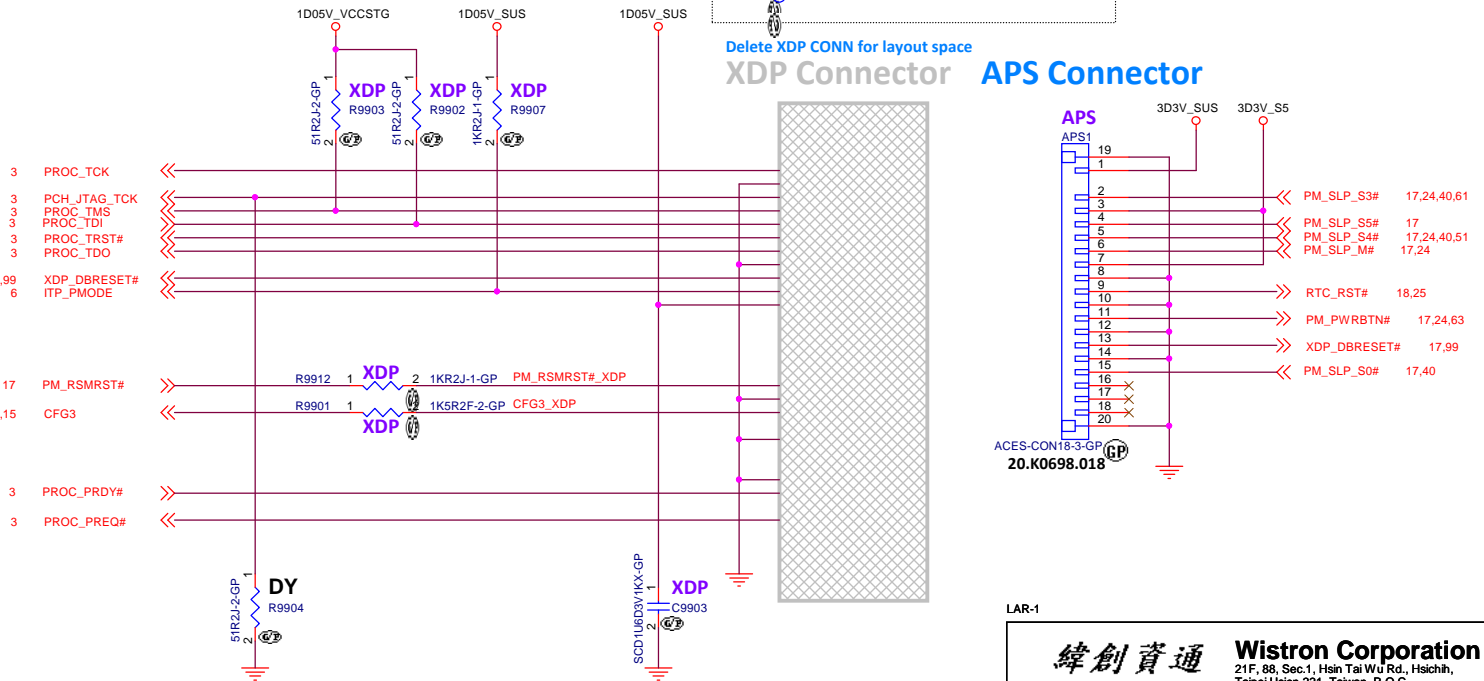
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XDP Test Point

TP9901	1	TPAD14-OP-GP	PROC_TCK
TP9902	1	TPAD14-OP-GP	PCH_JTAG_TCK
TP9903	1	TPAD14-OP-GP	PROC_TMS
TP9904	1	TPAD14-OP-GP	PROC_TDI
TP9905	1	TPAD14-OP-GP	PROC_TRST#
TP9906	1	TPAD14-OP-GP	PROC_TDO
TP9907	1	TPAD14-OP-GP	XDP_DBRESET#
TP9908	1	TPAD14-OP-GP	ITP_PMODE
TP9909	1	TPAD14-OP-GP	1D05V_SUS
TP9910	1	TPAD14-OP-GP	PM_RSMRST#_XDP
TP9911	1	TPAD14-OP-GP	CFG3_XDP
TP9912	1	TPAD14-OP-GP	PROC_PRDY#
TP9913	1	TPAD14-OP-GP	PROC_PREQ#

Delete XDP CONN for layout space

XDP Connector APS Connector



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Title **DEBUG (XDP/APS)**

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