LCFC NM-C921

Y550 M/B Schematics Document

Comet Lake H-Processor with DDR4 + NV N18P-G61/G62 GPU

2019-12-16

REV:1.0

Security Classification	LC Future Center Secret Data		
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Title: Cover Page		
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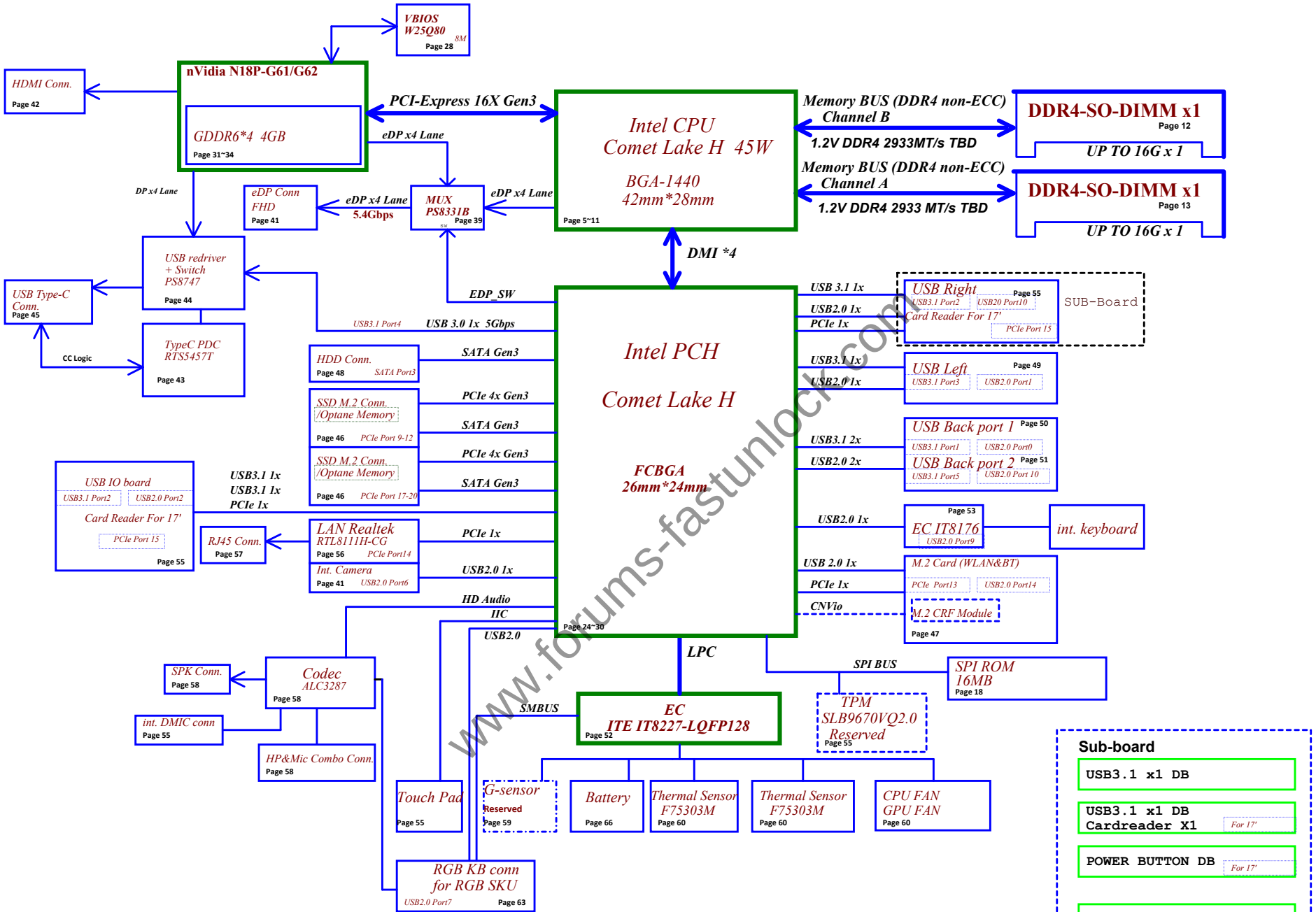

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Title	Block Diagram		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
i5@i7@i9@	CPU Part
PRC@	PRC
WW@	Worldwide
OPT@	NV GPU part
M4GX4@S4GX4@	VRAM part
N18PG61@	N18PG61 PART
N18PG62@	N18PG62 PART
GYSNC@	GSYNC support part
DDS@	Dynamic Display Switch part
MUX@	EDP MUX Switch part
MUX1@	Colay DDS and MUX
HDMI@	HDMI logo
CNVI@	CNVi support part
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
EMC_8111H@	LAN 8111H EMC Part
AG@	Anti-ghost Part
BL@	BL Part
RGB@	RGB Part
MP@	Mass Production Stage Part

BOM Structure	BTO Item
USB@	USB2.0 port1 for USB Port
NPI@	NPI stage stuff
DCI@	DCI
Debug@	USB2.0 port 1for Debug
TPM@	For support TPM sku part
GS@	Reserved for G-sensor
OPTANE@	For Optane SKU stuff
MIRROR@	MIRROR
NOMIRROR@	No MIRROR
ME@	ME part(connector)
EMC@	EMC part
EMC_NS@	EMC not stuff
RF@	RF part
RF-NS@	RF No part
CD@	Cost down part
UP9632_@	UP9632 part stuff

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7	RGB
8	NA
9	AG
10	Back USB3.0
11:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Right USB3.0(DB)
3	Left USB3.0
4	Type-C Port
5	Back USB3.0
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	NA
1B	NA
2	NA
3	HDD Gen3
4	NA
5	NA
7	NA

PCIE Port table	
Port	Function
1:8	NA
9:12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15	Card Reader
17:20	M.2 SSD/Optane

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Title: **Notes List**

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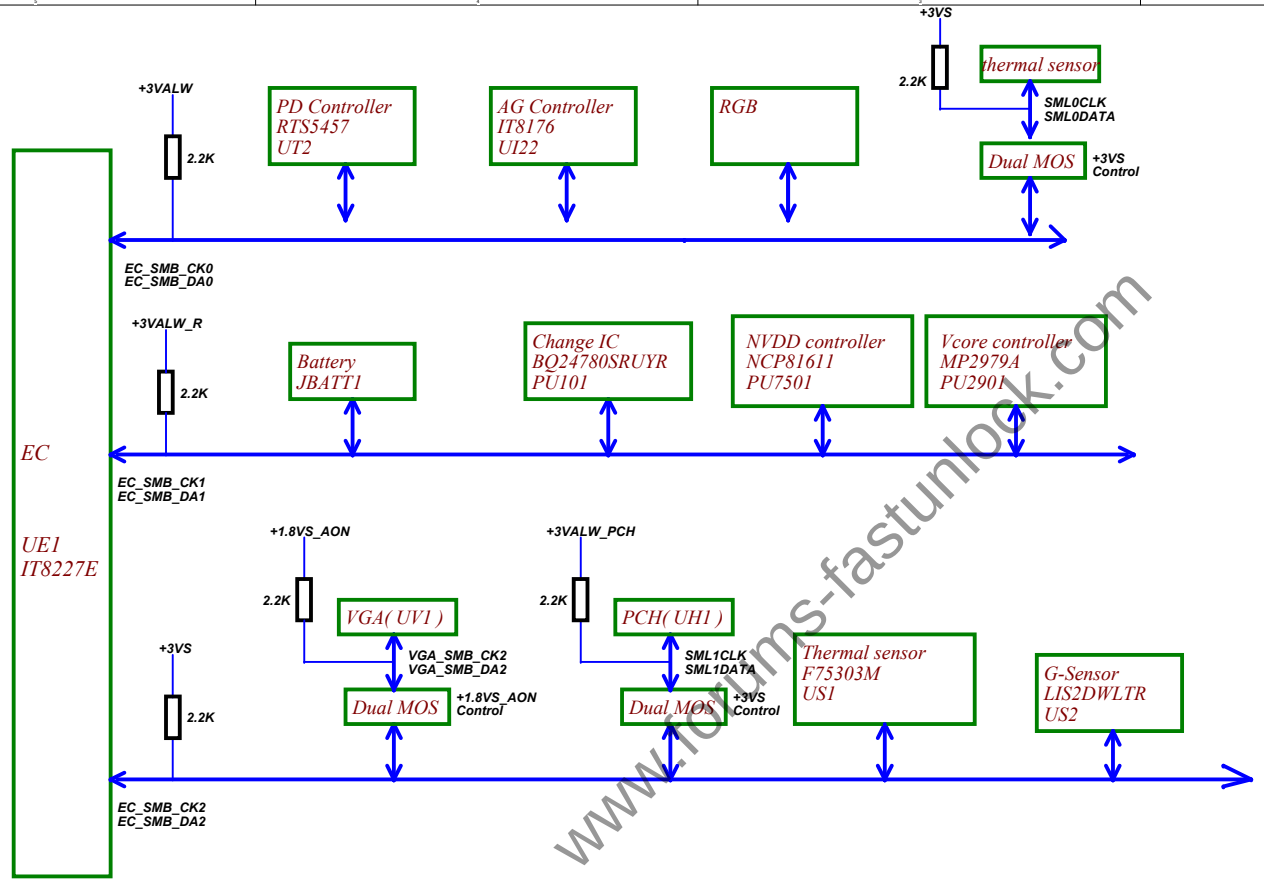


SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

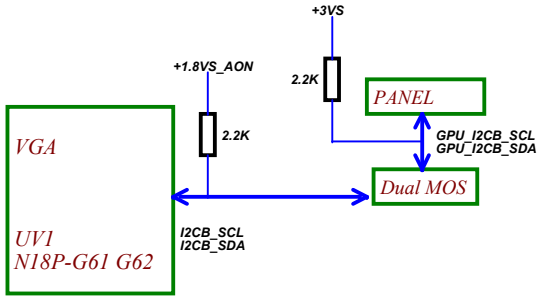
Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update
Thermal Sensor NCT7718M	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update



Security Classification	LC Future Center Secret Data		Title: I2C Block
Issued Date	2018/08/02	Deciphered Date	2018/08/02
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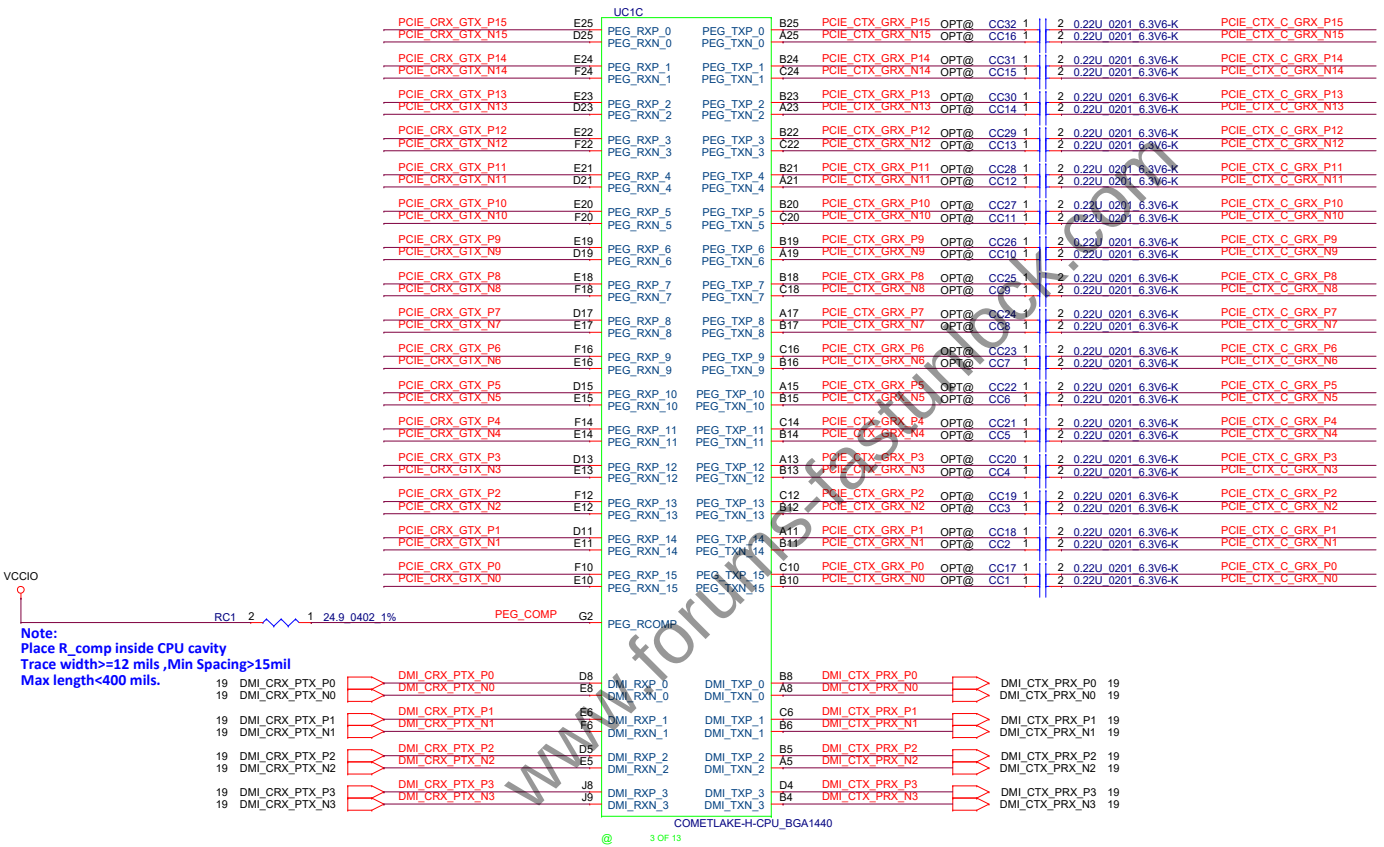
25 PCIE_CRX_GTX_N[0..15]

25 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] 25

PCIE_CTX_C_GRX_P[0..15] 25



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Title: CPU (1/7) DMI,PEG

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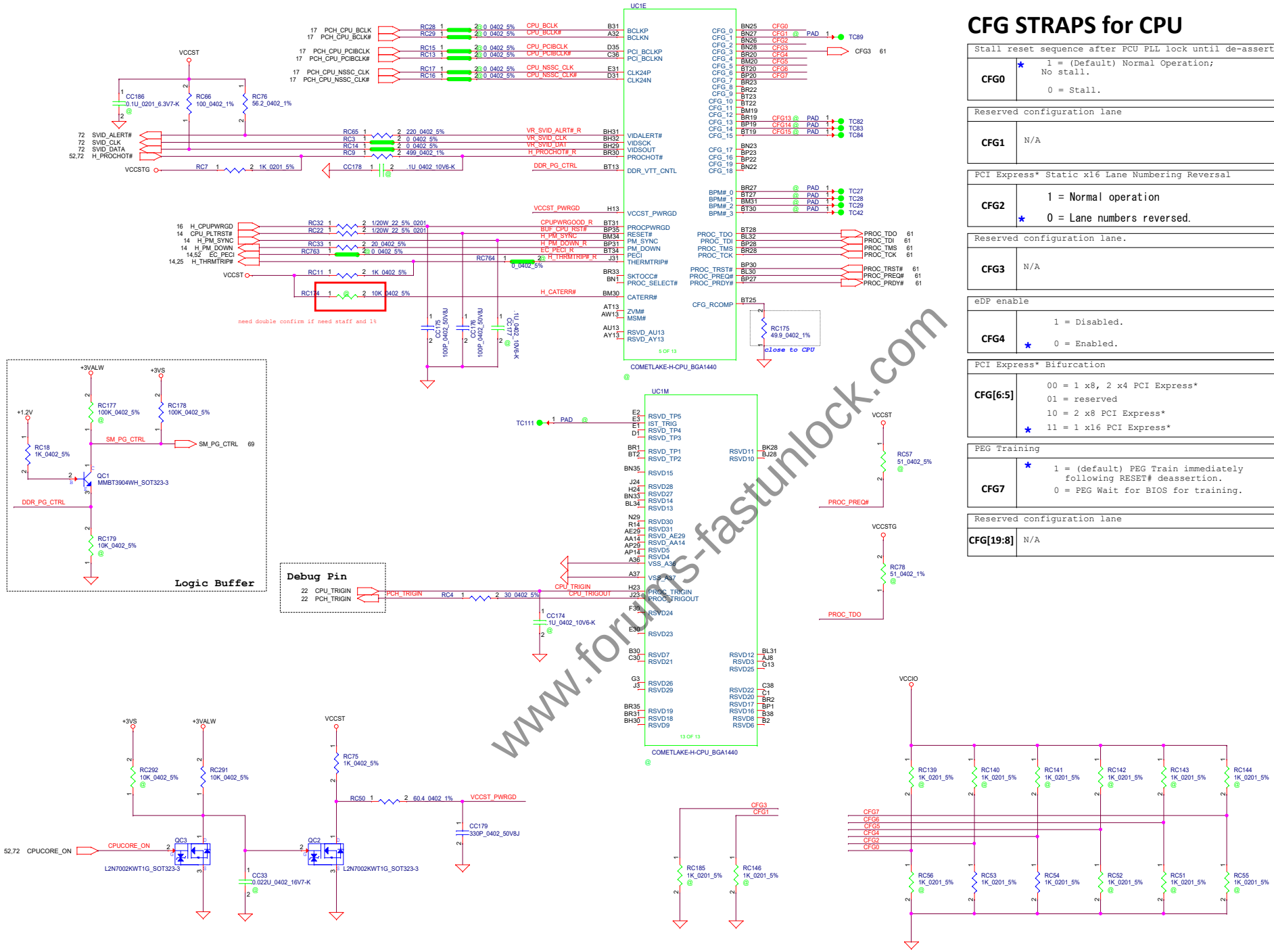

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.
Reserved configuration lane.	
CFG3	N/A
eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*
PEG Training	
CFG7	* 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.
Reserved configuration lane	
CFG[19:8]	N/A

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Title	CPU (2/7) PM, XDP, CLK, CFG		
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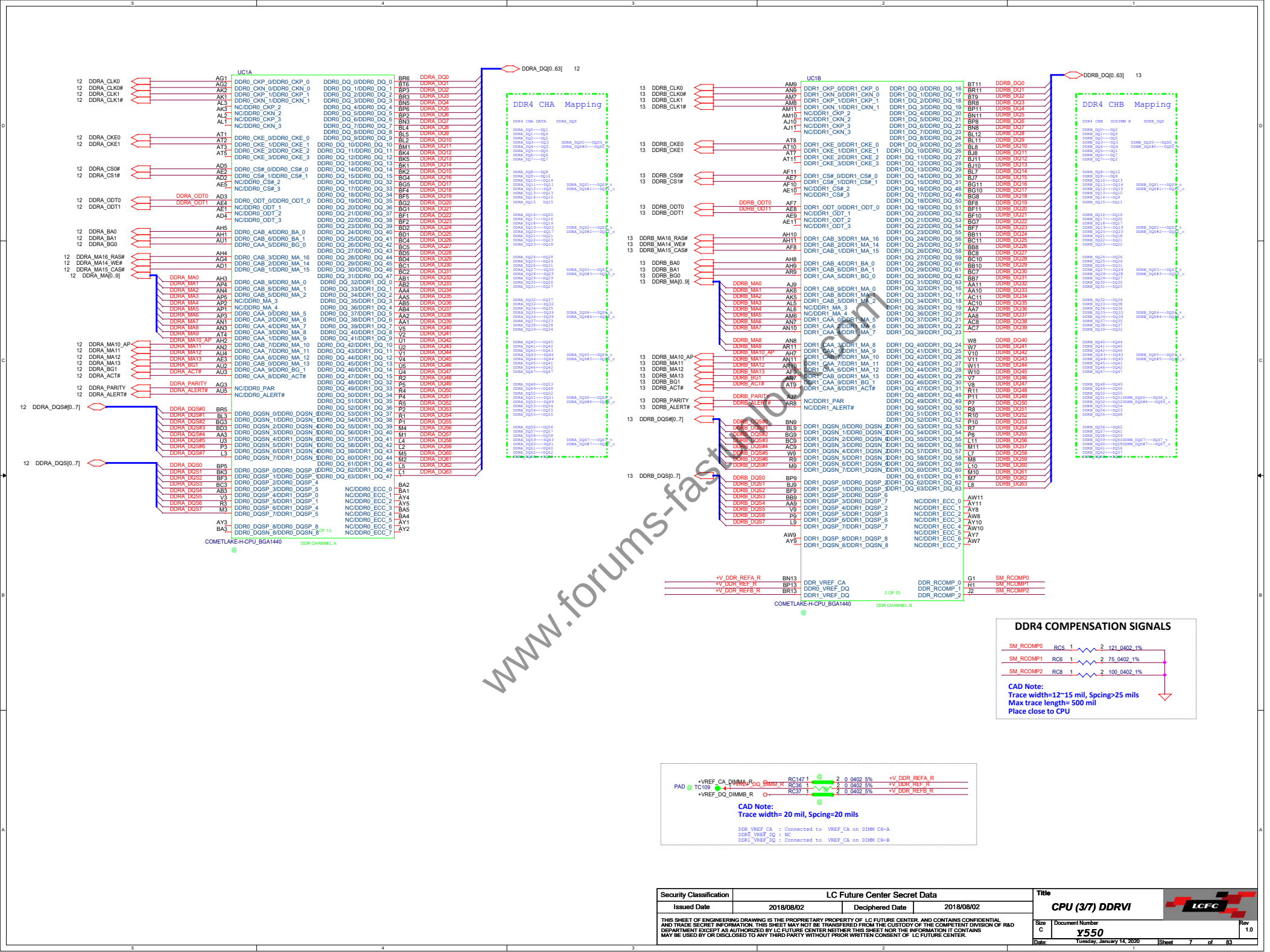

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	¥550	1.0

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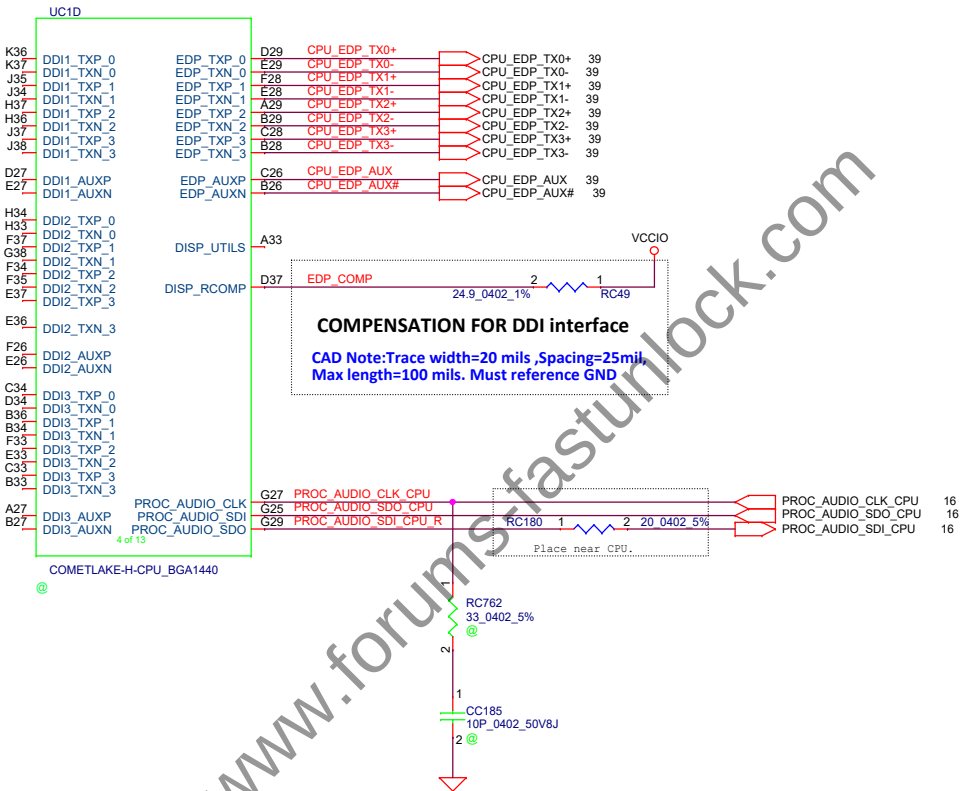

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *CPU (4/7) eDP, DDI*

Size	Document Number	Rev
A3	¥550	1.0

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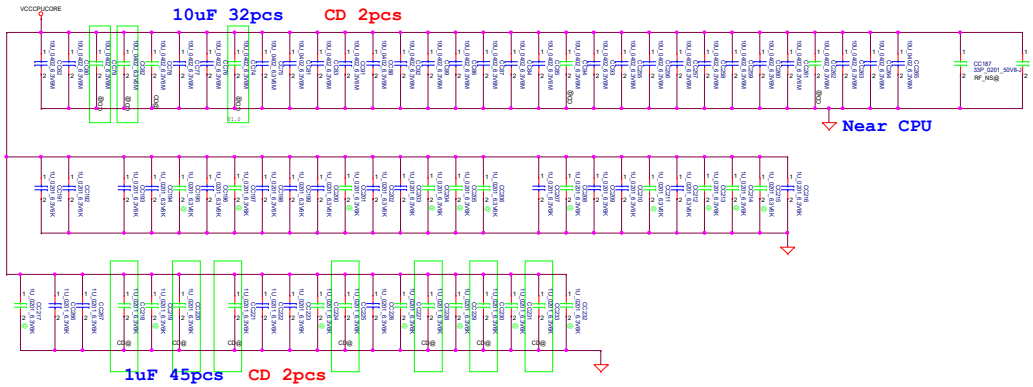
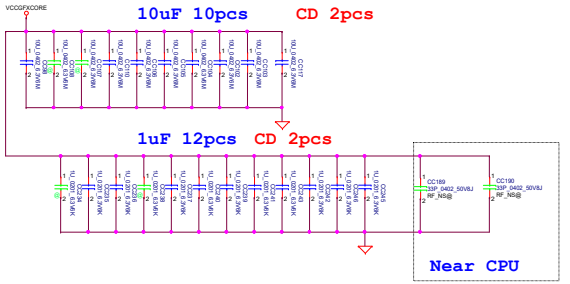
PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45



PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45



Security Classification	LC Future Center Secret Data		Title
Issued Date	2018/08/02	Deciphered Date	2018/08/02
			CPU (5/7) PWR, BYPASS

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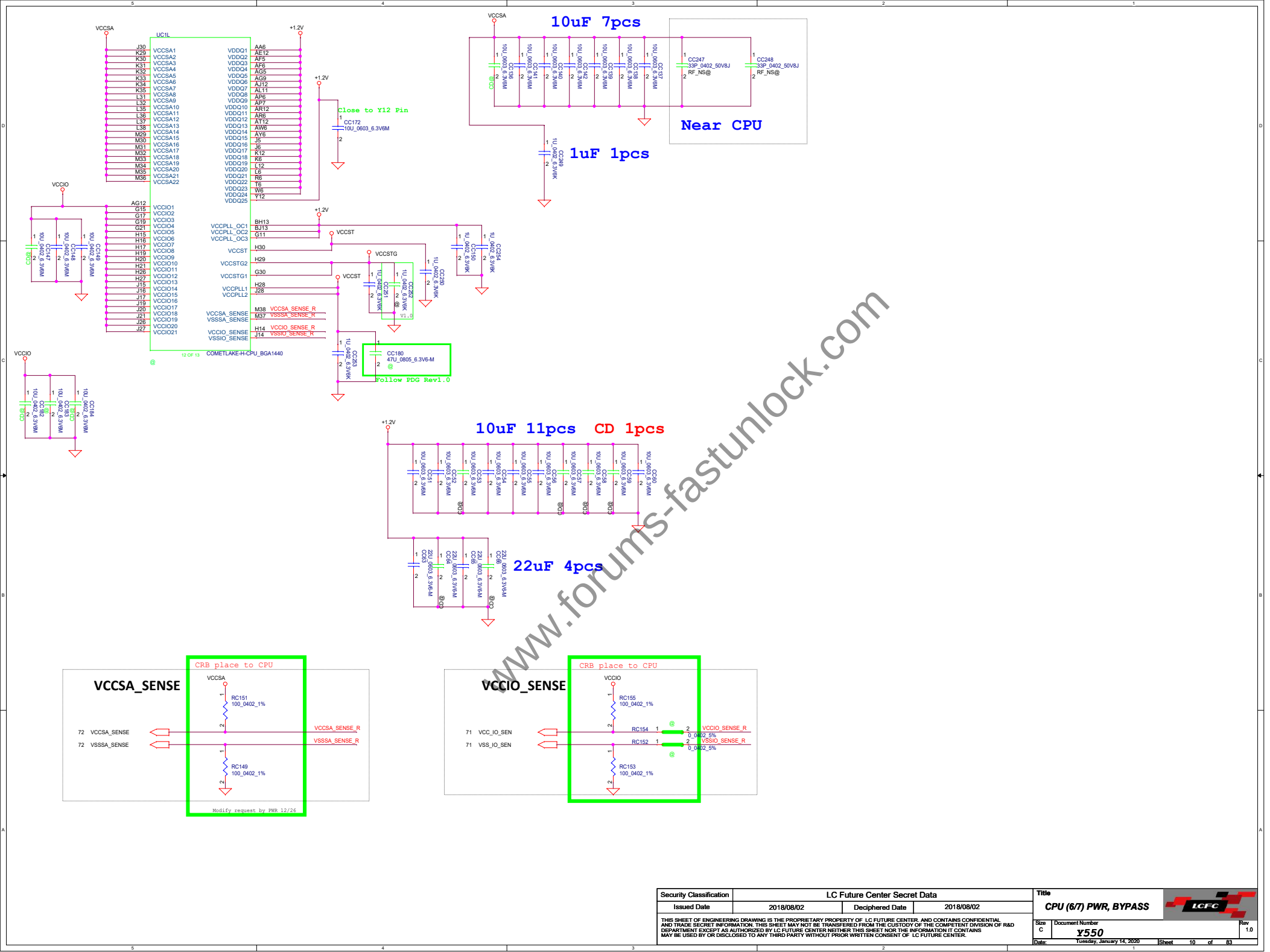

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Title: CPU (6/7) PWR, BYPASS

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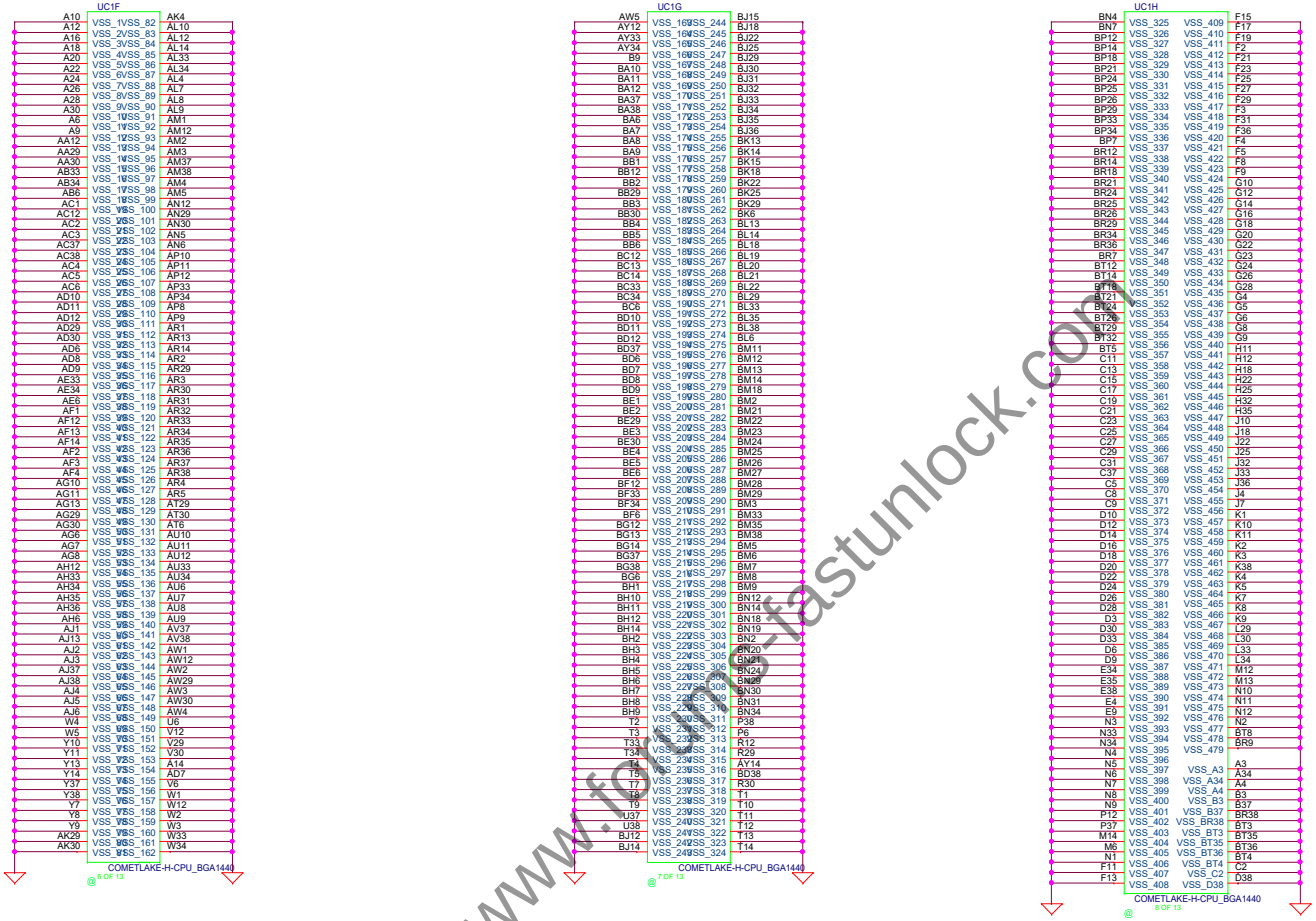

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Title: **CPU (6/7) PWR, VSS**

Size	Document Number	Rev
C	¥550	1.0

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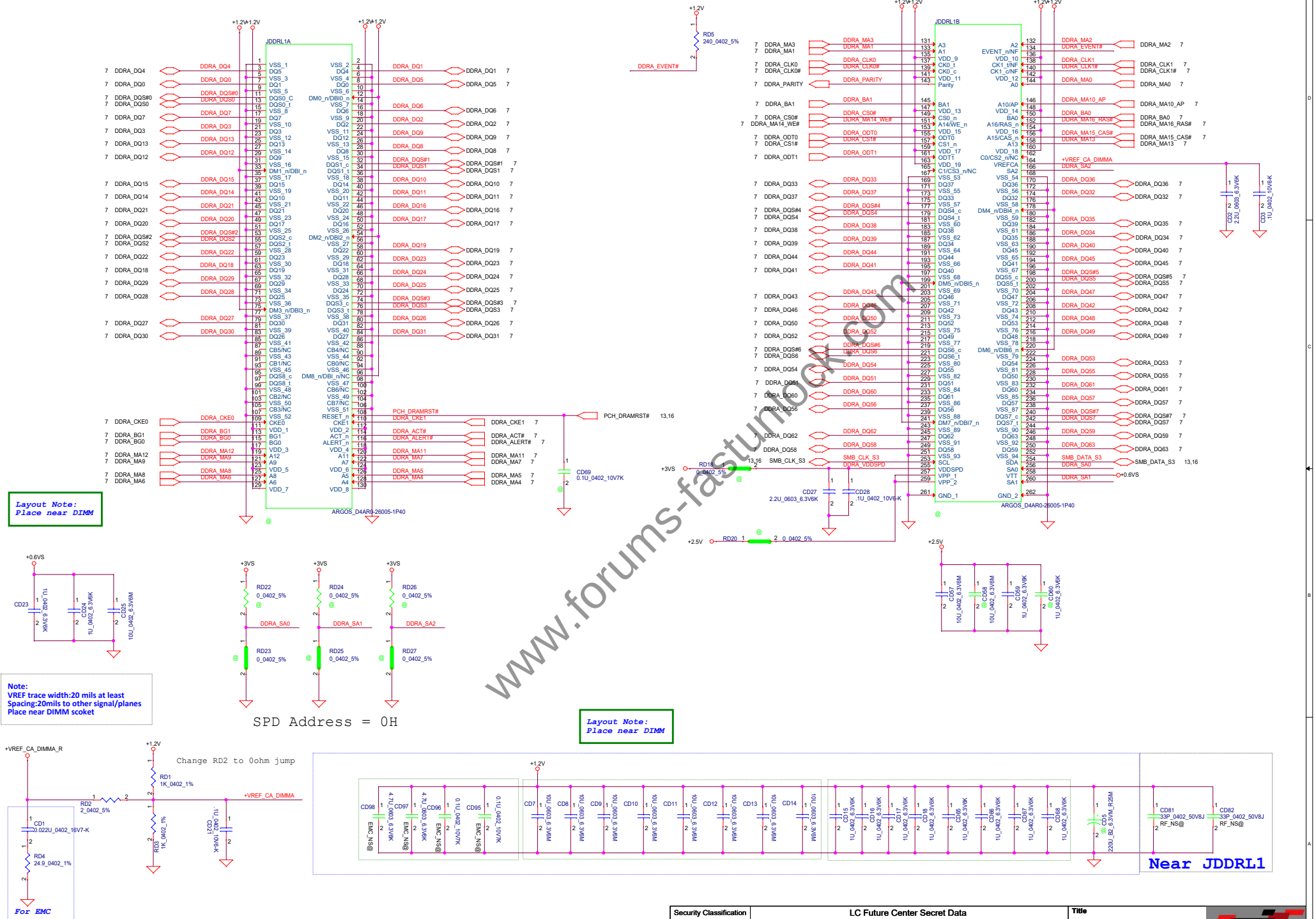
DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDRVI SO-DIMM A		
Size	Document Number		Rev
C	Y550		1.0
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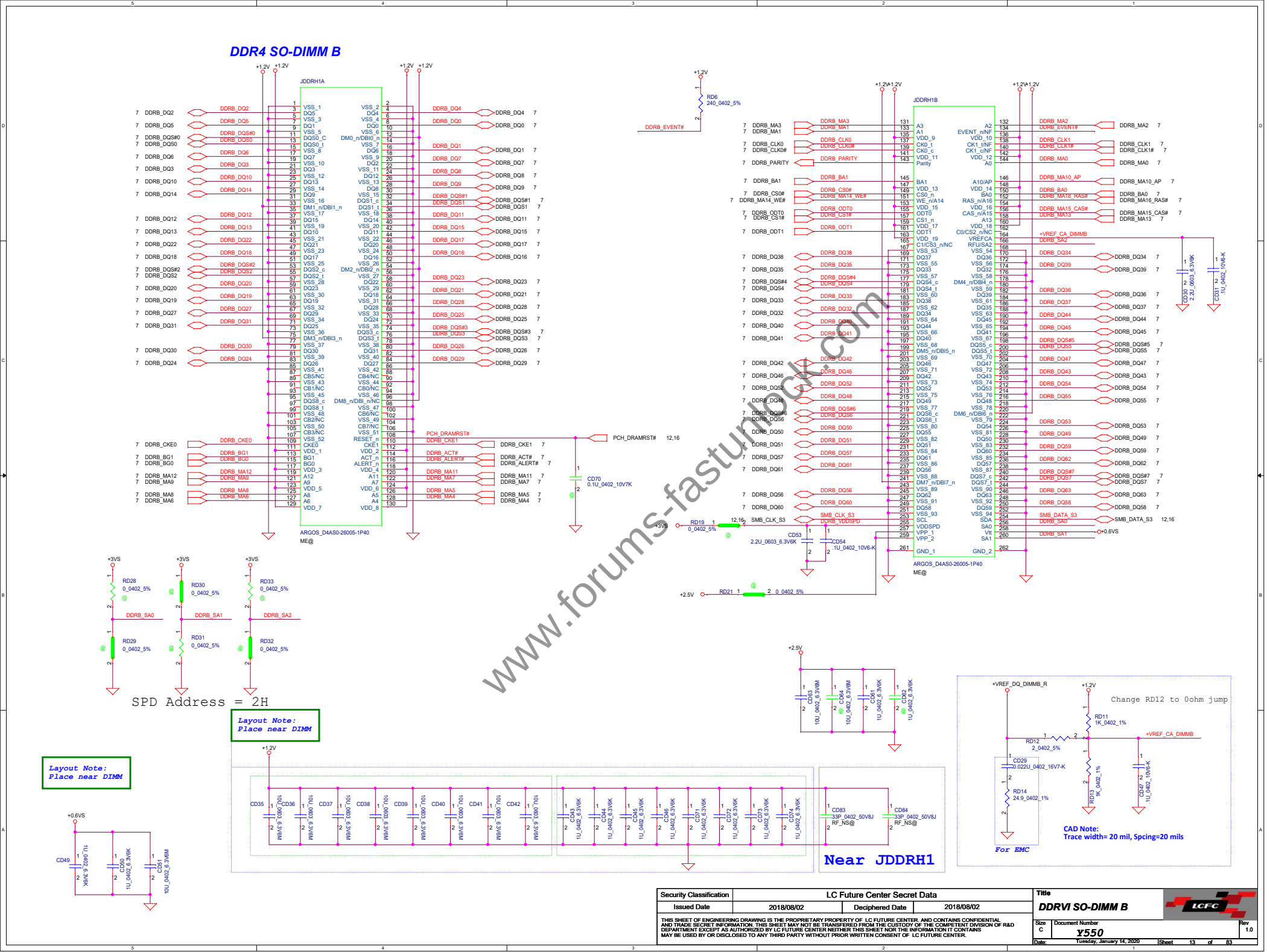
DDR4 SO-DIMM B



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Title	DDRVI SO-DIMM B		
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C	Y550		1.0
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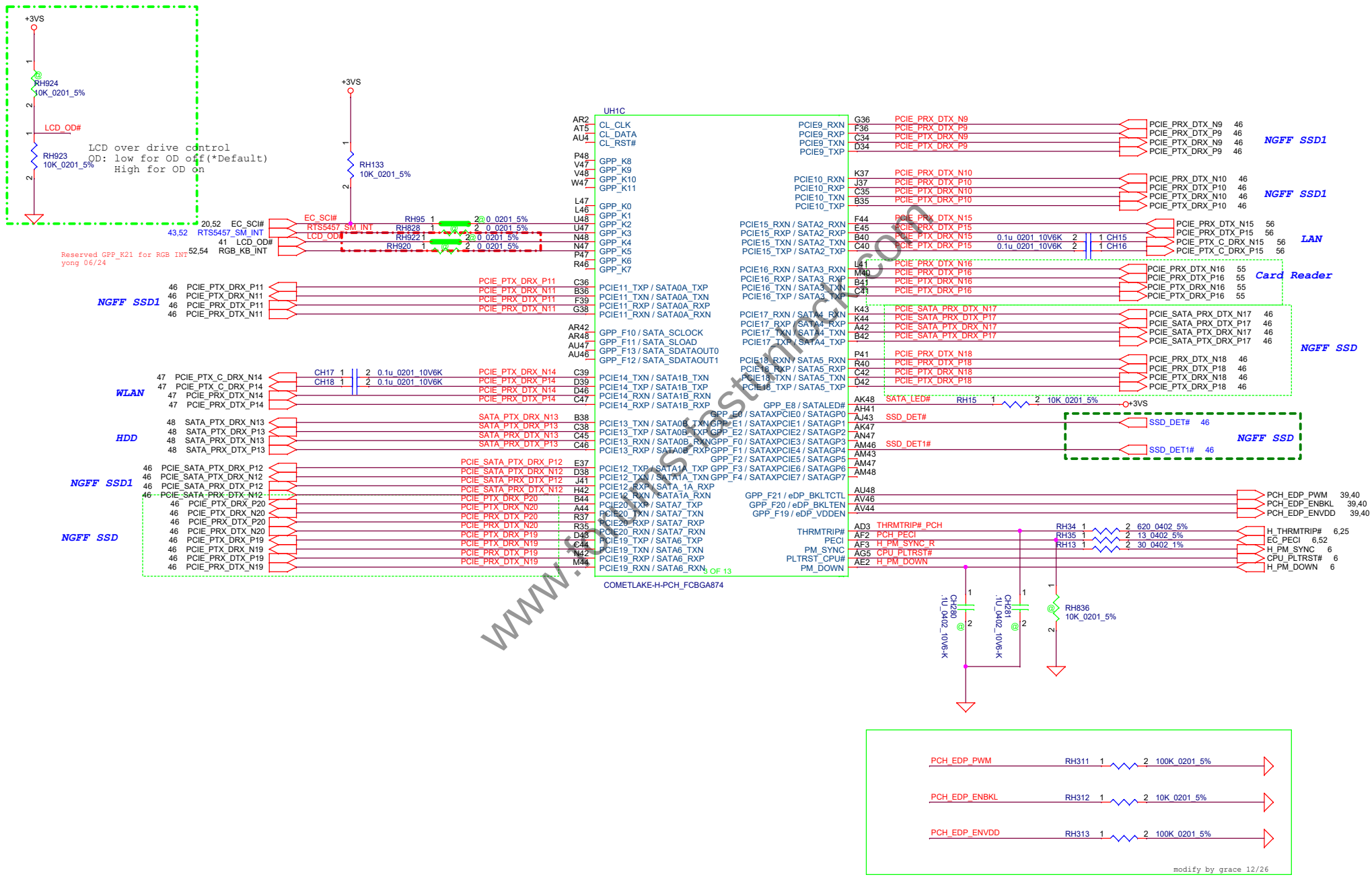

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Title: **PCH (1/9) PCIe/SATA/GPPFG**

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A3	¥550	1.0

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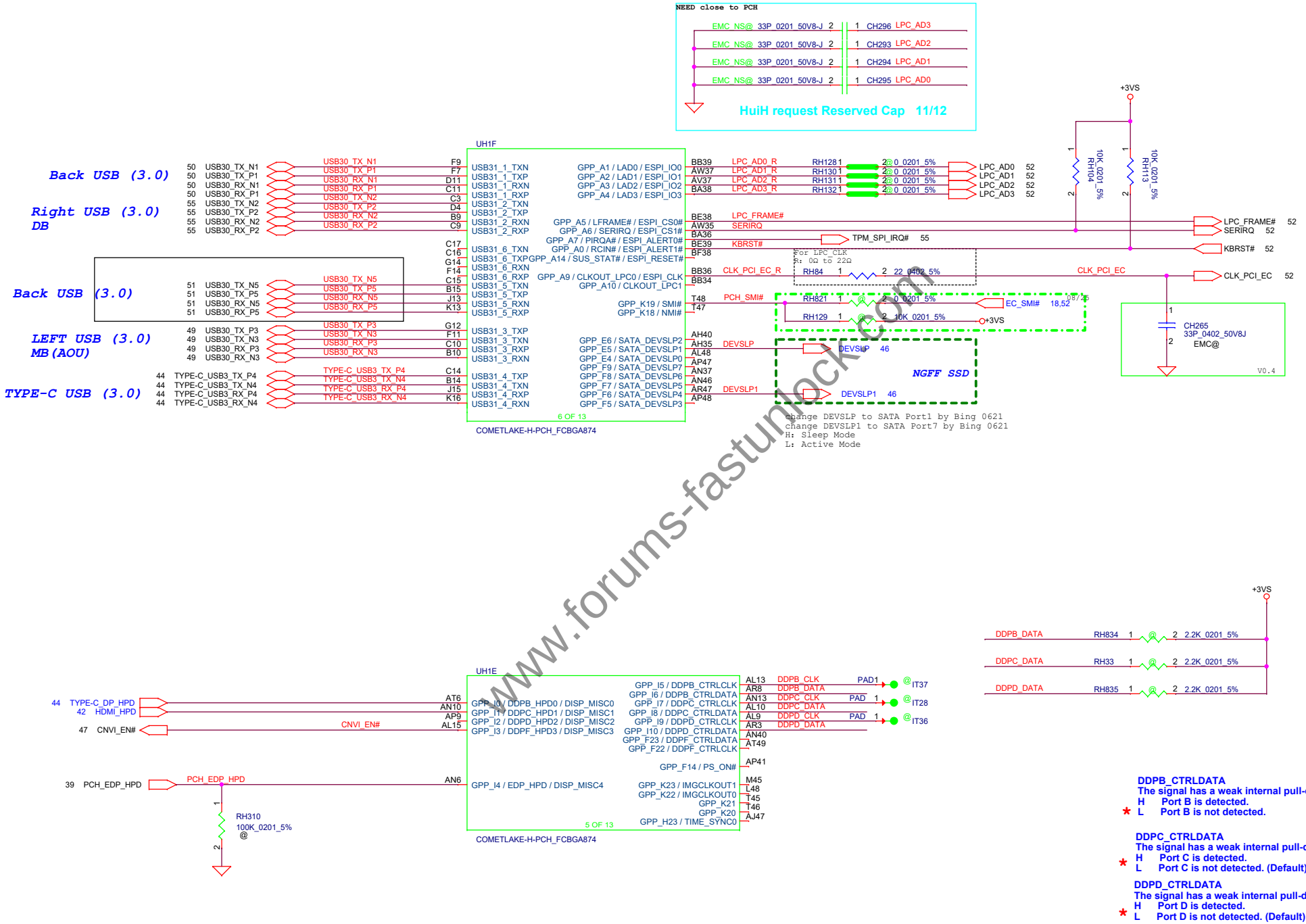

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
A3	Y550	1.0

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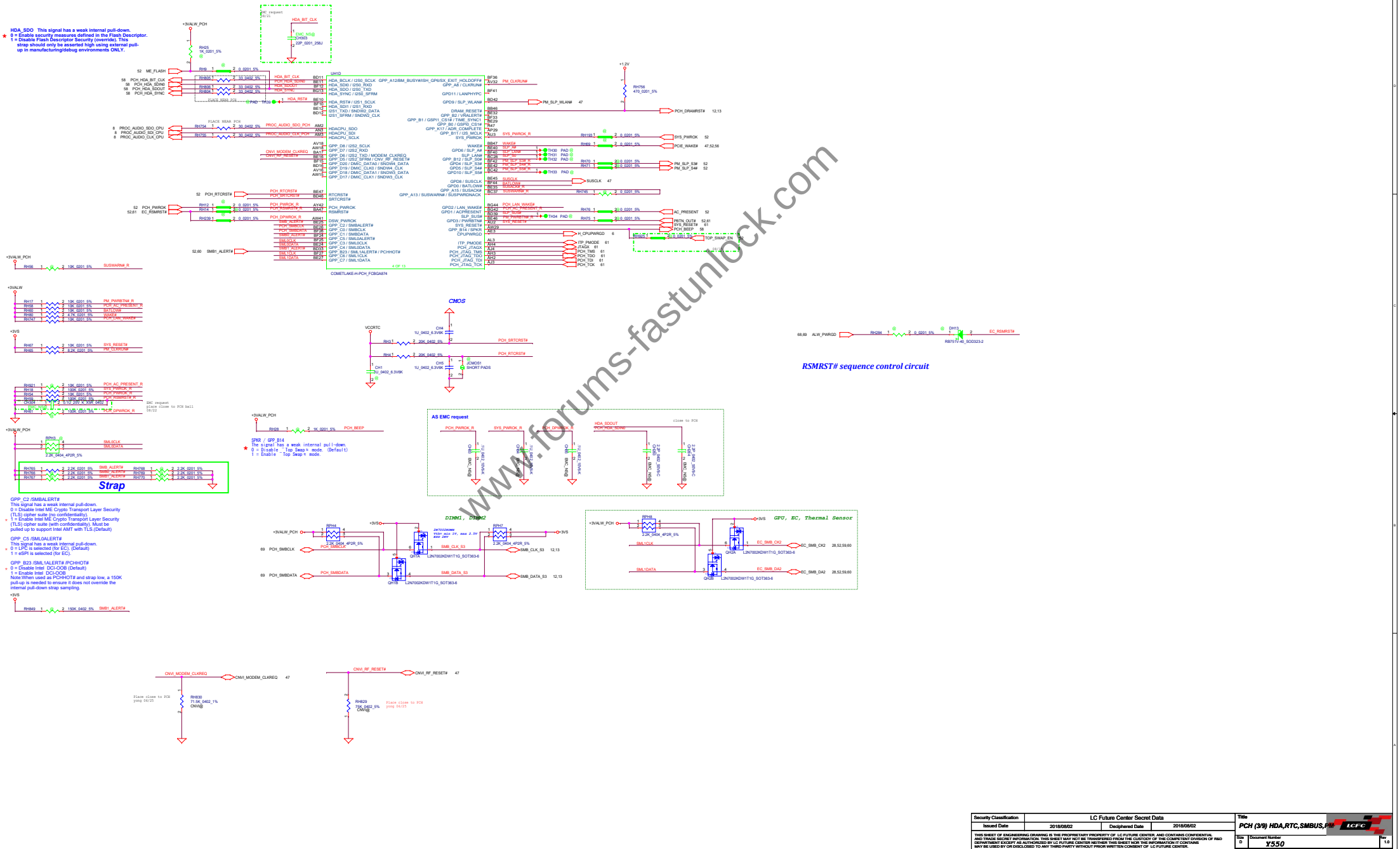

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Title	PCH (3/9) HDA,RTC,SMBUS,PM		
Size	Document Number		Rev
D	¥550		1.0
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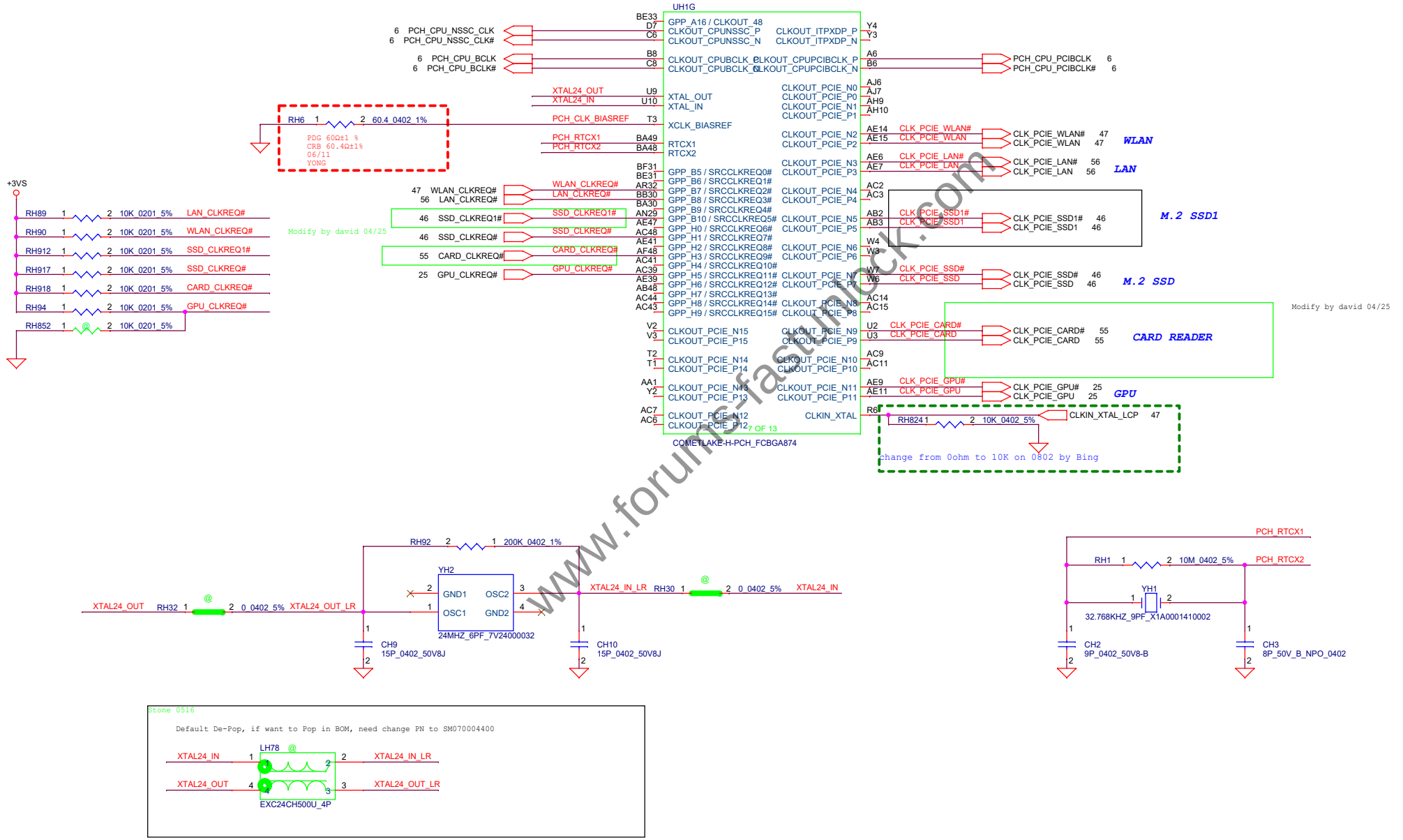

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (3/9) CLOCK,GPPBH**

Size	Document Number	Rev
A3	Y550	1.0

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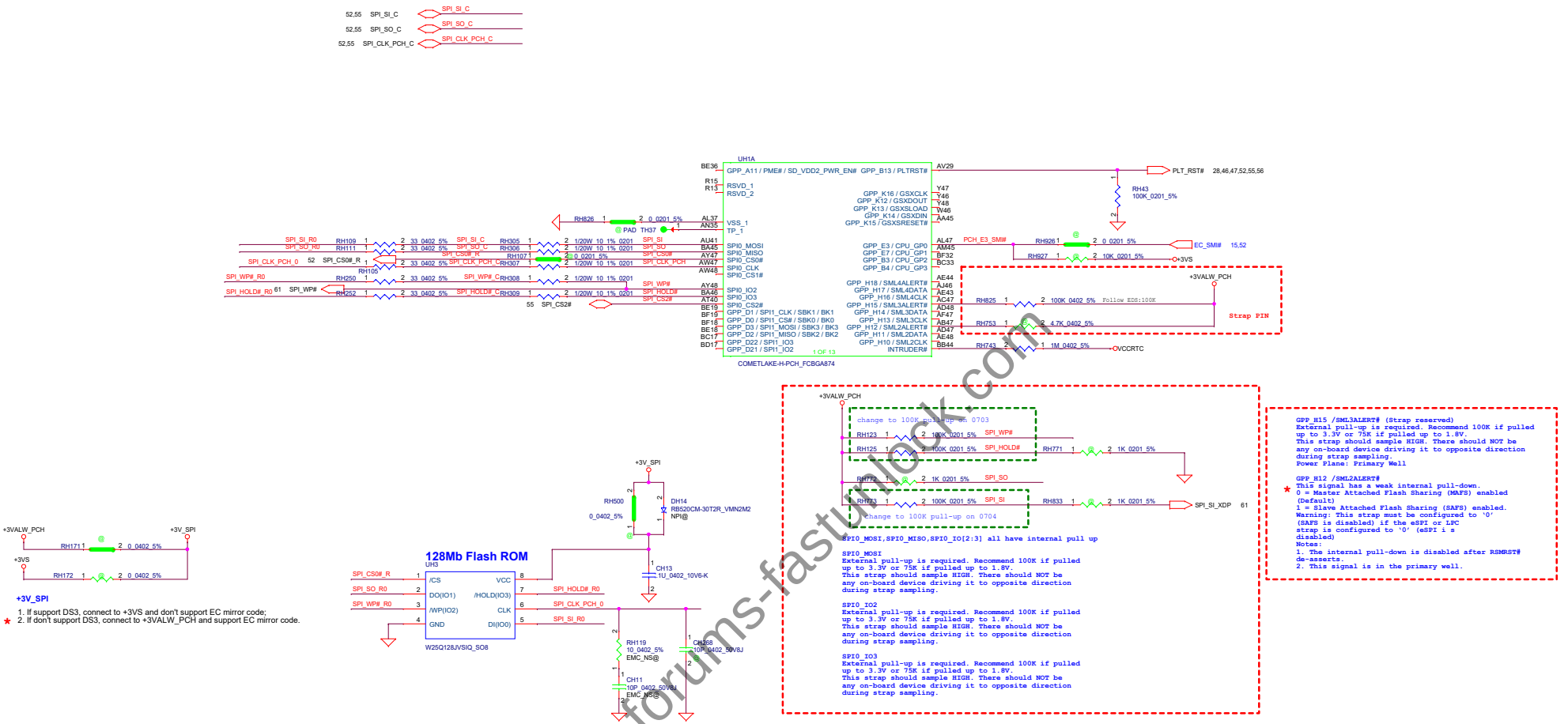

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Title: PCH (5/9) SPI,SMBUS,GPPBEGH

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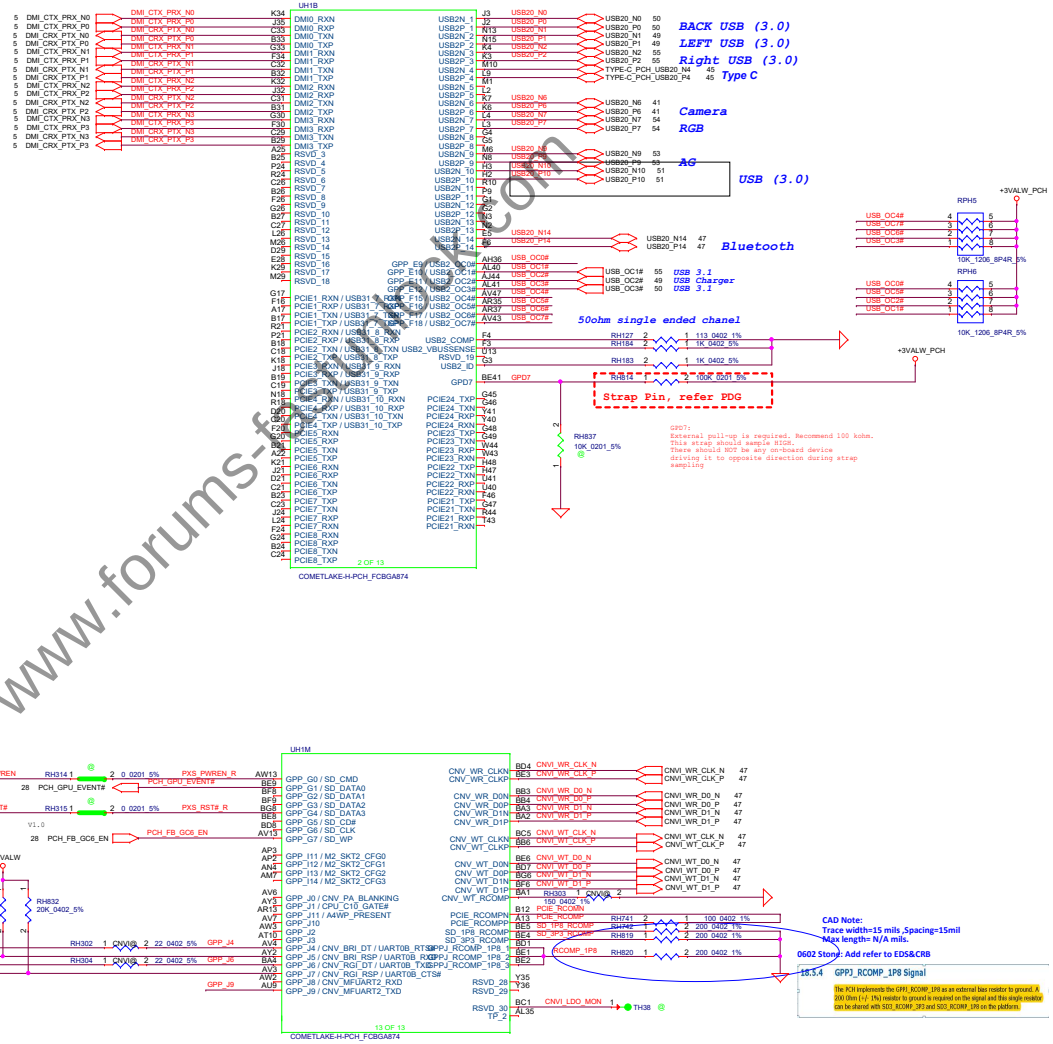
Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os



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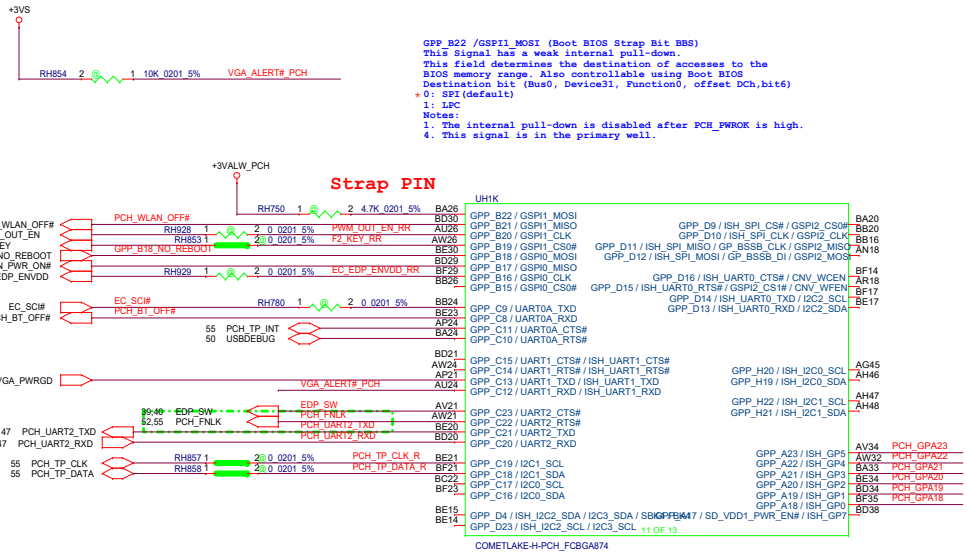
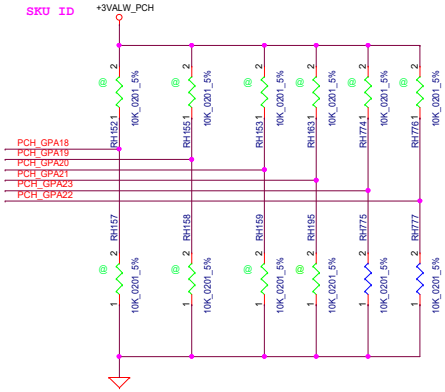
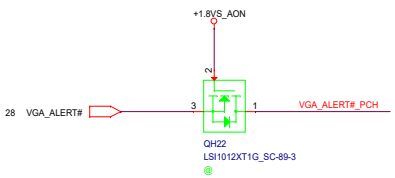
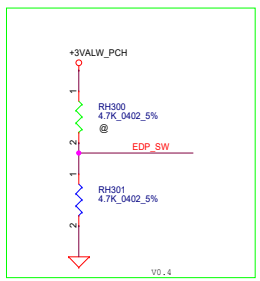


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC







Board ID table need modify
yong 07/10

PCH_GPA22 add for distinguish
L350: H
Y550:L
yong 07/11

Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22 (L340: H Y550: L)	PCH_GPA23 (Reserved)
Y550-15-N18E G0	0	0	0	0	0	0
Y550-15-N18E G1	0	0	0	1	0	0
Y550-15-N18P G61	0	0	1	0	0	0
Y550-15-N18P G62	0	0	1	1	0	0
Y540-17-N18E G0	0	1	0	0	0	0
Y540-17-N18E G1	0	1	0	1	0	0
Y540-17-N18P G61	0	1	1	0	0	0
Y540-17-N18P G62	0	1	1	1	0	0

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Title: PCH (6/9) GPPPABCD, I2C

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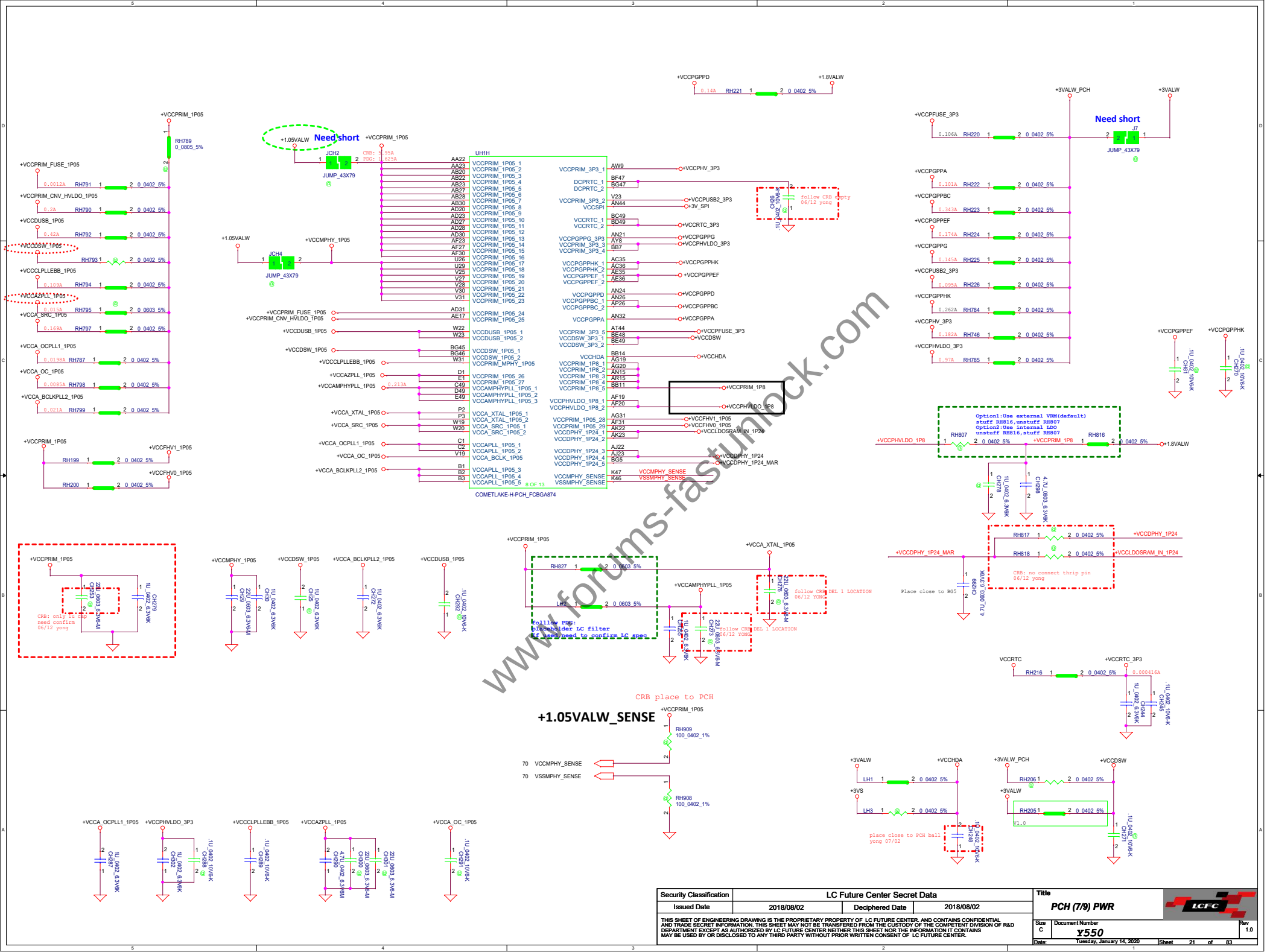

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PCH (7/9) PWR		
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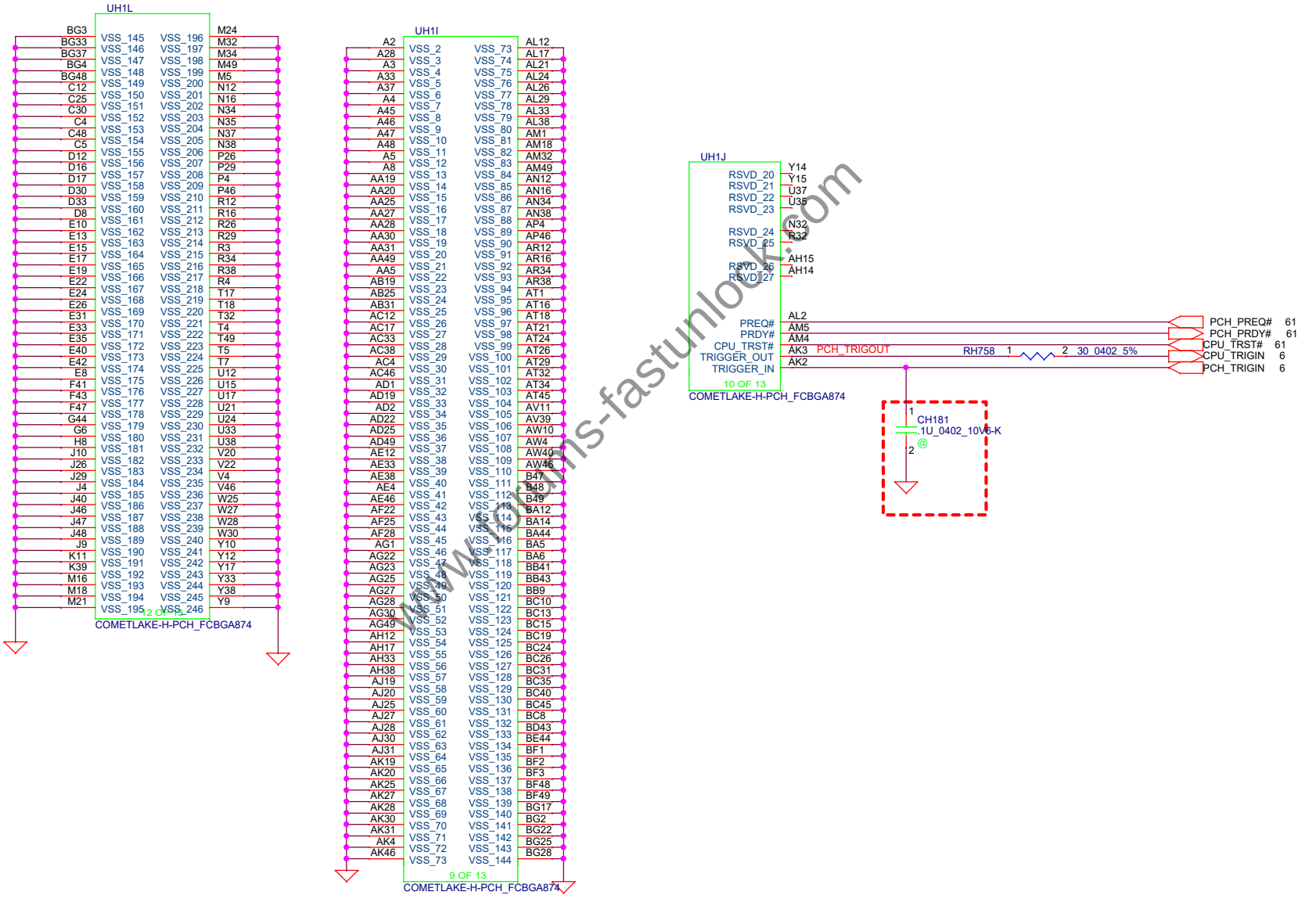

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PCH (9/9) VSS**

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Title: ***Blank***

LCFC

Size	Document Number	Rev
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N18P-G61 G62 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU EVENT	
GPIO3	OUT	-	GPU MUX controler	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight (PWM)enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power (LCD_VDD)enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	IN	N/A	IGPU Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA(TYPE-C)	
GPIO15	IN	N/A	Hot Plug Detect for IFPB(NA)	
GPIO16	OUT	-	DGPU PWM switch select	
GPIO17	IN	N/A	Hot Plug Detect for IFPD(DGPU eDP HPD)	
GPIO18	IN	N/A	Hot Plug Detect for IFPE(NA)	
GPIO19		N/A	NA	
GPIO20		N/A	GC6_MODE	
GPIO21	O	N/A	DGPU Backlight Enable	
GPIO22	O	N/A	ADC MUX select	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24		N/A	NA	
GPIO25			FVDDQ_PSI	
GPIO26		N/A	FP-FUSE	
GPIO27	IN	N/A	Hot Plug Detect for IFPC(HDMI)	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

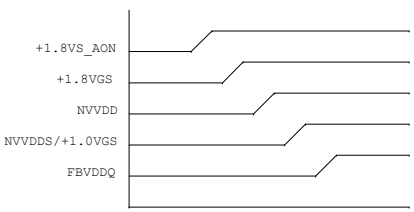
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N18P-G61 G62 Power Sequence

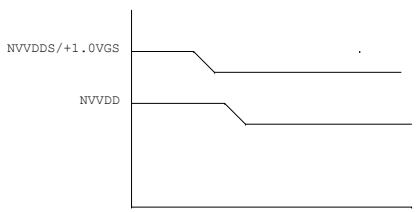


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

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Title: VGA Notes List

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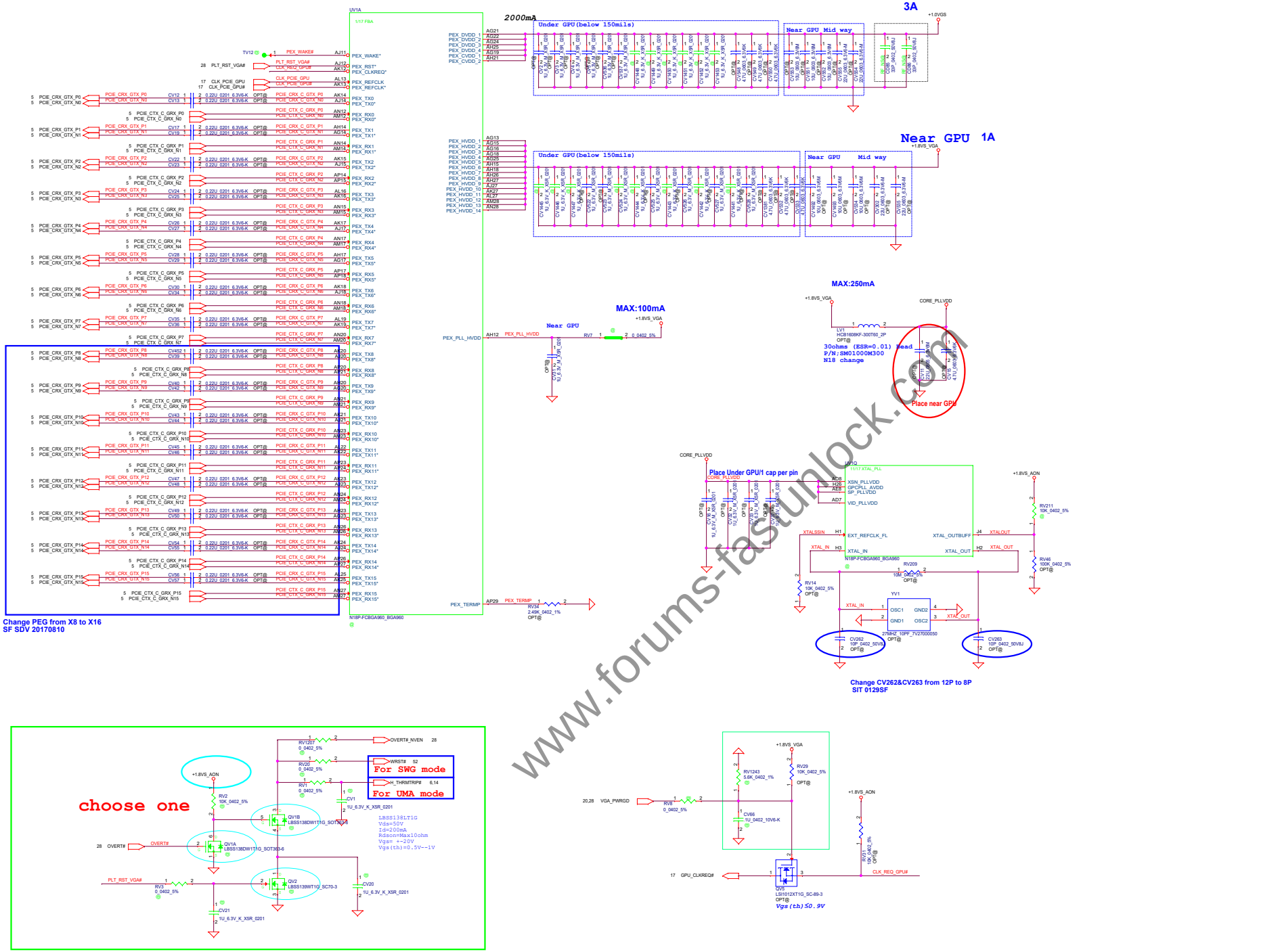

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_(1/6):PEG I/F		
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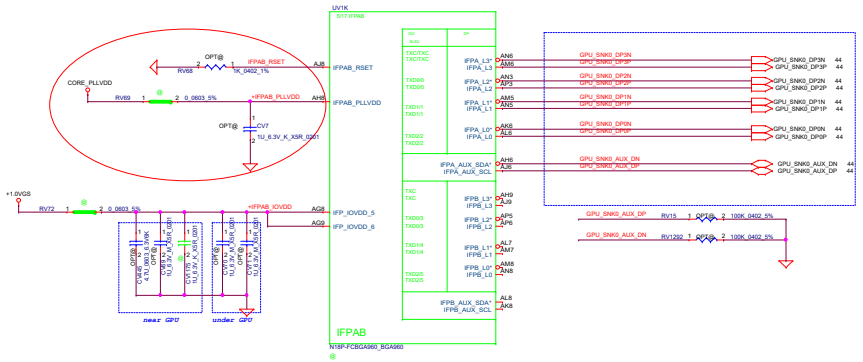
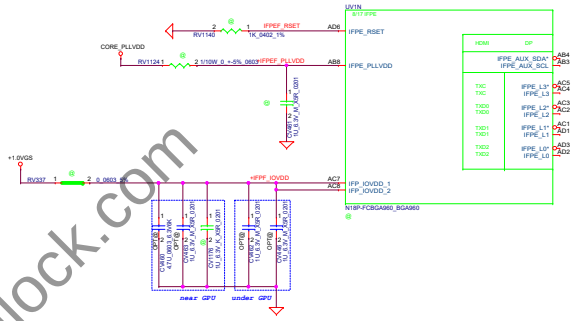
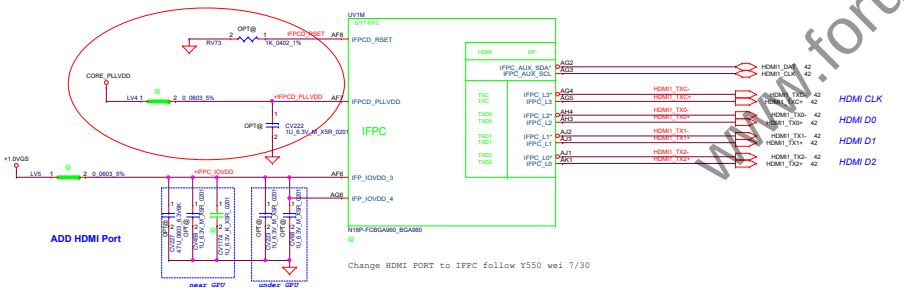
Ref NV DG-08780-001
If an IFP link is unused, in general it should be left unconnected.
This includes Main and Aux links.
IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF)
can be left unconnected if neither of IFPx /IFPy is in use



for Type-C DP





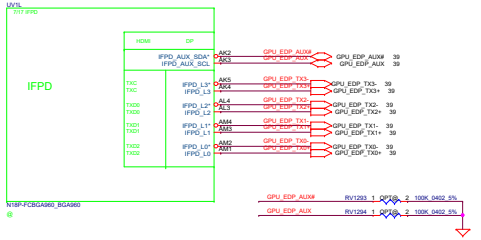
ADD HDMI Port

Change HDMI PORT to IFPC follow Y550 wei 7/30

For HDMI

Decoupling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV461	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV462	1uf	0.1uf	Under
CV484	1uf	0.1uf	Under



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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_(3/6):VRAM I/F		
Size: D	Document Number: Y550		Rev: 1.0
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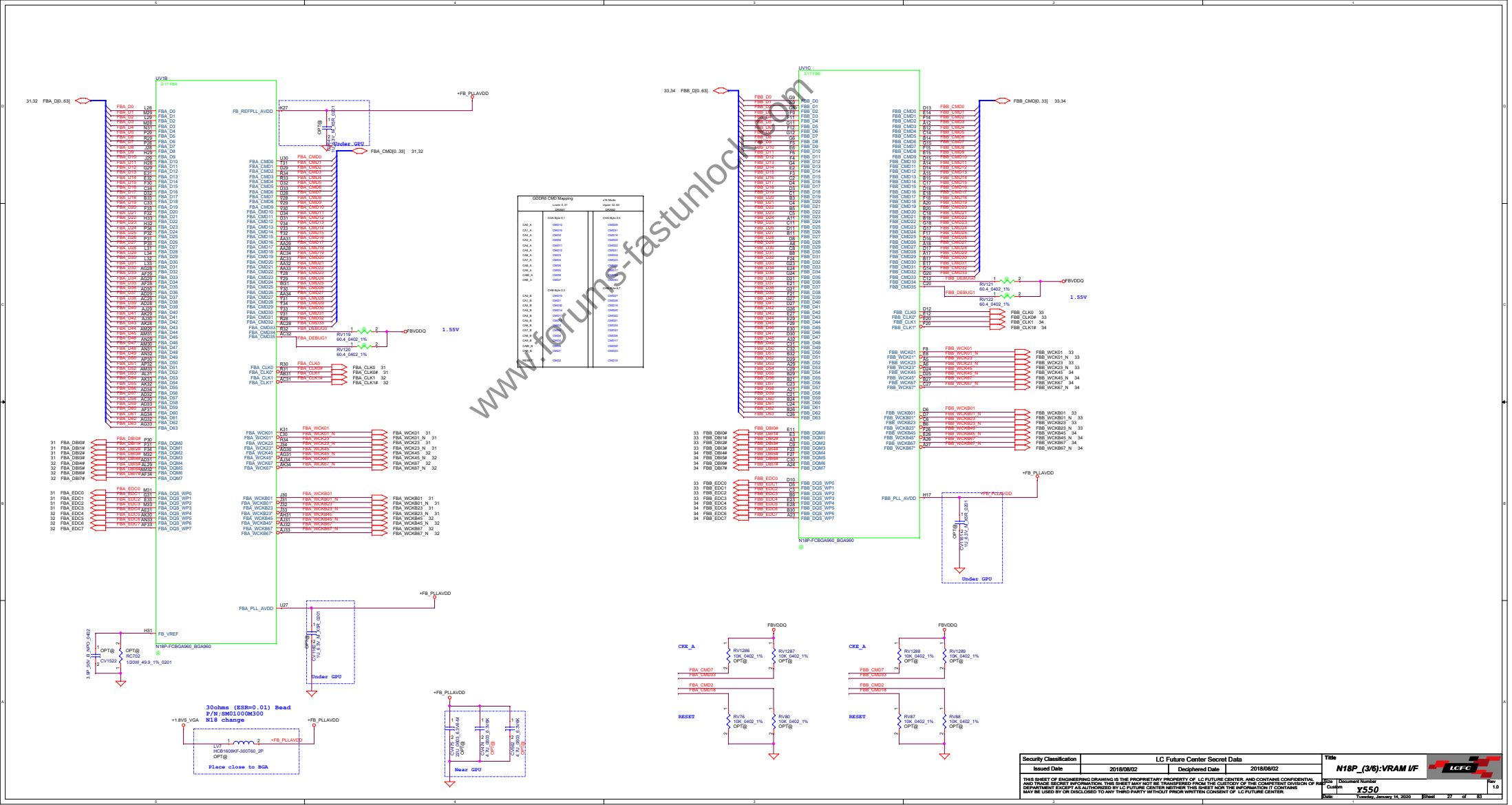

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Title: N18P_(3/6):VRAM I/F

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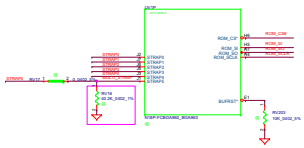
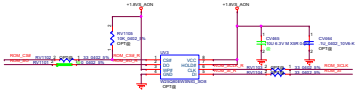
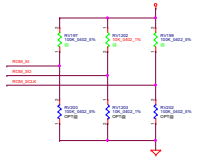
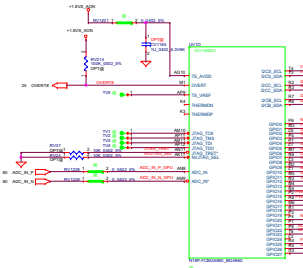


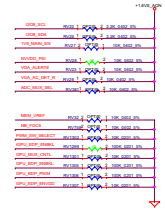


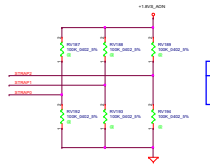


1:ENABLE 0:DISABLE
SCRD DISABLE
SCRD123 ENABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N18P	L	L	L	ENABLE

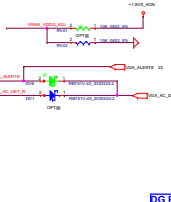


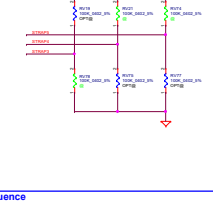




VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
4GB	Samsung 8Gb	K4E8032SBC-MC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H





VGA_DEVICE

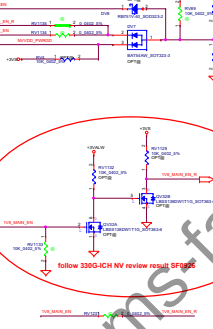
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

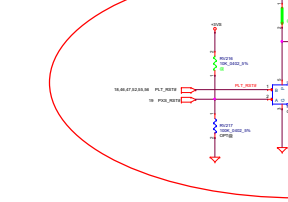
1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

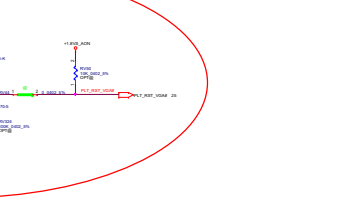
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

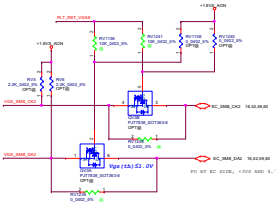
1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

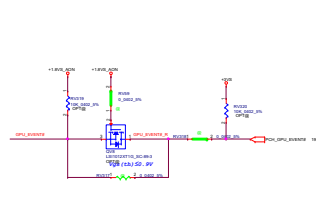
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE







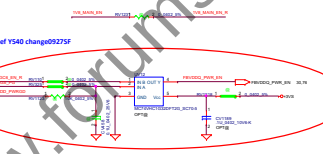




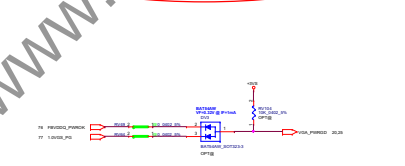
DG Power on/off sequence

For Optimus Power OFF
For GC6 Power OFF
For Power ON

follow 330G-ICH NV review result SF0836



For GC6 20180827 ref Y540 change0927SF



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5A Peak 8A

1.8V Total 1A (AON+MAIN)

0.5A

Cost down list:
1U 4Pcs

Partition A Under GPU(below 150mils)

Partition B Under GPU(below 150mils)

Under GPU(below 150mils)

Near GPU

under GPU

near GPU

CALIBRATION PIN	N18P
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	40.2Ohm

RV94 40.2ohm 60.4ohm

only for N18P

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

AG26,AJ28 NC pin,
only for under GPU 1.8VS_VGA layout trace

2A

V20B+

AON7408L
Vds=30V
Ids=15A
Rdson=28mohm@Vgs=4.66V
=20mohm@Vgs=6V
=18mohm@Vgs>10V
Vgs=+-20V
Vgsth=1~3V

Vg=16.4V@AC
Vg=7.38V@Battery

+1.8V_MAIN discharger circuit

Reserve PD3/PR4/PR5/CV38 for NV sequence requirement

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Title: N18P_(5/6):PWR

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BOTH GP107 AND N18P-G5 NEED
NC AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A9,B2,B23,D22,D28,D9,E4

UV1D
15/17 GND_1/2
N18P-FCBGA960_BGA960

UV1F
16/17 GND_2/2
Optional CND GNDs (2)
NC for 4-Lyr cards
N18P-FCBGA960_BGA960

UV1G
13/17 NVVDD
N18P-FCBGA960_BGA960

UV1E
9/17 XVDD
CONFIGURABLE POWER CHANNELS
N18P-FCBGA960_BGA960

NVVDD

UNDER GPU

NEAR GPU

trace width=16mils
differential voltage sensing.
differential signal routing.

VDD_SENSE L4 NVVDD_VDD_SENSE NVVDD_VDD_SENSE 79
GND_SENSE L5 NVVDD_VSS_SENSE NVVDD_VSS_SENSE 79

Add RV332 for NVVDDS discharge Hai Y520 SVT
Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725

+5VALW
RV60 47K_0402_5% OPT@
QV11 LBSS139WT1G_SC70-3 OPT@
28,77 1V0_MAIN_EN
QV29 AO3402_SOT-23-3
QV12 AO3402_SOT-23-3 OPT@
NVVDD
+1.0VGS

Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT

+5VALW
RV48 47K_0402_5%
RV61 470_0603_5%
QV6B 2N7002KDWH_SOT363-6
QV6A 2N7002KDWH_SOT363-6
28,76 FBVDDQ_PWR_EN
FBVDDQ

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Title: N18P_(6/6):PWR,VSS
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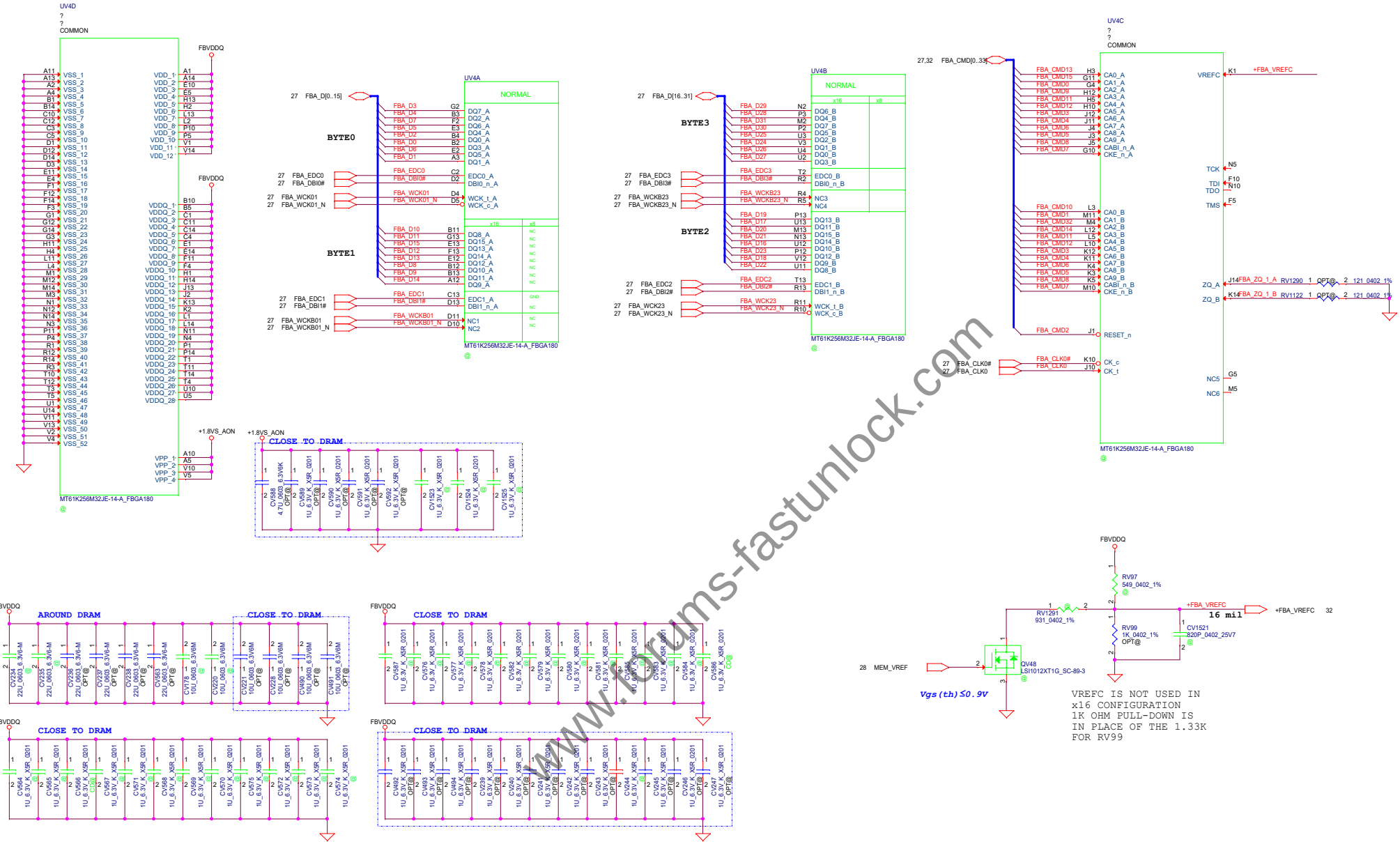

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_GDDR6_A_[31_0]		
Size C	Document Number Y550		Rev 1.0
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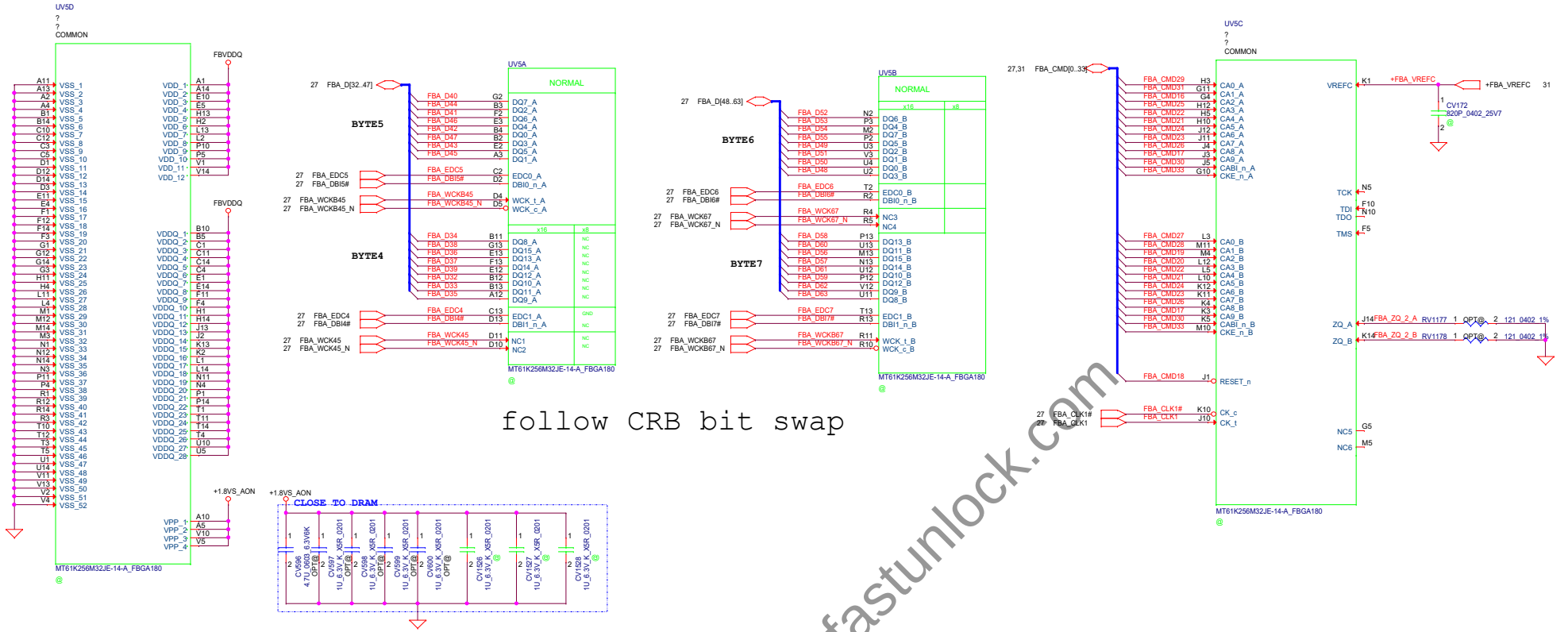

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_GDDR6_A_[63_32]		
Size C	Document Number Y550		Rev 1.0
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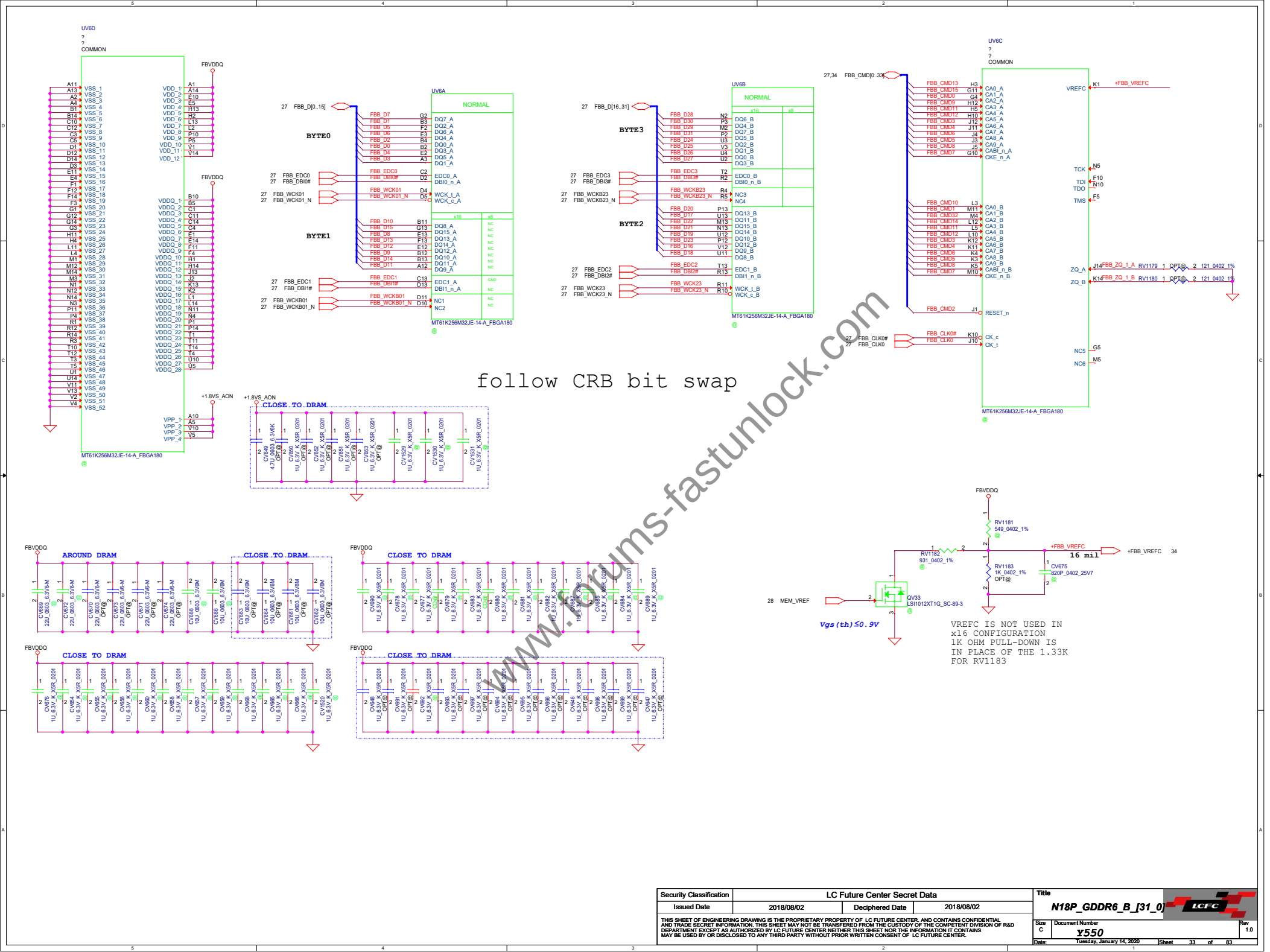

follow CRB bit swap

VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV1183

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_GDDR6_B_[31_0]		
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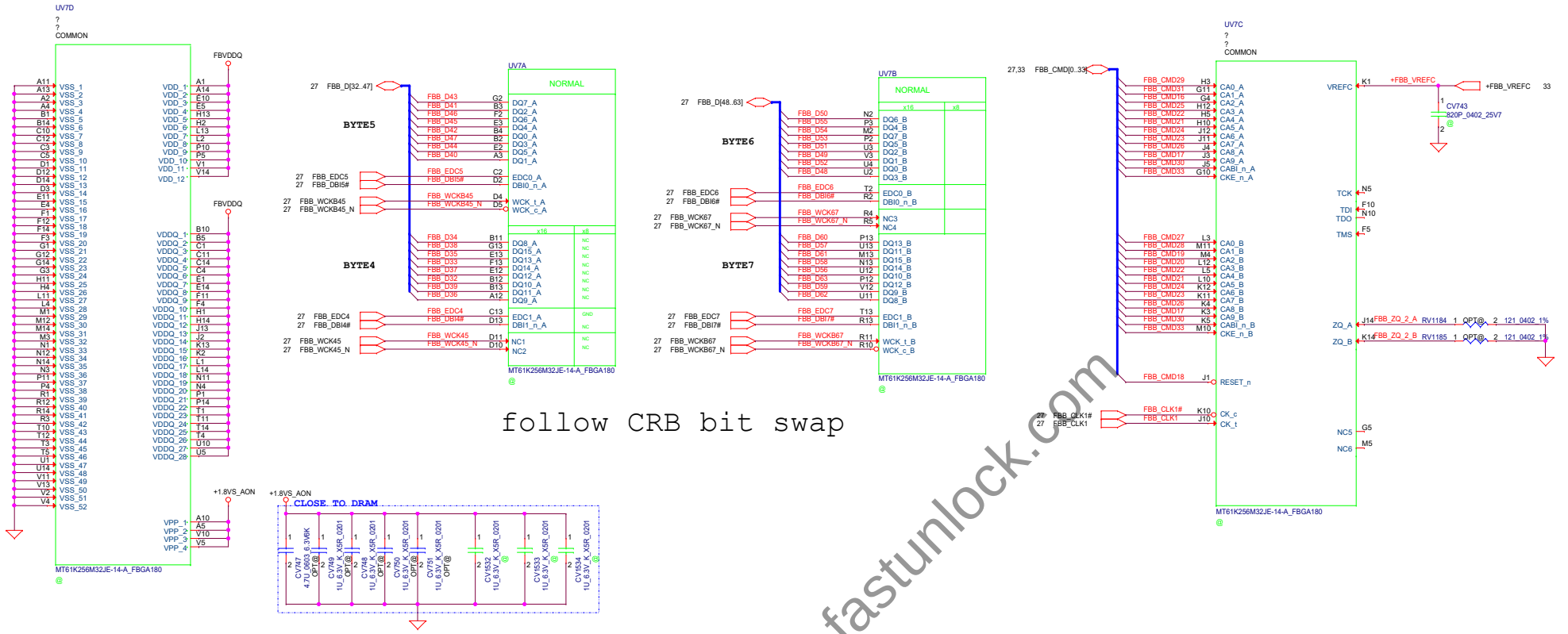

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18P_GDDR6_B_[63_32]		
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B	***Y550***	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Blank*

LCFC

Size	Document Number	Rev
B	¥550	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: ***Blank***

LCFC

Size	Document Number	Rev
B	***Y550***	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: ***Blank***

LCFC

Size	Document Number	Rev
B	***Y550***	1.0

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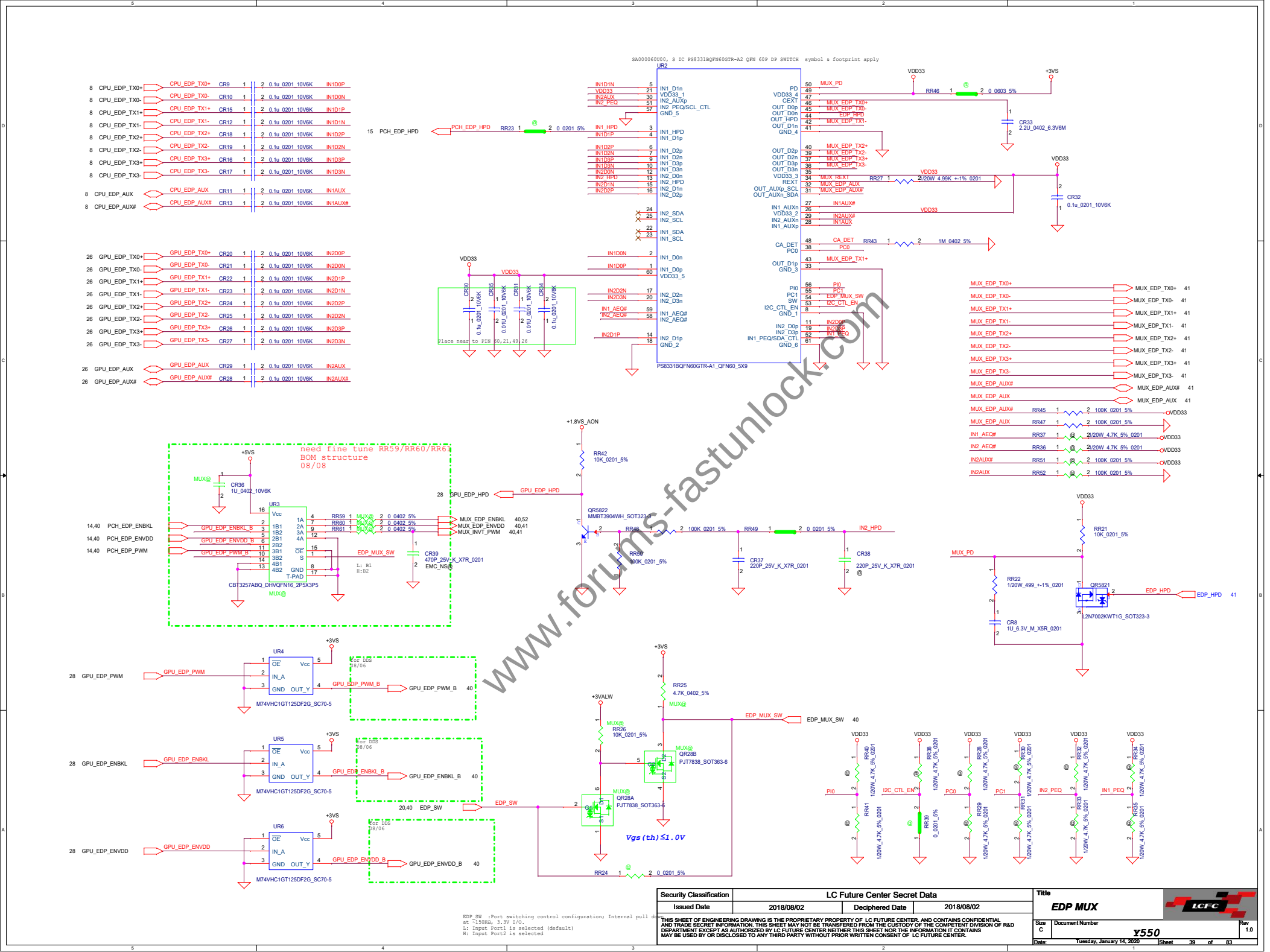
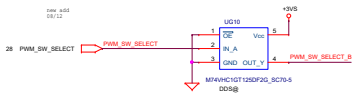
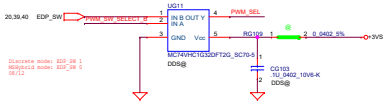
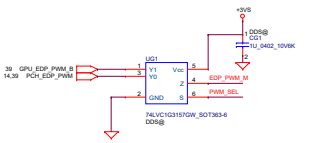


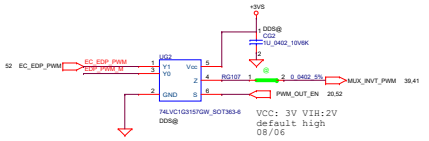
need fine tune RG107 RG108 RG88 BOM structure
08/08

EDP PWM LOGIC CONTROL

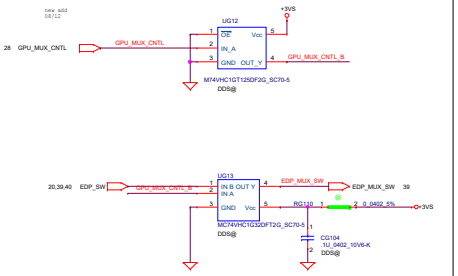




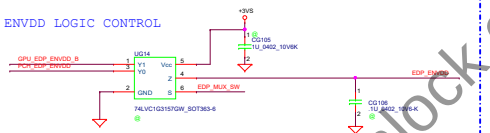




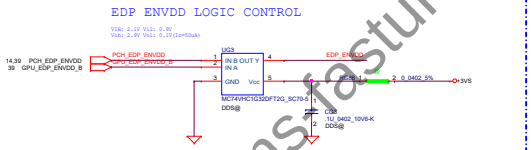
S	z
H	Y1
L	Y0

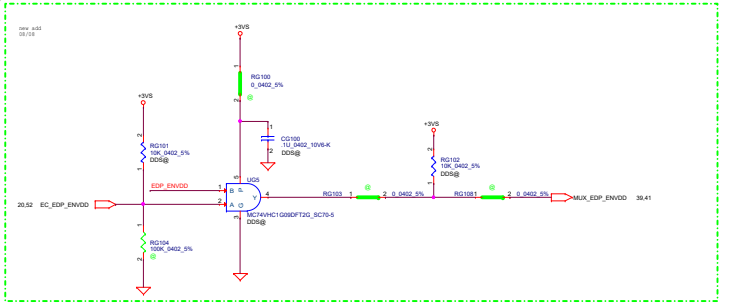


Co-lay EDP ENVDD LOGIC CONTROL

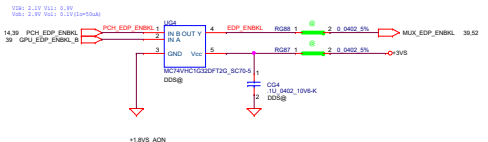


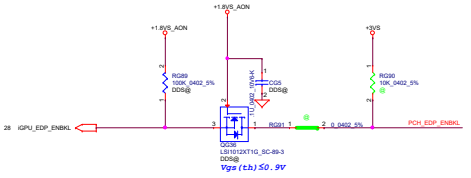
EDP ENVDD LOGIC CONTROL



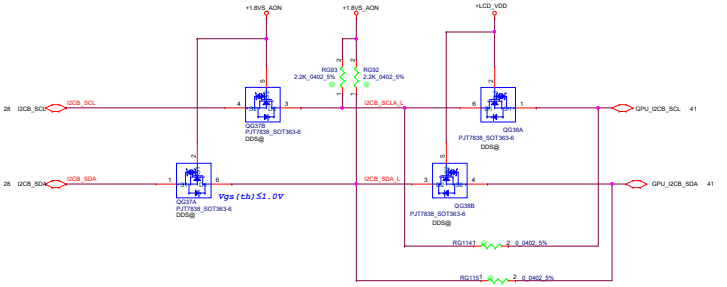


EDP backlight LOGIC CONTROL





level shift for I2C



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
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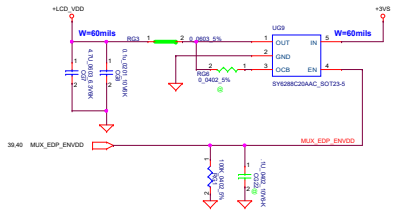
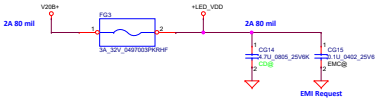
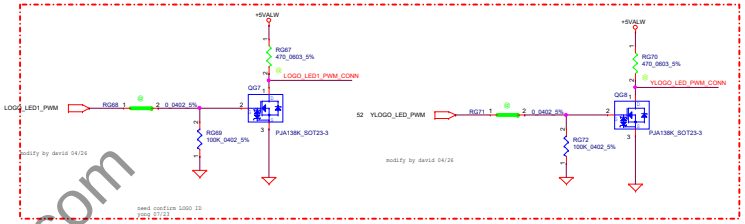
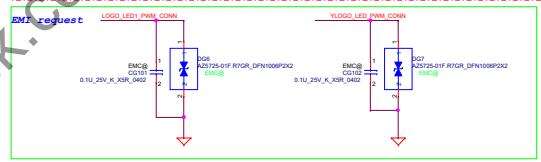
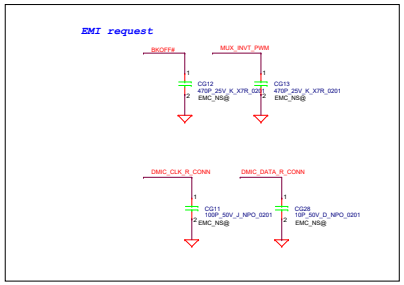
LCD POWER CIRCUIT

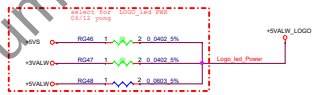


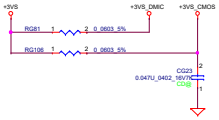


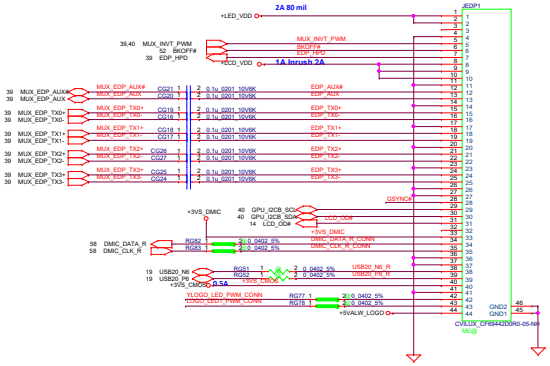


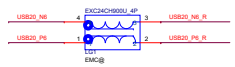


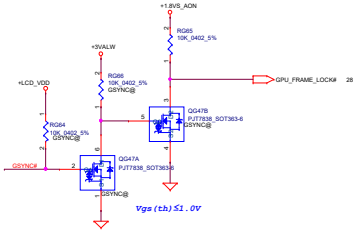












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	eDP/ CMOS/Touch screen
Size	D
Document Number	¥550
Rev	1.0
Date	Friday, February 14, 2020
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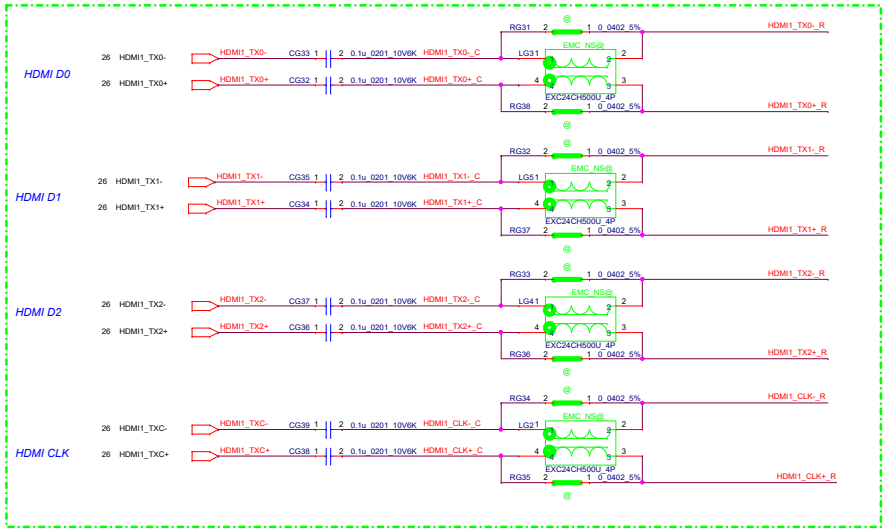
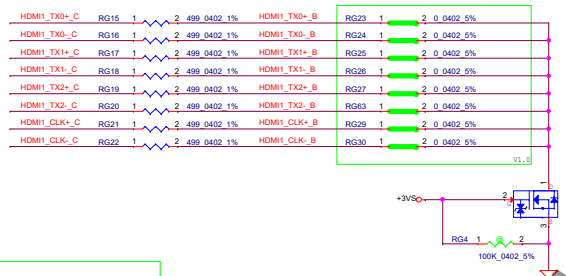
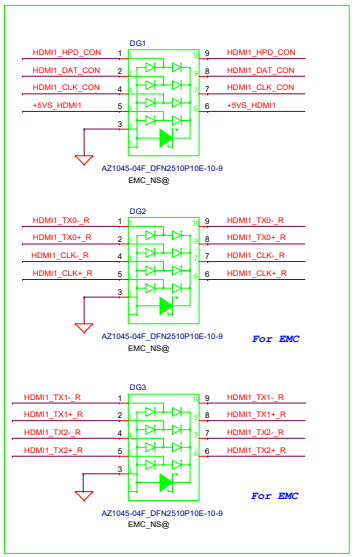
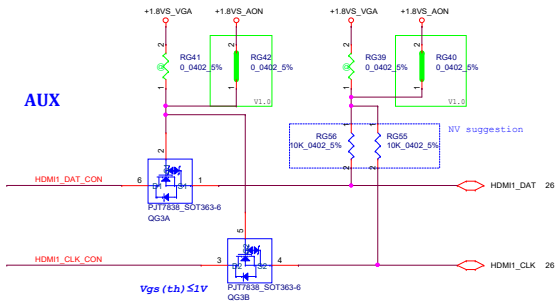
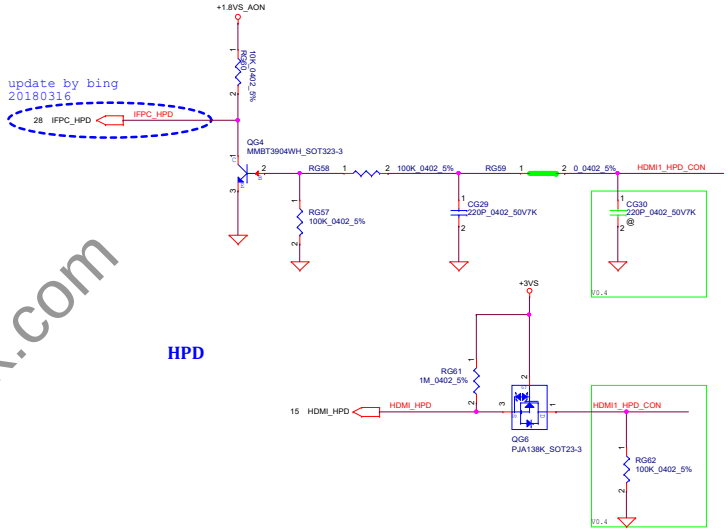
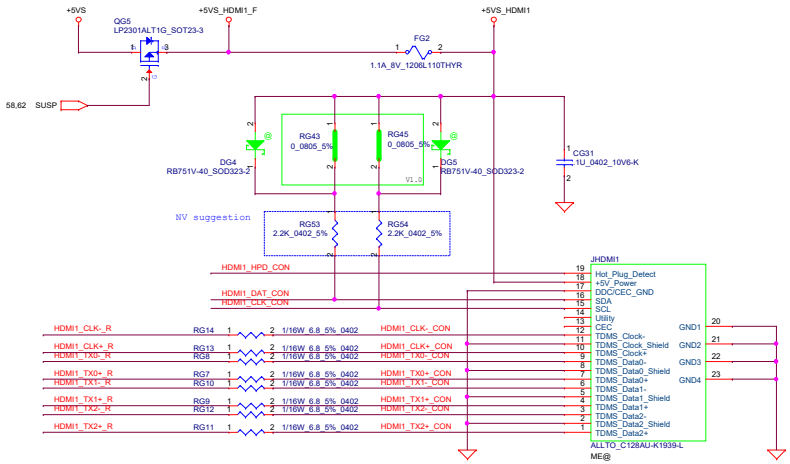












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	HDMI_CONN		
Size	Document Number		Rev
Custom	Y550		1.0
Date:	Friday, January 17, 2020	Sheet	42 of 83

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

VMON:
Used to monitor VBUS voltage.
Divide the VBUS voltage down to ADC full-scale input of 1.2V.
Then connect the divided voltage to this pin.

RA=RT42

RB=RT47

EC

2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV

VDS=-20
VGS=+-8V
Id=3A
Vth=-1v

RTS5457T-GR

RT60 for dead battery
Stuff: disable
unStuff: Enable

Modify by Yong808/21

follow stone request 08/21

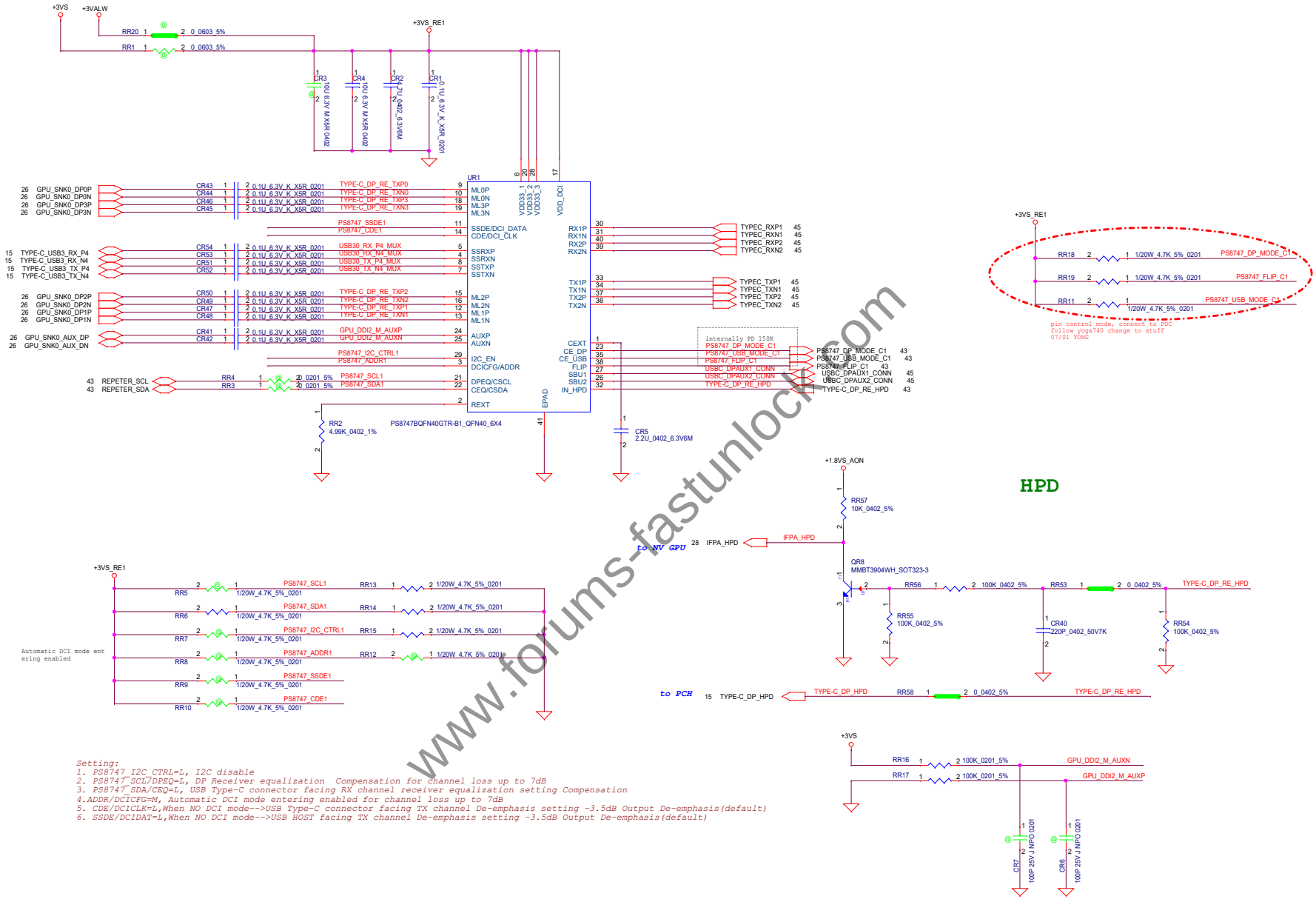
for redriver pin control mode used 06/13 yong

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: USB TYPE-C Controller

Size: Custom | Document Number: Y550 | Rev: 1.0

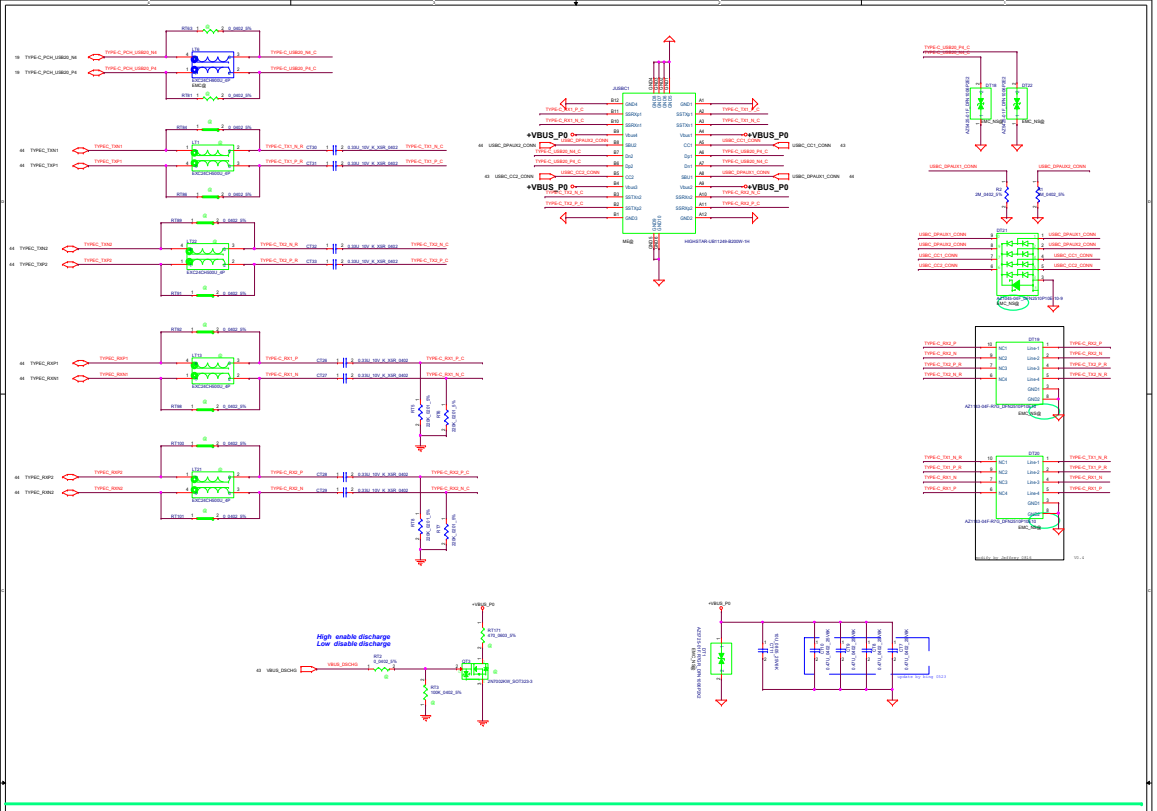
Date: Monday, January 20, 2020 | Sheet 43 of 83

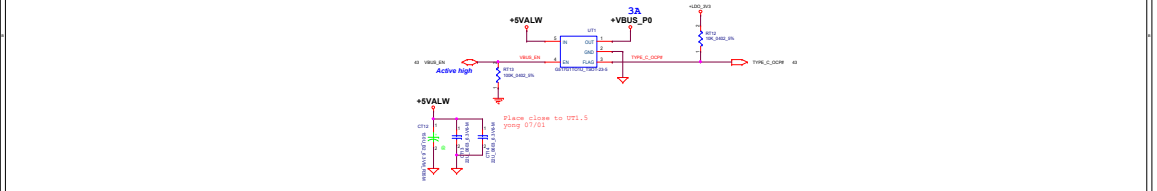


Setting:
1. PS8747_I2C_CTRL=L, I2C disable
2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
4.ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
5. CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
6. SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDI Redriver PS8330		
Size C	Document Number Y550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 44 of 83		





Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/08/02	Deciphered Date	2015/08/02
			USB TYPE-C Port

Document Number	Rev
¥550	1.0

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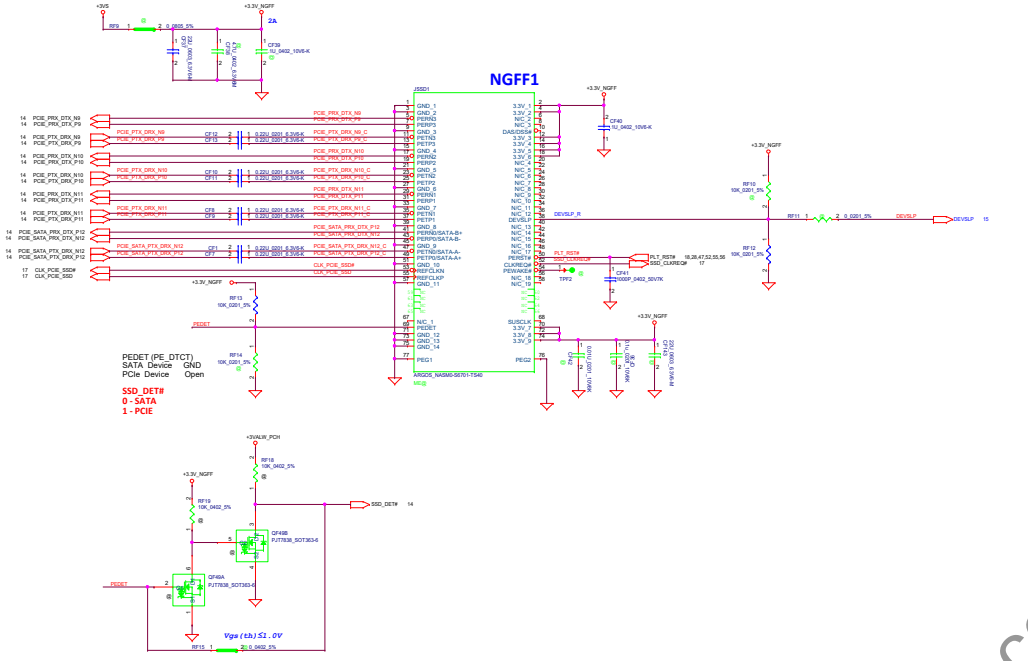
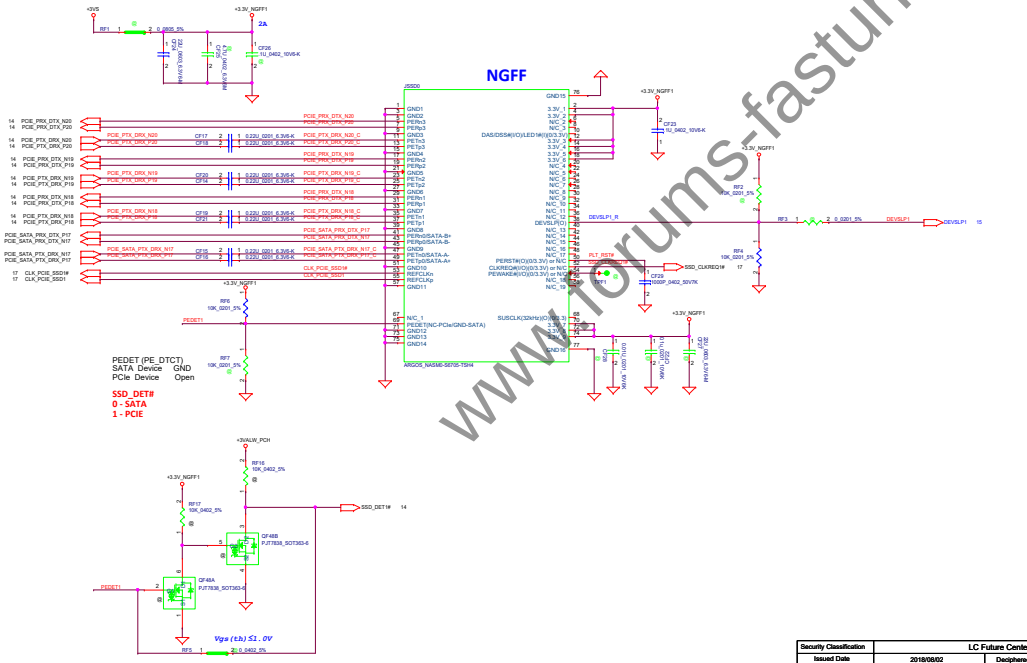
M.2 SSD(SATA/PCIE)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data	Title	NGFF WLAN
Issued Date	2018/08/02	Deciphered Date	2018/08/02
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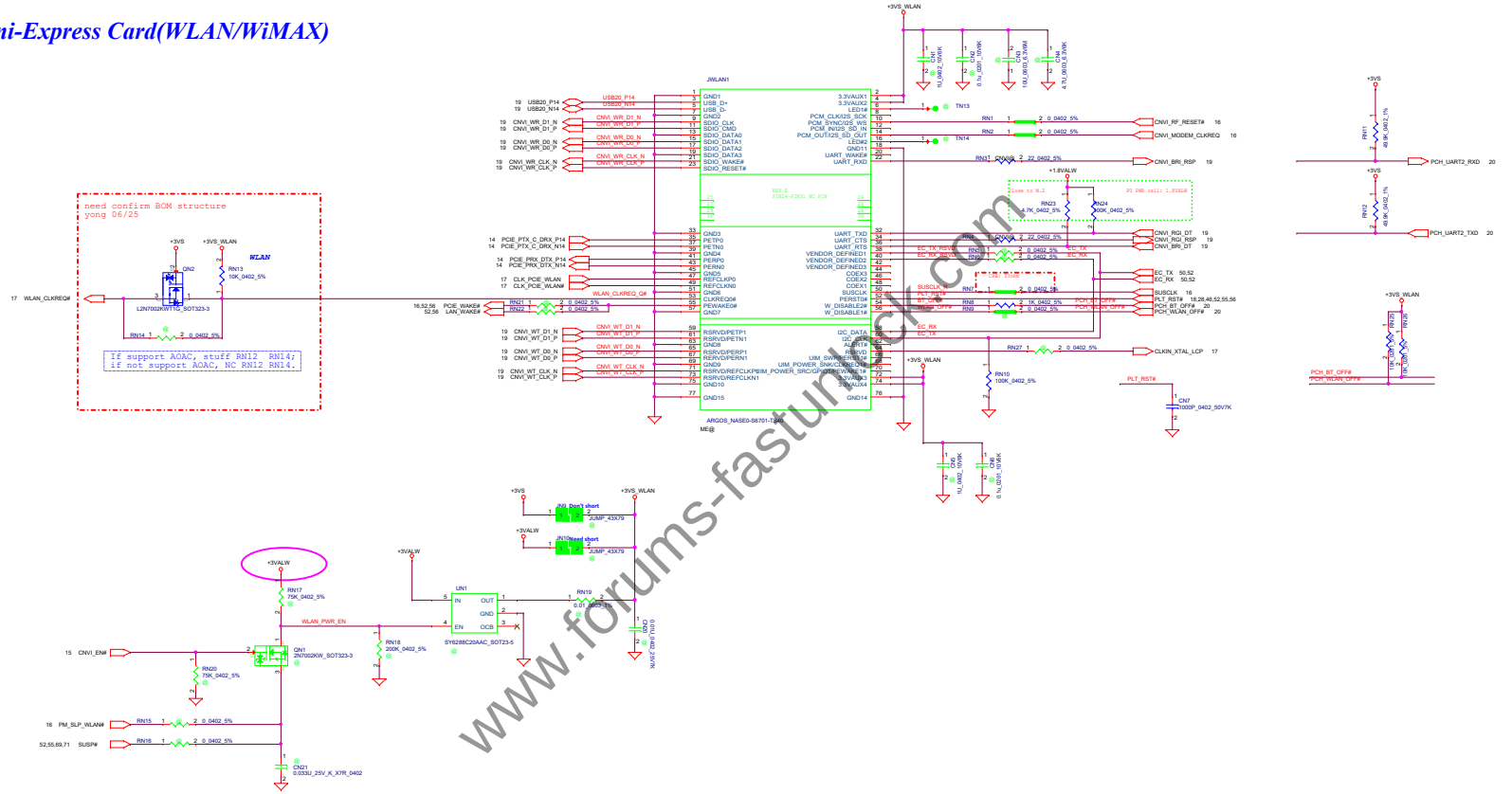
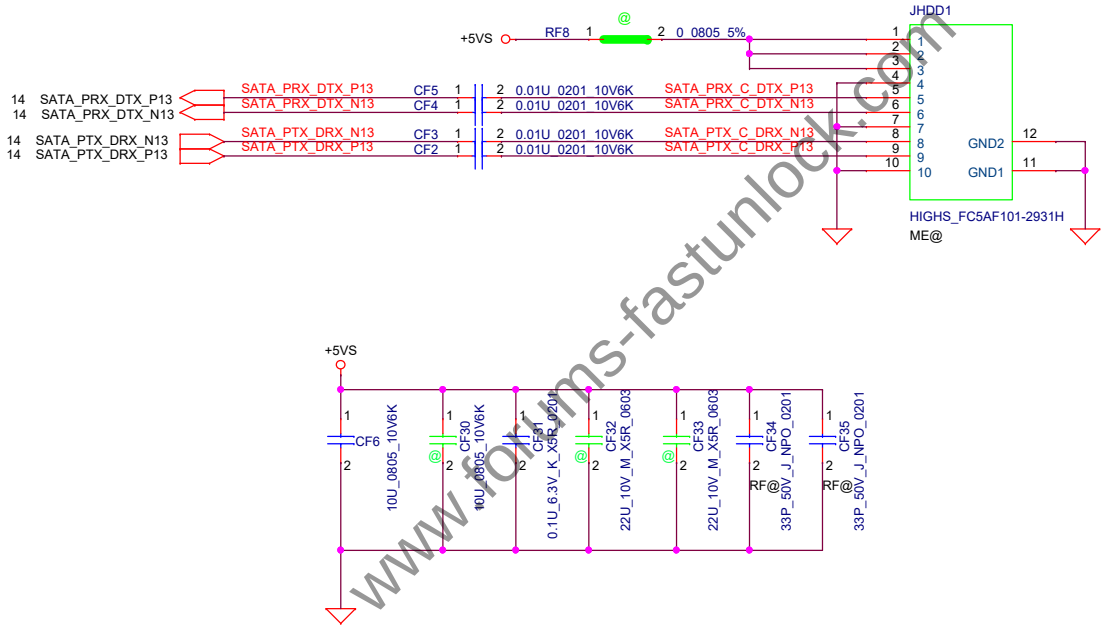
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

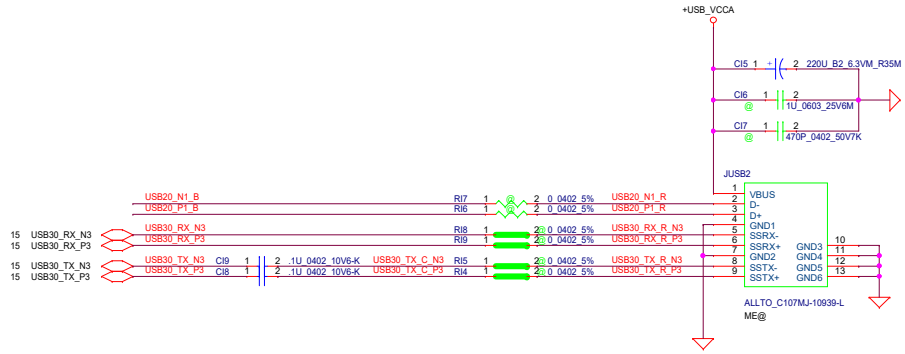
Title	CNVI		
Size D	Document Number ¥550		Rev 1.0
Date: Tuesday, January 14, 2020	Sheet 47 of 83		

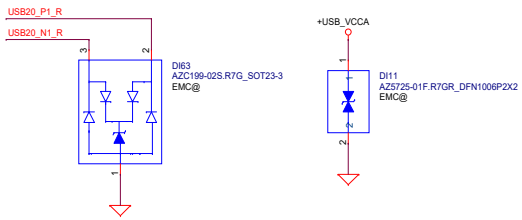
SATA HDD Conn.

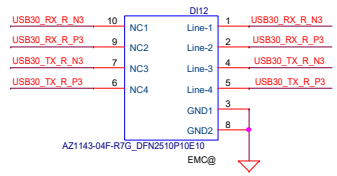


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

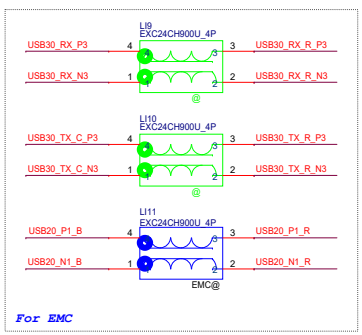
Title	HDD/XBOX CONN		
Size B	Document Number Y550		Rev 1.0
Date:	Wednesday, January 15, 2020	Sheet 48 of 83	





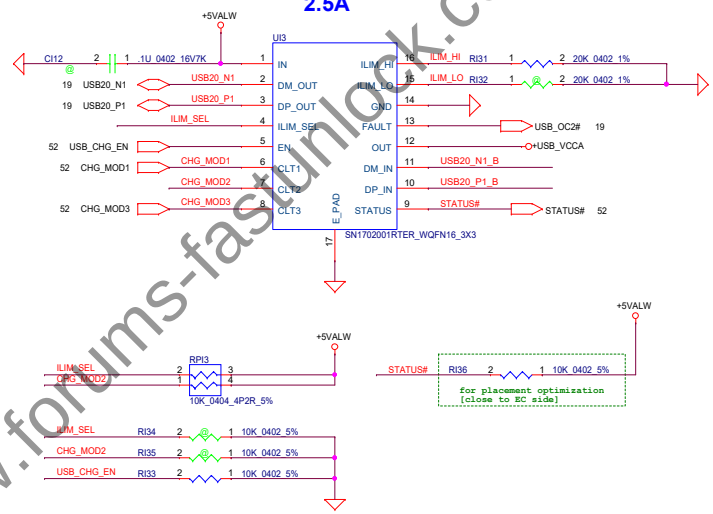


For EMC



For EMC

USB charger
2.5A



CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0/USB3.0 PORT (LEFT)**

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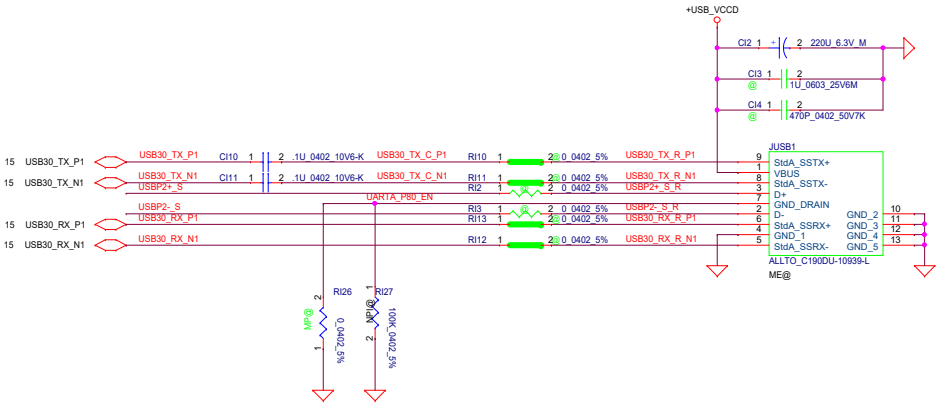
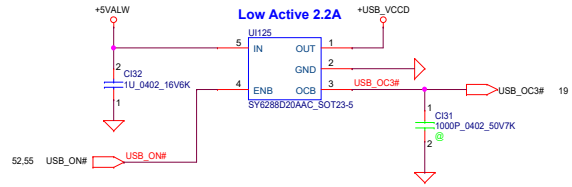
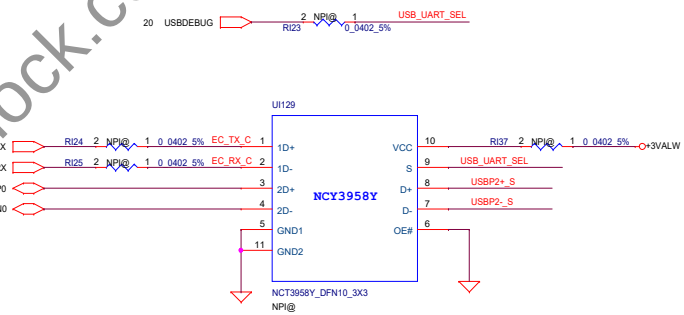
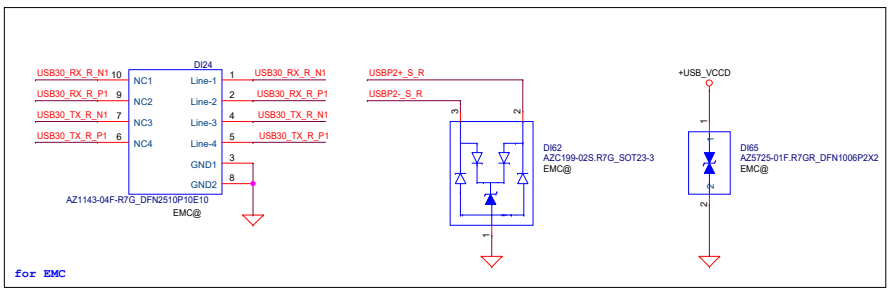


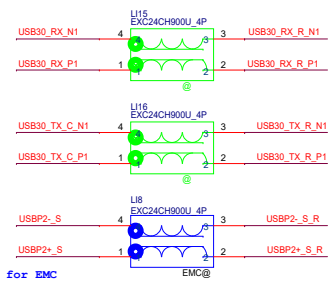
USB3.1 PORT x2

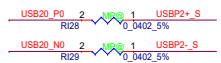


For USB Debug Function





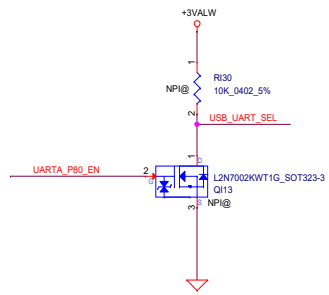




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0**

Size	Document Number	Rev
C	Y550	1.0

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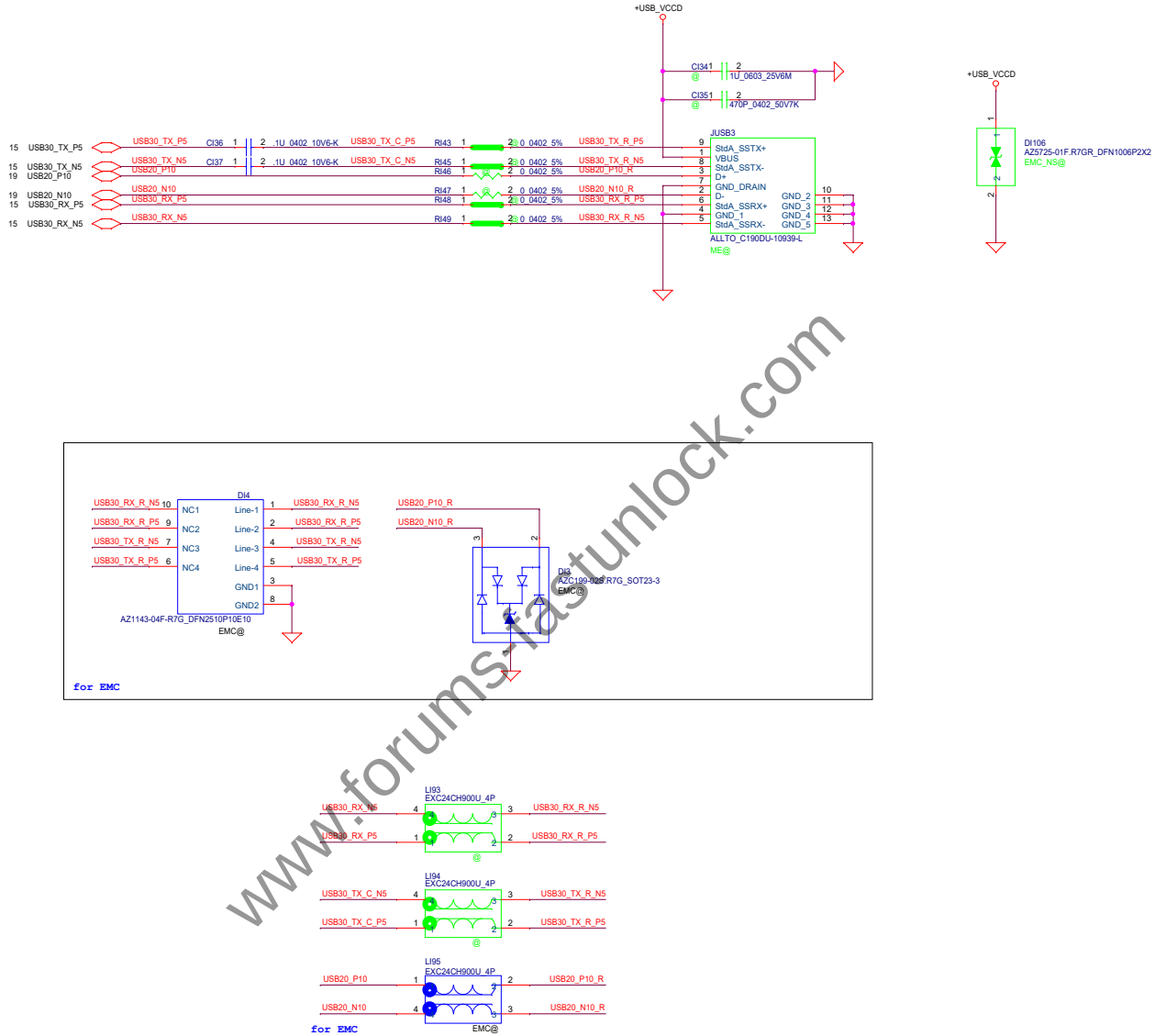

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	USB2.0		
Size C	Document Number Y550		Rev 1.0
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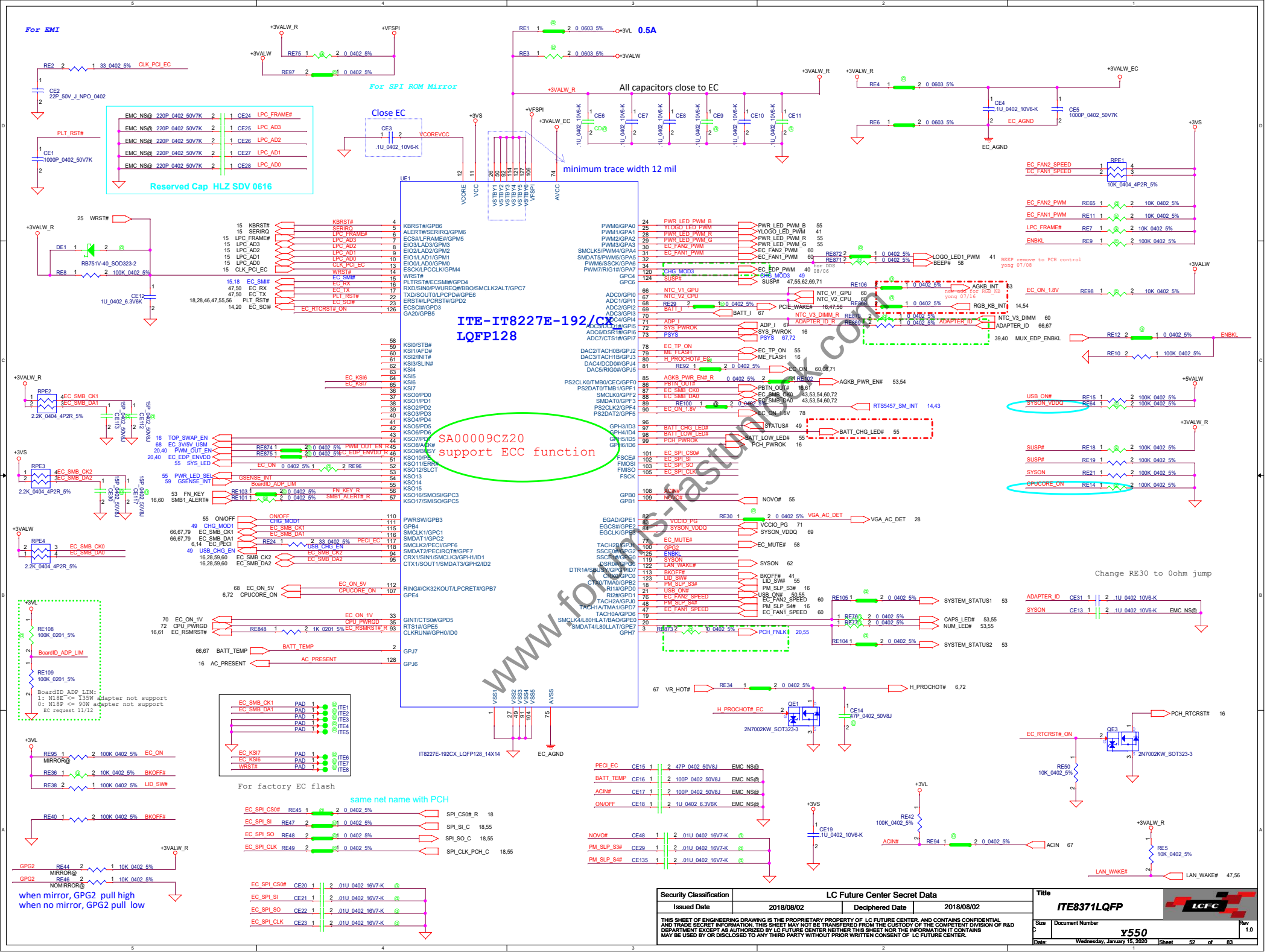

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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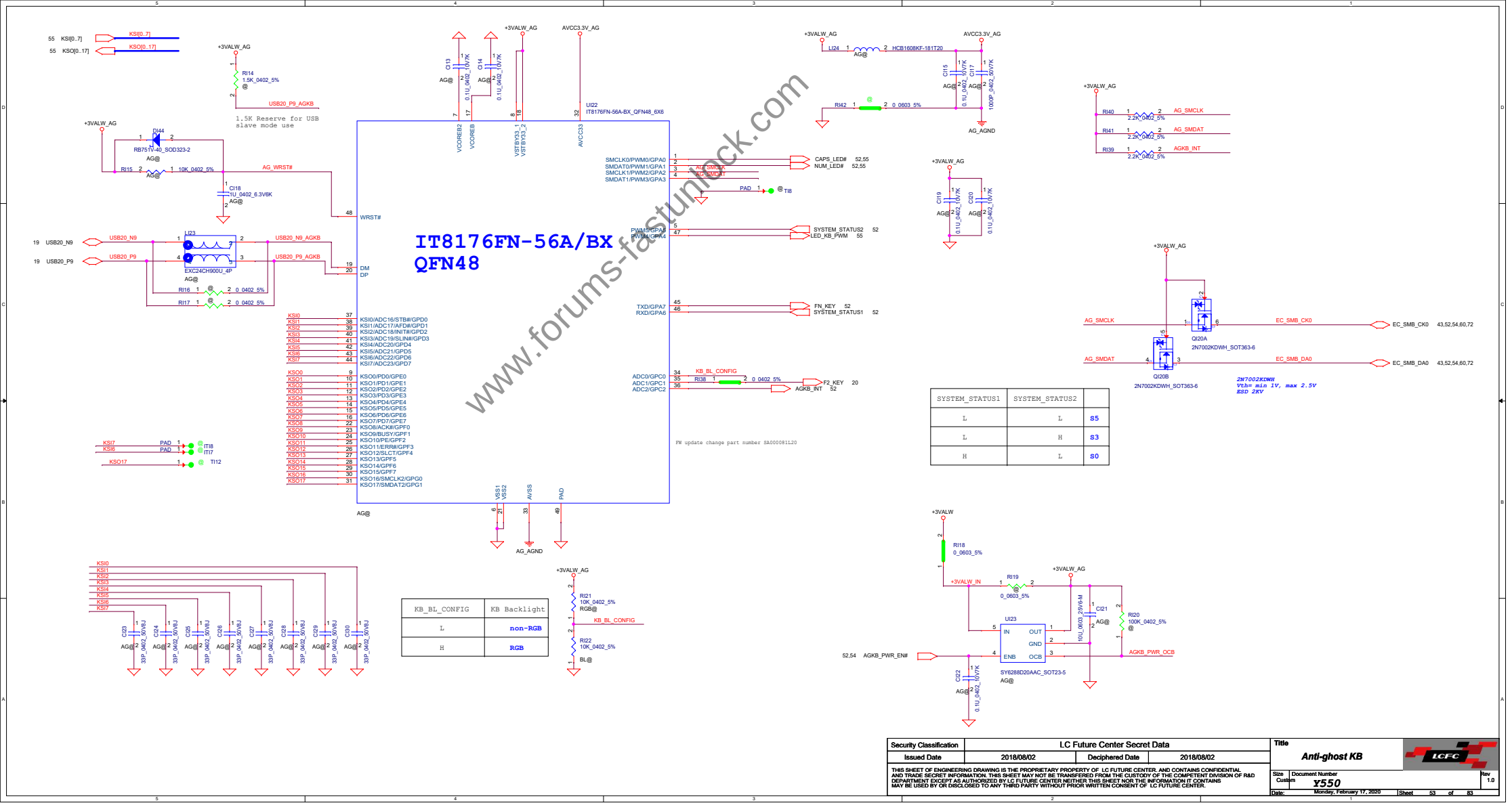
Title	ITE8371LQFP		
Size	Document Number		Rev
C	Y550		1.0
Date:	Wednesday, January 15, 2020	Sheet	52 of 83

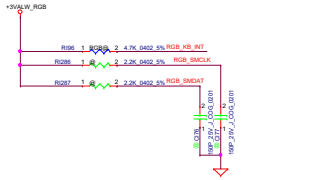


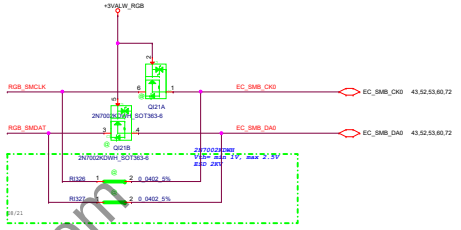
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

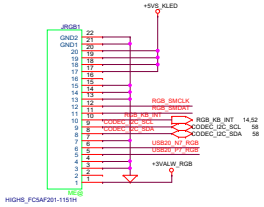
Title: Anti-ghost KB

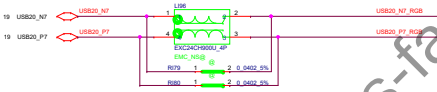
Size	Document Number	Rev
Custom	Y550	1.0

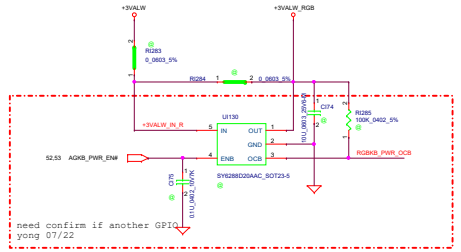
Date: Monday, February 17, 2020 Sheet 53 of 83











Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	RGB KB		
Size D	Document Number		Rev 1.0
	Y550		
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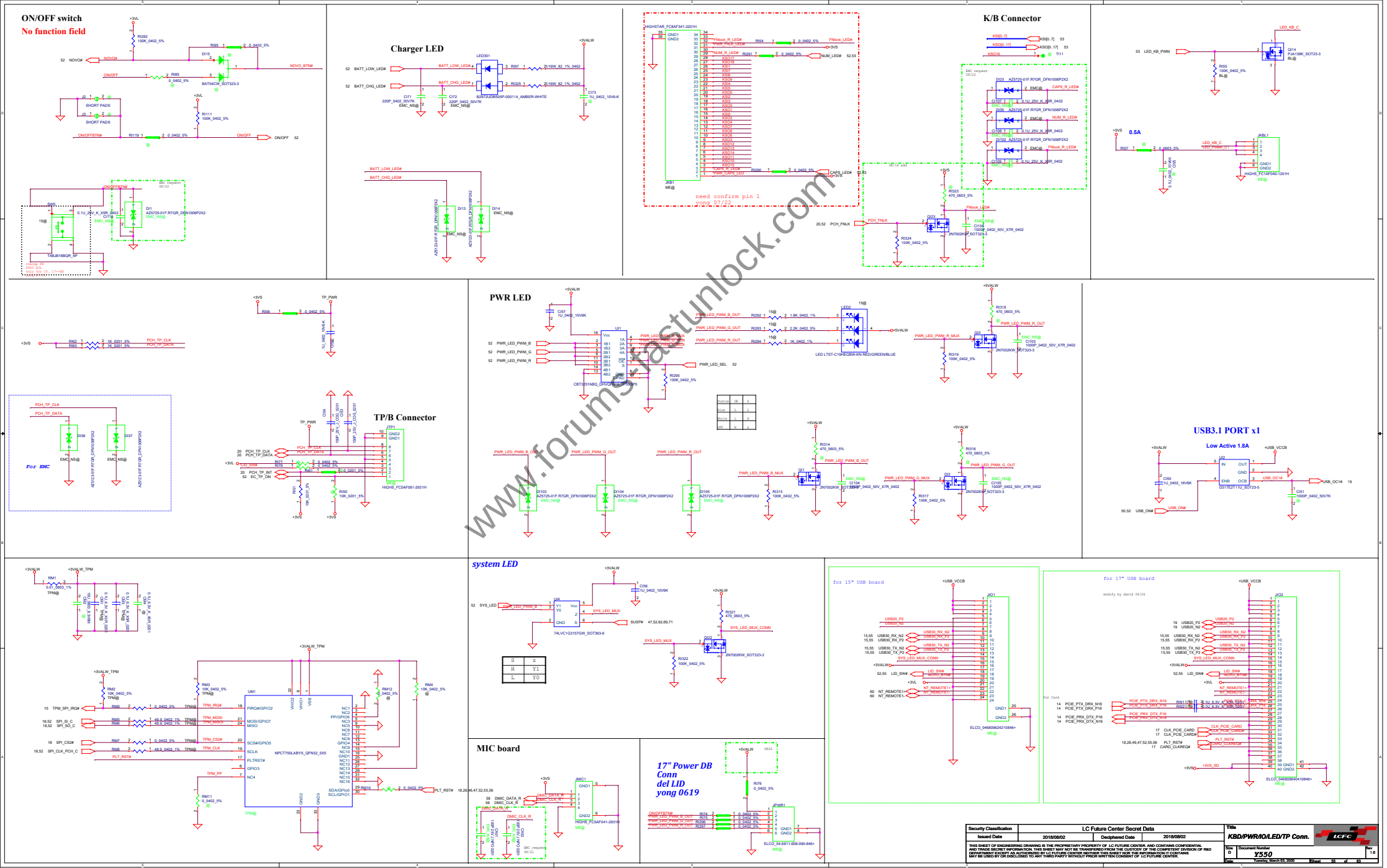
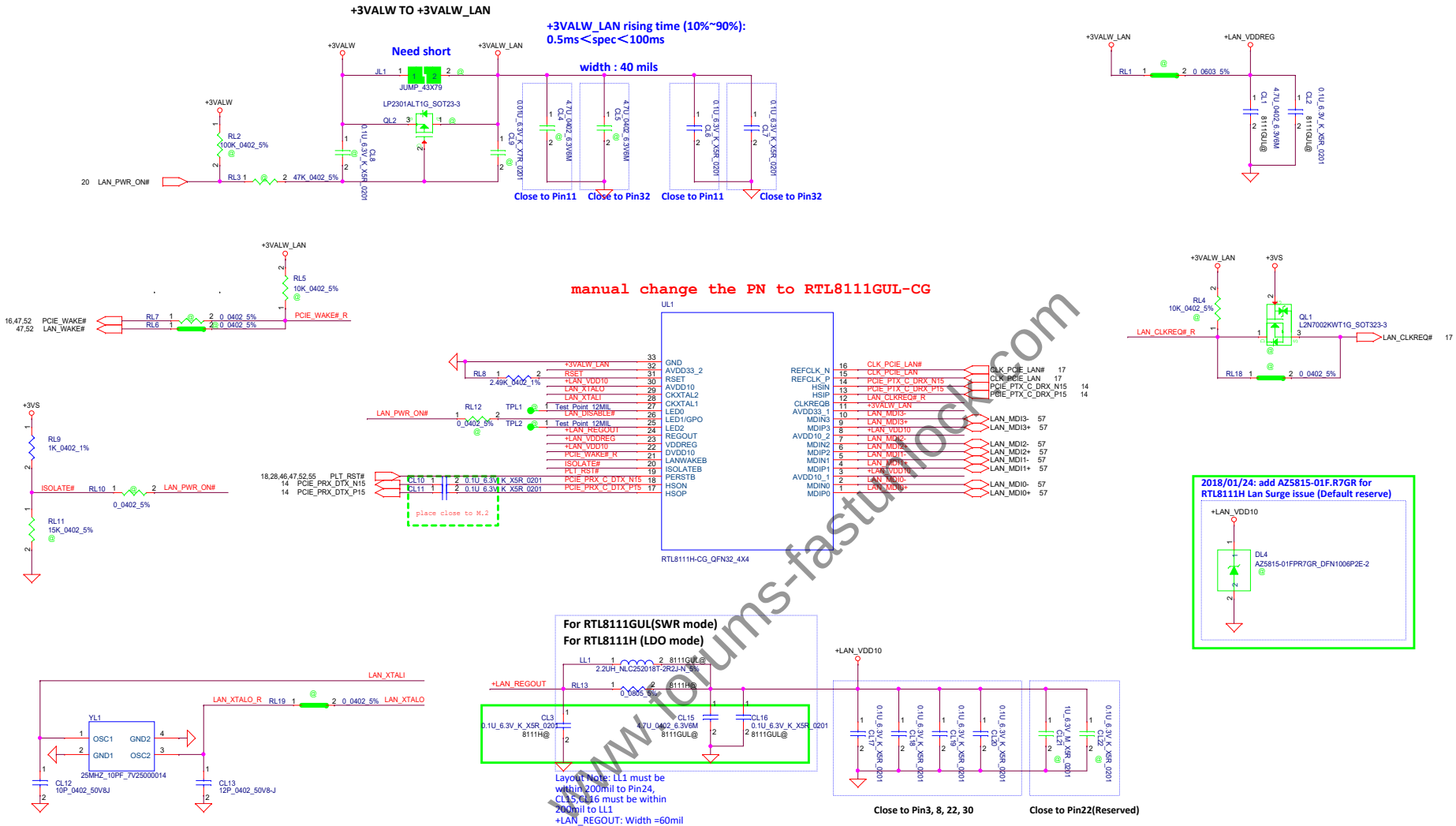

ON/OFF switch
No function field
Charger LED
K/B Connector
PWR LED
TP/B Connector
USB3.1 PORT x1
Low Active 1.8A
system LED
MIC board
17" Power DB Conn del LID yong 0619
for 15" USB board
for 17" USB board
need confirm pin 1 yong 07/22
www.forums-fractunlock.com
LC Future Center Secret Data
KBD/PWR/IO/LED/TP Conn.
¥550



Security Classification	LC Future Center Secret Data		
Issued Date	2019/02/13	Deciphered Date	2019/02/13

Title	LAN_RTL8111GUL_H		
Size	Document Number		Rev
C	Y550		1.0
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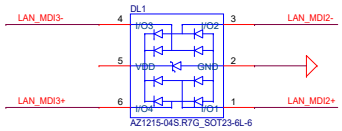
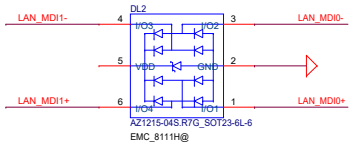
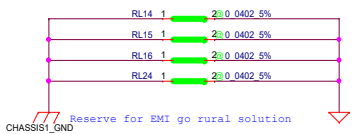
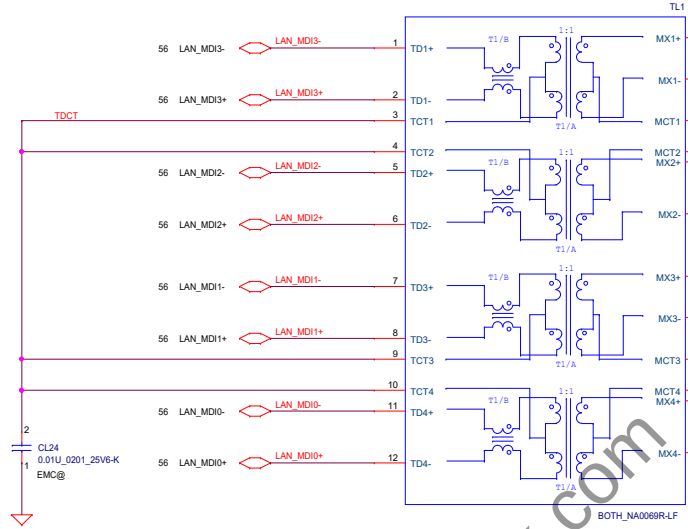
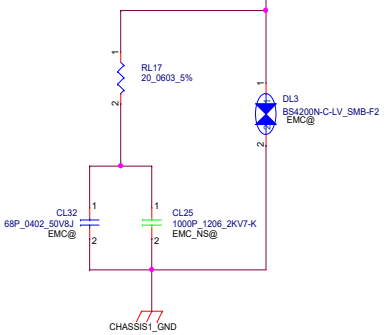
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

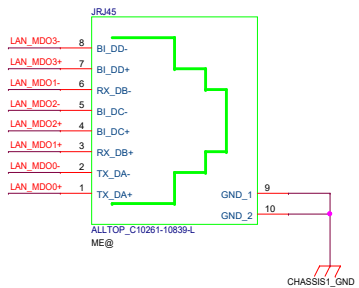












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	LAN_Transformer		
Size	Document Number		Rev
C	Y550		1.0
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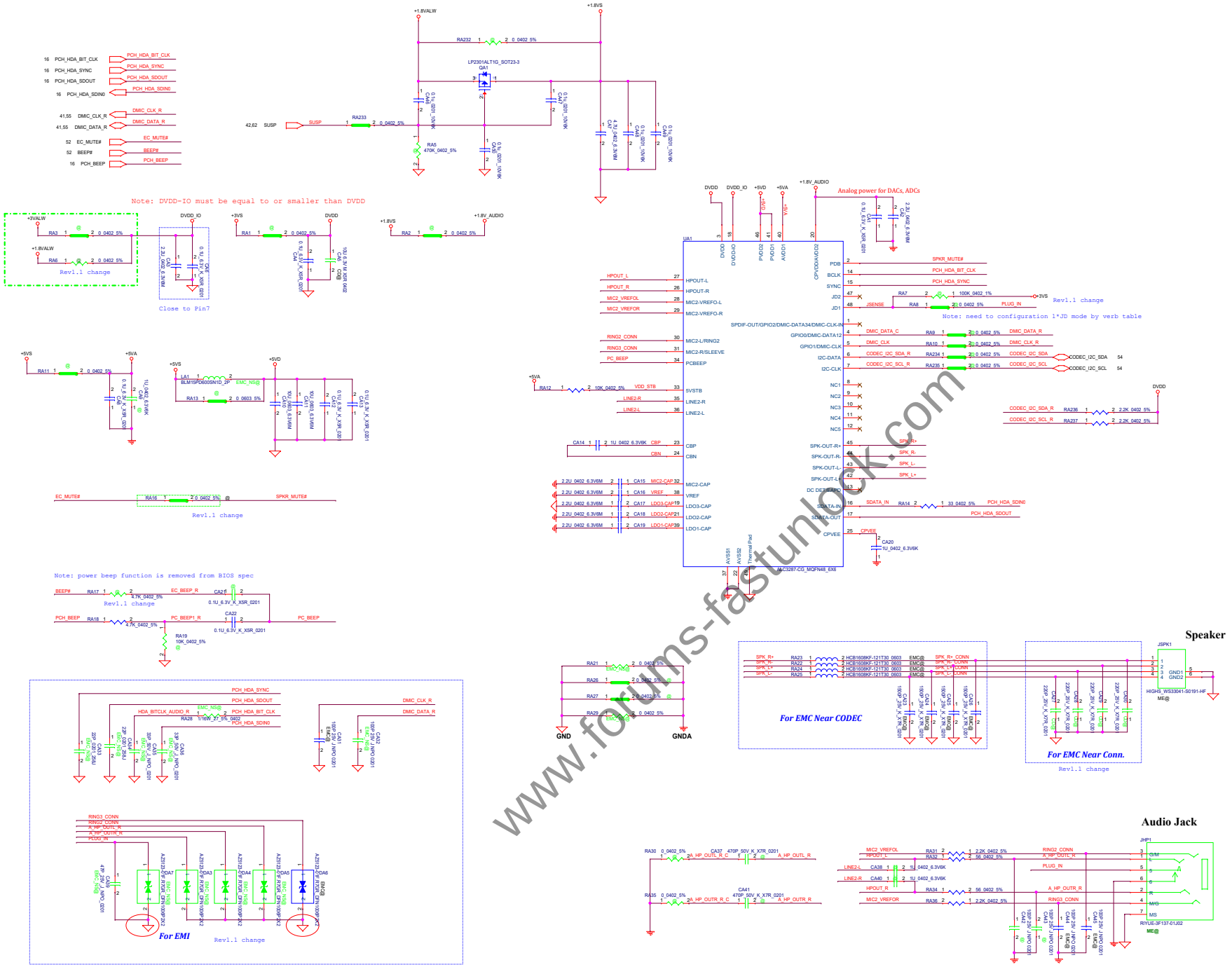

Security Classification	LC Future Center Secret Data		
Issued Date	2018/03/15	Deciphered Date	2019/03/14

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Title: **Codec ALC3287**

Size: Custom | Document Number: Y550 | Rev: 1.0

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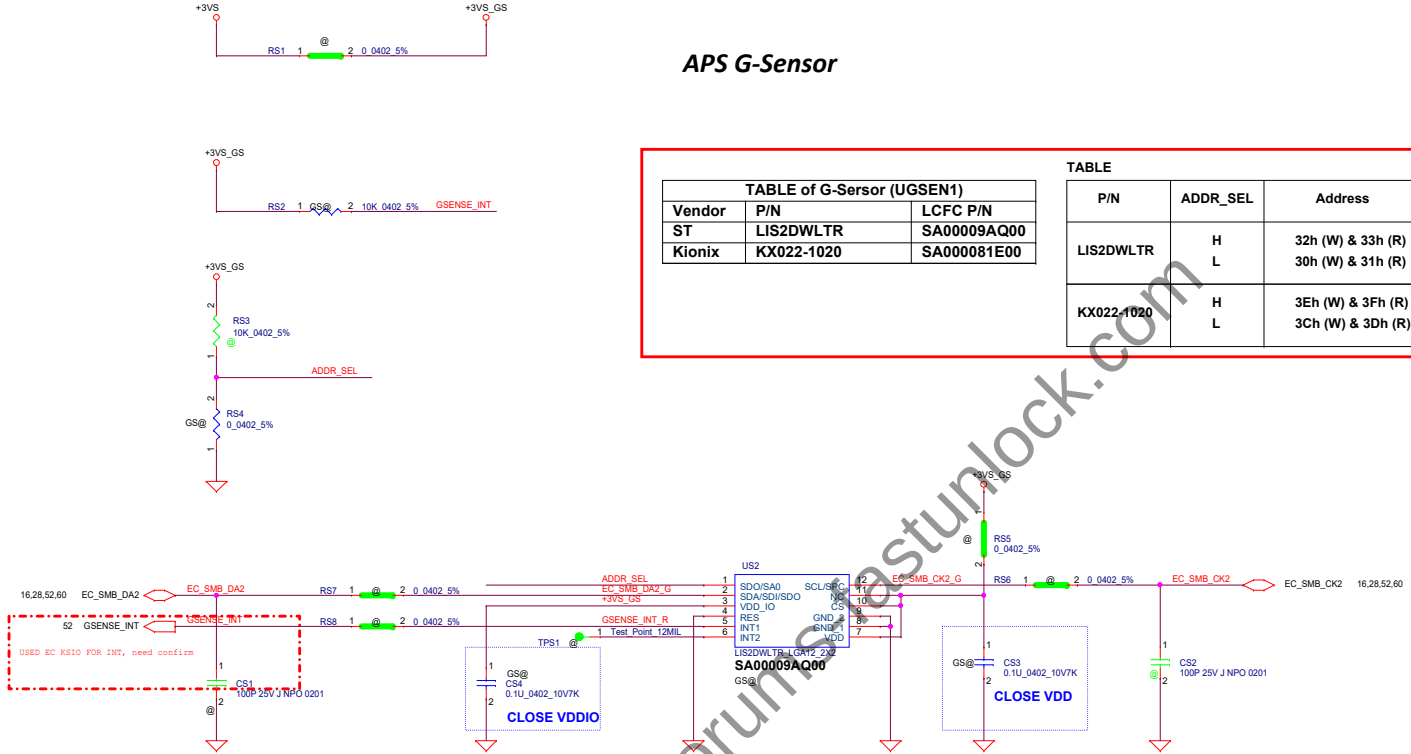
APS G-Sensor

TABLE of G-Sersor (UGSEN1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)



Security Classification	LC Future Center Secret Data		
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Title: USB2.0

Size	Document Number	Rev
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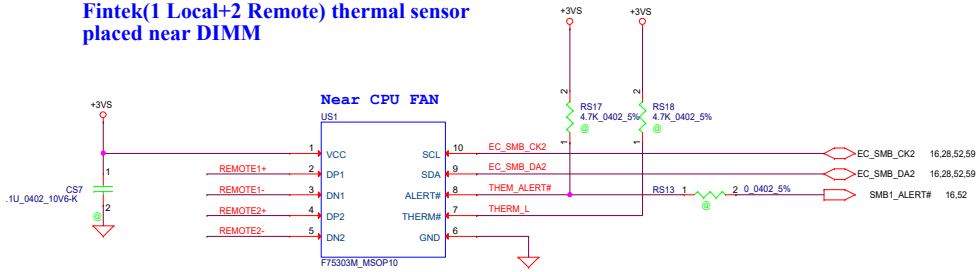
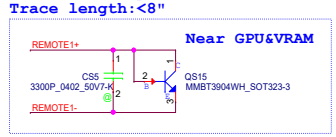
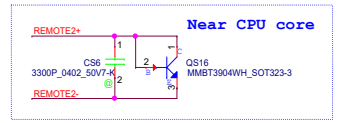
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM

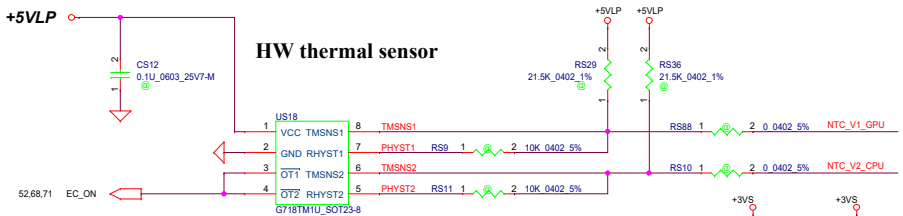


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

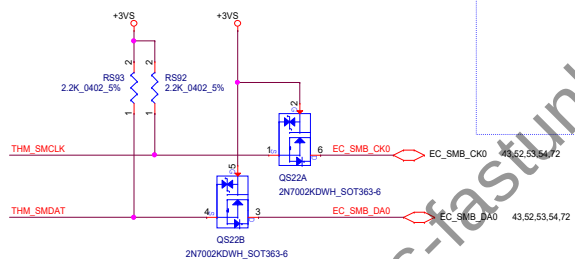


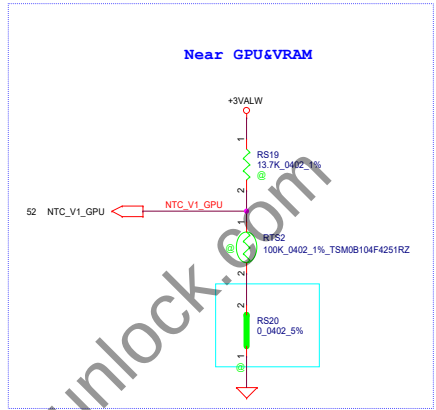


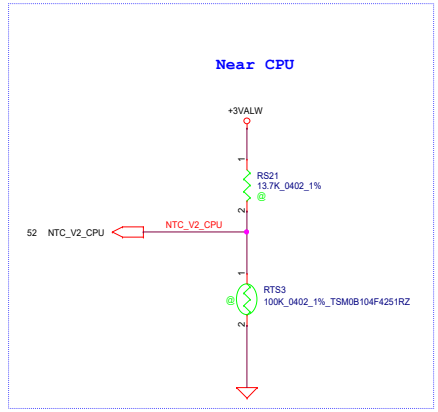
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

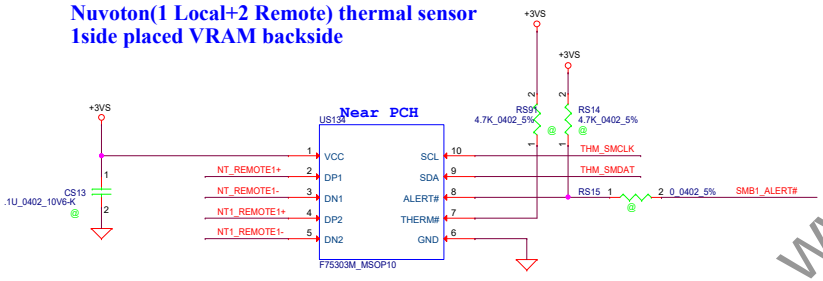


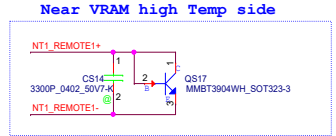


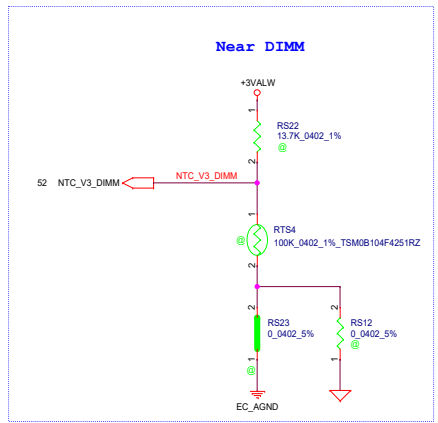


for layout optimized, change the EC_AGND to GND

Nuvoton(1 Local+2 Remote) thermal sensor 1side placed VRAM backside



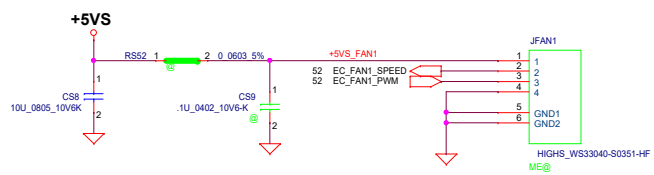




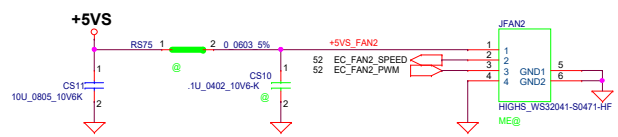
Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

FAN Conn Right



FAN Conn LEFT



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Thermal sensor/FAN CONN		
Size C	Document Number Y550		Rev 1.0
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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

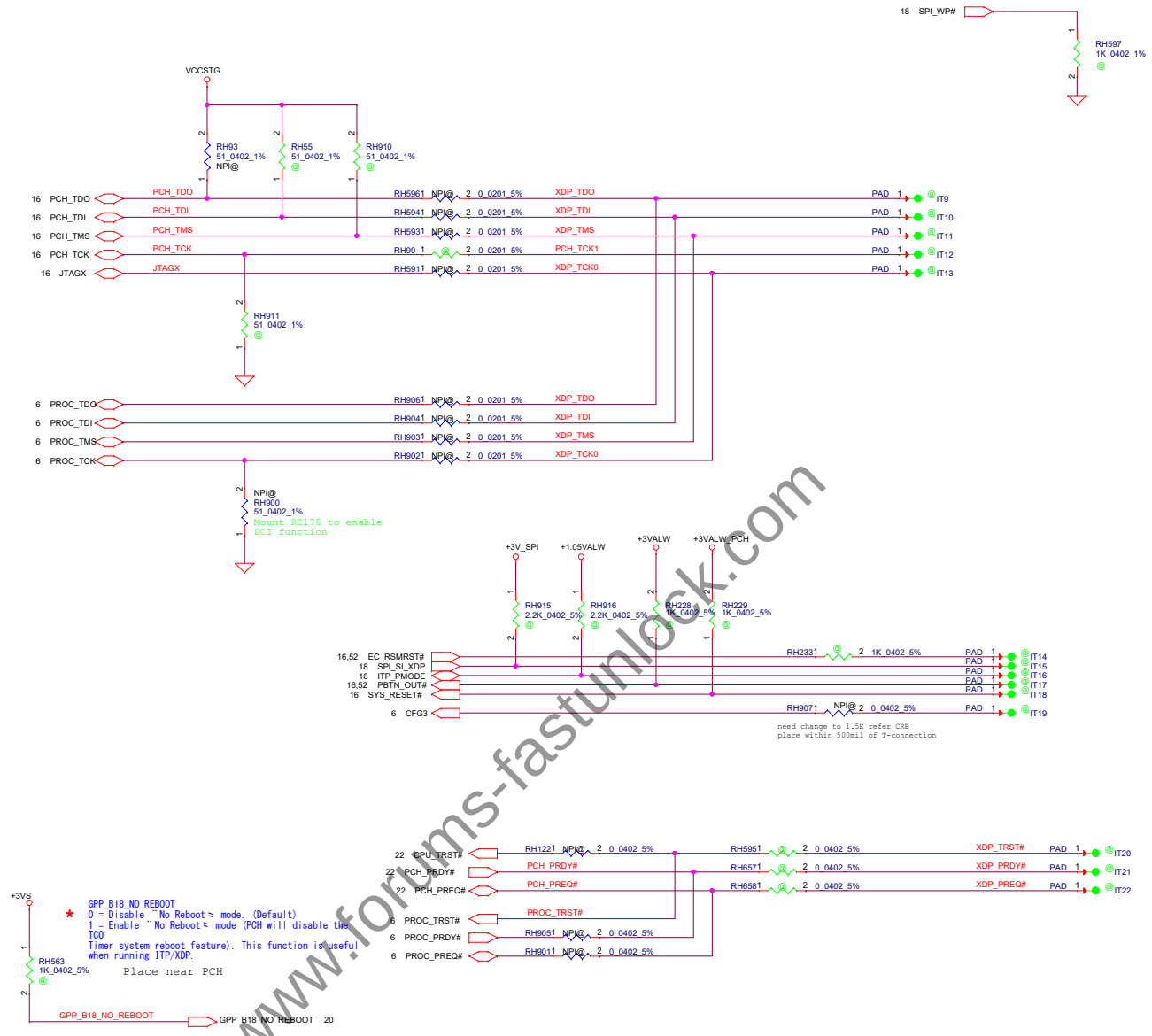
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	XDP		
Size	Document Number		Rev
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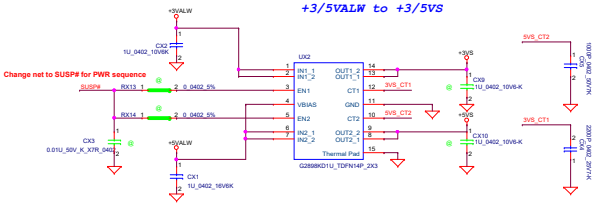
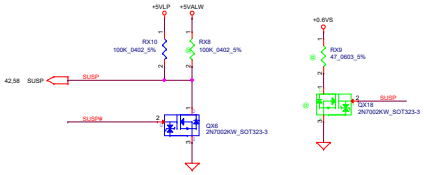
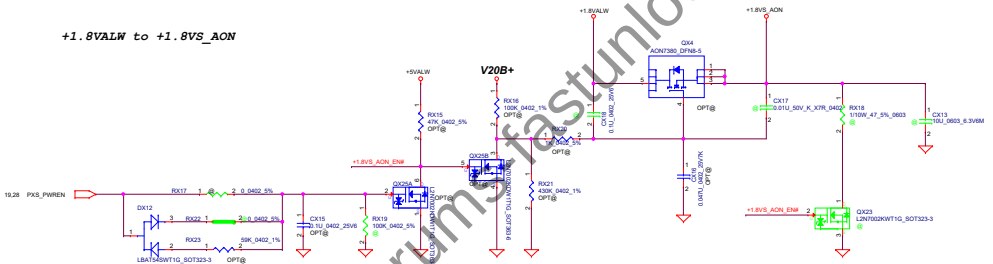
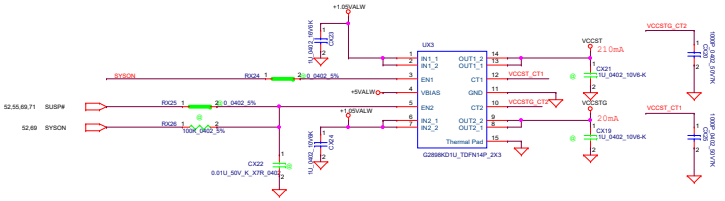
+3/5VALW to +3/5VS





+1.8VALW to +1.8VS_AON





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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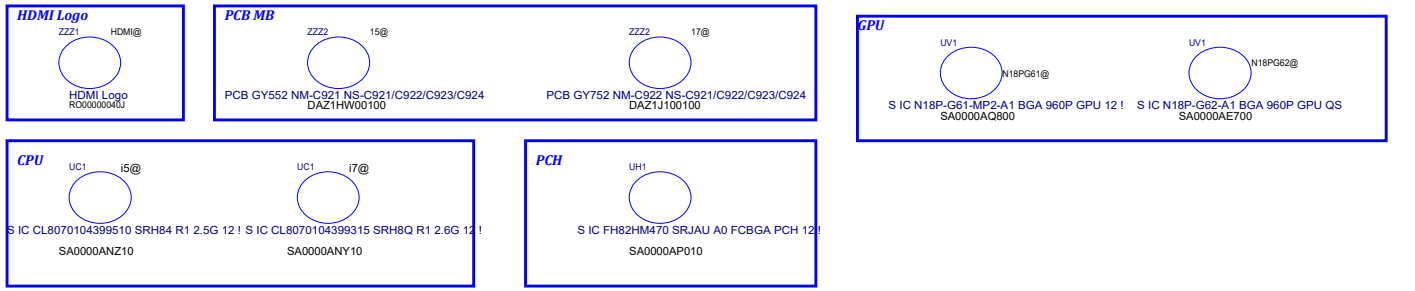
Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
D	¥550		1.0
Date:	Tuesday, January 14, 2020	Sheet	62 of 83

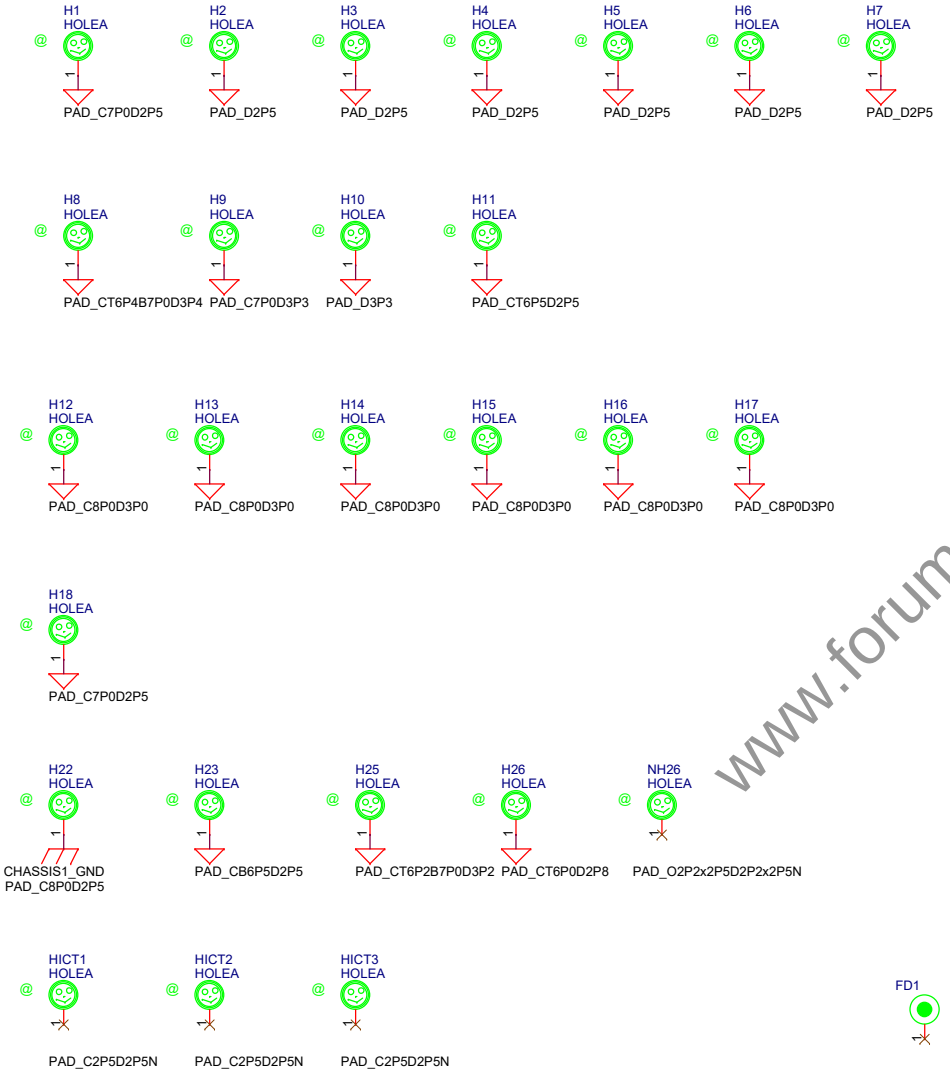


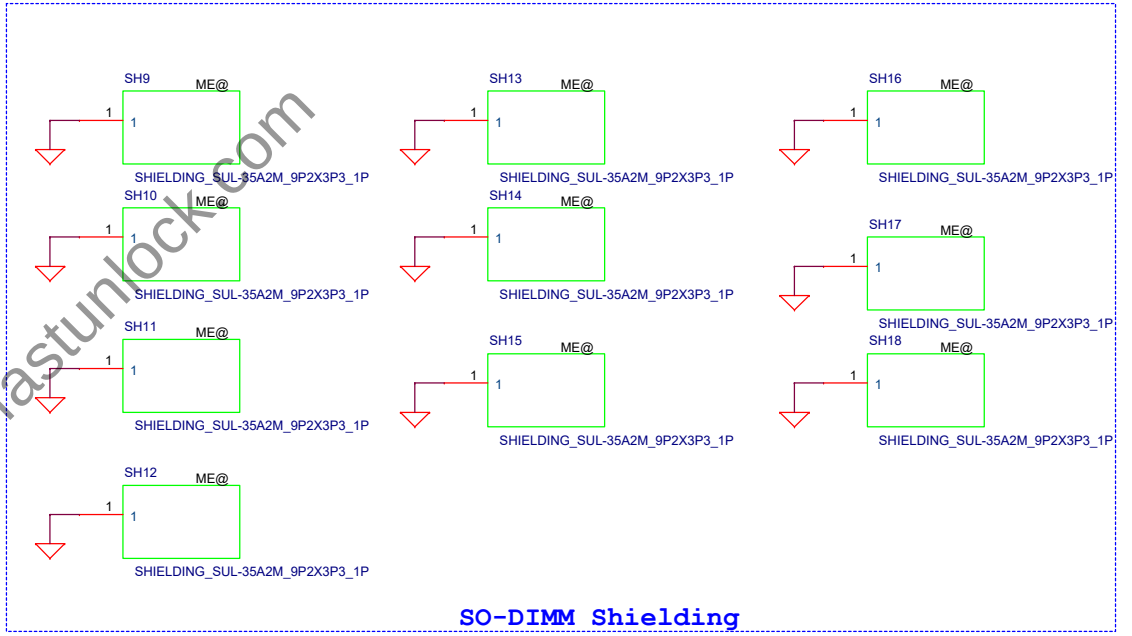
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

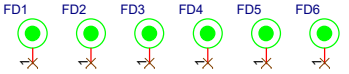
Title: *Virtual symbol*

Size	Document Number	Rev
C	¥550	0.1

Date: Friday, February 21, 2020 Sheet 63 of 83







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Hole**

Size	Document Number	Rev
B	Y550	1.0

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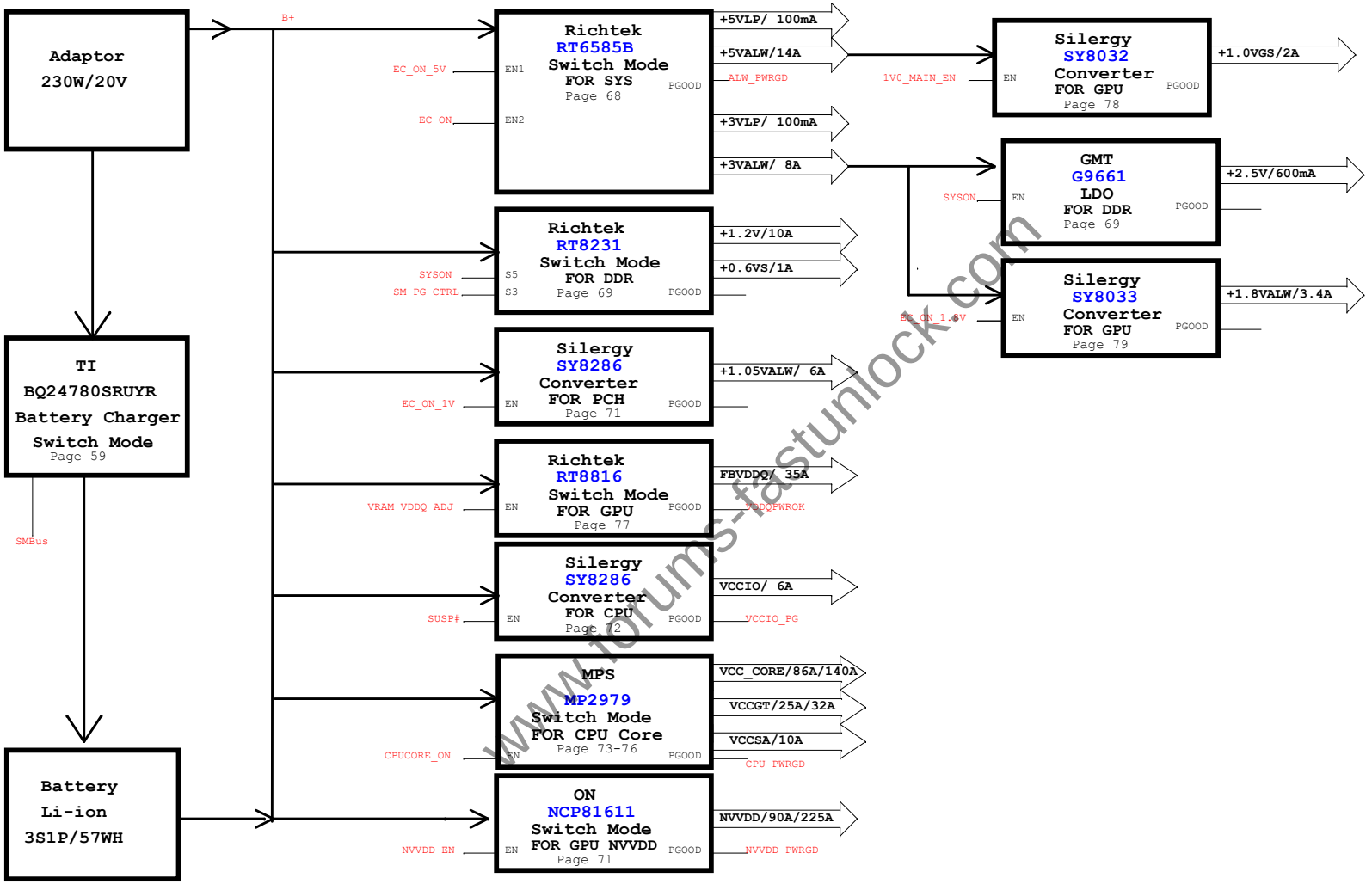
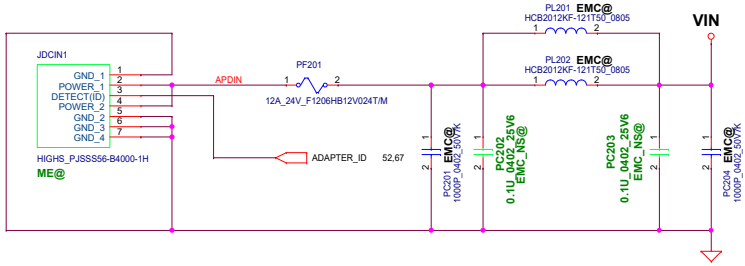


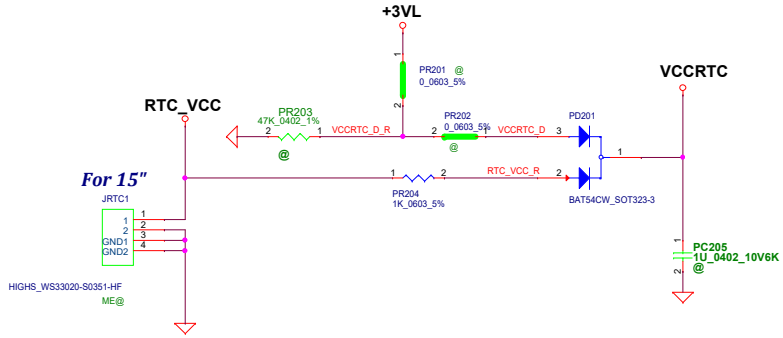
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

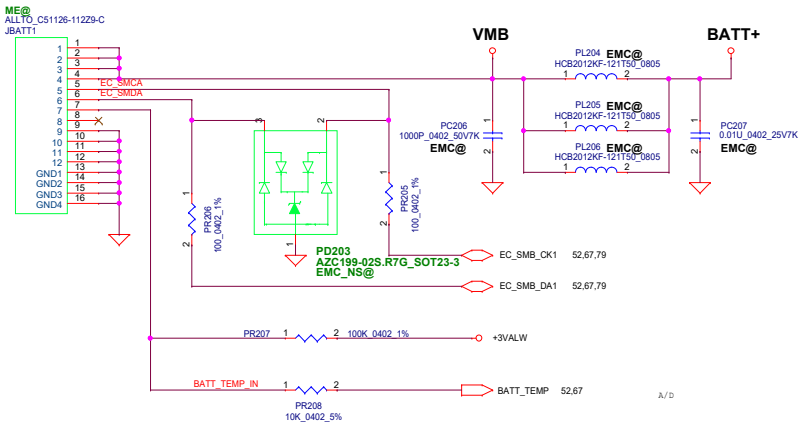
Title: **Power Diagram**

Size	Document Number	Rev
Custom	Y550	1.0

Date: Wednesday, February 19, 2020 Sheet 65 of 83

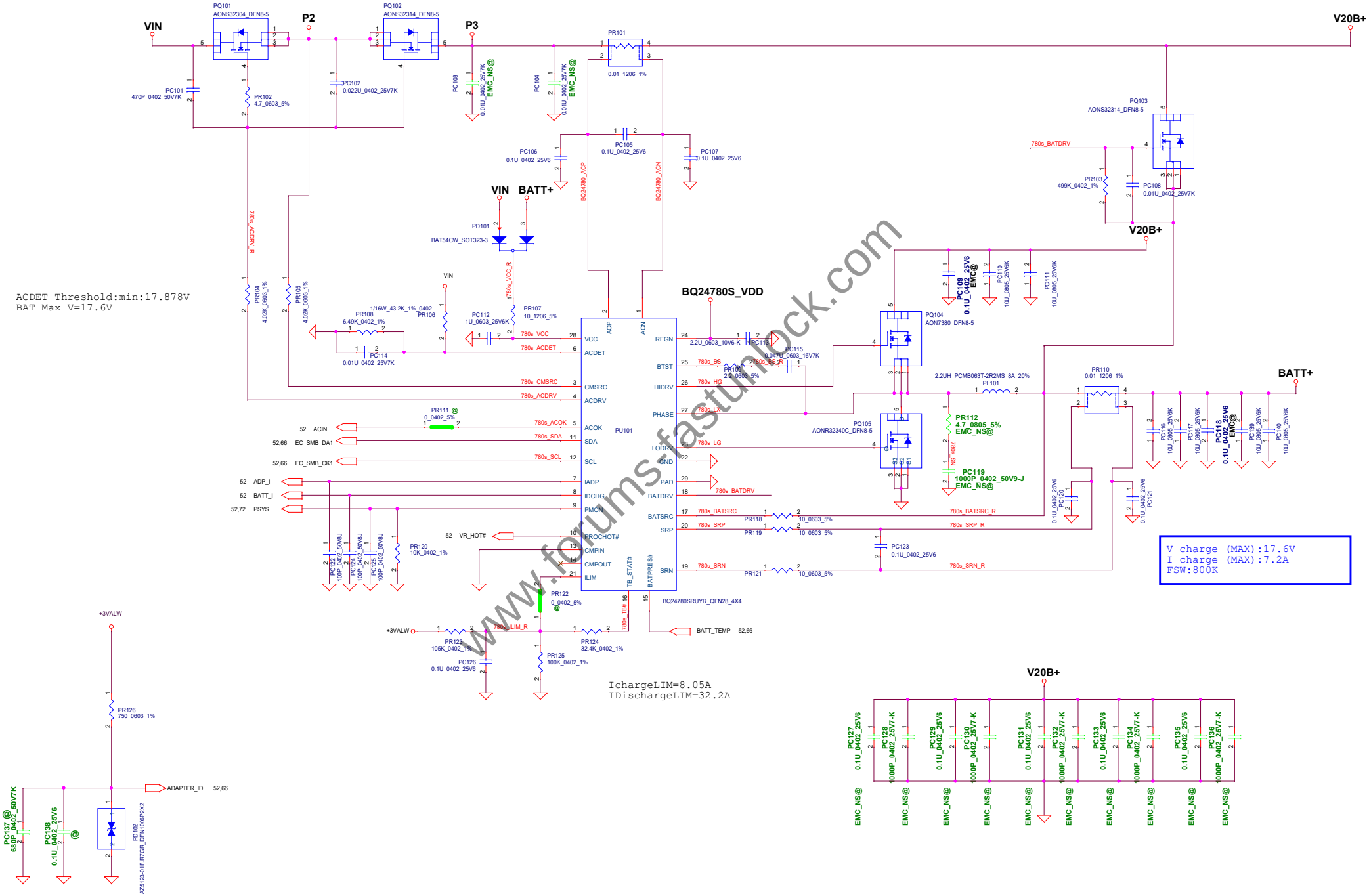






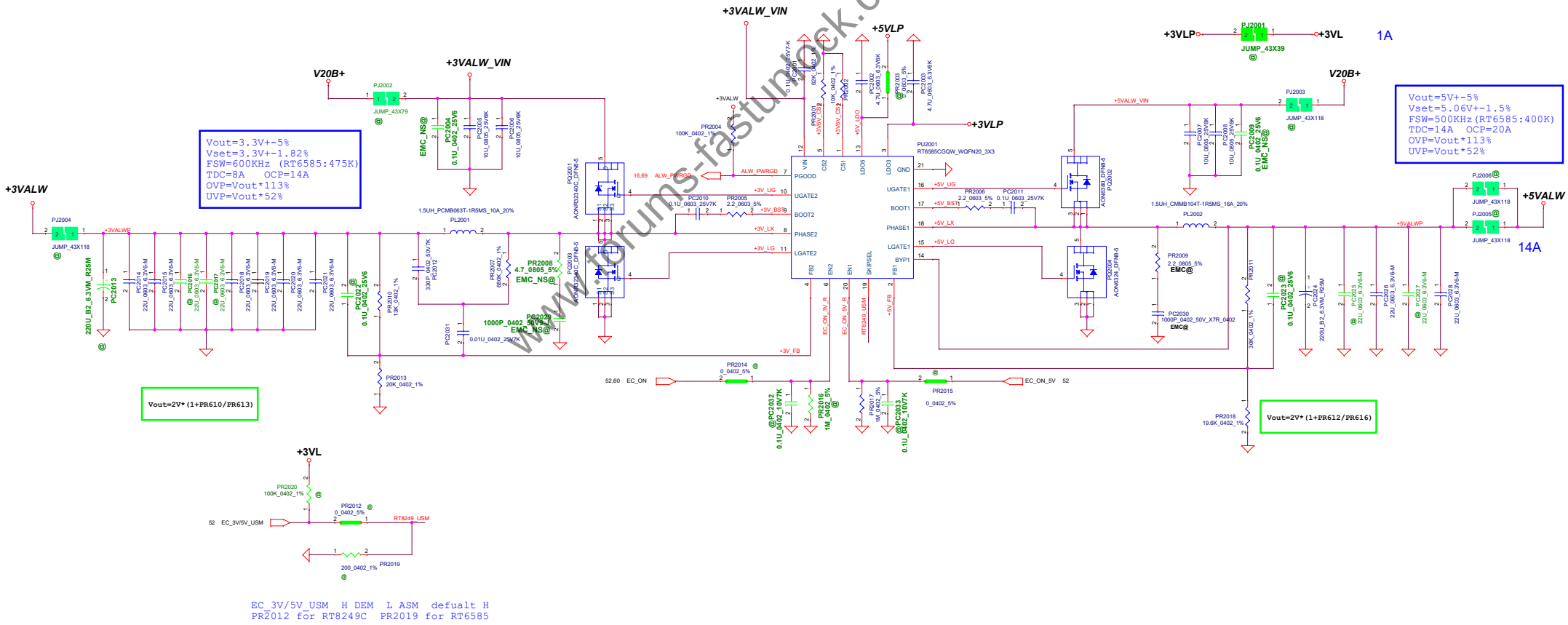
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size C	Document Number Y550		Rev 1.0
Date: Wednesday, February 19, 2020	Sheet 66 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-charger		
Size	Custom	Document Number	Y550
Rev	1.0		
Date:	Wednesday, February 19, 2020	Sheet	67 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-3/5VALW
Size	
Document Number	Y550
Rev	1.0
Date:	Wednesday, February 19, 2020
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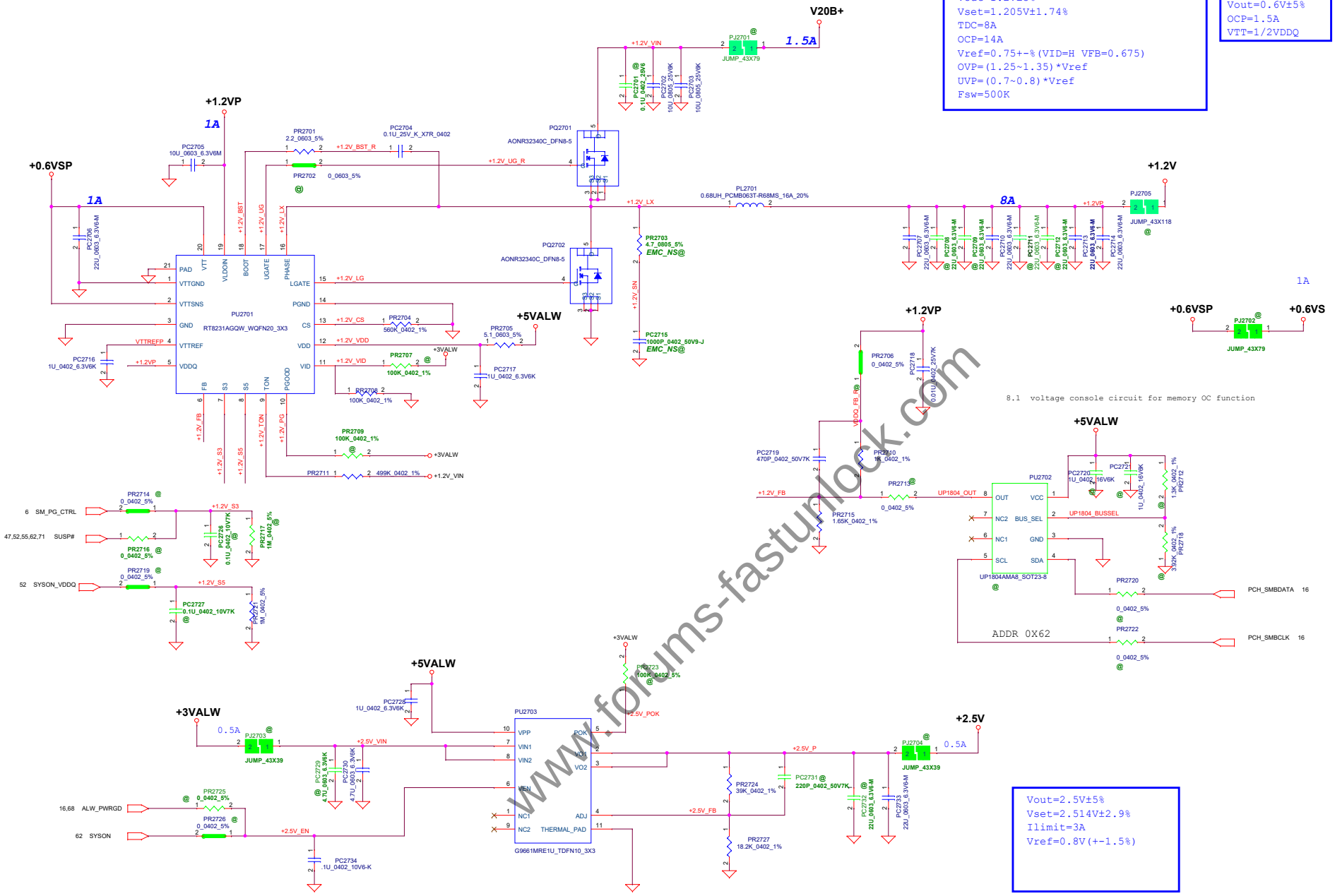

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VDDQ/VTT		
Size	Custom	Document Number	Y550
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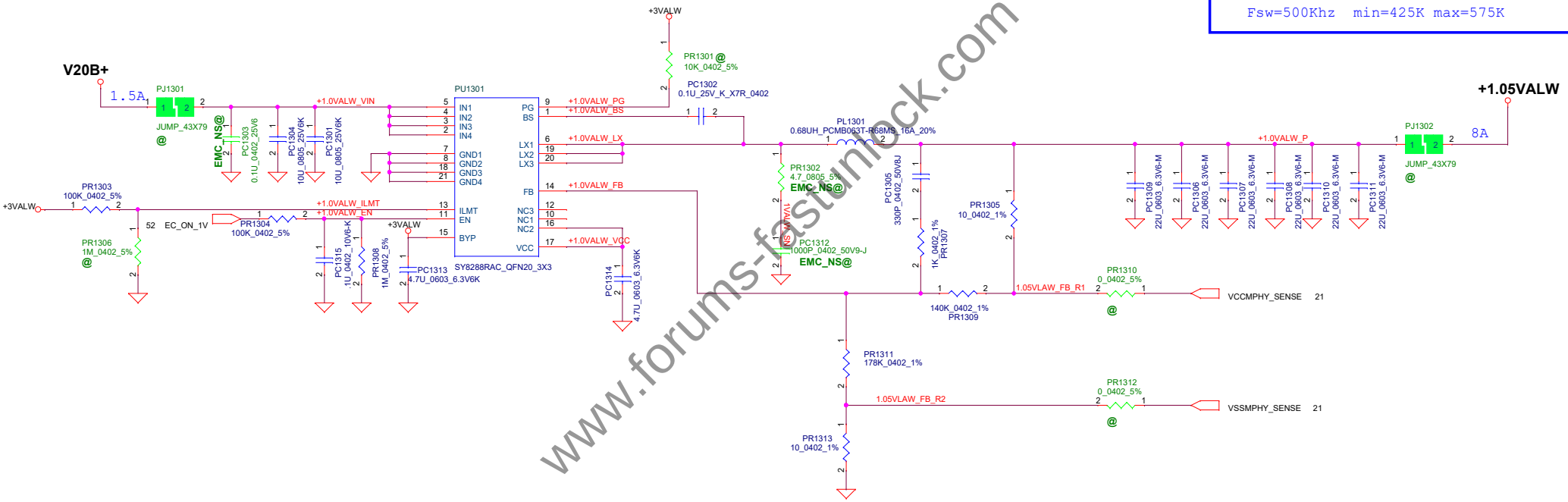
Vout=1.05V±5%
Vset=1.072V±1.87%
Vref=0.6V(+-1%)
TDC=8A
OCP=16A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.0VALW**

Size	Document Number	Rev
Custom	Y550	1.0

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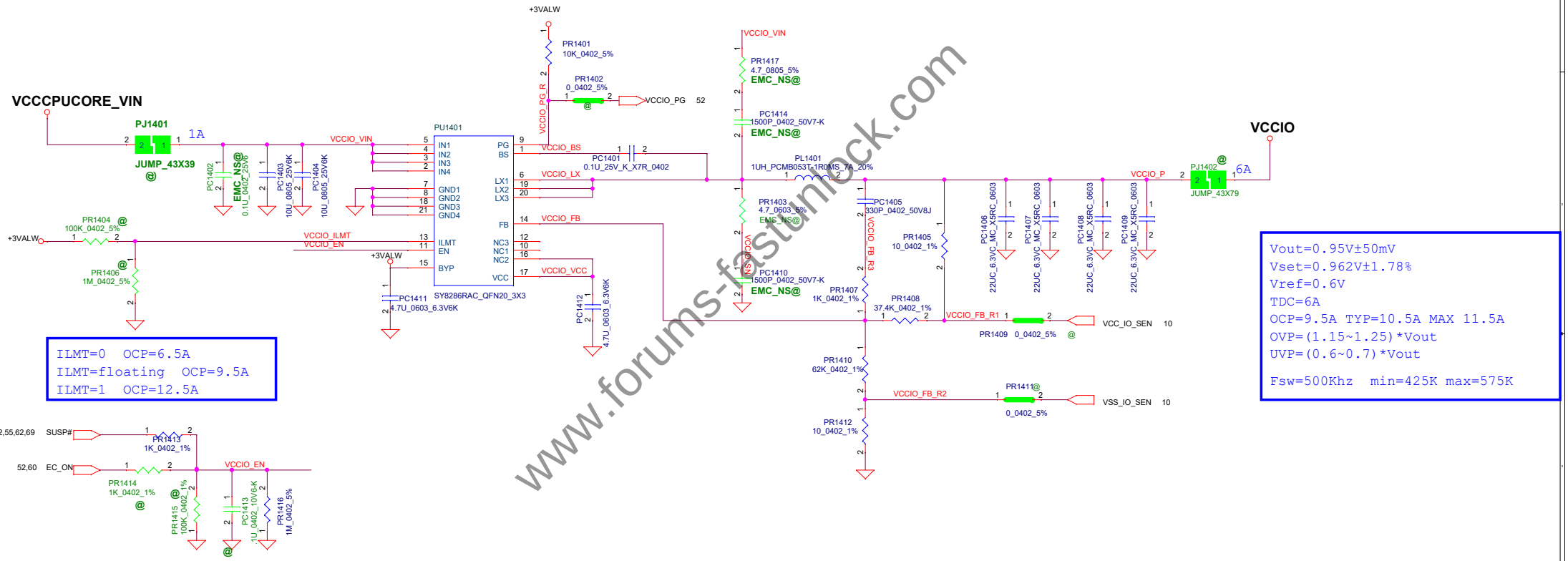

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VCCIO		
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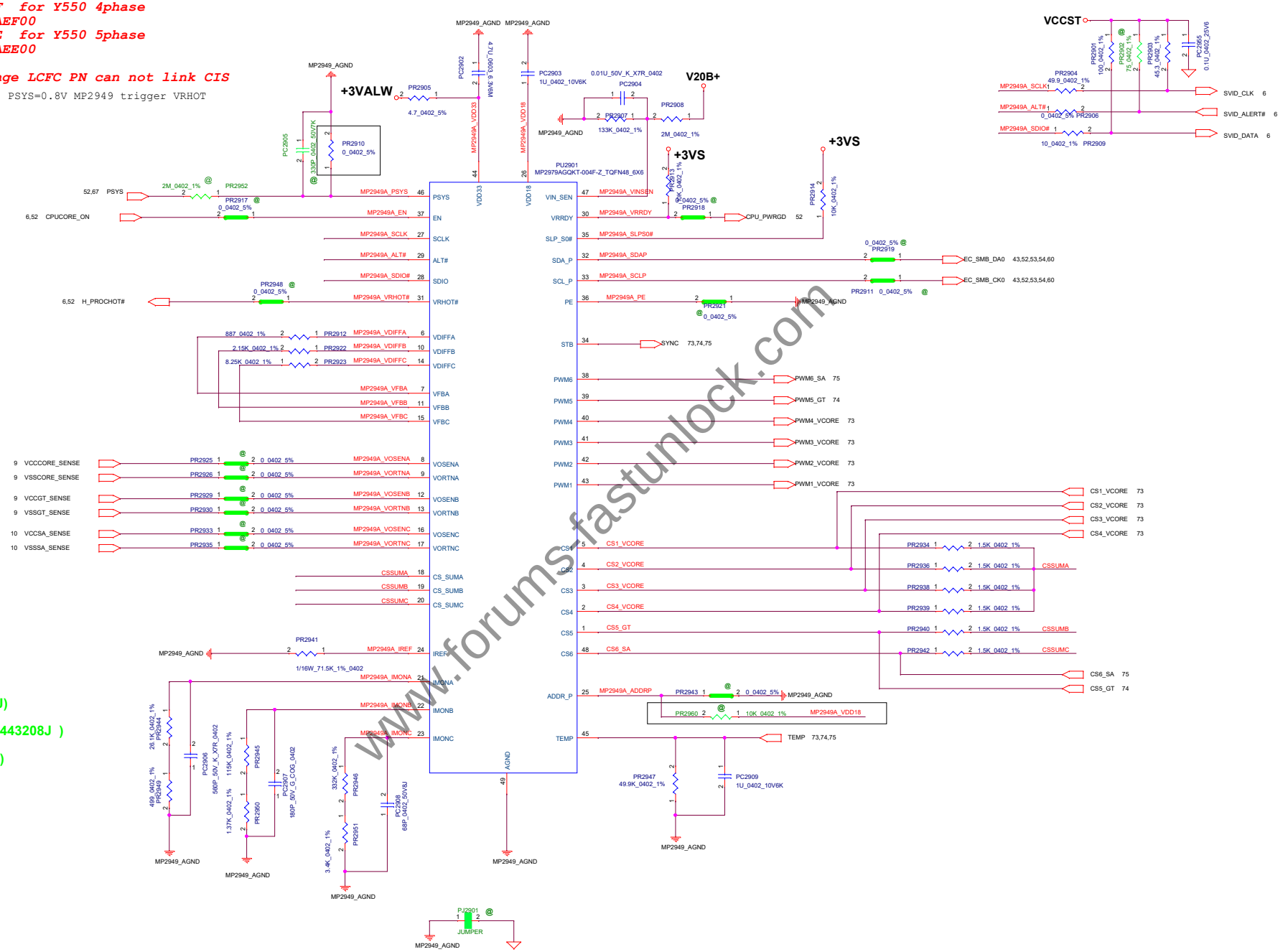
MP2979AGQKT-004F for Y550 4phase
LCFC PN: SA0000AEF00
MP2979AGQKT-004E for Y550 5phase
LCFC PN: SA0000AEE00

PU2901 only change LCFC PN can not link CIS

PSYS=0.8V MP2949 trigger VRHOT



5Phase
PR2912=887ohm(SD00000XK8J)
PR2944+PR2949=22.567K
(22.1K SD03422128J+432 SD03443208J)
PC2907=180pF(SE000017A00)
PR2939=750ohm(SD03475008J)

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-IMVP8_MP2949

Size: Custom | Document Number: Y550 | Rev: 1.0

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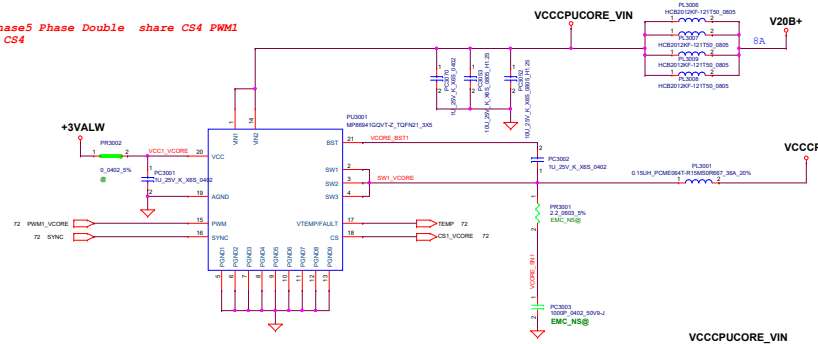
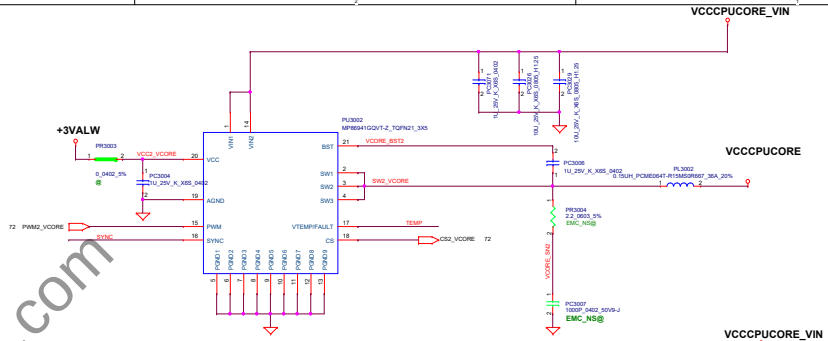
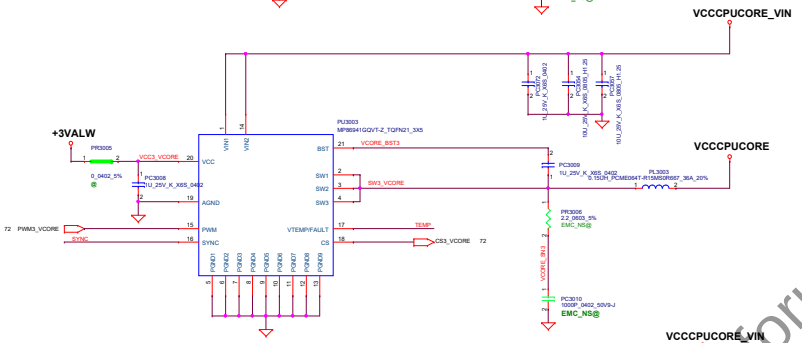
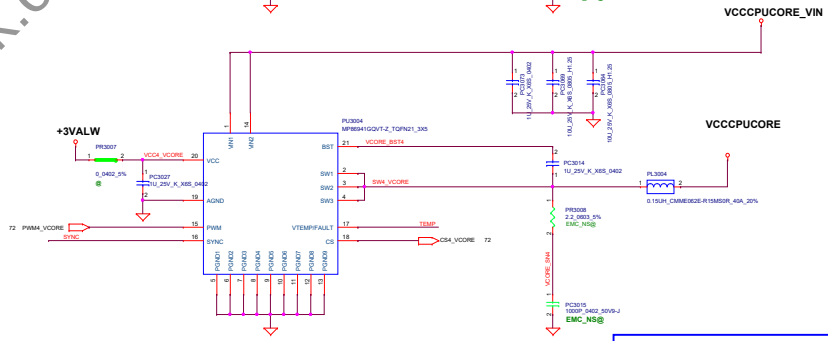
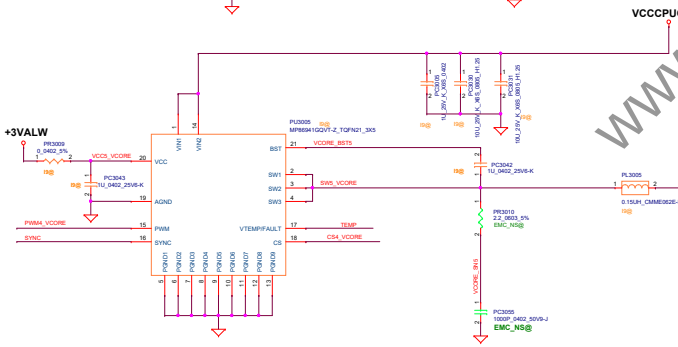
Phase4 Phase5 Phase Double share CS4 PWM1
CS share CS4





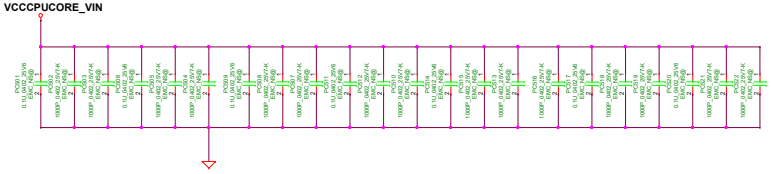


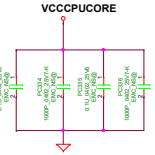




Vboot=0V Loadline=1.1mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=125A Performance Line(5phase) Iccmax=165A
TDC=86A Base Line(4phase) Iccmax=140A
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz

Y540:330u*2PCS+22u*19PCS
Y550:follow Y540 Vendor
PDG:470uF*4pcs+47uF*33pcs
Actual:330u*3PCS+22u*19PCS





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCCPUCORE

Size	Document Number	Rev
Custom	Y550	1.0

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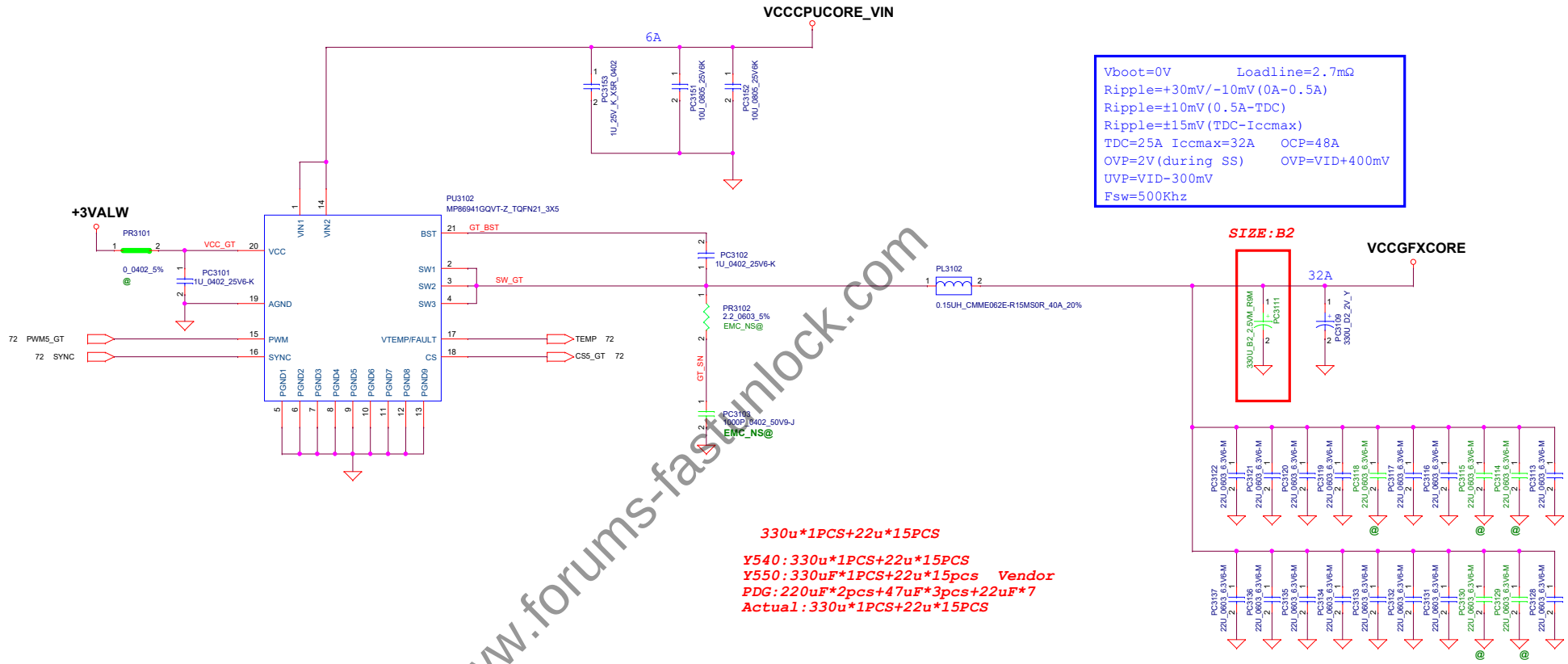

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCGFXCORE**

Size: Custom | Document Number: **Y550** | Rev: 1.0

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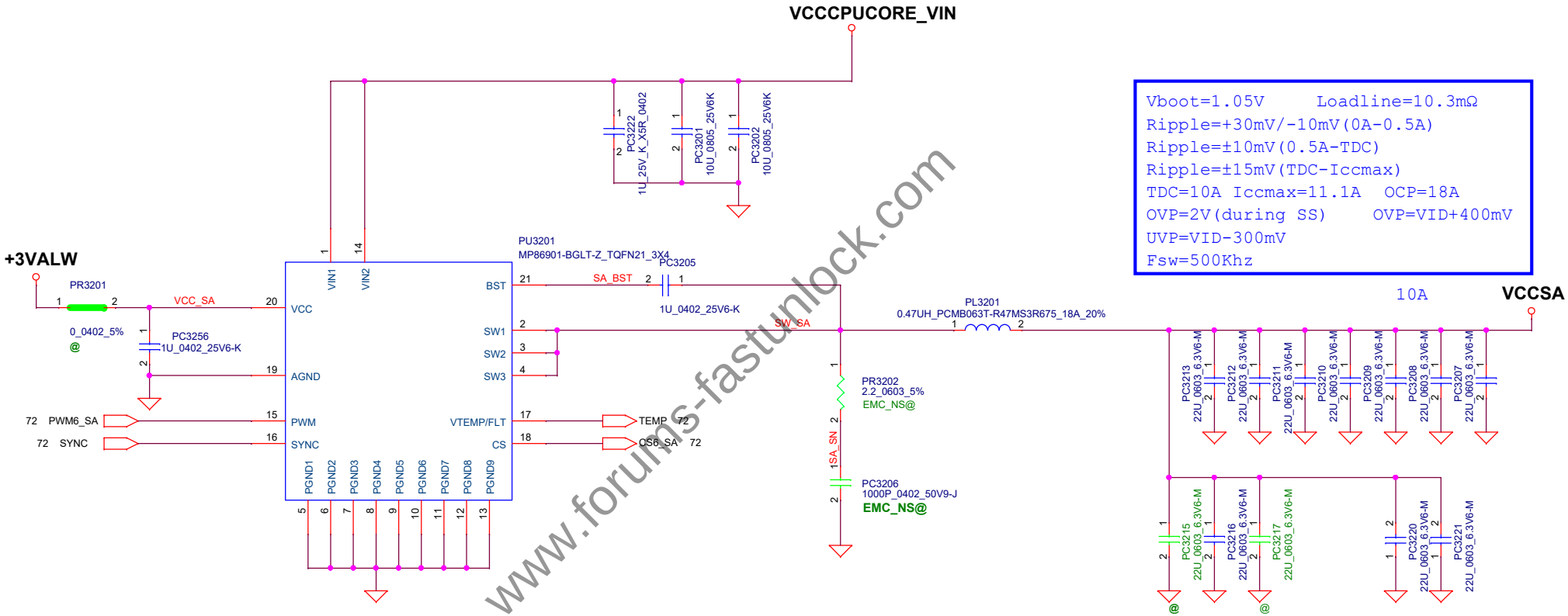

Y540:22u*10PCS
Y550:22u*10pcs Vendor
PDG:220uF*1pcs+47uF*4pcs+22uF*4
Actual:22u*10PCS

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCSA**

Size	Document Number	Rev
B	Y550	1.0

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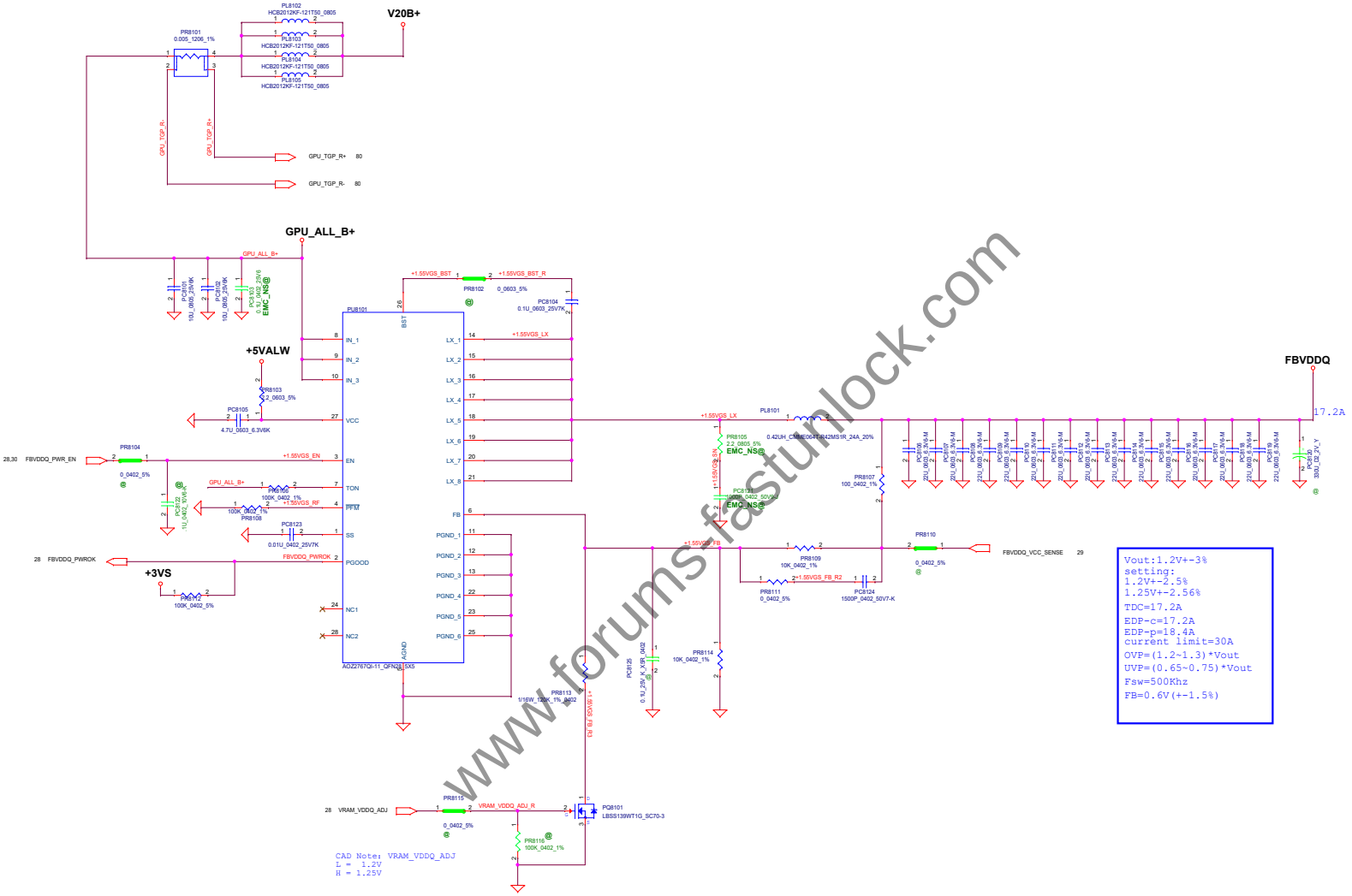
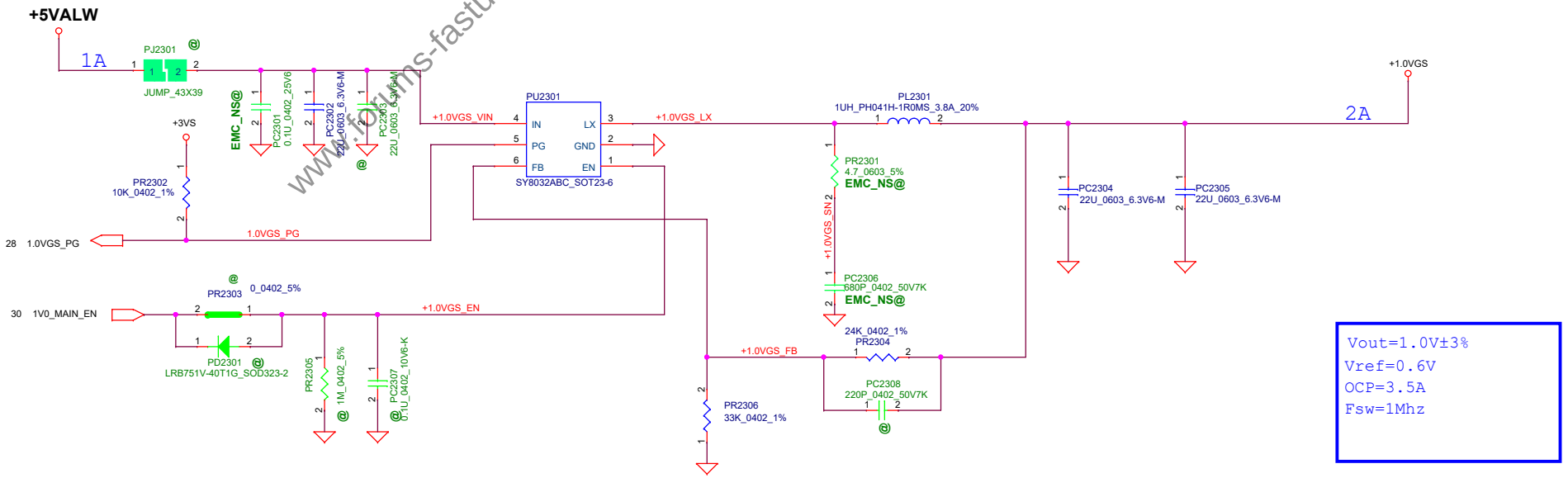


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

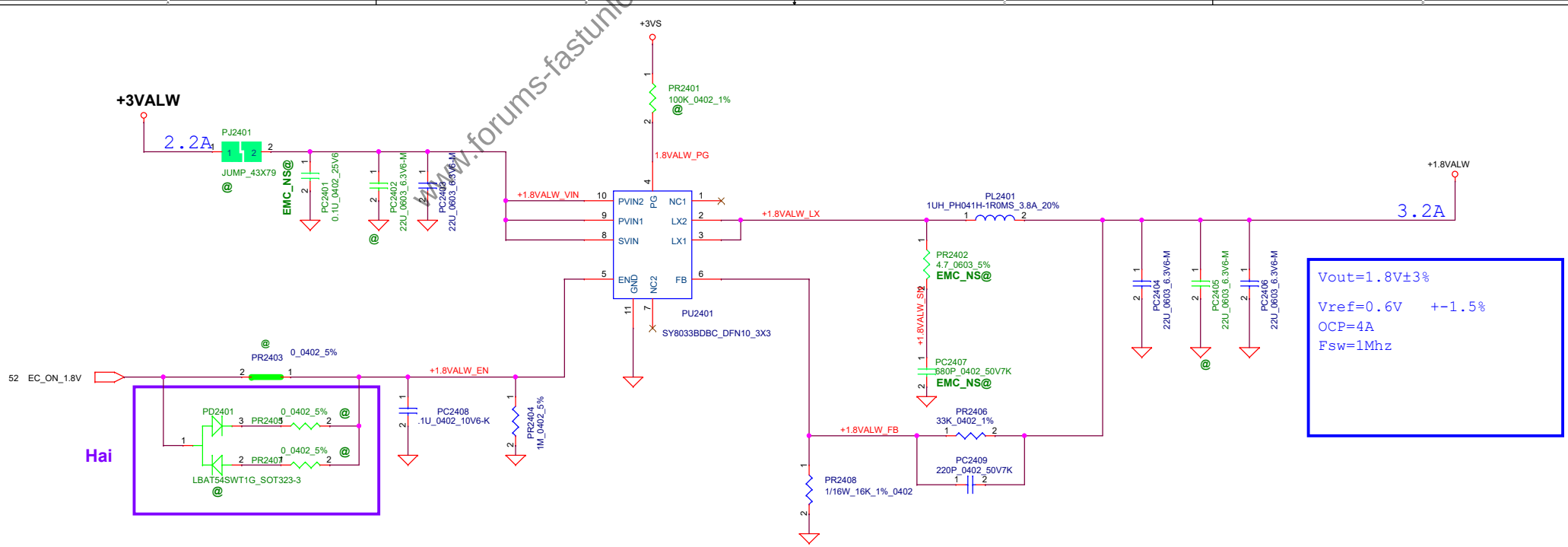
Title	PWR-FBVDDQ		
Size: Custom	Document Number: Y550		Rev: 1.0
Date: Wednesday, February 19, 2020	Sheet 75 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

Size: Custom	Document Number: ¥550	Rev: 1.0
Date: Wednesday, February 19, 2020	Sheet 77 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

Size: Custom	Document Number: ¥550		Rev: 1.0
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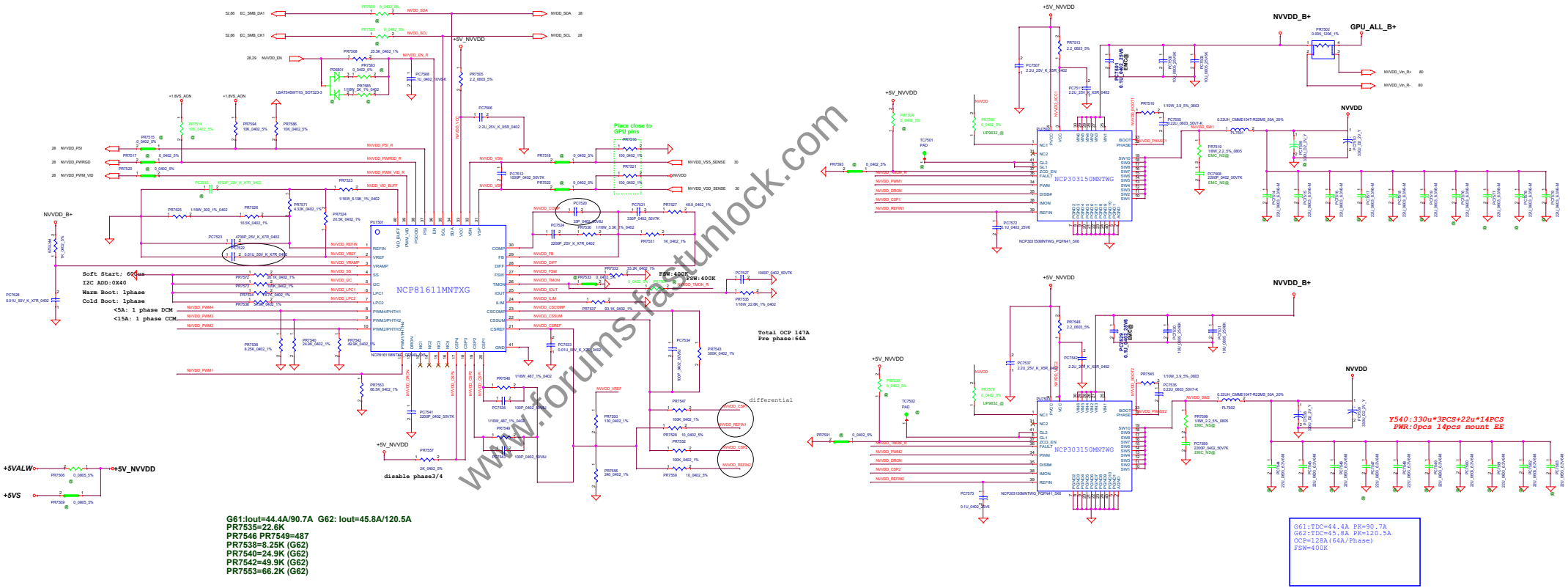
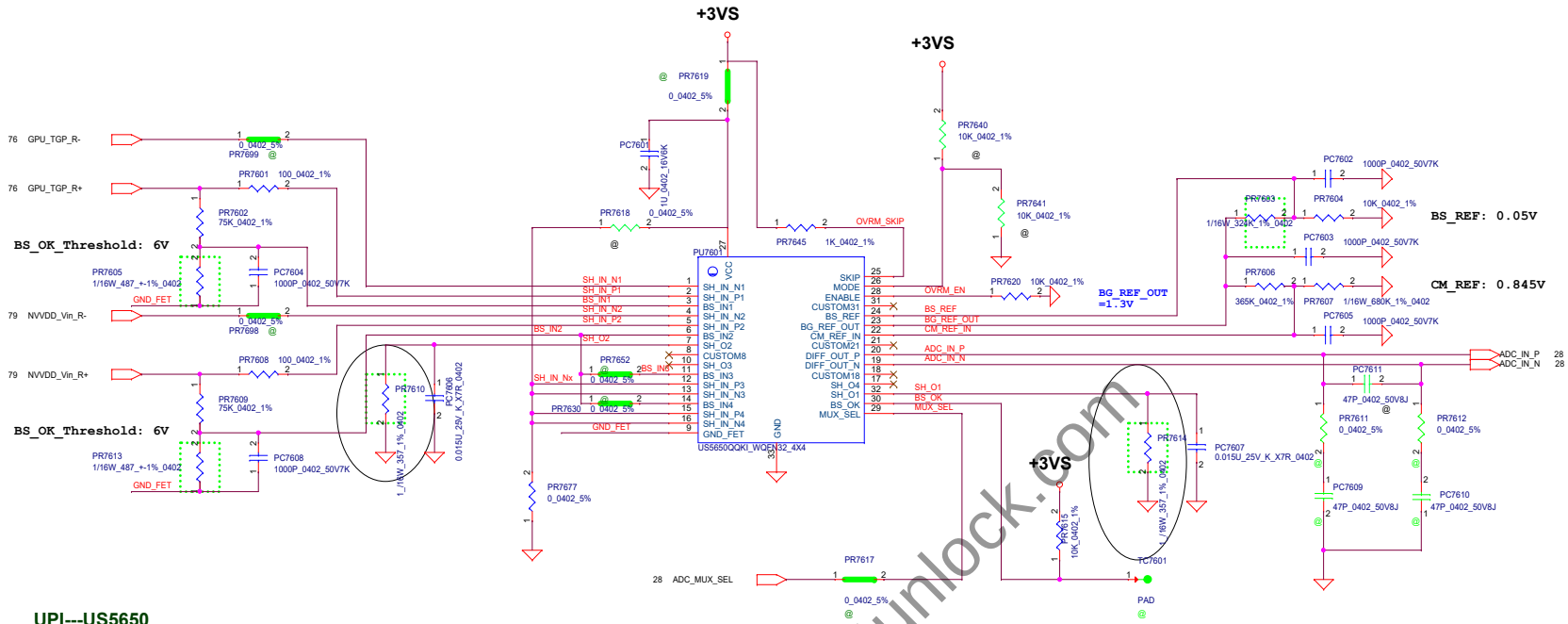


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-NVVDD		
Size: Custom	Document Number: Y550		Rev: 1.0
Date: Wednesday, February 14, 2018	Sheet 78 of 83		



UPI---US5650
PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-NVVDDS		
Size	Document Number	Rev	
C	Y550	1.0	
Date:	Wednesday, February 19, 2020	Sheet	80 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: ***Virtual symbol***

Size	Document Number	Rev
C	***¥550***	1.0

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Title

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Size	Document Number	Rev
C	***¥550***	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: ***Blank***

Size	Document Number	Rev
C	¥550	1.0

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