ZZZ1

PCB
Part Number = DAZXXXXX
LA-D961P

PCB@

Compal Confidential

CCA20/21 Schematics Document

AMD Bristol Ridge (colay Stoney Ridge) Platform

DGPU AMD R16-M1-30

LA-D961P REV: 0.2

2016-02-16

Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

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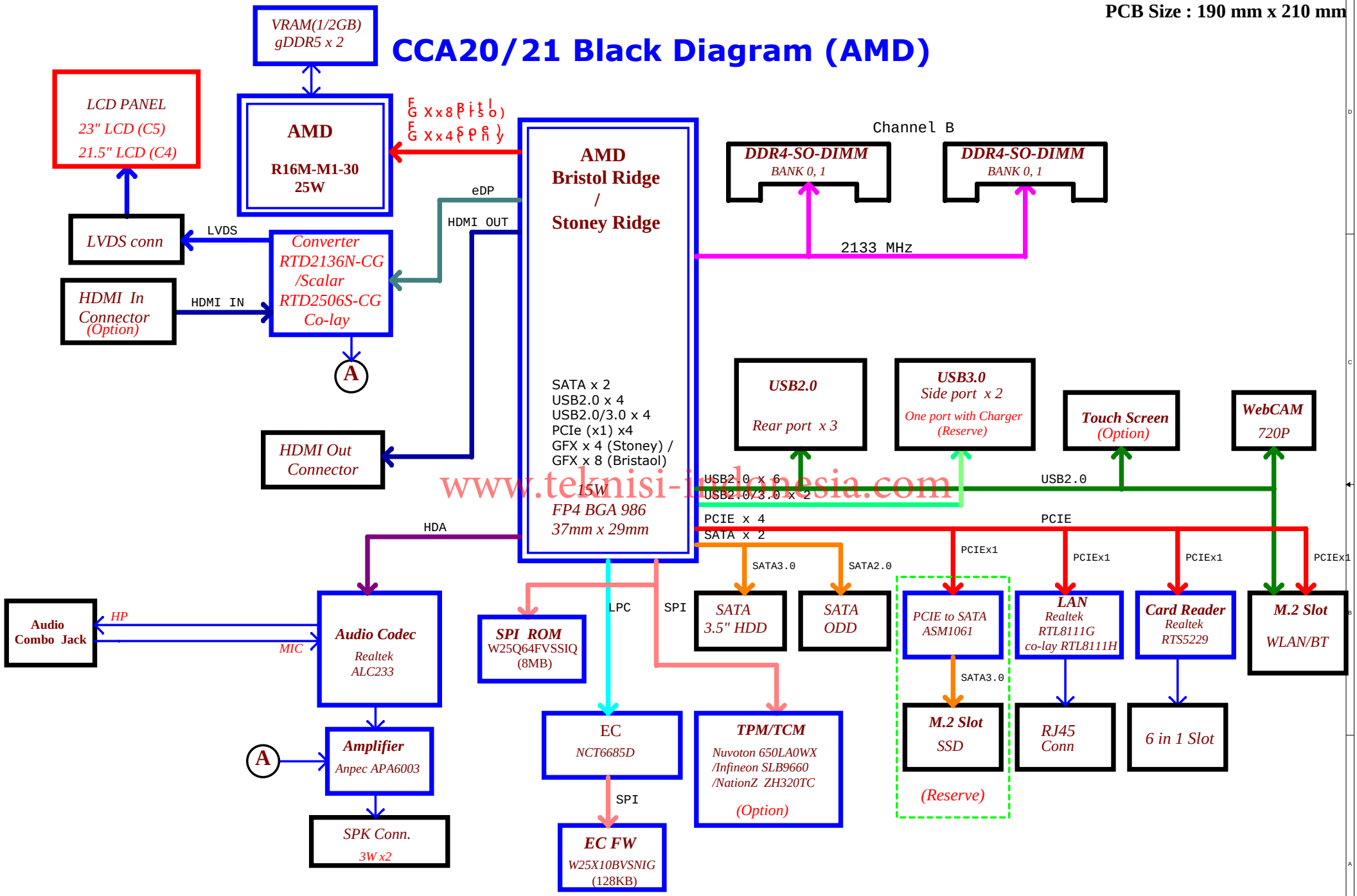
Title	COVER PAGE		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 1 of 56		

PCB Size : 190 mm x 210 mm

CCA20/21 Black Diagram (AMD)



Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

Compal Electronics, Inc.			
Title	CCA20/21 Black Diagram		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 2 of 56		

Voltage Rails

Power Plane	Description	S0	S3	S5
+DC20V	Adapter power supply (19V)	ON	ON	ON
+APU_CORE	Core voltage for processor core current	ON	OFF	OFF
+APU_CORE_NB	Voltage for processor Northbridge (NB) current	ON	OFF	OFF
+0.95_1.05VALW	0.95V always on power rail	ON	ON	ON
+0.95_1.05VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.2V_VDDQ_S3	VDDQ power rail for APU and DDR	ON	ON	OFF
+3V3_DSW	3.3V always for EC only	ON	ON	ON
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	3.3V RTC power	ON	OFF	OFF
+3VGS_S0	3.3V VGA power	ON	OFF	OFF
+1.8VGS_S0	1.8V VGA power	ON	OFF	OFF
+1.5V_VRM_S0	1.5V VGA/VRAM power	ON	OFF	OFF
+0.95VGS_S0	0.95V VGA power	ON	OFF	OFF
+VGA_CORE_S0	VGA power	ON	OFF	OFF
+APU_CORE_GFX	Voltage for processor Graphics (GFX) current	ON	OFF	OFF
+RTC_APU	1.5V RTC power	ON	ON	ON
+12VALW	12V switched power rail for Amp.	ON	ON	ON
+1.5VALW	1.5V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VRAM_1.5VP	1.5V for VRAM power rail	ON	OFF	OFF

PCIE(GPP) Port Table

Port	Device
0	LAN
1	WLAN/BT
2	Card reader
3	SATA Bridge

SATA Port Table

Port		Device
6G	0	HDD
	1	ODD

USB Port Table

	Port	Device
USB 2.0	0	USB20- (Rear I/O)
	1	USB20- (Rear I/O)
	2	USB2.0- (Rear I/O)
	3	WLAN/BT
	4	Touch Panel
	5	Web Camera
	6	USB30(2.0)- (Side I/O)
	7	USB30(2.0)- (Side I/O)
USB 3.0	0	
	1	
	2	USB30- (Side I/O)
	3	USB30- (Side I/O)

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	Pre-MP
4	MP

BOM Structure Table

BOM Structure	BTO Item
@	Unpop
DIS@	DIS pop component
UMA@	UMA pop component
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
RF@	RF pop component
@RF@	RF unpop component
CVT@	eDP to LVDS Converter IC
SC@	Scalar
SC_C4@	For Scalar CCA21
SC_C5@	For Scalar CCA20
HDMIIN@	HDMI-IN
CHG@	USB Charger Function
NCHG@	Non USB Charger Function
TPM@	TPM components for all TPM
Nuvton@	TPM for Nuvton
ST@	TPM for ST
Infineon@	TPM for Infineon
SSD@	Components for M2.Slot SSD
SSD_EMI@	EMI pop for SSD
@SSD_EMI@	EMI unpop for SSD
SSD_ESD@	ESD pop for SSD
@SSD_ESD@	ESD unpop for SSD
76_1G@	VRAM type for 1G
76_2G@	VRAM type for 2G
BR@	For Bristol only
BR_DIS@	For Bristol DIS only

SMBus List

EC SMBus Port0 (+3VS_S0)

Device	Address	HEX
SB-TSI (APU)	1001 100X b	98H
DGPU Temp.	1000 001X b	82H
Thermel IC	1001_101xb	9AH

EC SMBus Port2(+3V3_DSW)

Device	Address	HEX
RTD2506S	1001-0100xb	94
RTD2136N-CGT	1001-0100xb	94
CONVERTOR	0110-0010xb	62

APU SMBus Port0 (+3VS)

Device	Address	HEX
DDR JDIMM1	1010 001Xb	A2H
DDR JDIMM2	1010 011Xb	A6H
RTD2506S		

PCB

ZZZ
DA6001L3000
DA6001L3000, PCB 1PX LA-D961P REV0 M/B
PCB@

BARCODE

ZZZ8 @ BARCODE_8X8

ZZZ9 @ BARCODE_12X4

ZZZ10 @ BARCODE_20X4

ZZZ11 @ BARCODE_10X10

SKU ID(Project) Table

SKU (UMA&DIS)	BOM Configure Table
CCA21 MB 1 431A2P38L01 (UMA)	UMA@/PCB@/E2@/EMI@/ESD@/RF@/CVT@/NCHG@ /C4@
CCA21 (3rd Source) MB 2 431A2P38L02 (DIS) (X7668038L01)Hynix 1G	DIS@/PCB@/E2@/NCHG@/EMI@/ESD@/RF@/CVT@/SSD@/SSD_EMI@ /C4@/76_1G@
CCA21 MB 3 431A2P38L03 (DIS) (X7668038L02)Micron 1G	DIS@/PCB@/A9@/NCHG@/EMI@/ESD@/RF@/CVT@/SSD@/SSD_EMI@ /C4@/76_1G@
CCA20 MB 4 431A2P38L51 (UMA)	UMA@/PCB@/A6@/EMI@/ESD@/RF@/NCHG@ /C5@/SC@/SC_C5@/SSD@/SSD_EMI@/HDMIIN@
CCA20 (2nd Source) MB 5 431A2P38L52 (DIS) (X7668038L04)Samsung 2G	DIS@/PCB@/A6@/NCHG@/EMI@/ESD@/RF@/SC@/SC_C5@/C5@ /SSD@/SSD_EMI@/HDMIIN@/76_2G@
CCA20 MB 6 431A2P38L53 (DIS) (X7668038L03)Micron 2G	DIS@/PCB@/A9@/NCHG@/EMI@/ESD@/RF@/SC@/SC_C5@ /C5@/SSD@/SSD_EMI@/HDMIIN@/76_2G@

Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

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Title: NOTES LIST

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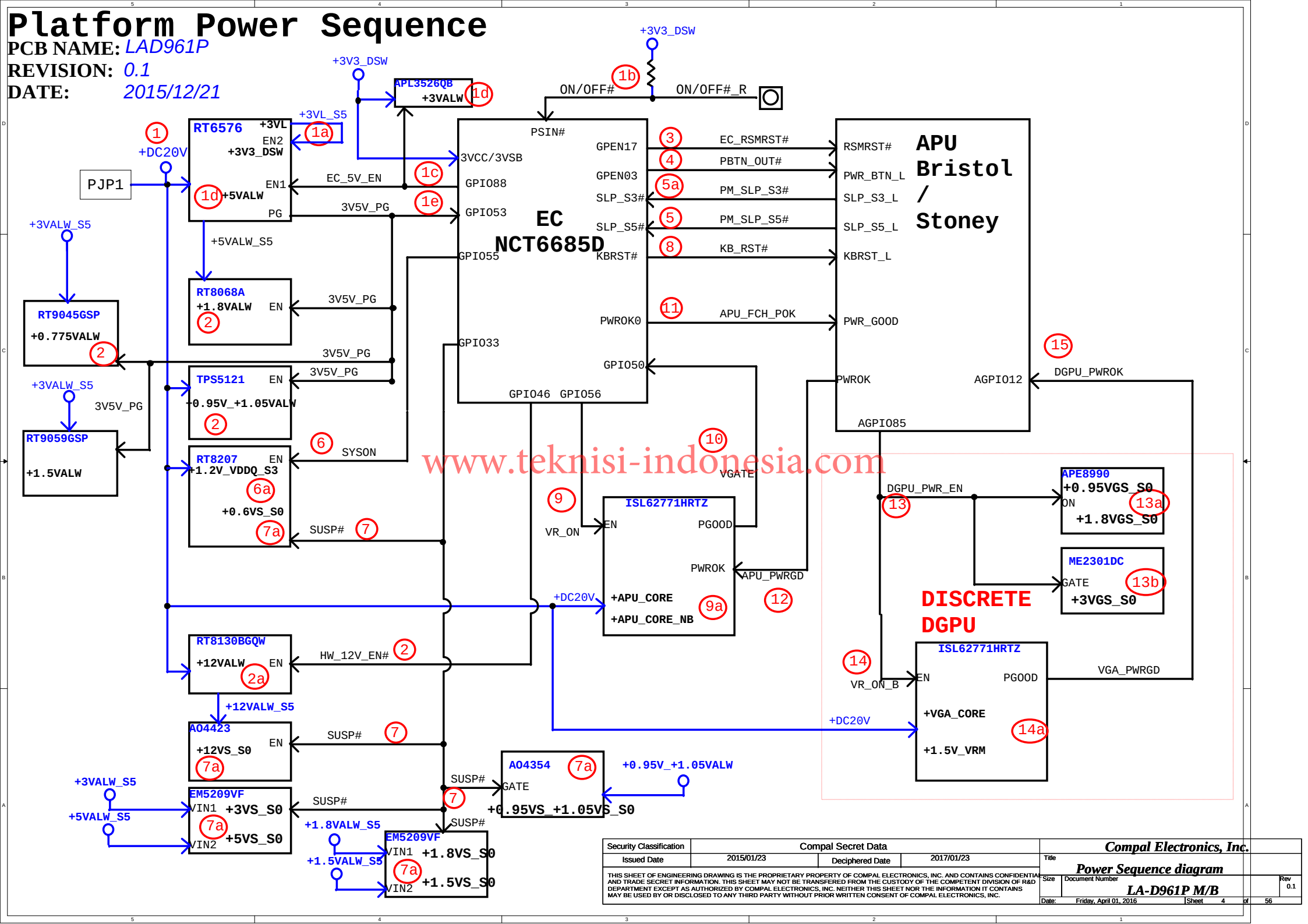
Platform Power Sequence

PCB NAME: *LAD961P*
REVISION: *0.1*
DATE: *2015/12/21*



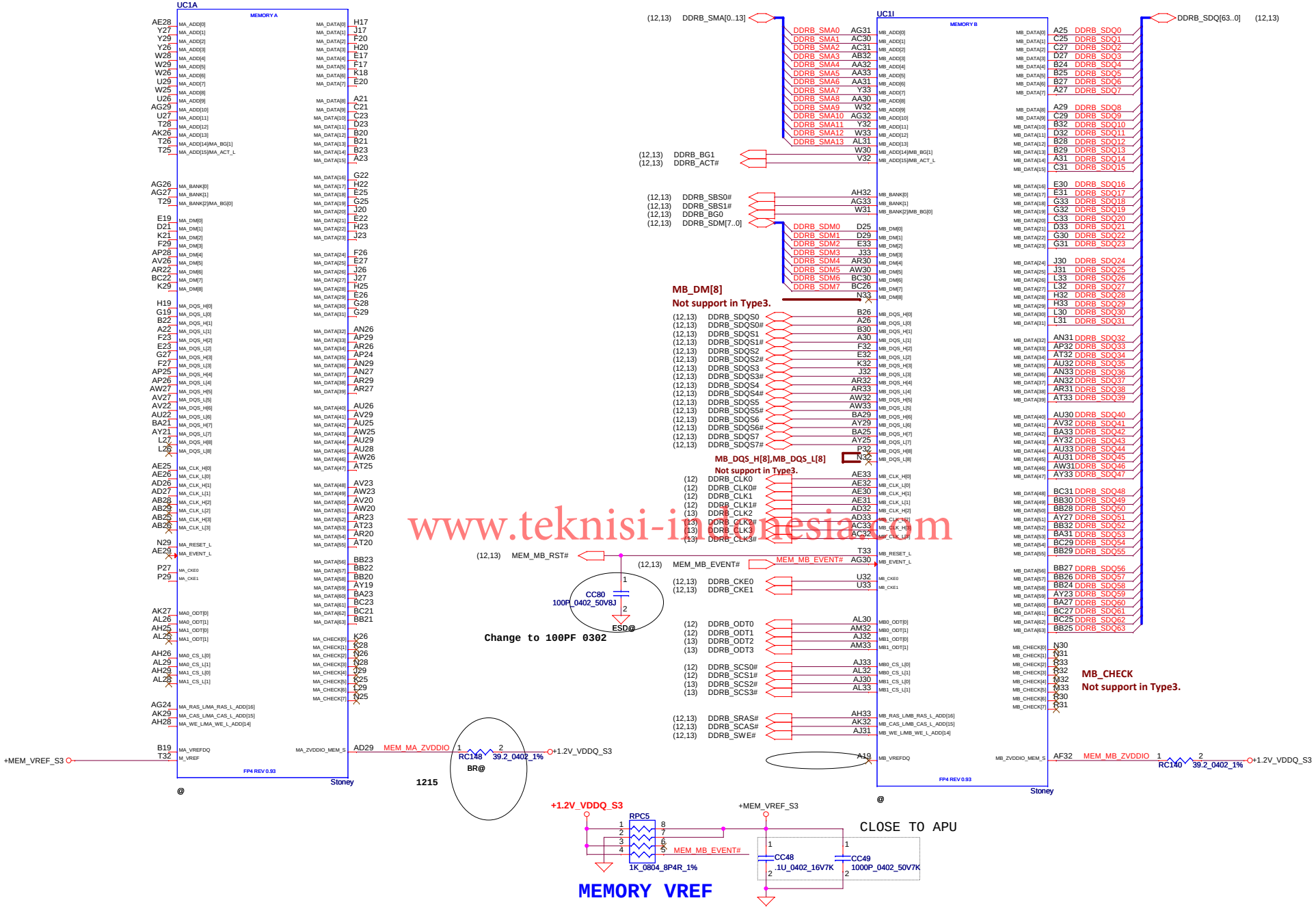
Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: *Power Sequence diagram*

Size | Document Number: *LA-D961P M/B* | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 4 of 56



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Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

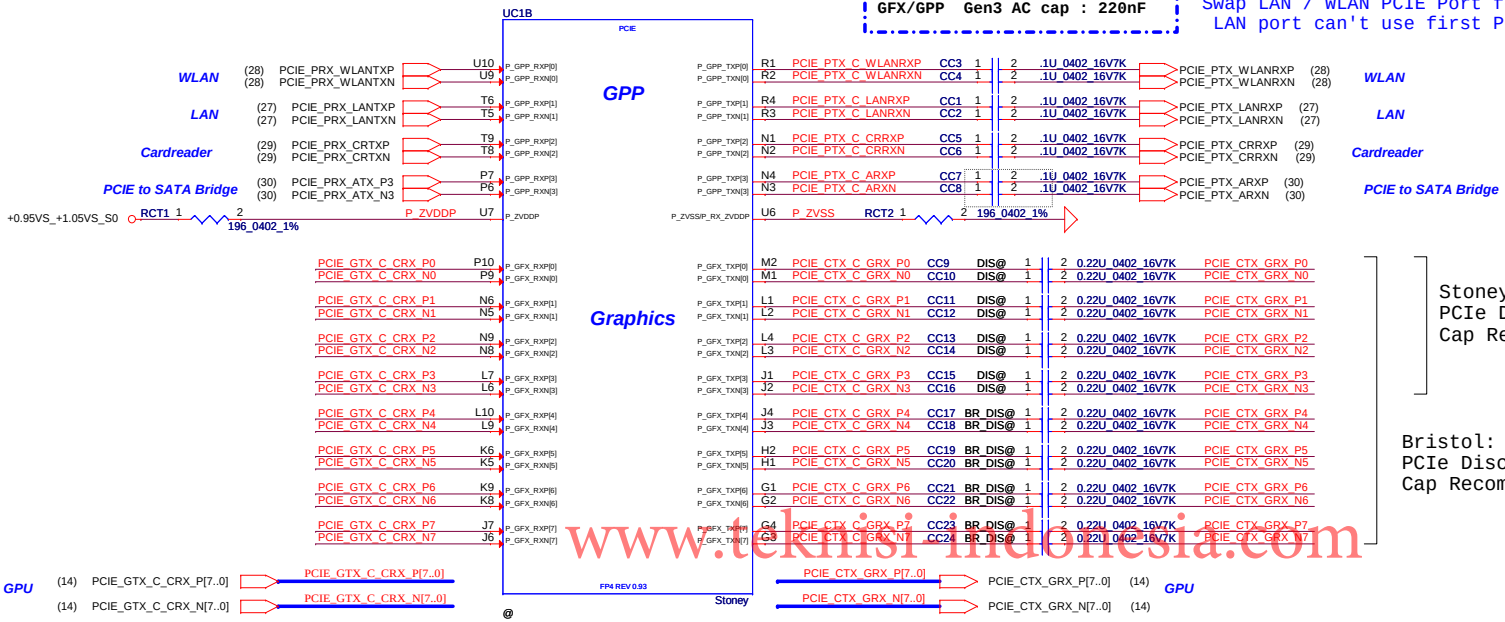
Title: FP4 MEMORY INTERFACE

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

Date: Friday, April 01, 2016 Sheet 5 of 56

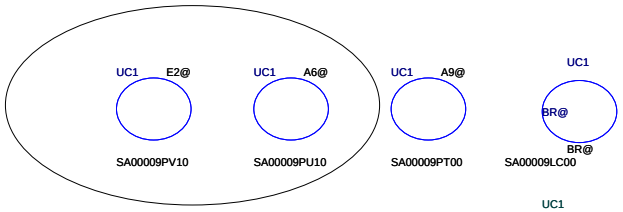
GFX/GPP Gen2 AC cap : 100nF
GFX/GPP Gen3 AC cap : 220nF

Swap LAN / WLAN PCIE Port for Lenovo DCL rule-
LAN port can't use first PCIE port. 1221



Stoney:
PCIe Discrete Graphics Port: PCI Gen3 x4
Cap Recommended Value: 220 nF

Bristol:
PCIe Discrete Graphics Port: PCI Gen3 x8
Cap Recommended Value: 220 nF



PVT USE R3 Part number 0330

Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: FP4 PCIE

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 6 of 56

Table 57. DisplayPort Configurations

Display Interface Configurations								
Display Interface	DP	DP x4				DP Aux +	DP Aux -	HPD	DP_BLON DP_DIGON DP_VARY_BL
		3	2	1	0				
DP		MainLink[3:0]				AUX[1]		HPD	not connected
DP++	DP	MainLink[3:0]				AUX[1]		HPD	not connected
	DVI or HDMI	Channel Clock	Ch 0	Ch 1	Ch 2	DDC Clock[2]	DDC Data[2]	HPD	not connected
Single-Link DVI		Channel Clock	Ch 0	Ch 1	Ch 2	DDC Clock[2]	DDC Data[2]	HPD	not connected
HDMI™		Channel Clock	Ch 0	Ch 1	Ch 2	DDC Clock[2]	DDC Data[2]	HPD	not connected
LVDS (Panel)		N/C	N/C	LVDS Translator		LVDS Translator[1]		HPD	Inverter Power LCD Logic Power Inverter Control

DP PORT	Port mapping
DP0	SCALER/CVT
DP1	HDMI-OUT
DP2	NC

HDMI out

(25) HDMI_TX2+ / (25) HDMI_TX2-
(25) HDMI_TX1+ / (25) HDMI_TX1-
(25) HDMI_TX0+ / (25) HDMI_TX0-
(25) HDMI_CLK+ / (25) HDMI_CLK-

eDP To LVDS Converter / Scaler

(21) EDP_TXP0 / (21) EDP_TXN0
(21) EDP_TXP1 / (21) EDP_TXN1

DP_VARY_BL, DP_BLON, DP_DIGON:
Type1&3--> VDD_18
Type2--> VDD_33

UC1C — DISPLAYIS/V2/JTAG/TEST — Stoney — FP4 REV 0.93

HDMI out

eDP To LVDS Converter

TPC1

TPC2 TPC3 TPC4 TPC5 TPC6 TPC7 TPC8 TPC9 TPC13 TPC14 TPC15 TPC16 TPC34 TPC33 TPC31 TPC32

Reserve 12/08

Remove UC12 , add RC20 on DP0_HPD 01/26
RC20 change to Short pad 0401

Remove RC9/RC20
change to idepedent resistor
0219

For APU_VDDGFX_RUN
(Bristol Only)

RC24 change to pop / RC26 change to non-pop for
HDMI-OUT mode 01/29

AMD requeir to separate pull down resistor for DP_STEREOSYNC/TEST36 12/23

Add 12/14

QC2 change to 2xBSS138 QC4/QC6 01/26
QC3 change to unpop 01/26

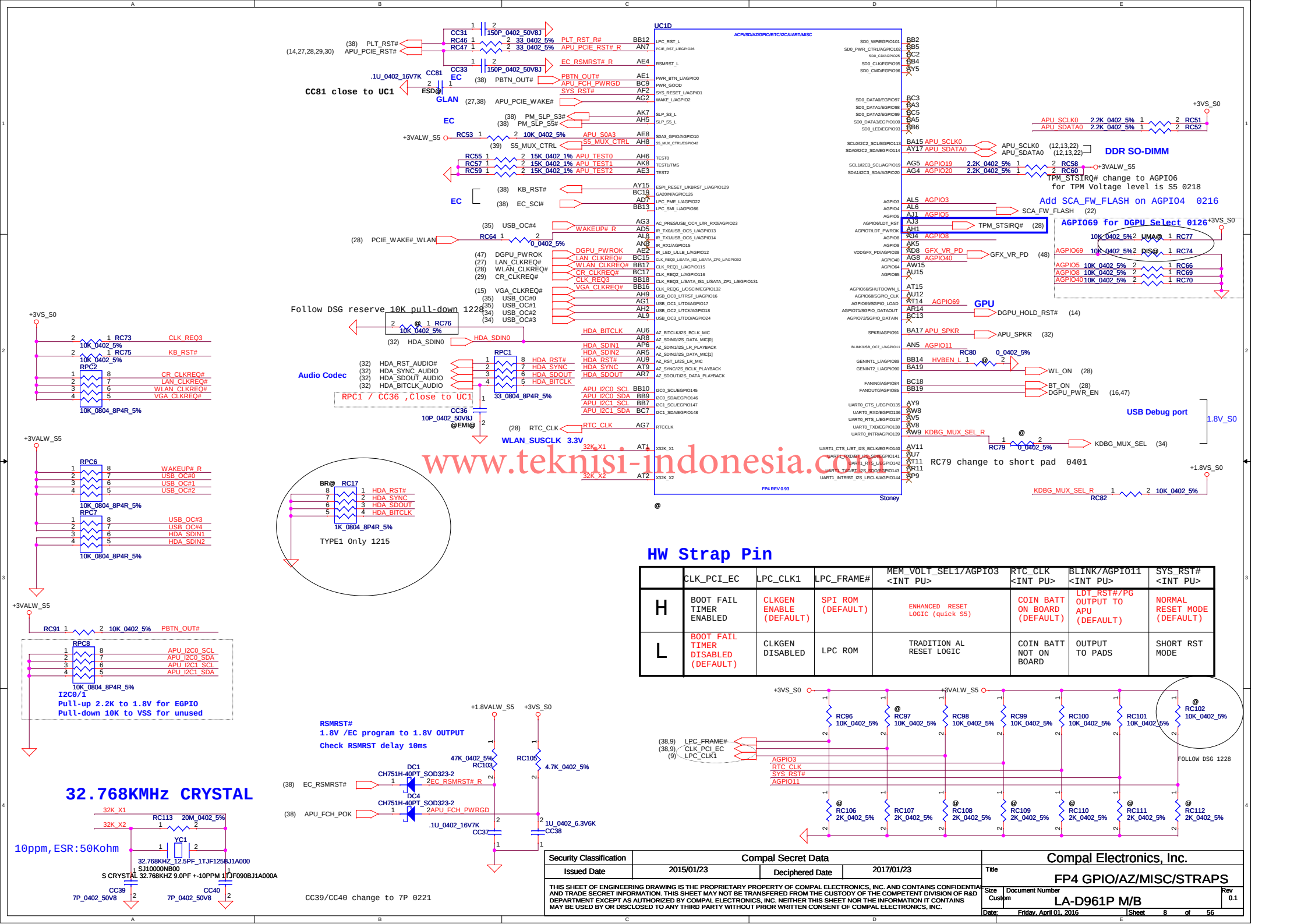
Remove HDT 12/08

TP place colse to APU
(Reduse EMI effect)

Resistor place colse to
APU (Reduse EMI effect)

Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.			
Title	FP4 DISP/MISC/HDT		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 7 of 56		



Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: FP4 GPIO/AZ/MISC/STRAPS

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

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RC115 place from UC1.AW1(SATA_ZVSS) =< 1000mil
RC117 place from UC1.AW2(SATA_ZVDDP)=<1000mil
2015/12/15

HDD
ODD

48MHz CRYSTAL

48M_X2_R — 0_0402_5% — 48M_X2
48M_X1 — 1M_0402_5%
CC41 6P_0402_50V8D
CC42 6P_0402_50V8D
YC2 48MHZ_8PF_X3S048000D81H-W
Part Number = SJ10000AF00

EC Clock
TPM Clock

dGPU
LAN
WLAN
Cardreader
PCIE to SATA

RC133/ CC79 Close to UC1 12/11

SOC to EC Level Shift

UC7 TXB0104PWR_TSSOP14
SA00001S200

BIOS Recovery

12/8 modify, Vendor recommend. Add 100K PD.

Close to UC1 IC

RPC4
100_0804_8P4R_5%

EC Pin47 (38) BIOS_SPI_CSOUT#

VCC: 0.8V~3.6V

UC9 74AUP1G32GW_TSSOP5

UC10 NL17SZ07DFT2G_SC70-5 Buffer

EC Pin56 (35,38) USB_BIOS_MISO

UC1E Stoney

USB Ports	USB 2.0 Signals	USB 3.0 Signals
Port 7	USB_HSD7P/N	USB_SS_3RXP/N USB_SS_3TXP/N
Port 6	USB_HSD6P/N	USB_SS_2RXP/N USB_SS_2TXP/N
Port 5	USB_HSD5P/N	USB_SS_1RXP/N[1] USB_SS_1TXP/N[1]
Port 4	USB_HSD4P/N	USB_SS_0RXP/N[1] USB_SS_0TXP/N[1]
Port 3	USB_HSD3P/N	N/A
Port 2	USB_HSD2P/N	N/A
Port 1	USB_HSD1P/N	N/A
Port 0	USB_HSD0P/N	N/A

Rear USB2 port 1
Rear USB2 port 2
Rear USB2 port 3
WLAN/BT combo
Touch Screen
CAMERA
Side USB3.0 port1
Side USB3.0 port2

USB3.0 Port0,Port1 only support on Type1,Type3 FP4

Side USB3.0 port1
Side USB3.0 port2

BIOS ROM

Close to SPI ROM

SPI ROM (8MByte/1.8V/Quad-IO)

UC8 W25Q64FWSSIQ_SO8
SA00006ZV10

Correct UC8 footprint 1222

SPI ROM SOCKET(co-lay)

CONN@ JROM1 ACES_91960-0084N_MX25L3206EM2I

* RC136 / CC47 Close to UC8 (SPI ROM)

Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: FP4 SATA/CLK/USB/SPI

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

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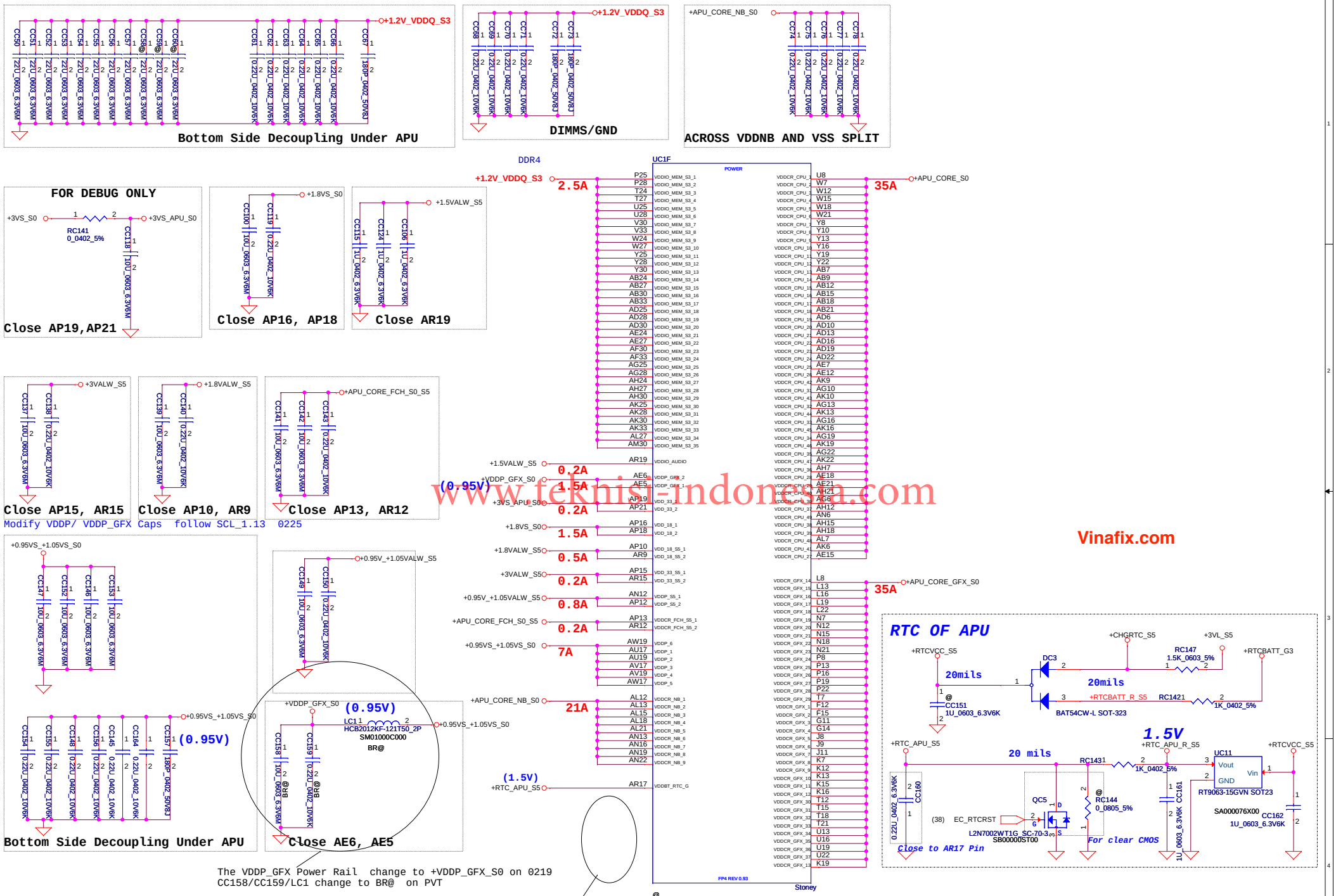
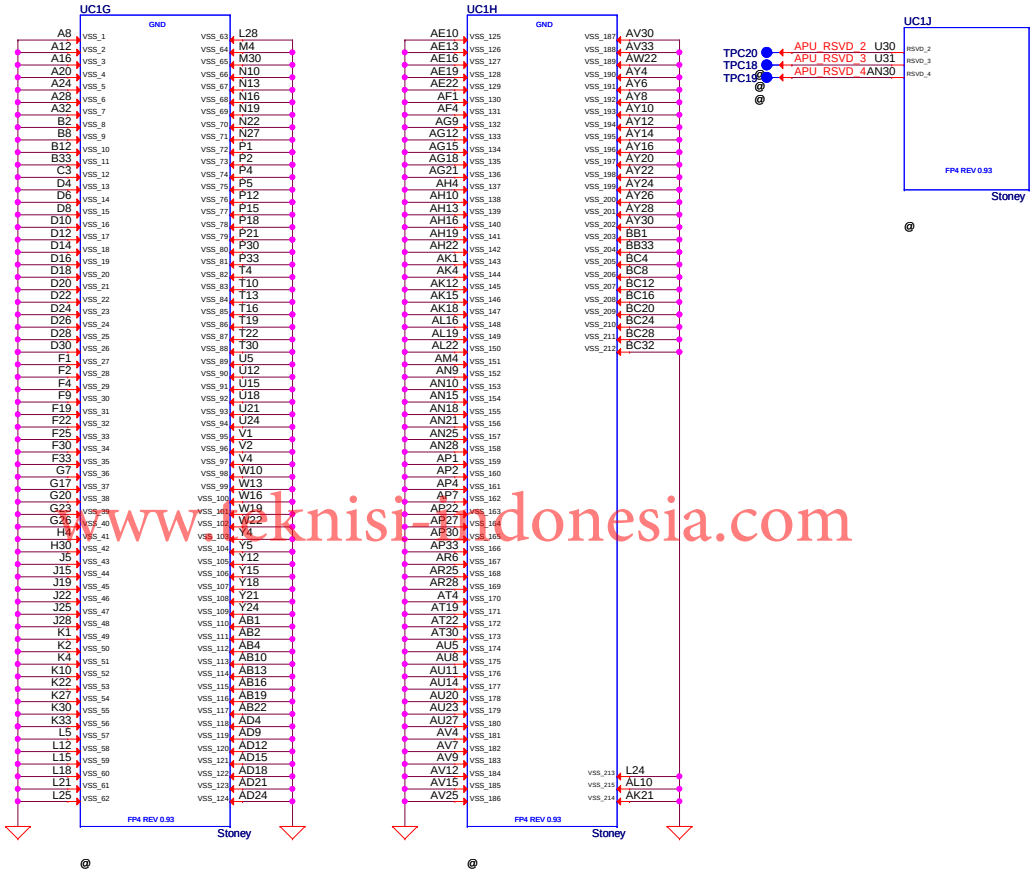


Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.			
Title	FP4 PWR		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 10 of 56		



Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: FP4 GND

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

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(8.0 mm) STD

Layout Note:
Place near JDIMM1

+1.2V_VDDQ_S3

CD34 0.1U_0402_25V6 @ | CD35 0.1U_0402_25V6 @ | CD36 0.1U_0402_25V6 @ | CD37 0.1U_0402_25V6 @ | CD39 0.1U_0402_25V6 @ | CD38 0.1U_0402_25V6 | CD9 0.1U_0402_25V6 | CD10 0.1U_0402_25V6 | CD11 0.1U_0402_25V6 | CD12 0.1U_0402_25V6 | CD13 0.1U_0402_25V6 | CD14 0.1U_0402_25V6 | CD15 180P_0402_50V8J

+1.2V_VDDQ_S3

CD17 100U_1206_6.3V6M

0.1U*12 (DNI x6)
180P*1
100uF*1
Follow reference board Gardenia

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

+0.6V_DDRA_VREFCA_S3

CD19 1nF*1 1000P_0402_50V7K

Layout Note:
Place near JDIMM1

+0.6VS_VTT_S0

CD22 4.7U_0603_6.3V6K | CD24 0.1U_0402_10V7K

4.7uF*1
0.1uF*1

Layout Note:
Place near JDIMM1

+2.5V_S3

CD25 0.1U_0402_25V6 | CD26 0.1U_0402_25V6 | CD27 180P_0402_50V8J

0.1uF*2
180F*1

+1.2V_VDDQ_S3

RD8 1K_0402_1%

+0.6V_DDRA_VREFCA_S3

RD9 1K_0402_1%

JDIMM1A STD

(5) DDRB_CLK0	137	CK0(T)	DQ0	8	DDRB_SDQ0
(5) DDRB_CLK0#	139	CK0#(C)	DQ1	7	DDRB_SDQ1
(5) DDRB_CLK1	138	CK1(T)	DQ2	20	DDRB_SDQ2
(5) DDRB_CLK1#	140	CK1#(C)	DQ3	21	DDRB_SDQ3
			DQ4	4	DDRB_SDQ4
(13,5) DDRB_CKE0	109	CKE0	DQ5	3	DDRB_SDQ5
(13,5) DDRB_CKE1	110	CKE1	DQ6	16	DDRB_SDQ6
			DQ7	17	DDRB_SDQ7
(5) DDRB_SCS0#	149	S0#	DQS0(T)	13	DDRB_SDQS0 (13,5)
(5) DDRB_SCS1#	157	S1#	DQS0#(C)	11	DDRB_SDQS0# (13,5)
	162	S2#/C0			DDRB_SDQ[8..15] (13,5)
	165	S3#/C1	DQ8	28	DDRB_SDQ8
			DQ9	29	DDRB_SDQ9
(5) DDRB_ODT0	155	ODT0	DQ10	41	DDRB_SDQ10
(5) DDRB_ODT1	161	ODT1	DQ11	42	DDRB_SDQ11
			DQ12	24	DDRB_SDQ12
(13,5) DDRB_BG0	115	BG0	DQ13	25	DDRB_SDQ13
(13,5) DDRB_BG1	113	BG1	DQ14	38	DDRB_SDQ14
(13,5) DDRB_SBS0#	150	BA0	DQ15	37	DDRB_SDQ15
(13,5) DDRB_SBS1#	145	BA1	DQS1(T)	34	DDRB_SDQS1 (13,5)
(13,5) DDRB_SMA[0..13]			DQS1#(C)	32	DDRB_SDQS1# (13,5)
DDRB_SMA0	144	A0			DDRB_SDQ[16..23] (13,5)
DDRB_SMA1	133	A1	DQ16	50	DDRB_SDQ16
DDRB_SMA2	132	A2	DQ17	49	DDRB_SDQ17
DDRB_SMA3	131	A3	DQ18	62	DDRB_SDQ18
DDRB_SMA4	128	A4	DQ19	63	DDRB_SDQ19
DDRB_SMA5	126	A5	DQ20	46	DDRB_SDQ20
DDRB_SMA6	127	A6	DQ21	45	DDRB_SDQ21
DDRB_SMA7	122	A7	DQ22	58	DDRB_SDQ22
DDRB_SMA8	125	A8	DQ23	59	DDRB_SDQ23
DDRB_SMA9	121	A9	DQS2(T)	55	DDRB_SDQS2 (13,5)
DDRB_SMA10	146	A10_AP	DQS2#(C)	53	DDRB_SDQS2# (13,5)
DDRB_SMA11	120	A11			DDRB_SDQ[24..31] (13,5)
DDRB_SMA12	119	A12	DQ24	70	DDRB_SDQ24
DDRB_SMA13	158	A13	DQ25	71	DDRB_SDQ25
(13,5) DDRB_SWE#	151	A14_WE#	DQ26	83	DDRB_SDQ26
(13,5) DDRB_SCAS#	156	A15_CAS#	DQ27	84	DDRB_SDQ27
(13,5) DDRB_SRAS#	152	A16_RAS#	DQ28	66	DDRB_SDQ28
			DQ29	67	DDRB_SDQ29
(13,5) DDRB_ACT#	114	ACT#	DQ30	79	DDRB_SDQ30
			DQ31	80	DDRB_SDQ31
	143	PARITY	DQS3(T)	76	DDRB_SDQS3 (13,5)
DIM1_ALERT#	116	ALERT#	DQS3#(C)	74	DDRB_SDQS3# (13,5)
MEM_MB_EVENT#	134	EVENT#			DDRB_SDQ[32..39] (13,5)
(13,5) MEM_MB_RST#	108	RESET#	DQ32	174	DDRB_SDQ32
			DQ33	173	DDRB_SDQ33
(13,22,8) APU_SDATA0	254	SDA	DQ34	187	DDRB_SDQ34
(13,22,8) APU_SCLK0	253	SCL	DQ35	186	DDRB_SDQ35
	166	SA2	DQ36	170	DDRB_SDQ36
SA1_DIM1	260	SA1	DQ37	169	DDRB_SDQ37
SA0_DIM1	256	SA0	DQ38	183	DDRB_SDQ38
			DQ39	182	DDRB_SDQ39
			DQS4(T)	179	DDRB_SDQS4 (13,5)
			DQS4#(C)	177	DDRB_SDQS4# (13,5)
	92	CB0_NC			DDRB_SDQ[40..47] (13,5)
	91	CB1_NC	DQ40	195	DDRB_SDQ40
	101	CB2_NC	DQ41	194	DDRB_SDQ41
	105	CB3_NC	DQ42	207	DDRB_SDQ42
	88	CB4_NC	DQ43	208	DDRB_SDQ43
	87	CB5_NC	DQ44	191	DDRB_SDQ44
	100	CB6_NC	DQ45	190	DDRB_SDQ45
	104	CB7_NC	DQ46	203	DDRB_SDQ46
	97	DQS8(T)	DQ47	204	DDRB_SDQ47
	95	DQS8#(C)	DQS5(T)	200	DDRB_SDQS5 (13,5)
			DQS5#(C)	198	DDRB_SDQS5# (13,5)
(13,5) DDRB_SDM[7..0]					DDRB_SDQ[48..55] (13,5)
DDRB_SDM0	12	DM0#/DBI0#	DQ48	216	DDRB_SDQ48
DDRB_SDM1	33	DM1#/DBI1#	DQ49	215	DDRB_SDQ49
DDRB_SDM2	54	DM2#/DBI2#	DQ50	228	DDRB_SDQ50
DDRB_SDM3	75	DM3#/DBI3#	DQ51	229	DDRB_SDQ51
DDRB_SDM4	178	DM4#/DBI4#	DQ52	211	DDRB_SDQ52
DDRB_SDM5	199	DM5#/DBI5#	DQ53	212	DDRB_SDQ53
DDRB_SDM6	220	DM6#/DBI6#	DQ54	224	DDRB_SDQ54
DDRB_SDM7	241	DM7#/DBI7#	DQ55	225	DDRB_SDQ55
	96	DM8#/DBI8#	DQS6(T)	221	DDRB_SDQS6 (13,5)
			DQS6#(C)	219	DDRB_SDQS6# (13,5)
					DDRB_SDQ[56..63] (13,5)
			DQ56	237	DDRB_SDQ56
			DQ57	236	DDRB_SDQ57
			DQ58	249	DDRB_SDQ58
			DQ59	250	DDRB_SDQ59
			DQ60	232	DDRB_SDQ60
			DQ61	233	DDRB_SDQ61
			DQ62	245	DDRB_SDQ62
			DQ63	246	DDRB_SDQ63
			DQS7(T)	242	DDRB_SDQS7 (13,5)
			DQS7#(C)	240	DDRB_SDQS7# (13,5)

CONN@
LOTES_ADDR0069-P007A
SP011412263

+1.2V_VDDQ_S3 — RD7 1 @ 2 0_0402_5% D1_PAR
RD10 2 1 1K_0402_1% DIM1_ALERT#

+1.2V_VDDQ_S3 — RD11 2 1 MEM_MB_EVENT#
1K_0402_1%

+3VS_S0 +3VS_S0
RD20 RD21 @ 4.7K_0402_5%
4.7K_0402_5% SA1_DIM1 SA0_DIM1
RD22 RD23 4.7K_0402_5%
4.7K_0402_5% @ ADDRESS: A2

+0.6V_DDRA_VREFCA_S3 — +3VS_S0 — RD28 2 1 VDDSPD1 0_0603_5%
CD21 1U_0402_6.3V6K | CD32 0.1U_0402_25V6

+1.2V_VDDQ_S3 — +0.6VS_VTT_S0 — +2.5V_S3 — CD18 4.7U_0402_10V6

JDIMM1B STD

111	VDD1	VDD11	141
112	VDD2	VDD12	142
117	VDD3	VDD13	147
118	VDD4	VDD14	148
123	VDD5	VDD15	153
124	VDD6	VDD16	154
129	VDD7	VDD17	159
130	VDD8	VDD18	160
135	VDD9	VDD19	163
136	VDD10		
	VDDSPD	VTT	258
255		VPP1	257
164	VREFCA	VPP2	259
1	VSS	VSS	99
2	VSS	VSS	102
5	VSS	VSS	103
6	VSS	VSS	106
9	VSS	VSS	107
10	VSS	VSS	167
14	VSS	VSS	168
15	VSS	VSS	171
18	VSS	VSS	172
19	VSS	VSS	175
22	VSS	VSS	176
23	VSS	VSS	180
26	VSS	VSS	181
27	VSS	VSS	184
30	VSS	VSS	185
31	VSS	VSS	188
35	VSS	VSS	189
36	VSS	VSS	192
39	VSS	VSS	193
40	VSS	VSS	196
43	VSS	VSS	197
44	VSS	VSS	201
47	VSS	VSS	202
48	VSS	VSS	205
51	VSS	VSS	206
52	VSS	VSS	209
56	VSS	VSS	210
57	VSS	VSS	213
60	VSS	VSS	214
61	VSS	VSS	217
64	VSS	VSS	218
65	VSS	VSS	222
68	VSS	VSS	223
69	VSS	VSS	226
72	VSS	VSS	227
73	VSS	VSS	230
77	VSS	VSS	231
78	VSS	VSS	234
81	VSS	VSS	235
82	VSS	VSS	238
85	VSS	VSS	239
86	VSS	VSS	243
89	VSS	VSS	244
90	VSS	VSS	247
93	VSS	VSS	248
94	VSS	VSS	251
98	VSS	VSS	252
262	GND	GND	261

CONN@
LOTES_ADDR0069-P007A
SP011412263

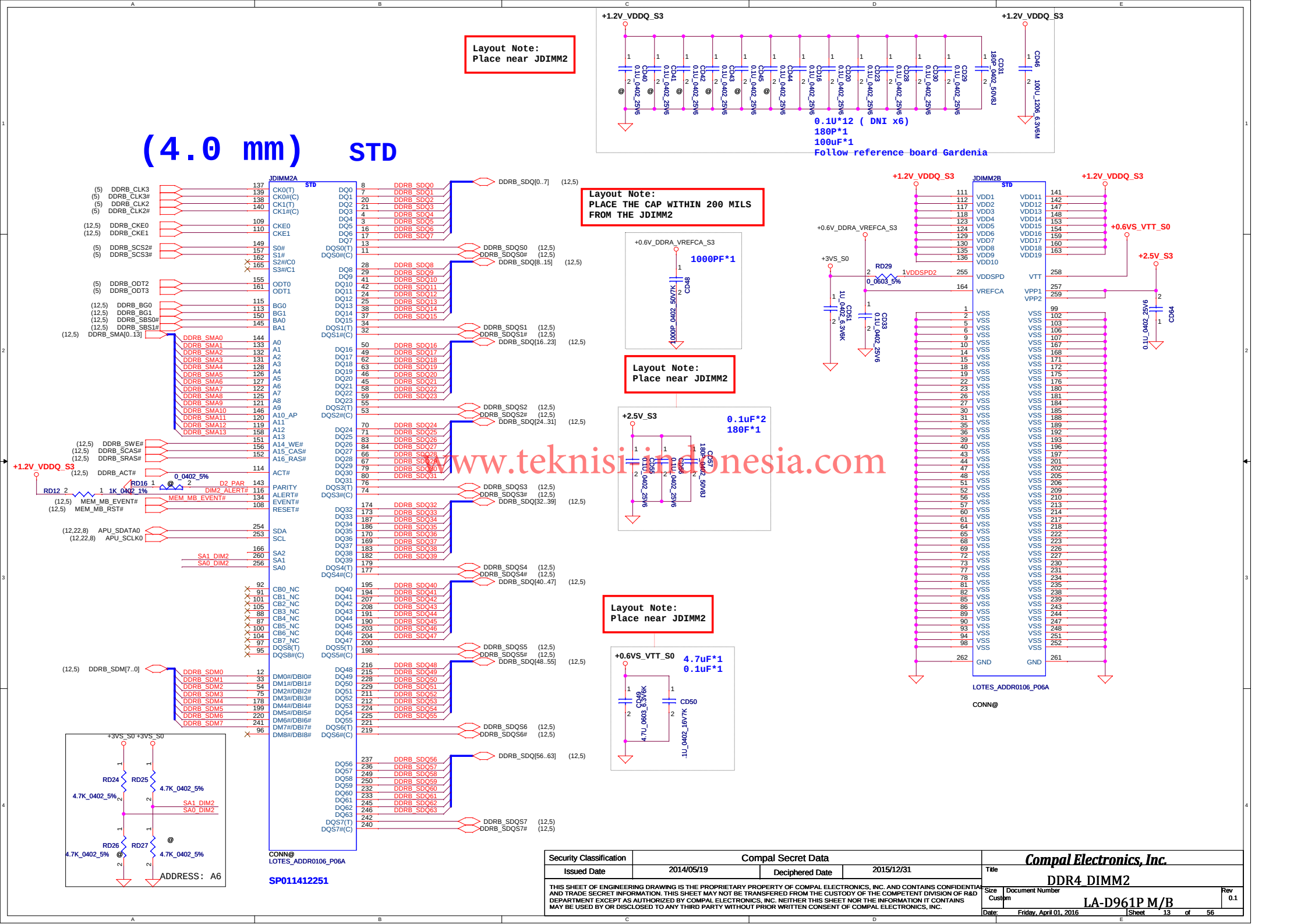
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DDR4_DIMM1

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

Date: Friday, April 01, 2016 Sheet 12 of 56



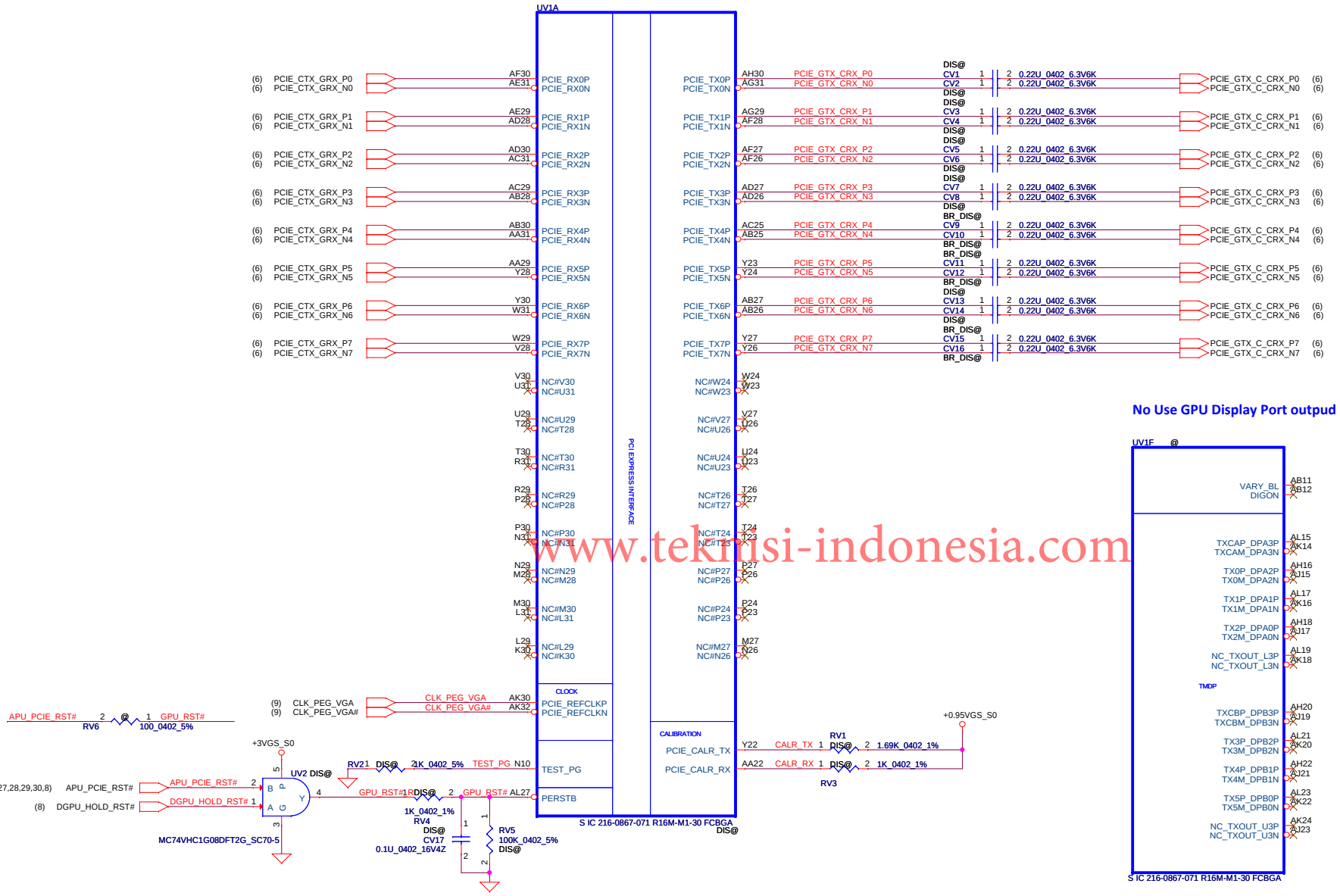
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DDR4 DIMM2

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 13 of 56



Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R16M-M1-30(1/5) PCIE/DP

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

Date: Friday, April 01, 2016 Sheet 14 of 56

Meso/M16M-R16M-M2-50

GPIO_11, 12, and 13 are added back.

The following balls cease to work as GPIOs or designated functional pins, and become **VDDC**:

- GPIO_1
- GPIO_2
- GPIO_14_HPD2
- GPIO_18_HPD3

The following ball ceases to work as a GPIO or designated functional pin, and becomes **NC**:

- GPIO_7_BLON

"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36.

The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:

- VARY_BL (AB11)
- DIGON (AB12)
- GENERCA (AB13)
- GENERICC (W9)
- DDC2CLK (AC11)
- DDC2DATA (AC13)
- HPD1 (AC14)
- GPIO_1 (U10)
- GPIO_2 (T10)
- GPIO_18 (W10)
- GPIO_14_HPD2 (Y9)

Exo/R16M-M1-30

The following balls cease to work as GPIOs or designated functional pins, and become **NC**:

- GPIO_1
- GPIO_2
- GPIO_7_BLON
- GPIO_11
- GPIO_12
- GPIO_13
- GPIO_14_HPD2
- GPIO_18_HPD3

"Jet"/"Sun" has a total of 25 VDDC balls.

The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".

Add GPU_VR_HOT# on GPIO5 1228

When PS_2 bit 3=0, PS_0 bits [3:1] define the size of the Primary Memory Aperture as per table opposite

Setting Memory Aperture Size

PS_0[3] romidcfg_2	PS_0[2] romidcfg_1	PS_0[1] romidcfg_0	Memory Aperture Size
0	0	0	128 MB
0	0	1	256 MB
0	1	0	64 MB
0	1	1	Reserved
1	0	0	512 MB-Not Supported
1	0	1	1 GB-Not Supported
1	1	0	2 GB-Not Supported
1	1	1	4 GB-Not Supported

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 09/25

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

MLPS MEMORY ID Setting:

Board_Config[2:0]	Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID [2:0]					
0 000	Hynix gDDR5	128Mx32 2PCS	1GB	H5GC4H24AJR-T2C	SA000085V00
1 001	Micron gDDR5	128Mx32 2PCS	1GB	EDW4032BABG-60-F-R	SA00007UZ00
2 010	Micron gDDR5	256Mx32 2PCS	2GB	MT51J256M32HF-60:A	SA000096K00
3 011	Samsung gDDR5	256Mx32 2PCS	2GB	K4G80325FB-HC03	SA000094R00

ZZZ4 — Hynix 1G — H1G@ — Part Number = X7668038L01
ZZZ5 — Micron 1G — M1G@ — Part Number = X7668038L02
ZZZ6 — Micron 2G — M2G@ — Part Number = X7668038L03
ZZZ7 — Samsung 2G — S2G@ — Part Number = X7668038L04

X7668038L01 : RV20 = NC , RV22 = 4.75K
X7668038L02 : RV20 = 8.45K , RV22 = 2K
X7668038L03 : RV20 = 4.53K , RV22 = 2K
X7668038L04 : RV20 = 6.98K , RV22 = 4.99K

RV7/RV8 modify to 4.7K 0303

CV22/CV23 change to 8.2P 02/21

ZZZ12 — 76_1G@ — 76_1G@ Part Number = X7668038L01
ZZZ13 — 76_2G@ — 76_2G@ Part Number = X7668038L03

Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

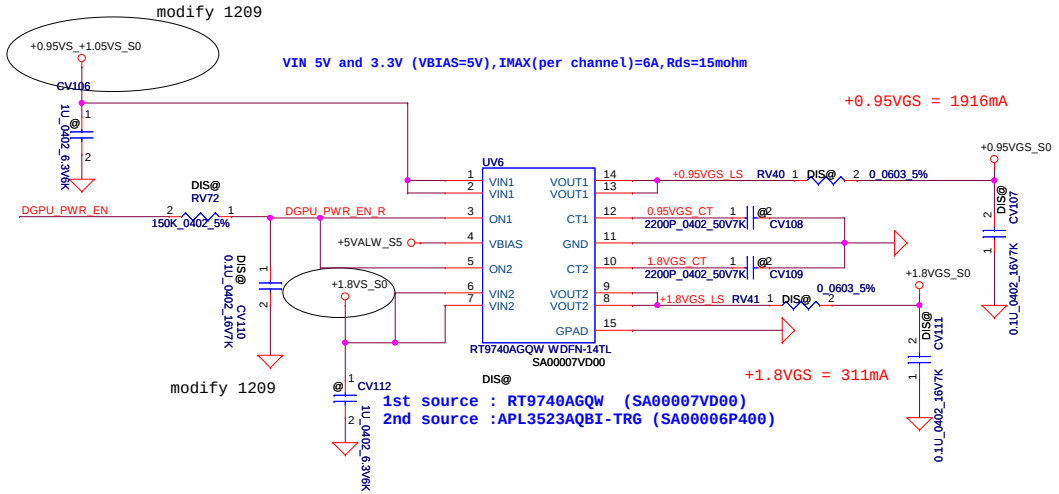
Compal Electronics, Inc.

Title: R16M-M1-30(2/5)_MSIC

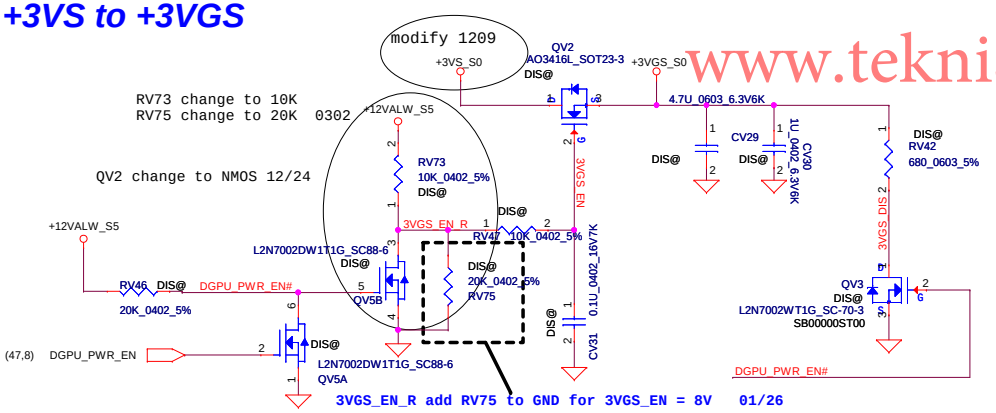
Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 15 of 56

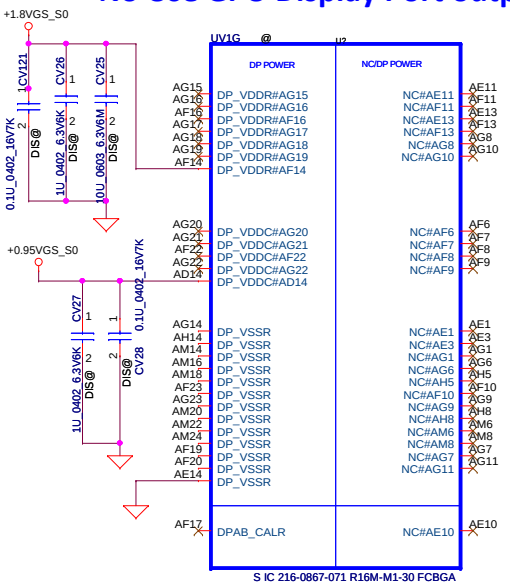
+1.8VS TO +1.8VGS
+0.95VS TO +0.95VGS
Load switch

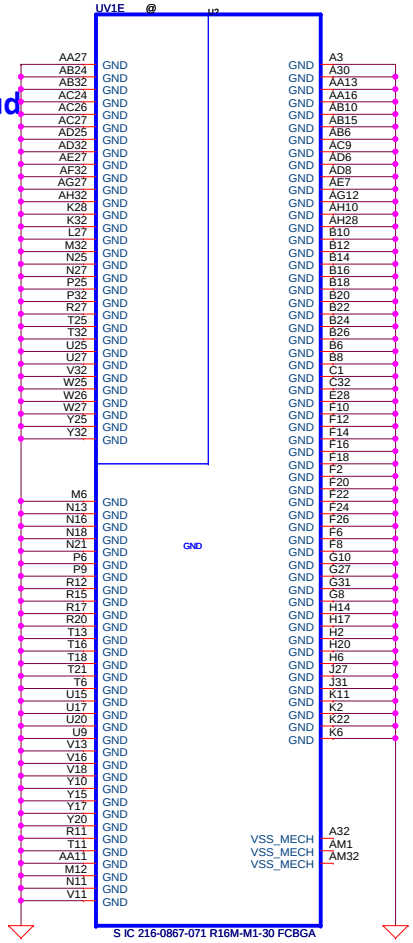


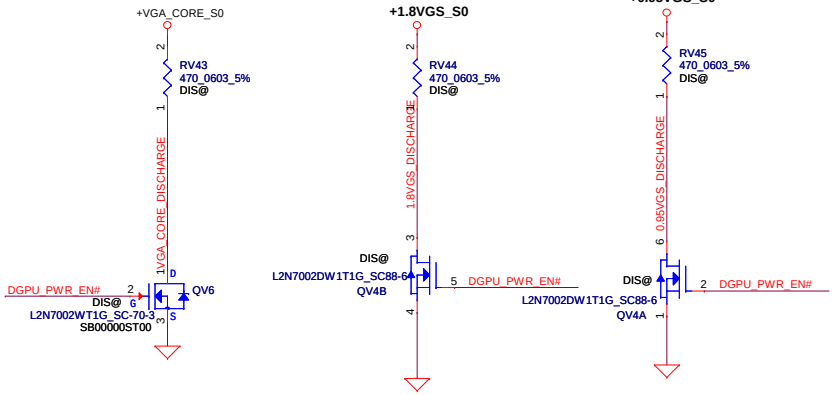
+3VS to +3VGS



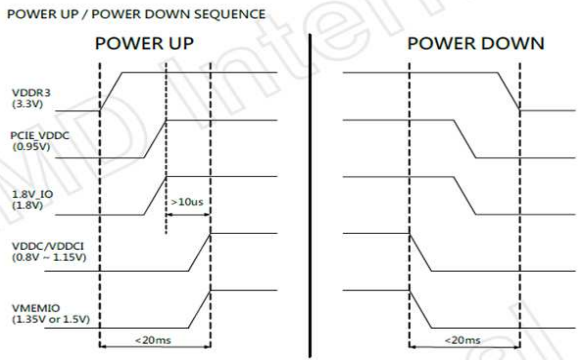
No Use GPU Display Port outpud







DGPU Power Sequence

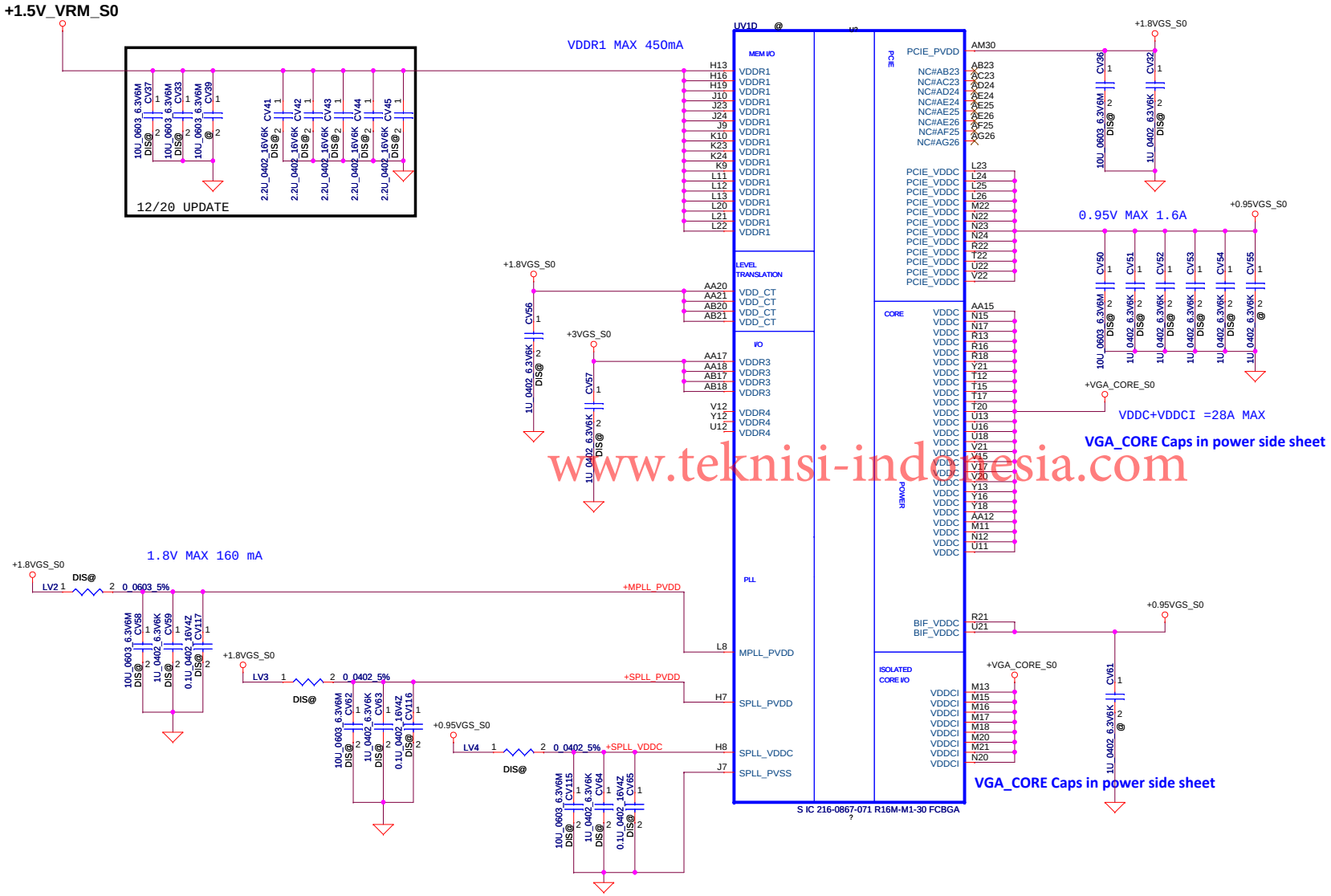


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

1.the 3.3-V rail ramp up first.
2.the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up

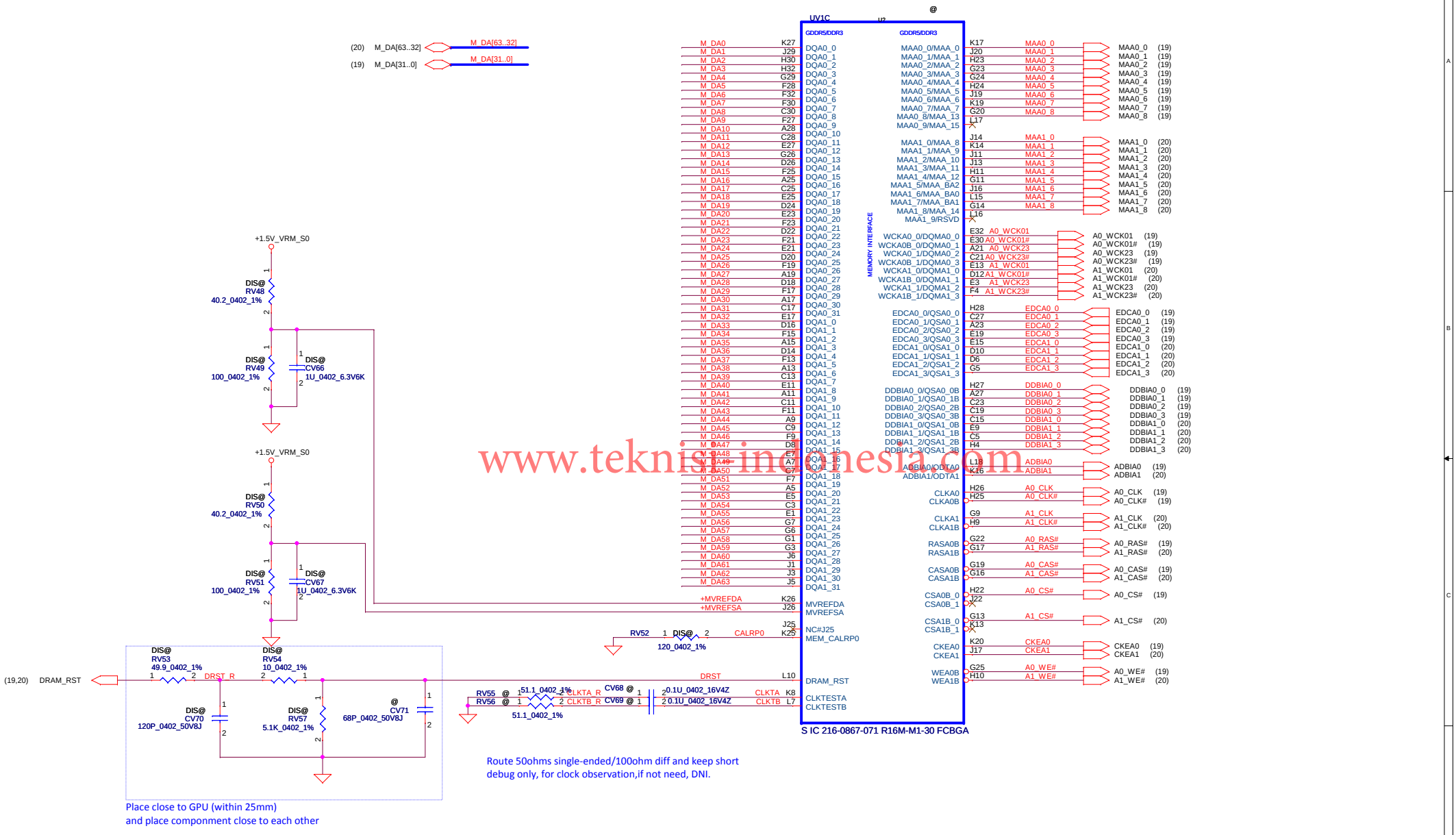
Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.			
Title	R16M-M1-30 (3/5) PWR/GND		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 16 of 56		



Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.			
Title	R16M-M1-30(4/5) PWR		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 17 of 56		



Security Classification	Compal Secret Data		
Issued Date	2015/10/01	Deciphered Date	2016/10/01

Compal Electronics, Inc.

Title: R16M-M1-30(5/5) MEM

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

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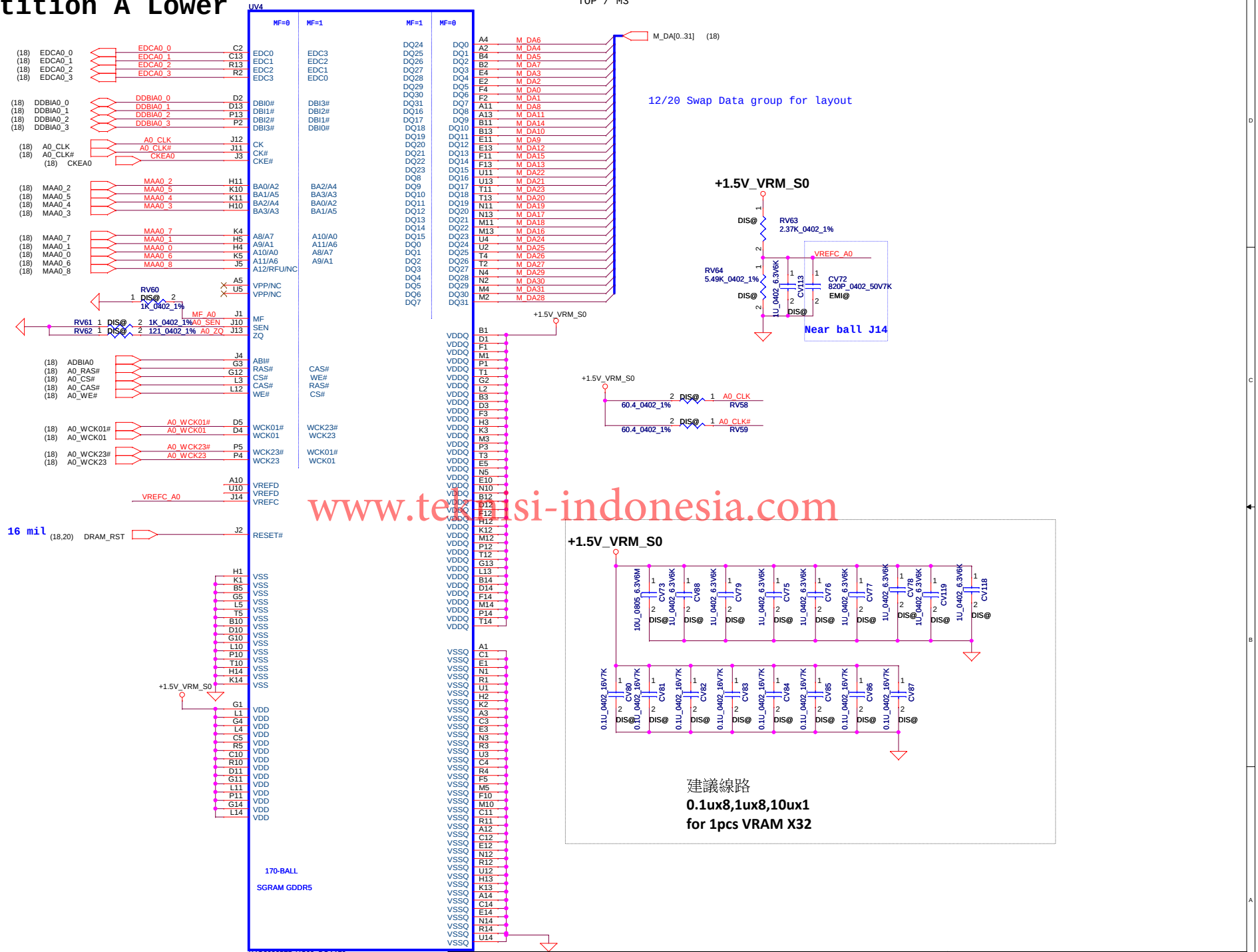
Memory Partition A Lower -32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

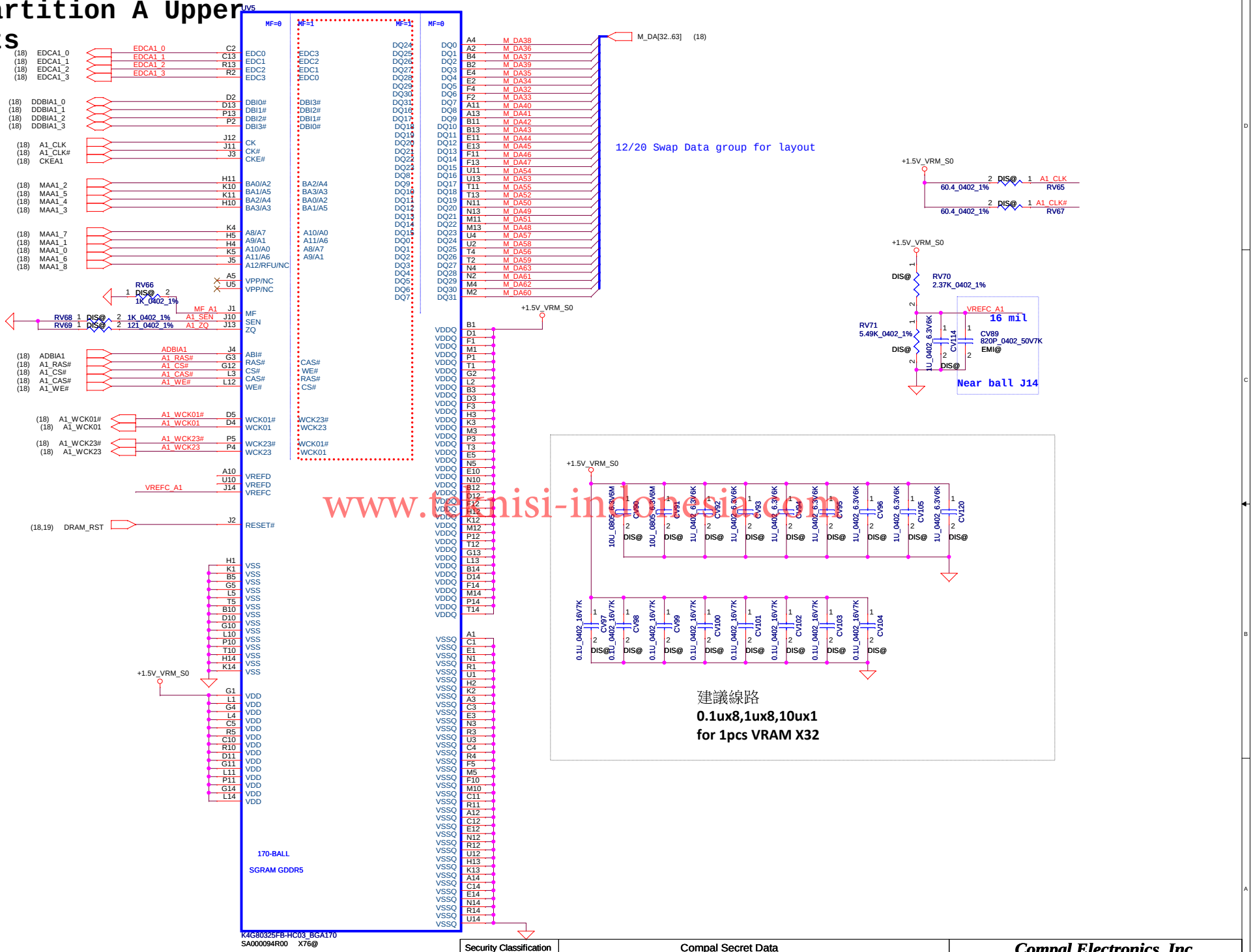
Compal Electronics, Inc.

Title: GDDR5 VRAM A Lower

Size | Document Number: LA-D961P M/B | Rev: 1.0

Date: Friday, April 01, 2016 | Sheet 19 of 56

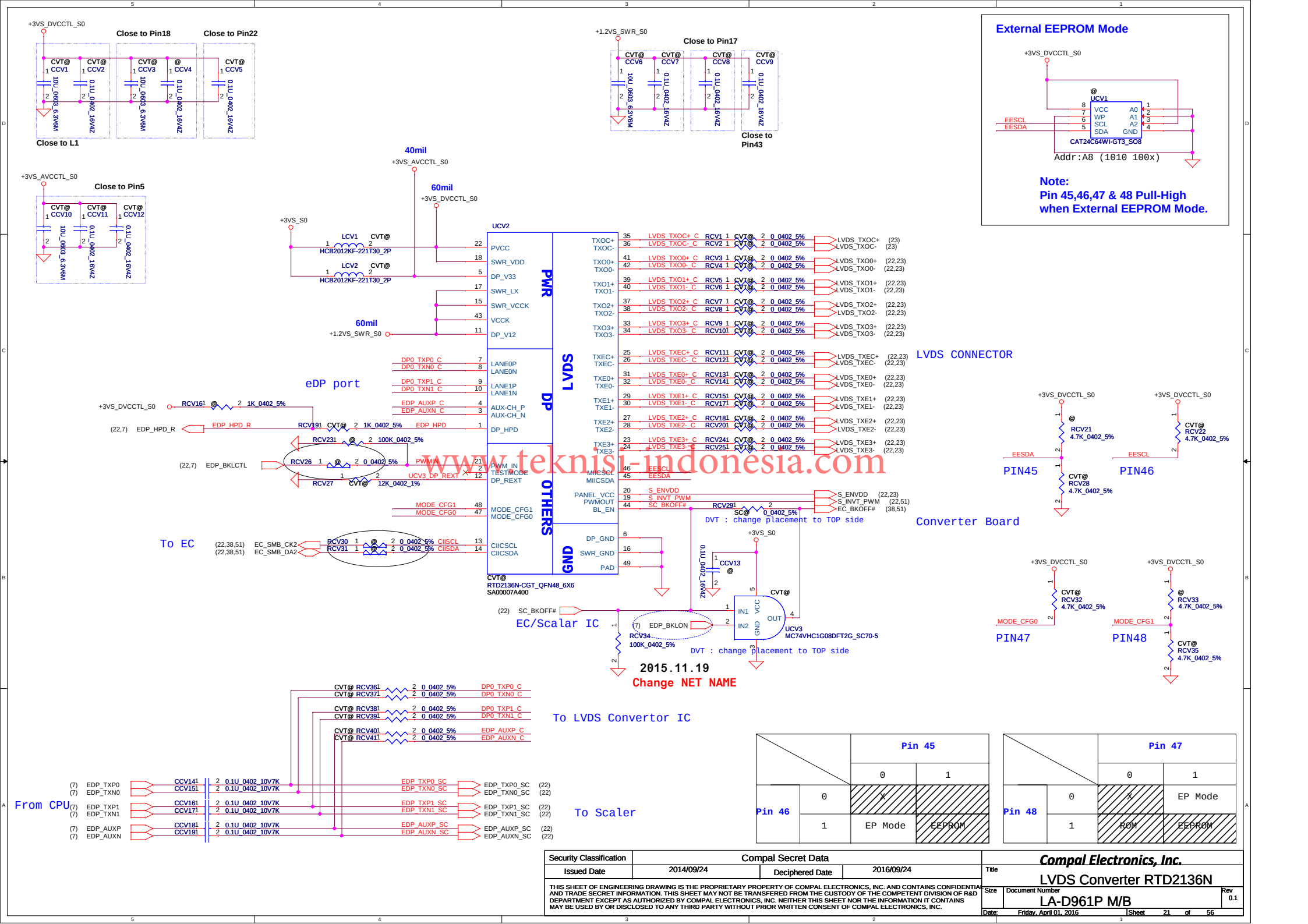
Memory Partition A Upper - 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/03/01	Deciphered Date	2014/03/01

Compal Electronics, Inc.

Title	GDDR5_A Upper		
Size	Document Number		Rev
	LA-D961P M/B		1.0
Date: Friday, April 01, 2016	Sheet 20 of 56		



	Pin 45	
	0	1
Pin 46 0	X	
Pin 46 1	EP Mode	EEPROM

	Pin 47	
	0	1
Pin 48 0	X	EP Mode
Pin 48 1	ROM	EEPROM

Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title	LVDS Converter RTD2136N		
Size	Document Number	LA-D961P M/B	Rev 0.1
Date: Friday, April 01, 2016	Sheet 21 of 56		

+3V_SCA _R use Power switch USC5 Date 01/29

+3V3_DSW

+3V_SCA_R

RSC51 10K_0402_5%

USC5 VOUT VIN GND EN# OCB

(38) SCALER_ON#

CSC1 0.1U_0402_16V4Z

RT9742DGJ5_SOT23-5

CSC5 1U_0402_6.3V6K

SC@

Main: SA00009R300 RT9742DGJ5 TSOT23 5P

Second: SA00009RN00 UP7549UMA5-20 SOT23 5P

+3VALW TO +1.1VALW

+1.1V_SCA_S5

284mA

LSC1 TAI_HCB2012KF-121T50

+1.1V_SCA_L

RSC7 39.2_0402_1%

CSC6 10U_0603_6.3V6M

RSC15 100_0402_1%

USC1 RT9059GSP_SO8

NC VOUT ADJ GND VDD VIN EN PGOOD

CSC4 1U_0402_6.3V6K

CSC7 4.7U_0603_10V6K

+1.1VALW=VFB(1+RSC7/RSC15)

,VFB=0.8V

main source : RT9059GSP

second srouce: APL5933CKAI

SPI 4M Change to 4M 0106

FOR Scalar Firmware Code

+3V_SCA_S5

SC@ RSC2 4.7K_0402_5%

RSC3 4.7K_0402_5%

SC@RSC9 22_0402_5%

SC@RSC8 22_0402_5%

SC@RSC10 0_0402_5%

SCA_SPI_CS#

SCA_SPI_SDO

SCA_SPI_WP#

USC2 SC@ W25X40CLSNIG_SO8 SA00006LS00

/CS VCC /HOLD /WP CLK GND DIO_IO0 DIO_IO1

SCA_SPI_HOLD#

SCA_SPI_CK_R

SCA_SPI_SDI_R

SCA_SPI_SDI

SC@ RSC11 22_0402_5%

RSC13 4.7K_0402_5%

RSC14 4.7K_0402_5%

SC@ RSC4 10K_0402_5%

SC@CSC2 0.1U_0402_16V4Z

@CSC3 0.1U_0402_16V4Z

SCA_XO_C SCA_XO

RSC41 0_0402_5% SCA_XI

YSC1 SC@ OSC NC NC OSC

14.31818MHZ_12PF_X3G01431ADC1H

RSC46 SC@ 1M_0402_5%

SC@ CSC24 12P_0402_50V8J

SC@ CSC25 12P_0402_50V8J

Add Project_ID select :

Pin63 change to PROJECT_ID3

Pin60 change to PROJECT_ID1

Pin61 change to PROJECT_ID2

+3V_SCA_S5

RSC43 10K_0402_5% SC_C4@

RSC53 10K_0402_5%

RSC55 10K_0402_5%

PROJECT_ID1 PROJECT_ID2 PROJECT_ID3

RSC47 10K_0402_5%

RSC54 10K_0402_5%

RSC60 10K_0402_5%

SC_C5@

+3V_SCA_R +3V_SCA_S5

SC@ LSC2 TAI_HCB2012KF-121T50

158mA

SC@ CSC9 10U_0603_6.3V6M

SC@ CSC10 1U_0402_6.3V6K

SC@ CSC11 1U_0402_6.3V6K

SC@ CSC12 0.1U_0402_16V4Z

SC@ CSC13 1U_0402_6.3V6K

SC@ CSC14 0.1U_0402_16V4Z

SCA_SPI_CK_R @EMI@ RSC59 0_0402_5% SCA_SPI_CK_R_1 CSC27 @EMI@ 10P_0402_50V8J

For EMI / RSC59 , CSC27 Close to USC2 1210

USC4

PVCC33 PVCC33 PVCC33 PVCC33 PVCC33

25 40 76 89 94 108

eDP

(21) EDP_TXP0_SC EDP_TXP0_SC 1

(21) EDP_TXN0_SC EDP_TXN0_SC 2

(21) EDP_TXP1_SC EDP_TXP1_SC 4

(21) EDP_TXN1_SC EDP_TXN1_SC 5

RX2P_0/LANE0P_0/MHLP_0 6

RX2N_0/LANE0N_0/MHLN_0 7

GDI_GND 8

RX1P_0/LANE1P_0 9

RX1N_0/LANE1N_0 10

RX0P_0/LANE2P_0

RX0N_0/LANE2N_0

RXCP_0/LANE3P_0

RXCN_0/LANE3N_0

MHL_V33

RX2P_1/LANE0P_1/MHLP_1

RX2N_1/LANE0N_1/MHLN_1

GDI_GND

RX1P_1/LANE1P_1

RX1N_1/LANE1N_1

RX0P_1/LANE2P_1

RX0N_1/LANE2N_1

RXCP_1/LANE3P_1

RXCN_1/LANE3N_1

GDI_V11

HDMI-Port0

HDMI-Port1

+3V_SCA_S5 0.67mA

+1.1V_SCA_S5 @ 0_0402_5% RSC21

CSC17 0.1U_0402_16V4Z SC@

HDMI IN

(24) HDMI_IN_D2+ HDMI_IN_D2+ 11

(24) HDMI_IN_D2- HDMI_IN_D2- 12

HDMI_IN_D1+ 14

(24) HDMI_IN_D1+

(24) HDMI_IN_D1-

(24) HDMI_IN_D0+

(24) HDMI_IN_D0-

(24) HDMI_IN_CK+

(24) HDMI_IN_CK-

HDMI_IN_D1- 15

HDMI_IN_D0+ 16

HDMI_IN_D0- 17

HDMI_IN_CK+ 18

HDMI_IN_CK- 19

+1.1V_SCA_ADC 20

CSC18 CSC19 SC@ 0.1U_0402_16V4Z SC@

10U_0603_6.3V6M

EDP_HPD_R Pull-low 100K to GND close APU 1218

(21,7) EDP_HPD_R EDP_HPD_R 21

(24) HDMI_IN_HPD HDMI_IN_HPD 22

CBUS0/GPIO 23

CBUS1/GPIO 24

NC 25

NC 26

NC 27

NC 28

NC 29

NC 30

NC 31

NC 32

Add RPSC1 for Panel ID pull-high 01/26

+3V3_DSW

RPSC1

PANEL_ID3 1 8

PANEL_ID2 2 7

PANEL_ID1 3 6

4 5

10K_0804_8P4R_5%

Add Panel_ID4 on Pin34 02/16

(38) PANEL_ID4 SC@ PANEL_ID3 34

(38,51) PANEL_ID3 PANEL_ID3 35

(38) SC_MODE3 SC_MODE3 36

(38,51) PANEL_ID1 PANEL_ID1 37

(38,51) PANEL_ID2 PANEL_ID2 38

(24) EDID_WP EDID_WP 39

GPIO/PWM0/I2S_MCK/CLKO

GPIO/PWM1/I2S_SCK/IRQB

GPIO/PWM2/I2S_WS

GPIO/PWM3/IICSCL0/RXD/I2S_SD0/SPDIF0

GPIO/PWM4/ IICSDA0/TXD/I2S_SD1/SPDIF1

GPIO/PWM5/I2S_SD2/SPDIF2

Add HDMI_CABLE_DET# on Pin44 01/26

Add SCA_FW_FLASH on Pin43 02/16

(8) SCA_FW_FLASH RSC52 0_0402_5% CABLE_DET# 44

(24,38) HDMI_CABLE_DET#

NC 41

A-ADC0/GPIO 42

A-ADC1/GPIO/MUX_DDCSCLVGA 43

A-ADC2/GPIO/MUX_DDCSDAVGA 44

A-ADC3/GPIO 45

GPIO/PWM1/PWM5 46

+3V_SCA_S5 RSC421 SC@ 4.7K_0402_5% SC_EESCL 47

RSC441 SC@ 4.7K_0402_5% SC_EESDA 48

SC_DDCSCL 49

SC_DDCSDA 50

GPIO/IICSCL1/IICSCL_AUX

GPIO/IICSDA1/IICSDA_AUX

GPIO/DDCSCLVGA/RXD

GPIO/DDCSDAVGA/TXD

VCCK11 51

+1.1V_SCA_S5 52

SC_WP_PRO 53

GPIO/PWM0/I2S_SD3/SPDIF3

GPIO/PWM3/PWM4

AUDIO_DAC_GND

SC@ CSC22 0.1U_0402_16V4Z

GPIO/PWM0/I2S_MCK/LINE_INL

GPIO/I2S_SCK/LINE_INR

GPIO/I2S_WS/AUDIO_REF

SC@ CSC26 1U_0402_6.3V6K SC_57

GPIO/I2S_SD0/SPDIF0/SOUTL

(33) S_LINE_OUTL

(33) S_LINE_OUTR

GPIO/I2S_SD1/SPDIF1/SOUTR

PROJECT_ID1 60

PROJECT_ID2 61

GPIO/IICSCL2//RXD/I2S_SD2/SPDIF2/HOUTL

GPIO/IICSDA2/TXD/I2S_SD3/SPDIF3/HOUTR

remove HP-OUT 12/09

+3V_SCA_S5 +3V_SCA_S5

RSC64 2.2K_0402_5% SC@

RSC65 2.2K_0402_5% SC@

SC@ QSC3B

SC_DDCSCL

SC_DDCSDA

L2N7002DW1T1G_SC88-6

QSC3A

EC_SMB_CK2 (21,38,51)

SMBus

EC_SMB_DA2 (21,38,51)

SB00000PV00 L2N7002DW1T1G_SC88-6 SC@

QSC3 Change to SB00000PV00 0220

PGND PGND PGND

33 75 90 95

SA00009DL00

S IC RTD2506S-CG LQFP 128P DISPLAY CTRL SC@

AUDIO_DAC_V33 62

GPIO/PWM0/PMW3/INT1/T2/DVI_CTRL2/IHS 63

GPIO/PWM2/INT0/DVI_CTRL1/IENA/CLKO 64

GPIO 65

GPIO 66

GPIO/TXO3+_8b_10b 67

GPIO/TXO3-_8b_10b 68

GPIO/TXO2+_8b_10b 69

GPIO/TXO2-_8b_10b 70

GPIO/TXO1+_8b_10b 71

GPIO/TXO1-_8b_10b 72

GPIO/TXO0+_8b_10b 73

GPIO/TXO0-_8b_10b 74

PROJECT_ID3

S_ENVDD

CSC15 SC@ 0.1U_0402_16V4Z

+3V_SCA_S5

S_ENVDD (21,23)

LVDS_TXE3+_S RSC291 SC@ 2 0_0402_5% LVDS_TXE3+ (21,23)

LVDS_TXE3-_S RSC301 SC@ 2 0_0402_5% LVDS_TXE3- (21,23)

LVDS_TXE2+_S RSC331 SC@ 2 0_0402_5% LVDS_TXE2+ (21,23)

LVDS_TXE2-_S RSC341 SC@ 2 0_0402_5% LVDS_TXE2- (21,23)

LVDS_TXE1+_S RSC351 SC@ 2 0_0402_5% LVDS_TXE1+ (21,23)

LVDS_TXE1-_S RSC361 SC@ 2 0_0402_5% LVDS_TXE1- (21,23)

LVDS_TXE0+_S RSC371 SC@ 2 0_0402_5% LVDS_TXE0+ (21,23)

LVDS_TXE0-_S RSC381 SC@ 2 0_0402_5% LVDS_TXE0- (21,23)

LVDS

Swap LVDS ODD & EVEN 12/24

GPIO 77

GPIO 78

TXE3+_8b_10b 79

TXE3-_8b_10b 80

TXEC+_8b_10b 81

TXEC-_8b_10b 82

TXE2+_8b_10b 83

TXE2-_8b_10b 84

TXE1+_8b_10b 85

TXE1-_8b_10b 86

TXE0+_8b_10b 87

TXE0-_8b_10b 88

LVDS_TXO3+_S RSC161 SC@ 2 0_0402_5% LVDS_TXO3+ (21,23)

LVDS_TXO3-_S RSC221 SC@ 2 0_0402_5% LVDS_TXO3- (21,23)

LVDS_TXEC+_S RSC311 SC@ 2 0_0402_5% LVDS_TXEC+ (21,23)

LVDS_TXEC-_S RSC321 SC@ 2 0_0402_5% LVDS_TXEC- (21,23)

LVDS_TXO2+_S RSC181 SC@ 2 0_0402_5% LVDS_TXO2+ (21,23)

LVDS_TXO2-_S RSC231 SC@ 2 0_0402_5% LVDS_TXO2- (21,23)

LVDS_TXO1+_S RSC191 SC@ 2 0_0402_5% LVDS_TXO1+ (21,23)

LVDS_TXO1-_S RSC201 SC@ 2 0_0402_5% LVDS_TXO1- (21,23)

LVDS_TXO0+_S RSC241 SC@ 2 0_0402_5% LVDS_TXO0+ (21,23)

LVDS_TXO0-_S RSC261 SC@ 2 0_0402_5% LVDS_TXO0- (21,23)

NC 91

NC 92

VCCK11 93

+1.1V_SCA_S5 CSC20 SC@ 0.1U_0402_16V4Z

+3V_SCA_S5 10K_0402_5% RSC49 S_INVT_PWM

GPIO(Flash WP)/INT0 96

GPIO/INT1/IVS 97

GPIO/T0 98

GPIO/PWM2/PMW3/T1 99

GPIO/PWM_IN/AUX_D2/DCLK/T2EX 100

GPIO/PWM4/PWM_OUT/AUX_D1 101

NC 102

SPI_CLK/SDIO 103

SPI_SI/MCU_SCLK 104

SPI_SO/SCSB 105

SPI_CEB/IRQB 106

NC 107

VCCK11 109

GPIO/DDCSCL0/AUXP/PWM4 110

GPIO/DDCSDA0/AUXN/PWM5 111

GPIO/DDCSCL1/AUXP 112

GPIO/DDCSDA1/AUXN 113

GPIO/DDCSCL2/AUXP 114

GPIO/DDCSDA2/AUXN 115

NC 116

X0 117

XI 118

RX_V33 119

REXT(12k to GND) 120

NC 121

NC 122

NC 123

NC 124

NC 125

NC 126

NC 127

NC 128

SCA_SPI_WP#

SC_MODE1

SC_MODE2

SC_BKOFF#

EDP_BKLCTL

S_INVT_PWM

SC_MODE1 (38)

SC_MODE2 (38)

SC_BKOFF# (21)

EDP_BKLCTL (21,7)

S_INVT_PWM (21,51)

RSC12 22_0402_5%

SCA_SPI_CK

SCA_SPI_SDI

SCA_SPI_SDO

SCA_SPI_CS#

CSC8 @EMI@ 10P_0402_50V8J

* CSC8 Close to USC2

+1.1V_SCA_S5 CSC211 SC@ 0.1U_0402_16V4Z

EDP_AUXP/N swap for error pin define 01/26

EDP_AUXP_SC EDP_AUXP_SC (21)

EDP_AUXN_SC EDP_AUXN_SC (21)

HDMI_IN_SCLK HDMI_IN_SCLK (24)

HDMI_IN_SDAT HDMI_IN_SDAT (24)

SC_SMLCLK1

SC_SMLDATA1

Remove RSC50/RSC51 ,add QSC4 for SC_SMLCLK/DATA1 01/26

SCA_XO

SCA_XI

REXT

+3V_SCA_S5 SC@ 0.1U_0402_16V4Z CSC23

Remove RSC45

CSC23 change to 0.1U 01/26

SC@ RSC48 12K_0402_1%

+3V_SCA_S5

SC_BKOFF# RSC391 @ 2 10K_0402_5%

S_ENVDD RSC401 @ 2 4.7K_0402_5%

SC_SMLCLK1 RSC451 SC@ 2 4.7K_0402_5%

SC_SMLDATA1 RSC501 SC@ 2 4.7K_0402_5%

Add RSC45 / RSV50 pull-high for SC_SML 0217

+3VS_S0

SC@ QSC4B

SC_SMLCLK1 APU_SCLK0 (12,13,8)

L2N7002DW1T1G_SC88-6

SC@ QSC4A

SC_SMLDATA1 APU_SDATA0 (12,13,8)

L2N7002DW1T1G_SC88-6

EEPROM 16K

+3V_SCA_S5

CSC16 0.1U_0402_16V4Z

RSC17 4.7K_0402_5%

USC3 A0 A1 A2 GND VCC WP SCL SDA

BR24G16F-3GTE2 SOP8

SA00001N800

SC_WP_PRO_R RSC25 47_0402_5% SC_WP_PRO

SC_EESCL_R RSC27 0_0402_5% SC_EESCL

SC_EESDA_R RSC28 0_0402_5% SC_EESDA

FOR OSD/HDCP Parameter Value

AMD	PROJECT_ID1	PROJECT_ID2	PROJECT_ID3
C4	H	H	L
C5	H	L	L
S5	H		H

+3V_SCA_S5

4.7K_0402_5% SC@ RSC56 SC_MODE1

4.7K_0402_5% SC@ RSC57 SC_MODE2

4.7K_0402_5% SC@ RSC58 SC_MODE3

RSC56/RSC57/RSC58 change to unpop 0401

	SC_MODE1	SC_MODE2	SC_MODE3 (Reserve)
PC mode	L	L	X
Monitor mode	L	H	X
AMP Mute	H	L	X
S5 Mode	H	H	X

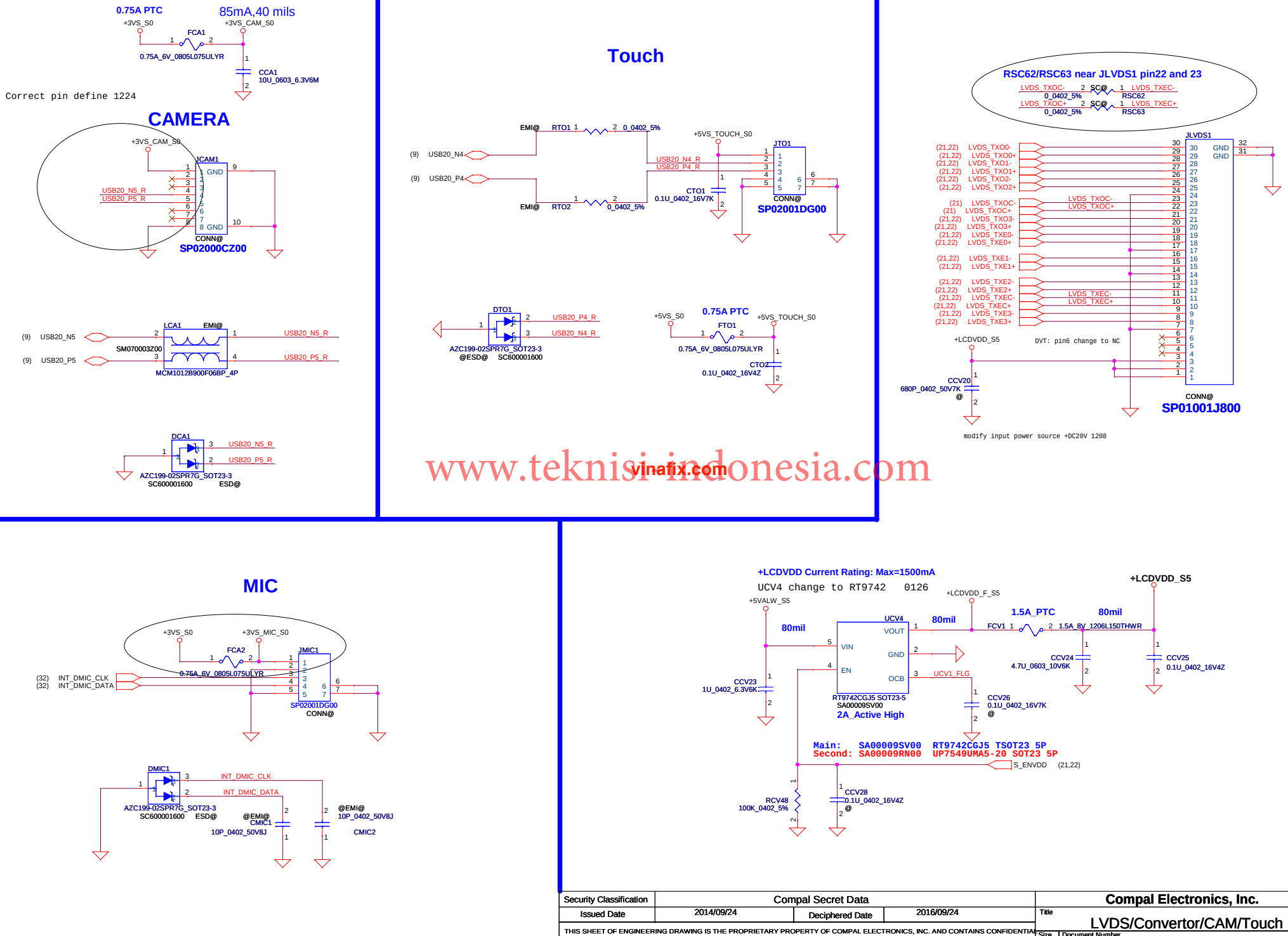
Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: Scalar RTD2506S

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 22 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: LVDS/Convertor/CAM/Touch

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

Date: Friday, April 01, 2016 Sheet 23 of 56

Add UHI1 switch for HDMI_IN power 02/19

HDMI-in Connector

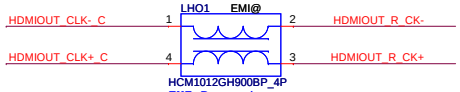
Reserve RHI14 for Non-Write protect 12/18

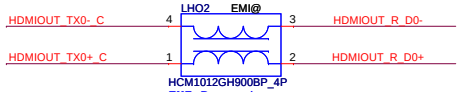
Add DHI4 02/15

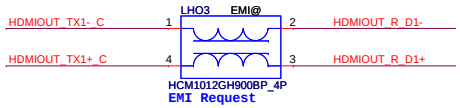
reserve 0 ohm to GND 0225

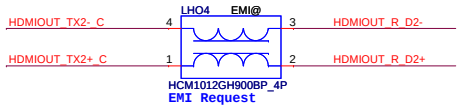
Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

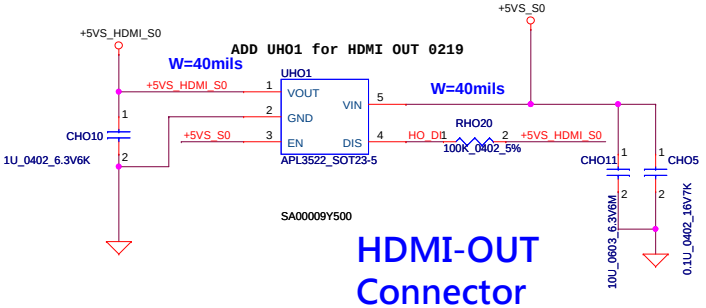
Compal Electronics, Inc.			
Title	HDMI-IN conn		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 24 of 56		



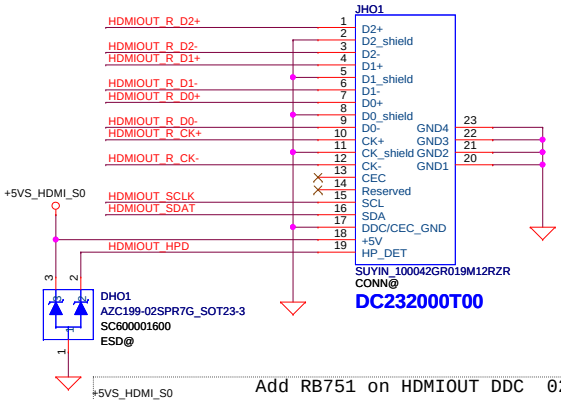


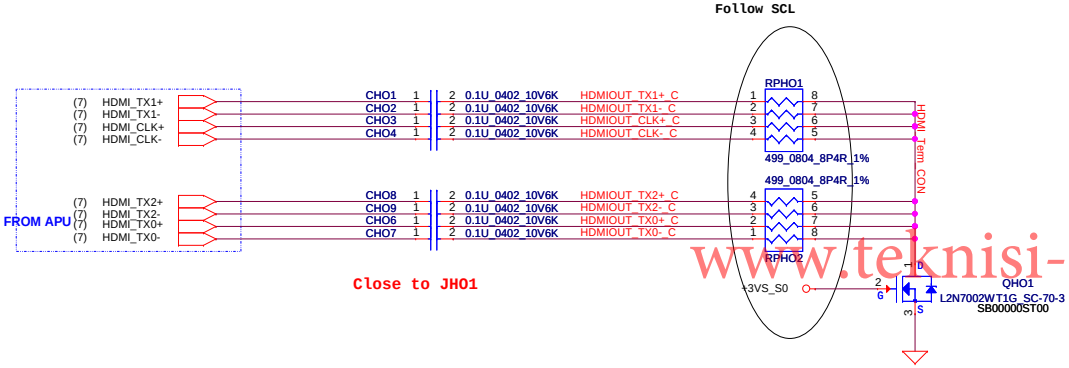


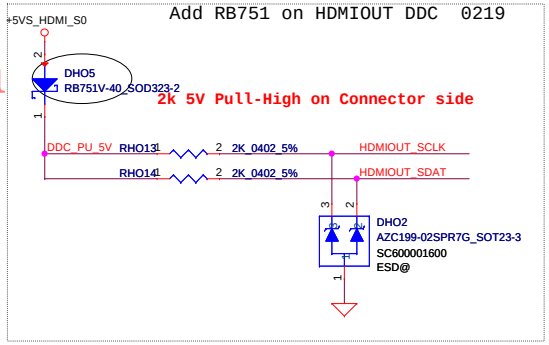


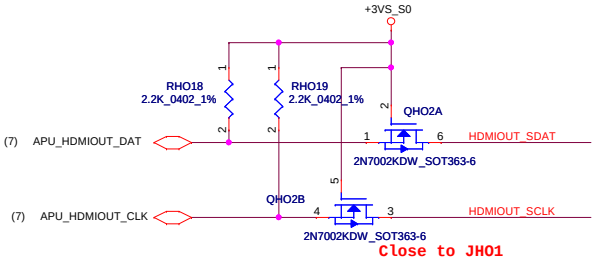


HDMI-OUT Connector

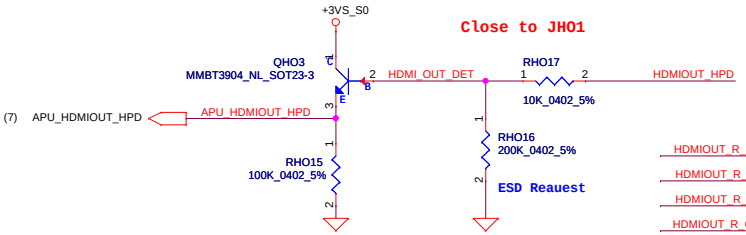


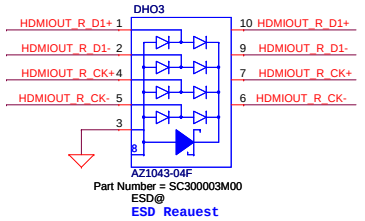


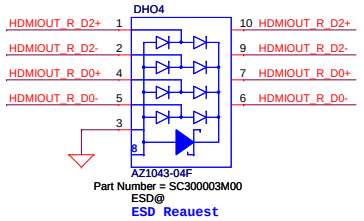




QHO2 change to SB00000PV00 0217



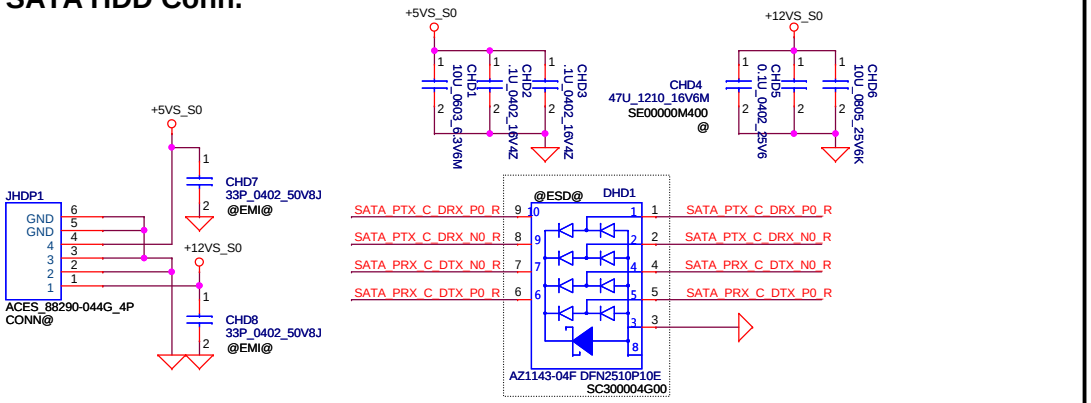


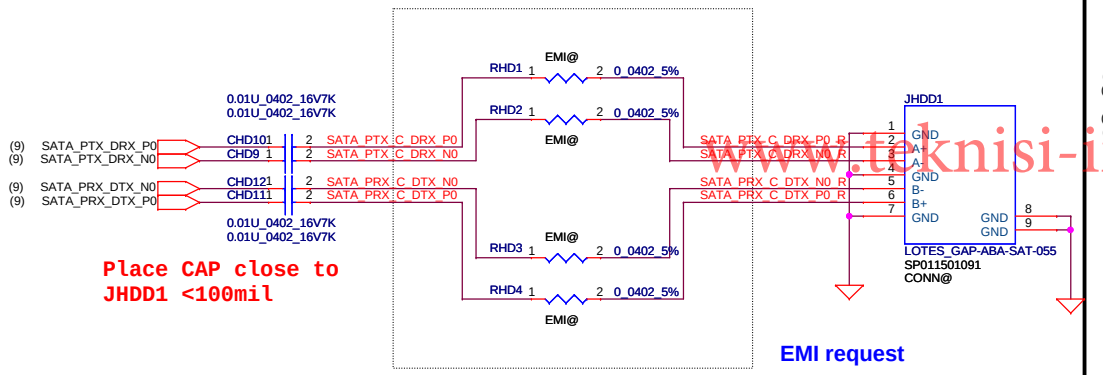


Security Classification	Compal Secret Data		
Issued Date	2014/04/02	Deciphered Date	2015/10/02

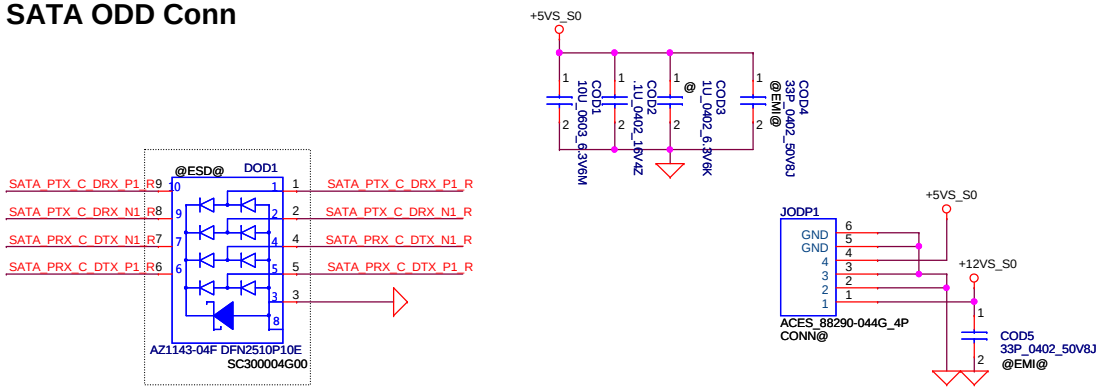
Compal Electronics, Inc.	
Title	P21-HDMI
Size	Document Number: LA-D961P M/B
Rev	0.1
Date:	Friday, April 01, 2016
Sheet	25 of 56

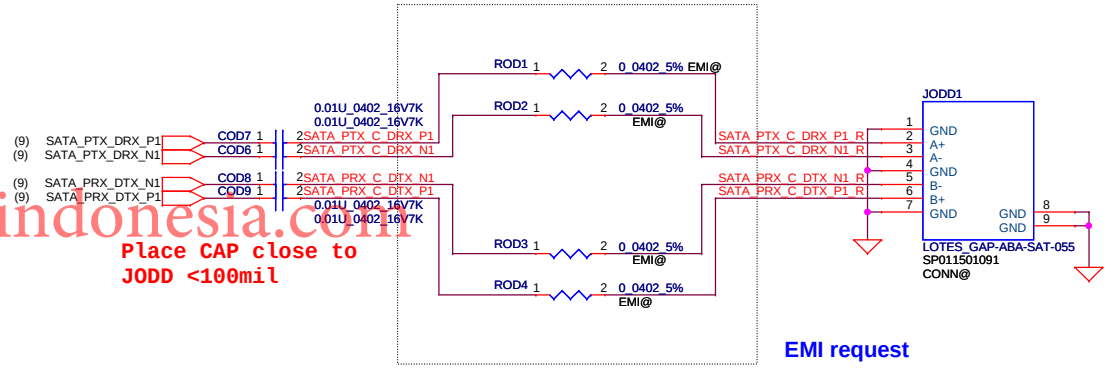
SATA HDD Conn.





SATA ODD Conn





Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

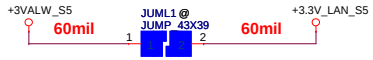
Compal Electronics, Inc.

Title: HDD/ODD

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

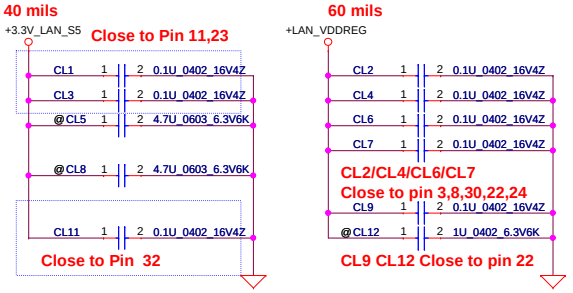
Date: Friday, April 01, 2016 | Sheet 26 of 56

WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN_S5 rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)



LED Status

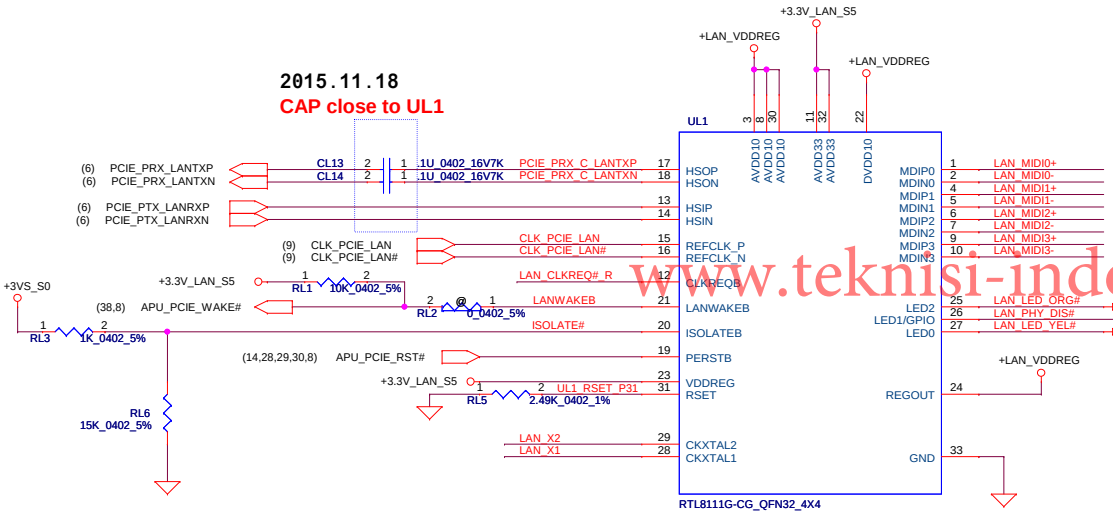
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

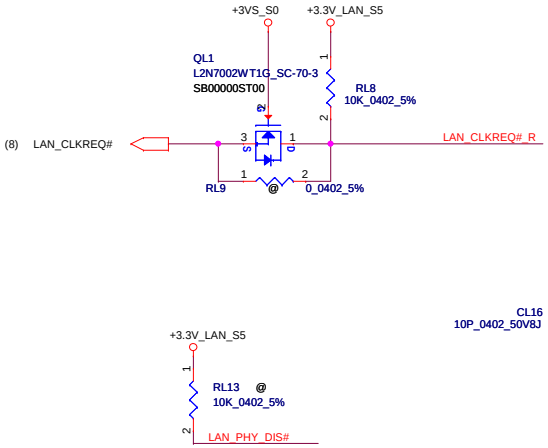
always on

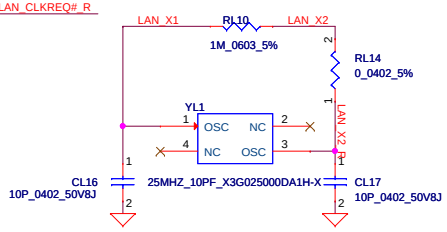
blinking

2015.11.18

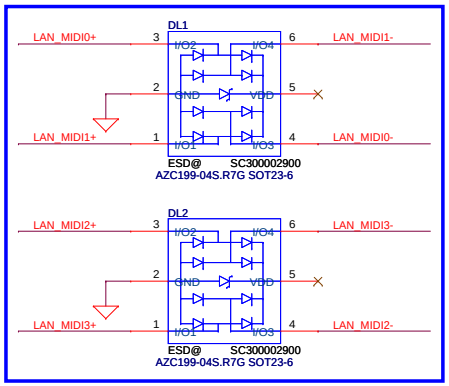
CAP close to UL1

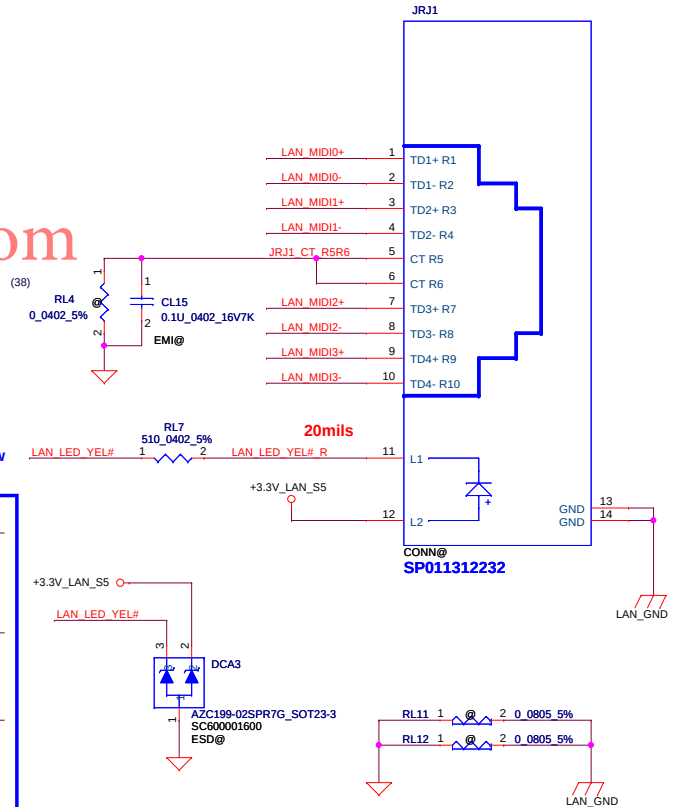






SA00005V700





Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: LAN RTL8111G-CG

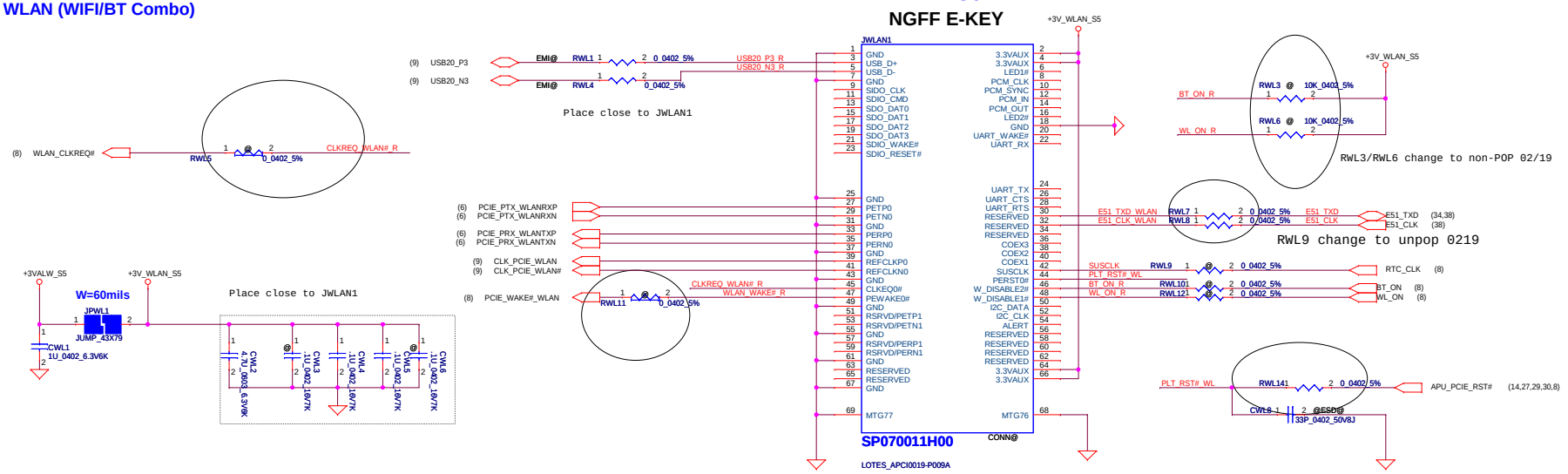
Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 27 of 56

WLAN (WIFI/BT Combo)

WLAN Conn.

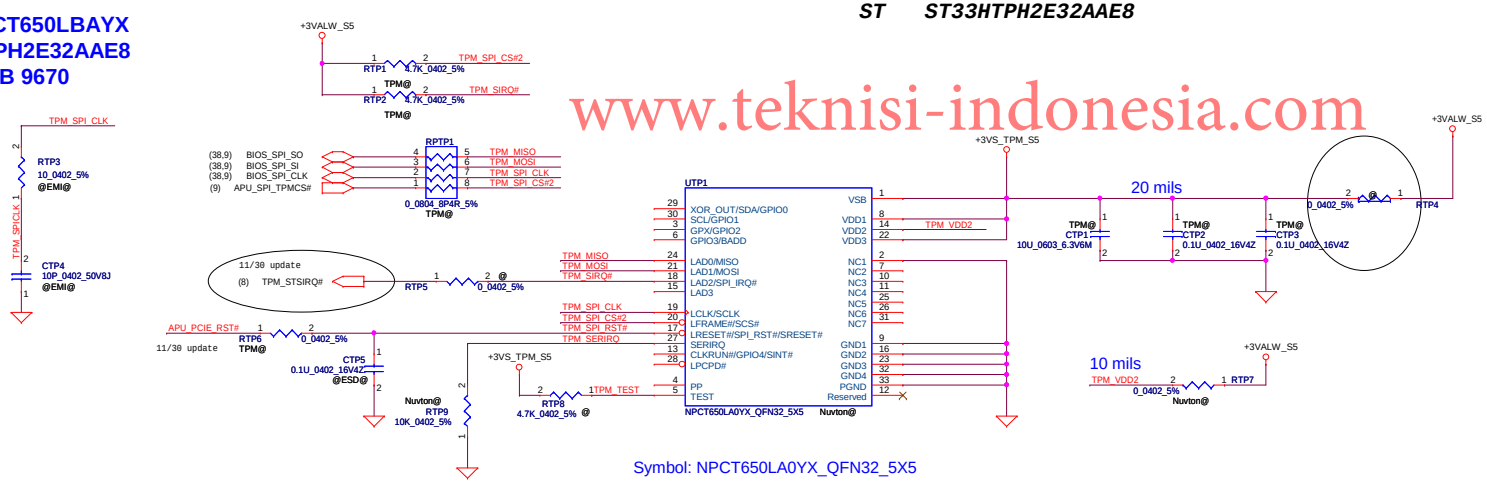
NGFF E-KEY



TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



Symbol: NPCT650LA0YX_QFN32_5X5

TPM/TCM IC

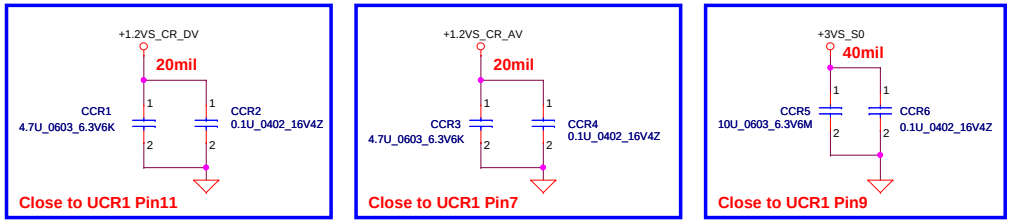
ST_ST33HTPH2E32AAE8(SPI) Infineon_SLB 9670(SPI)

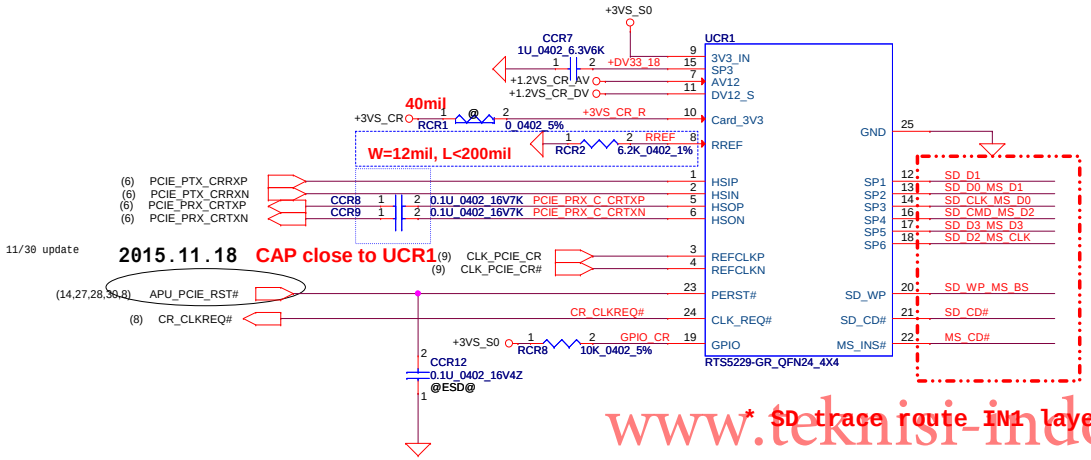
(Default)

Pop / Un-pop For Co-lay	RTP7	RTP9	BOM Config
Nuvton_NPCT650LBAYX（SPI）	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	X	X	Infineon@+TPM@

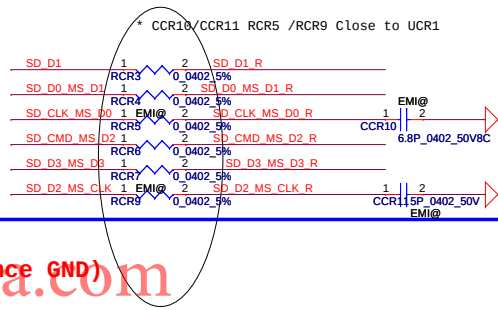
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/04/02	Deciphered Date	2015/10/02

Title	WLAN (NGFF) / TPM		
Size	Document Number		Rev
	LA-D961P M/B		0.1
Date:	Friday, April 01, 2016	Sheet	28 of 56

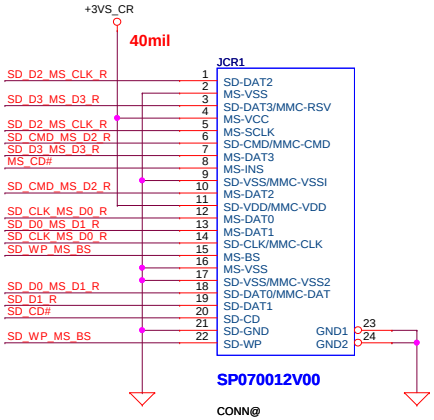


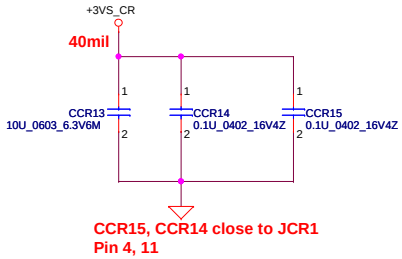


Length of per trace 2inch no more 2 via
mismatch trace length <100mil
50ohm +-15% impedance.



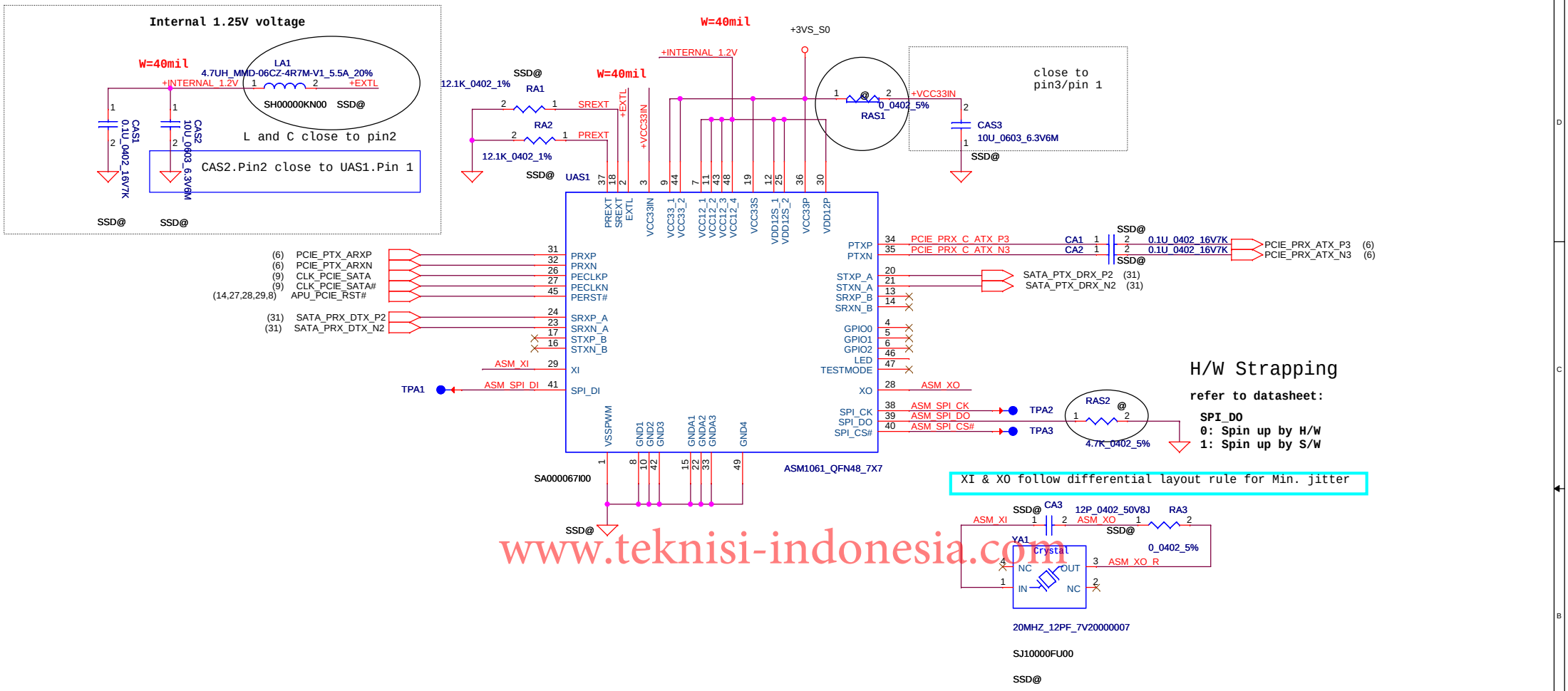
* SD trace route IN1 layer (reference GND)





Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title	PCIE-Card Reader-RTS5229		
Size	Document Number		Rev
	LA-D961P M/B		0.1
Date:	Friday, April 01, 2016	Sheet	29 of 56



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/01	Deciphered Date	2013/09/01
Title	ASM1061		
Size B	Document Number LA-D961P M/B		Rev 0.1
Date: Friday, April 01, 2016	Sheet 30 of 56		

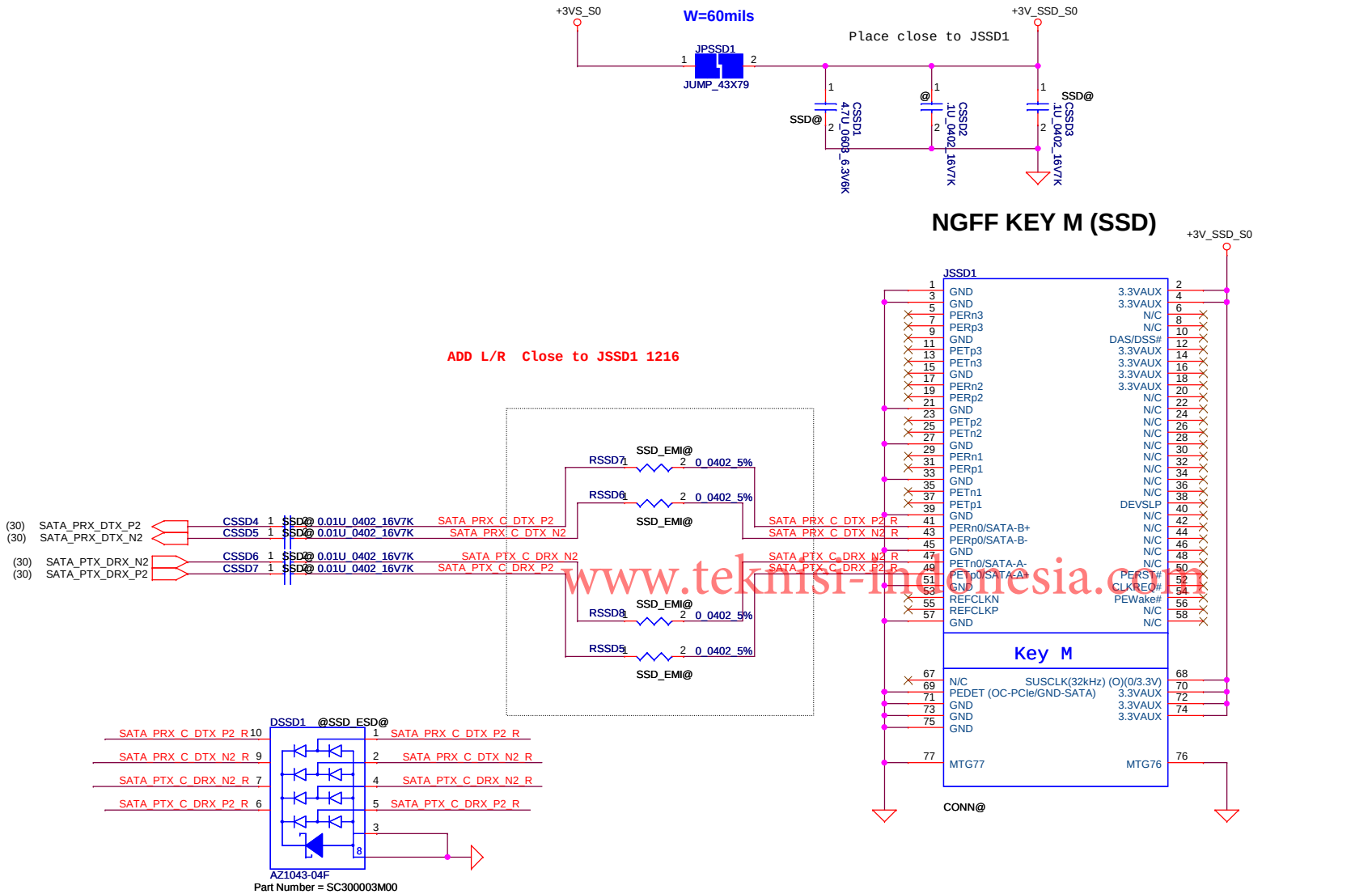


Table 31. Socket 2 SATA-based SSD Module Pinout

74	3.3V	CONFIG_2 = GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 = GND	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved for MFG Clock	GND	57
56	Reserved for MFG Data	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	SATA-A+	49
48	N/C	SATA-A-	47
46	N/C	GND	45
44	N/C	SATA-B-	43
42	N/C	SATA-B+	41
40	N/C	GND	39
38	DEVSLP (I)(0/3.3V)	N/C	37
36	N/C	N/C	35
34	N/C	GND	33
32	N/C	N/C	31
30	N/C	N/C	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	CONFIG_0 = GND	21
20	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
10	DAS/DSS# (IO)(OD)	N/C	11
8	N/C	N/C	9
6	N/C	N/C	7
4	3.3V	N/C	5
2	3.3V	GND	3
		CONFIG_3 = GND	1

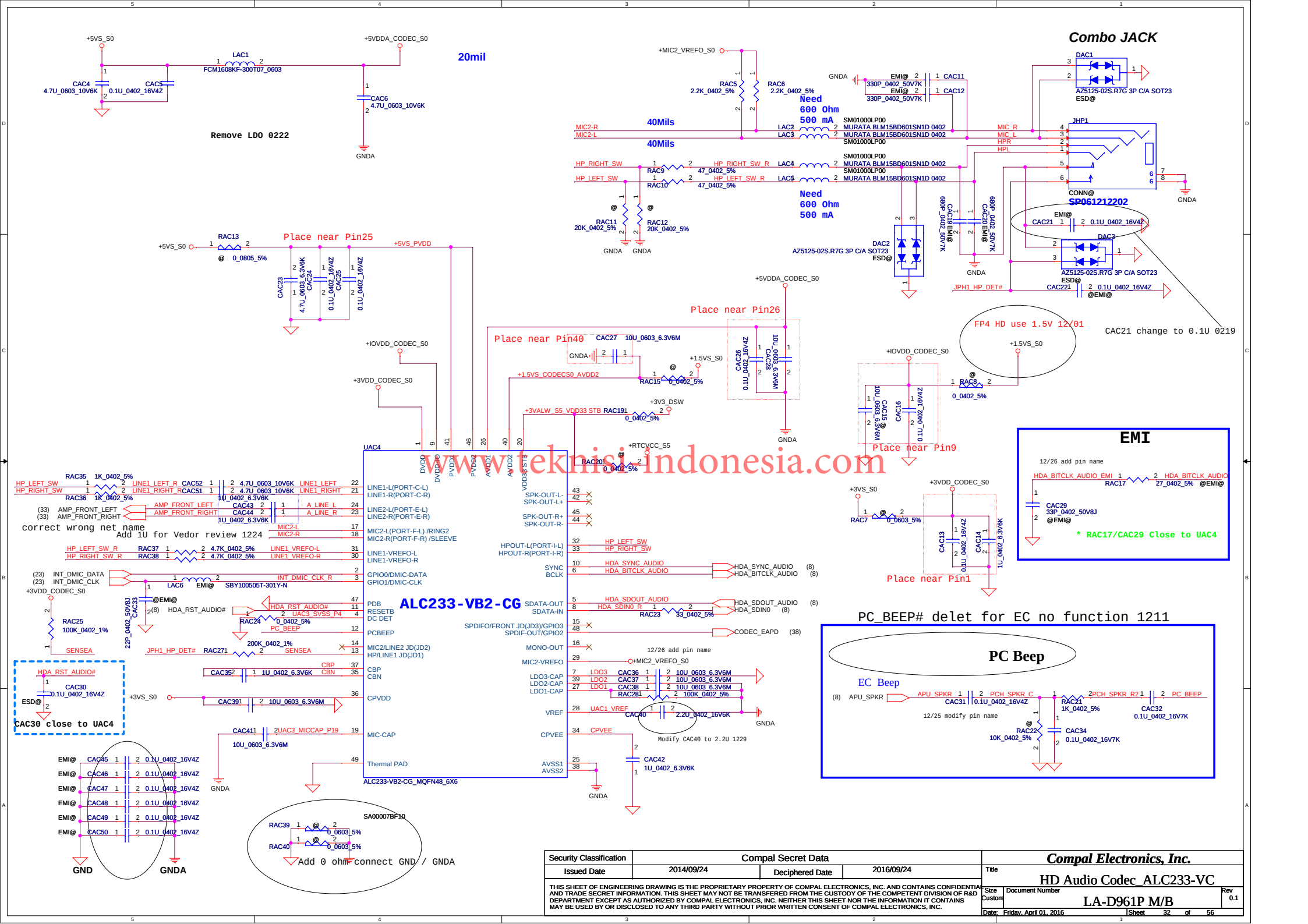
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: SSD (M2) - SATA

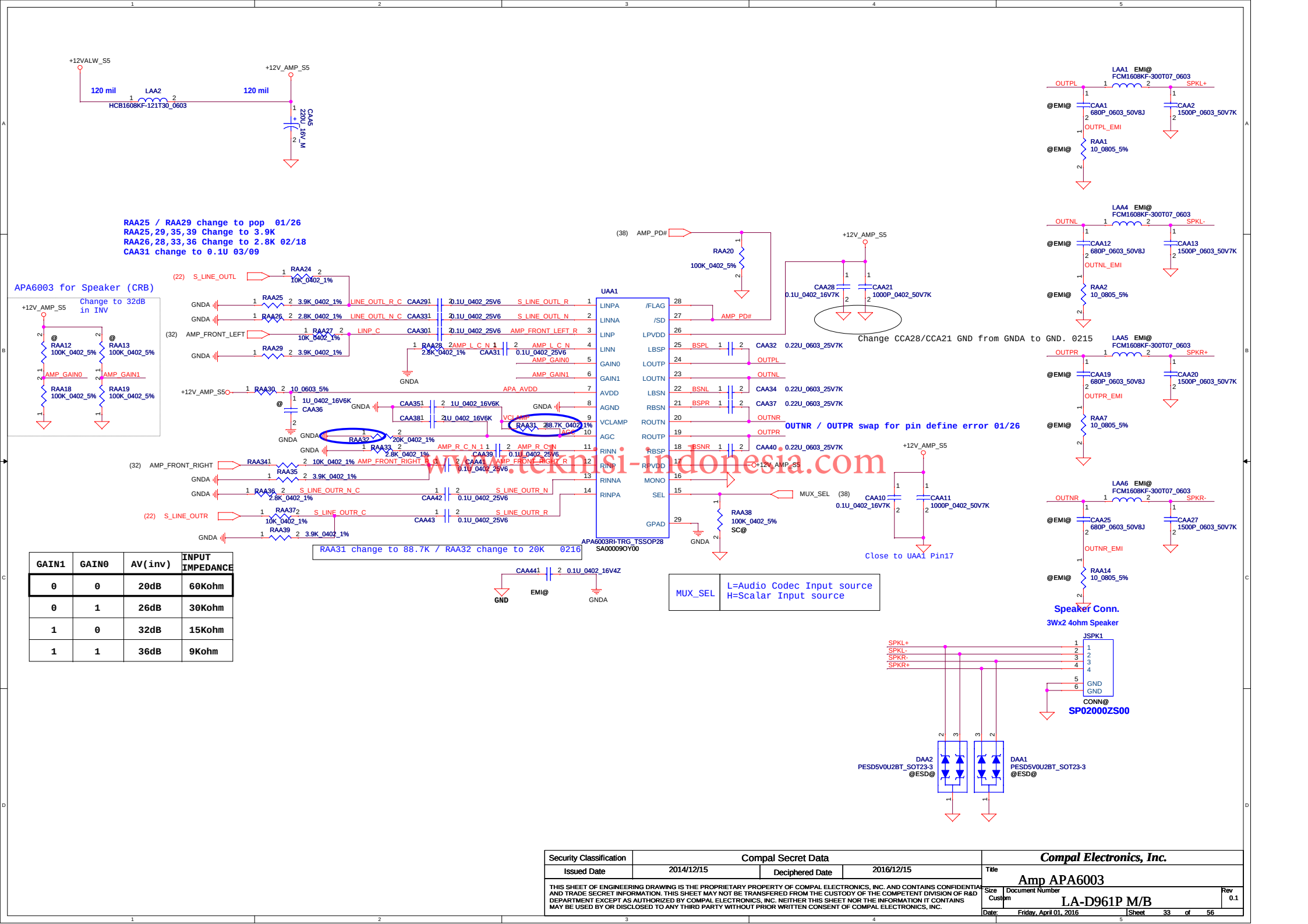
Size: B | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 31 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title	HD Audio Codec_ALC233-VC		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 32 of 56		



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

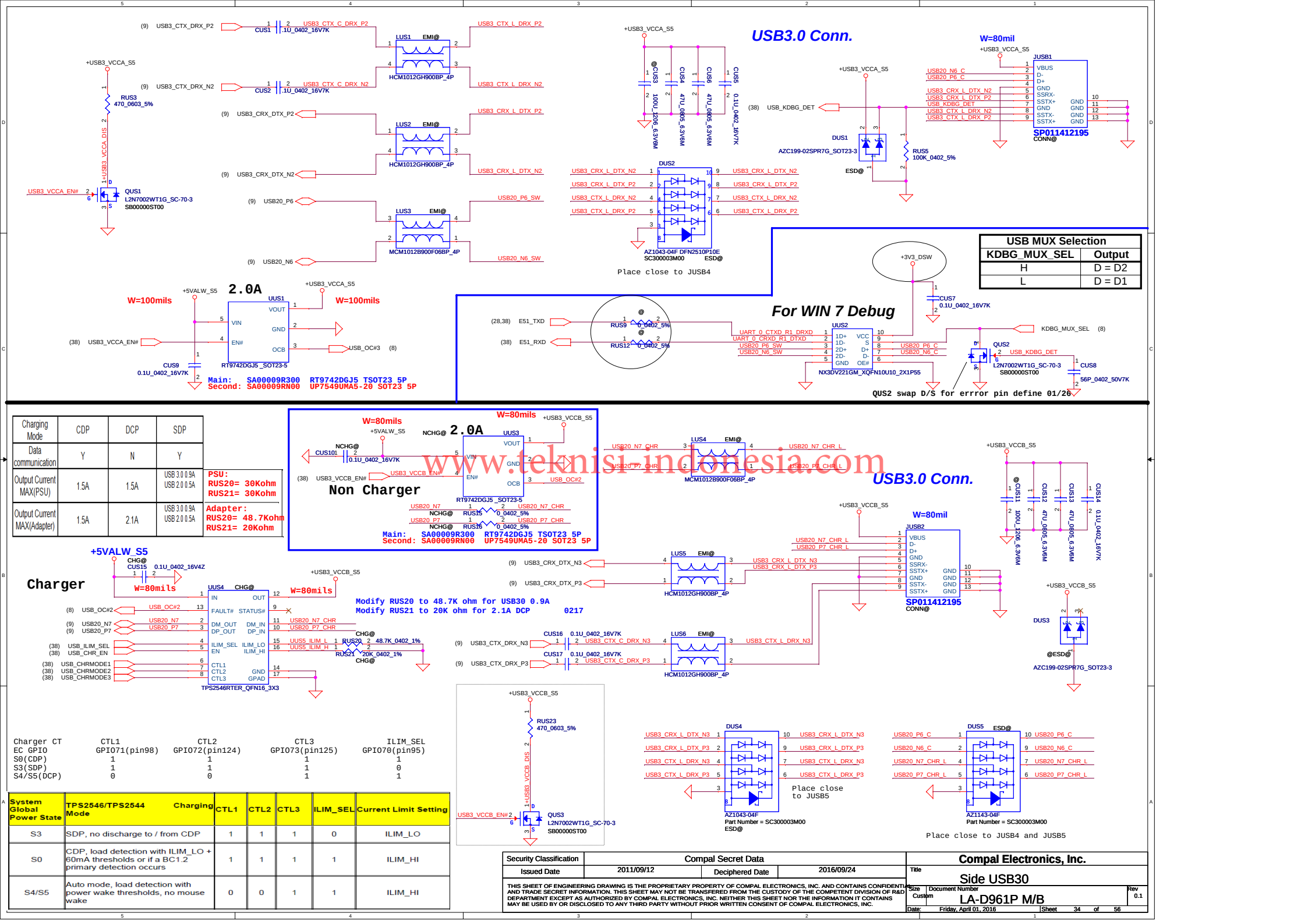
Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

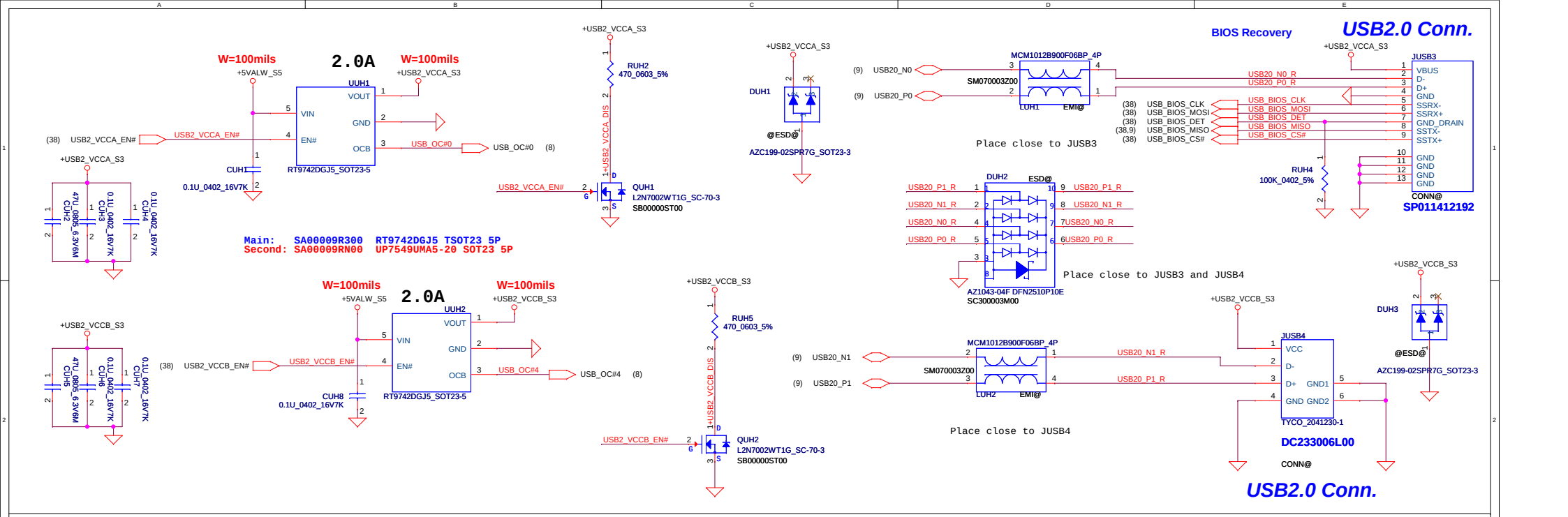
Compal Electronics, Inc.

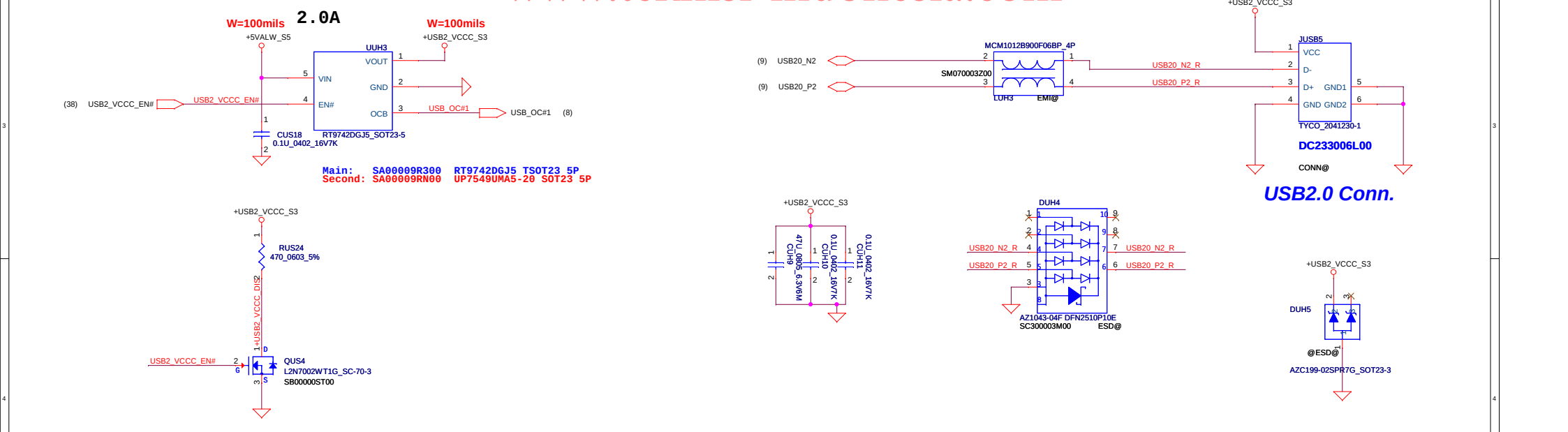
Title: Amp APA6003

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 33 of 56


USB3.0 Conn.
W=80mil
+USB3_VCCA_S5
JUSB1
SP011412195
CONN@
USB MUX Selection
KDBG_MUX_SEL | Output
H | D = D2
L | D = D1
For WIN 7 Debug
+3V3_DSW
USB_KDBG_DET
KDBG_MUX_SEL (8)
QUS2 swap D/S for errror pin define 01/26
2.0A
W=100mils
+5VALW_S5
RT9742DGJ5_SOT23-5
Main: SA00009R300 RT9742DGJ5 TSOT23 5P
Second: SA00009RN00 UP7549UMA5-20 SOT23 5P
Charging Mode | CDP | DCP | SDP
Data communication | Y | N | Y
Output Current MAX(PSU) | 1.5A | 1.5A | USB 3.0 0.9A / USB 2.0 0.5A
Output Current MAX(Adapter) | 1.5A | 2.1A | USB 3.0 0.9A / USB 2.0 0.5A
PSU:
RUS20= 30Kohm
RUS21= 30Kohm
Adapter:
RUS20= 48.7Kohm
RUS21= 20Kohm
Non Charger
W=80mils
NCHG@ 2.0A
+USB3_VCCB_S5
www.teknisi-indonesia.com
Charger
+5VALW_S5
CHG@
Modify RUS20 to 48.7K ohm for USB30 0.9A
Modify RUS21 to 20K ohm for 2.1A DCP 0217
TPS2546RTER_QFN16_3X3
Charger CT | CTL1 | CTL2 | CTL3 | ILIM_SEL
EC GPIO | GPIO71(pin98) | GPIO72(pin124) | GPIO73(pin125) | GPIO70(pin95)
S0(CDP) | 1 | 1 | 1 | 1
S3(SDP) | 1 | 1 | 1 | 0
S4/S5(DCP) | 0 | 0 | 1 | 1
System Global Power State | TPS2546/TPS2544 Charging Mode | CTL1 | CTL2 | CTL3 | ILIM_SEL | Current Limit Setting
S3 | SDP, no discharge to / from CDP | 1 | 1 | 1 | 0 | ILIM_LO
S0 | CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs | 1 | 1 | 1 | 1 | ILIM_HI
S4/S5 | Auto mode, load detection with power wake thresholds, no mouse wake | 0 | 0 | 1 | 1 | ILIM_HI
Place close to JUSB4
Place close to JUSB5
Place close to JUSB4 and JUSB5
Security Classification | Compal Secret Data
Issued Date | 2011/09/12 | Deciphered Date | 2016/09/24
Compal Electronics, Inc.
Title: Side USB30
Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1
Date: Friday, April 01, 2016 | Sheet 34 of 56





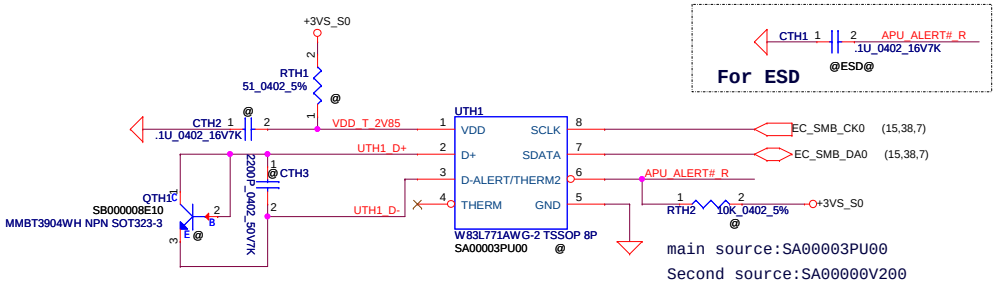
Security Classification	Compal Secret Data		
Issued Date	2014/09/24	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: Rear USB PORT

Size	Document Number	Rev
Custom	LA-D961P M/B	0.1

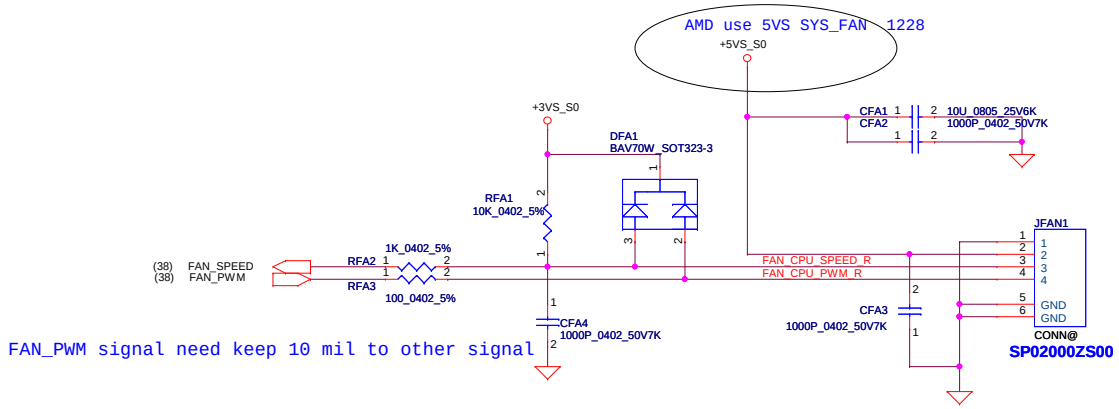
Date: Friday, April 01, 2016 Sheet 35 of 56



EC

main source:SA00003PU00
Second source:SA00000V200

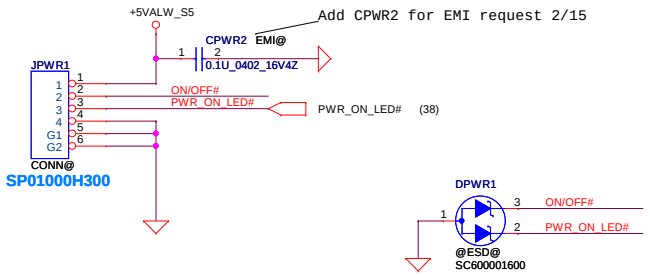
SMBus address Hex 9A(1001 101).

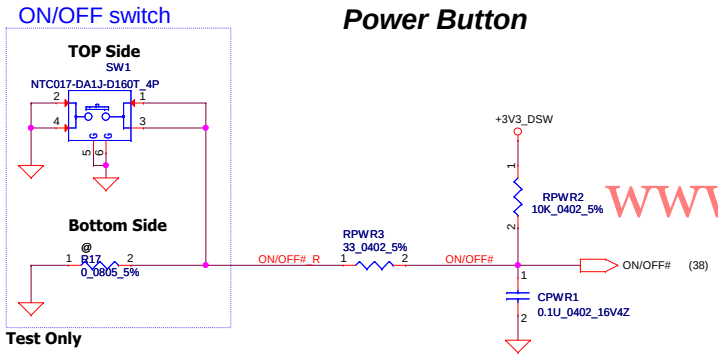


FAN_PWM signal need keep 10 mil to other signal

Security Classification	Compal Secret Data		
Issued Date	2014/04/02	Deciphered Date	2015/10/02

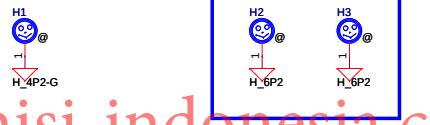
Compal Electronics, Inc.			
Title	Thermal / FAN		
Size	Document Number		Rev
	LA-D961P M/B		0.1
Date:	Friday, April 01, 2016	Sheet	36 of 56





WIFI Hole

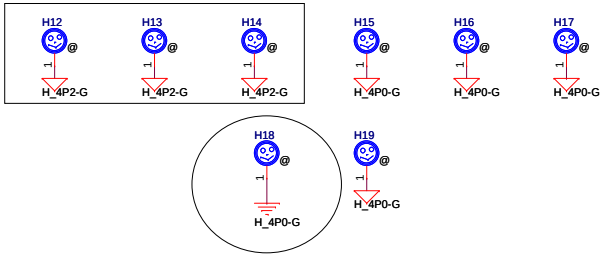
SSD Hole



Screw Hole

MB up side

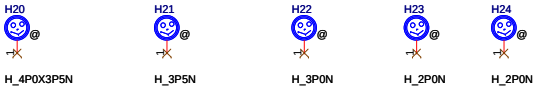
4mm x 4 / 4.8mm x3



H18 for Convertor board GND SCREW HOLE 1217

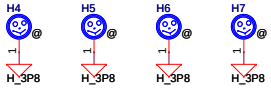
4.0mmX3.5mm x1/3.5mm x 1 / 3.0mm x1

2P0 x2



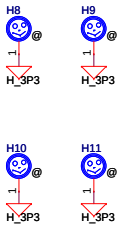
CPU Hole

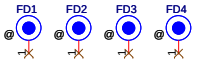
3.8mm x 4



GPU Hole

3.3mm x 4





Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

Compal Electronics, Inc.			
Title	PWR SW/LED/SCREW		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 37 of 56		

Place closely UEC2

CEC12 change to pop for EMI request 2/15

ADD EN_1.8V_EN 12/08

Side USB Port

Rear USB Port

USB_KDBG_DET move to Pin14 / PWR_0.95V_PG move to Pin8 0222

LPC Address Select:
0: 2Eh/2Fh
1: 4Eh/4Fh

REC53 CEC28 Close to UEC2 1209

V1.0 update

0122 update

HDMI_IN_function change to pin126 (12/17)

1Mb SPI ROM

AD Voltage Range:
0 to 2.048 V

Add Panel_ID4 0216

Ra (100K)
EVT : 30K Ohm : 0.76V
DVT : 56K Ohm : 1.18V
PVT : 100K Ohm : 1.67V
MP : 150K Ohm : 1.98V

change BID table 1225

remove APU_EC_RST# ,add INA300_LATCH 1214

Rear USB Port

BIOS recovery

(24mA sink current)

Add INA300_ALERT# on pin49 1214

Change with pin 51

Rear USB Port

Power

PWR_0.95V_PG move to pin63 0223

Pin73 Reserve for INTEL platform 0222

REC39 CEC22 Close to UEC1 (SPI ROM)

CEC26 /27 change to 15P 02/18

AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis

EC DEBUG port
Reserve R2009 for EC debug.

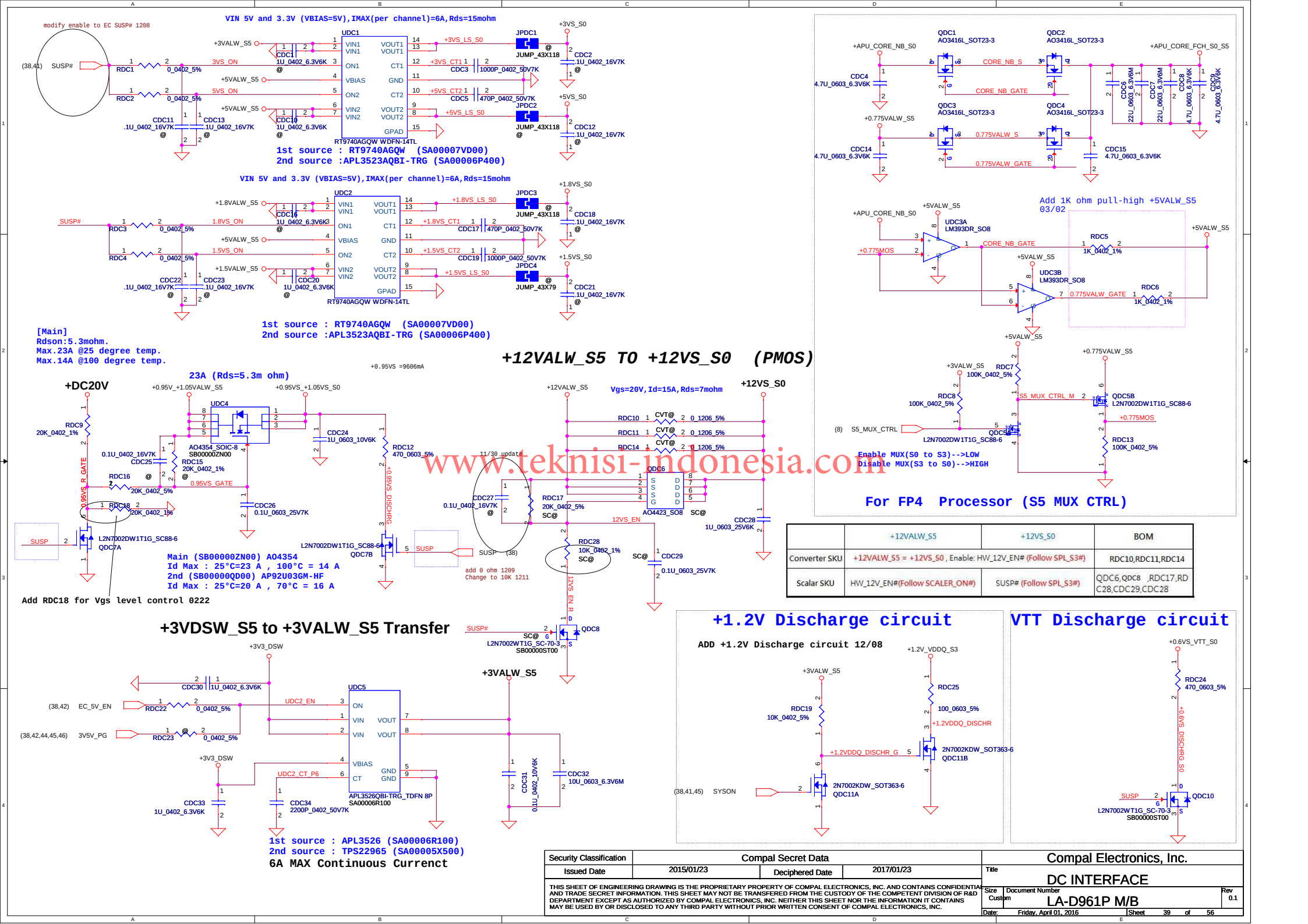
Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: EC NCT6685D

Size: Custom | Document Number: LA-D961P M/B | Rev: 0.1

Date: Friday, April 01, 2016 | Sheet 38 of 56



	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC10,RDC11,RDC14
Scalar SKU	HW_12V_EN#(Follow SCALER_ON#)	SUSP# (Follow SPL_S3#)	QDC6,QDC8 ,RDC17,RDC28,CDC29,CDC28

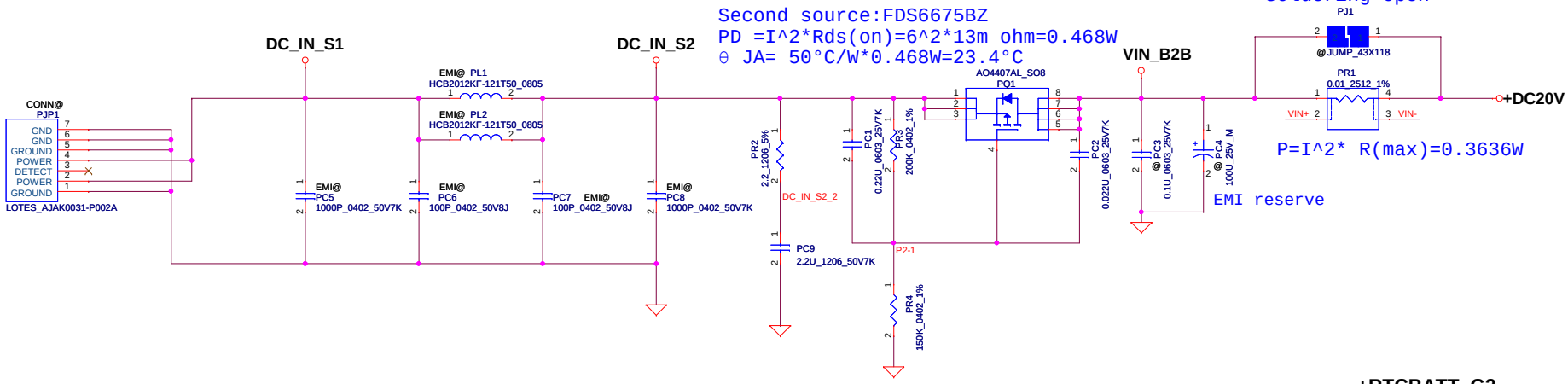
Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.			
Title	DC INTERFACE		
Size: Custom	Document Number: LA-D961P M/B		Rev: 0.1
Date: Friday, April 01, 2016	Sheet 39 of 56		

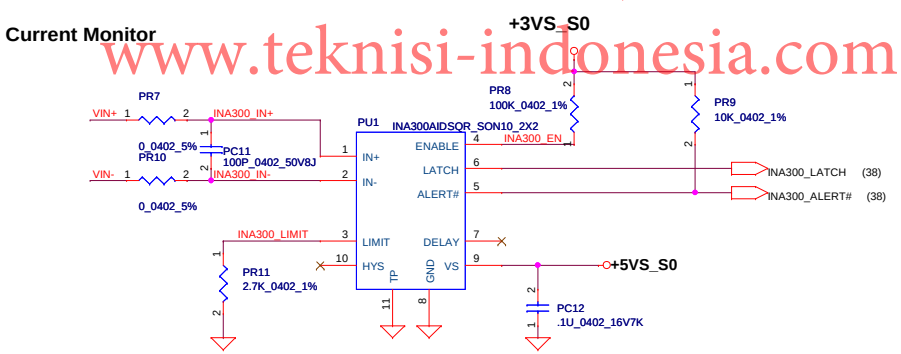
Main source:AO4407AL
PD =I^2*Rds(on)=6^2*11m ohm=0.396W
θ JA= 40°C/W*0.396W=15.84°C

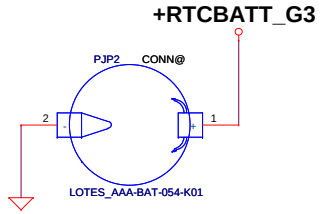
Second source:FDS6675BZ
PD =I^2*Rds(on)=6^2*13m ohm=0.468W
θ JA= 50°C/W*0.468W=23.4°C

soldering open



Current Monitor





RTC BATT CONNECTER

120W:
Full Load(100%) --> 6A
Vtrip=6*10m=60mV
VLimit=Vtrip; Rlimit=(60mV+0.5mV)/20uA= 3.025K

Trigger(90%) --> 5.4A
Vtrip=5.4*10m=54mV
Rlimit=(54mV+0.5mV)/20uA=2.725K
Select Rlimit=2.7K
I_Trigger-->5.35A

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

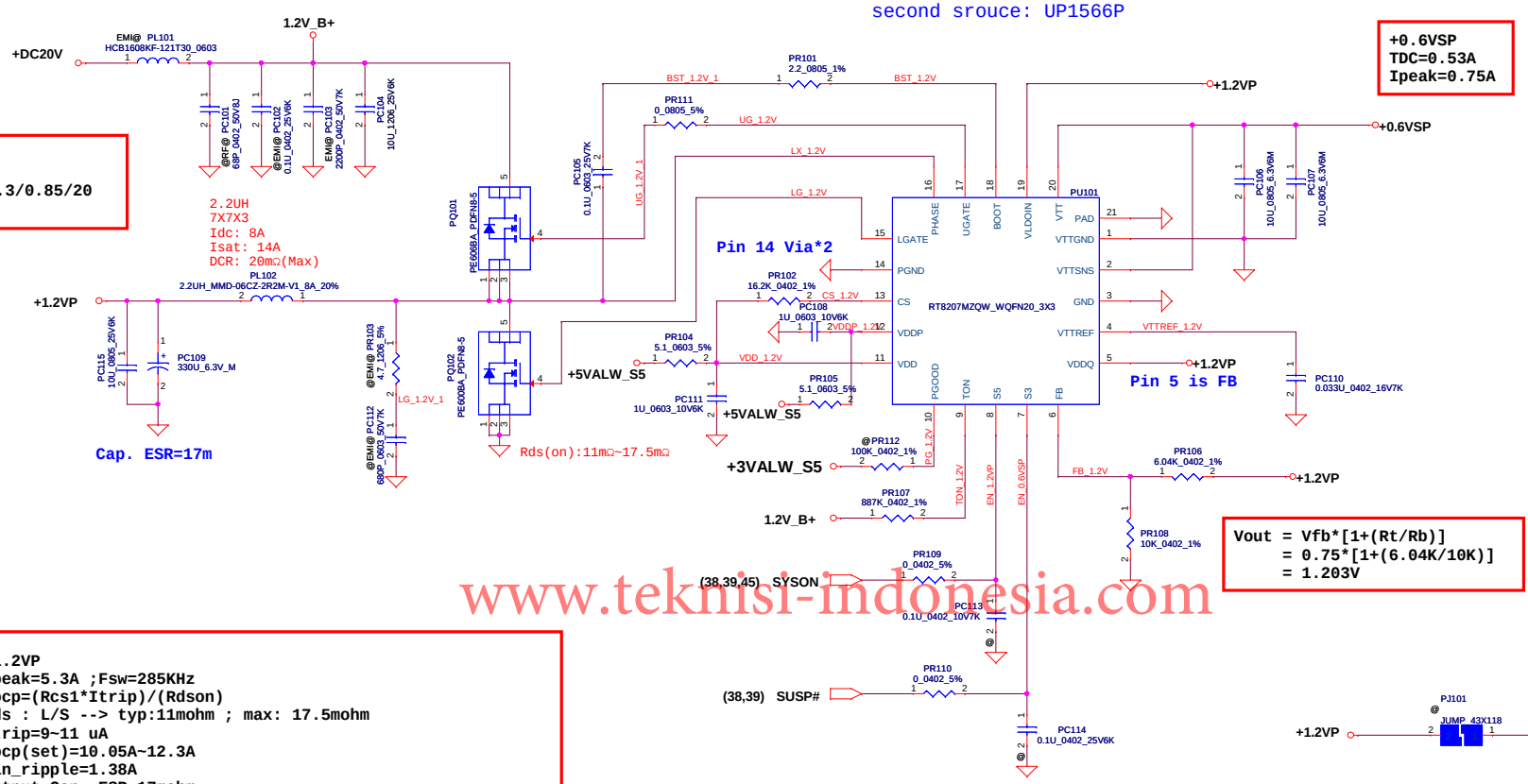
Title: **DCIN / CONN**

Size: Custom	Document Number	Rev: 0.1
Date: Friday, April 01, 2016	Sheet 40 of 56	

main source :RT8207M
second srouce: UP1566P

+0.6VSP
TDC=0.53A
Ipeak=0.75A

+1.2VP
Vin = 20V
Iin = 1.2*5.3/0.85/20
= 0.37A



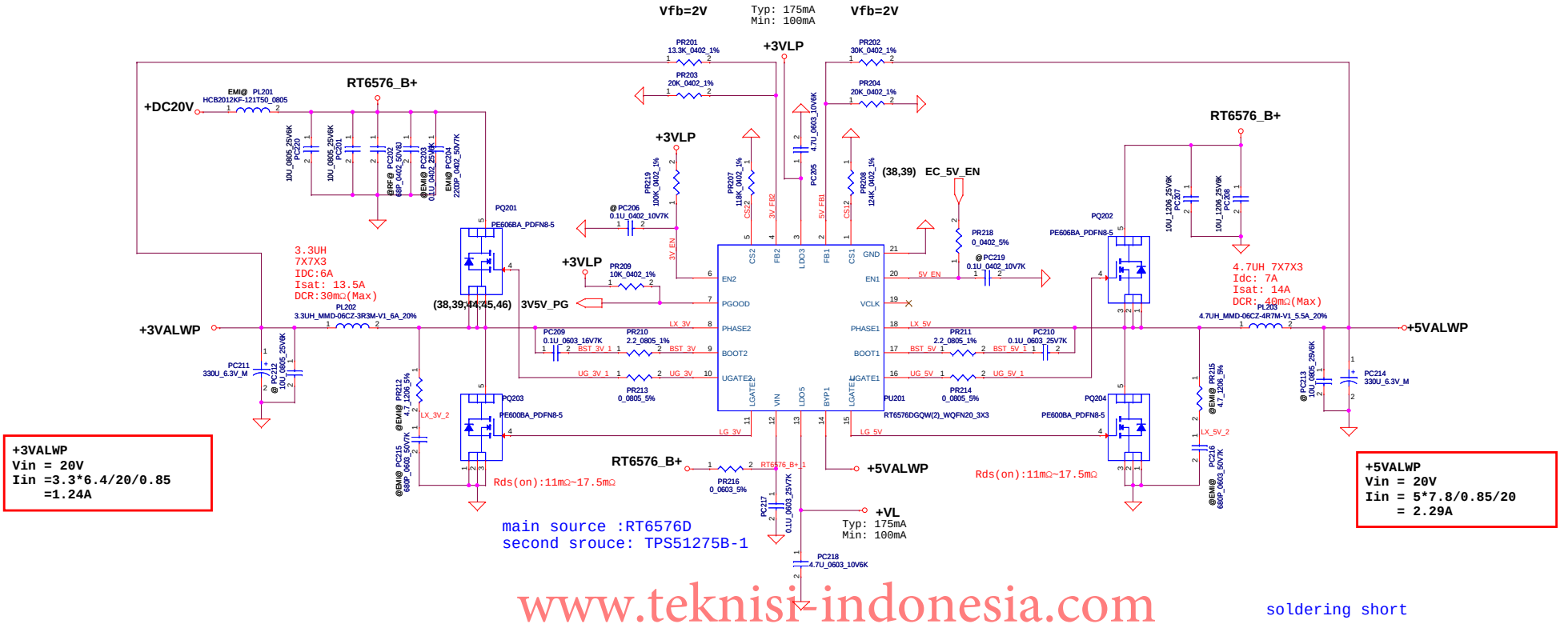
+1.2VP
Ipeak=5.3A ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(Rdson)
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9~11 uA
Iocp(set)=10.05A~12.3A
Iin_ripple=1.38A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.799A
LIR=Delta IL/Ipeak=0.339
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=533uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.37uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/29

Title: P49_PWR-DDR4/VTT(RT8129/RT9045)

Size	Document Number	Rev
Custom		0.1

Date: Friday, April 01, 2016 Sheet 41 of 56



soldering short

+5VALWP — @PJ201 JUMP_43X118 — +5VALW_S5

soldering short

+3VALWP — @PJ202 JUMP_43X118 — +3V3_DSW

+3VLP — PR221 0_0603_5% — +3VL_S5

PR220 @0_0603_5%

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+3VALWP
Ipeak=6.4A ;Itdc=4.48A;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9~11 uA
Iocp(set)=Iocp(set)=10.3A~12.7A
Iin_ripple=1.66A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.352A
LIR=Delta IL/Ipeak=0.36
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=240uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.87uF

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
=5V

+5VALWP
Ipeak =7.4A ;Itdc=5.2A; Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9~11 uA
Iocp(set)=11A~13.5A
Iin_ripple=2.36A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.66A
LIR=Delta IL/Ipeak=0.34
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=214uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.7uF

Title: +3VALWP / +5VALWP
Size: C
Document Number:
Rev: 0.1
Date: Friday, April 01, 2016
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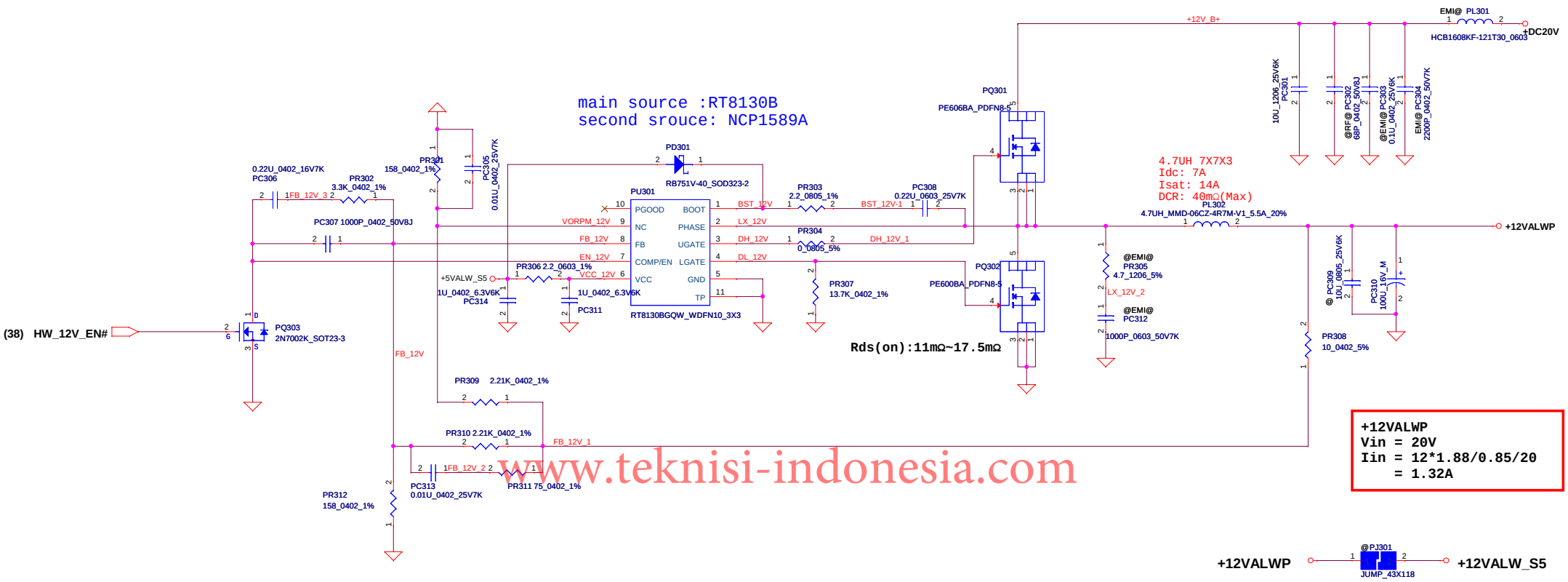


```
+12VALWP
Vin = 20V
Iin = 12*1.88/0.85/20
    = 1.32A
```

```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(2.21K/0.158K)]
     = 11.989V
```

```
+12VALW
Ipeak=1.88A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9.5~10.5uA
Iocp(set)=10.3A ~ 12.3A
Iin_ripple=0.35A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta IL/Ipeak=1.81
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=2.9uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.53uF
```

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

Title: **+12VS**

Size: Custom	Document Number	Rev: 0.1
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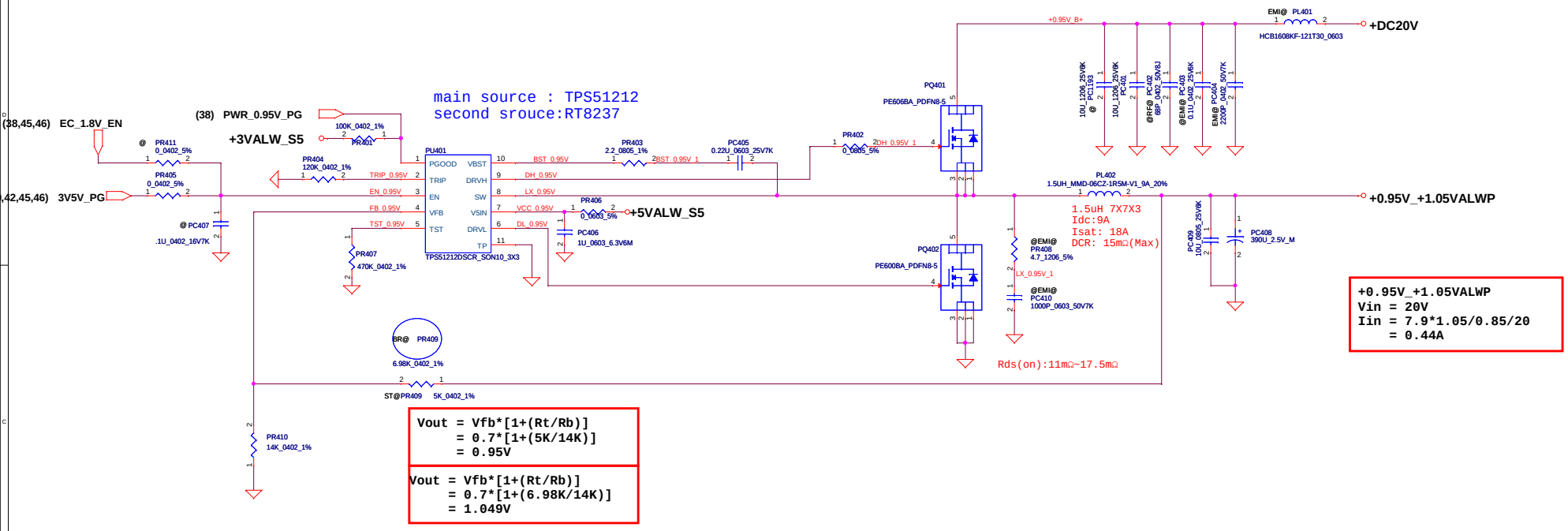

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/14K)]
= 0.95V

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(6.98K/14K)]
= 1.049V

+0.95V_+1.05VALWP
Vin = 20V
Iin = 7.9*1.05/0.85/20
= 0.44A

+0.95V_+1.05VALWP — @ PJ401 JUMP_43X118 — +0.95V_+1.05VALW_S5

+0.95VALW
Ipeak=7.9A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9.5~10.5uA
Iocp(set)=10.35A ~ 12.41A
Iin_ripple=1.31A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta IL/Ipeak=0.26
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=699uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.43uF

+1.05VALW
Ipeak=7.9A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:11mohm ; max: 17.5mohm
Itrip=9.5~10.5uA
Iocp(set)=10.45A ~ 12.52A
Iin_ripple=1.176A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.28A
LIR=Delta IL/Ipeak=0.29
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=591uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.47uF

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

Title: +1.05VALW

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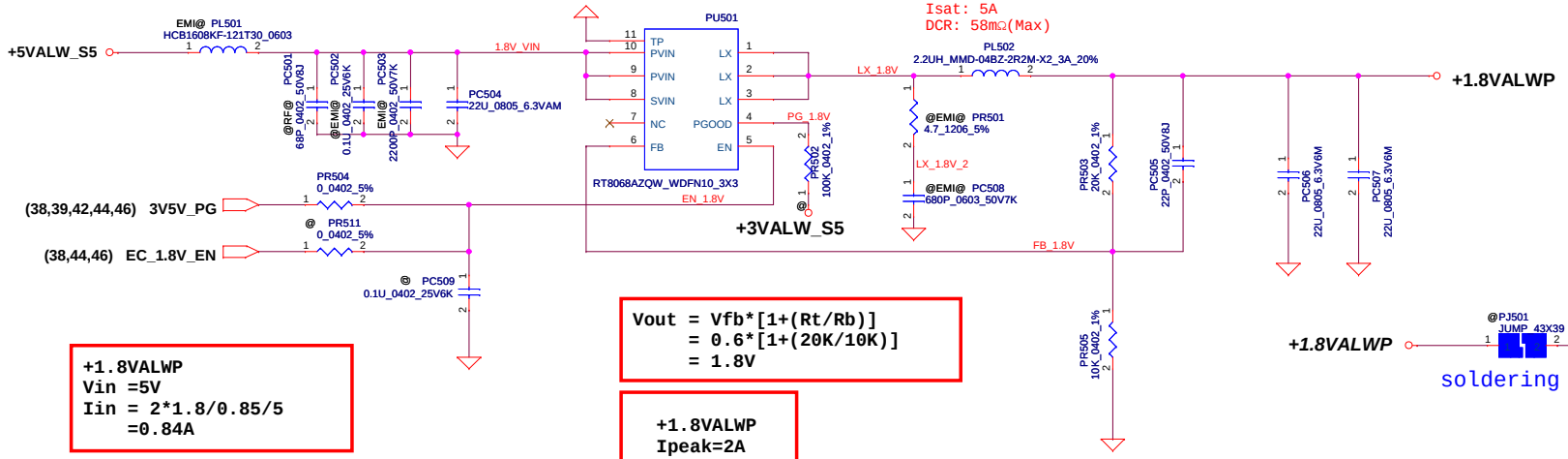
main source : RT8068A
second srouce:UP1727P

2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR: 58mΩ(Max)



+1.8VALWP
Vin =5V
Iin = 2*1.8/0.85/5
=0.84A

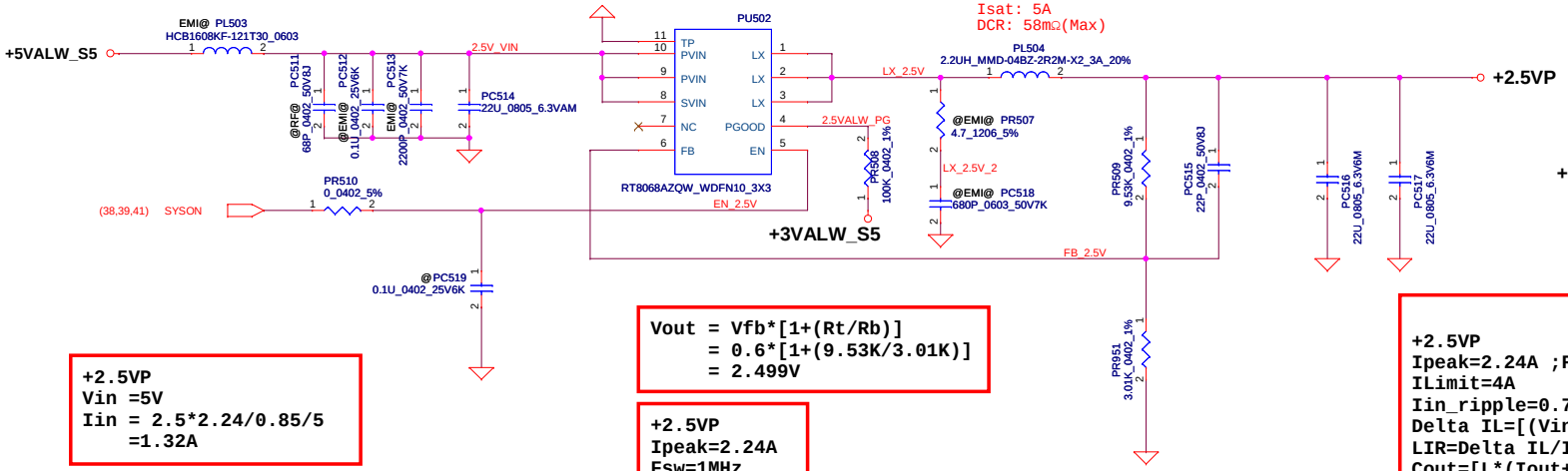
Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(20K/10K)]
= 1.8V

+1.8VALWP
Ipeak=2A
Fsw=1MHz

+1.8VALWP
Ipeak=2A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.69A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta IL/Ipeak=0.26
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=18.3uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.65uF

main source : RT8068A
second srouce:UP1727P

2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR: 58mΩ(Max)



+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A

Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(9.53K/3.01K)]
= 2.499V

+2.5VP
Ipeak=2.24A
Fsw=1MHz

+2.5VP
Ipeak=2.24A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

Title: +1.8VSP

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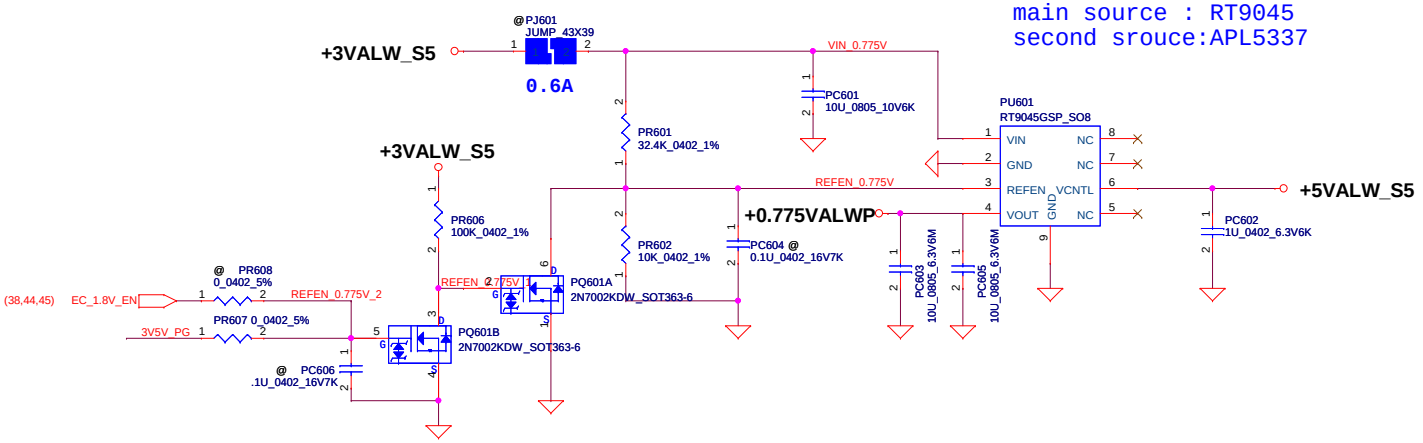
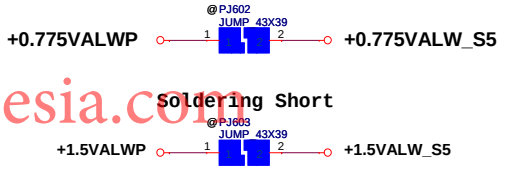
main source : RT9045
second srouce:APL5337



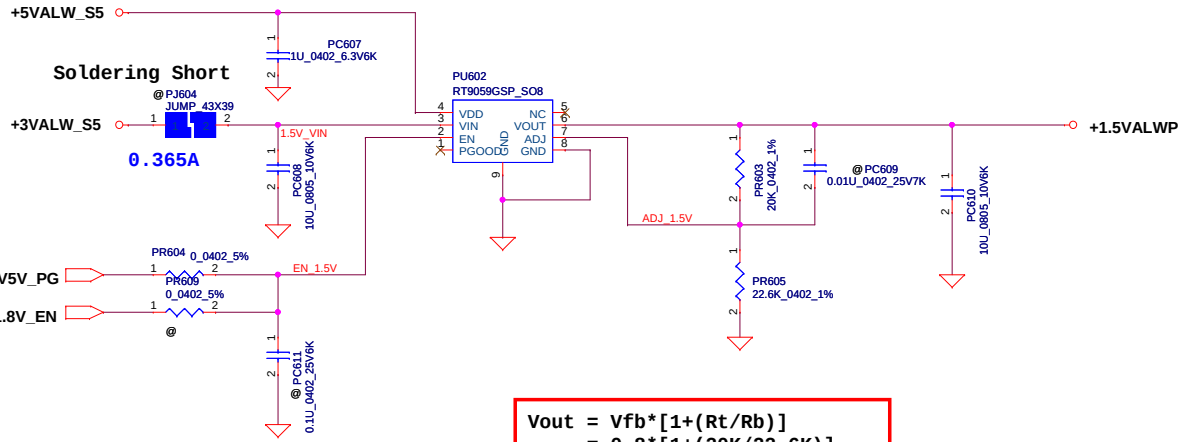
Vout = Vin*R2/(R1+R2)
= 3.3*[10K/42.4K]
= 0.7783V

+0.775VS
Imax=0.2A ;

RT9045:
Current Limit=1.8A(min)~3.5A(Max)
PD = (VIN - VOUT) x IOUT + VIN x IQ
PD(MAX)=(3.3-0.775)*0.2+3.3*2.5mA = 0.5132W
θ JA= 39.8°C/W
IQ+2.5mA
PD*θJA = 20.425°C



main source : RT9059GSP
second srouce: APL5933CKAI



+1.5VS
Ipeak=0.25A ;
Current Limit=3.1A(min)~3.6A(Typ)~4.2A(Max)

RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA,IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.453W
θ JA= 33.7°C/W*0.903=15.29°C

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(20K/22.6K)]
= 1.507V

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

Title: P46 PWR-0.775V/1.5V RT9045/9059

Size	Document Number	Rev
		0.1

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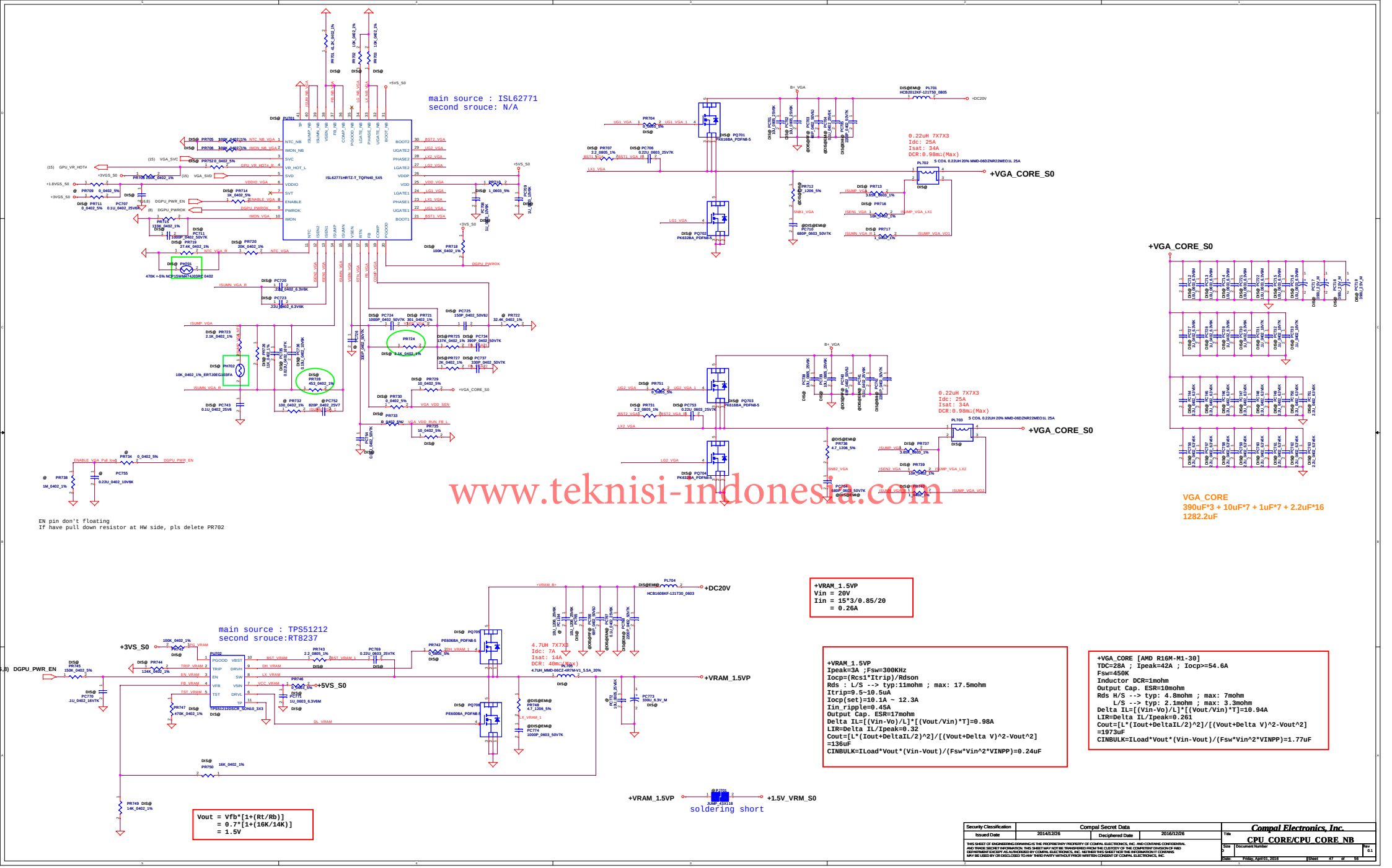

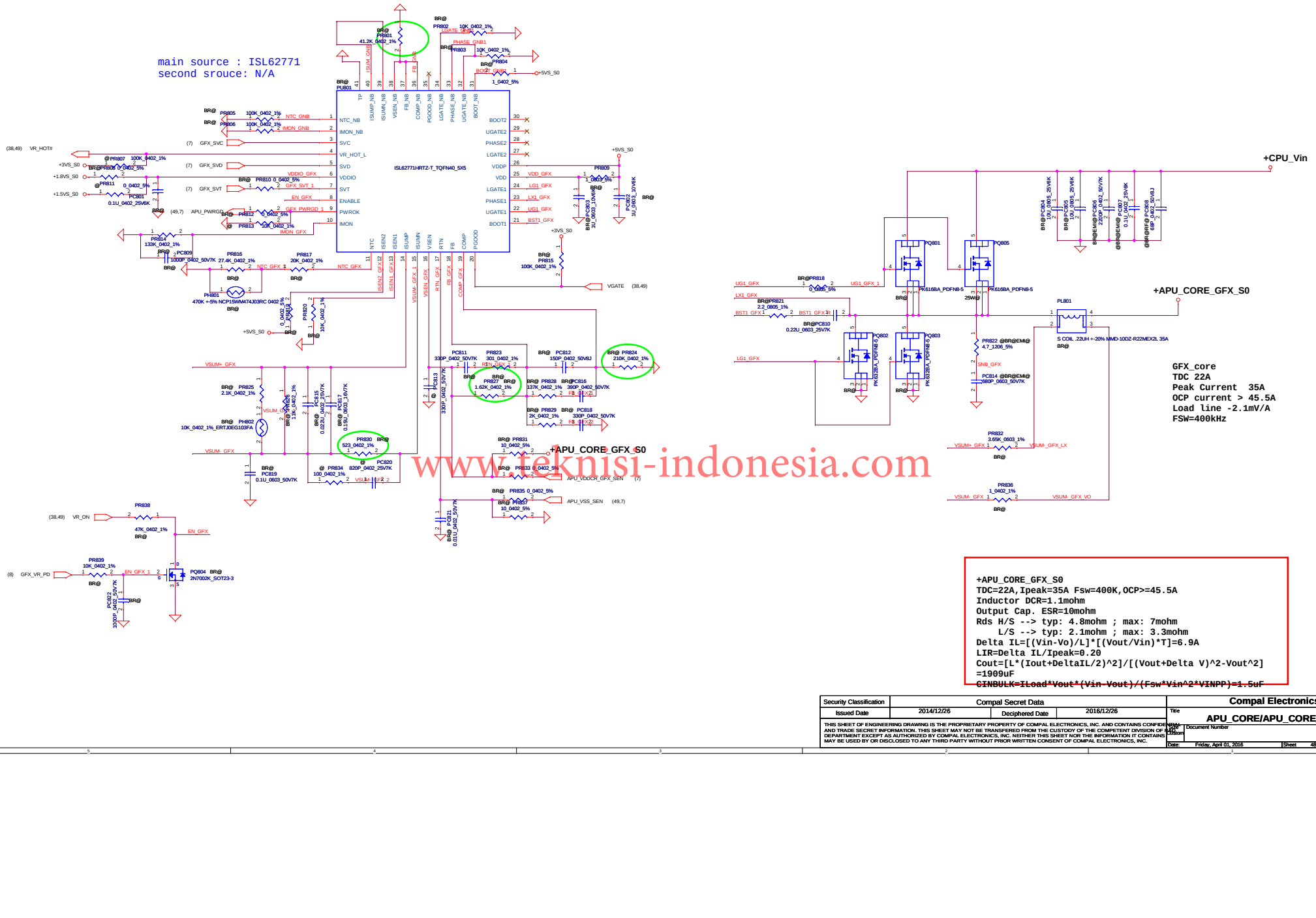

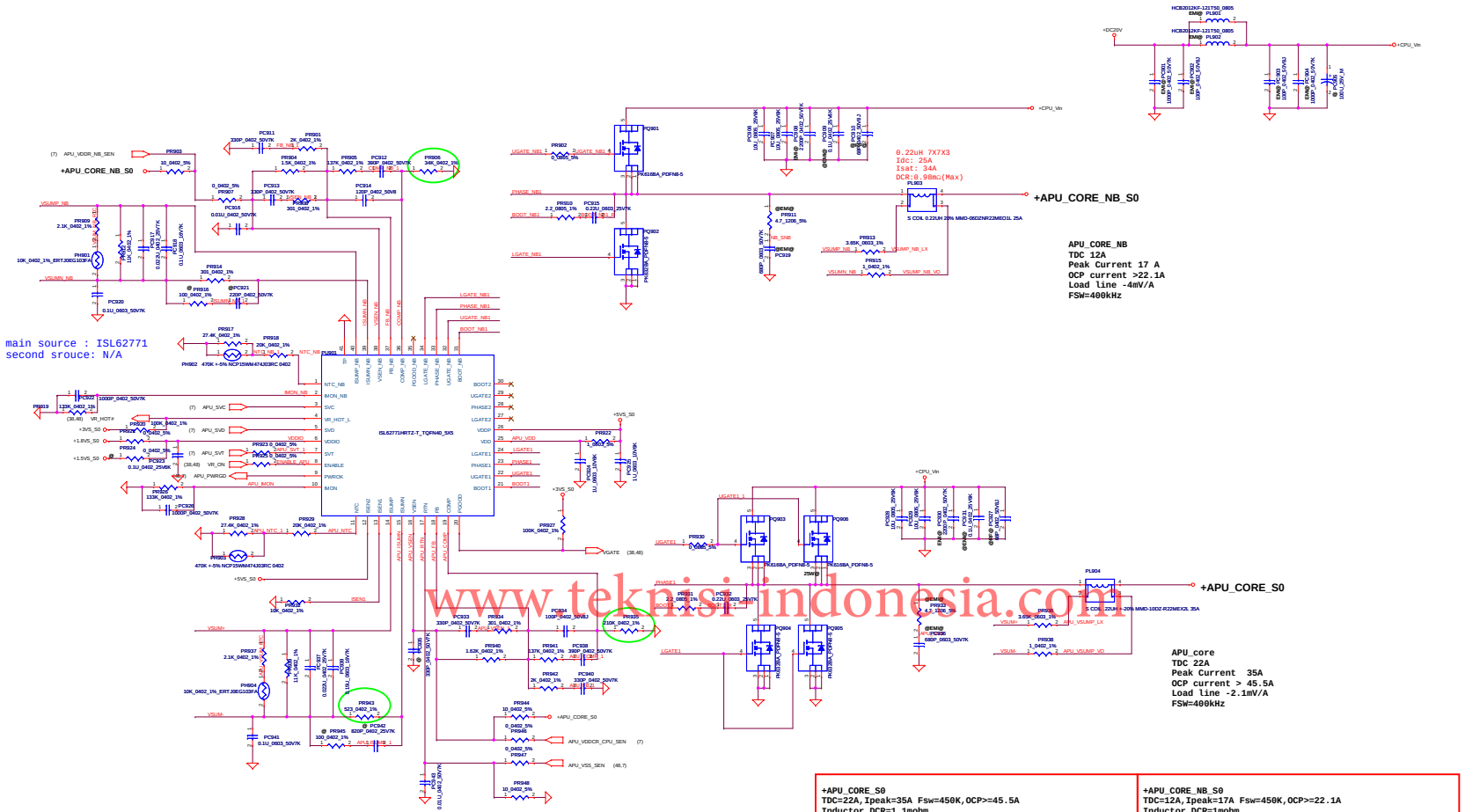

+APU_CORE_S0	+APU_CORE_NB_S0
TDC=22A,Ipeak=35A Fsw=450K,OCP>=45.5A	TDC=12A,Ipeak=17A Fsw=450K,OCP>=22.1A
Inductor DCR=1.1mohm	Inductor DCR=1mohm
Output Cap. ESR=10mohm	Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm	Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm	L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=8.565A	Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=12.54A
LIR=Delta IL/Ipeak=0.245	LIR=Delta IL/Ipeak=0.73
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =1293uF	Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =400.6uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.89uF	CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.82uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/12/26	Deciphered Date	2016/12/26
			Title: APU_CORE/APU_CORE_NB
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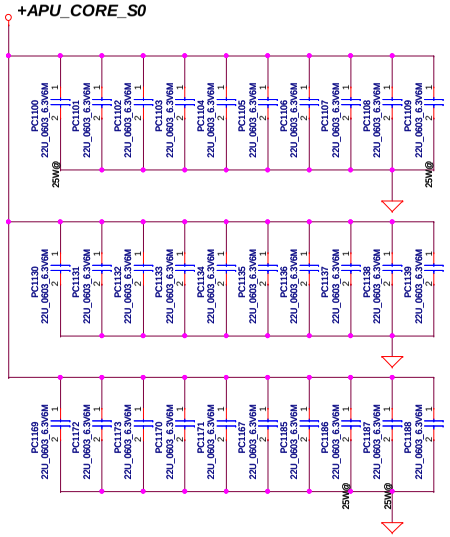
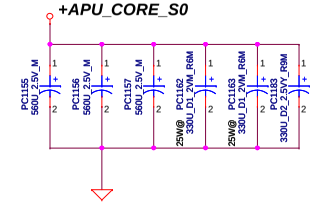
+APU_CORE_S0

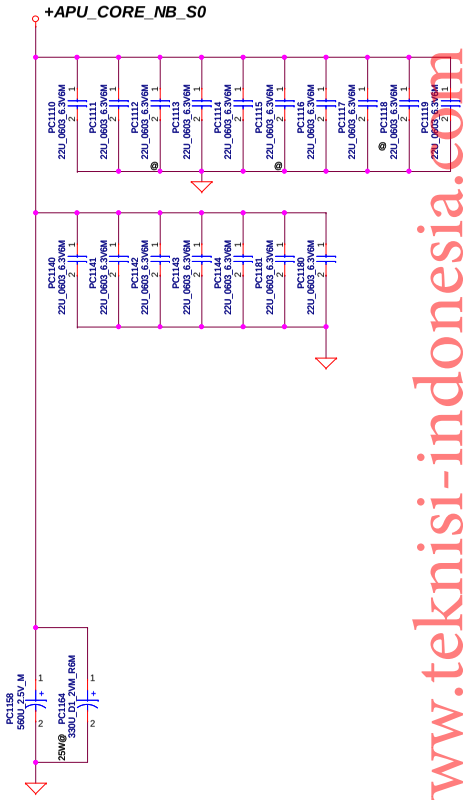




APU_CORE
560uF*3
330uF*1
22uF*26

APU_CORE(AMD SCL)
22uF*9
0.22uF*8
180pF*1

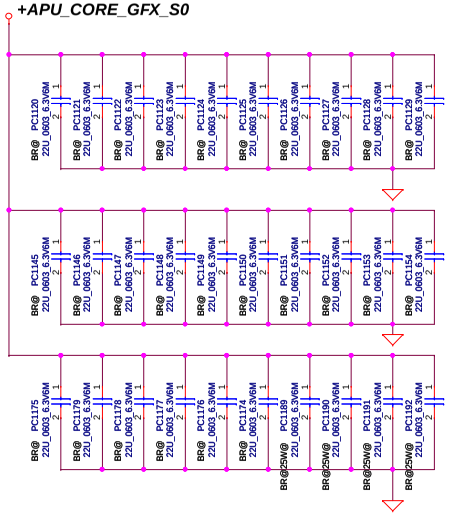
+APU_CORE_NB_S0

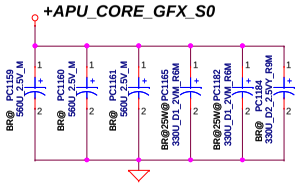


APU_CORENB
560uF*1
22uF*14

APU_CORENB(AMD SCL)
22uF*4
0.22uF*8
180pF*1

+APU_CORE_GFX_S0





GFX_CORE
560uF*3
330uF*1
22uF*26

GFX_CORE(AMD SCL)
22uF*9
0.22uF*9
180pF*1

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
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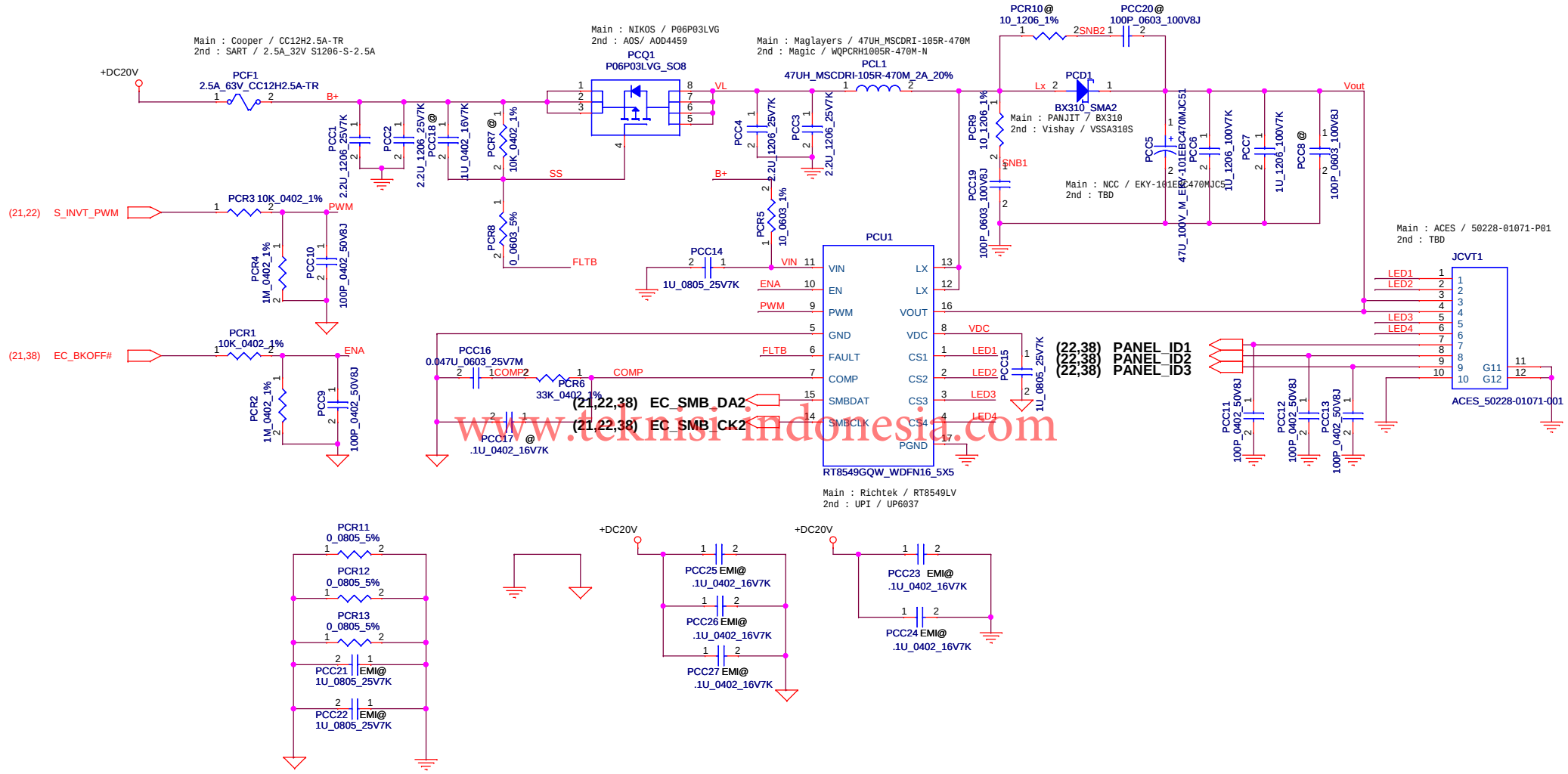
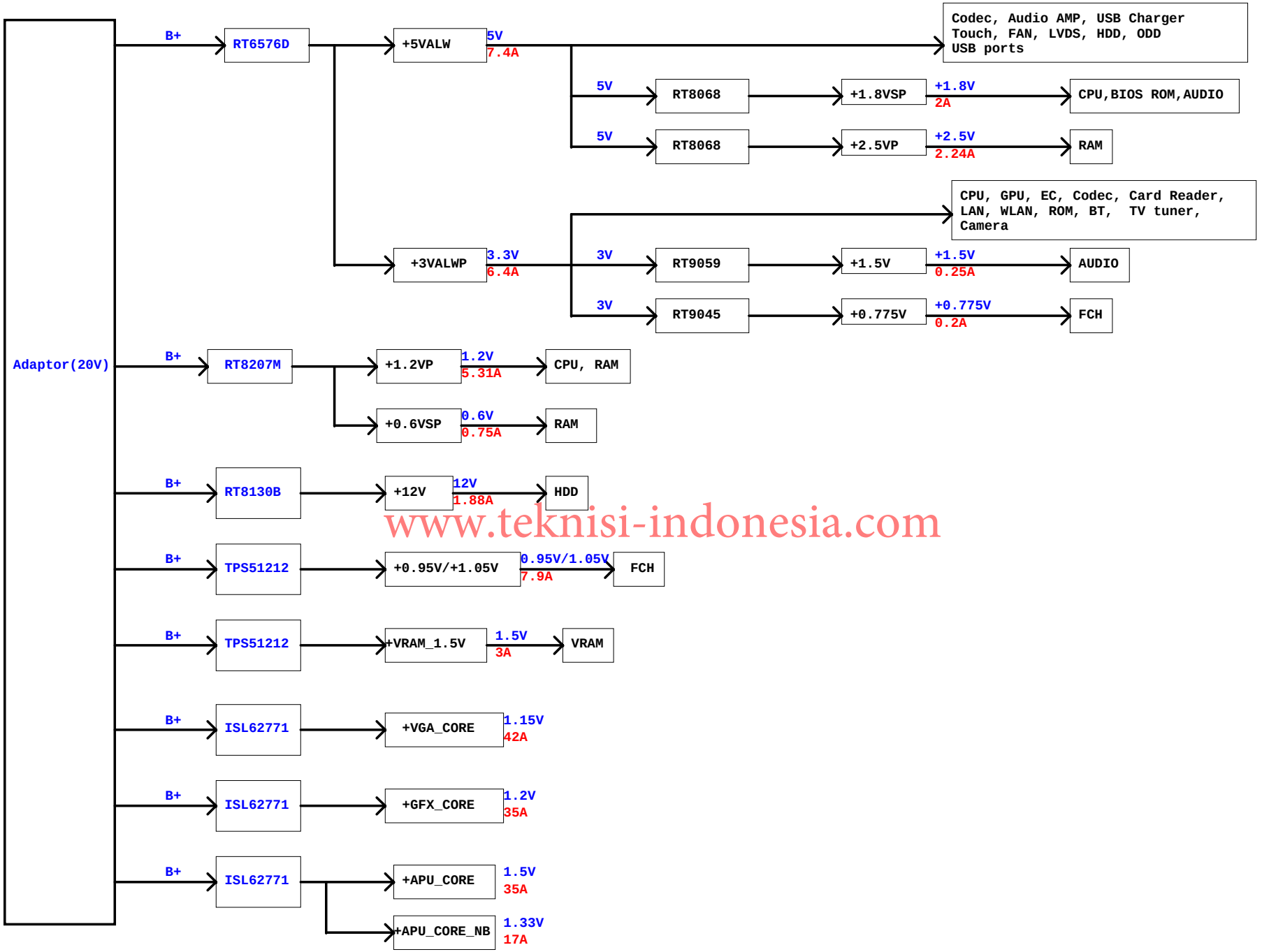


Security Classification	Compal Secret Data		
Issued Date	2015/11/25	Deciphered Date	2015/11/25

Compal Electronics, Inc.			
Title	CONVERTER/B		
Size B	Document Number LA-D952P M/B		Rev 0.1
Date:		Sheet 51 of 56	



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: **Power Rail**

Size	Document Number	Rev
Custom		0.1

Date: Friday, April 01, 2016 Sheet 52 of 56

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2016/02/03	P41_PWR-RT8207M(DDR4 VDDQ/VTT)	pop PC115	reduce ripple
		P44_VDDP_0.95V_1.05V (TPS51212)	pop PC409	reduce ripple
		P48_GFX_CORE(ISL62771) P49_APU_CORE(ISL62771)	change PL904,PL801 to 0.22uH 10*10*4 0.82mohm choke add PC1183,PC1184 330uF 9mohm SP-CAP PR943=523ohm, PR830=523ohm,PR827=1.62K, PR906=34K,PR824=210K,PR935=210K, change decoupling MLCC to 22uF 0603 pop PR920=100K	AMD VRM test modify VR_HOT# pull high
		P47 VGA_CORE/VRAM (ISL62771)	pop PR708=100K	GPU_VR_HOT# pull high
2	2016/02/18	P47 VGA_CORE/VRAM (ISL62771)	PR714=1K ohm, PR745=150K ohm , PC770=0.1u reserve PC1194 10U_1206_25V	VGA/VRAM Power Sequence reserve for VRAM Vin drop
		P44_VDDP_0.95V_1.05V (TPS51212) P42 PWR_3V/5V (RT6576)	reserve PC1193 10U_1206_25V PR220 unpop, PR221pop PR209 change to 10K	reserve for 0.95V Vin drop +3VL to RTC 3V5V_PG pull high for RT9059 EN

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/12	Deciphered Date	2012/08/12

Title	PWR_PIR		
Size	Document Number		Rev
Custom	B555 VAA15 LA-A072P MB		0.5
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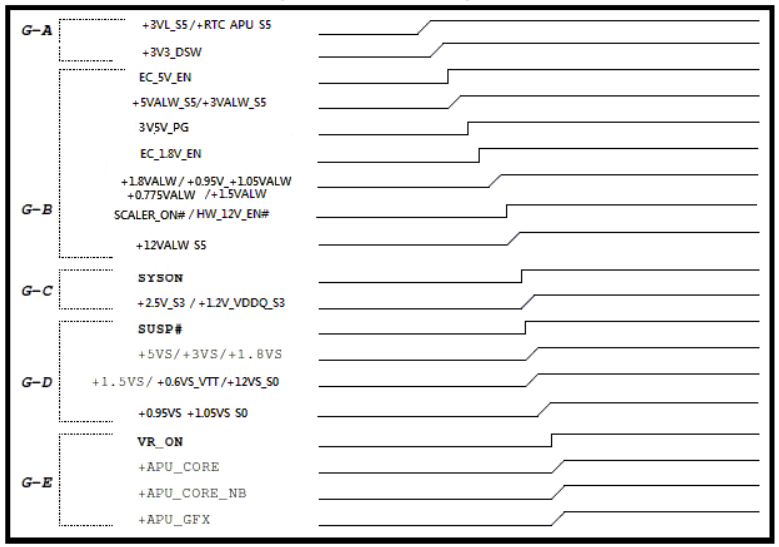
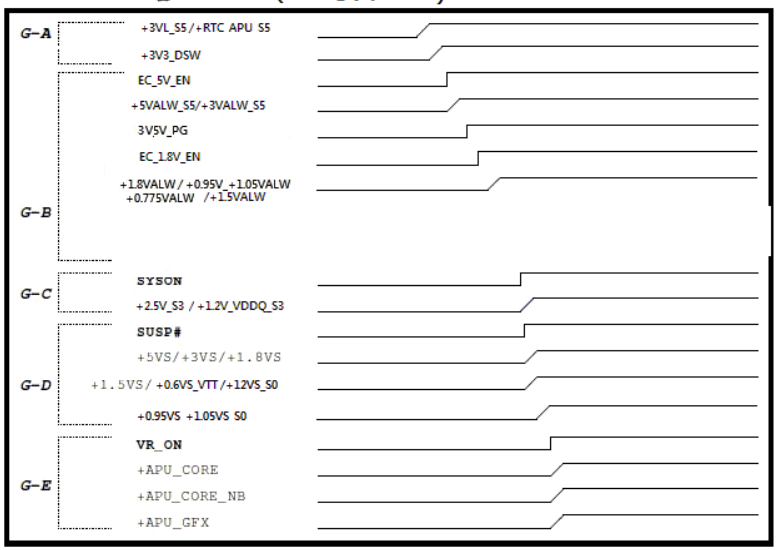
POWER SEQUENCE (For Scaler SKU)



POWER SEQUENCE (For CVT SKU)



Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.

Title: Power Sequence Timing

Size | Document Number: LA-D961P M/B | Rev: 0.1

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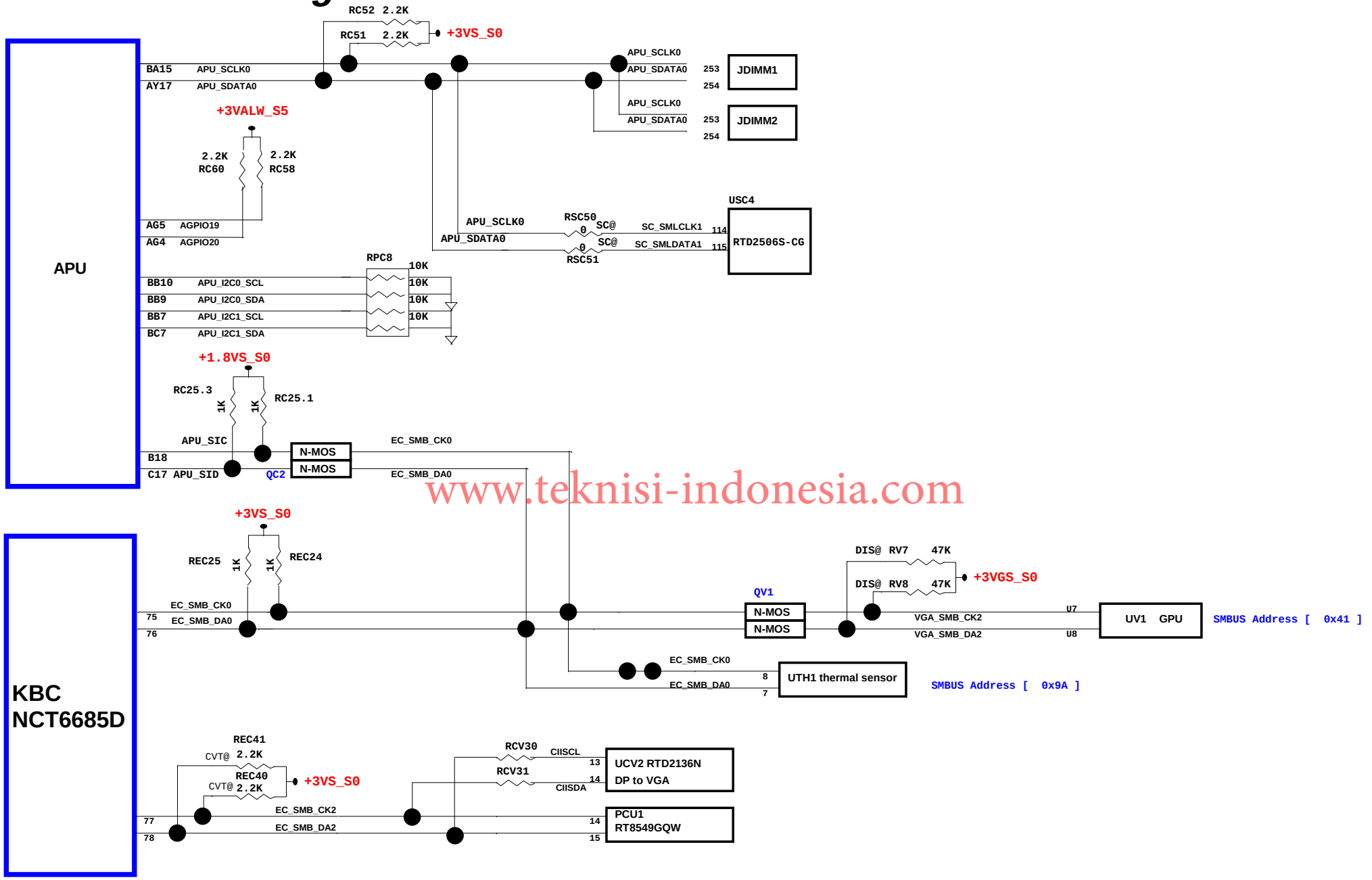
SMBus Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2015/01/23	Deciphered Date	2017/01/23

Compal Electronics, Inc.			
Title	SMBus block diagram		
Size	Document Number	LA-D961P M/B	Rev 0.1
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HW PIR (Product Improve Record)

Note Color *Version change list (P.I.R. List)* *EVT to DVT for HW*

Item	Page	Modify List	Reason for change	Date
1	7	QC2 change to 2xBSS138 QC4/QC6 / Remove QC3		
2	7	Remove UC12 , add RC20 on DP0_HPD		
3	7	Remove RC9/RC20 change to idepedent resistor		
4	7	RC24 change to pop / RC26 change to non-pop		
5	8			
6	8			
7	8	TPM_STSIRQ# change to AGPIO6	TPM Voltage level is S5	
8	10	+1.8VS_S0_Cap :Remove CC99	(AMD SCL check list updated)	
9	10	The VDDP_GFX Power Rail change to +VDDP_GFX_S0	Rename and VDDP_GFX power rail only use on Bristol	
10	10	Remove CC163 (+RTC_APU_S5 Cap)	follow AMD SCH CKL	
11	22	Add RPSC1 for Panel ID pull-high		
12	22	+3V_SCA_R use Power switch USC5	MOSFET switch have power leakage ,change to Load switch	
13	22	Add Panel_ID4 on Pin34	For C5/C4 panel detect	
14	22	Add HDMI_CABLE_DET# on Pin44	For HDMI-IN S5 Mode wake up , connect to SCALAR and EC .	
15	22	Add SCA_FW_FLASH on Pin43	For SCALAR FW FLASH to announce CPU	
16	22	Add RSC45 / RSV50 pull-high for SC_SML		
17	22	Remove RSC50/RSC51 ,add QSC4 for SC_SMLCLK/DATA1	Level shift	
18	22	EDP_AUXP/N swap	for error pin define	
19	24	Add RHI16 for Customer requier		
20				
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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/23	Deciphered Date	2017/01/23
Title	HW-PIR		
Size	Document Number		Rev
	LA-D961P M/B		0.1
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