

LKL-1 17821 Kabylake-U Schematics

2018-01-12

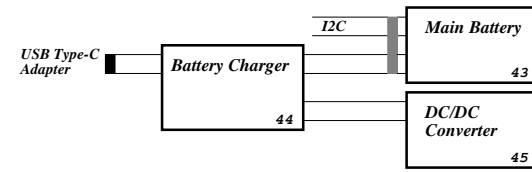
REV : 2A

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BOM1

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title COVER PAGE		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018		Sheet 1 of 105

Revision: SC



BOB1		緯創資通 Wistron Corporation 21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsiehli, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLOCK DIAGRAM			
Size A2	Document Number	Rev 2A	
Date: Friday, January 19, 2018		Sheet 2 of	105
LKL-1			

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title **RESERVED**

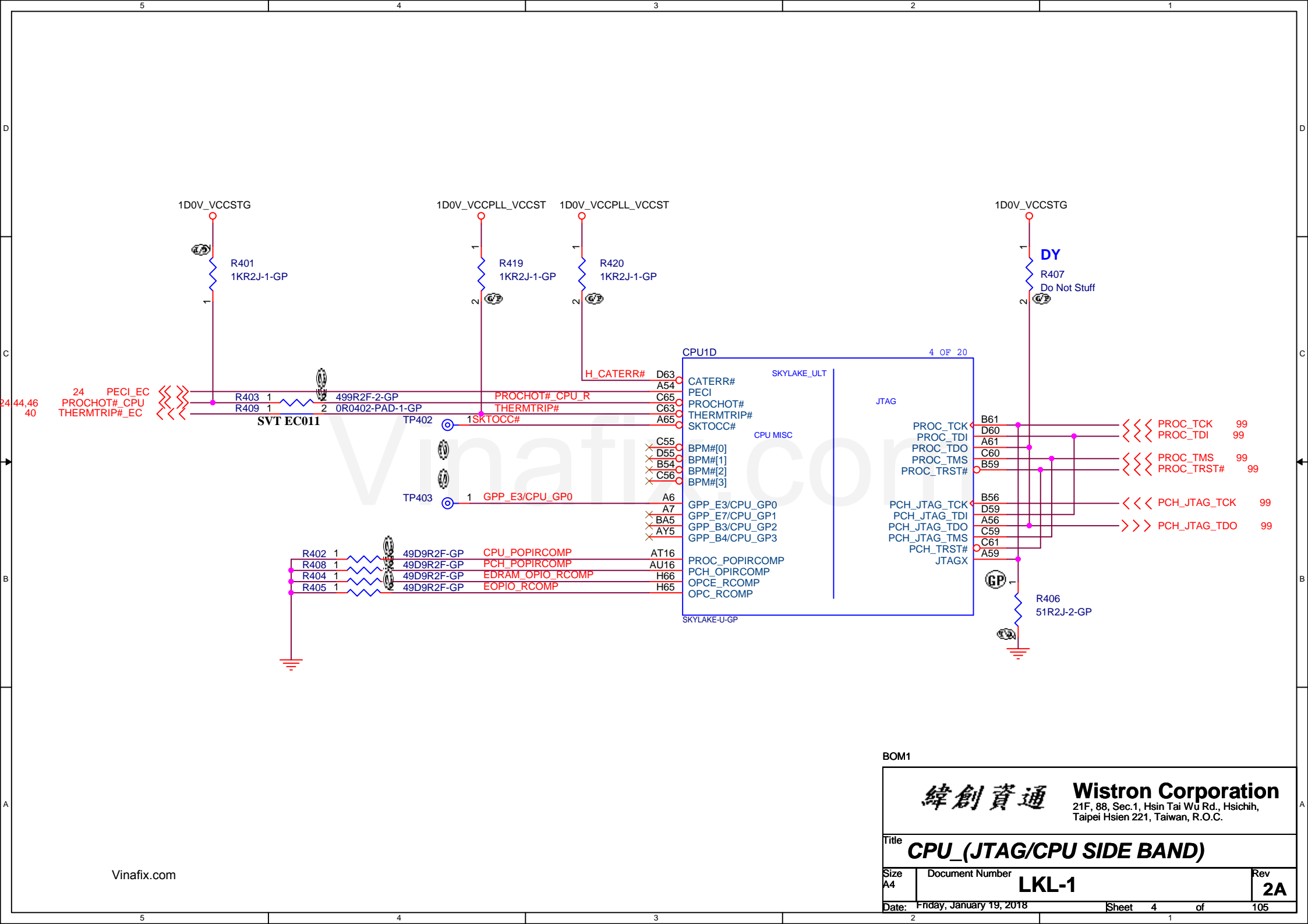
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Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 3 of 105



BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title CPU_(JTAG/CPU SIDE BAND)		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018		
Sheet 4 of 105		

DDR4 ball type: Interleaved Type

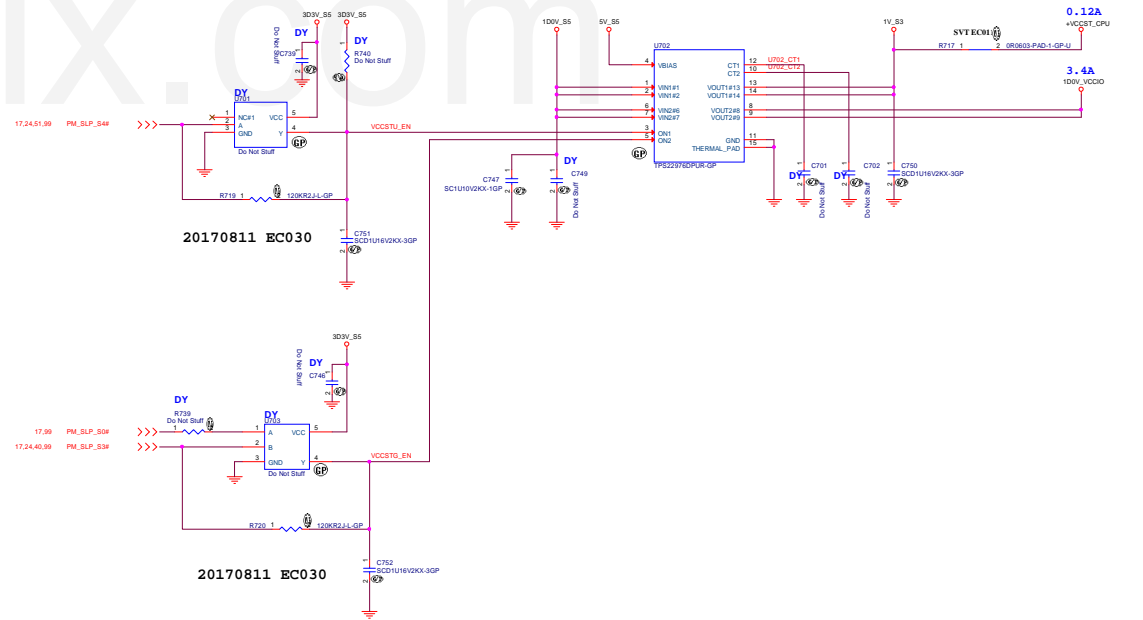
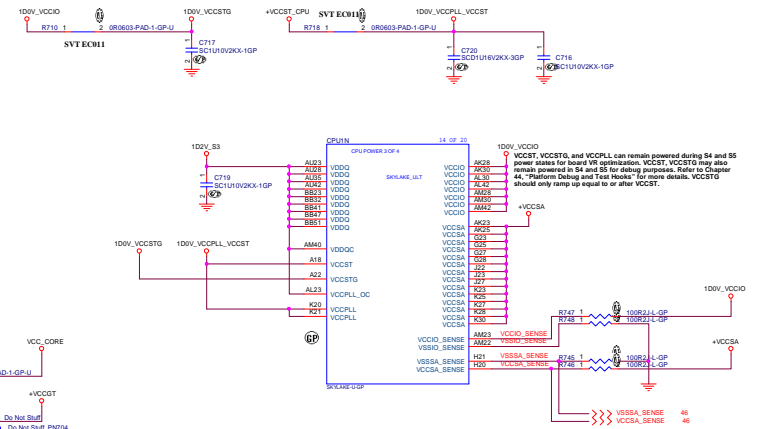
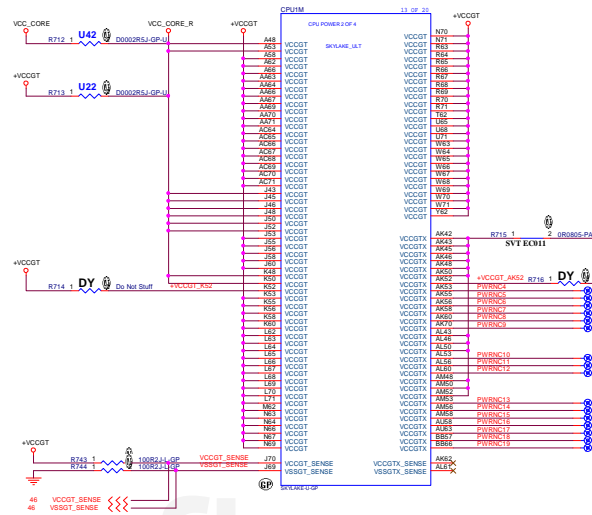
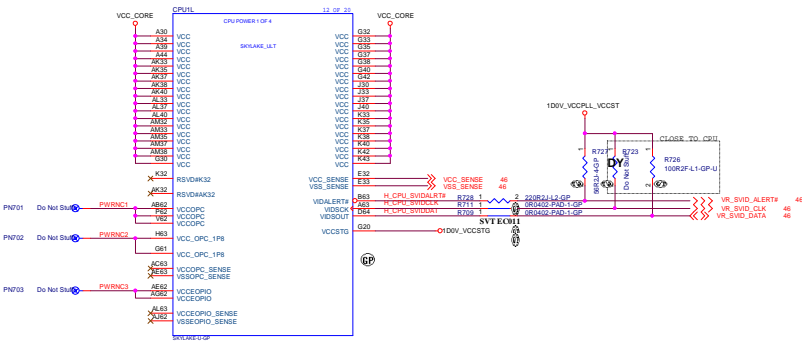
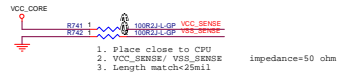


Diagram showing the connection of the XDP R604 1KR2J-1-CP component to the CF33 pin header. The component has two pins: pin 1 is connected to the CF33 header, and pin 2 is connected to ground. The CF33 header is labeled with the text "[BDW Only] PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)".

The diagram shows a circuit for the Display Port Presence Strap. A red wire labeled 'CFG4' is connected to pin 1 of a resistor. The resistor is labeled 'R605 1KR2J-1-GP'. The other end of the resistor is connected to pin 2, which is also connected to ground (indicated by a ground symbol).

DISPLAY PORT PRESENCE STRAP	
CFG[4]	<p>U : ENABLED An external Display Port device is connected to the Embedded Display Port.</p> <p>1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.</p>



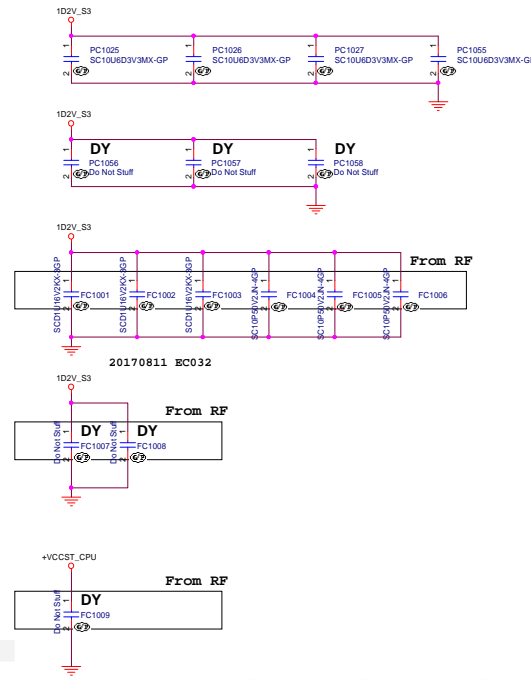
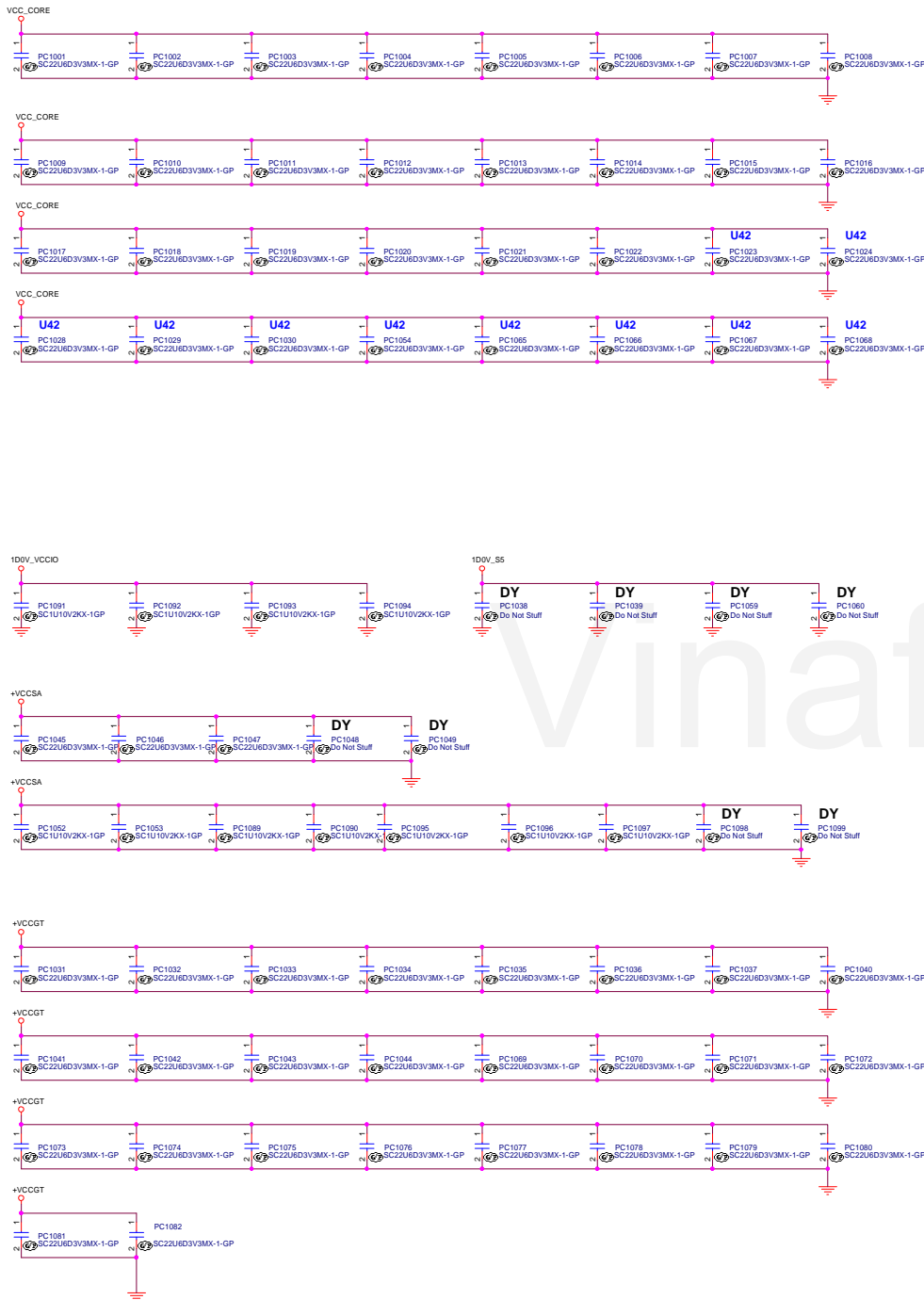


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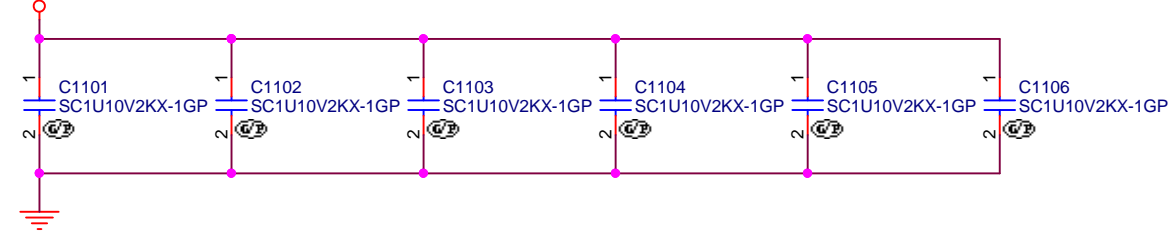
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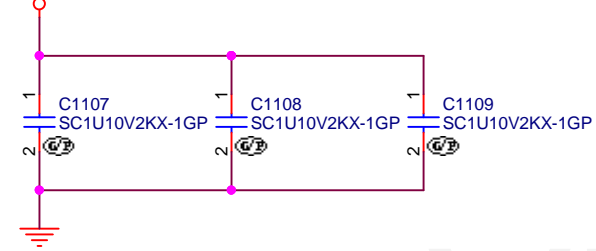
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title CPU (RESERVED)		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018		Sheet 9 of 105



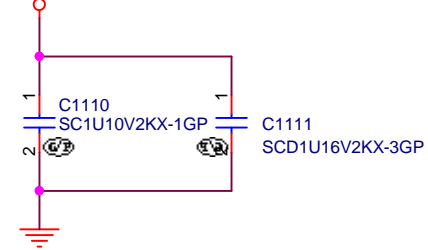
VCC_CORE



+VCCGT



+VCCSA



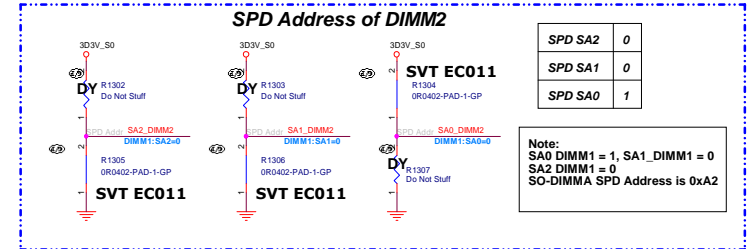
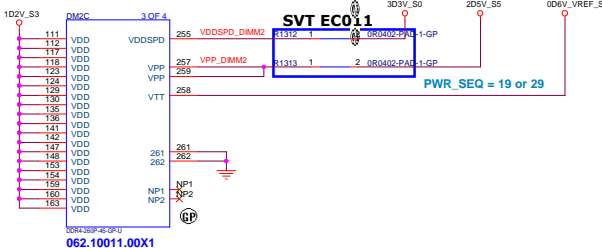
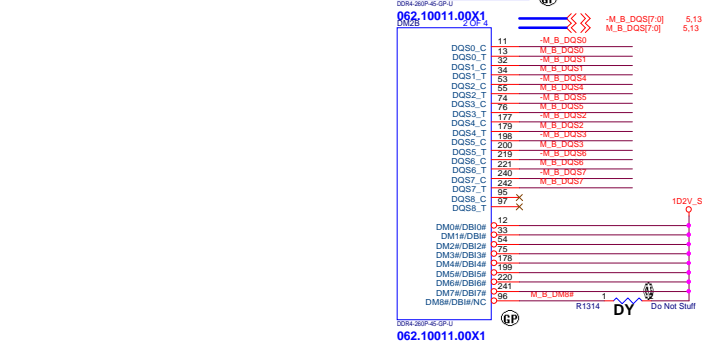
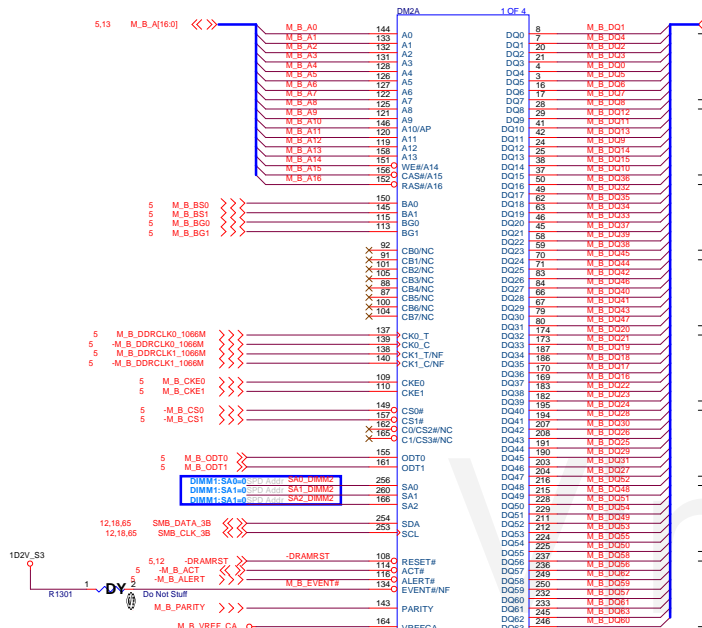
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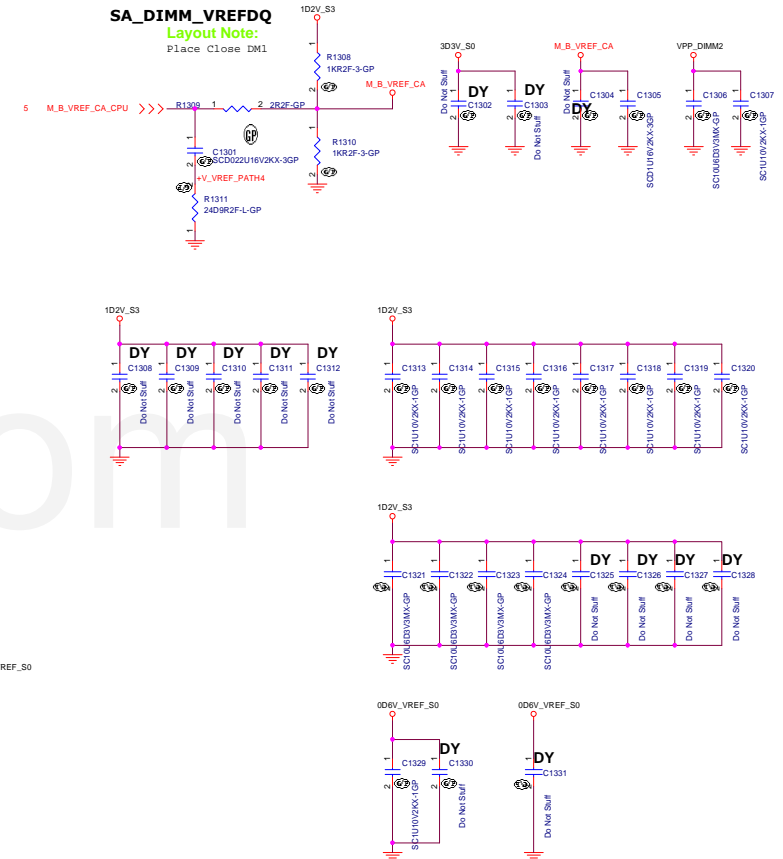
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title CPU (POWER CAP2)	
Size A4	Document Number LKL-1
Date: Friday, January 19, 2018	Sheet 11 of 105
Rev 2A	



D00	8	M_B_D01	»»	M_B_DQ[83:0]	513
D00	7	M_B_D04			
D01	20	M_B_D05			
D02	21	M_B_D05			
D03	4	M_B_D06			
D04	3	M_B_D06			
D05	16	M_B_D06			
D06	17	M_B_D07			
D07	28	M_B_D08			
D08	29	M_B_D012			
D09	29	M_B_D011			
D10	42	M_B_D013			
D11	24	M_B_D014			
D12	25	M_B_D014			
D13	38	M_B_D015			
D14	37	M_B_D015			
D15	50	M_B_D038			
D16	49	M_B_D038			
D17	62	M_B_D035			
D18	63	M_B_D034			
D19	46	M_B_D035			
D20	45	M_B_D037			
D21	58	M_B_D038			
D22	59	M_B_D038			
D23	70	M_B_D039			
D24	71	M_B_D014			
D25	83	M_B_D042			
D26	84	M_B_D048			
D27	66	M_B_D049			
D28	67	M_B_D047			
D29	75	M_B_D053			
D30	80	M_B_D047			
D31	174	M_B_D051			
D32	175	M_B_D021			
D33	187	M_B_D019			
D34	186	M_B_D015			
D35	170	M_B_D017			
D36	169	M_B_D015			
D37	183	M_B_D022			
D38	182	M_B_D022			
D39	195	M_B_D024			
D40	184	M_B_D028			
D41	207	M_B_D029			
D42	208	M_B_D029			
D43	191	M_B_D025			
D44	180	M_B_D025			
D45	203	M_B_D041			
D46	204	M_B_D041			
D47	216	M_B_D062			
D48	215	M_B_D048			
D49	229	M_B_D050			
D50	229	M_B_D054			
D51	211	M_B_D052			
D52	212	M_B_D053			
D53	224	M_B_D055			
D54	225	M_B_D055			
D55	237	M_B_D058			
D56	236	M_B_D058			
D57	249	M_B_D062			
D58	250	M_B_D059			
D59	237	M_B_D057			
D60	233	M_B_D061			
D61	240	M_B_D061			
D62	246	M_B_D059			



SA_DIMM_VREFDQ
Layout Note:
Place Close DM1



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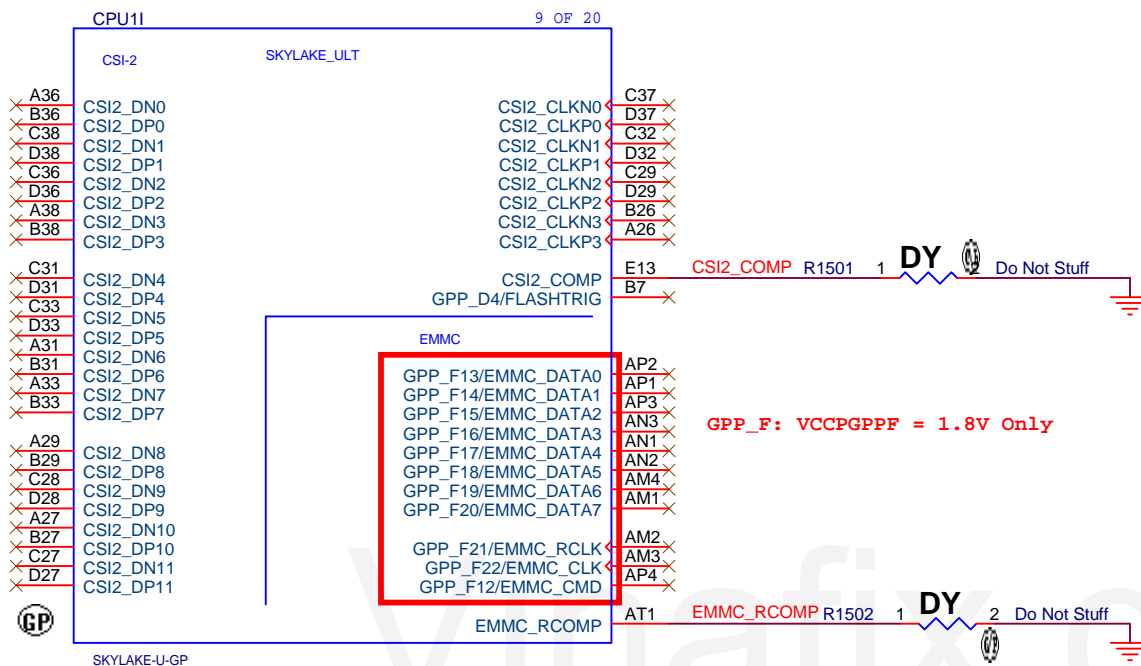
Size
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Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 14 of 105



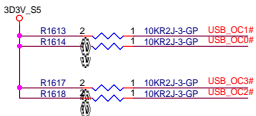
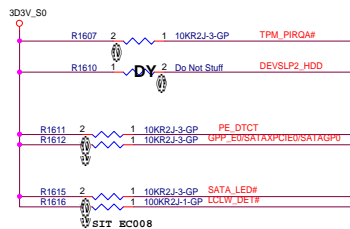
BOM1

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Title CPU (CSI2/EMMC)

Size A4 Document Number LKL-1 Rev 2A

Date: Friday, January 19, 2018 Sheet 15 of 105

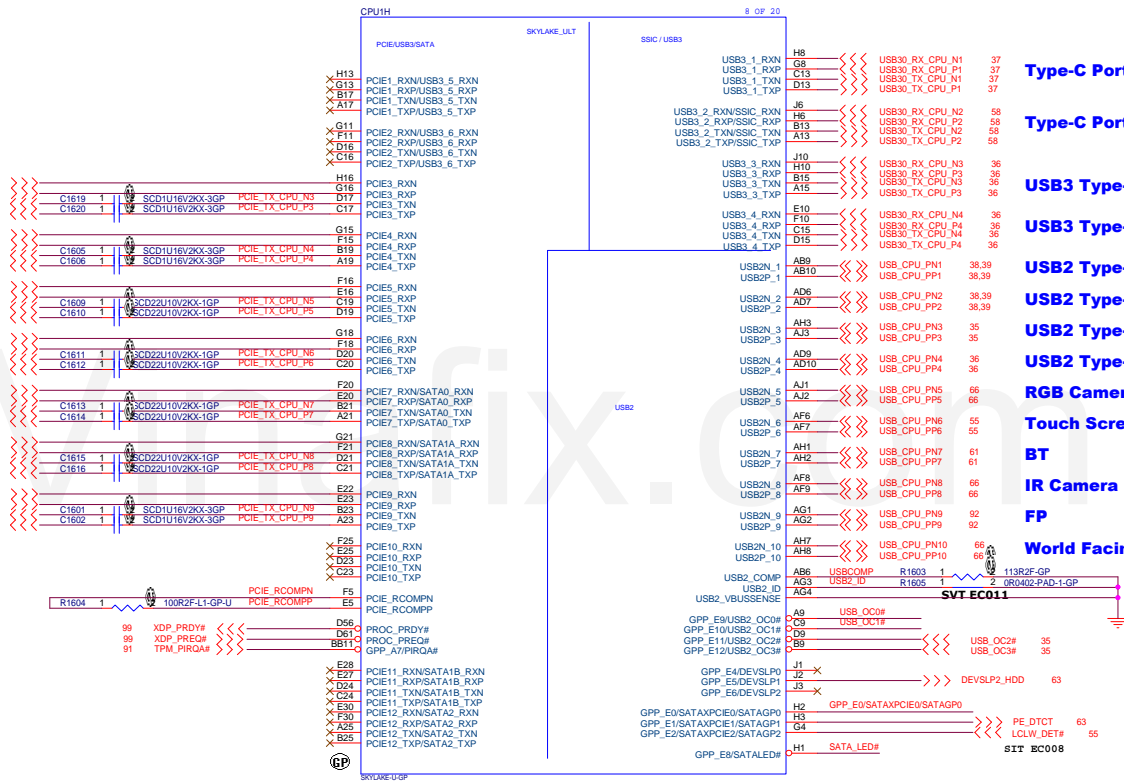


NGFF WLAN

LAN

M.2 PCIe SSD

CARD READER



Type-C Port1

Type-C Port2

USB3 Type-A (AOU)

USB3 Type-A

USB2 Type-C

USB2 Type-C

USB2 Type-A (AOU)

USB2 Type-A

RGB Camera

Touch Screen

BT

IR Camera

FP

World Facing Camera

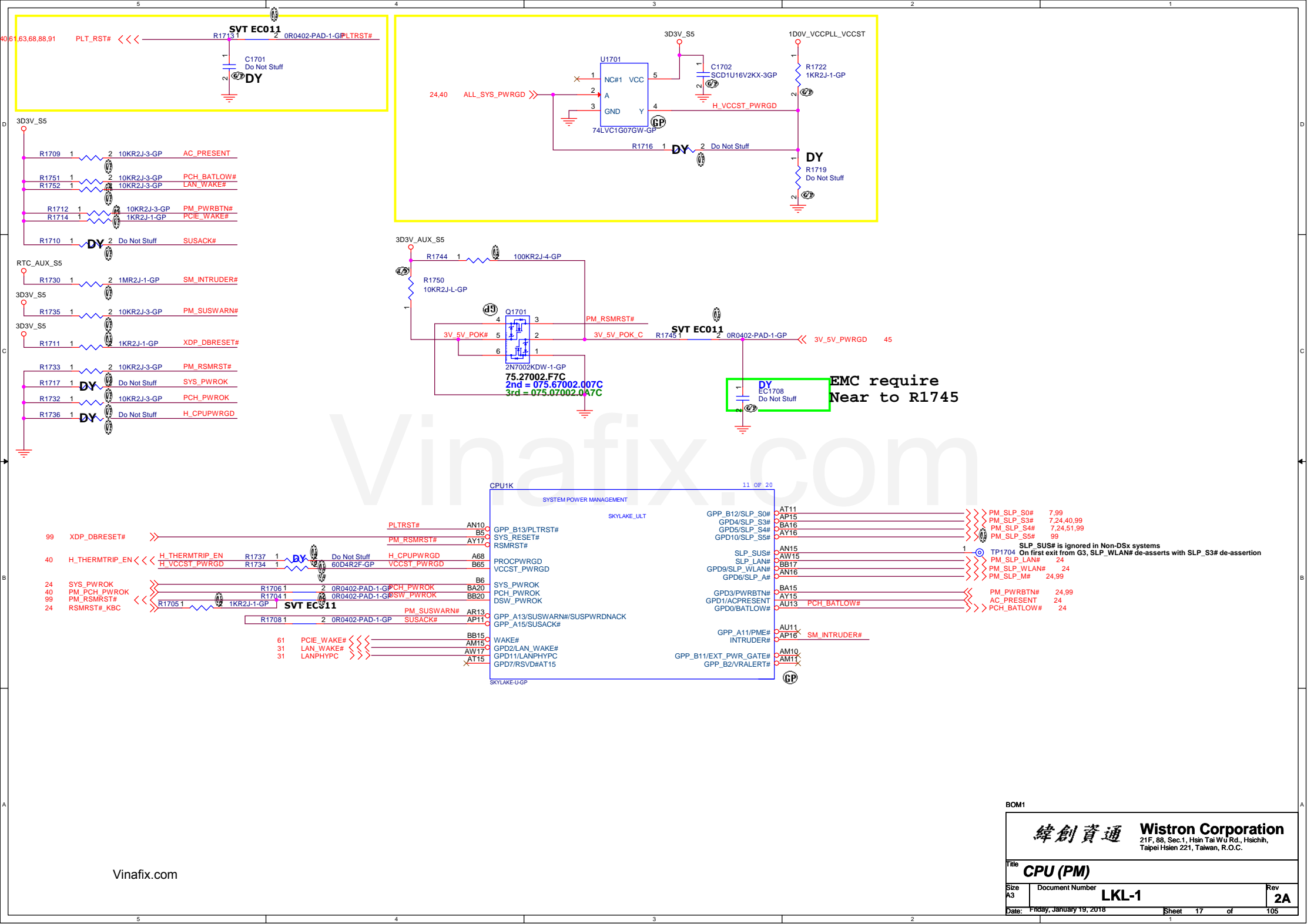
USB30 Configure

Pair	Device
1	Type-C Port1
2	Type-C Port2
3	USB3.0 Port1 (AOU)
4	USB3.0 Port2
5	NA
6	NA

USB20 Configure

Pair	Device
1	Type-C
2	Type-C
3	USB3.0 Port1 (AOU)
4	USB3.0 Port1
5	RGB Camera
6	Touch Screen
7	BT
8	IR Camera
9	Finger Print
10	World Facing Camera

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PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

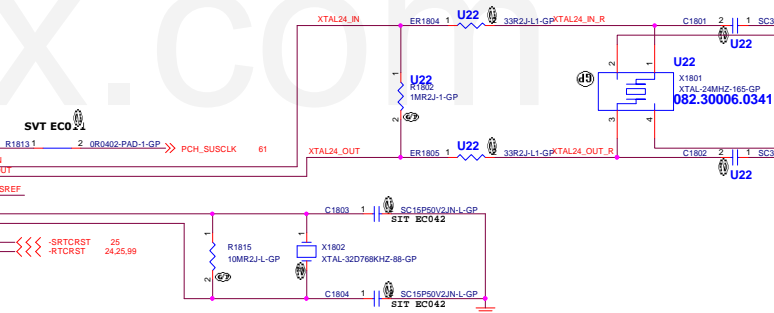
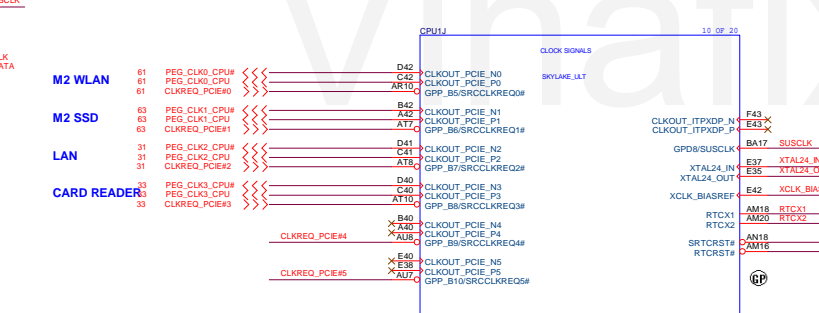
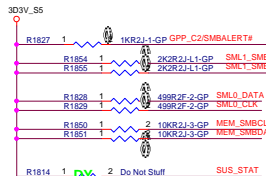
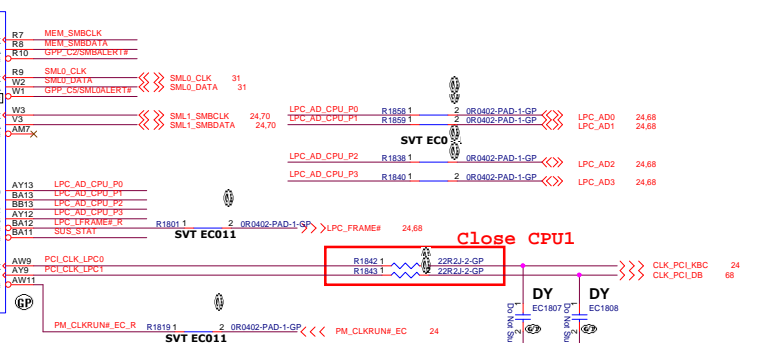
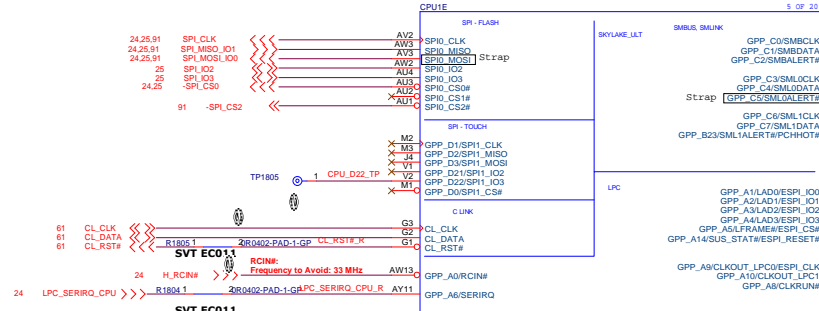
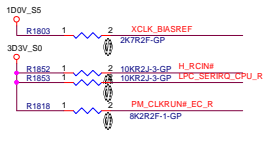
This signal has a weak internal pull-up.

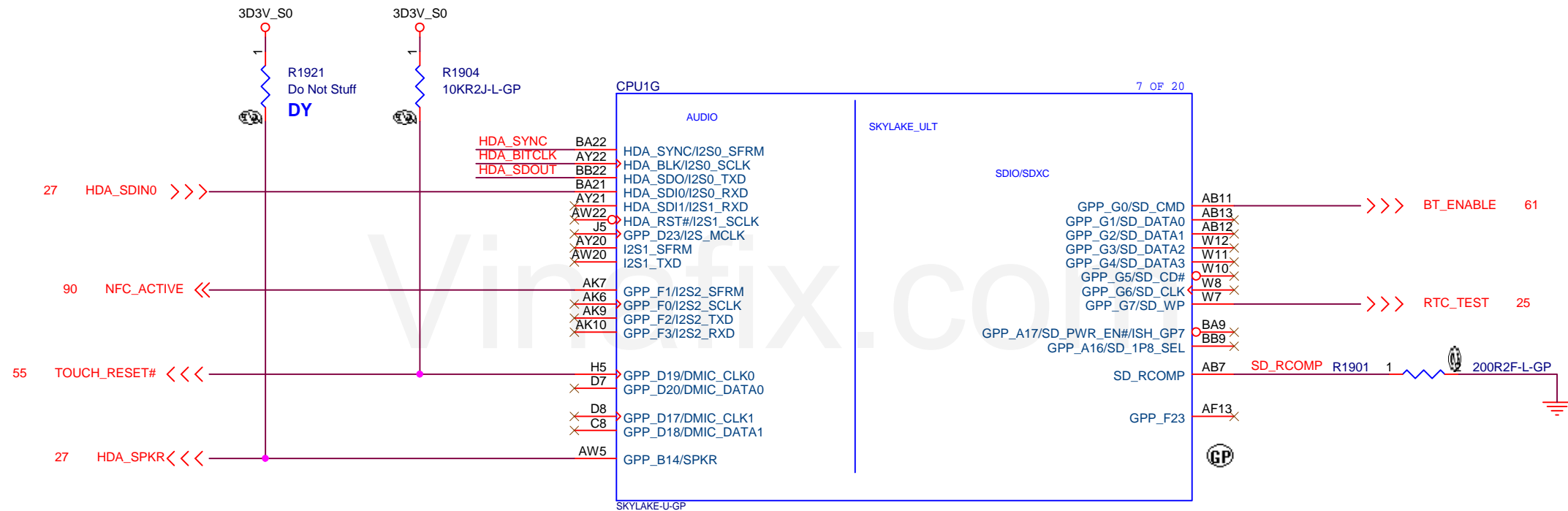
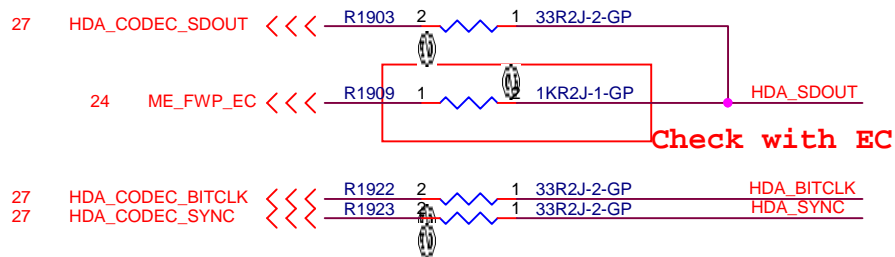


PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

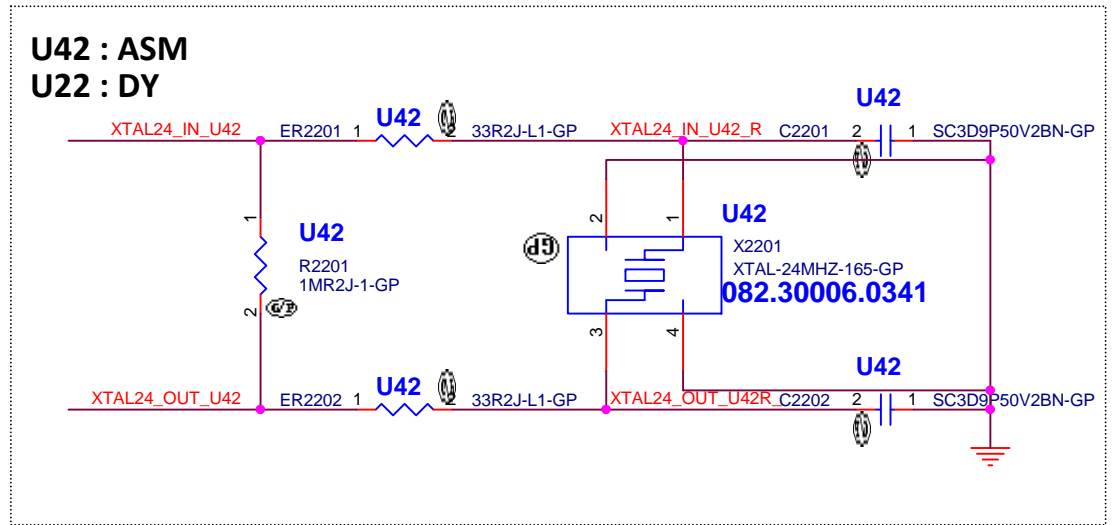
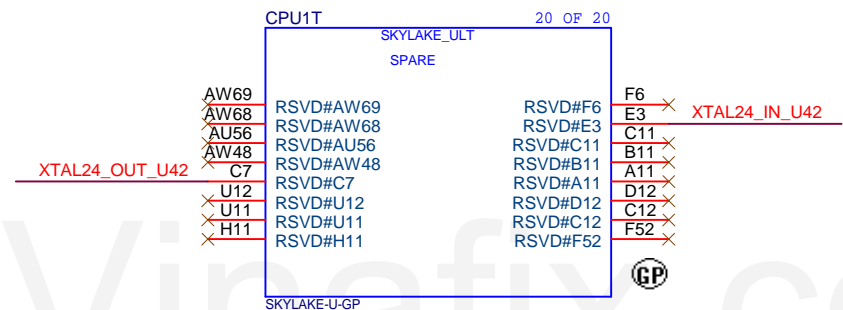
This signal has a weak internal pull-down.





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Title CPU (HDA/SDIO/SDXC)		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018	Sheet 19	of 105



BOM1			
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Title CPU (RSVD)			
Size A4	Document Number LKL-1		Rev 2A
Date:	Friday, January 19, 2018	Sheet 22 of	105



SSID = KBC

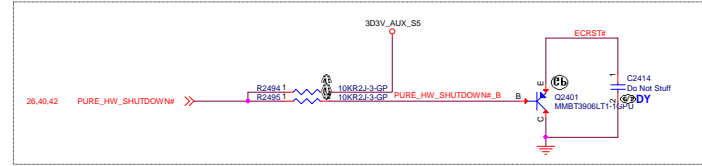
0922 SVT EC005

KBC PN: 071.00288.0A0G

MODEL_ID (PIN 96)	Full Down(R2449)	Full High (R2448)	Voltage
LKL YOGA	non-vPRO	100.0K	10.0K 2.75V
LKL Clamshell	non-vPRO	100.0K	33.0K 2.481V
	vPRO	100.0K	47.0K 2.245V
	non-vPRO	100.0K	64.9K 2.001V
	vPRO	100.0K	76.8K 1.867V
	non-vPRO	100.0K	100.0K 1.650V
			143.0K 1.358V

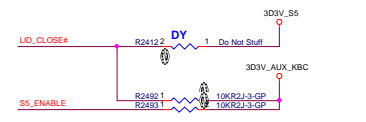
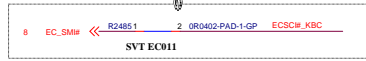
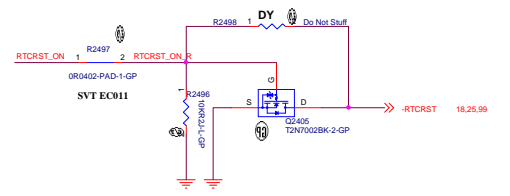
BOM CTRL

PCB VER (PIN 98)	Full Down R2419	Full High R2418	Voltage
SA	100.0K	10.0K	3V
SB	100.0K	20.0K	2.75V
SD	100.0K	33.0K	2.481V
SE	100.0K	47.0K	2.245V
SF	100.0K	64.9K	2.001V
SF	100.0K	76.8K	1.867V
-1 SIT-R	100.0K	100.0K	1.650V
-1M SVT	100.0K	143.0K	1.358V
-1N	100.0K	191.0K 64.19135.6DL	1.134V

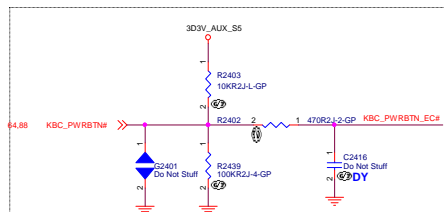
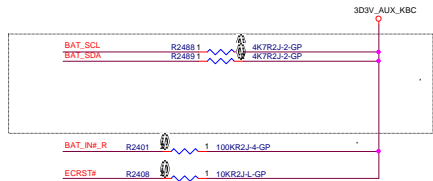


NOTE:
Please be aware that the SPI interface trace length between PC1 and EC should not exceed 650mm. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500ns.

NOTE:
Locate resistors R2415 and R2417 close to the U2401.



EC GPIO standard PH/PL



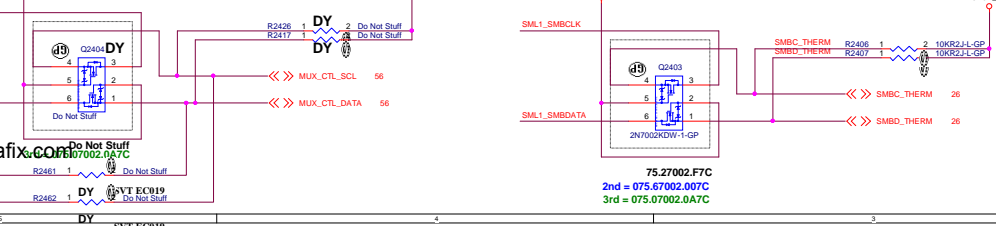
NOTE:
Please place R2410 close to AGND pin.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

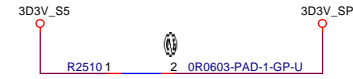
NOTE:
C2412 must place close to VCORF pin.

NOTE:
PWM Signal:
1. If missed, select alternative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

GPIO42	LID_CLOSE#	NB Lid function
GPIO80	SENSOR_LID_OPEN#	Tablet detect function

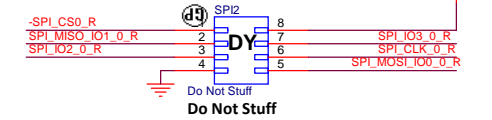


(EOL)	16MB SOIC8 (U2101)	Common WPN	LRV2 vPro BIOS	LRV2 non-vPro BIOS
	WINBOND W25Q128FVSIQ	72.25128.0E1	072.25128.0AC1	072.25128.0A81
	WINBOND W25Q128JVSQ	072.25128.0B71	072.25128.0B61	072.25128.0B51
	MACRONIX MX25L12873FM2I-10G	72.12873.001	072.25128.0B21	072.25128.0B11
	MICRON N25Q128A13ESEDFF	072.25128.0R01	072.25128.0B41	072.25128.0B31



SVT EC011

SPI ROM Socket (SPI2)

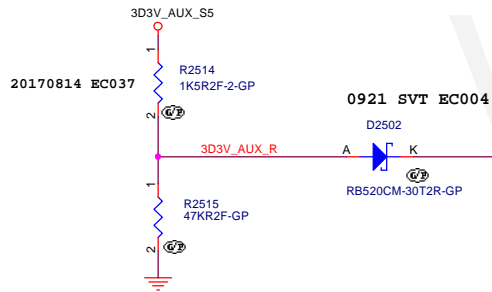
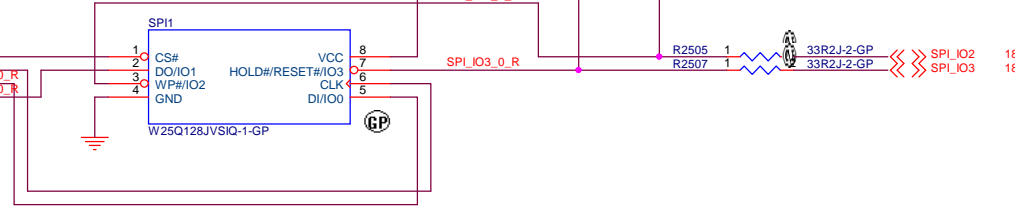


Co-Layout Design on SPI1

TABLE

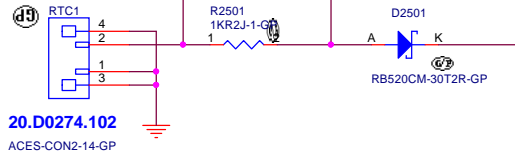
SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D2101.K	GND	GND	2		
3	CS#	R2104.2	CLK	CLK	4		
5	MISO	R2109.2	R2108.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

18,24
8,24,91
24,91
24,91

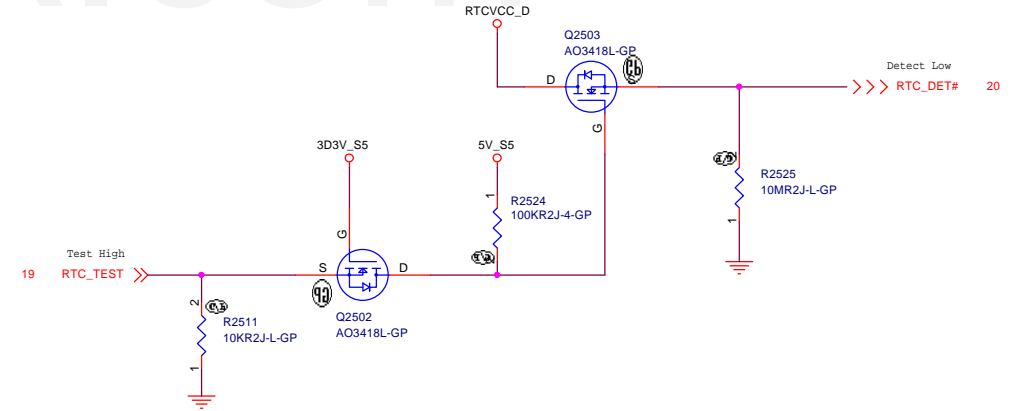
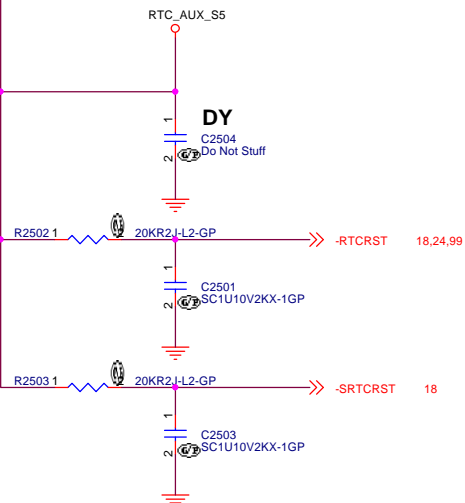


0921 SVT EC004

RTC CONN



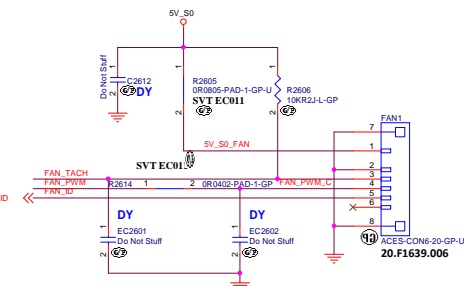
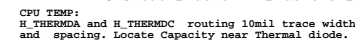
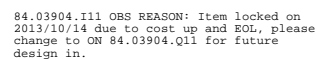
20.D0274.102
ACES-CON2-14-GP



BOM1

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Title			
FLASH/RTC			
Size A3	Document Number LKL-1		Rev 2A
Date:	Friday, January 19, 2018	Sheet 25 of	105

MVP_PWRGD_THERM



signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

$$5V * 100K / (100K + 40K) = 3.57V$$

OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

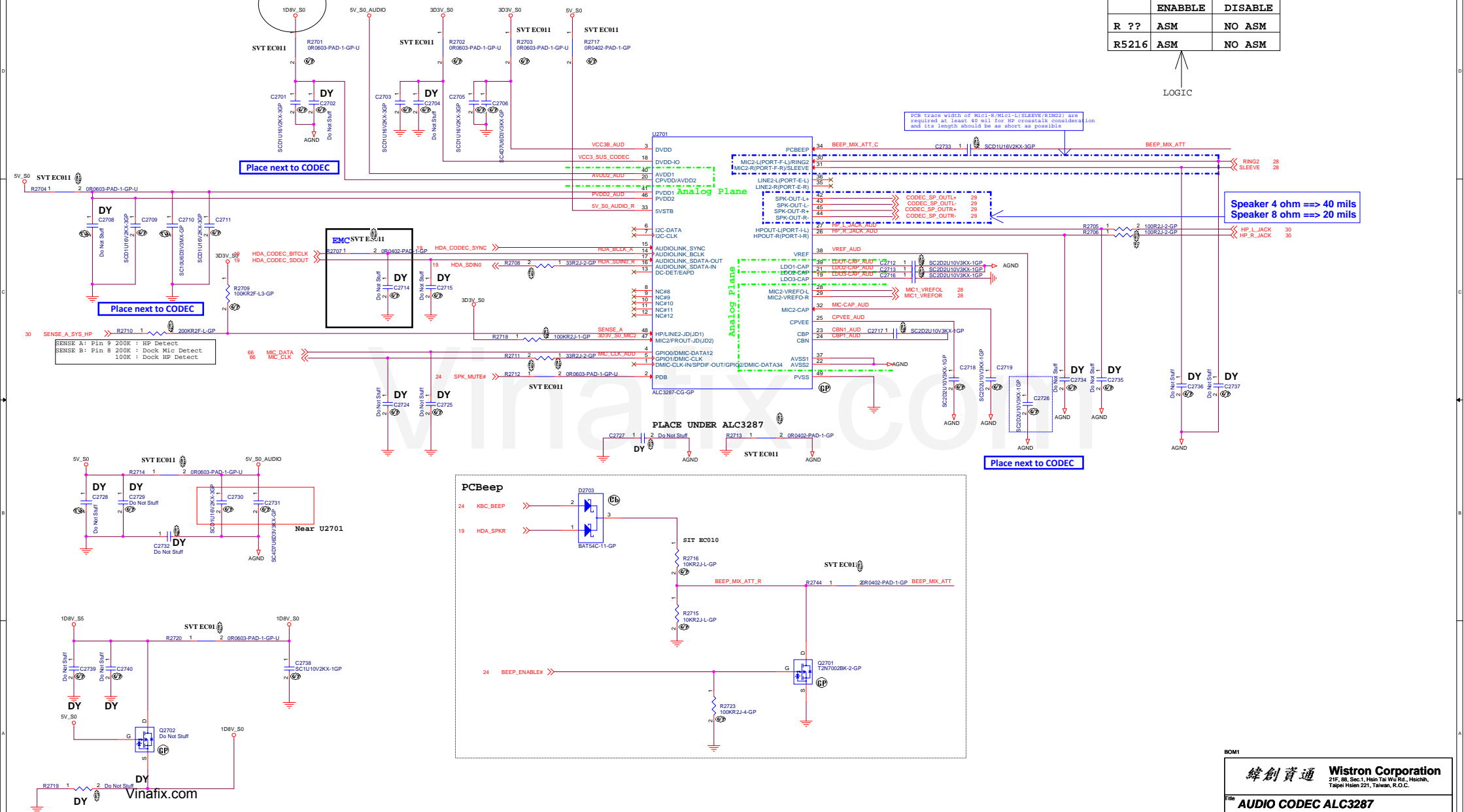


TABLE MIC HW ENABLE/DISABLE		
	ENABBLE	DISABLE
R ??	ASM	NO ASM
R5216	ASM	NO ASM

LOGIC

Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

PLACE UNDER ALC3287

Place next to CODEC

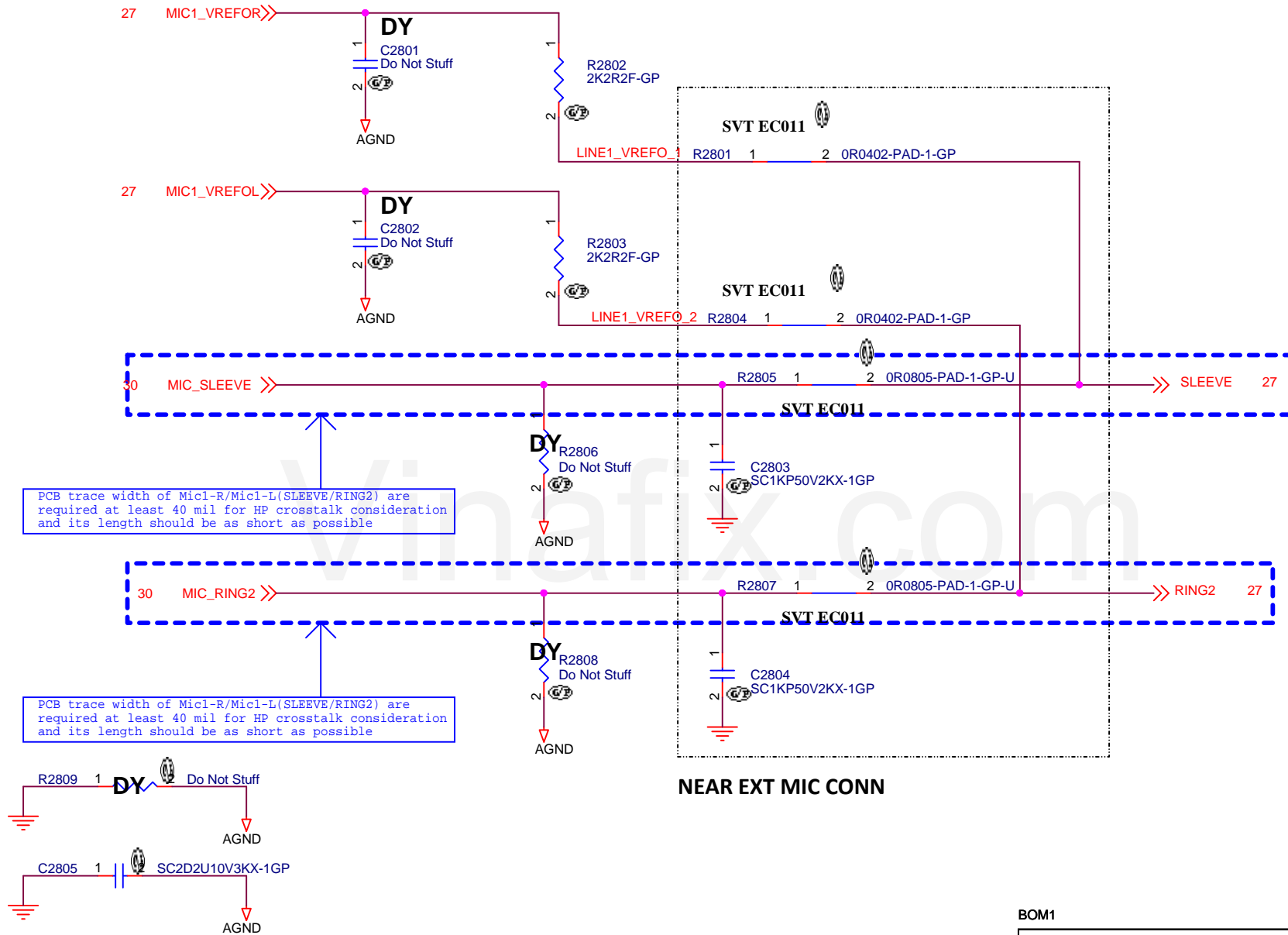
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO CODEC ALC3287**

Size Custom	Document Number LKL-1	Rev 2
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	DATE	FILED	CITY	STATE	ZIP
	DEC 09 1987	FBI	ATLANTA	GA	30303

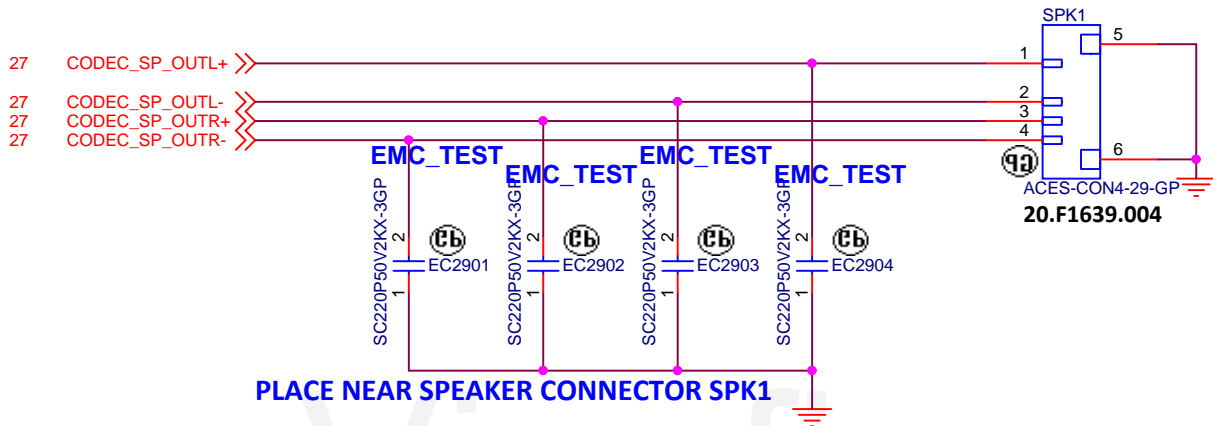


NEAR EXT MIC CONN

BOM1			
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
Title AUDIO MIC I/F			
Size A4	Document Number LKL-1		Rev 2A
Date: Friday, January 19, 2018		Sheet 28 of 105	

SSID = AUDIO

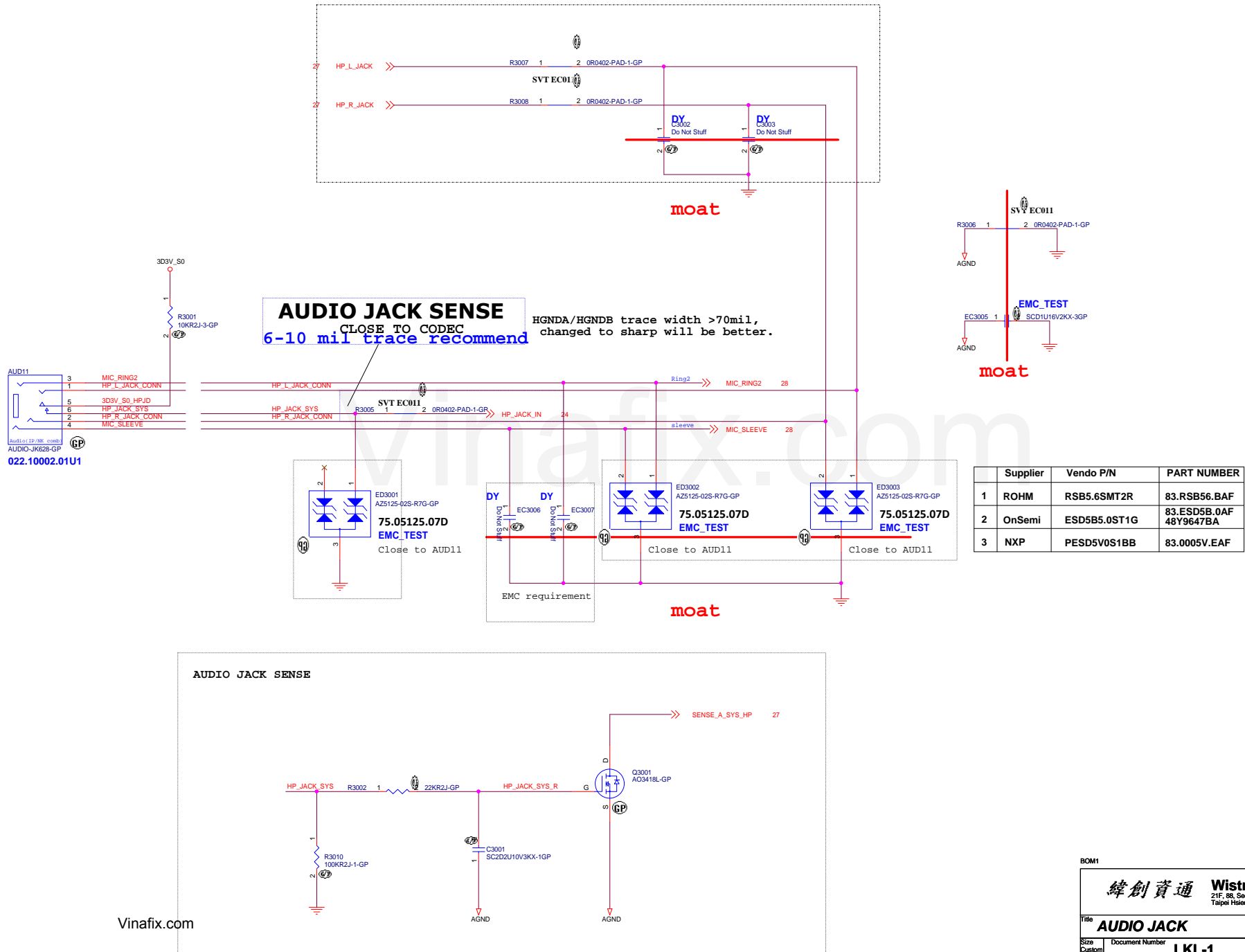
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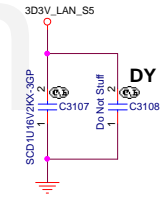


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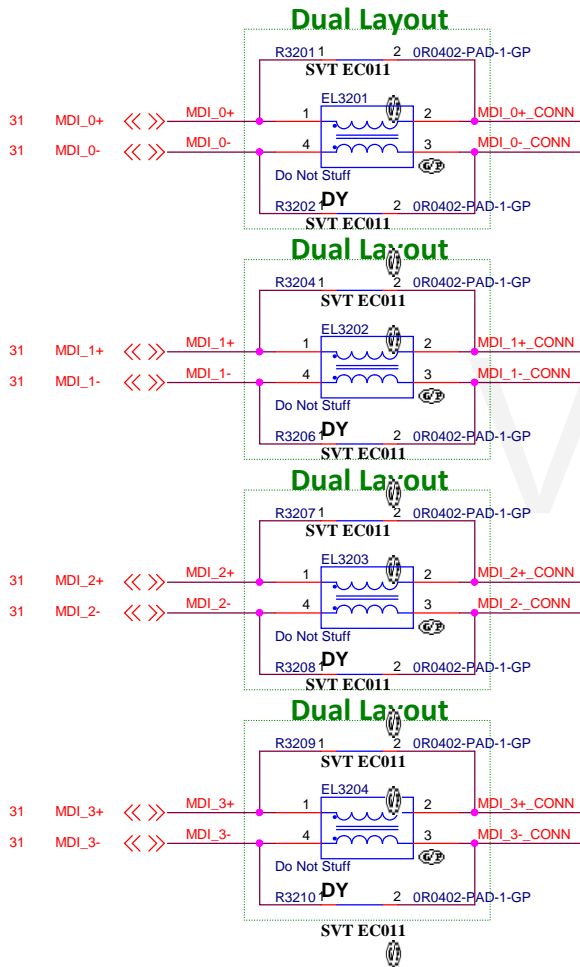
緯創資通		Wistron Corporation	
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Title			
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Size A4	Document Number LKL-1		Rev 2A
Date:	Friday, January 19, 2018	Sheet 29 of	105

NEAR AUDIO JACK CONN

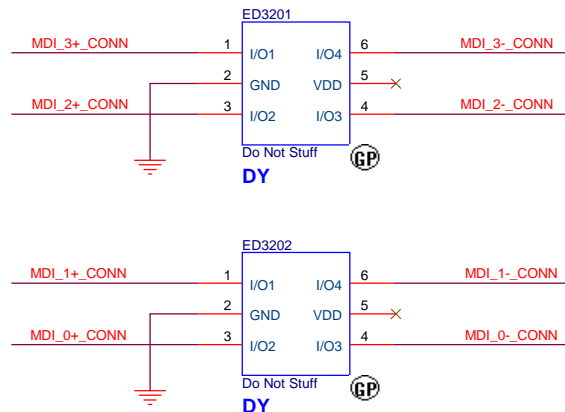
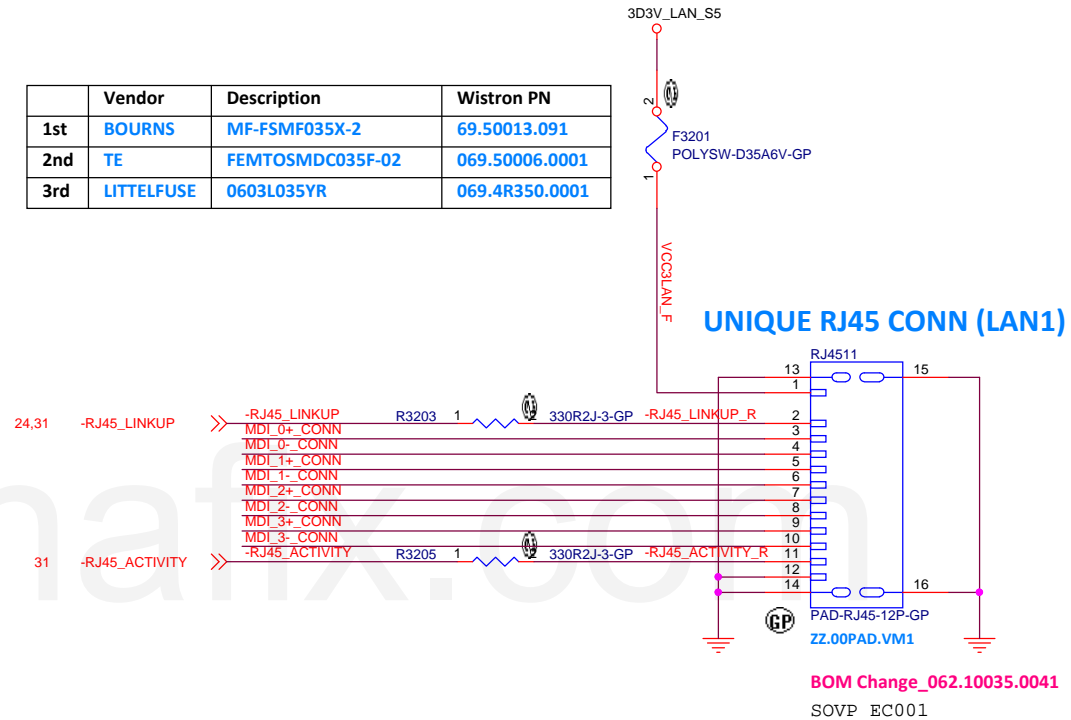




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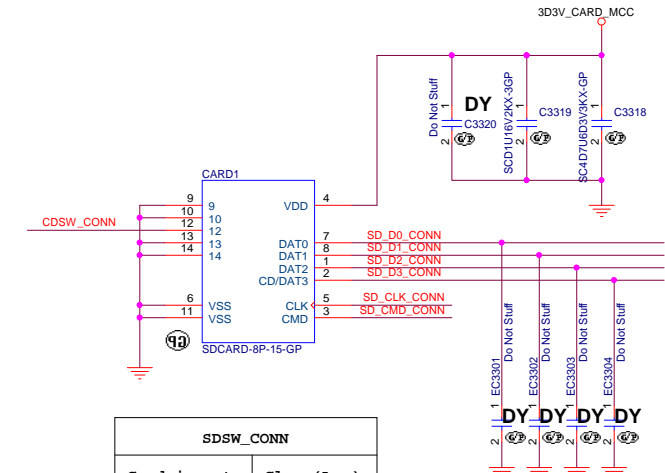
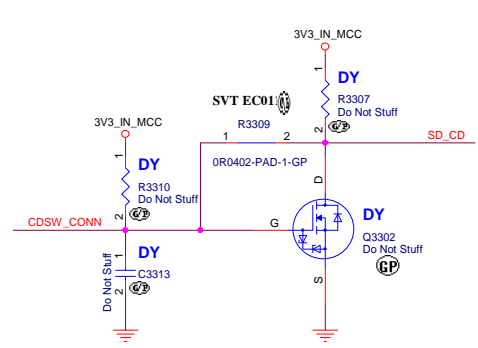
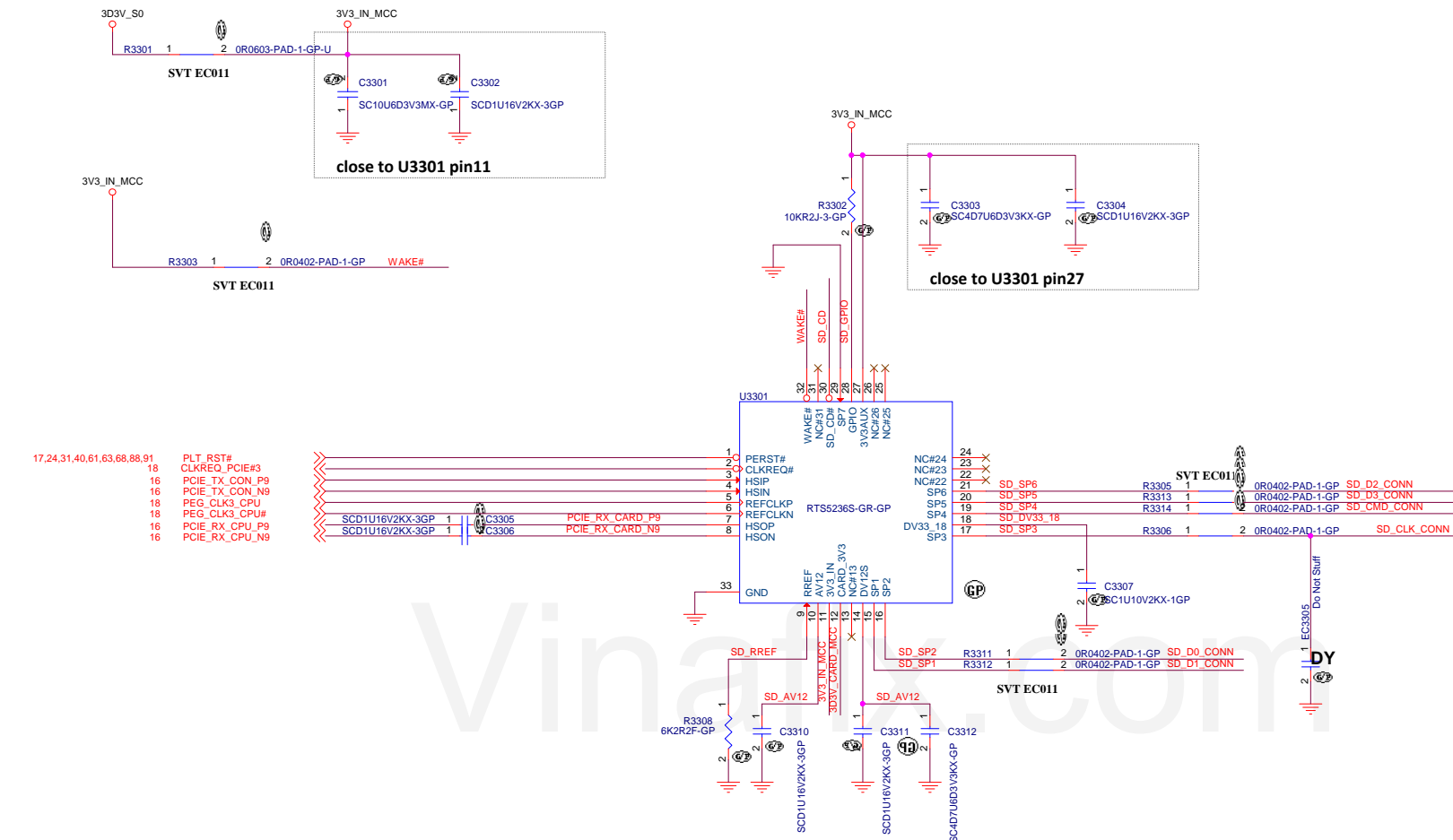


	Vendor	Description	Wistron PN
1st	BOURNS	MF-FSMF035X-2	69.50013.091
2nd	TE	FEMTOSMDC035F-02	069.50006.0001
3rd	LITTELFUSE	0603L035YR	069.4R350.0001

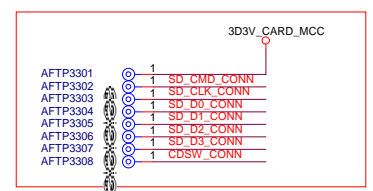


BOM1

緯創資通		Wistron Corporation	
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Title GBE DONGLE I/F			
Size Custom	Document Number LKL-1	Rev 2A	
Date: Friday, January 19, 2018		Sheet 32 of 105	



SDSW_CONN	
Card insert	Close(Low)
No Card	Open



These test pins trace should be short and close to connector

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BOM1

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Title

CARD READER IC/CONN

Size

Custom

Document Number

LKL-1

Rev

2A

Date:

Friday, January 19, 2018

Sheet

33

of

105

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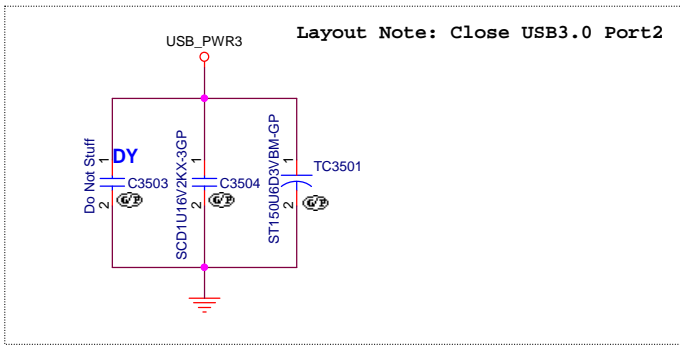
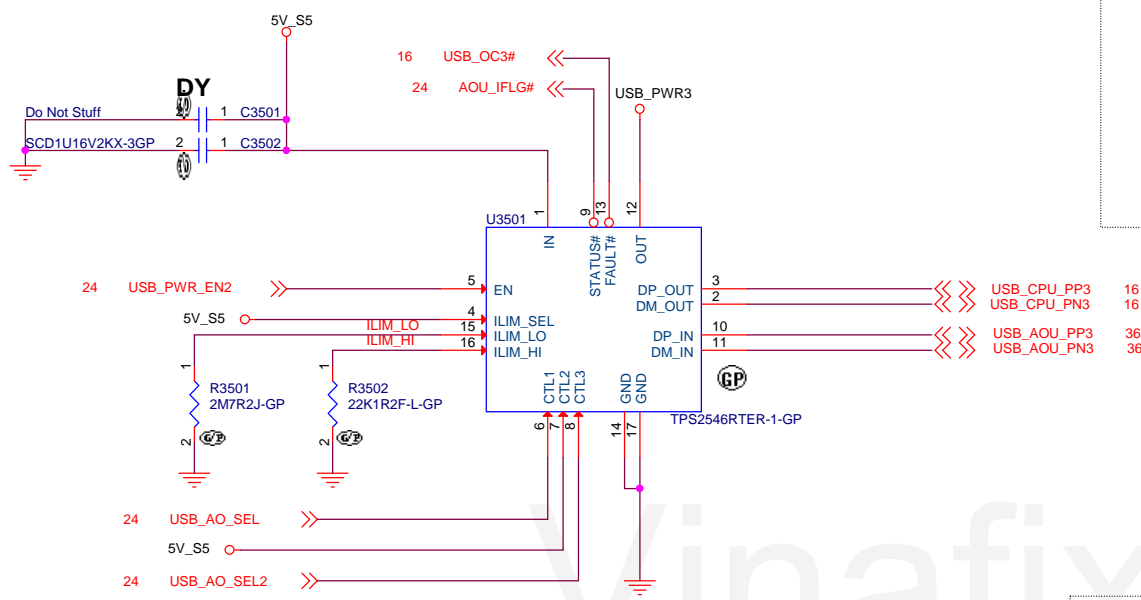
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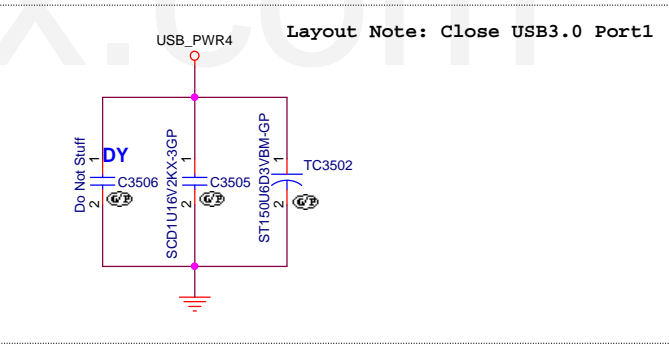
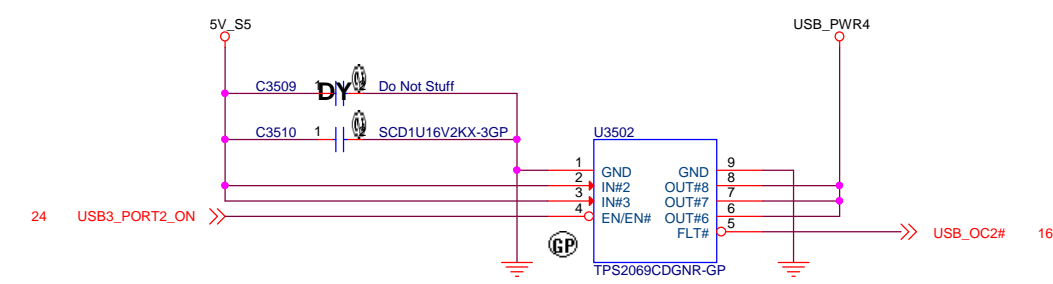
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Title RESERVED		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018		Sheet 34 of 105

Main Func = USB Charger

For USB3.0 System Port1 (For AOU)



For USB3.0 System Port2



FOR ON BOARD SINGLE USB 3.0 CONNECTOR
Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3302

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGMR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

BOM1

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Title

USB CHARGER/SWITCH

Size

Custom

Document Number

LKL-1

Date

Friday, January 19, 2018

Sheet

35

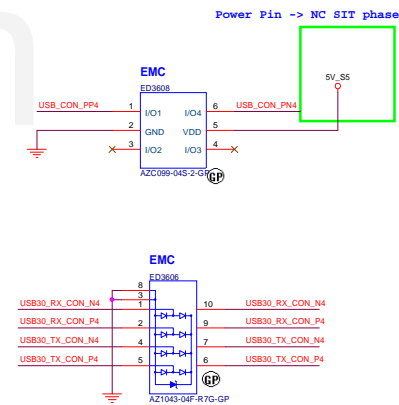
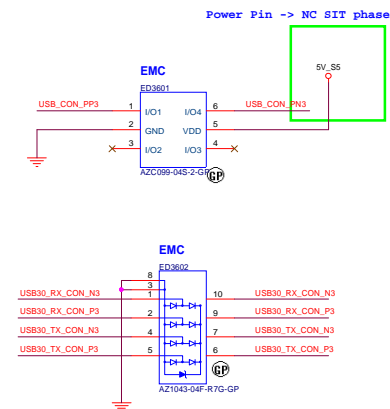
of

105

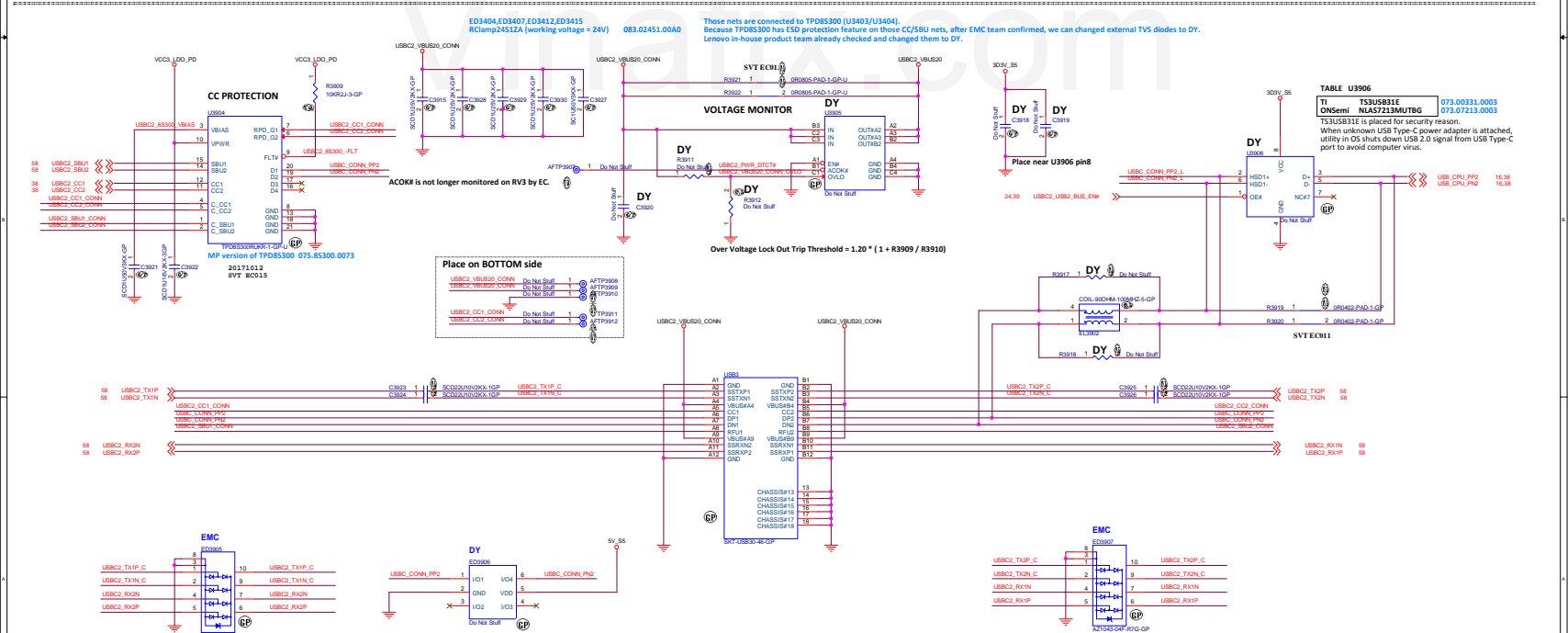
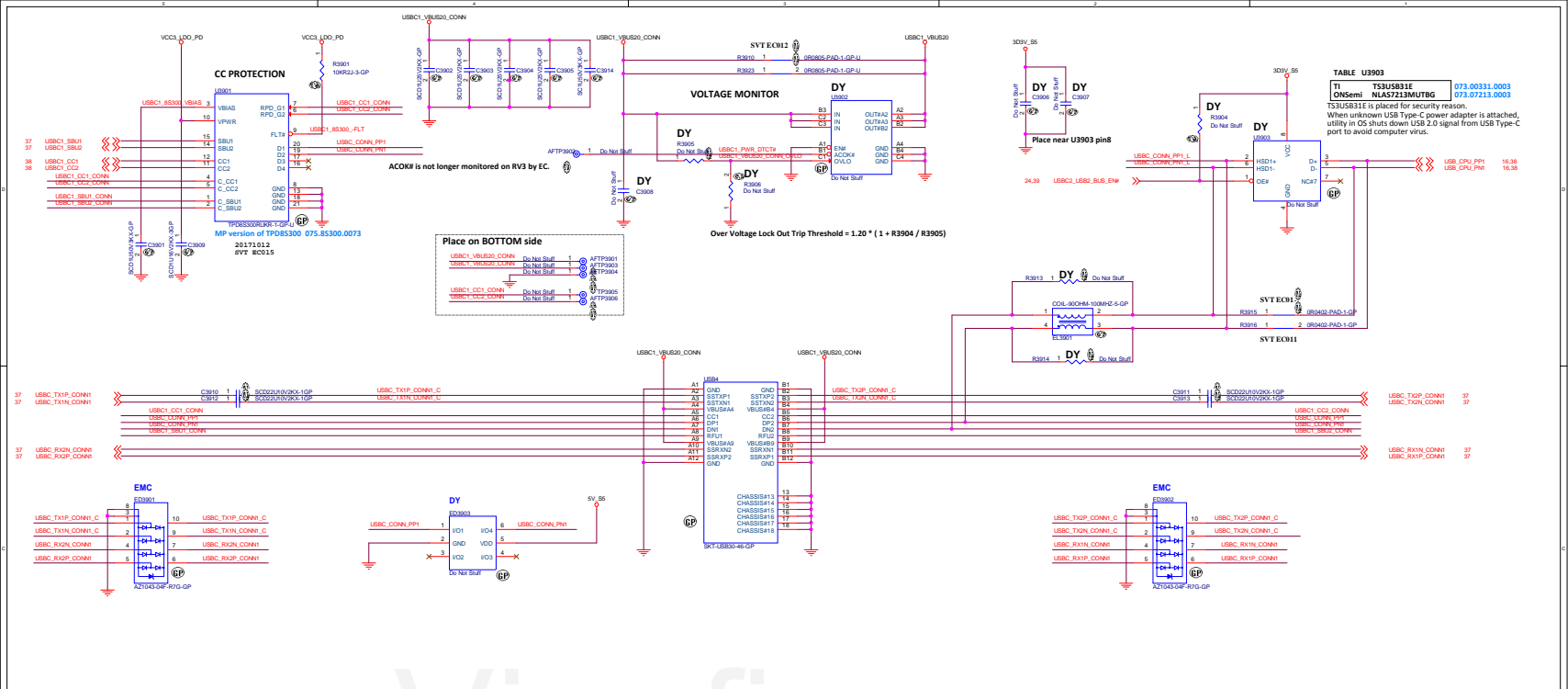
Rev

2A

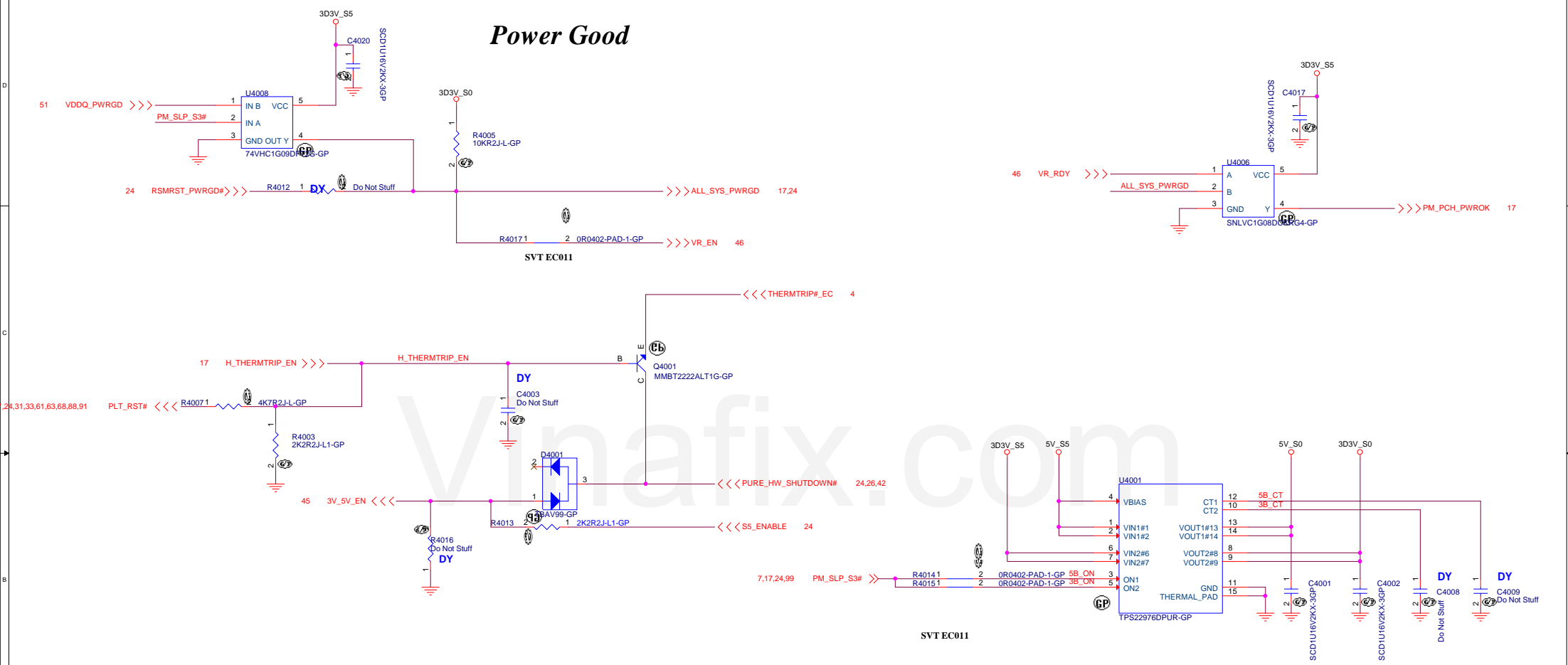
Main Func = USB3.0 Port2



BOM1	
<div>  <div> 緯創資通 </div> <div> Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Neichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>	
Title	
USB3.0 CONN	
Size	Document Number
Custom	LKL-1
Date	Rev
Friday, January 19, 2018	2A
Sheet	of
36	106



Main Func = Power Plane & Sequence



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Title
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Size
A4

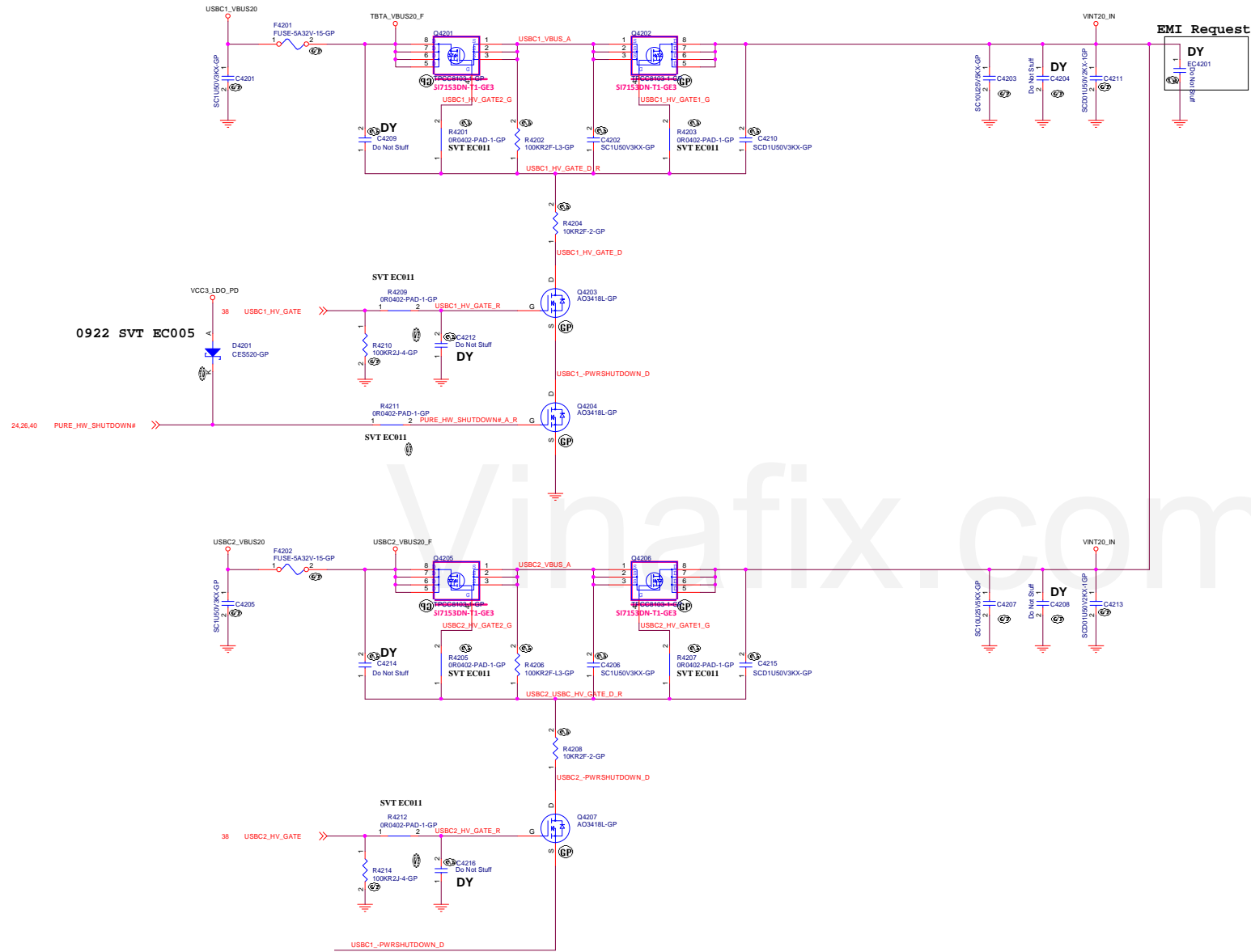
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LKL-1

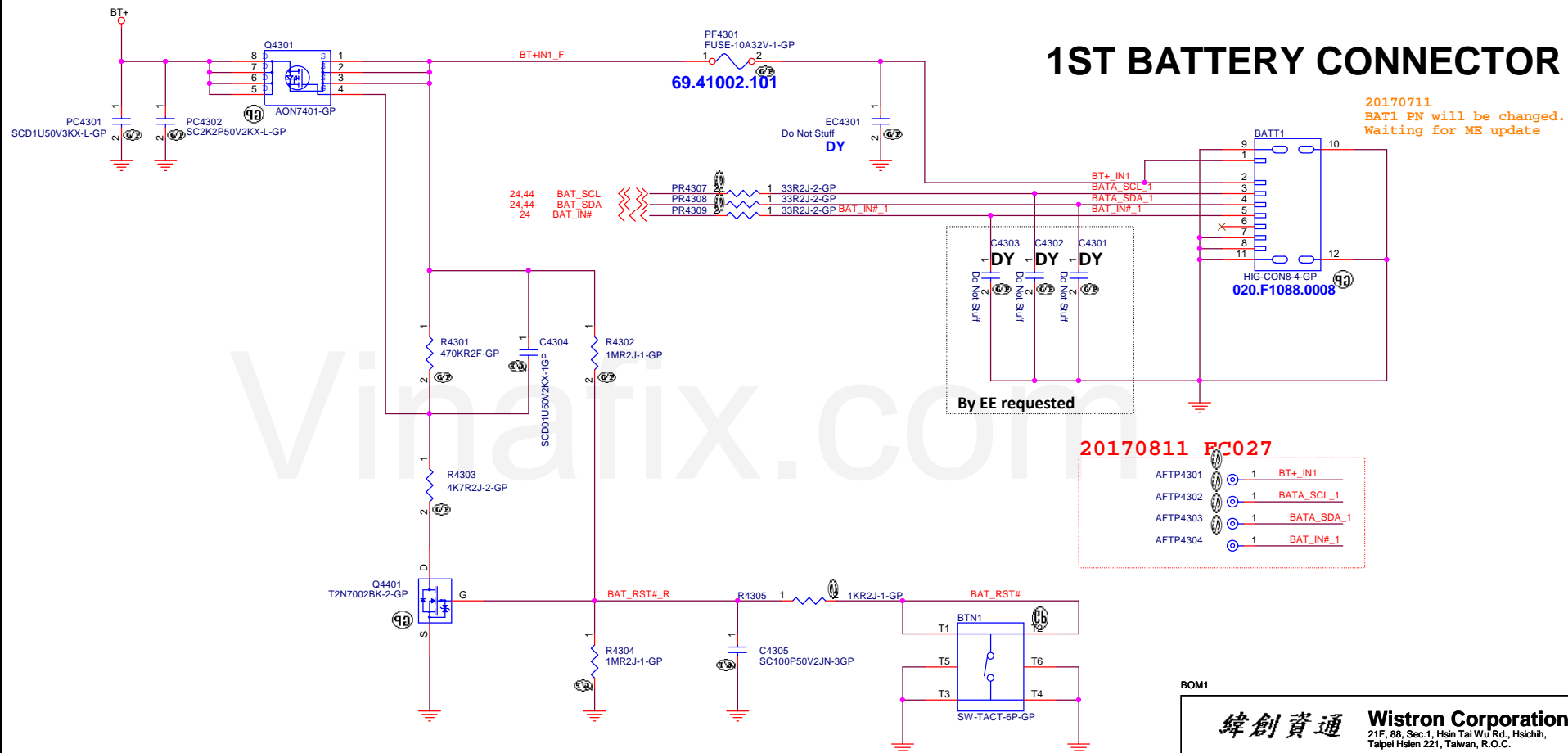
Rev
2A

Date: Friday, January 19, 2018

Sheet 41 of 105

Table
Q4201,Q4202,Q4203,Q4204
1st SI7153DN-T1-GE3 VISHAY Need to apply WPN and symbol
2nd TPCC8103 TOSHIBA 084.08103.M001





BOM1

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File

BATT_CONN

Size
Custom

Document Number

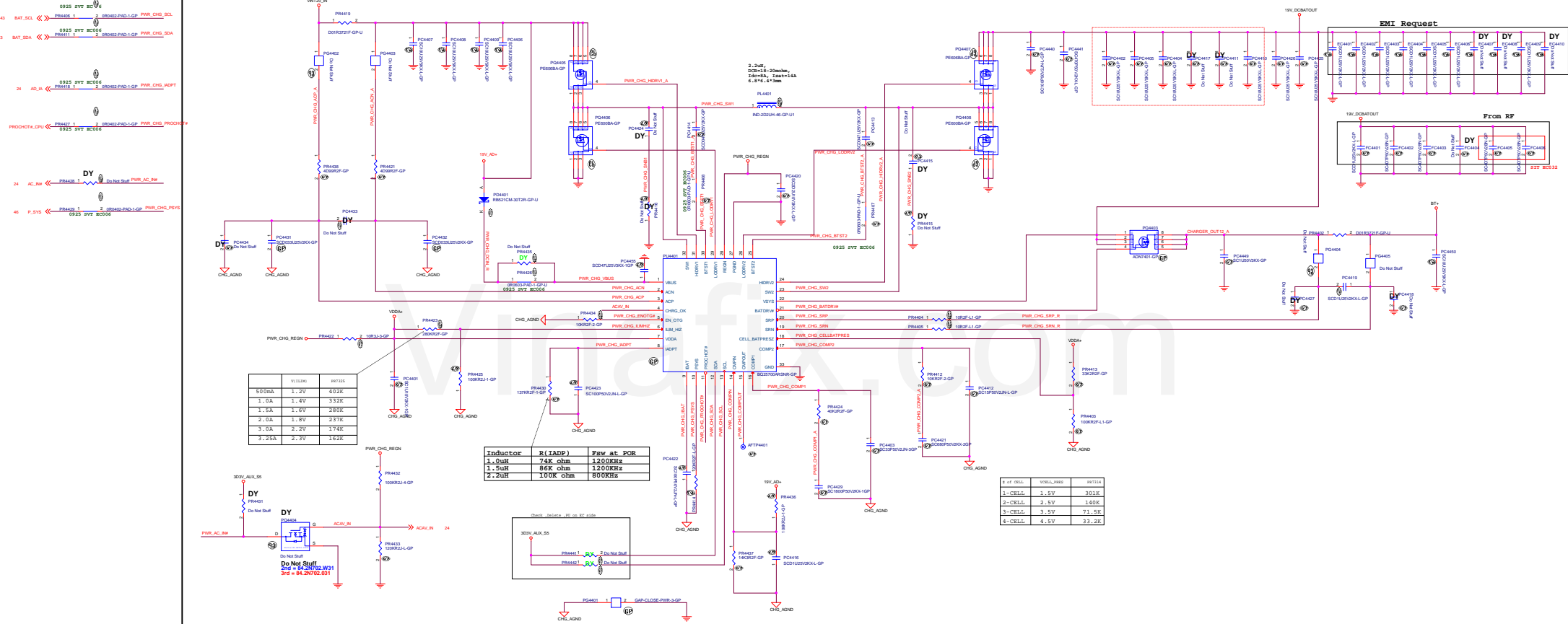
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 43 of 105

OFFPAGE



	V11L1	V11L2
500mA	1.2V	402K
2.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(1ADP)	Few at POR
1.0uH	74K ohm	1200KHz
1.5uH	86K ohm	1200KHz
2.2uH	100K ohm	800KHz

1 of 10	V11L1	V11L2
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

0925 SVT 3C006

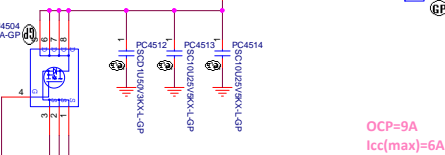
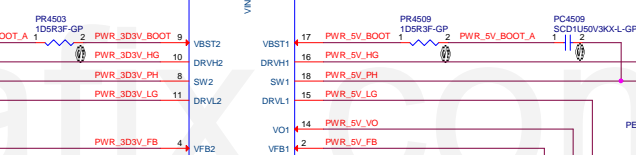
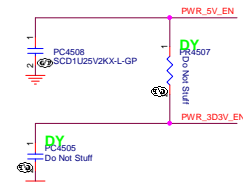
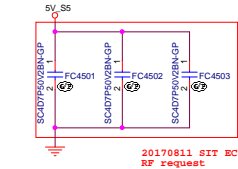
3V_5V_EN >>> PR4501 1 2 0R0402-PAD-1-GP PWR_5V_EN

0925 SVT 3C006

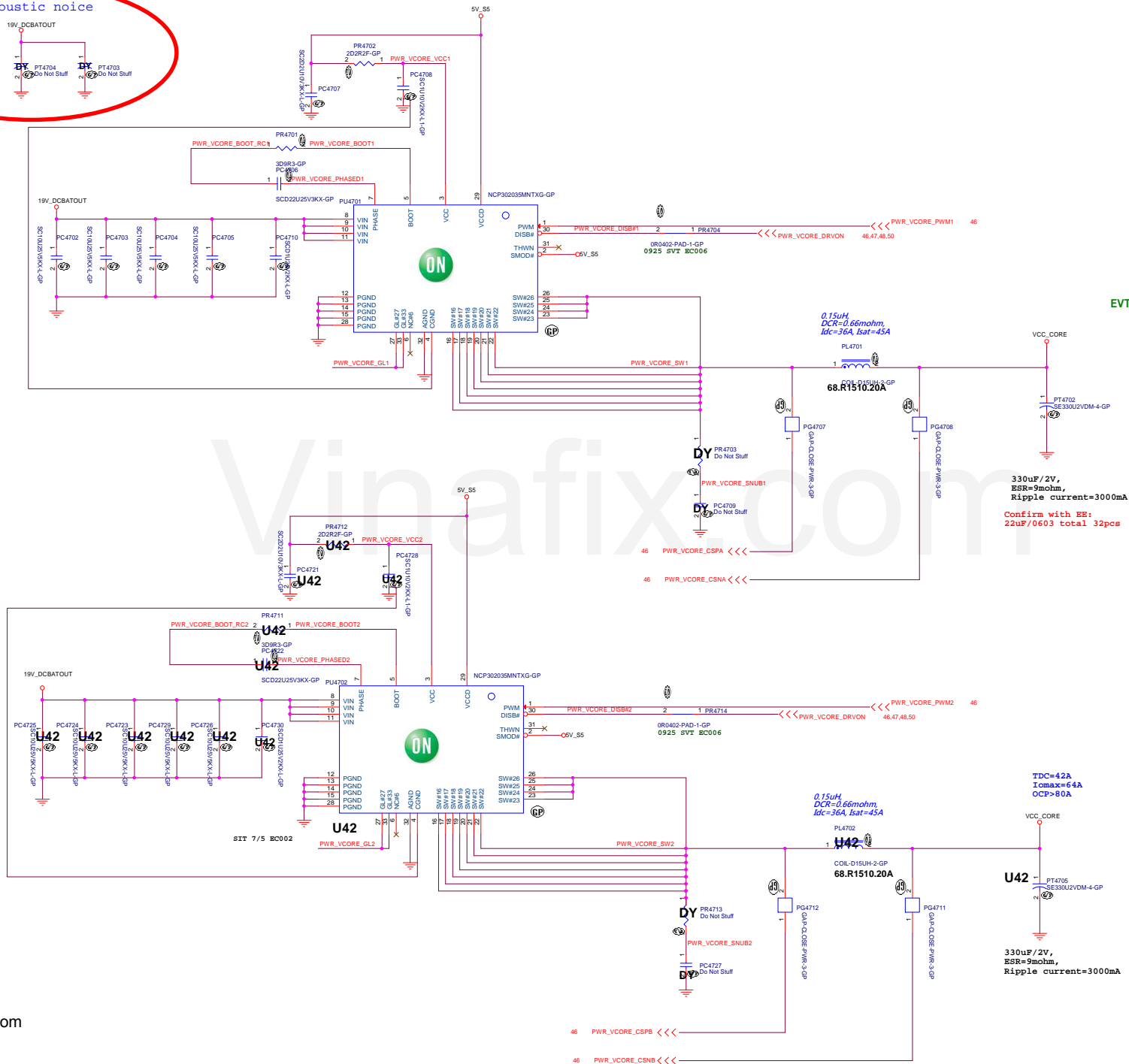
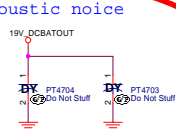
3V_5V_EN >>> PR4502 1 2 0R0402-PAD-1-GP PWR_3D3V

0925 SVT 3C006

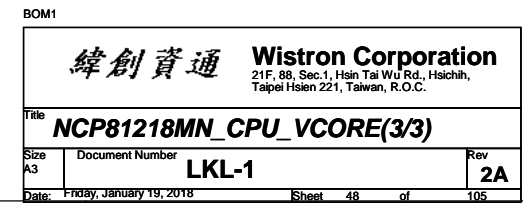
3V_5V_PWRGD <<< PR4504 1 2 0R0402-PAD-1-GP PWR_3D3V



For acoustic noise



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Main Func = CPU_CORE

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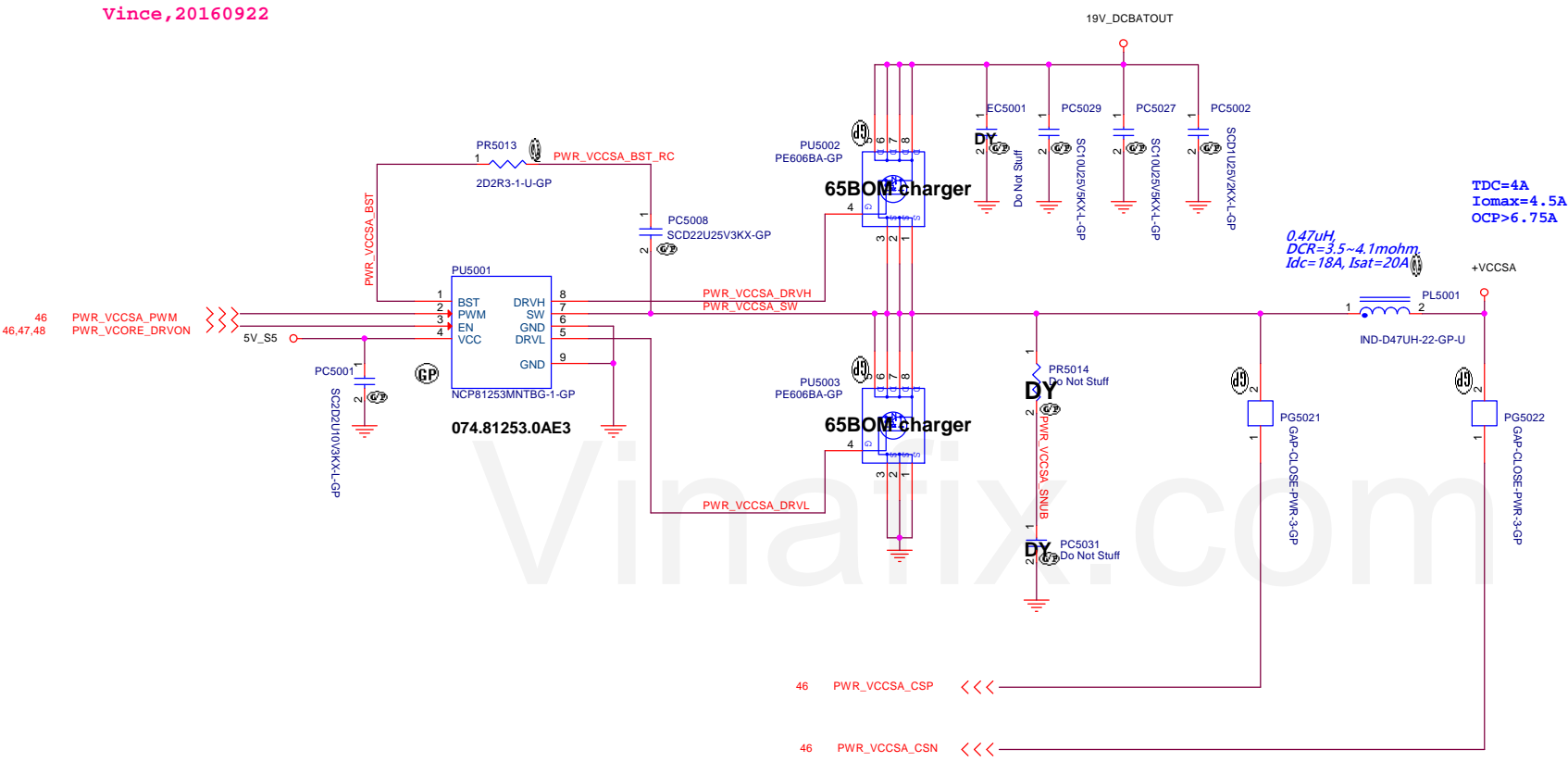
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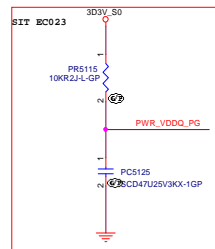
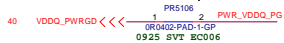
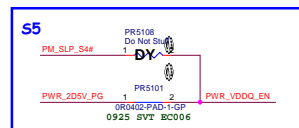
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Size	Document Number		Rev
A4	LKL-1		2A
Date:	Friday, January 19, 2018	Sheet 49 of	105

Main Func = CPU_CORE

Vince, 20160922

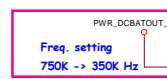
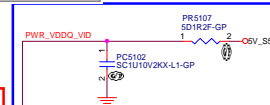




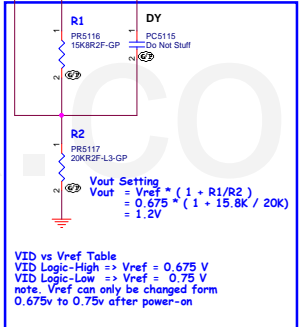
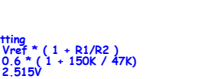
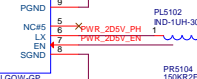
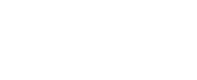
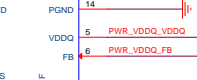
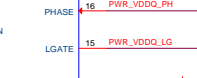
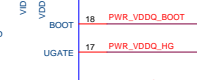
VID

Table 1. VID and Reference Voltage Setting

VID	Reference Voltage (V)
High	0.675
Low	0.75



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



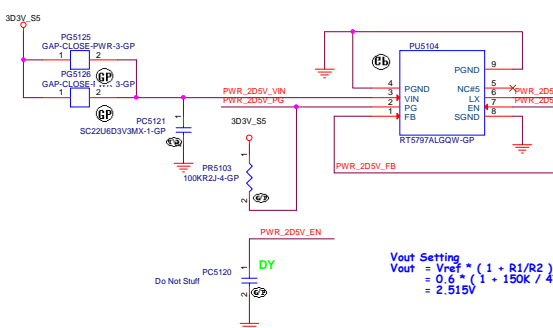
TDC=2A

I_{max}= 3A

Chilisin, 2.5mmx2.0mmX1.2mm

DCR: 59m Ohm

I_{dc}: 3 A, I_{sat}: 4A

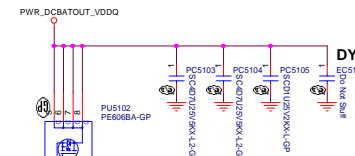
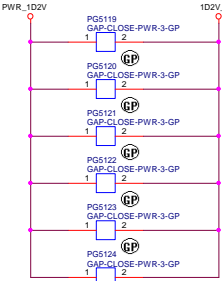


Vout Setting

$V_{out} = V_{ref} * (1 + R1/R2)$

$V_{out} = 0.6 * (1 + 150K / 47K)$

$V_{out} = 2.515V$

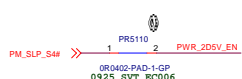
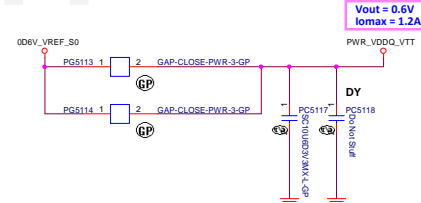
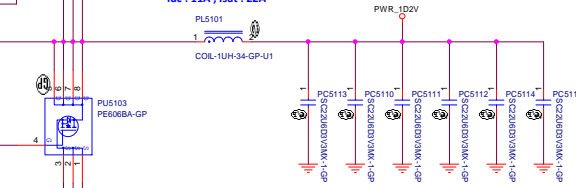


Cytec, 6.6mmx7.3mmx3.0 mm

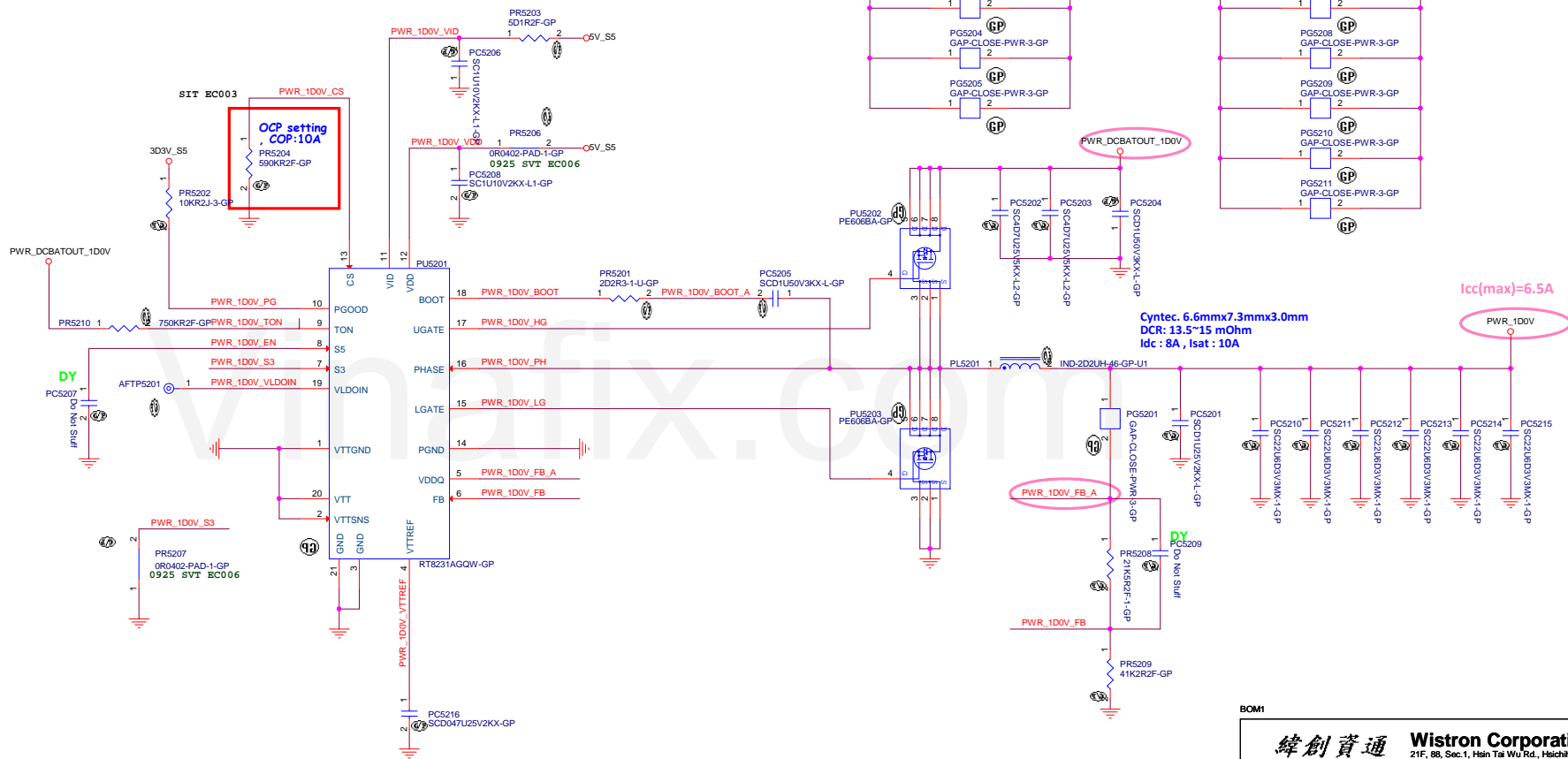
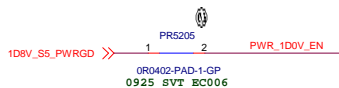
DCR: 9~10mOhm

I_{dc}: 11A, I_{sat}: 22A

I_{cc(max)}=5.33A



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BOM

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Rev
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Date: Friday, January 19, 2018 Sheet 52 of 105

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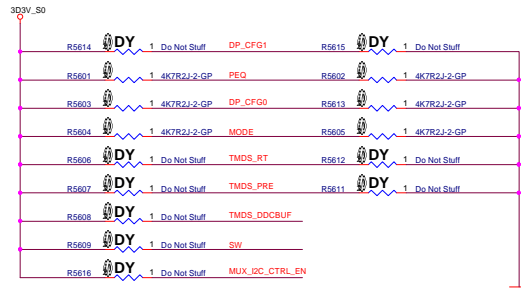
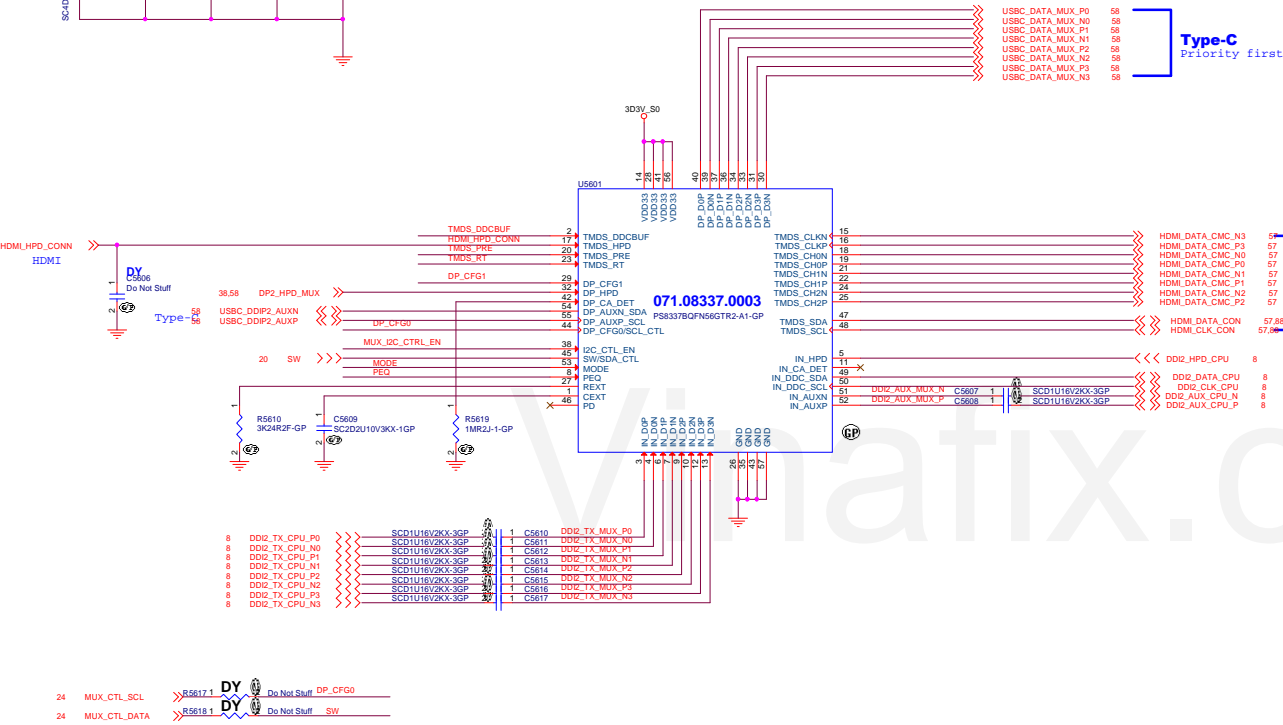
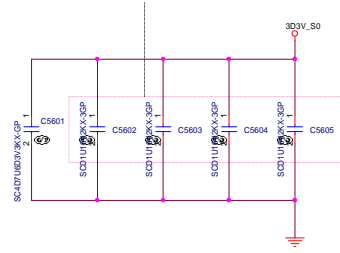
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Title RESERVED		
Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018	Sheet 54 of	105



Type-C HDMI_SELECT
Type-C is higher priority than HDMI.

0.1uF caps are near of each VDD33 pin

H	4.7K
M	150K
L	DY



Type-C
Priority first

System HDMI

- TMDS_PRE1 = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis
The pin internal pull down at ~150K, 3.3V I/O.
- TMDS_RT1 = L: Standard open drain driver
= H: Open drain driver with termination resistors
The pin internal pull down at ~150K, 3.3V I/O.
- TMDS_DDCBUF1 = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor
The pin internal pull down at ~150K, 3.3V I/O.
- PEQ1 = L: default, LEO, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2
The pin internal pull down at ~150K, 3.3V I/O.
- DP1_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable
The pin internal pull down at ~150K, 3.3V I/O.
- DP1_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
The pin internal pull down at ~150K, 3.3V I/O.
- MODE1 = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable
The pin internal pull down at ~150K, 3.3V I/O.
- For Control Switching:
SW 1= L: DP output is selected
SW 1= H: TMDS output is selected
- For Automatic Switching:
SW1 = L: DP output has higher priority
The pin internal pull down at ~150K, 3.3V I/O.
SW1 = H: TMDS output has higher priority.

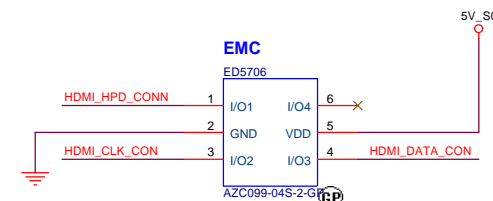
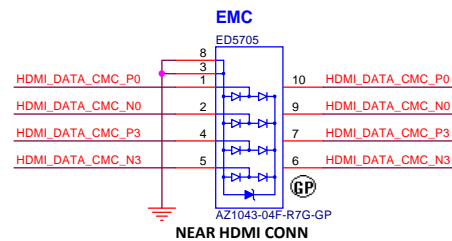
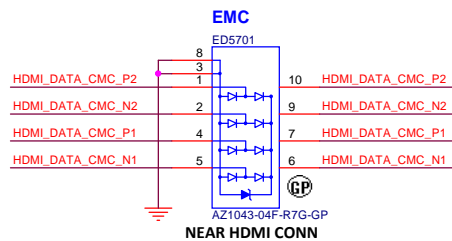
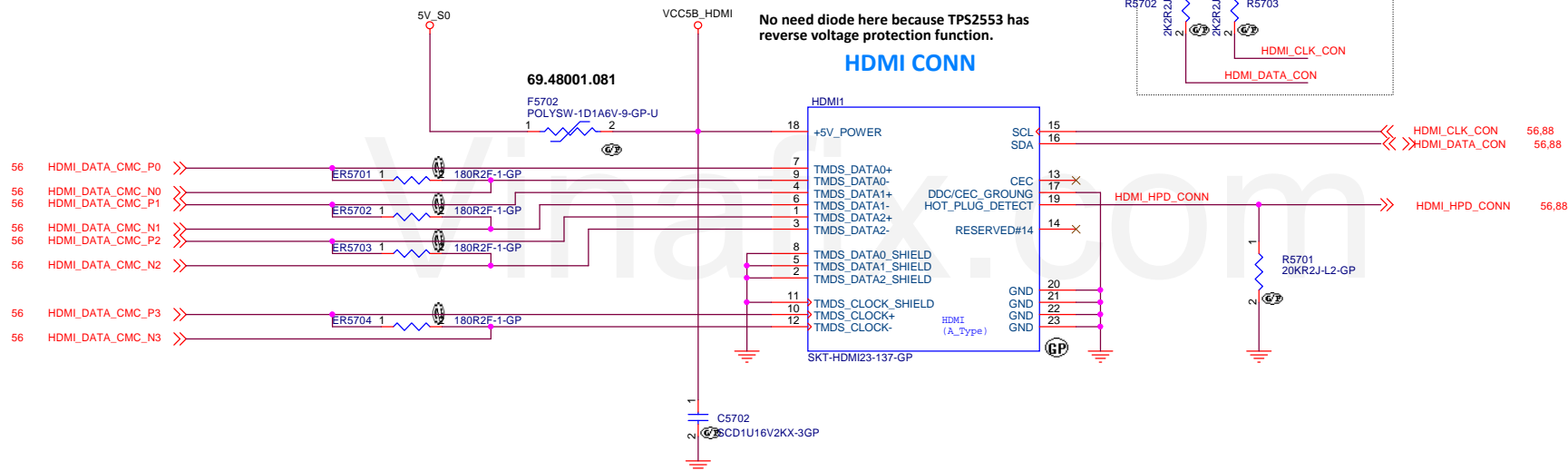
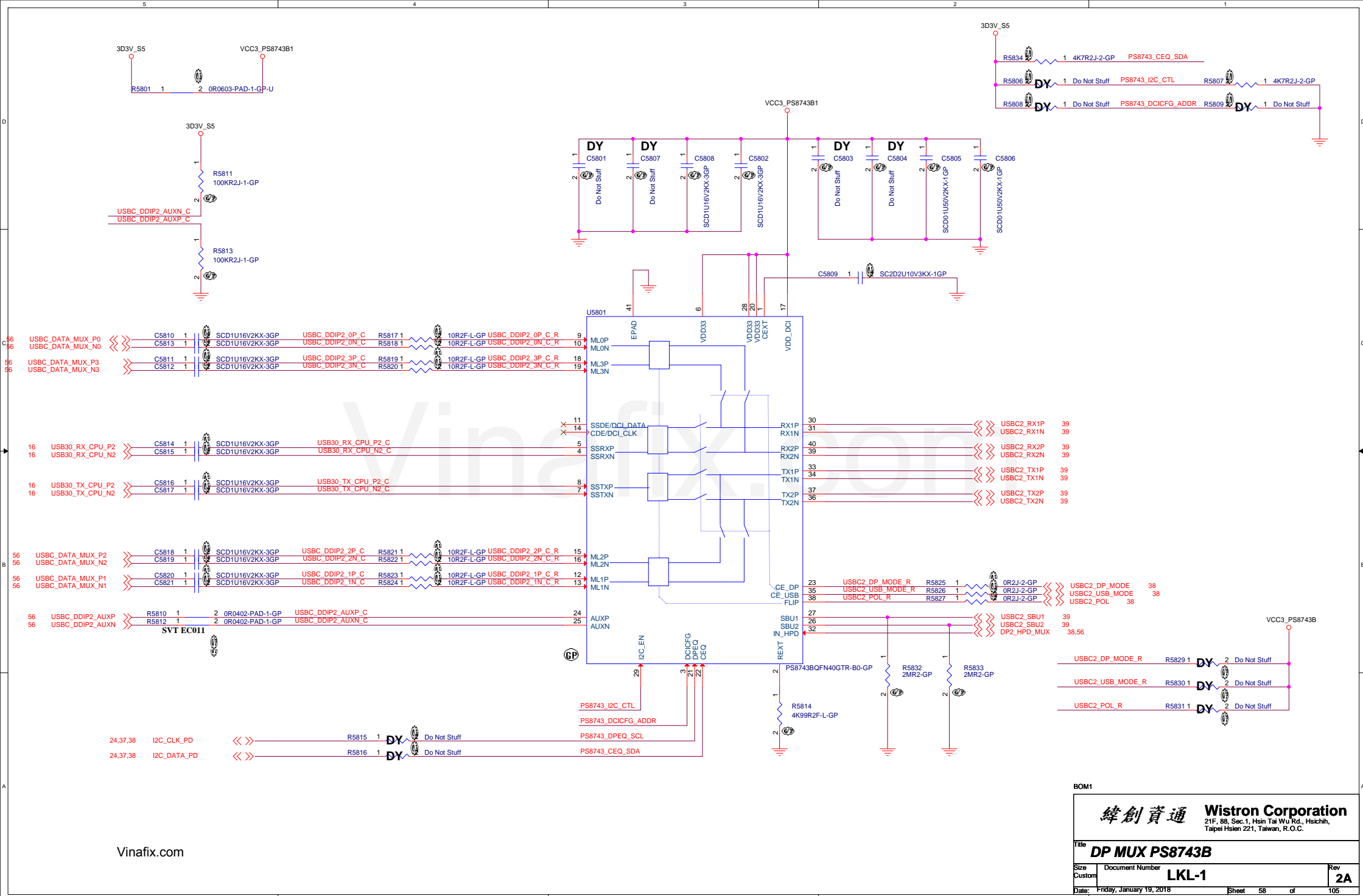


TABLE of TVS DIODE: D2905,D2906

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDMI RE-DRIVER/CONN	
Size Custom	Document Number LKL-1
Date: Friday, January 19, 2018	Rev 2A
Sheet 57 of 105	



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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Size A4	Document Number LKL-1	Rev 2A
Date: Friday, January 19, 2018		Sheet 59 of 105

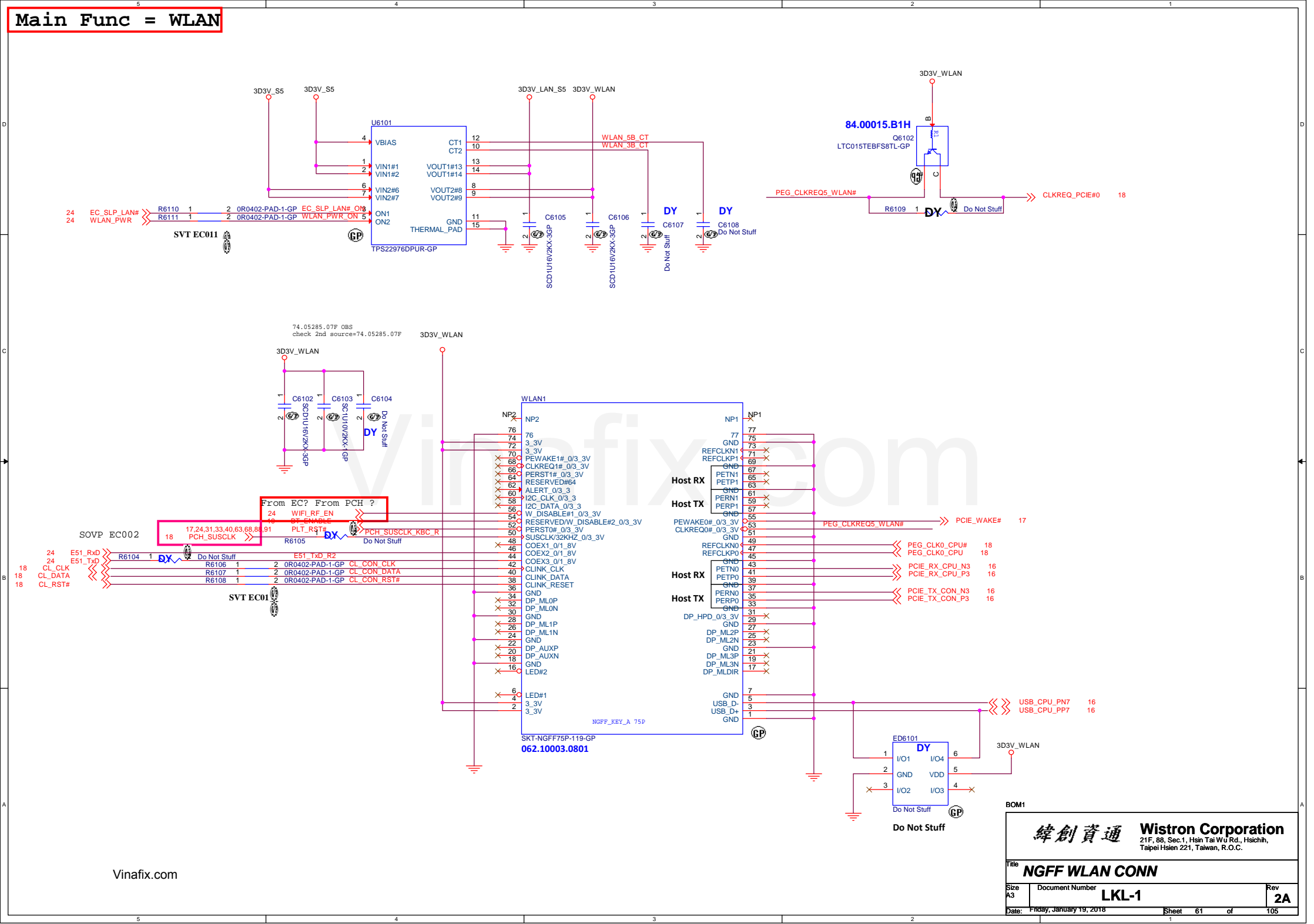
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Title RESERVED			
Size A4	Document Number LKL-1		Rev 2A
Date: Friday, January 19, 2018		Sheet 60 of	105

Main Func = WLAN



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A4

Document Number
LKL-1

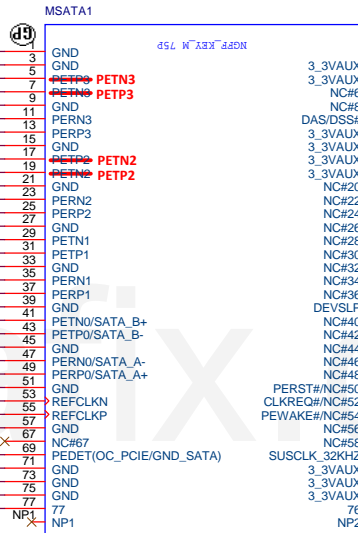
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Date: Friday, January 19, 2018

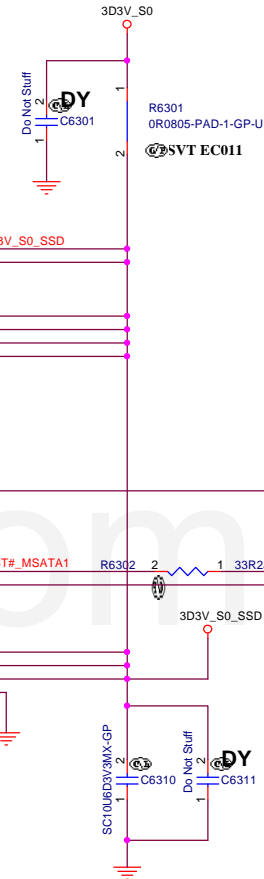
Sheet 62 of 105

16 PCIE_RX_CPU_N5
16 PCIE_RX_CPU_P5
16 PCIE_TX_CON_N5
16 PCIE_TX_CON_P5
16 PCIE_RX_CPU_N6
16 PCIE_RX_CPU_P6
24 SSD_DTCT#
16 PCIE_TX_CON_N6
16 PCIE_TX_CON_P6
16 PCIE_RX_CPU_N7
16 PCIE_RX_CPU_P7
16 PCIE_TX_CON_N7
16 PCIE_TX_CON_P7
16 PCIE_RX_SATA_P8
16 PCIE_RX_SATA_N8
16 PCIE_TX_SATA_N8
16 PCIE_TX_SATA_P8
18 PEG_CLK1_CPU#
18 PEG_CLK1_CPU
16 PE_DTCT

(PE_DTCT)
SATA Device GND
PCIe Device Open



SKT-NGFF75P-77-GP
062.10003.0511
20171012
SVT EC016



BOM1

Title		NGFF SSD SLOT	
Size	Document Number	Rev	
A3	LKL-1	2A	
Date:	Friday, January 19, 2018	Sheet	63 of 105

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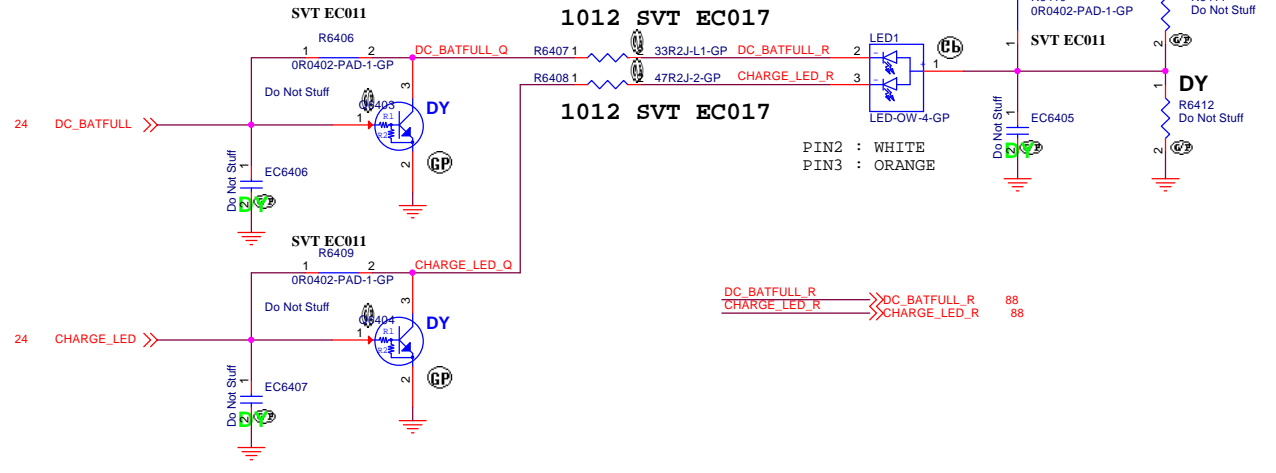
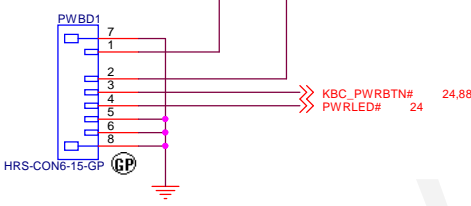
Dual LED

1012 SVT EC017

1012 SVT EC017

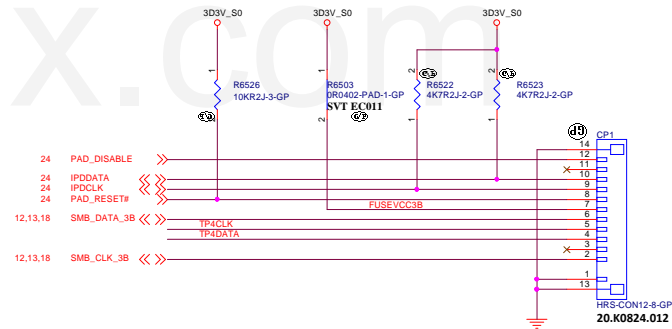
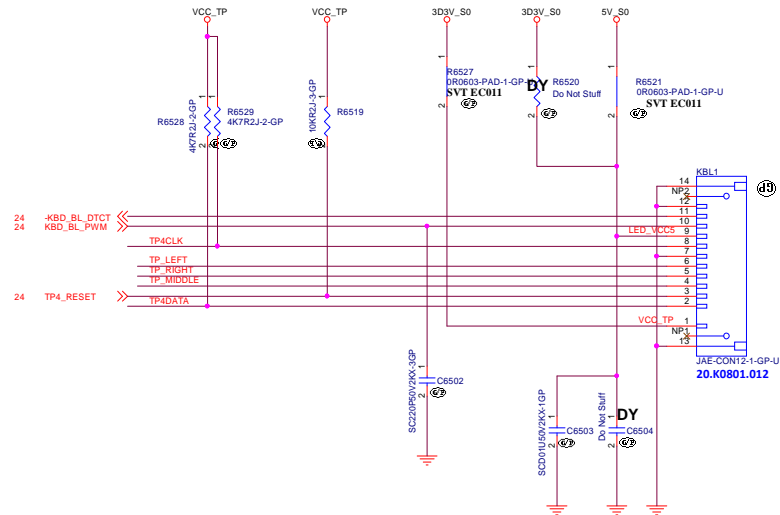
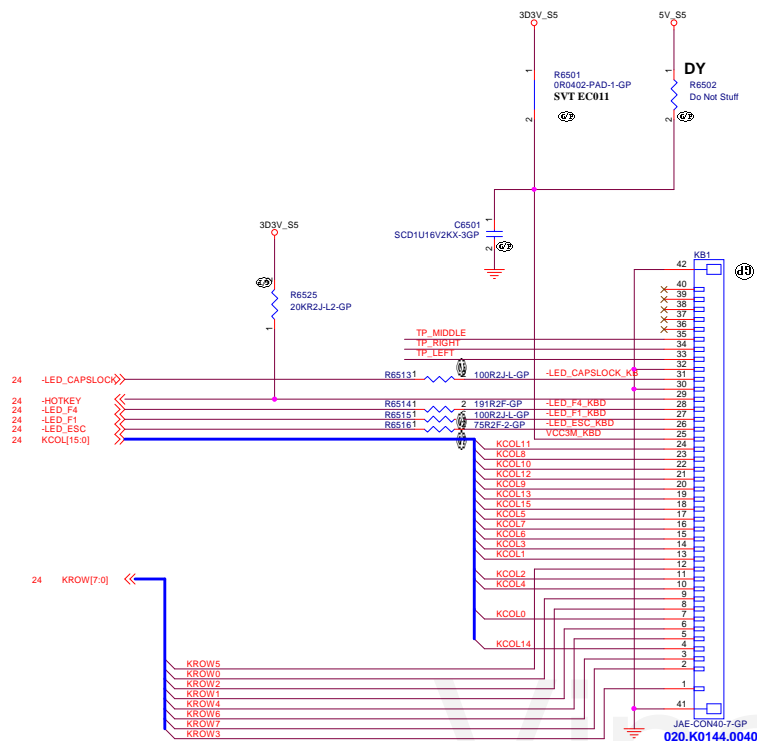
PIN2 : WHITE
PIN3 : ORANGE

PWR BD to MB

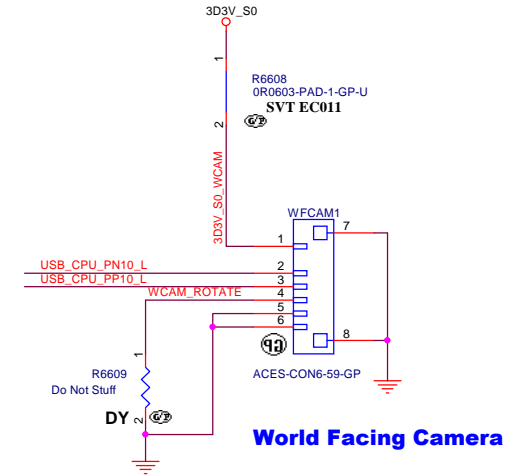
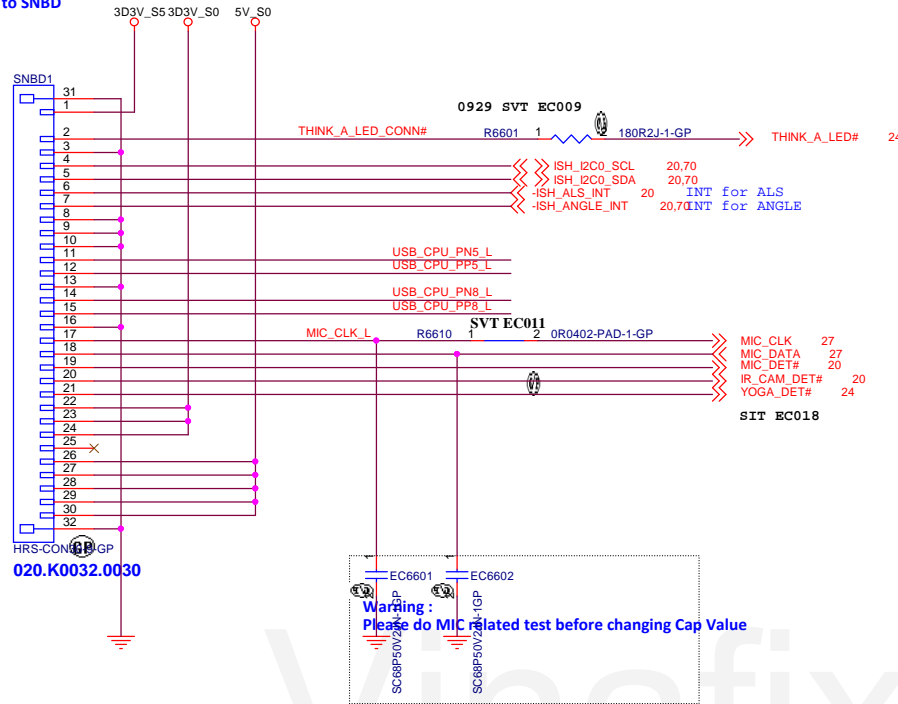


DC_BATFULL_R >>> DC_BATFULL_R 88
CHARGE_LED_R >>> CHARGE_LED_R 88

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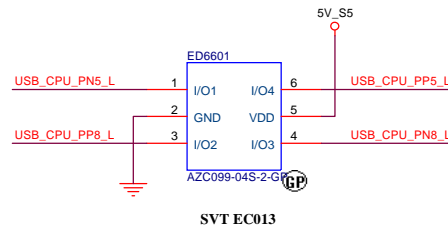
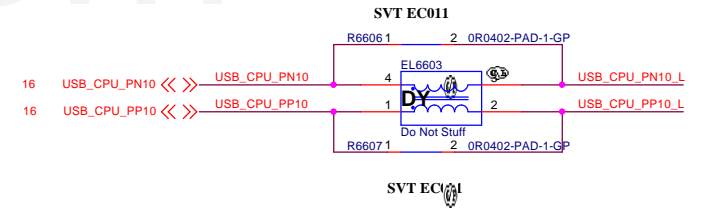
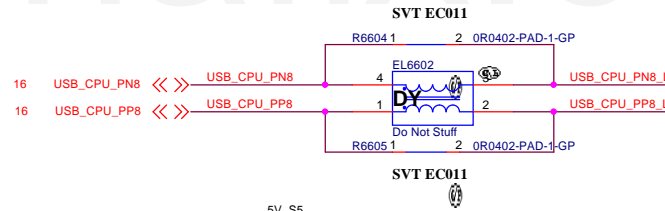
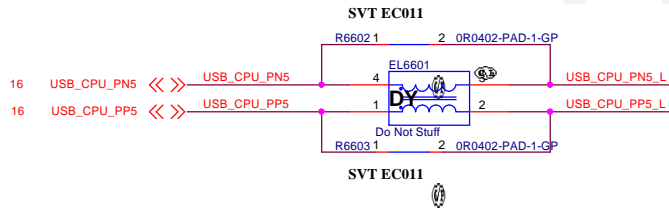
MB to SNBD



Default camera direction is, LED on the right side of Lens/CMOS.

Pin4 supply = High : Normal image (default, and if this pin not be connected = normal image)

Pin4 supply = Low : Upside down image (means if we can rotate camera module 180 degree = LED on left side, use this mode)



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Title (RESERVED)	
Size A3	Document Number LKL-1
Date: Friday, January 19, 2018	Rev 2A
Sheet 66 of 105	

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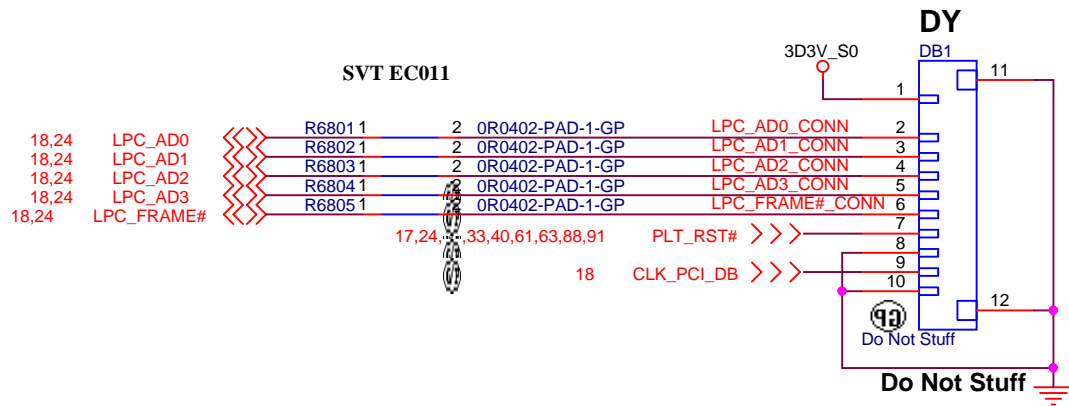
Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 67 of 105



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Title **DEBUG CONN**

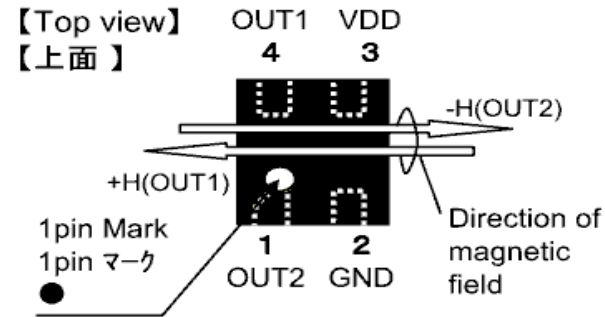
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Document Number
LKL-1

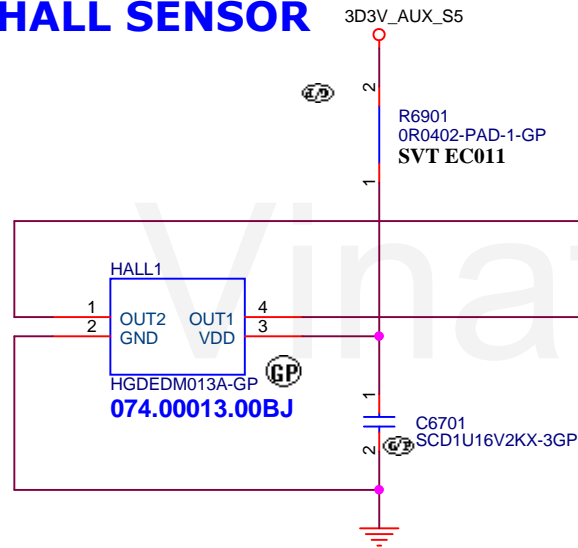
Rev
2A

Date: Friday, January 19, 2018

Sheet 68 of 105



HALL SENSOR



» LID_CLOSE# 20,24

» SENSOR_LID_OPEN# 20,24

LID_CLOSE# : NB Lid function
SENSOR_LID_OPEN# : Tablet detect function

Pin1 need place at "Upper Right Corner"

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Size A4 Document Number **LKL-1** Rev **2A**

Date: Friday, January 19, 2018 Sheet 69 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title **RESERVED**

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 71 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 72 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 73 of 105
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Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 74 of 105
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Title
RESERVED

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 75 of 105

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Title **RESERVED**

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 76 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title **RESERVED**

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 77 of 105

BLANK

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Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 78 of 105
--------------------------------	-----------------

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Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 79 of 105
--------------------------------	-----------------

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Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 80 of 105
--------------------------------	-----------------

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Title **RESERVED**

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 81 of 105

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Title
RESERVED

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 82 of 105

BLANK

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Title
RESERVED

Size A4	Document Number LKL-1	Rev 2A
------------	---------------------------------	------------------

Date: Friday, January 19, 2018	Sheet 83 of 105
--------------------------------	-----------------

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Title
RESERVED

Size
A4

Document Number
LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 84 of 105

BLANK

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GPU CORE

Size
A4

Document Number

LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 85 of 105

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GPU Discrete Power

Size
A4

Document Number

LKL-1

Rev
2A

Date: Friday, January 19, 2018

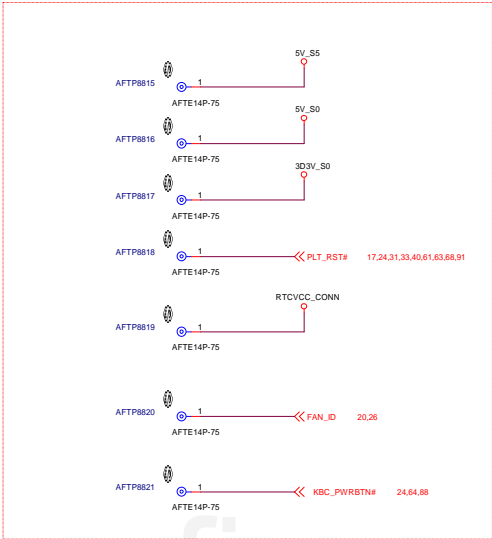
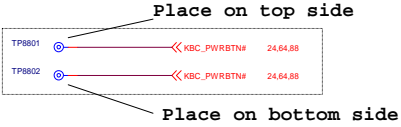
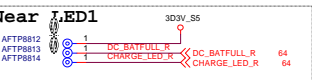
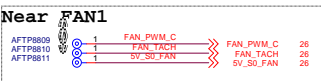
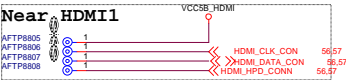
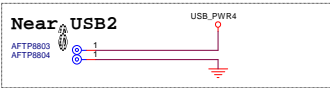
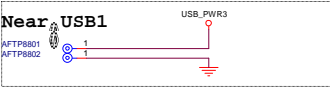
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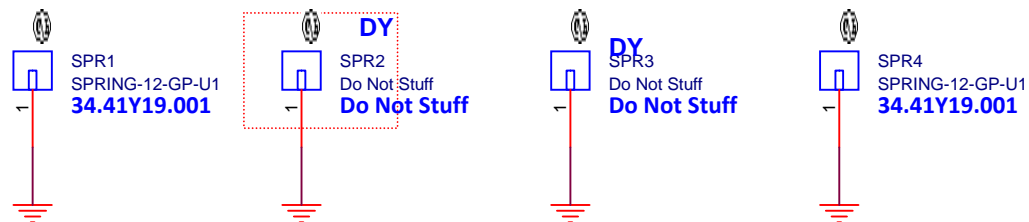
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Title			
Reserved			
Size	Document Number		Rev
A4	LKL-1		2A
Date: Friday, January 19, 2018		Sheet 87 of	105



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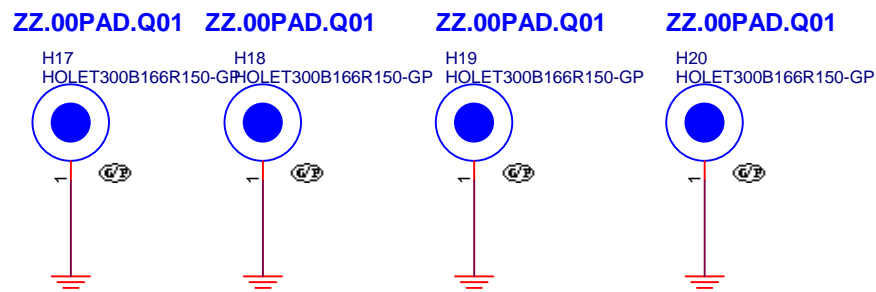
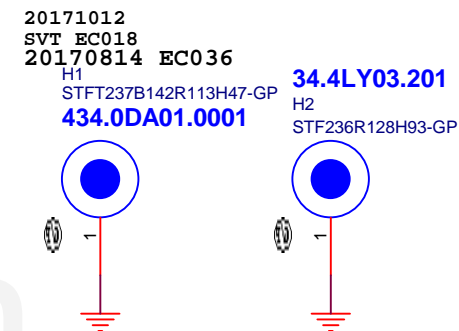
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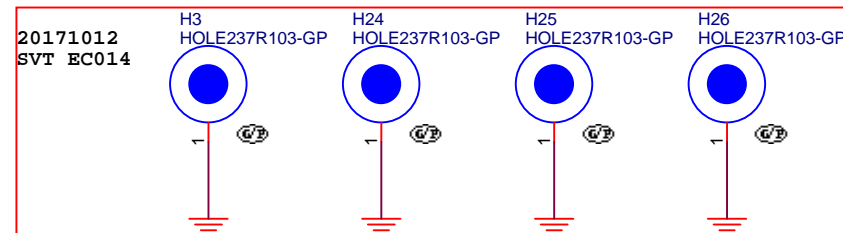
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20170822
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SIT EC043



34.4H602.00134.4H602.001



20170822
SIT EC046

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UNUSED PARTS/EMI Capacitors

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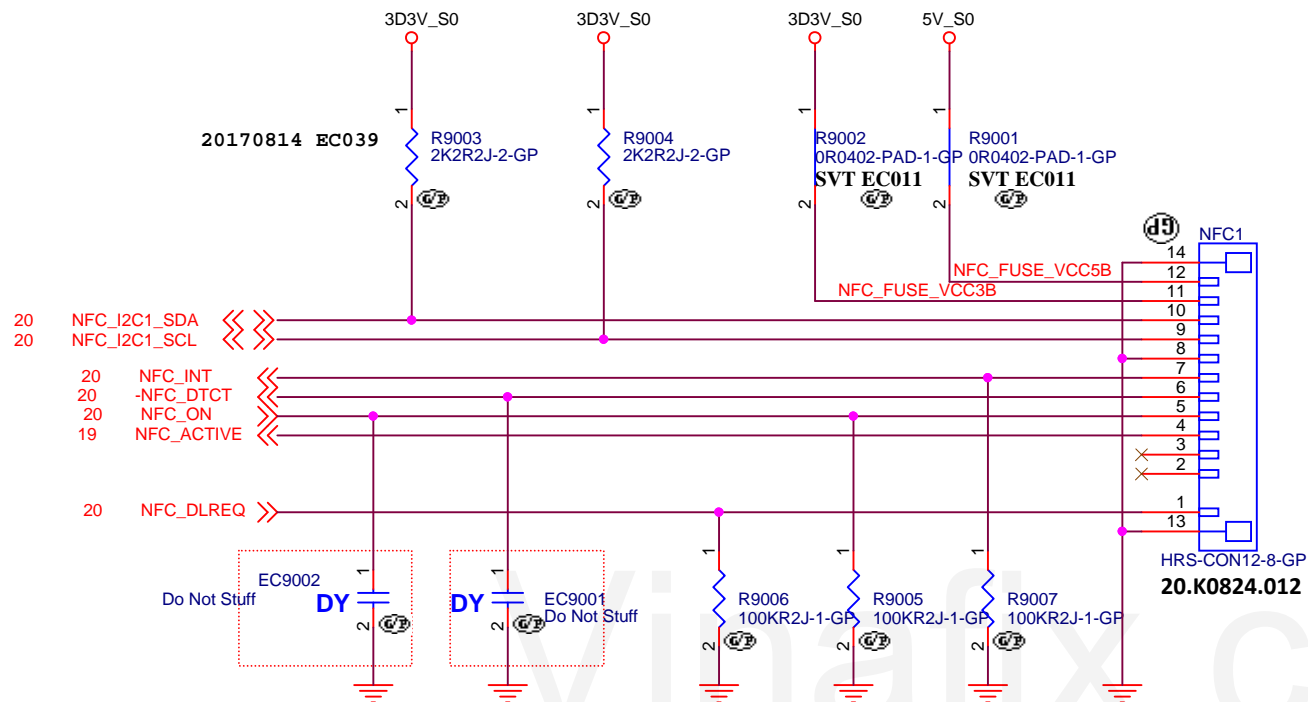
Document Number

LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 89 of 105



TO NFC

20170811 EC029 20170808 EC021
EMC request EMC request

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V - 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UIICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Vinafix.com Remark: P - power supply, G - ground, I - input, O - output, I/O - input/output

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NFC

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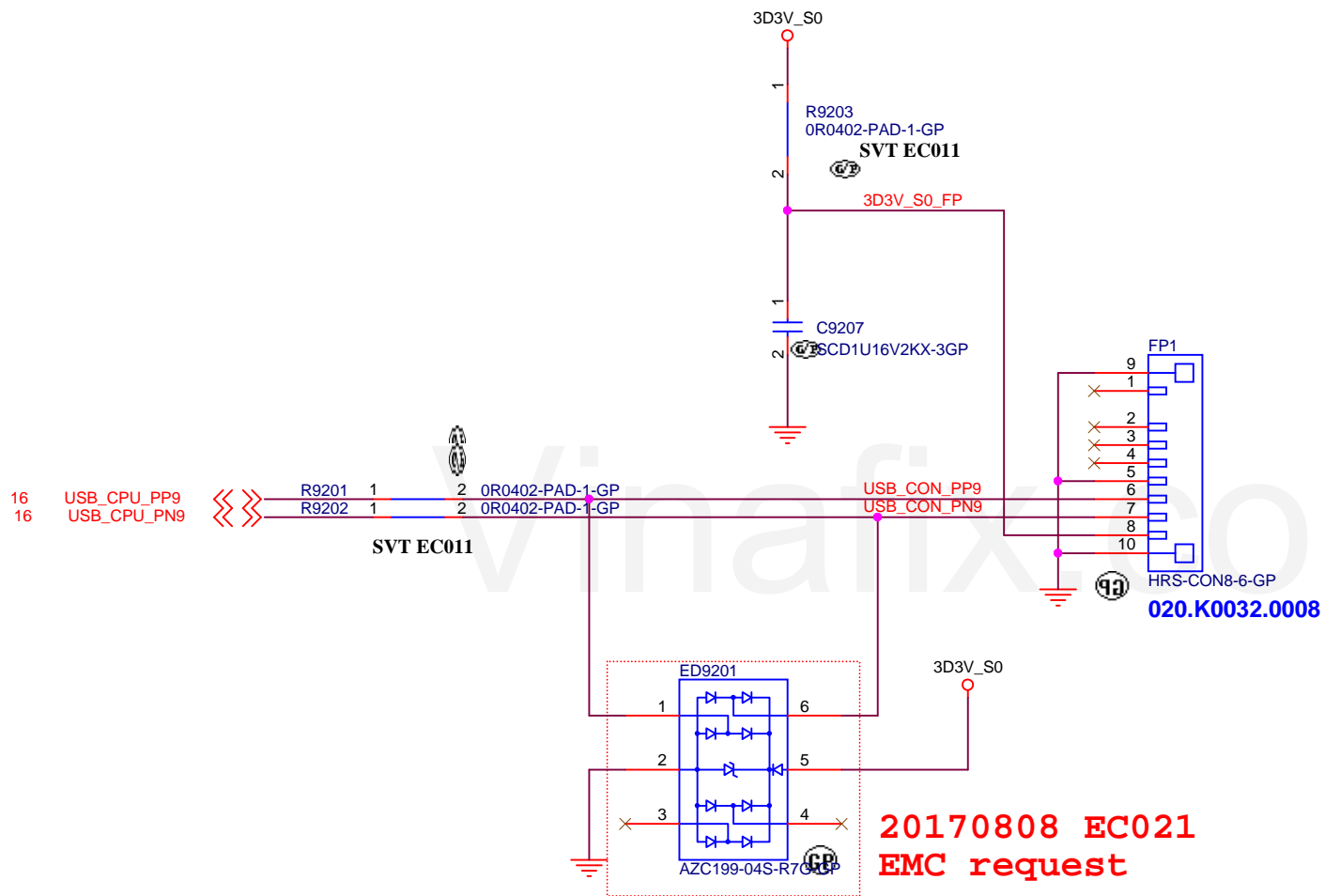
Document Number

LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 90 of 105



20170808 EC021
EMC request

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Title

Reserved

Size
A4

Document Number

LKL-1

Rev
2A

Date: Friday, January 19, 2018

Sheet 92 of 105

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<div>Date</div> <div>Friday, January 19, 2018</div>		<div>Sheet</div> <div>93</div>	<div>of</div> <div>105</div>

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緯創資通		Wistron Corporation	
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Title			
Reserved			
Size A4	Document Number LKL-1		Rev 2A
Date:	Friday, January 19, 2018	Sheet 94 of	105

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Size <div>A4</div>	Document Number <div>LKL-1</div>	Rev <div>2A</div>
Date <div>Friday, January 19, 2018</div>		Sheet <div>95</div> of <div>105</div>

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緯創資通		Wistron Corporation	
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Title			
Reserved			
Size	Document Number		Rev
A4	LKL-1		2A
Date: Friday, January 19, 2018		Sheet 96 of	105

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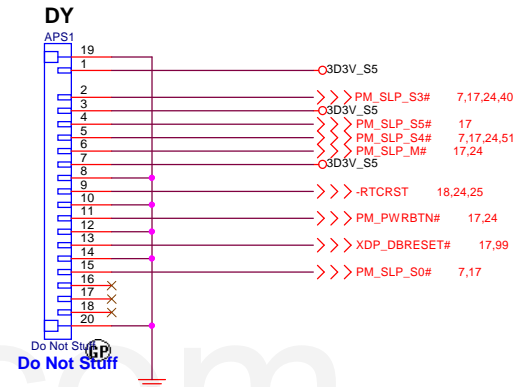
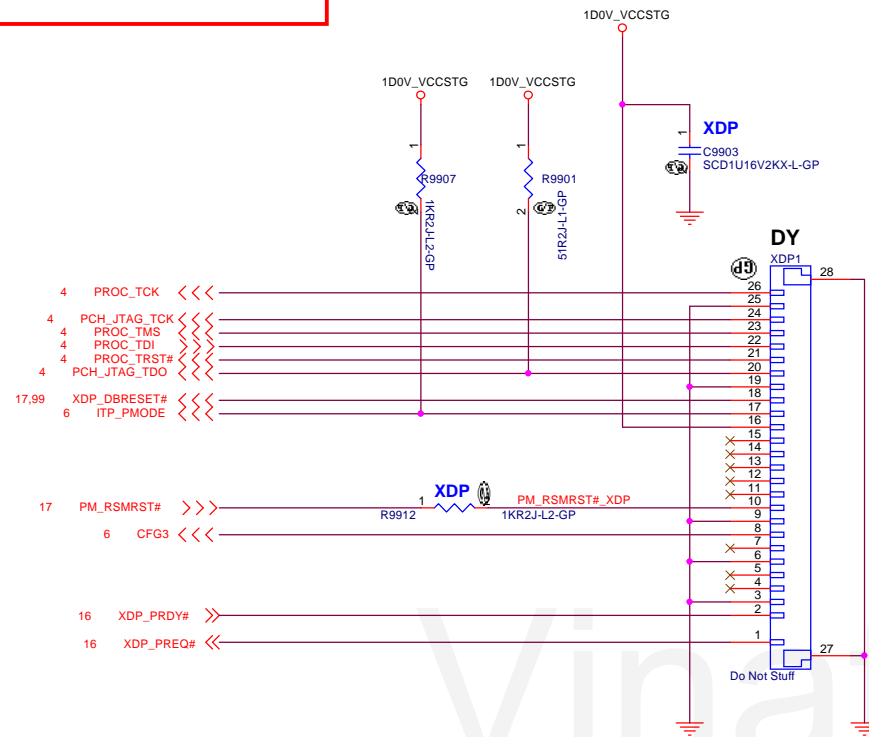
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Title Reserved			
Size A4	Document Number LKL-1		Rev 2A
Date: Friday, January 19, 2018		Sheet 97 of	105

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