Model Name : 2020 G1TGL13"X360 Project
Name : GPT32
File Name : LA-K261P

Compal LA-K261P

GPT32 MB Schematic Document

TIGER LAKE-U(4+2)-DDR4

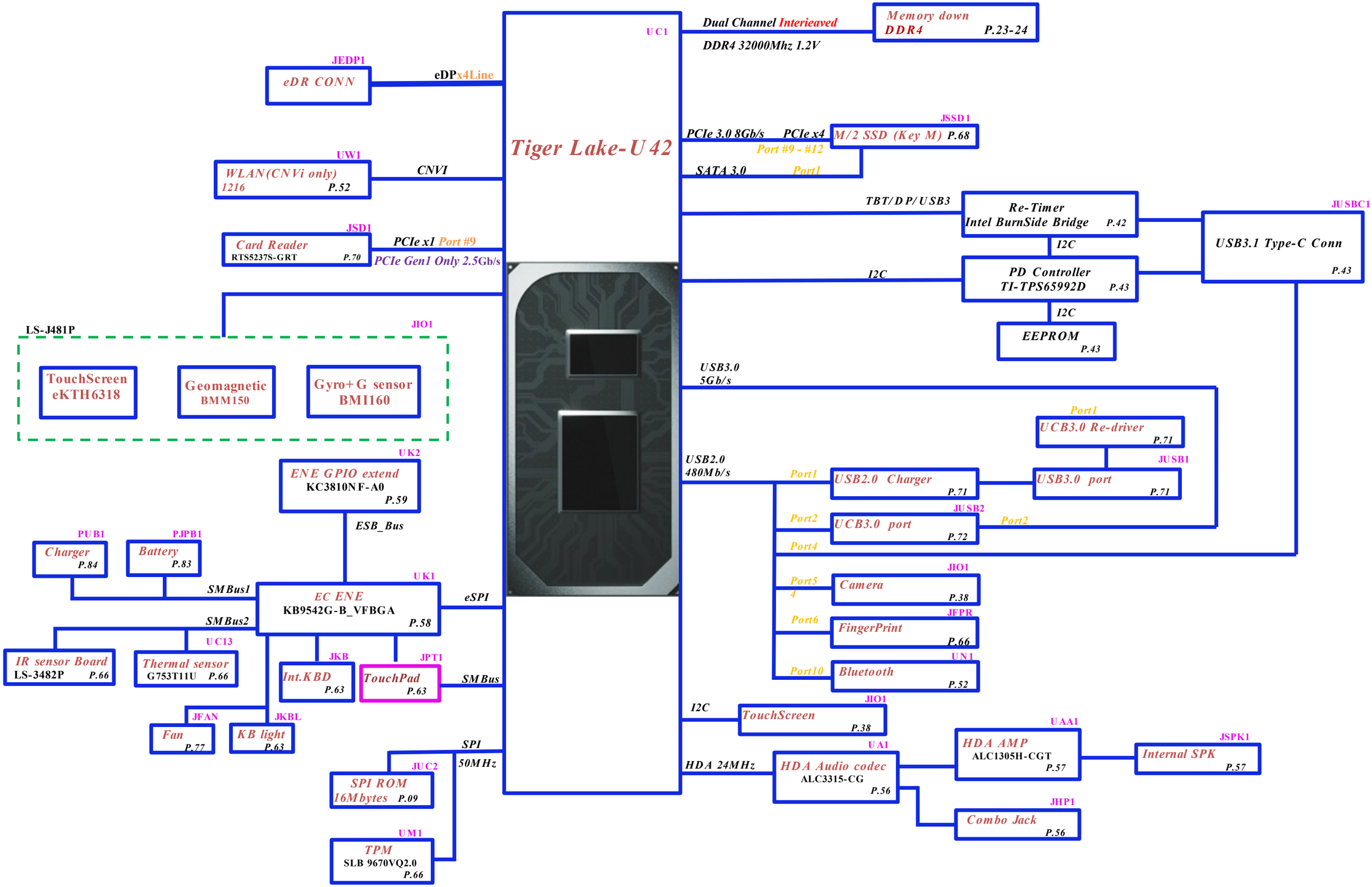
MEMORY DOWN X2(1.0MM_10L)

Rev: 1.0

2020.08.11

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size	Document Number: *LA-K261P*	Rev: 1.0
Date: Friday, August 14, 2020	Sheet 1 of 100	



Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.			
Title: Block Diagrams			
Size	Document Number: LA-K261P		Rev: 1.0
Date: Friday, August 14, 2020	Sheet 2 of 100		

Power Map

ACIN/Type-C Adapter

CHARGER ISL9538BHRTZ-T _TQFN32_4X4 PUB1

BATTERY

+3V_LID

+12.6VB

+12.6VB → IMVP8 VR RT3613EEGQW-02 _WQFN32_4X4 PUZ1 (EN:DRVEN_VCCIN) → +VCCIN — CPU

+12.6VB → RT6543AGQW _WQFN20_3X3 PUG1 (EN:+1.8V_PG) → +VCCIN_AUX — CPU

+12.6VB → G5616BRZ1U _TQFN20_3X3 PUM1 (S3 EN:SM_PG_CTRL)
- → +0.6VS_VTT (PJM3) — DDR
- → +1.2V_VDDQ (PJM2) — CPU DDR (S5 EN:PG_+2.5V, S5 EN:PM_SLP_S4#)

+12.6VB → FUSE MF-MSMF075/24-2 0.75A 24VUL/TUV FU2 → INVPWR_B+ — LCD

+12.6VB → SY8388BRHC _QFN16_2P5X2P5 PU301 (EN: ENLDO_3V5V, MAINPWON)
- → +3VALWP → PJ302 → +3VALW_LPH
- → +3VLP → PJ303 → +3VL
- → SPOK

+3VALW_LPH → SY8032IABC _SOT23-6 PU2501 (EN:PM_SLP_S4#) → +2.5V (PJ2502) — DDR (PG:PG_+2.5V)

+3VALW_LPH → EM5209VF _DFN14_3X2 U4021 (EN:SUSP#) → +3VS

+3VS → +3VS

+3VALW_LPH → JPLPH1 → +3VALW_LPH_R → AOZ1336_ DFN8_2X2 LPHU2 LPH@ (EN:EC_ON) → +3VALW

+3VALW →
- AOZ1336 _DFN8_2X2 UC15 (EN:PCH_PWR_EN)
  - +3V_PRIM → RC217 → +3V_PRIM_SOC — CPU
  - +3V_PRIM → RM4 → +3VS_TPM — TPM
- AOZ1336DI _DFN8_2X2 UT1 (EN:TBT_RETIMER_0_LS_EN) → +3VS_RETIMER_0 — TBT BURNSIDE-BRIDGE
- RT1130 → +3V_TBT_FLASH — TBT FLASH ROM
- QWL1 → +3VS_WLAN — WLAN
- LPHR2 → +3VALW_EC — EC
- RC216 → +3VALW_DSW — CPU

+3VALW_LPH → SY8032IABC _SOT23-6 PU1801 (EN:PCH_PWR_EN) → +1.8V_PRIM
- RT83 → +1.8V_MIC_VCC — MIC
- RC219 → +1.8V_PRIM_MCP — CPU
- Q18 (EN:SUSP) → +1.8VS
  - RAA1 RAA2 → +1.8VS_AVDD
  - LA4 → +1.8VS_AVDD

+12.6VB → LAA5 LAA6 → AMP. ALC1305H-CGT UAA1

+12.6VB → SY8288CRAC _QFN20_3X3 PU302 (EN: ENLDO_3V5V, MAINPWON)
- → +5VALWP → PJ305 → +5VALW
- → +5VLP → PJ306 → +5VL

+5VALW → EM5209VF _DFN14_3X2 U4021 (EN:SUSP#) → +5VS
- LA5 LA7 → AUDIO ALC3315-CG UA1
- R24 → +5VS_KBL — Keyboard Backlight
- R5261 R5262 → +5VS_FAN — FAN

+5VALW → AON7408L US3 → +2546PWR — USB Charger

+5VALW → G517G1TO1U US2 → +USB_VCCA — USB CONN.

+5VALW → SY6288F1ABC PUI1 → +3VS_SHUTTER — SHUTTER DOOR

+5VALW → APW8743CQBI-TRG _TQFN16_3X3 PU1001 (EN:PG_AUX)
- → +1.05VO_VNNBYPASS
- → +1.05VO_EXTBYPASS — CPU

+3VS →
- G517AH1TP1U UG1 (EN:SOC_ENVDD) → +LCDVDD — LCD
- G517AH1TP1U FG4 (EN:TS_PWR_EN) → +3VS_TOUCH — Touch screen
- G517AH1TP1U UG2 (EN:CAM_PWR_EN) → +3VS_CAMERA — CAMERA
- LA3 RA5 → +3VDS_AUDIO +DVDD — AUDIO
- RAA3 → +3VS_DVDD_IO — AMP.
- R6562 → +3V_TP — ClickPad
- R6603 → +3VS_IR — IR THERMAL SENSOR
- RF1 → +3V_FPR — Finger Printer
- THERMAL SENSOR
- JHW9 → +3VS_SSD — SSD
- RR1 → +3VS_CR — Card Reader
- RB85 → +3VS_8713 — USB3 Redriver

+3VL → DC1 → +RTCVCC → RC462 → +3V_LID

EC KB9542G-F _VFBGA124
- VCC_LPC ← +1.8V_PRIM (RK215) → +1.8VCC_LPC_EC
- VCC0 ← +3V_LID (RK301) → +3V_LID_EC
- VCC1 UK1 ← +3VL (LPHR2) → +3VALW_EC
- VCC2
- VCC_IO2

KC3810NF (UK2)

6K0020A (UU300)

+3VALW_LPH → PCF8563T-5_SO8 (LPHU1) — Timer

+3VL, +3V_LID → Hall sensor U4018

+3VL → RT67 → PD PTPS65992DADRJKT _WQFN_4X6 UT4
- LDO_1V5 → +1.5V_TBTA_PDLDO
- LDO_3V3 → +3V_TBTA_PDLDO

SPI ROM UT13 ← RT1201

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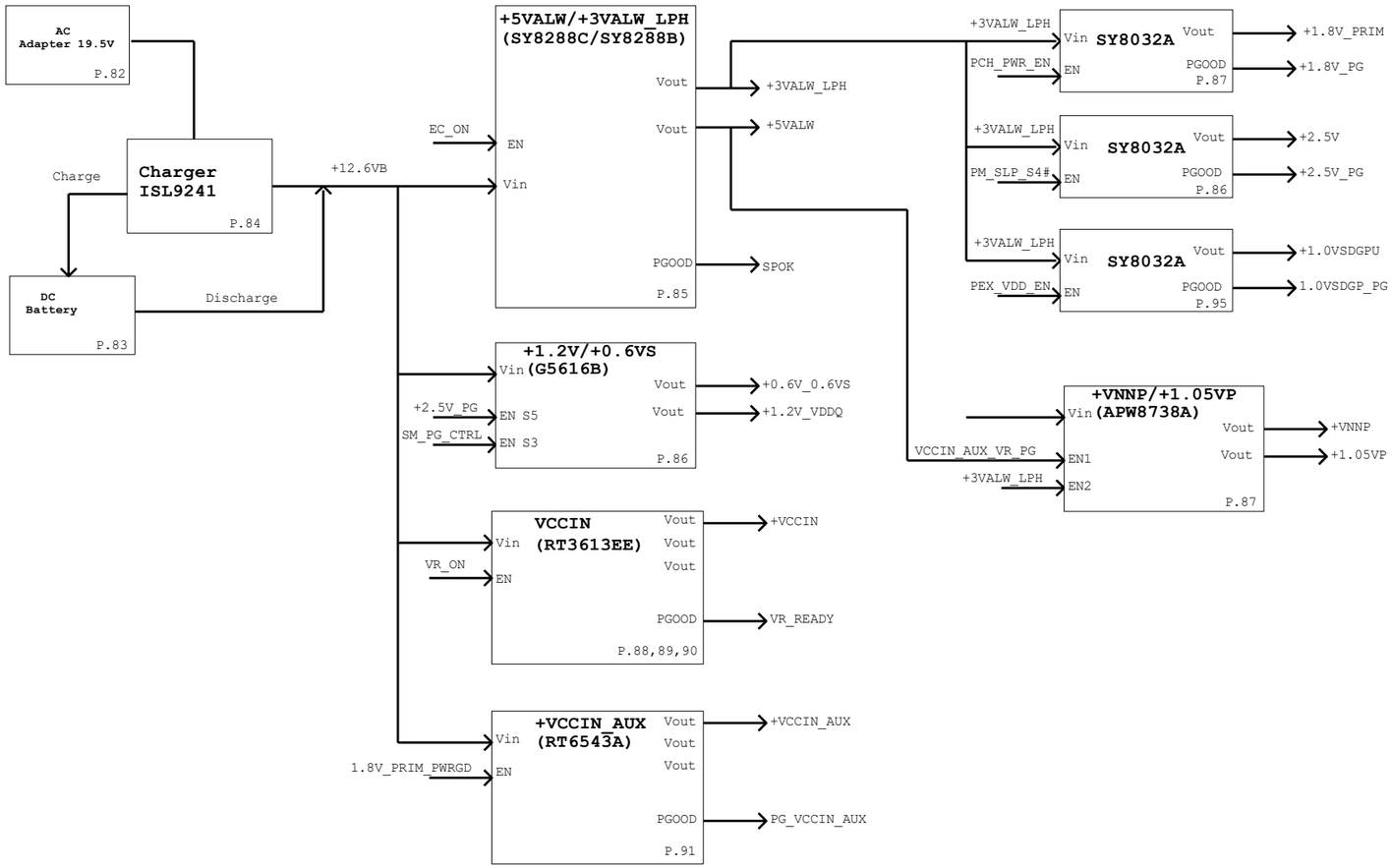
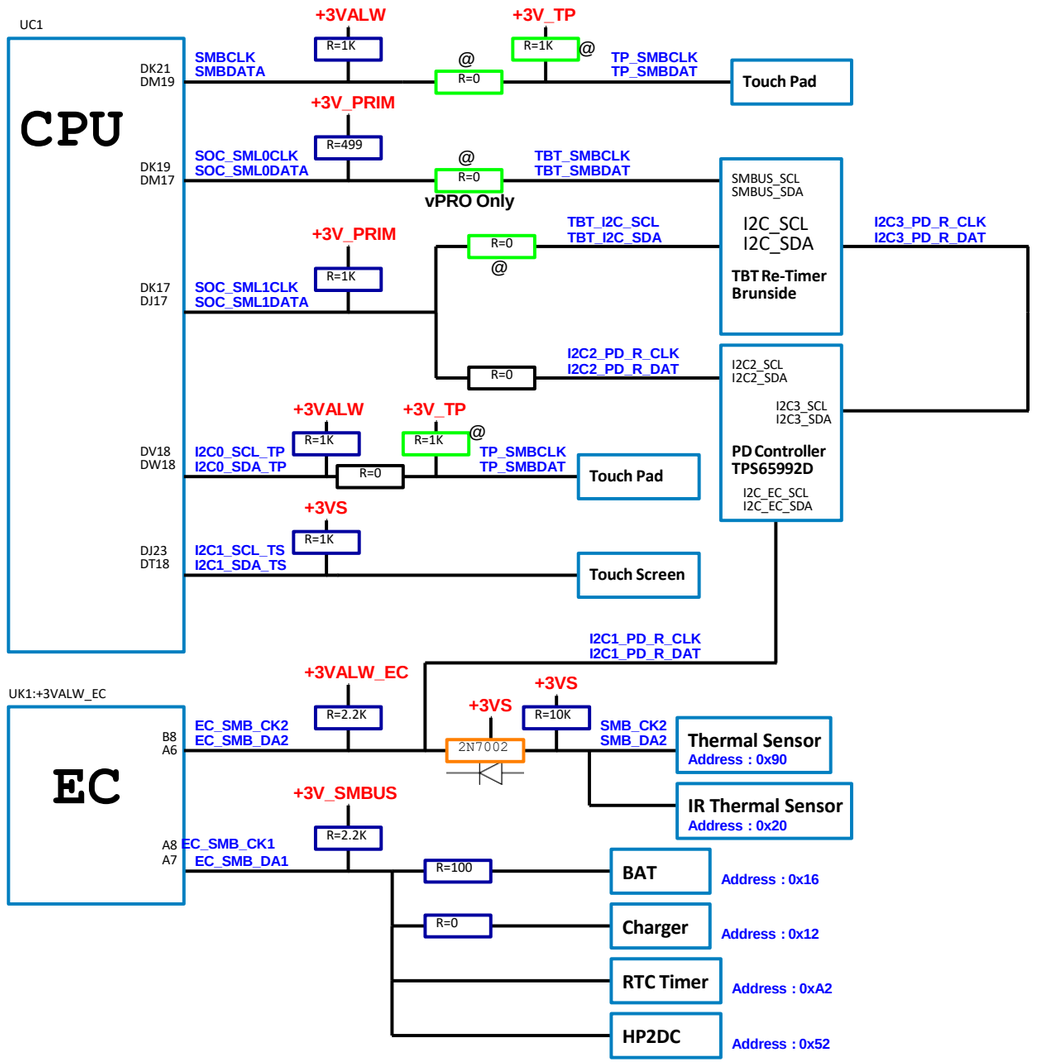
Issued Date	2019/11/29	Deciphered Date	2020/12/31
Title: Power MAP			
Document Number: LA-J474P			Rev: 0.2
Date: Friday, August 14, 2020		Sheet 4 of 100	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title: Power Block Diagram

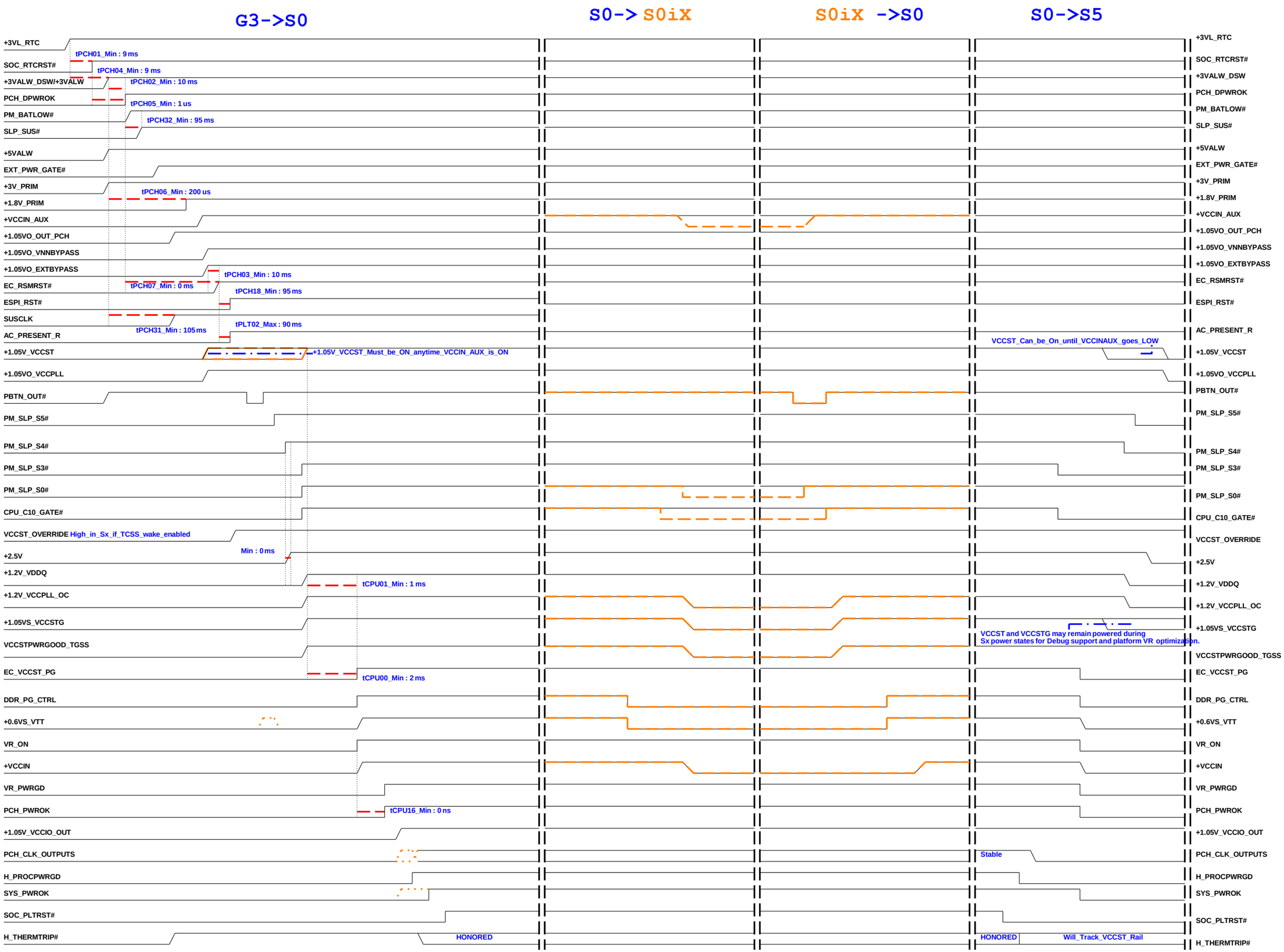
Size: LCIse	Document Number: 2019OPP ICL		Rev: 0.1
Date: Friday, August 14, 2020	Sheet 81 of 100		



Compal Electronics, Inc.		
Title: Notes List		
Size: Custom	Document Number: LA-K261P	Rev: 0.3
Date: Friday, August 14, 2020	Sheet 3 of 100	

[FQA01-PWR Sequence_TGL-UP3_DDR4_Volume_S0iX]

Will be Update



Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **Power Sequence**

Size: | Document Number: **LA-K261P** | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 5 of 100

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

SOC SMBUS Address Table

SOS_SMBUS Net Name	Power Rail	Device	Addres(7bit)	Addres(8bit)	
				Write	Read
SOC_SMDCLK SOC_SMDDATA	+3V_PRIM	TP (Reserve)	0x2C	0x58	0x59
SOC_SMDCLK SOC_SMDDATA	+3V_PRIM	NC	TBC	TBC	TBC
SOC_SMDCLK SOC_SMDDATA	+3V_PRIM	PDxxxx	0x23	0x46	0x47

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8 bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VL_EC	BAT	0x0B	0x16	0x17
		CHGR	0x09	0x12	0x13
		Timer	0x51	0xA2	0xA3
EC_SMB_CK2 EC_SMB_DA2	+3VL	PD	0x23	0x46	0x47
	+3VS	Thermal Sensor	0x48	0x90	0x91
		IR Sensor	0x10	0x20	0x21
EC_SMB_CK3 EC_SMB_DA3	+3VS_SHUTTER	ShutterMCU	0x64 0x4E	0xC9 0x0D	0xCA 0x9E
	+3VALW	BMI160 [G+Gyro]	0x68	0xD0	0xD0
		BMM150 [Geometric]	0x11	0x22	0x23

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0(S/B)
2	USB3.0(S/B)
3	X
4	Type-C (TBT)
5	Camera
6	FPR
7	X
8	X
9	X
10	Bluetooth

BOM Structure Table (1/2)

Function	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION		CLK
0	1		1	USB3.0(S/B)		
1	2		2	USB3.0(S/B)		
2	3		3			X
3	4		4	Card Reader		CLK2
4	5					
5	6					
6	7					
7	8					
8	9					
9	10					
10	11	0				X
11	12	1a				X
12	13			PCIe x4	X	CLK3
13	14					
14	15					
15	16	2			SATA SSD	X

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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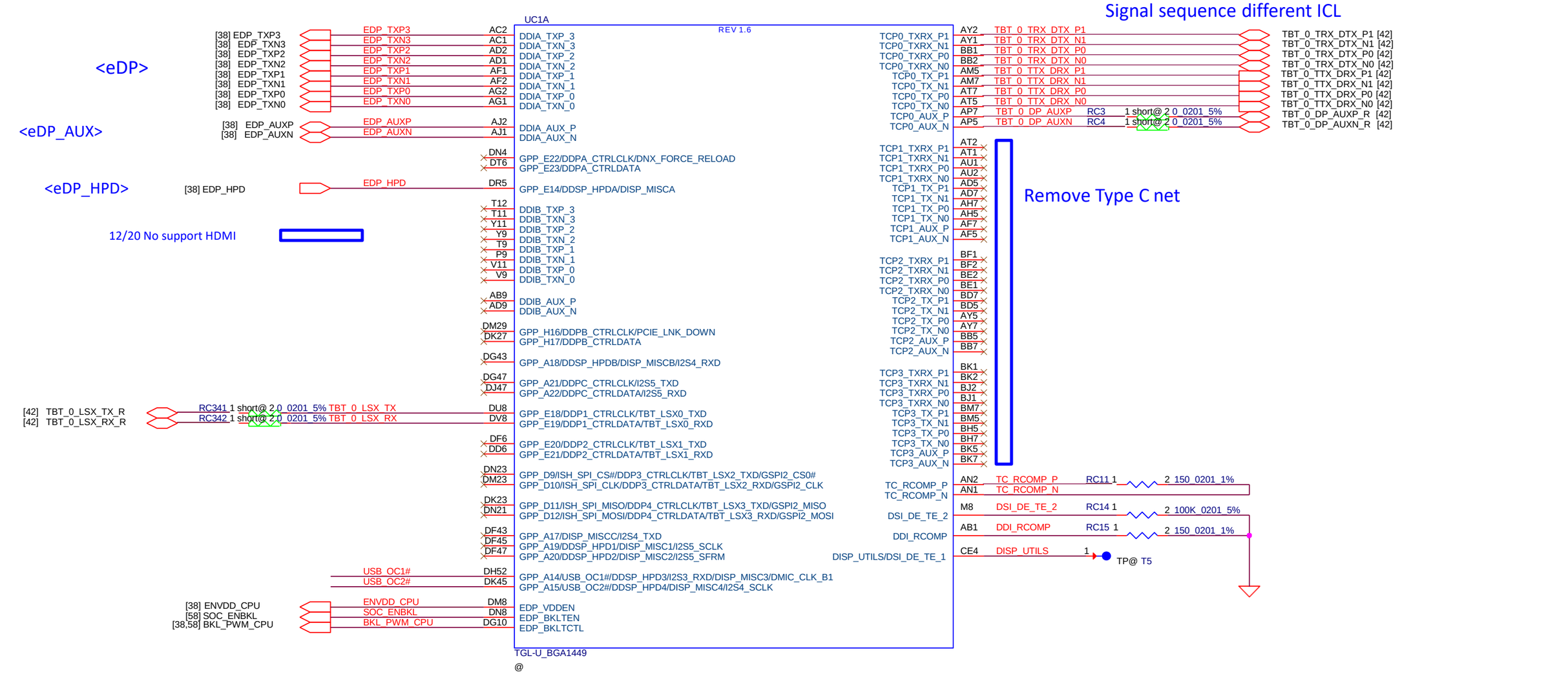
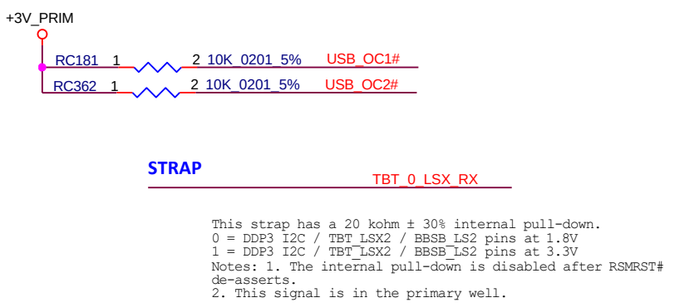
Title: Notes List

Size: Custom | Document Number: LA-K261P | Rev: 1.0

Date: Friday, August 14, 2020 | Sheet 6 of 100





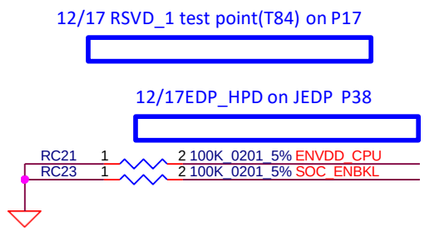


Table 32. USB3/USB2 Port Pairing for USB-C* Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.

Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(1/14)DDI,EDP

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12/9 Remove SOC_GPP_E7 reserved @PH

+1.05V_VCCST

RC26 1 — 2 CATERR# 1K_0201_5%

RC27 2 — 1 H_THERMTRIP# 1K_0201_5%

CC2 2 — 1 0.1U_0201_10V6K @ESD@

+1.05VS_VCCSTG_OUT_LGC_TERM

RC24 1K_0201_5%

[58,84] H_PROCHOT# — RC25 1 — 2 499_0201_1%

[58] H_PECI

CC1 ESD@ 100P_0201_50V8J

T6 TP@

T7 TP@

[63] I2C_INT#_TP

UC1U

REV 1.6

CATERR#	M7	PROC_TRST#	K4 SOC_XDP_TRST#
H_PECI	BK9	PROC_TMS	B9 SOC_XDP_TMS
H_PROCHOT#	E2	PROC_TDO	D12 SOC_XDP_TDO
H_THERMTRIP#	M5	PROC_TDI	A12 SOC_XDP_TDI
PROC_POPIRCOMP	CT39	PROC_TCK	B6 SOC_XDP_TCK0
PCH_OPIRCOMP	CB9	PCH_JTAGX	D8 SOC_XDP_TCK0
SOC_TP_1	CW12	PCH_TMS	A9 SOC_XDP_TMS
SOC_TP_2	CM39	PCH_TDO	E12 SOC_XDP_TDO
XDP_ITP_PMODE	DF4	PCH_TDI	B12 SOC_XDP_TDI
	DB42	PCH_TCK	A7 PCH_JTAG_TCK1
I2C_INT#_TP	DB41	PCH_TRST#	H4 SOC_XDP_TRST#
	DF8	PROC_PREQ#	C11 XDP_PREQ#
NMI_DBG#_CPU	DU5	PROC_PRDY#	D11 XDP_PRDY# — TP@ T306
SOC_GPP_H2	DF31	EAR_N/EAR_N_TEST_NCTF	G1 SOC_EAR
SOC_GPP_H1	DV32	GPP_F7	DT15 GPP_F7
SOC_GPP_H0	DW32	GPP_F9	DR15
	DJ27	GPP_F10	DT14 GPP_F10

TGL-U_BGA1449

@

12/25 Remove reserve UART_BT_WAKE#

+3V_PRIM

GPP_F7 RC33 1 — @ — 2 4.7K_0201_5%

GPP_F10 RC39 1 — @ — 2 4.7K_0201_5%

RC30 2 — 1 PROC_POPIRCOMP 49.9_0201_1%

RC31 2 — 1 PCH_OPIRCOMP 49.9_0201_1%

+3V_PRIM

RC4027 10K_0201_5%

[59] NMI_DBG#_CPU — NMI_DBG#_CPU

+3V_PRIM

RC32 100K_0201_5%

[17,43] VCCIN_AUX_CORE_ALERT#_R — DC9 — H_PROCHOT#

RB751S-40_SOD523-2

SOC_WWAN_WAKE#--->GPP_F7

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

INTERNAL PD 20K

12/9 Del SOC_WWAN_WAKE#--->GPP_F7, @ PH and @PD

+1.05VS_VCCSTG

12/18 Check RC34 is CMC@?

RC34 1K_0201_5%

SOC_EAR

RC38 1K_0201_5% @

12/18 SOC_EAR for CFG0_R CMC conn

SOC_WWAN_RST#-->GPP_F10

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

INTERNAL PD 20K

12/9 Del SOC_WWAN_RST#-->GPP_F10, @PD

12/16 RC42 GLITCH@-->SMT

12/9 SOC_WWAN_OFF#_SW-->GPP_F9

SOC_GPP_H2
BOOT STRAP3 - BIT3
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H1
BOOT STRAP1 - BIT2
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H0
BOOT STRAP1 - BIT1
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

+3V_PRIM

RC35 1 @ 2 4.7K_0201_5% SOC_GPP_H2

RC36 1 @ 2 4.7K_0201_5% SOC_GPP_H1

RC296 1 @ 2 4.7K_0201_5% SOC_GPP_H0

H_PECI CC3 2 — 1 0.1U_0201_10V6K @ESD@

SOC_XDP_TRST# CC4 2 — 1 0.1U_0201_10V6K @ESD@

SOC_XDP_TDO CC5 2 — 1 0.1U_0201_10V6K @ESD@

SOC_XDP_TDI CC6 2 — 1 0.1U_0201_10V6K @ESD@

12/9 Modify ORB P79-->P07 12/9 Check CMC@ SMT or not

+1.05VO_OUT_FET

RC2601 CMC@ 2 — 1K_0201_5% XDP_ITP_PMODE

RC2631 @ 2 — 1K_0201_5%

RC2671 CMC@ 2 — 51_0201_5% SOC_XDP_TCK0

XDP_ITP_PMODE
DFX TEST MODE
INTERNAL PU 20K
This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.

RC2701 @ 2 — 51_0201_5% PCH_JTAG_TCK1

RC2731 @ 2 — 51_0201_5% SOC_XDP_TRST#

+1.05VS_VCCSTG_OUT_LGC_TERM

RC2471 CMC@ 2 — 51_0201_5% SOC_XDP_TMS

RC2481 CMC@ 2 — 51_0201_5% SOC_XDP_TDI

RC2531 CMC@ 2 — 100_0201_5% SOC_XDP_TDO

RC2551 @ 2 — 51_0201_5% XDP_PREQ#

12/9 Modify CFG0 CFG7 CFG14 on CPU CFG Page 19

Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(1/14)DDI,MSIC,XDP

Size: — Document Number: LA-K261P — Rev: 0.3

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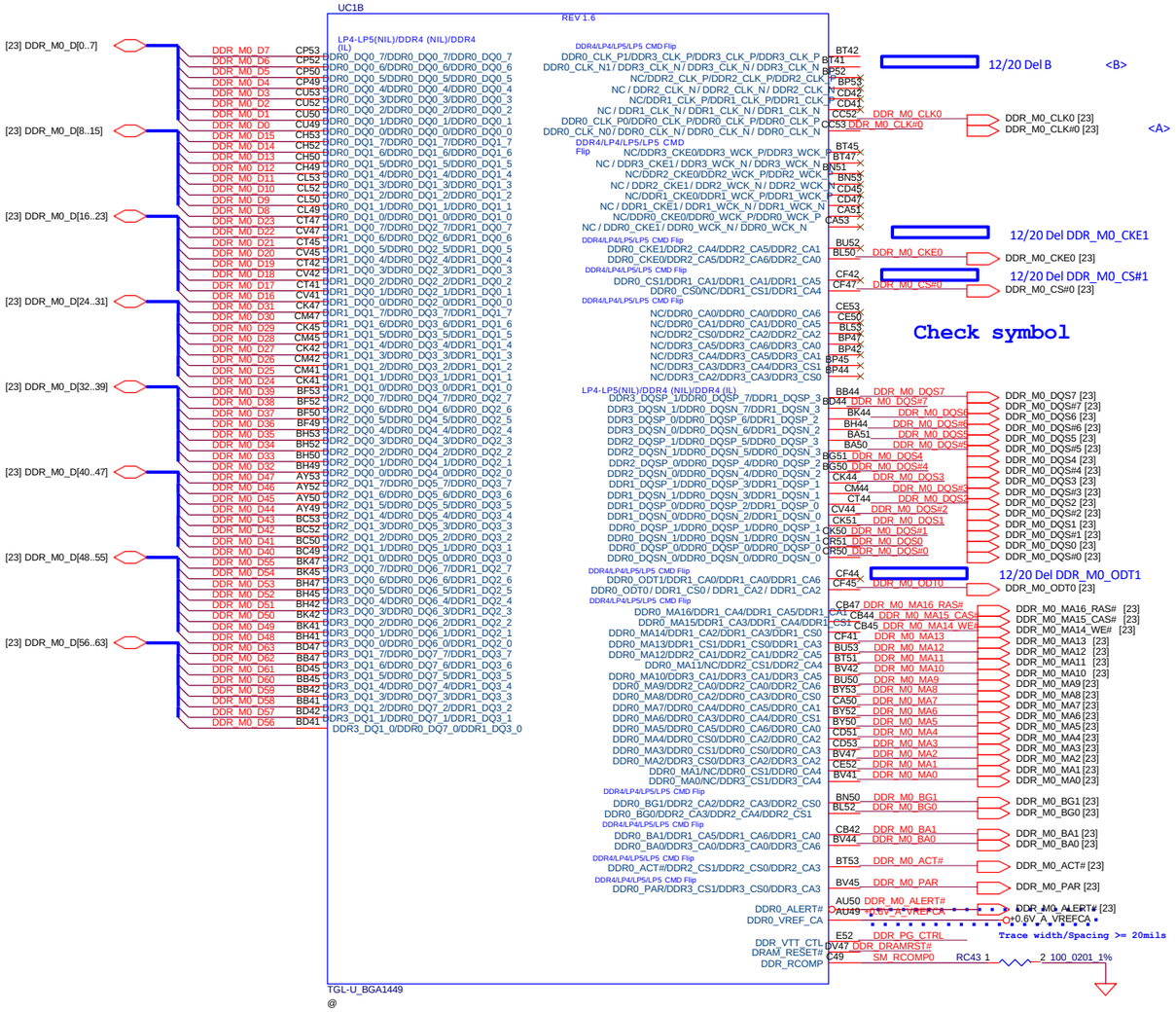
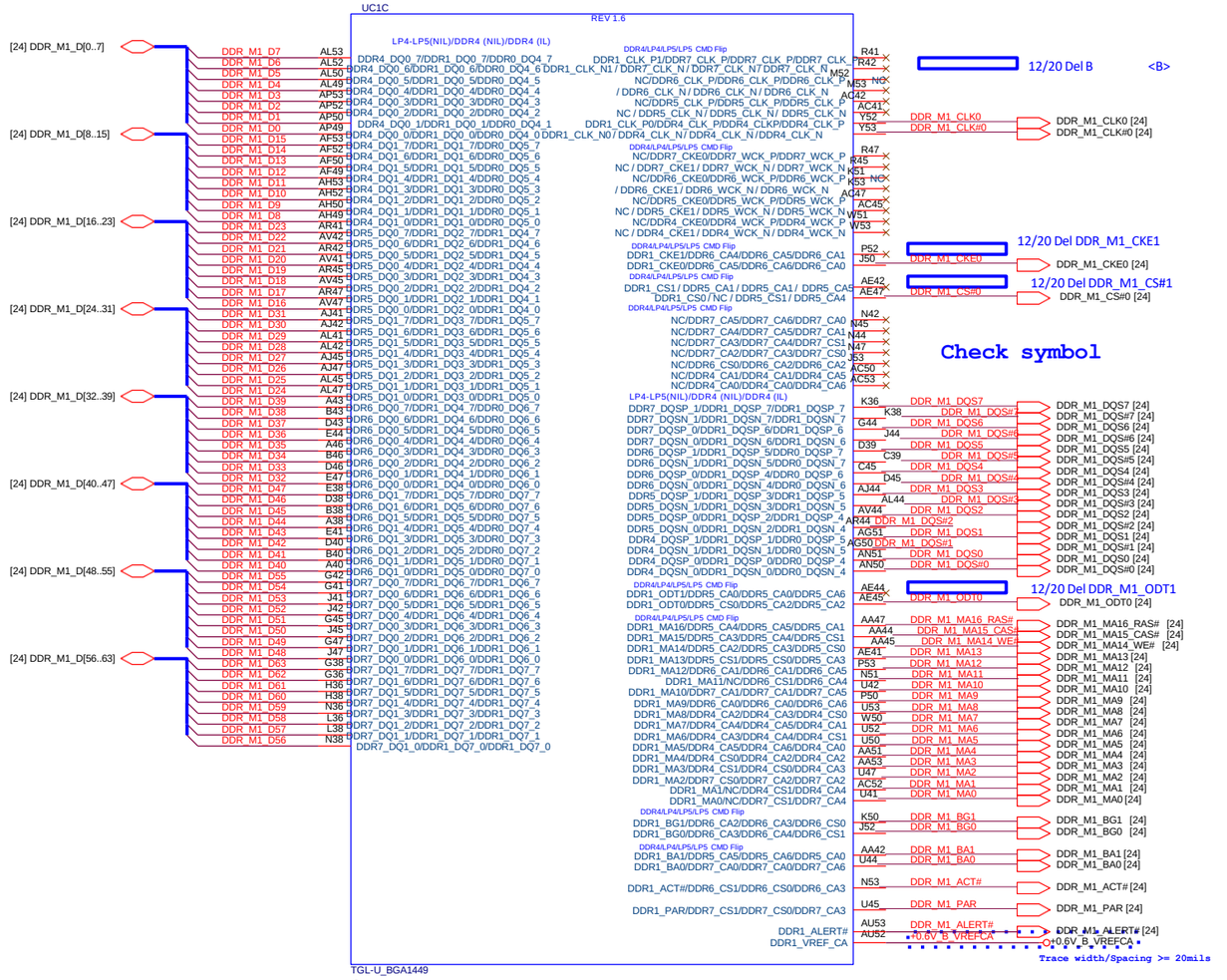
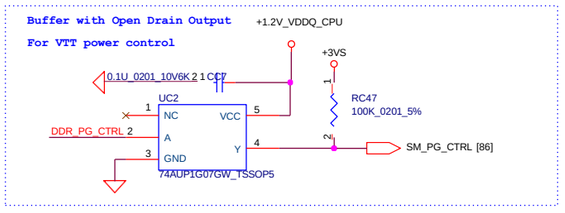
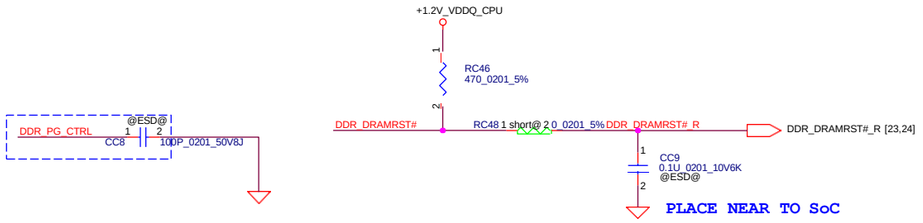
Follow Intel DDR4 NIL

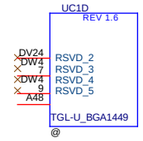
DDR4: Refer to 609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5





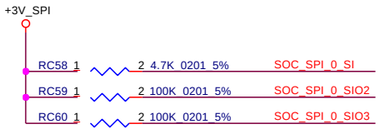






Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

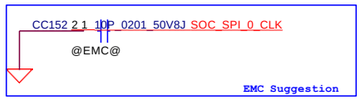
Compal Electronics, Inc.	
Title: TGL-UP3(3/14)DDR4	
Size:	Document Number: LA-K261P
Rev: 0.3	
Date: Friday, August 14, 2020	Sheet 8 of 100



SOC_SPI_0_SI
BOOT HALT
NO INTERNALPU/PD
HIGH: ENABLED
LOW: DISABLED

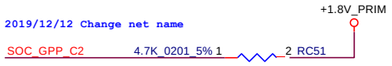
SOC_SPI_0_SIO2
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
NO INTERNAL PU/PD

SOC_SPI_0_SIO3
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
NO INTERNAL PU/PD



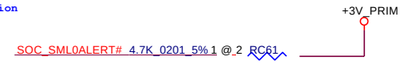
SOC_GPP_C2
TLS CONFIDENTIALITY
INTERNAL PD 20K
HIGH: TLS CONFIDENTIALITY ENABLE
LOW: TLS CONFIDENTIALITY DISABLE(Default)

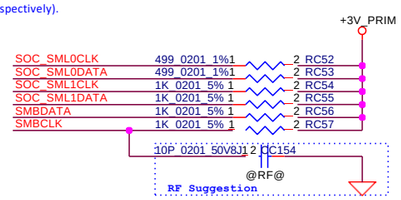
2019/12/12 Change net name

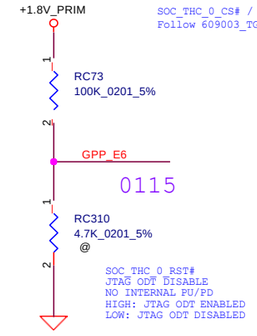


RVP is different from EDS description

SOC_SML0ALERT#
ESPI OR EC LESS
INTERNAL PD 20K
HIGH: ESPI DISABLE
LOW: ESPI ENABLE
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).







SOC_THC_0_CS# / SOC_THC_0_CLK
Follow 609003_TGL_U_DDR4_SODIMM_RVP_SCH

SOC_THC_0_RST#
JTAG ODT DISABLE
NO INTERNAL PU/PD
HIGH: JTAG ODT ENABLED
LOW: JTAG ODT DISABLED

<TPM>
<TPM>
<TPM>

[66] SOC_SPI_0_CLK
[66] SOC_SPI_0_SO
[66] SOC_SPI_0_SI
T12 TP@
[66] SOC_SPI_0_CS2#

[58] EC_SLP_S0IX#
[38] TS_INT#

UC1E
REV 1.6

SOC_SPI_0_CLK	DJ37	SPI0_CLK
SOC_SPI_0_SIO3	DG35	SPI0_IO3
SOC_SPI_0_SIO2	DJ39	SPI0_IO2
SOC_SPI_0_SO	DJ33	SPI0_MISO
SOC_SPI_0_SI	DJ35	SPI0_MOSI
SOC_SPI_0_CS1#	DF35	SPI0_CS1#
SOC_SPI_0_CS0#	DG37	SPI0_CS0#
SOC_SPI_0_CS2#	DF39	SPI0_CS2#
	DJ6	GPP_E11 / THC0_SPI1_CLK
EC_SLP_S0IX#	DN5	GPP_E2 / THC0_SPI1_IO3
TS_INT#	DR9	GPP_E1 / THC0_SPI1_IO2
SOC_GPP_E12	DM6	GPP_E12 / THC0_SPI1_IO1
SOC_GPP_E13	DK6	GPP_E13 / THC0_SPI1_IO0
	DK8	GPP_E10 /THC0_SPI1_CS#
	DV11	GPP_E8 / SATA_LED#
	DW9	GPP_E17/THC0_SPI1_INT#
GPP_E6	DT8	GPP_E6/THC0_SPI1_RST#
	DN15	GPP_F11/THC1_SPI2_CLK
	DK13	GPP_F15/GSXSRESET#/THC1_SPI2_IO3
	DM13	GPP_F14/GSXDIN/THC1_SPI2_IO2
	DN13	GPP_F13/GSXSLOAD/THC1_SPI2_IO1
	DJ15	GPP_F12/GSXDOUT/THC1_SPI2_IO0
	DK15	GPP_F16/GSXCLK/THC1_SPI2_CS#
	DN10	GPP_F18/THC1_SPI2_INT#
	DV14	GPP_F17/THC1_SPI2_RST#
	DH3	CL_CLK
	DH4	CL_DATA
	DF2	CL_RST#

TGL-U_BGA1449
@

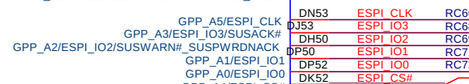
DK21	SMBCLK	GPP_C0/SMBCLK
DM19	SMBDATA	GPP_C1/SMBDATA
DN19	SOC_GPP_C2	GPP_C2/SMBALERT#
DK19	SOC_SML0CLK	GPP_C3/SML0CLK
DM17	SOC_SML0DATA	GPP_C4/SML0DATA
DN17	SOC_SML0ALERT#	GPP_C5/SML0ALERT#
DK17	SOC_SML1CLK	GPP_C6/SML1CLK
DJ17	SOC_SML1DATA	GPP_C7/SML1DATA
CY50	SOC_GPP_B23	GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#
DN53	ESPI_CLK	GPP_A5/ESPI_CLK
DJ53	ESPI_IO3	GPP_A3/ESPI_IO3/SUSACK#
DH50	ESPI_IO2	GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK
DP50	ESPI_IO1	GPP_A1/ESPI_IO1
DP52	ESPI_IO0	GPP_A0/ESPI_IO0
DK52	ESPI_CS#	GPP_A4/ESPI_CS#
DL50	ESPI_RST#	GPP_A6/ESPI_RESET#

SOC_SML0CLK [42]
SOC_SML0DATA [42]

Reserve to Burnside

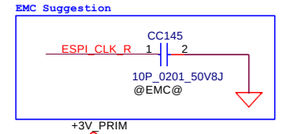
SOC_SML1CLK [42,43]
SOC_SML1DATA [42,43]

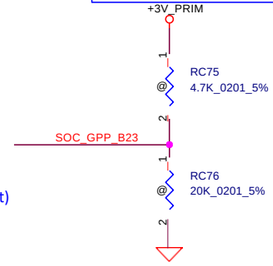
TBT PD



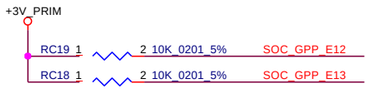
To EC

EMC Suggestion

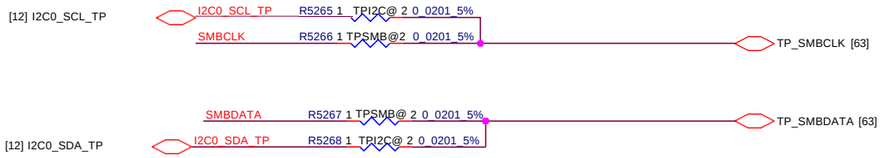


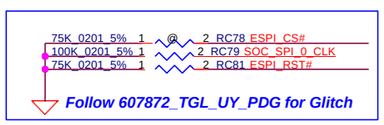


SOC_GPP_B23
CPUNSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 MHz (form internal divider)
LOW: 38.4 MHz (direct form crystal) (Default)



SOC_GPP_E12	SOC_GPP_E13	
L	L	13" CS
L	H	15" X360
H	L	17" CS
H	H	13" X360





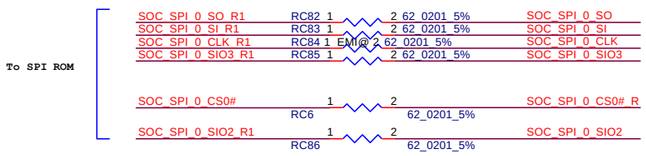
12/16 RC79 GLITCH@-->SMT

12/16 RC81 GLITCH@-->@ Follow 2019 OPP ICL U

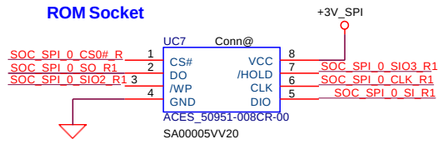
Single SPI ROM_CS0#

Follow 607872_TGL_UY_PDG

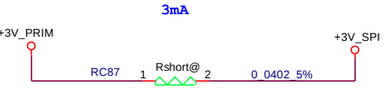
12/10 Check SOC_SPI_0_CS0# R status



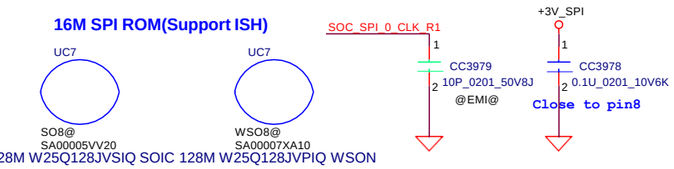
ROM Socket



3mA

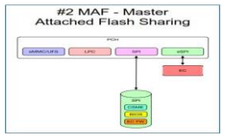


16M SPI ROM(Support ISH)



128M W25Q128JVSIQ SOIC 128M W25Q128JVPIQ WSON

From EC
(For share ROM)



MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus

Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(4/14)SPI,ESPI,SMB,LPC

Size: C | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 9 of 100

2019/12/09
1.Remove SOC_CNVI_EN# (DL53) for Wlan power is EC control
2.Change SOC_GPP_A10 to SERIRQ for TPM
3.Change Net name from CLKREQ_CNV# to XTAL_CLKREQ follow 19 OPP ICL
4.Change Net name from SOC_BT_ON to BT_ON_PCHfollow 19 OPP ICL

UC1G
REV 1.6

DW15	GPP_F8/I2S_MCLK2_INOUT	GPP_R0/HDA_BCLK/I2S0_SCLK	DR38 HDA_BIT_CLK
DW24	GPP_D19/I2S_MCLK1	GPP_R1/HDA_SYNC/I2S0_SFRM	DU37 HDA_SYNC
SOC_DG_BB_FORCE_PWR DG41	GPP_A23/I2S1_SCLK	GPP_R2/HDA_SDO/I2S0_TXD	DT37 HDA_SDOUT
DT38	GPP_R7/I2S1_SFRM	GPP_R3/HDA_SDI0/I2S0_RXD	DV37 HDA_SDIN0
DV38	GPP_R6/I2S1_TXD		
HDA_SDIN1 DW38	GPP_R5/HDA_SDI1/I2S1_RXD	GPP_R4/HDA_RST#	DV41 HDA_RST#
		GPP_A7/I2S2_SCLK/DMIC_CLK_A0	DL53
[38] PCH_DMIC_CLK0	PCH_DMIC_CLK0 DN31	GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0	DG51 CNV_RF_RESET# → CNV_RF_RESET# [52]
[38] PCH_DMIC_DATA0	PCH_DMIC_DATA0 DM31	GPP_A10/I2S2_RXD/DMIC_DATA1	DG50 TPM_SERIRQ_R → TPM_SERIRQ_R [66]
	GPP_S6/SNDW3_CLK/DMIC_CLK_A0		
	GPP_S7/SNDW3_DATA/DMIC_DATA0	GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1	DL49 CLKREQ_CNV# → CLKREQ_CNV# [52]
DK33	GPP_S4/SNDW2_CLK/DMIC_CLK_A1	GPP_A11/PMC_I2C_SDA/I2S3_SCLK	DL52
DK31	GPP_S5/SNDW2_DATA/DMIC_DATA1		
		GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0	DH49 BT_ON → BT_ON [52]
DW35	GPP_S2/SNDW1_CLK/DMIC_CLK_B0		
DV35	GPP_S3/SNDW1_DATA/DMIC_CLK_B1	SNDW_RCOMP	DF33 SNDW_RCOMP — RC90 1 — 200_0201_1% — 2
DT32	GPP_S0/SNDW0_CLK		
DR35	GPP_S1/SNDW0_DATA		

TGL-U_BGA1449
@

CLKREQ_CNV# — 1 — RC104 — @ — 2 — 100K_0201_5%

SOC_DG_BB_FORCE_PWR — 0_0201_5% — 2 — short@ — 1 — RC6194 — DG_BB_FORCE_PWR_R → DG_BB_FORCE_PWR_R [42,43]

HDA_BIT_CLK

@RF@ CC101 22P_0402_50V8 — 1 — 2 — G

HDA for AUDIO

2019/12/09
1.Add RC206 for follow SPEC & 19 OPP ICL

[56] HDA_RST#_R — RC206 1 — 2 33_0201_5% HDA_RST#
[56] HDA_SDOUT_R — RC95 1 — 2 33_0201_5% HDA_SDOUT
[56] HDA_BIT_CLK_R — RC96 1 — EMI@ — 2 33_0201_5% HDA_BIT_CLK
[56] HDA_SYNC_R — RC98 1 — 2 33_0201_5% HDA_SYNC
[56] HDA_SDIN0 — HDA_SDIN0

75K_0201_5% 1 — 2 RC99 CNV_RF_RESET#
100K_0201_5% 1 — 2 RC101 HDA_BIT_CLK
33K_0201_5% 1 — 2 RC102 HDA_RST#
33K_0201_5% 1 — @ — 2 RC103 HDA_SDIN1

2019/12/11
Change BOM Structure from GLITCH@ to pop

Follow
607872_TGL_UY_PDG for Glitch

2019/12/09
Remove SOC DMIC for no support

572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

To Enable ME Override

HDA_SDOUT
FLASH DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

[58] ME_EN — RC5 1 — short@ — 2 0_0201_5% HDA_SDOUT

1 — @ — 2 — RC97 100K_0201_5%

Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(5/14)HDA,SNDW

Size: A3 | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 10 of 100

2019/12/09
1.Change Net name from CLK_PCIE_P/N0 to CLK_PEG_P/N0 follow 19 OPP
ICL 2.Remove PCIE Port4 & Port5 & Port6 for no use

Follow 607872_TGL_UY_PDG_Rev0p5 for Glitch

+3V_PRIM
RC121 1 2 100K_0201_5% PM_SLP_S0#
RC123 1 2 100K_0201_5% SLP_SUS#
RC124 1 @ 2 100K_0201_5% PM_SLP_S5# RC125 1
2 100K_0201_5% PM_SLP_S4#
RC127 1 2 100K_0201_5% PM_SLP_S3#

2019/12/09
1.Change Bom Structure from GLITCH@ to pop 2.PM_SLP_S5# change to unpop

+3V_PRIM
RC136 1 2 10K_0201_5% SYS_RESET#
CC147 2 ESD@ 1 0.1U_0201_10V6K

2019/12/09
1.Remove SYS_PWROK & PCH_PWROK & SOC_PLTRST# ORB ESD Cap

ESD Suggestion

+RTCVCC
RC1381 2 20K_0201_5% SOC_SRTCRST#
CC21 1 2 1U_0201_6.3V6M
CLRP1 1 2 SHORT PADS CLR_ME
RC1391 2 20K_0201_5% SOC_RTCRST#
CC22 1 2 1U_0201_6.3V6M
CLRP2 1 2 SHORT PADS CLR_CMOS
RC1431 @ 2 1M_0201_5% SM_INTRUDER#
CC23 1 @ 2 0.1U_0201_10V6K
RC3341 2 1M_0201_5%
RC144 1 2 100K_0201_5% EC_RSMRST#
CLRP3 2 1 SHORT PADS SYS_RESET#

SM_INTRUDER#
NO INTERNAL PU/PD
HIGH: SPI VOLTAGE IS 1.8V
LOW: SPI VOLTAGE IS 3.3V

+1.05V_VCCST
From EC(open-drain)
RC145 1K_0201_5%
[58] EC_VCCST_PG_R RC1471 2 60.4_0201_1% EC_VCCST_PG

UC1K REV 1.6
BW1 CLKOUT_PCIE_P6 GPP_F19/SRCCLKREQ6#
BW2 CLKOUT_PCIE_N6 GPP_H11/SRCCLKREQ5#
GPP_H10/SRCCLKREQ4#
CB2 CLKOUT_PCIE_P5 GPP_D8/SRCCLKREQ3#
CB1 CLKOUT_PCIE_N5 GPP_D7/SRCCLKREQ2#
GPP_D6/SRCCLKREQ1#
GPP_D5/SRCCLKREQ0#
BW4 CLKOUT_PCIE_P4
BW5 CLKOUT_PCIE_N4
CLKOUT_PCIE_P3
CLKOUT_PCIE_N3
CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
BY4 CLKOUT_PCIE_P1
BY3 CLKOUT_PCIE_N1
CN7 CLKOUT_PCIE_P0
CN8 CLKOUT_PCIE_N0
XCLK_BIASREF
XTAL_OUT
XTAL_IN
GPD8/SUSCLK
RTCX2
RTCX1
RTCRST#
SRTCRST#
DU14
DF23
DG25
DT24 CLKREQ_PCIE#3
DT30 CLKREQ_PCIE#2 DV30
DW30
DM1 SOC_XTAL38.4_OUT DL1
SOC_XTAL38.4_IN
DW41 SUSCLK_R RC376 1 short@ 2 0_0402_5%
DT47 SOC_RTCX2
DR47 SOC_RTCX1
DN37 SOC_RTCRST#
DM37 SOC_SRTCRST#
TGL-U_BGA1449
@

SSD [68] CLK_PCIE_P3 [68] CLK_PCIE_N3 CLK_PCIE_P3 CLK_PCIE_N3 CL7 CL8
CR [70] CLK_PCIE_P2 [70] CLK_PCIE_N2 CLK_PCIE_P2 CLK_PCIE_N2 CB4 CB5

2 RC120 1 XCLK_BIASREF DJ5 60.4_0402_1%

CLKREQ_PCIE#3 [68] SSD
CLKREQ_PCIE#2 [70] CR

SUSCLK [52]
SOC_RTCRST# [58]
SOC_SRTCRST# [58]

+3VS
CLKREQ_PCIE#2 10K_0201_5% 1 2 RC106
CLKREQ_PCIE#3 10K_0201_5% 1 2 RC107

SPIVCCIOSEL
3.3V / 1.8V SELECT FOR SPI
HIGH: 1.8V
LOW: 3.3V
Follow 609003_TGL_U_DDR4_SODIMM_RVP_SCH

+3VALW
PM_BATLOW# 8.2K_0201_5% 2 1 RC112
WAKE# 8.2K_0201_5% 2 1 RC114
LAN_WAKE# 10K_0201_5% 2 1 RC115
SPIVCCIOSEL 4.7K_0201_5% 2 @ 1 RC116
4.7K_0201_5% 2 1 RC117
SOC_PD_INT# 75K_0201_5% 2 @ 1 RC118
SUSCLK 1K_0201_5% 1 @ 2 RC119

Follow 609003_TGL_U_DDR4_SODIMM_RVP_SCH

+3VS
CPU_C10_GATE#1 @ 2 RC122 100K_0201_5%

UC1L REV 1.6
SLP_SUS#
PM_SLP_S5#
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_S0#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13/PLTRST#
DSW_PWROK
SYS_PWROK
PCH_PWROK
INTRUDER#
SPIVCCIOSEL
PROCPWRGD
GPD3/PWRBTN#
GPD10/SLP_S5#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD6/SLP_A#
GPD9/SPL_WLAN#
GPP_B12/SLP_S0#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
GPD7
VCCSTPWRGOOD_TCSS
VCCST_PWRGD
VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE2#
BM9 H_PROCPWRGD
DK41 PBTN_OUT#_R
DN41 PM_BATLOW#
DK43 AC_PRESENT_R
CW40 SOC_PD_INT#
DN27 CPU_C10_GATE#
DG31 SX_EXIT_HOLDOFF#
DK39 WAKE#
DM41 LAN_WAKE#
DT41 GPD11
DN43 TBT_RETIMER_RESET#
CE5 VCCSTPWRGOOD_TCSS RC134 1 short@ 2 0_0201_5%
BP8 EC_VCCST_PG
BP9 VCCST_OVERRIDE RC135 1 short@ 2 0_0201_5%
DR12 SOC_GPP_F20
DW12 SOC_GPP_F21
TGL-U_BGA1449
@

[58] SLP_SUS#
[58,86] PM_SLP_S4#
[16,58] PM_SLP_S3#
[58] PM_SLP_S0#
[58] EC_RSMRST#
[58] SYS_PWROK
[58] PCH_PWROK

TP@T35
SOC_PD_INT# [42,43]
CPU_C10_GATE# [16]
SX_EXIT_HOLDOFF# [58]
TP@ T36
TBT_RETIMER_RESET# [42]
VCCST_OVERRIDE_R
VCCST_OVERRIDE_R [16]
TP@ T37

12/24 Add TBT_RETIMER_RESET#_R for TBT

CPU_C10_GATE#1 2 RC506 100K_0201_5%
SOC_GPP_F21 1 @ 2 RC126 100K_0201_5%
EC_VCCST_PG 1 2 CC151 @ESD@ 0.1U_0201_10V6K
ESD Suggestion

[58] AC_PRESENT RC141 1 short@ 2 0_0201_5% AC_PRESENT_R
[58] PBTN_OUT# RC142 1 short@ 2 0_0201_5% PBTN_OUT#_R
[58] PCH_DPWROK RC6195 1 short@ 2 0_0201_5% PCH_DPWROK_R

EC_RSMRST# 2 DC2 1 PCH_DPWROK_R
PM_SLP_S4# 3 LRB715FT1G_SOT323-3
PM_SLP_S3# 2 DC4 1 PCH_DPWROK_R
SLP_SUS# 3 LRB715FT1G_SOT323-3

tCPU22/ tPCH28b
EC_VCCST_PG_R 2 DC3 1 PM_SLP_S3#
PCH_PWROK 3 LRB715FT1G_SOT323-3
@
tPLT17
[58,88] VR_ON VR_ON 2 DC5 1 PM_SLP_S3#
RB751S-40_SOD523-2
@

12/16 DC3 DC5 change to @, follow 2019 OPP ICL U

SOC_RTCX2 RC323 1 short@ 2 SOC_RTCX2_R 0_0201_5%
RC62 10M_0201_1%
SOC_RTCX1 RC324 1 short@ 2 SOC_RTCX1_R 0_0201_5%
YC1 1 2 32.768KHZ 9PF 20PPM 9H03270045 SJ100011U00
CC24 1 2 10P_0201_50V8J
CC25 1 2 10P_0201_50V8J

2019/12/09 Add
DC17 EC_RSMRST# 1 2 PCH_PWROK
RB751V-40_SOD323-2 SCS00000Z00
DC18 2 1 RB751V-40_SOD323-2 SCS00000Z00
SPOK [58,85]
@ESD@ CC354 2 1 0.1U_0402_16V7K
Need Check

SOC_XTAL38.4_IN RC64 1 EMI@ 2 SOC_XTAL38.4_IN_R 33_0201_5%
RC63 200K_0402_1%
SOC_XTAL38.4_OUT RC65 1 EMI@ 2 SOC_XTAL38.4_OUT_R 33_0201_5%
YC2 1 2 3 4 38.4MHZ_10PF_8Y38420005 SJ10000VM00
CC19 2 1 12P_0201_50V8J
CC20 2 1 12P_0201_50V8J

PCH PLTRST Buffer
RC150 1 short@ 2 0_0201_5%
+3VS
CC28 @ 1 2 UC4 0.1U_0201_10V6K
SOC_PLTRST# 1 2
74AHC1G08GW_SOT353-5 @
PLT_RST# 4
PLT_RST# [42,52,58,66,68,70,80]
RC154 100K_0201_5% 1 2

12/16 RC154 GLITCH@-->SMT

Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.
Title: TGL-UP3(6/14)CLK,GPIO
Size: Document Number: LA-K261P
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+3V_PRIM

10K_0201_5% 1 — 2 RC6180 SPK_DET#

2019/12/09
1.Change Net name SOC_DGPU_PWR_EN to DGPU_PWR_EN
2.Change Net name SOC_DGPU_HOLD_RST# to DGPU_HOLD_RST# 3.Remove SOC_NGFF_SSD_WAKE# Single
4.Change DU19 Single from SOC_GC6_FB_EN to GPU_ALL_PGOOD
5.Remove SOC_WL_WAKE# single (DJ19) with WLAN_WAKE is EC control
6.Remove SOC_VRAM_TYPE Single (DF21)

+3VS

(For R-BOM)
For EC Debug UART / MIPI60

RC163 1 — 2 49.9K_0201_1% UART_2_CRXD_DTXD

RC164 1 — 2 49.9K_0201_1% UART_2_CTXD_DRXD

UC1F
REV 1.6

SOC_GPP_B18
[56,59] HDA_SPKR
[52] WL_OFF#
RAM_ID1
RAM_ID3
RAM_ID2
RAM_ID0

DC53	GPP_B16/GSPI0_CLK	
DA51	GPP_B18/GSPI0_MOSI	
DC49	GPP_B17/GSPI0_MISO	
DC50	GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#/GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5	
DC52	GPP_B15/GSPI0_CS0#	
CY49	GPP_B20/GSPI1_CLK	
CY53	GPP_B22/GSPI1_MOSI	
CY52	GPP_B21/GSPI1_MISO	
DA50	GPP_B19/GSPI1_CS0#	
DV21	GPP_C9/UART0_TXD	
DT21	GPP_C8/UART0_RXD	
DR21	GPP_C11/UART0_CTS#	
DW21	GPP_C10/UART0_RTS#	
DV19	GPP_C13/UART1_TXD/ISH_UART1_TXD	
DT19	GPP_C12/UART1_RXD/ISH_UART1_RXD	
DR18	GPP_C15/UART1_CTS#/ISH_UART1_CTS#	
DU19	GPP_C14/UART1_RTS#/ISH_UART1_RTS#	
DJ21	GPP_C21/UART2_TXD	
DG23	GPP_C20/UART2_RXD	
DJ19	GPP_C23/UART2_CTS#	
DF21	GPP_C22/UART2_RTS#	
DV18	GPP_C17/I2C0_SCL	
DW18	GPP_C16/I2C0_SDA	
DJ23	GPP_C19/I2C1_SCL	
DT18	GPP_C18/I2C1_SDA	
DJ29	GPP_H5/I2C2_SCL	
DJ31	GPP_H4/I2C2_SDA	
DF29	GPP_H7/I2C3_SCL	
DG29	GPP_H6/I2C3_SDA	
DF25	GPP_H9/I2C4_SCL/CNV_MFUART2_TXD	
DF27	GPP_H8/I2C4_SDA/CNV_MFUART2_RXD	

TGL-U_BGA1449
@

DR27	GPP_D14/ISH_UART0_TXD	SOC_SLP_DS0# [42]
DW27	GPP_D13/ISH_UART0_RXD	
DV25	GPP_D16/ISH_UART0_CTS#	SOC_GPP_D16 — 1 TP@ T218
DT25	GPP_B15/GSPI0_CS0#	
DB45	GPP_B6/ISH_I2C0_SCL	ISH_I2C_0_SCL_R
DB44	GPP_B5/ISH_I2C0_SDA	ISH_I2C_0_SDA_R
CY39	GPP_B8/ISH_I2C1_SCL	
DB47	GPP_B7/ISH_I2C1_SDA	SPK_DET# [57]
DD47	GPP_B10/I2C5_SCL/ISH_I2C2_SCL	
DD44	GPP_B9/I2C5_SDA/ISH_I2C2_SDA	
DJ8	GPP_E16/ISH_GP7	
DR7	GPP_E15/ISH_GP6	SEN_MODE [58]
DR24	GPP_D18/ISH_GP5	DYNAMIC_SAR_EN [58]
DU25	GPP_D17/ISH_GP4	LID_SW2# D
DV31	GPP_D3/ISH_GP3/BK3/SBK3	
DU31	GPP_D2/ISH_GP2/BK2/SBK2	ACCEL_INT# — KB_DISABLE [58] / ACCEL_INT# [67]
DT27	GPP_D1/ISH_GP1/BK1/SBK1	INT2_A_G
DV27	GPP_D0/ISH_GP0/BK0/SBK0	INT1_A_G
DR51	GPP_RCOMP	GPP_RCOMP RC1661 200_0201_1% 2
DN33	GPP_T3	
DT35	GPP_T2	
DG17	GPP_U5	
DG19	GPP_U4	

SENSOR 12/24 Add

Check

Device Mode

cool-sense

12/24 Follow G2 15 360 ICL, no TS_DET# (GPP_D18)

12/24 Follow G2 15 360 ICL

12/25 TGL use GPP_A13 for BT

12/25 Remove off page

Touch Pad

UART_2_CTXD_DRXD
RC1177 1 — @ 2 0_0402_5% — UART_2_CRXD_DTXD

[9] I2C0_SCL_TP — I2C0_SCL_TP
[9] I2C0_SDA_TP — I2C0_SDA_TP
[38] I2C1_SCL_TS — I2C1_SCL_TS
[38] I2C1_SDA_TS — I2C1_SDA_TS

+3VS

RC155 1 — 2 1K_0201_5% — I2C0_SCL_TP
RC159 1 — 2 1K_0201_5% — I2C0_SDA_TP

Touch Pad

+3VS

@RC380 10K_0201_5% — @RC382 10K_0201_5% — @RC384 10K_0201_5% — @RC386 10K_0201_5%

RAM_ID0
RAM_ID1
RAM_ID2
RAM_ID3

@RC381 10K_0201_5% — @RC383 10K_0201_5% — @RC385 10K_0201_5% — @RC387 10K_0201_5%

+3V_PRIM

RC268 1 — 2 10K_0201_5%

@ DC19
LID_SW2# D — 2 RB751S40 SOD523 SCS00003700 — 1 — LID_SW2# — LID_SW2# [58,64]

0319

Strap Pin

+3VS

@RC376 4.7K_0201_5% — @RC377 4.7K_0201_5%

SOC_GPP_B18
No Reboot
INTERNAL PD 20K
HIGH: No Reboot
LOW: Reboot Enable (Default)

SOC_GPP_B18
HDA_SPKR

@RC378 20K_0201_5% — @RC379 20K_0201_5%

HDA_SPKR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)

	RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0	PartNumber - Description	SDP/DDP	X76 Number
NO RAM	0	0	0	0	NO on board RAM		
Hynix_16G	0	0	0	1	SA0000CZ100 , S IC D4 16G/3200 H5ANAG6NCMR-XNC FBGA96P SA0000CZ110 , S IC D4 16G/3200 H5ANAG6NCMR-XNCA32!	DDP	X7685032LC6
Micron_16G	0	0	1	0	SA0000CSR00 , S IC D4 16G/3200 MT40A1G16RC-062E:B FBGA SA0000CSR20 , S IC D4 16G/3200 MT40A1G16RC-062E:B A32!	SDP	X7685032LCB
Samsung_16G	0	0	1	1	SA0000CZ200 , S IC D4 16G/3200 K4AAG165WA-BCWE FBGA96P SA0000CZ210 , S IC D4 16G/3200 K4AAG165WA-BCWEA32!	SDP	X7685032LCC
Hynix_8G	0	1	0	0	SA0000CZ300 , S IC D4 8G/3200 H5AN8G6NCJR-XNC FBGA 96P SA0000CZ310 , S IC D4 8G/3200 H5AN8G6NCJR-XNC A32!	SDP	
Micron_8G	0	1	0	1	SA0000CMS00 , S IC D4 512M16 MT40A512M16TB-062E:J FBGA SA0000CM530 , S IC D4 512M16 MT40A512M16TB-062E:J A32!	SDP	X7685032LC9
Samsung_8G	0	1	1	0	SA0000CZ500 , S IC D4 8G/3200 K4A8G165WC-BCWE FBGA 96P SA0000CZ510 , S IC D4 8G/3200 K4A8G165WC-BCWE A32!	SDP	X7685032LCA
Hynix_8G	0	1	1	1	SA0000CZ330 , S IC D4 8G/3200 H5AN8G6NDJR-XNC FBGA 96P SA0000CZ340 , S IC D4 8G/3200 H5AN8G6NDJR-XNC A32 !	SDP	X7685032LC8
TBD	1	0	0	0		TBD	
	1	0	0	1			
	1	0	1	0			

+3VS — +3VALW_EC

RC363 10K_0201_5% — RC365 10K_0201_5%

QC14A
ISH_I2C_0_SCL_R — 1 — 6 — ISH_I2C_0_SCL [38,58,67]
L2N7002SDW1T1G 2N SC88-6
SB00001FF00

QC14B
ISH_I2C_0_SDA_R — 4 — 3 — ISH_I2C_0_SDA [38,58,67]
L2N7002SDW1T1G 2N SC88-6
SB00001FF00

+3VS

ISH_I2C_0_SDA_R RC1172 1 — 2 1K_0402_5%
ISH_I2C_0_SCL_R RC6184 1 — 2 1K_0402_5%
INT1_A_G RC982 1 — 2 10K_0201_5%
INT2_A_G RC1173 1 — 2 10K_0201_5%

+3V_PRIM

ACCEL_INT# — 1 RC6183 2 — 10K_0201_5%

0406

DC12
INT1_A_G — 2 RB751S40 SOD523 SCS00003700 — 1 — SEN_AG_INT#1 — SEN_AG_INT#1 [38] — 6 AXIS INT#1

@ DC13
2 RB751S40 SOD523 SCS00003700 — 1 — SEN_AG_INT#3 — SEN_AG_INT#3 [38] — 3 AXIS INT#1

@ DC14
2 RB751S40 SOD523 SCS00003700 — 1 — GSEN_INT1# — GSEN_INT1# [67] — GSENSOR INT#1

@ DC15
INT2_A_G — 2 RB751S40 SOD523 SCS00003700 — 1 — SEN_AG_INT#2 — SEN_AG_INT#2 [38] — 6 AXIS INT#2

@ DC16
2 RB751S40 SOD523 SCS00003700 — 1 — GSEN_INT2# — GSEN_INT2# [67] — GSENSOR INT#2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/11/29	Deciphered Date 2020/12/31	Title: TGL-UP3(7/14)GPIO
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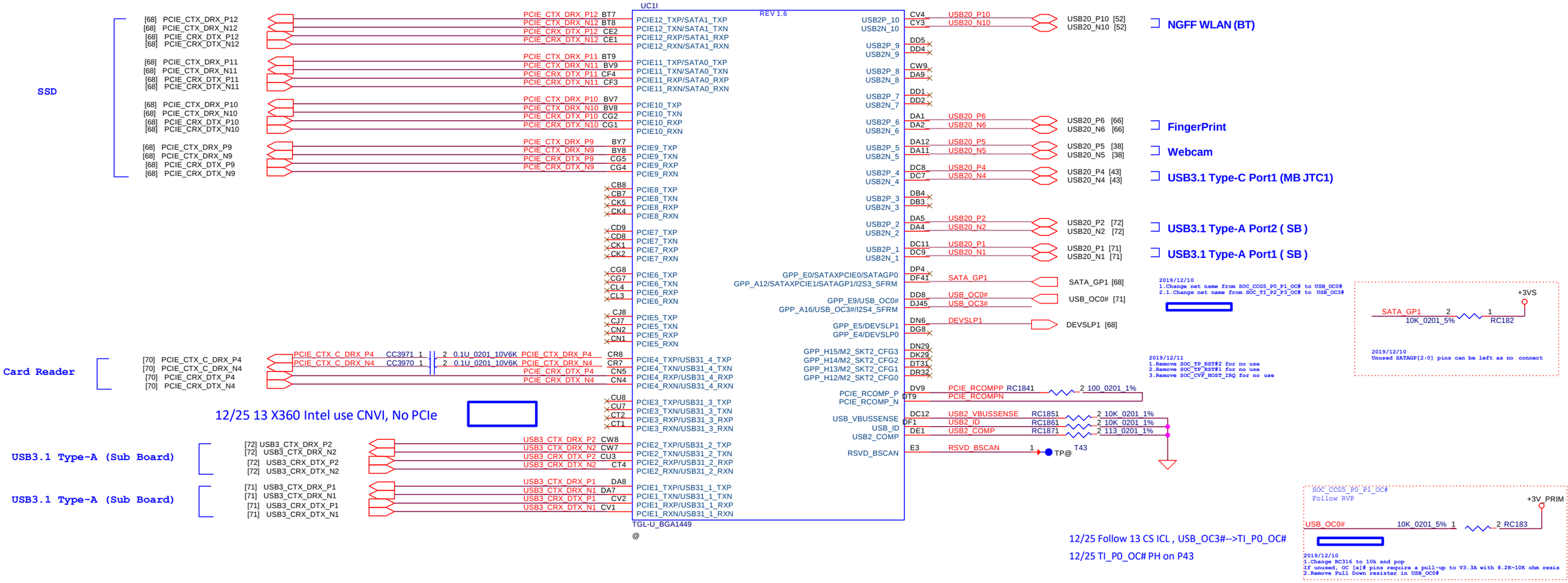
			Date: Friday, August 14, 2020 — Sheet 12 of 100



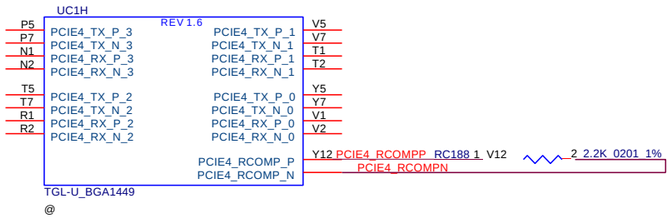


Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): • CLKOUT_PCIE_P[6:0] • CLKOUT_PCIE_N[6:0] PCH-LP (Y): • CLKOUT_PCIE_P[6:1] • CLKOUT_PCIE_N[6:1]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

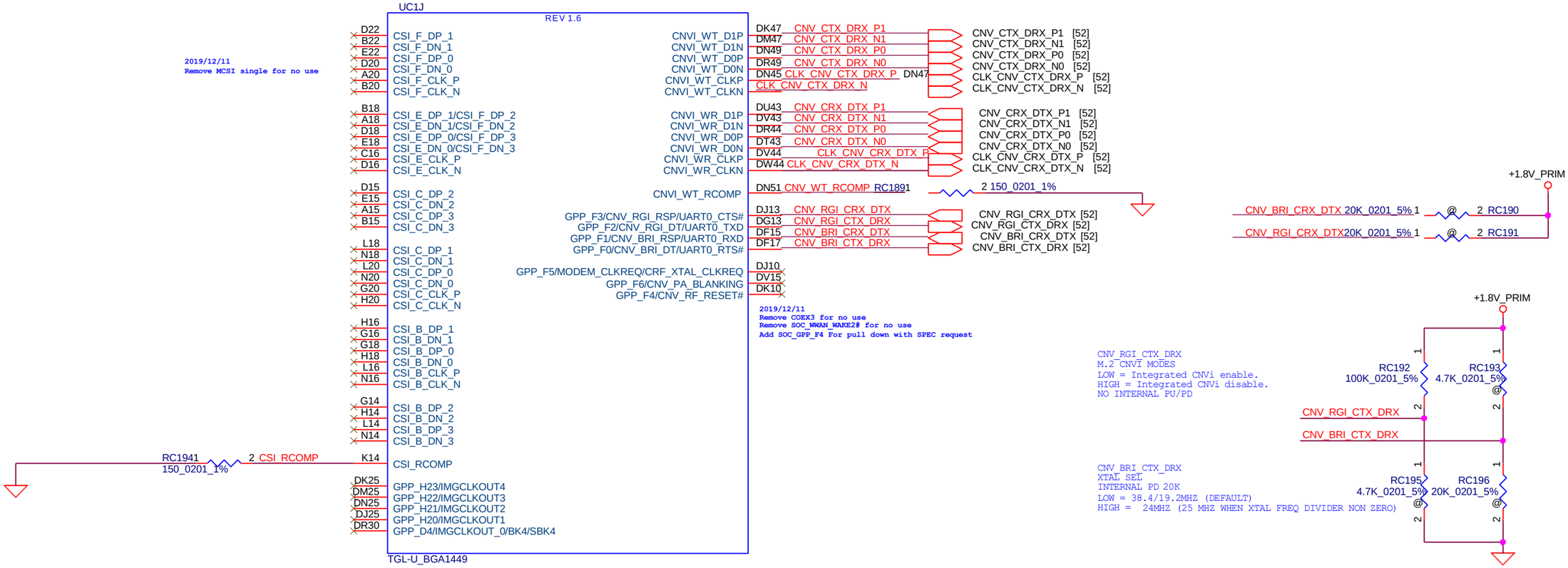
Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(8/14)PCIE,USB,SATA

Size: C | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 13 of 100



Compal Electronics, Inc.

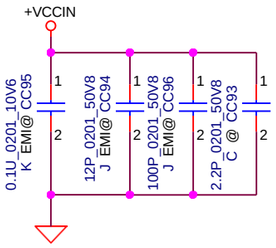
Title: TGL-UP3(9/14)CSI,CNV

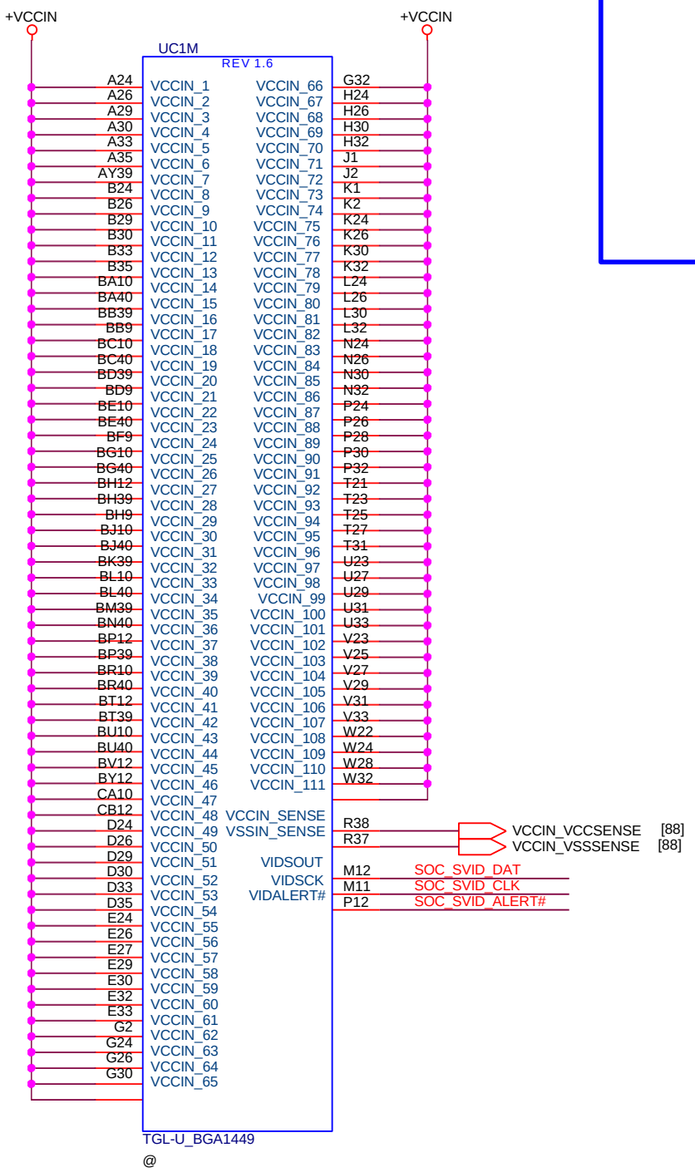
Size: C | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 14 of 100

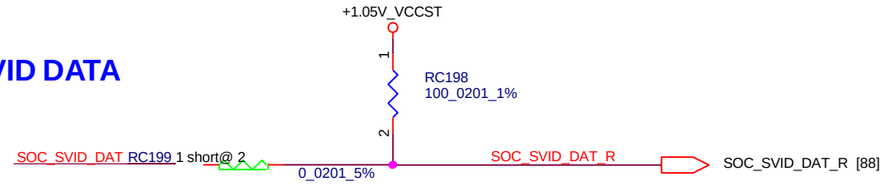
Package size?

EMC CAPS-PLACE
< 5mm from SOC VCCIN

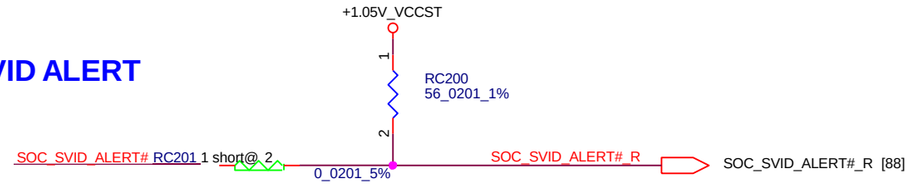




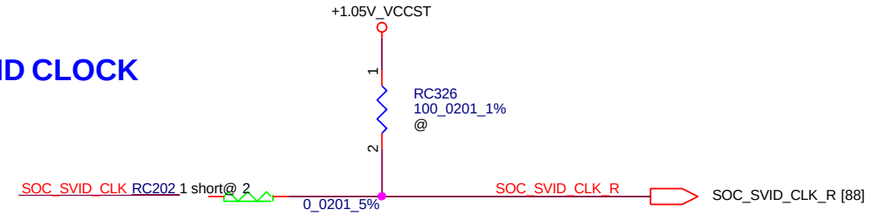
SVID DATA



SVID ALERT



SVID CLOCK



Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: **TGL-UP3(10/14)Power, SVID**

Size | Document Number: **LA-K261P** | Rev: 0.3

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RC505 1 short@ 2 0_0402_5%
RC504 1 short@ 2 0_0402_5%
RC501 1 short@ 2 0_0402_5%
RC502 1 short@ 2 0_0402_5%
RC503 1 short@ 2 0_0402_5%
+1.2V_VDDQ
+1.2V_VDDQ_CPU

EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (@RF@)
2.2pF* 3 (@RF@)

+1.2V_VDDQ_CPU
2.2P_0201_50V8C @RF@ CC34
12P_0201_50V8J @RF@ CC35
+1.2V_VDDQ_CPU
2.2P_0201_50V8C @RF@ CC36
12P_0201_50V8J @RF@ CC37
+1.2V_VDDQ_CPU
2.2P_0201_50V8C @RF@ CC38
12P_0201_50V8J @RF@ CC39

+1.2V_VDDQ_CPU
UC1O
REV 1.6
AA39 VDD2_1
AB40 VDD2_2
AC39 VDD2_3
AD40 VDD2_4
AD51 VDD2_5
AD52 VDD2_6
AE39 VDD2_7
AF40 VDD2_8
AG39 VDD2_9
AH40 VDD2_10
AJ39 VDD2_11
AK40 VDD2_12
AK51 VDD2_13
AK52 VDD2_14
AL39 VDD2_15
AM40 VDD2_16
AN39 VDD2_17
AP40 VDD2_18
AR39 VDD2_19
AT52 VDD2_20
AU40 VDD2_21
AW40 VDD2_22
AW51 VDD2_23
AW52 VDD2_24
BD51 VDD2_25
BD52 VDD2_26
BK51 VDD2_27
BK52 VDD2_28
BV51 VDD2_29
BV52 VDD2_30
CA40 VDD2_31
CC40 VDD2_32
CC49 VDD2_33
CC50 VDD2_34
CE40 VDD2_35
CG40 VDD2_36
CH39 VDD2_37
CJ40 VDD2_38
CL40 VDD2_39
CN40 VDD2_40
CP47 VDD2_41
CR40 VDD2_42
D50 VDD2_43
E51 VDD2_44
F49 VDD2_45
T51 VDD2_46
T52 VDD2_47
VCCSTG_OUT_LGC
TGL-U_BGA1449
@
VCCSTG_OUT_1 AF9
VCCSTG_1 AF12
VCCSTG_2 AD12
VCCSTG_OUT_2 AN10
VCCSTG_OUT_3 AM9
VCCSTG_OUT_4 AG10
VCCIO_OUT V15
VCCST_1 BT2
VCCST_2 BT1
VCCST_3 BT4
VCCSTG_3 BP2
VCCSTG_4 BP1
VCCSTG_5 BP4
+1.05VS_VCCSTG_OUT_FUSE
+1.05VS_VCCSTG_OUT_LGC
+1.05VS_VCCSTG_OUT_LGC_TERM
RC203 1 short@ 2 0_0402_5%
+1.05V_VCCIO_OUT
+1.05VS_VCCSTG_OUT_LGC
+1.05V_VCCST
+1.05VS_VCCSTG

+1.05V_VCCST
1U_0402_10V6K CC44
CC45 1U_0201_10V6M
+1.05VS_VCCSTG
1U_0402_10V6K CC46
CC47 1U_0201_10V6M
+1.05VS_VCCSTG_OUT_FUSE
1U_0201_10V6M CC33
1U_0201_10V6M CC155
1U_0201_10V6M CC156

VCCSTG_EN_LS_R
CC10 1U_0201_6.3V6M
+1.05VO_OUT_FET
CC51 1U_0402_10V6K
+5VALW
CC61 1U_0402_10V6K
[16] VCCST_EN_LS
R205 VCCSTG_EN_LS 1 short@ 2 VCCSTG_EN_LS_R 0_0201_5%
RC213 VCCST_EN_LS 1 2 VCCST_EN_LS_R 0_0201_5%
CC63 1U_0201_6.3V6M

tCPU26:CPU_C10_GATE# de-assertion to VCCSTG stable = 10us<Tr<65us(S0i3)

G2894KD1U use G5016KD1U_TDFN14-11_2X3 pin to pin

UC5
IN1 OUT1
EN1 CT1
BIAS GND
EN2 CT2
IN2 OUT2
GND PAD
G2894KD1U TDFN2X3_14
RC286 1 short@ 2 0_0603_5%
CC428 1_2 68P_0402_50V8J
CC430 1_2 68P_0402_50V8J @
RC287 1 short@ 2 0_0603_5%
+1.05VS_VCCSTG
CC53 0.1U_0201_10V6K
+1.05V_VCCST
CC4028 0.1U_0201_10V6K

+1.05VO_OUT_FET
CC60 1U_0402_10V6K

I (Max) : 0.5 A(+1.05V_VCCST)
RDS(Typ) : 3.5 mohm
V drop : 0.0016V

I (Max) : 0.3 A(+1.05VS_VCCSTG)
RDS(Typ) : 3.5 mohm
V drop : 0.0004V

Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

+1.2V_VDDQ_CPU
1U_0201_10V6M CC171
CC170
CC169
CC166
CC165
CC164
CC163
CC174
CC175
CC176
CC177
CC178
CC270
CC271
CC105
CC69
+1.2V_VDDQ_CPU
10U_0402_6.3V6M CC68
CC73
CC113
CC114
CC115
CC116
CC117
CC118
CC119
CC120
CC157
CC159
CC158
CC160
CC162
CC161
+1.2V_VDDQ
47U_0603_6.3V6M CC122
CC123

12/11 VCCSTG follow ICL U design. SMT VCCSTG power

VCCST_EN

+3V_PRIM
100K_0201_5% R151 VCCST_OVERRIDE_LS
100K_0201_5% R152 VCCST_OVERRIDE_N
100K_0201_5% R153 VCCST_OVERRIDE_R
VCCST_OVERRIDE_N
QC2B PJT7838 2N SOT-363-6 VGS(Max) : 1.0 V
VCCST_OVERRIDE_LS [16,58]
QC2A PJT7838 2N SOT-363-6 VGS(Max) : 1.0 V
[11] VCCST_OVERRIDE_R
VCCST_OVERRIDE_R

QC2 Foorprint use
DMN63D8LDW-7 (SB000013K00) need to confrim

[58] EC_VCCST_EN
R3844 1 @ 2 0_0201_5%
VCCST_EN_LS [16]

From EC to VCCST
VR Power SW Enable

VCCST/VCCSTG Enable

[38,58,78,86,93] SUSP#
[11,58] PM_SLP_S3#
SUSP# RC303 1 @ 2 0_0201_5%
PM_SLP_S3# RC304 1 2 0_0201_5%
DC7 LRB715FT1G_SOT323-3
1 VCCST_EN_LS
[16,58] VCCST_OVERRIDE_LS
VCCST_OVERRIDE_LS 1 short@ 2 VCCST_STG_COM_EN
RC340 0_0201_5%
DC8 LRB715FT1G_SOT323-3
1 VCCSTG_EN_LS
[11] CPU_C10_GATE#
CPU_C10_GATE# 1 2 0_0201_5% 3
RC331

	Singal Name	Input		
Volume	VCCST_OVERRIDE_LS	H	D	L
	PM_SLP_S3# (SUSP#)	D	H	L
	EC_VCCST_EN Output	H	H	L

Figure 228. VCCST Enable Logic

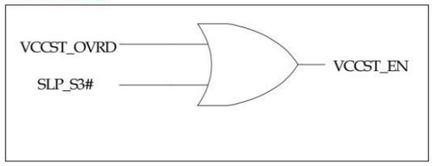
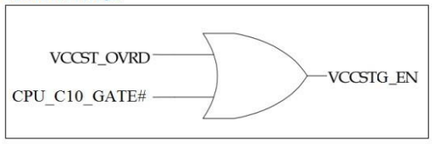
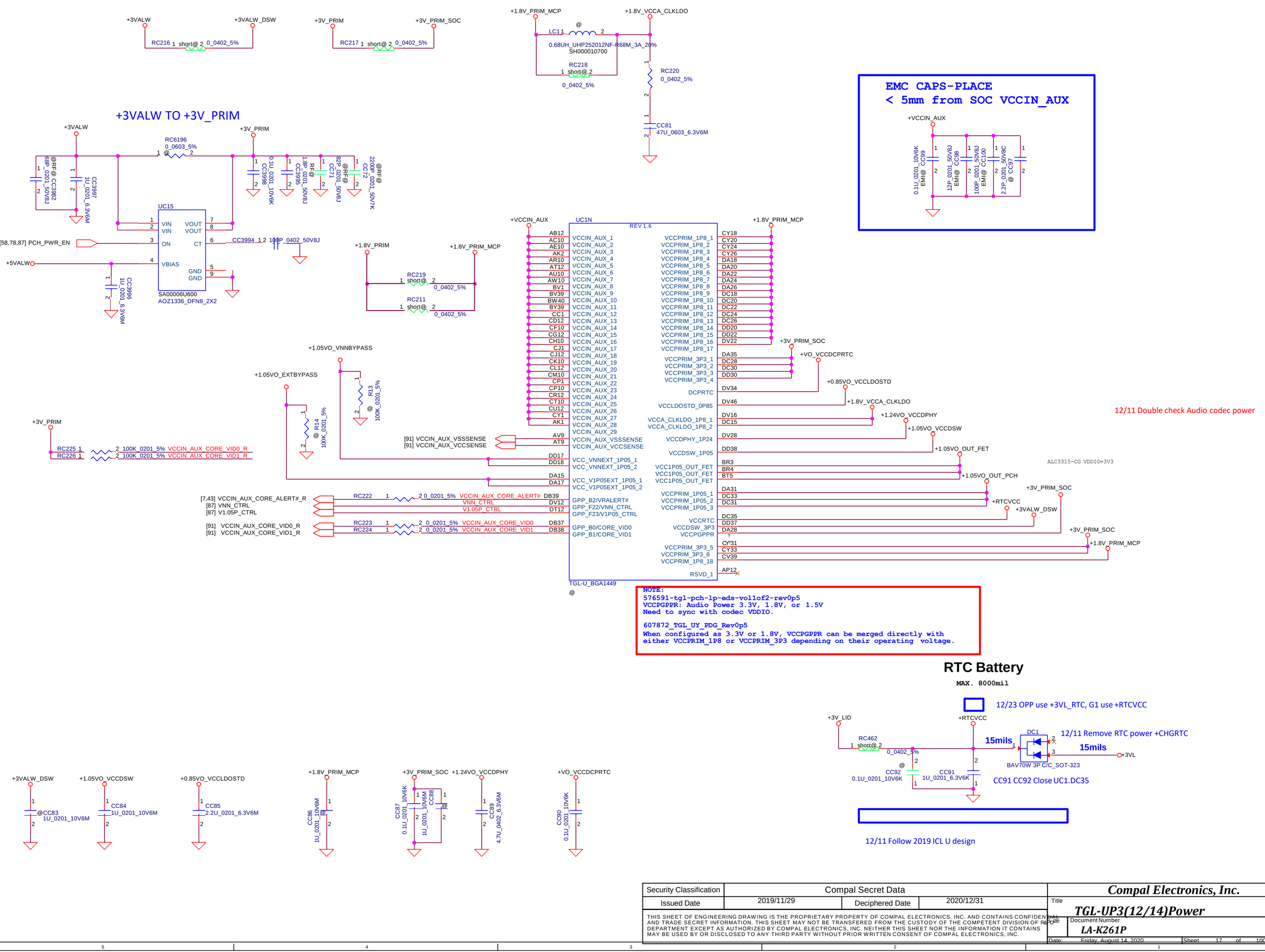


Figure 229. VCCSTG Enable Logic

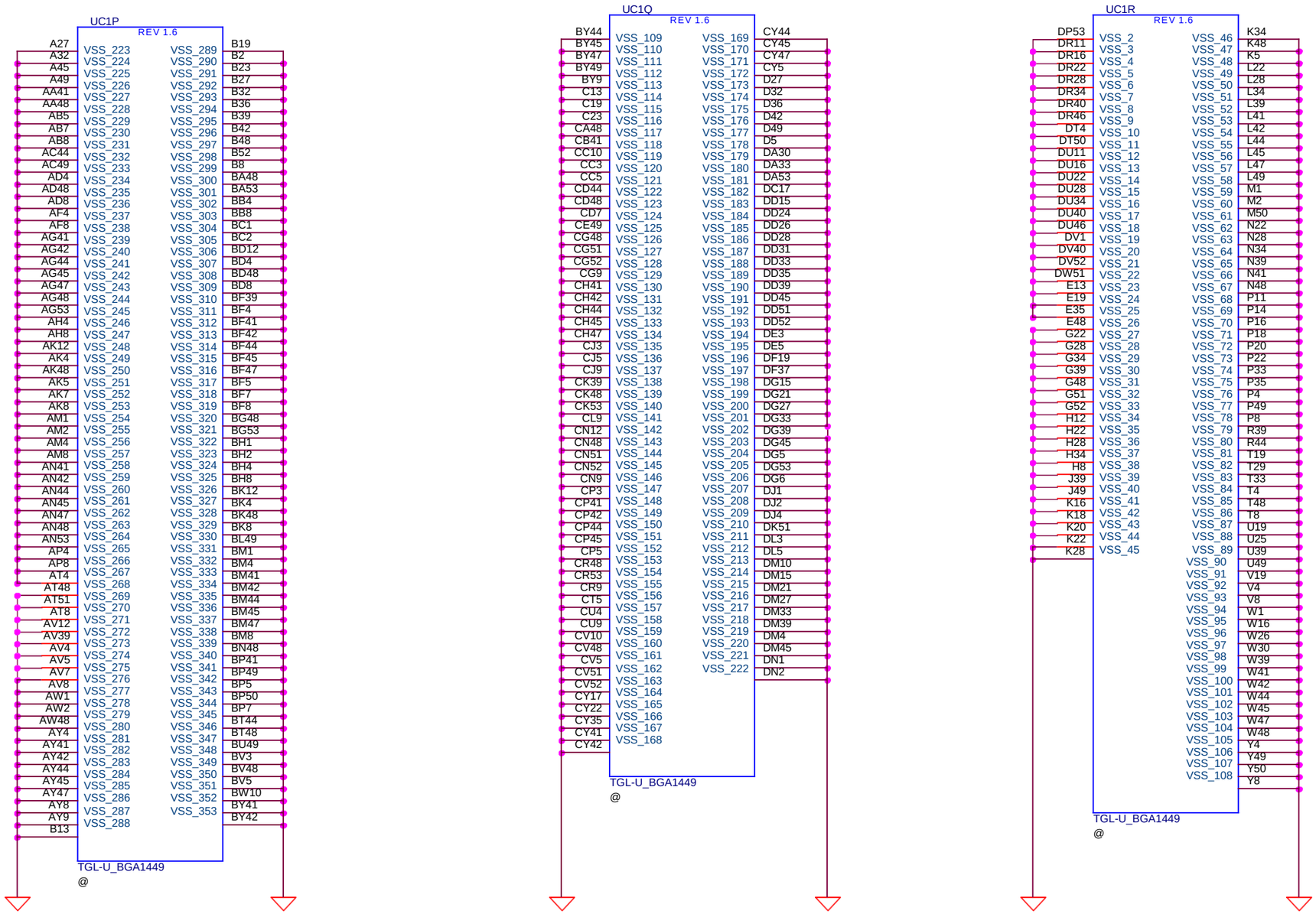


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/11/29	Deciphered Date	2020/12/31
Title	TGL-UP3(11/14)Power		
Size	Document Number LA-K261P		Rev 0.3
Date:	Friday, August 14, 2020	Sheet	16 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.			
Title: TGL-UP3(12/14)Power			
Size: C	Document Number: LA-K261P		Rev: 0.3
Date: Friday, August 14, 2020	Sheet 17 of 100		



Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

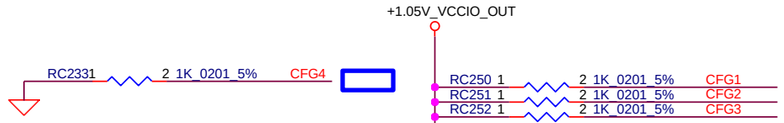
Compal Electronics, Inc.

Title: **TGL-UP3(13/14)GND**

Size | Document Number: **LA-K261P** | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 18 of 100

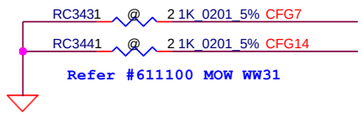
CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port



12/10 Refer 607872_TGL_UP3_UP4_PLATFORM_DOCUMENT_REV1.0 Page114

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

12/10 Fine tune @ and test point

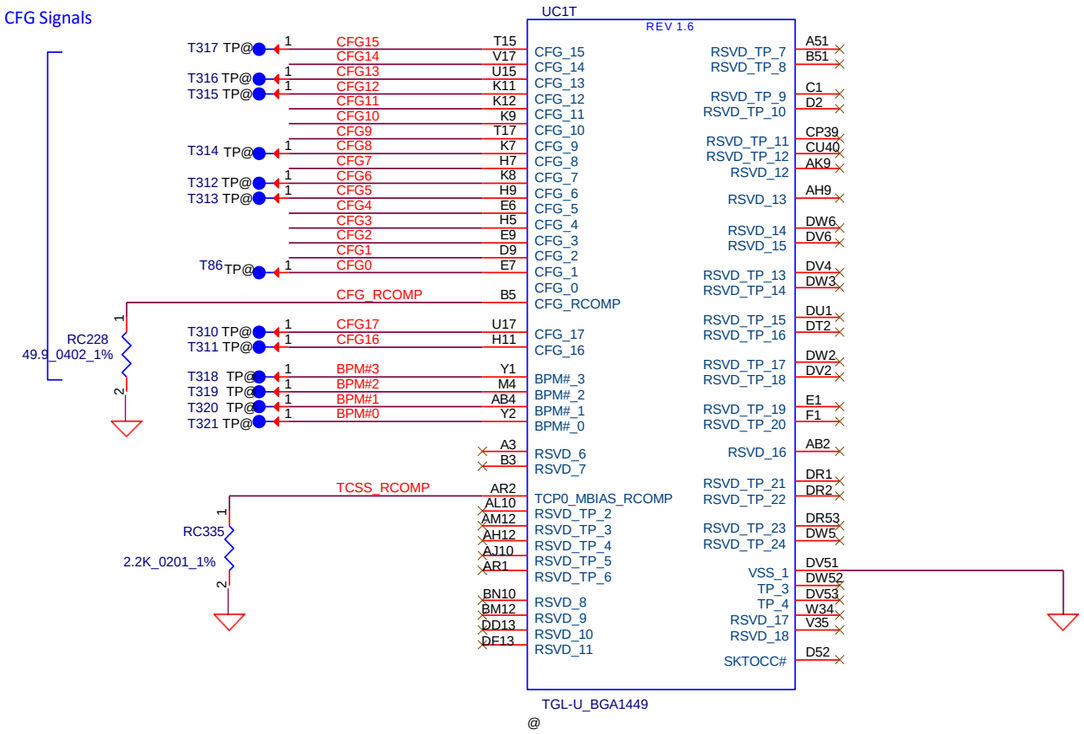


12/10 ORB no PH or PD on CFG7 and CFG14

12/11 change BPM#0~3 to test point

Check

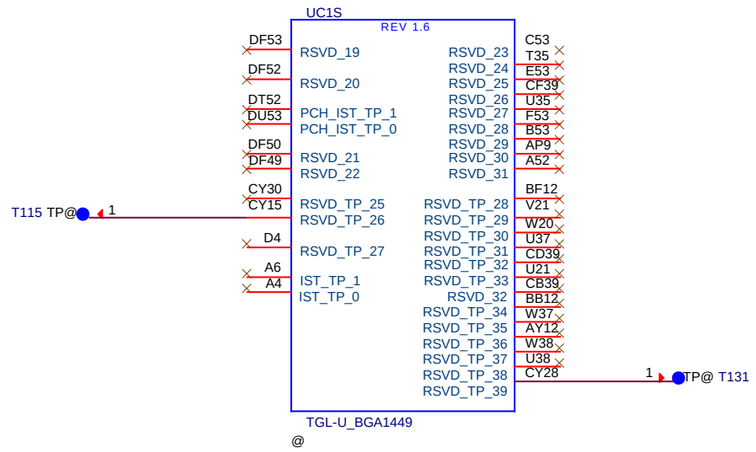
(For Strap & XDP)
CFG Signals



Processor BPM#[3:0] nets can be left floated when not use for debug. Processor CFG[19:0] and PCH chipset test interfaces might have dual purpose usage. From

Follow #614056
For ES1 FIVR Power ON

Check reserve or not



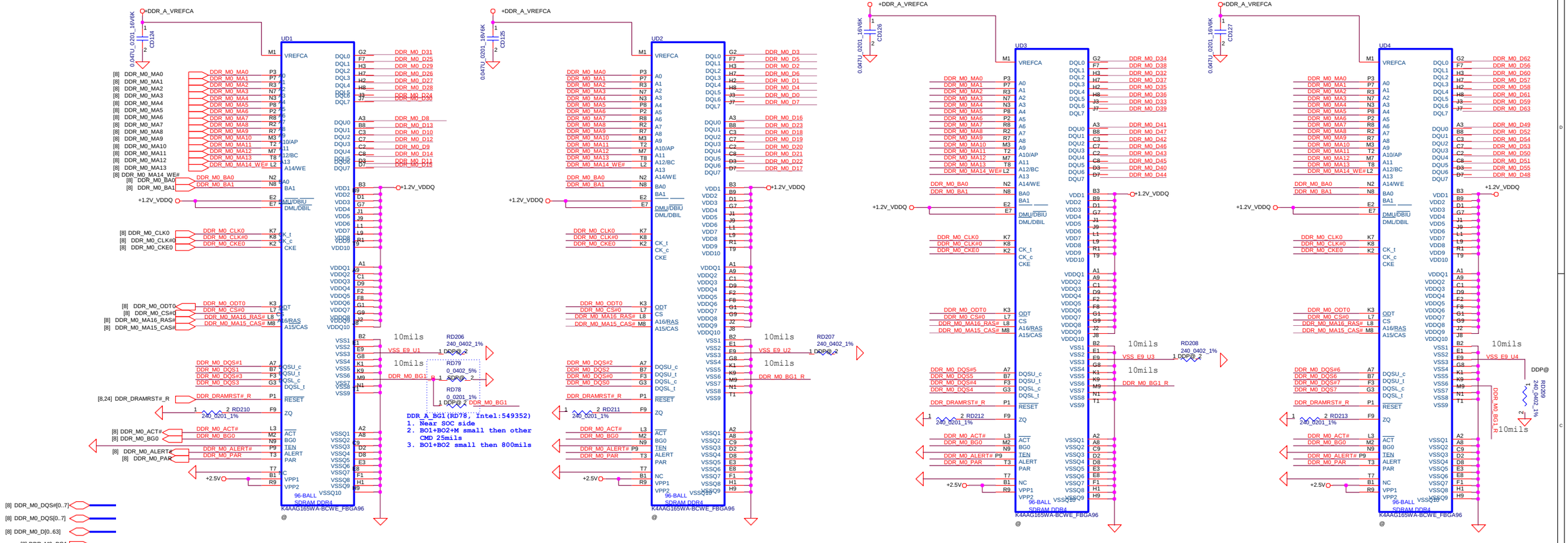
Security Classification	Compal Secret Data		
Issued Date	2019/11/29	Deciphered Date	2020/12/31

Compal Electronics, Inc.

Title: TGL-UP3(14/14)RSVD,CFG

Size: C | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 19 of 100



For layout need use 12.3x15.5 package size

need change 0201

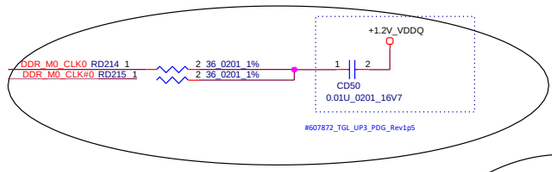
SDP@ RD206 0_0402_5% SD028000080
SDP@ RD208 0_0402_5% SD028000080
SDP@ RD207 0_0402_5% SD028000080
SDP@ RD209 0_0402_5% SD028000080

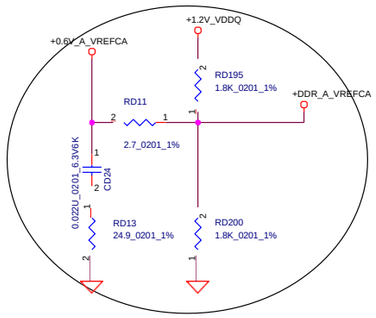
TABLE

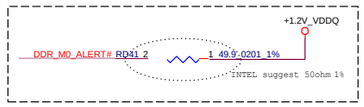
	SDP	DDP
RD79	ASM	NA
RD78	NA	ASM
RD220	NA	ASM
RD206 RD207 RD208 RD209	0_5% 0_5% 0_5% 0_5%	240_1% 240_1% 240_1% 240_1%

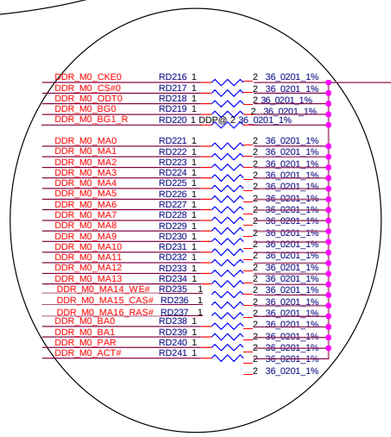
DDR4 mapping	SDP	DDP
E9	VSS	240_1%
M9	VSS	BG1
T7	VSS	VSS
RCOMP[0] (SOCside)	100_1%	100_1%

TERMINATION









VDDQ
1uF*16
10uF*5

4 as near each on board RAM device as possible

2019/11/14
change CD237 PN to SGA00009S00

Follow MA51

CD237
330U_D3_2.5VY_R6M
SGA00009S00

0327 RF ADD

0205 RF ADD

Add for cap downsize

VPP
1uF*8
10uF*3

2 as near each on board RAM device as possible

VTT
1uF*8
10uF*2

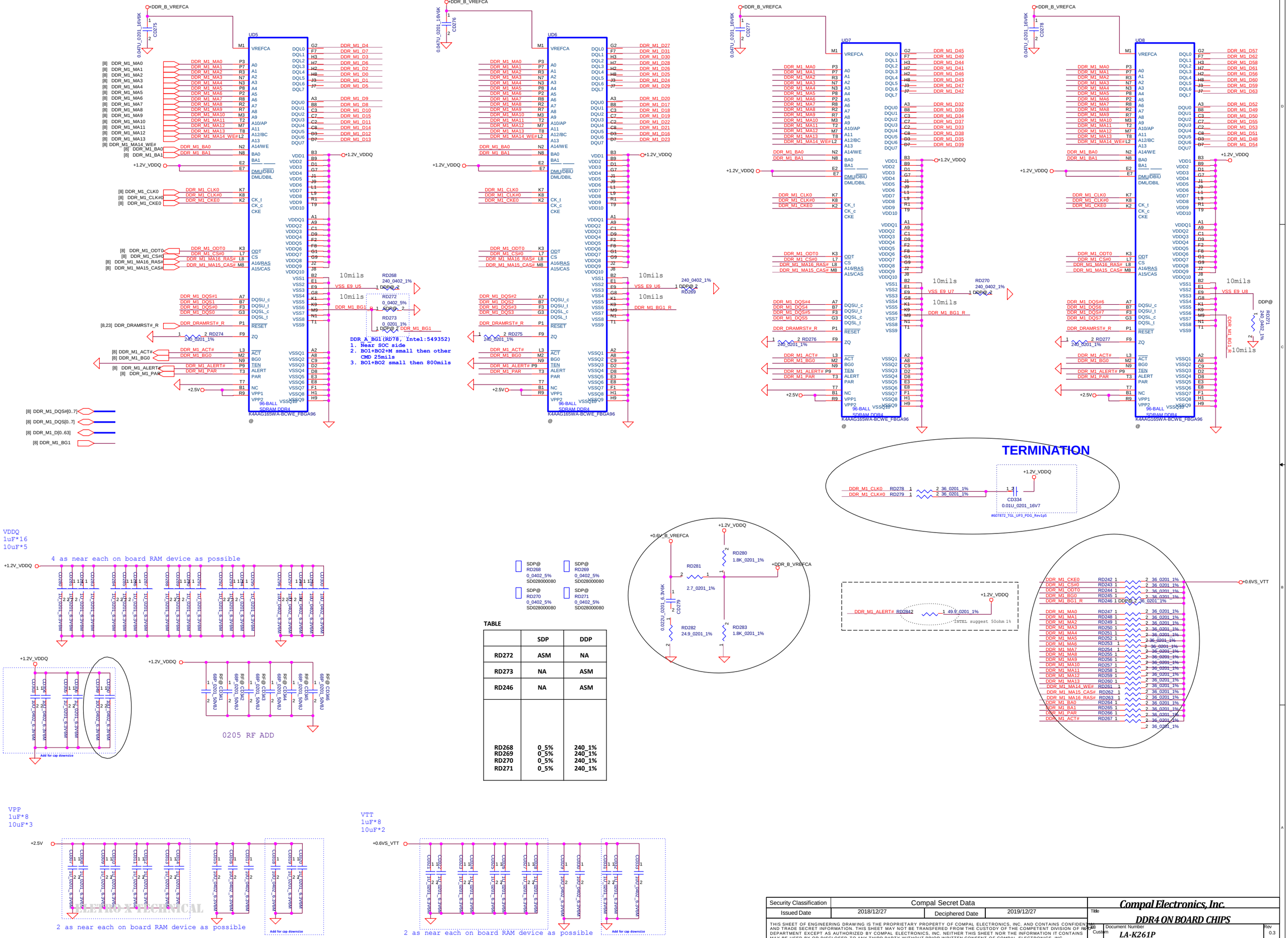
2 as near each on board RAM device as possible

Base on Intel SPEC

The ALERT signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title: DDR4 ON BOARD CHIPS			
Size: Custom	Document Number: LA-K261P		Rev: 0.3
Date: Friday, August 14, 2020	Sheet 23 of 100		



VDDQ
1uF*16
10uF*5

4 as near each on board RAM device as possible

0205 RF ADD

SDP@ RD268 0_0402_5% SD028000080
SDP@ RD269 0_0402_5% SD028000080
SDP@ RD270 0_0402_5% SD028000080
SDP@ RD271 0_0402_5% SD028000080

TABLE

	SDP	DDP
RD272	ASM	NA
RD273	NA	ASM
RD246	NA	ASM
RD268	0_5%	240_1%
RD269	0_5%	240_1%
RD270	0_5%	240_1%
RD271	0_5%	240_1%

TERMINATION

VPP
1uF*8
10uF*3

2 as near each on board RAM device as possible

VTT
1uF*8
10uF*2

2 as near each on board RAM device as possible

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

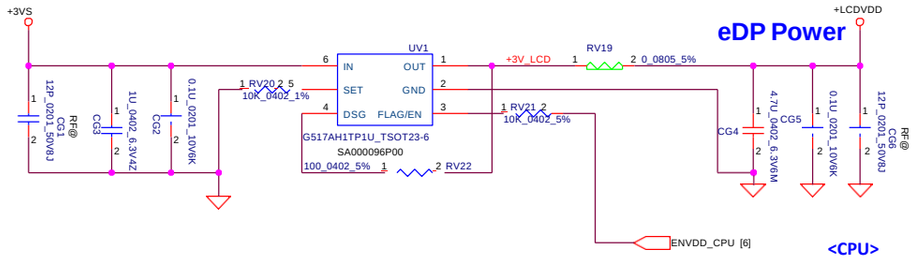
Compal Electronics, Inc.

Title: DDR4 ON BOARD CHIPS

Size: Custom | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 24 of 100

eDP



eDP Power

W=60mils
SM010014520 3000ma
220ohm@100mhz
DCR 0.04
INVPWR_B+
W=60mils
+12.6VB
FU2 1
2
SP040009I00
0.5A_15V_MF-MSMF050-2~D
@EMI@ C117
680P_0402_50V7K
0.1U_0402_16V7K
C118 RF@

<EC>
[58] EC_BKOFF#
RV2 1 short@ 2 0_0201_5% DISPOFF#
RV3
10K_0402_5%

<CPU>
[6] EDP_HPD
RV6 1 short@ 2 0_0201_5% EDP_HPD_PANEL
RV7
100K_0402_5%

<CPU>

[6] EDP_AUXP	CV7 1	2 .1U_0201_6.3V7K	EDP_AUXP_C
[6] EDP_AUXN	CV8 1	2 .1U_0201_6.3V7K	EDP_AUXN_C
[6] EDP_TXP0	CV9 1	2 .1U_0201_6.3V7K	EDP_TXP0_C
[6] EDP_TXN0	CV10 1	2 .1U_0201_6.3V7K	EDP_TXN0_C
[6] EDP_TXP1	CV11 1	2 .1U_0201_6.3V7K	EDP_TXP1_C
[6] EDP_TXN1	CV12 1	2 .1U_0201_6.3V7K	EDP_TXN1_C
[6] EDP_TXP2	CV13 1	2 .1U_0201_6.3V7K	EDP_TXP2_C
[6] EDP_TXN2	CV14 1	2 .1U_0201_6.3V7K	EDP_TXN2_C
[6] EDP_TXP3	CV15 1	2 .1U_0201_6.3V7K	EDP_TXP3_C
[6] EDP_TXN3	CV16 1	2 .1U_0201_6.3V7K	EDP_TXN3_C

[16,58,78,86,93] SUSP#

For +3VS_SHUT Discharge

+5VALW
+3VS_SHUTTER
RV14 100K_0402_1%
RV15 200_0402_1%
QV2B
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
QV2A
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
2
DS8 ESD@
I2C1_SCL_TS
I2C1_SDA_TS
TS_RST#
TS_INT#
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00

+1.8V_PRIM
+MIC_VCC
RA12 2 short@ 1 0_0402_5%

+3VALW
RC22 1 short@ 2 0_0402_5%
+3V_SEN

12/24 SHUT_FBC-->SHUTTER_FBC
[59] CAM_WP#
[58,73] SHUTTER_FBC
Camera
[73] SHUTTER_ENB
12/24 SHUT_ENB-->SHUTTER_ENB

JIO1CONN@
GND2
GND1
CAM_WP#
SHUTTER_FBC
USB20_P5_R
USB20_N5_R
SHUTTER_ENB
D_MIC_DATA
D_MIC_CLK
+3V_CAMERA
+3VS_SHUTTER
+MIC_VCC
+3VS_TS
+3V_SEN
I2C1_SCL_TS
I2C1_SDA_TS
TS_INT#
TS_RST#
TS_STOP#
ISH_I2C_0_SCL
ISH_I2C_0_SDA
SEN_AG_INT#1
SEN_AG_INT#2
SEN_AG_INT#3
ACES_51540-03001-001
ACES_51540-03001-001_30P

+3VS_TS
I2C1_SCL_TS RV53 1 2 1K_0201_1%
I2C1_SDA_TS RV54 1 2 1K_0201_1%

PV: add PU to touch power rail

12/24 Add PWM Mux

PWM MUX

<CPU> [6,58] BKL_PWM_CPU BKL_PWM_CPU R259 1 @ 2 0_0201_5% INVTPWM
<EC> [58] BKL_PWM_EC BKL_PWM_EC R5816 1 @ 2 0_0201_5%

For PWM reserve,close UV27

PWM MUX UV27		
PRI_PMW_SEL	Path	Function
H	A2 to DA	Privacy ON
L	A1 to DA	Privacy OFF

<EC> BKL_PWM_EC
<CPU> BKL_PWM_CPU
UV27
A2
A1
GND
VDD
SEL
DA
AZAW1210C_SC70-6
SA000098O00
PWM_MUX_EN_R
RV4978 1 short@ 2 0_0201_5% PWM_MUX_EN
PWM_MUX_EN [59]
+3VALW_EC
INVTPWM
<Panel>
RV10 100K_0201_5%
@ RV9 100K_0201_5%

@EMI@ CV25 1 2 0.1U_0201_10V6K TS_RST#
@EMI@ CV26 1 2 0.1U_0201_10V6K TS_INT#
@EMI@ CV27 1 2 0.1U_0201_10V6K SEN_AG_INT#1
@EMI@ CV28 1 2 0.1U_0201_10V6K SEN_AG_INT#2

eDP

JEDP1CONN@
INVPWR_B+
EDP_TXP3_C
EDP_TXN3_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP0_C
EDP_TXN0_C
EDP_AUXP_C
EDP_AUXN_C
EDP_HPD_PANEL
DISPOFF#
INVTPWM
[58] PRI_EN
PRI_EN
RV4979 1 2 100K_0201_5%
+LCDVDD
[58] PRI_DETECT#
PRI_DETECT#
GND2
GND1
ACES_51519-04001-001
ACES_51519-04001-001_40P_T
SP01002TL00

CV17 2 1 220P_0402_50V7K INVTPWM
CV18 2 1 220P_0402_50V7K DISPOFF#

Camera

From CPU

[13] USB20_P5 R6569 1 short@ 2 0_0201_5% MUX_USB20_P5
[13] USB20_N5 R6570 1 short@ 2 0_0201_5% MUX_USB20_N5

LU1 EMI@
MUX_USB20_N5
MUX_USB20_P5
USB20_N5_R
USB20_P5_R
DLM0NSN900HY2D_4P
SM070005U00

ESD Part:
Main: SC300003Z00, S DIO(BR) PUSB3F98 DFN2510A-10 ESD(NXP)
2rd: SC300005N00, S DIO(BR) L5V5UV3NA-4C SLP2510P8(LITE ON)
DS6 @ESD@
USB20_P5_R
USB20_N5_R
D_MIC_DATA
D_MIC_CLK
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00

+3VS
+3V_CAMERA_R
+3V_CAMERA
UV2
IN
OUT
SET
GND
DSG
FLAG/EN
G517AH1TP1U_TSOT23-6
SA000096P00
RV24 1 short@ 2 0_0402_5%
CAM_PWR_EN_R
2 RV11 1
21K_0402_1%
100_0402_5% 1 2 RV16
CV21 1U_0402_6.3V4Z
CV22 0.1U_0201_10V6K
CV23 4.7U_0402_6.3V6M
CV24 0.1U_0201_10V6K
CAM_PWR_EN_R RV5 1 2 10K_0402_5%
CAM_PWR_EN [59]

DMIC

[10] PCH_DMIC_DATA0 RA65 1 short@ 2 0_0201_5% D_MIC_DATA
[10] PCH_DMIC_CLK0 S SUPPRE_TAI-TECH HCB1005KF-221T15_0402 2 1 LA11 D_MIC_CLK
SM01000Q500 EMI@
10P_0201_50V8J 2 1 CA50 Close to SOC
@EMI@

Touch Screen

+3VS
+3VS_TS_R
+3VS_TS
UV3
IN
OUT
SET
GND
DSG
FLAG/EN
G517AH1TP1U_TSOT23-6
SA000096P00
RV23 1 short@ 2 0_0402_5%
RV17 10K_0402_5%
TS_PWR_EN [59]
RV18 1 2 100_0402_5%
RV81 42.2K_0402_1%
CV5 1U_0402_6.3V4Z
CV6 0.1U_0201_10V6K
CV19 4.7U_0402_6.3V6M
CV20 0.1U_0201_10V6K

[9] TS_INT#
RTS2 1 short@ 2 0_0201_5%
RTS1 10K_0402_5%
TS_INT#_R
CTS3 68P_0201_25V8 @RF@

TS_INT#
RV13 2 @ 1 10K_0402_5%
+3VS_TS

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.
Title: eDP CONN/Camera/TS
Size: A3
Document Number: LA-J494P
Rev: 0.3
Date: Friday, August 14, 2020
Sheet 38 of 100

MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)

+3VS_RETIMER_0 Tolerance (+ 5%/-7.5%):
Burnside Bridge power pins which connected to +3VS_RETIMER_0 should be 3.465v maximum and 3.07v minimum for normal operation.
+3VS_RETIMER_0 ripple: 40mVp-p

[11] TBT_RETIMER_RESET#
[11,52,58,66,68,70,80] PLT_RST#
RT2 2 @ 1 0_0201_5% TBT_RETIMER_RESET# R
RT1 2 short@ 1 0_0201_5%

+3V_PRIM
RT4 1 @ 2 10K_0201_1% DG_BB_FORCE_PWR_R
RT5 1 TypeC@ 2 10K_0201_1%
RT6 1 TypeC@ 2 100_0201_1% DG0_TEST_PWR_GOOD
RT7 1 TypeC@ 2 10K_0201_1% DG0_POC_GPIO5

+3VS_RETIMER_0
RT14 1 @ 2 10K_0201_1% DG0_FLSH_SHARE_EN
RT11 1 2 10K_0201_1%
RT15 1 @ 2 10K_0201_1% DG0_FLSH_MSTR_SLV
RT16 1 TypeC@ 2 10K_0201_1%
RT17 1 TypeC@ 2 10K_0201_1% DG0_POC_GPIO12
RT18 1 @ 2 10K_0201_1%

+3VALW
RT19 1 TypeC@ 2 10K_0201_1% DG0_FLASH_BUSY#
RT20 1 @ 2 10K_0201_1%

DG1_RST#:
For PD based systems, DG1_RST# should be output from PD.
For TCPC based systems, DG1_RST# should be output from SOC/EC.
DG1_BB_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG1_FLASH_BUSY#:
If Flash sharing is being used, PU should be used.
If Flash sharing isn't being used, PD should be used.
DG1_FLSH_SHARE_EN:
'0' - Flash isn't shared. 1 Flash per Re-timer '1' - Flash is shared between 2 Re-timers
DG1_FLSH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F. '1' - Set Re-timer to be Master on shared flash SPI I/F

+3VS
RT32 1 TypeC@ 2 10K_0201_1% DG0_POC_GPIO6

+3VALW
RT38 1 @ 2 10K_0201_1% TBT_RETIMER_RESET# R
RT39 1 @ 2 10K_0201_1%

08/16
Refe RVP Page 109,114,119,123 design to EC

UT2A @

MISC & DEBUG

DG0_SPI_DI C6 EE_DI
DG0_SPI_DO B4 EE_DO
DG0_SPI_CS# B6 EE_CS#
DG0_SPI_CLK C7 EE_CLK
FLASH
DG0_JTAG_TDI A3 TDI
DG0_JTAG_TMS C3 TMS
DG0_JTAG_TCK B5 TCK
DG0_JTAG_TDO C5 TDO
JTAG
T137 TP@
AN0_THERMDA M11 THERMDA
M12 TEST_EDM
B2 FUSE_VQPS_64
A11 MONDC
A12 NC_A12
L12 MONDC_SVR
DG0_TEST_PWR_GOOD B3 TEST_PWR_GOOD
B11 TEST_EN
A1 ATEST_P
A2 ATEST_N
DEBUG
Main
POC GPIO
I2C_SCL C9
I2C_SDA E7
I2C_INT A10
FORCE_PWR B10
FLASH_BUSY# A9
POC_GPIO_5 B9
POC_GPIO_6 A8
PERST# B8
SMBUS_SCL A7
SMBUS_SDA B7
POC_GPIO_10 A4
POC_GPIO_11 A5
POC_GPIO_12 A6
NC_L3 L3
RESET# L11
XTAL_25_IN L9
XTAL_25_OUT M9
RSENSE L5
RBIAS L4
TBT_I2C_SCL RT1137 2 @ 1 0_0201_5% SOC_SML1CLK
TBT_I2C_SDA RT1138 2 @ 1 0_0201_5% SOC_SML1DATA
TBT_I2C_INT# RT1139 2 @ 1 0_0201_5% SOC_PD_INT#
SOC_SML1CLK [9,43]
SOC_SML1DATA [9,43]
SOC_PD_INT# [11,43]
TBT_I2C_SCL RT8 2 short@ 1 0_0201_5%
TBT_I2C_SDA RT10 2 short@ 1 0_0201_5%
TBT_I2C_INT# RT84 2 short@ 1 0_0201_5%
I2C3_PD_R_CLK [43]
I2C3_PD_R_DAT [43]
I2C3_PD_R_INT# [43]
DG_BB_FORCE_PWR_R [10,43]
DG0_FLASH_BUSY#
DG0_POC_GPIO5
DG0_POC_GPIO6
TBT_RETIMER_RESET# R
TBT_SMBUS
DG0_FLSH_SHARE_EN
DG0_FLSH_MSTR_SLV
DG0_POC_GPIO12
DG0_RST# [43]
DG0_XTAL_25M_XI
DG0_XTAL_25M_XO
AN0_RBIAS 1 RT21 2 4.75K_0402_0.5% TypeC@
AN0_RSENSE
Reserve to SOC
BURNSIDE-BRIDGE_BGA105
SA0000CAH10
R1 PN:SA0000CAH10 S IC JHL8040R QURW A1 BGA 105P BURNSIDE
R3 PN:SA0000CAH20 S IC JHL8040R SIMN7 A1 THUNDERBOLT A32!
SA0000CAH50 S IC JHL8040R SIMN6 A1 FCCSP THUNDERBOLT

I2C to PD,SOC

[43,64] TBT_RETIMER_0_LS_EN
[12] SOC_SLP_DS0#
RT12 2 1 100K_0201_5% TBT_RETIMER_0_LS_EN_R
RT13 2 @ 1 0_0201_5%
High active
EN_VL:1.1V

TBT_SMBCLK RT11272 @ 1 0_0201_5% SOC_SML0CLK
TBT_SMBDAT RT11282 @ 1 0_0201_5% SOC_SML0DATA
SOC_SML0CLK [9]
SOC_SML0DATA [9]

TBT_SMBCLK RT94 2 1 100K_0201_5%
TBT_SMBDAT RT95 2 1 100K_0201_5%
Follow E team design PD 100K
SMBUS:
No support Vpro
Intel recommended PD 100K

+3VALW
+3VALW_UT1
RT107 1 short@ 2 0_0402_5%
+3V_PRIM
RT1061 @ 2 0_0402_5%
1U_0201_6.3V6M CT1

UT1
VIN1 VOUT1
VIN2 VOUT2
ON
CT
VBIAS
GND1
GND2
+3VS_RETIMER_OUT
LT3 BLM18KG331SN1D_2P SM01000KR00
@ CT228 470P_0201_25V7K
CT2 4.7U_0402_6.3V6M TypeC@
AOZ1336DI_DFN8_2X2
TypeC@
SA00006U600

TBT_RETIMER_0_LS_EN_R RT92 2 @ 1 100K_0201_5%
RT93 2 @ 1 10K_0201_5%
+3VALW_UT1

UT2D @

TBT PORTS

TypeC@
[6] TBT_0_TTX_DRX_P0 CT3 1 2 0.22U_0201_10V6M TBT_0_TTX_C_RD_DRX_P0 J1
[6] TBT_0_TTX_DRX_N0 CT5 1 2 0.22U_0201_10V6M TBT_0_TTX_C_RD_DRX_N0 J2
[6] TBT_0_TRX_DTX_P0 CT7 1 2 0.22U_0201_10V6M TBT_0_TRX_C_RD_DTX_P0 G1
[6] TBT_0_TRX_DTX_N0 CT9 1 2 0.22U_0201_10V6M TBT_0_TRX_C_RD_DTX_N0 G2
[6] TBT_0_TTX_DRX_P1 CT11 1 2 0.22U_0201_10V6M TBT_0_TTX_C_RD_DRX_P1 C1
[6] TBT_0_TTX_DRX_N1 CT13 1 2 0.22U_0201_10V6M TBT_0_TTX_C_RD_DRX_N1 C2
[6] TBT_0_TRX_DTX_P1 CT15 1 2 0.22U_0201_10V6M TBT_0_TRX_C_RD_DTX_P1 E1
[6] TBT_0_TRX_DTX_N1 CT17 1 2 0.22U_0201_10V6M TBT_0_TRX_C_RD_DTX_N1 E2
ASSRXp1
ASSRXn1
ASSTXp1
ASSTXn1
ASSRXp2
ASSRXn2
ASSTXp2
ASSTXn2
Port A - Host Side
Port B - TypeC Side
BSSRXp1
BSSRXn1
BSSTXp1
BSSTXn1
BSSRXp2
BSSRXn2
BSSTXp2
BSSTXn2
[6] TBT_0_LSX_TX_R M7
[6] TBT_0_LSX_RX_R L7 PA_LSTX_SBU1 PA_LSRX_SBU2
L8
[6] TBT_0_DP_AUXP_R M8 PA_AUX_P
[6] TBT_0_DP_AUXN_R PA_AUX_N
RT40 1M_0201_5% @
RT41 @ 1M_0201_5%
BURNSIDE-BRIDGE_BGA105

J12 TBT_0_TRX_RD_DTX_P0 RT23 1 TypeC@ 2 2.2_0201_1%
J11 TBT_0_TRX_RD_DTX_N0 RT24 1 TypeC@ 2 2.2_0201_1%
G12 TBT_0_TRX_RD_DTX_P0 RT25 1 TypeC@ 2 2.2_0201_1%
G11 TBT_0_TRX_RD_DRX_N0 RT26 1 TypeC@ 2 2.2_0201_1%
C12 TBT_0_TRX_RD_DTX_P1 RT27 1 TypeC@ 2 2.2_0201_1%
C11 TBT_0_TRX_RD_DTX_N1 RT28 1 TypeC@ 2 2.2_0201_1%
E12 TBT_0_TRX_RD_DRX_P1 RT29 1 TypeC@ 2 2.2_0201_1%
E11 TBT_0_TRX_RD_DRX_N1 RT30 1 TypeC@ 2 2.2_0201_1%
TBT_0_TRX_R_DTX_P0 CT4 1 2 0.33U_0201_25V6K
TBT_0_TRX_R_DTX_N0 CT6 1 2 0.33U_0201_25V6K
TBT_0_TRX_R_DRX_P0 CT8 1 2 0.22U_0201_25V6K
TBT_0_TTX_R_DRX_N0 CT10 1 2 0.22U_0201_25V6K
TBT_0_TTX_R_DRX_P0 CT12 1 2 0.33U_0201_25V6K
TBT_0_TTX_R_DTX_N1 CT14 1 2 0.33U_0201_25V6K
TBT_0_TRX_R_DTX_P1 CT16 1 2 0.22U_0201_25V6K
TBT_0_TRX_R_DRX_N1 CT18 1 2 0.22U_0201_25V6K
TBT_0_TRX_C_DTX_P0 [43]
TBT_0_TRX_C_DTX_N0 [43]
TBT_0_TTX_C_DRX_P0 [43]
TBT_0_TTX_C_DRX_N0 [43]
TBT_0_TRX_C_DTX_P1 [43]
TBT_0_TRX_C_DTX_N1 [43]
TBT_0_TTX_C_DRX_P1 [43]
TBT_0_TTX_C_DRX_N1 [43]
M10 TBT_0_SBU1
L10 TBT_0_SBU2
RT31 1 short@ 2 0_0201_5%
RT33 1 short@ 2 0_0201_5%
TBT_0_SBU1 R
TBT_0_SBU2 R
TBT_0_SBU1_R [43]
TBT_0_SBU2_R [43]
RT34 221K_0201_1% 2TypeC@
RT35 221K_0201_1% 2TypeC@
RT36 221K_0201_1% 2TypeC@
RT37 221K_0201_1% 2TypeC@

AC coupling caps and PU/PD on AUX lines are implemented inside Burnside Bridge

SC40000H800
TBT_0_TTX_R_DRX_P0 1 DT2 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TTX_R_DRX_P1 1 DT3 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TTX_R_DRX_N0 1 DT4 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TTX_R_DRX_N1 1 DT5 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TRX_R_DTX_P0 1 DT6 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TRX_R_DTX_P1 1 DT7 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TRX_R_DTX_N0 1 DT8 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2
TBT_0_TRX_R_DTX_N1 1 DT9 2 ESD@ AZ5B8S-01F.R7G_DFN0603P2Y2

UT2C @

GND

VSS_ANA: B1, B12, D1, D2, D11, D12, F1, F2, F7, F9, F11, F12, G7, H1, H2, H11, H12, J9, K1, K2, K11, K12, G5, G6, G3
BURNSIDE-BRIDGE_BGA105

25M XTAL (Type-C Port0)

25MHZ 20PF +-10PPM 8Y25070020
SJ10000XC00
Crystal
YT1
DG0_XTAL_25M_XI R2 EMI@ 1 33_0201_5%
DG0_XTAL_25M_XO R2 EMI@ 1 33_0201_5%
RT1133
+0.9VO_TBT_0_SVR_IND
C2 27P_0201_25V8 TypeC@
C3 27P_0201_25V8 TypeC@
Suggest adding GND shield across Crystal and 18pF caps for better RFI.

UT2B @

Power

+3VO_TBT_0_ANA
+3VO_TBT_0_LC RT1132
+0.9VO_TBT_0_LC
+0.9VO_TBT_0_LVR
VCC3P3_ANA L2
VCC3P3_LC E5
VCC0P9_SVR_ANA F6 G6
VCC0P9_SVR E3 G3
VCC0P9_SVR_PB_ANA E9 G9
VCC0P9_LC J3
VCC0P9_LVR L6
VCC0P9_LVR_SENSE M6
VCC3P3_SX E6
VCC3P3_SVR M4 M5
VCC3P3_SVR J5 J7
VCC3P3A L1
SVR_IND M1
SVR_VSS M2 M3
NC_J6 J6
+3VS_RETIMER_0
+3VS_RETIMER_0_A
+0.9VO_TBT_0_SVR_IND
BURNSIDE-BRIDGE_BGA105

JTAG (Type-C Port0)

+3VO_TBT_0_LC
RT46 10K_0402_5%
RT47 10K_0402_5%
RT48 10K_0402_5%
RT49 10K_0402_5%
JTAG1
DG0_JTAG_TDI
DG0_JTAG_TMS
DG0_JTAG_TCK
DG0_JTAG_TDO
GND
ACES_50228-0067N-001
CONN@

SPI ROM (Type-C Port0)

+3VALW +3VS_RETIMER_0
RT1129 @ 2 0_0402_5%
RT1130 short@ 2 0_0402_5%
+3V_TBT_FLASH
DT1 1N4148WS-L_SOD323-2
CT34 2.2U_0201_10V6K TypeC@
DG0_SPI_CS# RT42 1 TypeC@ 2 2.2K_0201_5%
DG0_SPI_DO RT43 1 TypeC@ 2 2.2K_0201_5%
DG0_SPI_WP# RT44 1 TypeC@ 2 3.3K_0201_5%
DG0_SPI_HOLD# RT45 1 TypeC@ 2 3.3K_0201_5%
DG0_SPI_CS# RT52 2 short@ 1 0_0201_5% DG0_SPI_CS#_R 1
DG0_SPI_DO RT53 2 short@ 1 0_0201_5% DG0_SPI_DO_R
DG0_SPI_WP#
UT3
CS# VCC
DO(IO1) HOLD#(IO3)
WP#(IO2) CLK
GND DI(IO0)
W25Q80DVSSIG_SO8
TypeC@
SA00003EW10
DG0_SPI_HOLD#
DG0_SPI_CLK_R RT54 1 EMI@ 2 2.2_0201_1% DG0_SPI_CLK
DG0_SPI_DI_R RT55 2 short@ 1 0_0201_5% DG0_SPI_DI
DG0_SPI_CLK_R
CT72 @EMI@ 10P_0201_25V8

Power Supply Decoupling of Type-C Port0

+0.9VO_TBT_0_SVR_IND
LT1 0.68UH_DFE252012P-R68M-P2_3.5A_20% TypeC@
+0.9VO_TBT_0_SVR
CT230 TypeC@ 47U_0603_6.3V6M
CT19 TypeC@ 47U_0603_6.3V6M
18P_0201_25V8J
2.2U_0201_6.3V6M
Pin P9
Pin G9
Pin J3
Pin E5
Pin L2
Pin M4
Pin M5
Pin J5
Pin J7
Share Same GND plane and connect to M2 & M3 pins (SVR_VSS) of BB
+3VS_RETIMER_0
+3VO_TBT_0_LC
+3VO_TBT_0_ANA
+3VS_RETIMER_0_A
RT50 0_0402_5% 2 short@ 1
RT51 0_0402_5% 2 short@ 1
10U_0402_6.3V6M
4.7U_0402_6.3V6M
2.2U_0201_6.3V6M
18P_0201_25V8J
All 0201 decoupling caps should be places as close as possible to the re-timer power pins
Follow Burmside Bridge Ref Schematic
Place holder for RC filter to reduce ripple to VCC3v3A pin

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/12/31

Compal Electronics, Inc.
Title: TBT_TYPE-C Port0 (1/2)
Size: Document Number: LA-K261P
Rev: 0.3
Date: Friday, August 14, 2020
Sheet 42 of 100

Feature List:
1. Support TBT/USB/DP/MF Retimer over SingleType-C port
2. Support Source of 5v @ 3A from Type-C port
3. Support Sink of up to 20v @ 5A over Type-C port
4. Support USB2 directly over Type-C port

SOC + EC (Ice Lake)
I2C Network
PD Solution

I2C1(Slave) to EC
[58,66] EC_SMB_CK2
[58,66] EC_SMB_DA2
[58] TBT_PD_IC2_INT#

I2C2(Slave) to PCH
[9,42] SOC_SML1CLK
[9,42] SOC_SML1DATA
[11,42] SOC_PD_INT#

I2C3(Master) to BB
[42] I2C3_PD_R_CLK
[42] I2C3_PD_R_DAT
[42] I2C3_PD_R_INT#

UT4
PTPS65992DADRJKT VQFN 38P USB PD S
SA0000DV800
R1:SA0000DLV10
S IC PTPS65992DADRJKT WQFN 38P USB PD S, A.3
R3:SA0000DV800
S IC SN1905027RJKR WQFN 38P USB PD A32 !, A.3

EC
PCH
BBR

placement issue, change 22U*2 to10U*4

Right PD Controller SPI FLASH

UT13
CAT24C256WI-GT3_SO8
SA000088F00

CC/SBU OVP

UT5
PJE138K 1N SOT-523-3
SB00001KM00

UT6
PJE138K 1N SOT-523-3
SB00001KM00

W = 200 mils

DT13
CEST23NC24VU_SOT23-3
ESD@

JUSBC1
LOTES_GAP-AUSB0459-P1
CONN@

Need check pin define

DIV = R2/(R1+R2)
ADCIN1 = 1 (0.04)
ADCIN2 = 7 (0.75)
I2C Index #4
Address: 0x46

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DCINx} / (R_{UP} + R_{DCINx})[1]			Without using R_{UP} or R_{DCINx}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

Table 6. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value [1]	ADCIN2 decoded value [1]	I^2C address Index[2]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	Negotiate Highest Voltage [3]: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the "APP" mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable he sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

Table 5. I^2C Default Slave Address for I2C_EC_SCL/SDA.

I^2C address index (decoded from ADCIN1 and ADCIN2)[1]	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

DT10
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00

LT2
DLM0NSN900HY2D_4P
SM070005U00

0520 Remove EMI 0 ohm

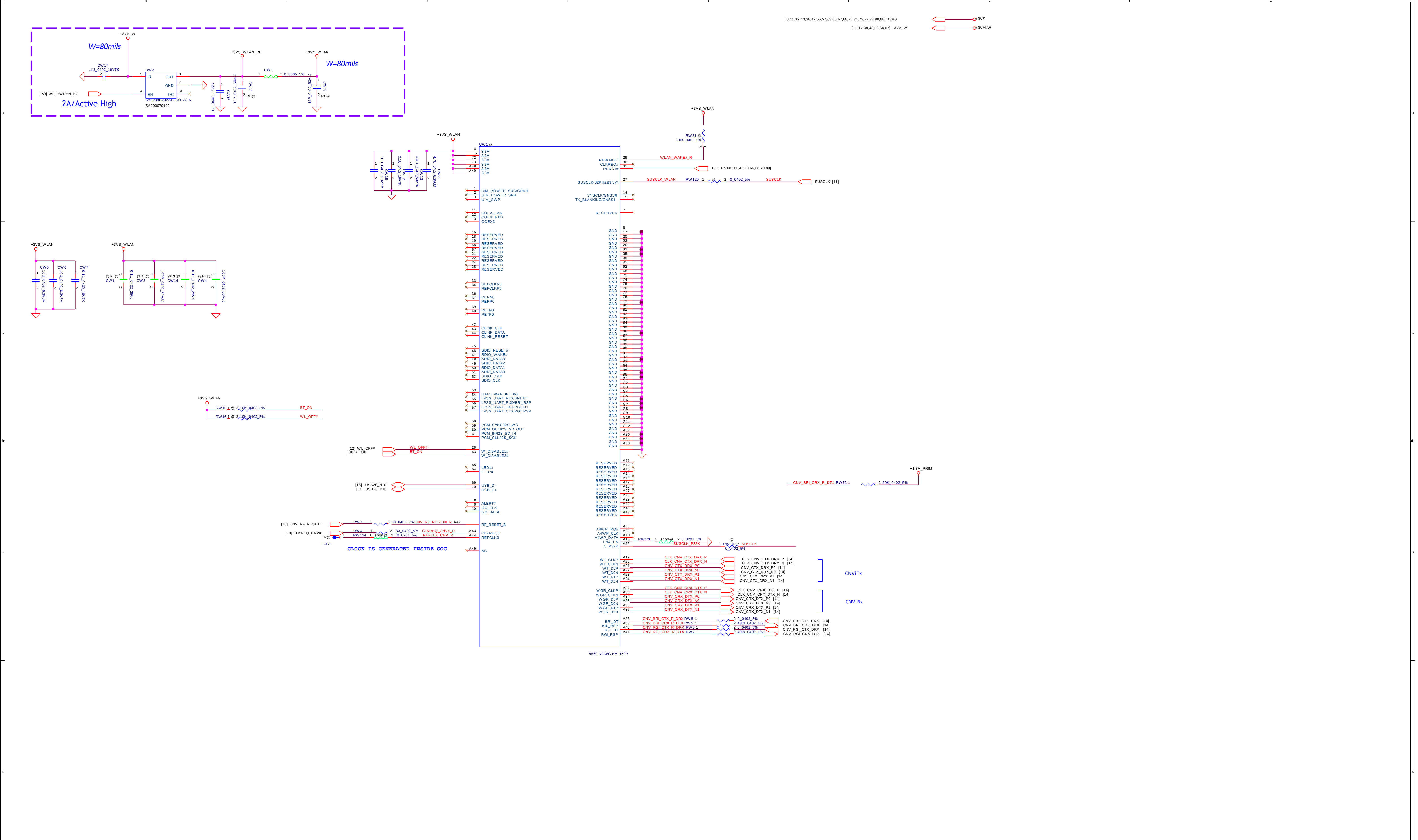
PIN SWAP 0205

DT11
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00

Double

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/12/31

Compal Electronics, Inc.
Title: TBT TYPE-C Port0 (2/2)
Size: Custom | Document Number: LA-K261P | Rev: 0.3
Date: Friday, August 14, 2020 | Sheet 43 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/11/28	Deciphered Date	2019/11/28

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Compal Electronics, Inc.

Title: **WLAN-BT**

Document Number: LA-J471PR03 — Rev V0.4

Date: Friday, August 14, 2020 — Sheet 52 of 99

RTD3 support

2019/06/26
RA8,RA9,RA10 change to 10ohm
follow LA-H481P

To SPK Amp

close to CODEC:ALC3292

UA1
ALC3315-CG_MQFN48_6X6
SA0000CYU00

need to check

DVDD-IO must be equal to or smaller than DVDD

RA13 , RA15 follow Vendor review change to 30ohm

Headphone

need check CA13 stuff or not

To AMP

Codec IO power
Place near Pin3

Codec HDA-link power
Place near Pin18

Codec ADCs/DACs power
Place near Pin20

Codec Mixers/IO power
Place near Pin40

Vendor reveiw
Place near Pin39

PC Beep
Close to Codec pin34

Low Active

Need to check to connect +DVDD

Reserve for ESD request.

Codec Stage power
Place near Pin41
Place near Pin46

600ohms @100MHz 2A
P/N: SM01000EE00

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/12/31

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Compal Electronics, Inc.

Title: AUDIO ALC3292-CG

Size: Custom | Document Number: LA-K261P | Rev: 0.3

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+12.6VB
+19VB_PVDD_AMP
LAA5 1 short@ 2 0_0603_5%
LAA6 1 short@ 2 0_0603_5%

+19VB_PVDD_AMP
@CAA1
10U_0603_25V6M
CAA7 10U_0603_25V6M
CAA8 10U_0603_25V6M
CAA9 0.1U_0402_25V6K
CAA45 1000P_0402_50V7K
CAA46 10U_0603_25V6M
CAA47 10U_0603_25V6M
close to Pin1 & Pin56
CAA13 10U_0603_25V6M
CAA14 10U_0603_25V6M
CAA15 0.1U_0402_25V6K
CAA47 1000P_0402_50V7K
close to Pin51

+19VB_PVDD_AMP
@CAA2
10U_0603_25V6M
CAA10 10U_0603_25V6M
CAA11 10U_0603_25V6M
CAA12 0.1U_0402_25V6K
CAA48 1000P_0402_50V7K
CAA49 10U_0603_25V6M
close to Pin42 & Pin43
CAA16 10U_0603_25V6M
CAA17 10U_0603_25V6M
CAA18 0.1U_0402_25V6K
CAA50 1000P_0402_50V7K
close to Pin48

+19VB_PVDD_AMP
CAA23 10U_0603_25V6M
CAA24 0.1U_0402_25V6K
CAA25 1000P_0402_50V7K
Place near Pin37

+1.8VS_AVDD_AMP
RAA2 1 short@ 2 +1.8VS
0_0402_5%
CAA5 0.1U_0201_6.3V6K
CAA6 1U_0201_6.3V6M
Place near Pin21

+1.8VS
RAA1 1 short@ 2
0_0402_5%
+1.8VS_DVDD
CAA3 0.1U_0201_6.3V6K
CAA4 1U_0201_6.3V6M
Place near Pin17

+3VS_DVDD_IO
RAA3 1 short@ 2 +3VS
0_0402_5%
CAA19 0.1U_0201_6.3V6K
CAA20 1U_0201_6.3V6M
Place near Pin16

+1.8VS_AVDD_AMP
@RAA4 0_0201_5%
1U_0402_25V6K
RAA6 100K_0201_5%
CAA21 1U_0402_25V6K
+3VS_DVDD_IO
+1.8VS_DVDD
+19VB_PVDD_AMP

close to UAA1

UAA1
PVDD-A 1
PVDD-A 56
PVDD-B 51
PVDD-C 48
PVDD-D 43
PVDD-D 42
AVDD1 37
AVDD2 21
PGVdd 6
GVDD-AB 3
GVDD-CD 40
DVDD-IO 16
DVDD 17

OUTA_SPK_L- 0.22U_0402_25V7K 1 2 CAA26 BST_A 2 BST-A
OUTB_SPK_L+ 0.22U_0402_25V7K 1 2 CAA27 BST_B 50 BST-B
OUTC_SPK_R- 0.22U_0402_25V7K 1 2 CAA28 BST_C 49 BST-C
OUTD_SPK_R+ 0.22U_0402_25V7K 1 2 CAA29 BST_D 41 BST-D
10U_0402_6.3V6M 1 2 CAA30 +LDO_A1.5V 22 LDOA1.5

OUTA_SPK_L-_R RAA9 1 2 39K_0402_0.1% ISENSEP_L 25 LISENDE_P
OUTA_SPK_L-_R_CONN RAA10 1 2 39K_0402_0.1% ISENSE_L 26 LISENDE_N/LVSENSE_P
OUTB_SPK_L+_CONN RAA11 1 2 39K_0402_0.1% VSENSEN_L 27 LVSENSE_N
22.1K_0402_1% 1 RAA12 2 5 OCADJ
OUTC_SPK_R-_R RAA13 1 2 39K_0402_0.1% ISENSEP_R 28 RISENSE_P
OUTC_SPK_R-_R_CONN RAA14 1 2 39K_0402_0.1% ISENSE_R 29 RISENSE_N/RVSENSE_P
OUTD_SPK_R+_CONN RAA16 1 2 39K_0402_0.1% VSENSEN_R 30 RVSENSE_N
32 NC
31 NC
36 NC
35 NC

SD00001O100
RAA30 RAA31 RAA32 RAA33 RAA34 RAA35
10K_0402_0.1%
Realtek FAE review:change to DGND.

GND 4
AGND 34
AGND 33
AGND 24
AGND 20
DGND 19
PGND-CD 46
PGND-CD 45
PGND-AB 54
PGND-AB 53
ThermalPad 57
ALC1305H-CGT_QFN56_7X7
SA00009HI10
RAA24 10K_0201_5%
Realtek FAE review:change to DGND.

SDA 7 I2C_DATA_AMP [56]
SCL 8 I2C_CLK_AMP [56]
ASEL 18 AMP_ADD_SEL
SYNC-IN 39
SYNC-OUT 38
+3VS_DVDD_IO
RAA7 10K_0201_5%
RAA8 10K_0201_5%
I2C Address Selection
Low:0x20
Hi:0x22

OUT-A 55 OUTA_SPK_L-
OUT-B 52 OUTB_SPK_L+
OUT-C 47 OUTC_SPK_R-
OUT-D 44 OUTD_SPK_R+
VREF 23 VREF_AMP CAA31 1 2 0.1U 16V K X7R 0402
MCLK 9 I2S_MCLK_R I2S_MCLK_R [56]
BCLK 10 I2S_BCLK_R I2S_BCLK_R [56]
LRCK 11 I2S_LRCK_R I2S_LRCK_R [56]
DACDAT 12 I2S_DOUT_R I2S_DOUT_R [56]
SPDIC_IN 13
SPDIF OUT/I2S DATOUT 14 I2S_DIN_R I2S_DIN_R [56]
PDBJD 15 AMP_PD
RAA37 1 2 I2S_MCLK_R 10K_0201_5%

[56] AMP_EAPD
DAA1 RB751S-40_SOD523-2 SCS00003700
RAA36 10K_0201_5%
+3VS_DVDD_IO
[56,59] EC_MUTE#
DAA2 RB751S-40_SOD523-2 SCS00003700
AMP_PD

OUTB_SPK_L+_CONN
OUTA_SPK_L-_R_CONN
@ESD@ D517 CEST23NC24VU_SOT23-3 SCA00004500

OUTD_SPK_R+_CONN
OUTC_SPK_R-_R_CONN
@ESD@ D518 CEST23NC24VU_SOT23-3 SCA00004500

OUTB_SPK_L+ LAA1 BLM21PG121SN1D_2P SM01000QG00 OUTB_SPK_L+_CONN
CAA32 330P_0402_50V8J @EMI@
RAA18 10_0402_1%
CAA33 680P_0402_50V7K @EMI@
SD00001T580

OUTA_SPK_L- LAA2 BLM21PG121SN1D_2P SM01000QG00 OUTA_SPK_L-_R_CONN
CAA38 330P_0402_50V8J @EMI@
RAA23 10_0402_1%
RAA22 0.2_0805_1%
OUTA_SPK_L-_R
CAA40 680P_0402_50V7K @EMI@
RAA22 Place near Connector

OUTD_SPK_R+ LAA3 BLM21PG121SN1D_2P SM01000QG00 OUTD_SPK_R+_CONN
CAA41 330P_0402_50V8J @EMI@
RAA25 10_0402_1%
CAA42 680P_0402_50V7K @EMI@
SD00001T580

OUTC_SPK_R- LAA4 BLM21PG121SN1D_2P SM01000QG00 OUTC_SPK_R-_R_CONN
CAA43 330P_0402_50V8J @EMI@
RAA27 10_0402_1%
RAA26 0.2_0805_1%
OUTC_SPK_R-_R
CAA44 680P_0402_50V7K @EMI@
RAA26 Place near Connector

Realtek FAE suggestion:
LAA1~LAA4 change to 120_ohm Bead.
CAA33,CAA40,CAA42,CAA44 use 680p.

OUTC_SPK_R-_R_CONN
OUTD_SPK_R+_CONN
OUTA_SPK_L-_R_CONN
OUTB_SPK_L+_CONN
[12] SPK_DET#
JSPK1 ACES_50278-00601-001 CONN@
Follow E team LA-G172P

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/12/31

Compal Electronics, Inc.
Title: Speaker Amp:ALC1305H
Size: Custom
Document Number: LA-K261P
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+3VL [17,43,64,71,76,83,84,85]
+3VALW_EC [12,38,43,59,64,67,73,82]
+1.05V_VCCST [7,11,15,16,88]
+3VALW [11,17,38,42,52,64,67]
+3V_SMBUS [64]
+3VS [8,11,12,13,38,42,56,57,63,66,67,68,70,71,73,77,78,80,88]

ESD@ 2 CK4 1 0.1U_0201_10V6K 1 PLT_RST#

+3VALW_EC RK7 2 @ 1 330K_0402_5% EC_RST#
CK5 1 2 0.1U_0201_10V6K @ESD@

+1.8V_PRIM RK215 1 short@ 2 0_0402_5%
Close to Chip
CK210 1 2 1U_0201_6.3V6K

+3VALW_EC CK1 1 2 0.1U_0201_10V6K
CK2 1 2 0.1U_0201_10V6K
+3VALW_EC LK1 S SUPPRE_TAI-TECH HCB1005KF-221T15 0402 1 2 +EC_VCCA
ECAGND CK3 1 2 0.1U_0201_10V6K

+3VALW_EC RK2 100K_0402_1%
BOARD_ID
RK4 43K_0402_1%

2020 Moonage

RK4	DB	SI	PV	MV
13" X360	0	15K	27K	43K

0: SD028000080
15K: SD034150280
27K: SD034270280
43K: SD034430280

0731 change

+3VALW_EC Power source move to P.64

CC3973 Close EC BOT side
CC3973 1 2 ESPI_CLK_R
@EMI@ 10P_0201_50V8J

12/24 Add KB_DISABLE

[64,82,84] VCIN1_ACOK R45 1 short@ 2 VCIN1_AC_IN_R EC Pin110 0_0201_5%

[64,71] USB_IN_STATUS# 2 short@ 1 RK223 0_0201_5%

+3VALW_EC RK228 2 1 100K_0201_5% PRI_DETECT#

RK26 2 1 100K_0201_5% E51TXD_P80DATA

Follow Intel SCH add

RK222 1 2 10K_0201_5% SYS_PWROK
RK221 1 2 10K_0201_5% PCH_DPWROK
RK20 1 2 10K_0201_5% PCH_PWROK
CK10 1000P_0201_50V7K ESD@

replace to common part 0108

R5815 1 @ 2 OPMODE 4.7K_0201_5%

OPMODE (Internal Pull High 40K) :

Pull Up : Intel eSPI Master Attached Flash Sharing Topology
Pull Down : The Legacy Share-SPI ROM Topology (SPI-Wire-OR mode)

+3V_LID RK234 2 0_0402_5% short@ 1
+3V_LID_EC 1
close to UK1 Pin J7
CK206 0.1U_0201_10V6K 2 1
CK207 2 1 100P_0201_50V8J VCIN1_AC_IN_R
close to UK1 Pin F5

Need to check

[6,38] BKL_PWM_CPU
RK55 1 2 100K_0201_1%
RK56 1 2 100K_0201_1%
BKL_PWM_ADI
CK204 0.1U_0201_10V6K 1 2
CK205 1 2
CK208 0.01U_0201_16V7 1 2
RK57 806K_0402_1% 2 1
0.1U_0201_10V6K 2 2

[11] PM_SLP_S0#
[9] EC_SLP_S0IX#
PM_SLP_S0# RK219 1 @ 2 0_0201_1% EC_SLP_S0IX#_R
EC_SLP_S0IX# RK220 1 short@ 2 0_0201_5%
follow TD design to reserve

SOC_SRTCRST# [11]
EC_RTC_RST 2 1 RK49 10K_0201_5%
QK4A L2N7002SDW1T1G 2N SC88-6 SB00001FF00 QK4 6 5 4

SOC_RTCRST# [11]
EC_RTC_RST 5 4 QK4B L2N7002SDW1T1G 2N SC88-6 SB00001FF00 QK4 3 2
@ RK50 10K_0201_5% 1 2

UK1
KB9542G FVFBGA
SA0000BPU30

VCC_LPC 1.8_3.3V
J4 VCC_LPC
TP@ T2410 EC_GPIO00 M2 GPIO00/GA20
TP@ T2411 ESPI_ALERT# EC_GPIO2_SERIRQ M3 GPIO01/KBRST#/ESPI_ALERT#
TP@ T2412 GPIO02/SERIRQ
LFRAME#/ESPI_CS#
LAD3/ESPI_IO3
GPIO04
LAD2/ESPI_IO2
LAD1/ESPI_IO1
LAD0/ESPI_IO0
PCICLK/ESPICLK
GPIO05/PCIRST#
GPIO07/ESPI_RST#
[9] ESPI_CS# ESPI_CS# K4
[9] ESPI_IO3_R ESPI_IO3_R N3
[12] KB_DISABLE KB_DISABLE J5
[9] ESPI_IO2_R ESPI_IO2_R M4
[9] ESPI_IO1_R ESPI_IO1_R K5
[9] ESPI_IO0_R ESPI_IO0_R N4
[9] ESPI_CLK_R ESPI_CLK_R N5
[12] SEN_MODE SEN_MODE M5
[9] ESPI_RST# ESPI_RST# N9
LPC /eSPI

VCC1 3.3V
M12 VCC1
+3VALW_EC
[63,66] TP_ENABLE TP_ENABLE K6 GPIO0A/OWM/RLC_RX2
USB_IN_STATUS#_R N6 GPIO0E/SCI#
[11] PCH_PWROK PCH_PWROK N12 GPIO1B/POWER_FAIL1
[88] VR_PWRGD VR_PWRGD L12 GPIO1A/NUMLED#
EC_RST# K13 ECRST#
M6 GPIO1D/CLKRUN#
MISC
[80] E51TXD_P80DATA E51TXD_P80DATA K10 GPIO16/TXD/SER_TXD/LPC_TXD
[80] E51RXD_P80CLK E51RXD_P80CLK K9 GPIO17/RXD/SER_CLK/LPC_CLK
[63] KBL_ON KBL_ON M9 GPIO0F/PWM0
[56] EC_BEEP# EC_BEEP# M8 GPIO10/PWM1
[38] BKL_PWM_EC BKL_PWM_EC K8 GPIO11/PWM2
[77] AC_LED# AC_LED# M13 GPIO19/PWM3/WDT_LED_ALT
PWM
[77] EC_FAN_PWM1 EC_FAN_PWM1 M10 GPIO12/FANPWM0
N10 GPIO13/FANPWM1
[77] FAN_SPEED1 FAN_SPEED1 M11 GPIO14/FANFB0
EC_RTC_RST N11 GPIO15/FANFB1
[63] KSI[0..7] KSI0 E9 GPIO30/KSI0/SER_TXD/TH3
KSI1 E12 GPIO31/KSI1
KSI2 E13 GPIO32/KSI2
KSI3 D12 GPIO33/KSI3
KSI4 D13 GPIO34/KSI4/EDICS
KSI5 C12 GPIO35/KSI5/EDICLK
KSI6 C13 GPIO36/KSI6/EDIDI
KSI7 E10 GPIO37/KSI7/EDIDO
IKB
[63] KSO[0..15] KSO0 J13 GPIO20/KSO0/HT0
KSO1 J12 GPIO21/KSO1/HT2
KSO2 H12 GPIO22/KSO2/HT1
KSO3 H13 GPIO23/KSO3/HT_EN
KSO4 J10 GPIO24/KSO4
KSO5 J9 GPIO25/KSO5
KSO6 H9 GPIO26/KSO6
KSO7 H10 GPIO27/KSO7
KSO8 G13 GPIO28/KSO8
KSO9 G12 GPIO29/KSO9
KSO10 F13 GPIO2A/KSO10
KSO11 F12 GPIO2B/KSO11
KSO12 G10 GPIO2C/KSO12
KSO13 G9 GPIO2D/KSO13
KSO14 F10 GPIO2E/KSO14
KSO15 F9 GPIO2F/KSO15
IKB
[38] PRI_EN PRI_EN D9 GPIO48/KSO16
[38] PRI_DETECT# PRI_DETECT# D10 GPIO49/KSO17
GWG
[64,84,85] EC_ON EC_ON F5 GPIO79/AC_IN
[76] ON/OFF# ON/OFF# G1 GPIO7A/ALW_PWR_EN
[64,66] LID_SW# LID_SW# G5 GPIO7B/ON/OFFBTN#
H1 GPIO7C/LID_IN
PLC
VCC0 3.3V
J7 VCC0
PECI
PECI_VTT H4
GPIO7F/PECI H2 EC_PECI RK216 1 2 43_0402_1% H_PECI [7]
GND1 G2
GND2 N13
AGND A11
ECAGND [82]
LK2 ECAGND 2 1 TAI-TECH HC81005KF-221T15 0402
Connect to PWR side

VCC
VCC_IO2

AVCC 3.3V
B11 AVCC +EC_VCCA
ADC
GPIO38/AD0 B13 B/I# B/I# [83,84]
GPIO39/AD1 A13 SHUTTER_FBC SHUTTER_FBC [38,73]
GPIO3A/AD2 B12 ADP_I ADP_I [84]
GPIO3B/AD3 A12 BOARD_ID
GPIO42/AD4 D6 ADP_ID
GPIO43/AD5 D7 BKL_PWM_ADI ADP_ID [82]
GPIO40/CIR_RX/AD6 B6 LID_SW2# LID_SW2# [12,64]
GPIO41/CIR_RLC_TX/AD7 B7
DAC
GPIO3C/DA0 B10 EC_VCCST_EN EC_VCCST_EN [16]
GPIO3D/SWTRAP/DA1 A9 OPMODE
GPIO3E/DA2 A10 PM_SLP_S3# PM_SLP_S3# [11,16]
GPIO3F/DA3 B9 BARREL_IN BARREL_IN [82]

RK226 1 @ 2 0_0201_5% +1.05EXTOBYPASS_PG
RK235 1 2 0_0201_5% PG_AUX [87,91]
PG_VCCIN_AUX

[88] VR_HOT# VR_HOT# 1 short@ 2 RK8 0_0201_5% H_PROCHOT# [7,84]
H_PROCHOT#_EC 1 short@ 2 RK9 0_0201_5%
+1.05EXTOBYPASS_PG [87]
@ESD@ CK12 1000P_0201_50V7K
replace to common part 0108

SM / ESB
GPIO08/PROCHOT2#/SCL4 L13 SLP_SUS# SLP_SUS# [11]
GPIO0D/RLC_TX2/SDA4 N8 SPOK SPOK [11,85]
GPIO0B/ESBCLK/SCL5 N7 KC3810_ESB_CLK KC3810_ESB_CLK [59]
GPIO0C/ESBDAT/SDA5 M7 KC3810_ESB_DAT KC3810_ESB_DAT [59]

3.3V VCC2 K12 +3VALW_EC
SM
GPIO44/SCL0 A8
GPIO45/SDA0 A7
GPIO46/IEDI_SCL/SCL1_BatMgr B8 EC_SMB_CK2_R 0_0201_5% 2 short@ 1 RK217 EC_SMB_CK1 [64,67,83,84]
GPIO47/IEDI_SDA/SDA1_BatMgr A6 EC_SMB_DA2_R 0_0201_5% 2 short@ 1 RK218 EC_SMB_DA1 [64,67,83,84]
EC_SMB_CK2 [43,66]
EC_SMB_DA2 [43,66]
PS2
GPIO4A/I2CD_CLK/PSCLK1/SCL2 D6 RESUME# RESUME# [73]
GPIO4B/I2CD_DAT/PSDAT1/SDA2 E7 EC_SMB_DA3 [73]
GPIO4C/PSCLK2/SCL3 E5 ISH_I2C_0_SCL_EC 0_0201_5% 2 short@ 1 RK232 ISH_I2C_0_SCL [12,38,67]
GPIO4D/PSDAT2/SDA3 D5 ISH_I2C_0_SDA_EC 0_0201_5% 2 short@ 1 RK233 ISH_I2C_0_SDA [12,38,67]
Shutter
IKB
GPIO4E/PSCLK3/KSO18 A5 TP_CLK TP_CLK [63]
GPIO4F/PSDAT3/KSO19 B5 TP_DATA TP_DATA [63]
GPIO52/KSO20 A4 BAT_CHG_LED BAT_CHG_LED [77]
SHI
GPIO60/SHICS# B1 SOC_ENBKL SOC_ENBKL [6]
GPIO61/SHICLK A1 SYS_PWROK SYS_PWROK [11]
GPIO62/SHID0 C1 ME_EN ME_EN [10]
VC
GPIO78/ADC8/SHIDI/VCIN0 C2 VCIN0_PH VCIN0_PH [82]
GPIO67/VCOUT0 E4 MAINPWON MAINPWON [85]
GPIO65/ADC9/VCIN1 D2 VCIN1_PH VCIN1_PH [82]
GPIO66/PROCHOT#/VCOUT1 E2 H_PROCHOT#_EC
GPIO50/LOCK# B4 TBT_PD_IC2_INT# TBT_PD_IC2_INT# [43]
GPIO53/CAPSLED# B3 CAP_LOCK# CAP_LOCK# [63]
GPIO54/WDT_LED A3 PWR_LED# PWR_LED# [63]
GPIO55/SCROLED# A2 AC_PRESENT AC_PRESENT [11]
GPIO56 B2 SYSON SYSON [78,86]
GPIO63/POWER_FAIL0/FANFB2 D4 EC_RSMRST# EC_RSMRST# [11]
GPIO64/FANFB3 D1 FPR_LOCK# FPR_LOCK# [66]
GPIO69 F4 VCCST_OVERRIDE_LS VCCST_OVERRIDE_LS [16]
GPIO6B/GWG F1 EC_SLP_S0IX#_R
GPIO68/IO2_SHR_ROM E1 EC_BKOFF# EC_BKOFF# [38]
GPIO6A/IO3_SHR_ROM F2 PCH_PWR_EN PCH_PWR_EN [17,78,87]
1.8_3.3V VCC_IO2 N1
SHR_ROM
GPIO5B/MISO_SHR_ROM K2 FPR_OFF# FPR_OFF# [66]
GPIO5C/MOSI_SHR_ROM J2 PLT_RST# PLT_RST# [11,42,52,66,68,70,80]
GPIO58/SPICLK_SHR_ROM L1 SX_EXIT_HOLDOFF#_R RK227 1 short@ 2 0_0201_5% SX_EXIT_HOLDOFF# [11]
GPIO5A/SPICS#_SHR_ROM N2 DYNAMIC_SAR_EN DYNAMIC_SAR_EN [12]
GPIO57/XCLK32K H5 VR_ON VR_ON [11,88]
GPIO5D/XCLKI J1 PBTN_OUT# PBTN_OUT# [11]
GPIO5E K1 PM_SLP_S4# PM_SLP_S4# [11,86]
GPIO59/DPWROK M1 PCH_DPWROK PCH_DPWROK [11]
GPIO7D G4 SUSP# SUSP# [16,38,78,86,93]
GPIO7E K7 EC_VCCST_PG_R EC_VCCST_PG_R [11]

+3VALW_EC CK8 1 2 4.7U_0402_6.3V6M
+1.05V_VCCST CK211 1 2 0.1U_0201_10V6K
Close to Chip

TP_CLK RK12 1 2 4.7K_0201_5%
TP_DATA RK13 1 2 4.7K_0201_5%
KC3810_ESB_CLK RK207 1 2 4.7K_0201_5%
KC3810_ESB_DAT RK208 1 2 4.7K_0201_5%

EC_ON RK29 2 1 100K_0201_5%
PCH_PWR_EN RK30 2 @ 1 100K_0201_5%
PLT_RST# RK31 2 1 100K_0201_5%
PBTN_OUT# R295 1 @ 2 1K_0201_5%

EC_SMB_CK1 2 RH232 1 2.2K_0201_5%
EC_SMB_DA1 2 RH233 1 2.2K_0201_5%
EC_SMB_CK2 2 RH234 1 2.2K_0201_5%
EC_SMB_DA2 2 RH235 1 2.2K_0201_5%

SYSON RK23 1 @ 2 100K_0201_5%
CK9 1 2 1000P_0201_50V8J ESD@
SUSP# RK27 1 @ 2 100K_0201_5%

Compal Electronics, Inc.

VR_HOT# 2 CK11 1 0.1U_0201_10V6K ESD@

Security Classification	Compal Secret Data		
Issued Date	2020/09/17	Deciphered Date	2018/09/17

Title: EC ENE-KB9022
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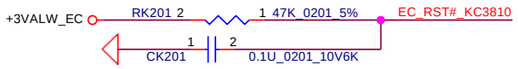
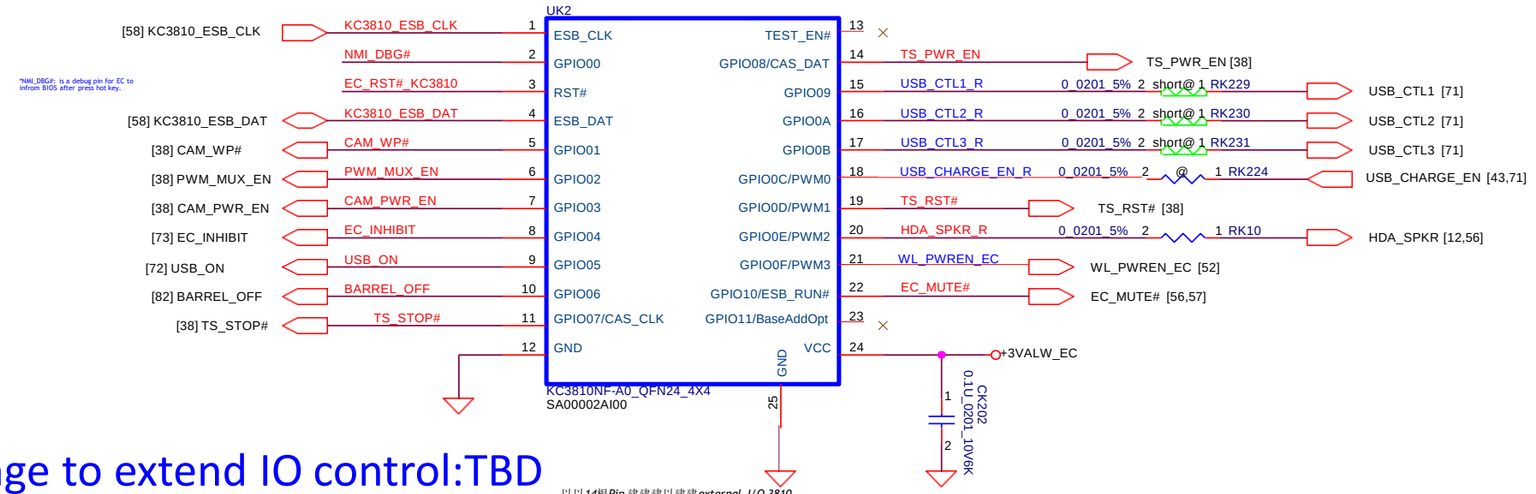
+3VALW_EC
+5VS

+3VALW_EC [12,38,43,58,64,67,73,82]
+5VS [56,77,78]

OMEN New ESB CLK&DAT for Extend I/O

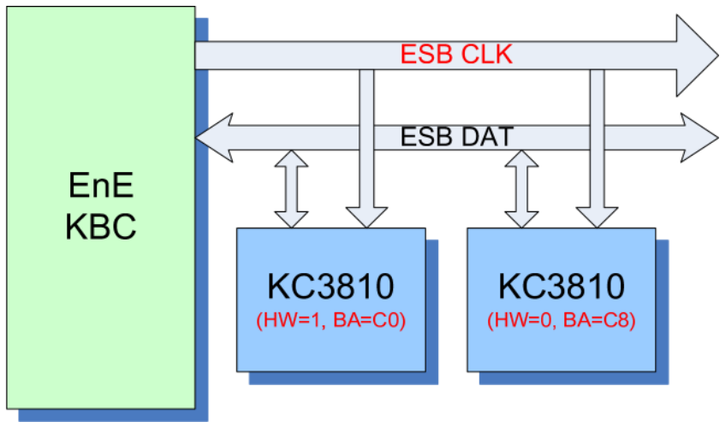
Some EC GPIO maybe change to extend IO control:TBD

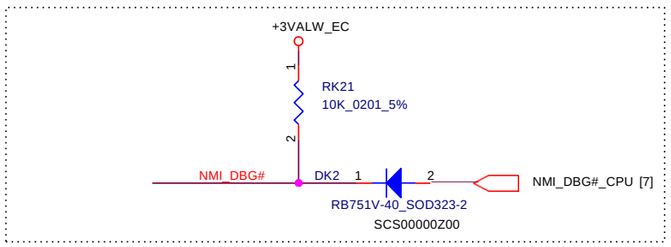




以以14根Pin 建建建以建建external I/O 3810,
1. USB_CTL1(GPIO4B Pin84),
2. USB_CTL2(GPIO3F Pin72),
3. USB_CTL3(GPIO1D Pin38),
4. USB_CHARGE_EN(GPIO1A Pin36),
5. GPU_OVERT#(GPIO0D Pin19) => DPF50 NO USE
6. LAN_PWR_EN(GPIO4D Pin86),
7. WL_PWREN_EC#(GPIO61 Pin98),
8. DCHG_I(GPIO40 Pin73) => DPF50 NO USE
9. USB_ON#(GPIO37 Pin 121),
10. LED : 5 Pin.

Some EC GPIO maybe change to extend IO control:TBD





Security Classification	Compal Secret Data		
Issued Date	2020/09/17	Deciphered Date	2018/09/17

Compal Electronics, Inc.

Title: TBD

Size: Custom | Document Number: LA-K261P | Rev: 0.3

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1	VDD Power Supply Voltage
2	DATA PS/2 Data
3	CLK PS/2 Clock
4	GND
5	I2C Clock or SMBus Clock
6	I2C Data or SMBus Data
7	I2C INT
8	Touchpad Enable/Disable

EC PS/2

CPU SMB

[58] TP_DATA
[58] TP_CLK
[9] TP_SMBCLK
[9] TP_SMBDATA
[58,66] TP_ENABLE

+3VS R6575 1 short@ 2 0_0402_5%

+3V_TP 0.1U_0201_6.3V6K @EMI@ CK23

CONN@ SDAN_606022-0080 41 JTP1

[7] I2C_INT#_TP R18 1 short@ 2 0_0201_5%

I2C_INT#_TP_R 10K_0201_5% R6551

DM5 ESD@ AZ1045-04F_DFN2510P10E-10-9 SC300001Y00

TP_SMBDATA CC167 56P_0201_25V8
TP_SMBCLK CC168 56P_0201_25V8

2019/11/22
For SVTP reserve Cap

DT15 ESD@ AZ1045-04F_DFN2510P10E-10-9 SC300001Y00

I2C_INT#_TP_R
TP_ENABLE

[58] KSI[0..7]
KSI7 KSI6 KSI5 KSI4 KSI3 KSI2 KSI1 KSI0

ESD@ CK20 100P_0402_50V8J

[58] KSO[0..15]
KSO15 KSO14 KSO13 KSO12 KSO11 KSO10 KSO9 KSO8 KSO7 KSO6 KSO5 KSO4 KSO3 KSO2 KSO1 KSO0

JKB1	KB Spec
Pin1	5V KSI1
Pin40	KSI1 5V

[11,17,38,42,52,58,64,67] +3VALW
[56,77,78] +5VS

ELETRO-X TECHNICAL

Keyboard conn

JKB1

+3VS_SHUTTER

[76] ON/OFF#_R
[73] SHUTTER_LED#
[58] PWR_LED#
[56] MIC_MUTE_LED#
[56] SPK_MUTE_LED#
[58] CAP_LOCK#
[73] SHUTTER_KEY

RK22 10K_0201_5% +3VS_SHUTTER_R
RK24 1K_0402_5% ON/OFF#_R
RK25 1K_0402_5% SHUTTER_LED#_R
RK33 680_0402_5% PWR_LED#_R
RK32 1K_0402_5% MIC_MUTE_LED#_R
RK41 1K_0402_5% SPK_MUTE_LED#_R
CAP_LOCK#_R
SHUTTER_KEY

+5VS_KB

+5VALW

R6581 0_0402_5% short@

+5VS_KB_R

HEFEN_AFB01-S40F1A-HF_40P SP01002T000 CONN@

Pin36 SHUT_LED power
Pin37 PWR_LED power
Pin38 MIC_MUTE_LED power
Pin39 SPK_MUTE_LED power
Pin40 CAPS_LED power

+5VALW RK5105 2 short@ 1 0_0603_5% +5VS_KBL

PWR_LED# RU1 680_0402_1% LEDU1 LTW-110DC5-C_WHITE SC500004Y20 @

Q2 PJ2301 1P SOT23-3 SB00000T900

R41 100K_0402_5%

PWR_LED#
High : Turn OFF
Low : Turn ON

C11 100P_0201_50V8J

+5VALW R23 100K_0201_5%

+5VS_KBL JKBL1 CONN@ ACES_51575-00401-001 SP01002BY00

KBL_ON_GND

Q9 AO3416L 1N SOT-23

KBL_ON [58]

RK44 100K_0201_5%

ESD@ CK17 CAP_LOCK#_R 100P_0201_50V8J
ESD@ CK18 SPK_MUTE_LED#_R 100P_0201_50V8J
ESD@ CK19 PWR_LED#_R 100P_0201_50V8J
ESD@ CK21 MIC_MUTE_LED#_R 100P_0201_50V8J
ESD@ CK22 SHUTTER_LED#_R 100P_0201_50V8J

ESD Diode

D1 ESD@ AZ1045-04F_DFN2510P10E-10-9 SC300001Y00

ON/OFF#_R
CAP_LOCK#_R
SHUTTER_LED#_R
SHUTTER_KEY

Caps Lock VCC 40 GND 34
Speaker Mute LED VCC 39 GND 33
MIC Mute LED VCC 38 GND 32
Power LED VCC 37 GND 31
Privacy CAM LED VCC 36 GND 30
Power Key 29 27
Privacy Cam 35 28

ELETRO-X TECHNICAL

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

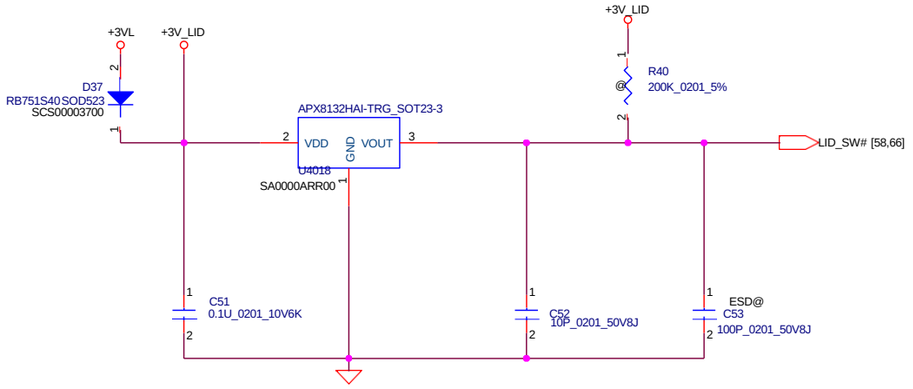
Compal Electronics, Inc.

Title: KB/TP

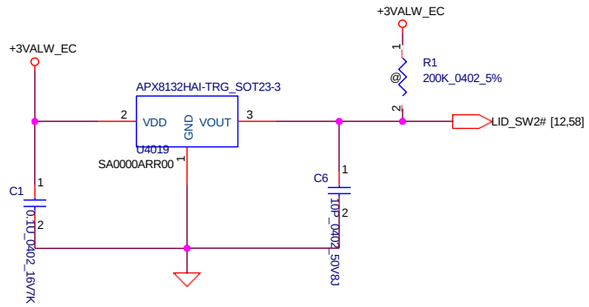
Size: Custom | Document Number: LA-K261P | Rev: 0.3

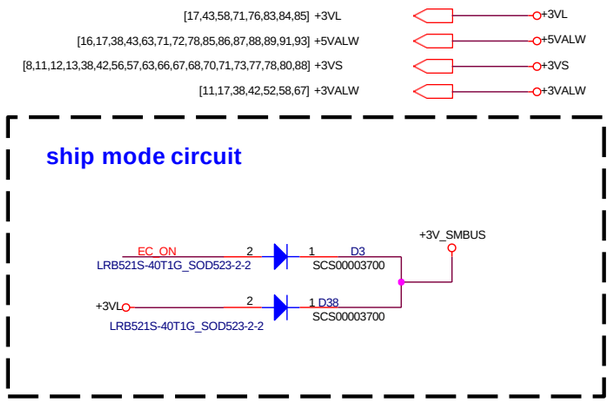
Date: Friday, August 14, 2020 | Sheet 63 of 100

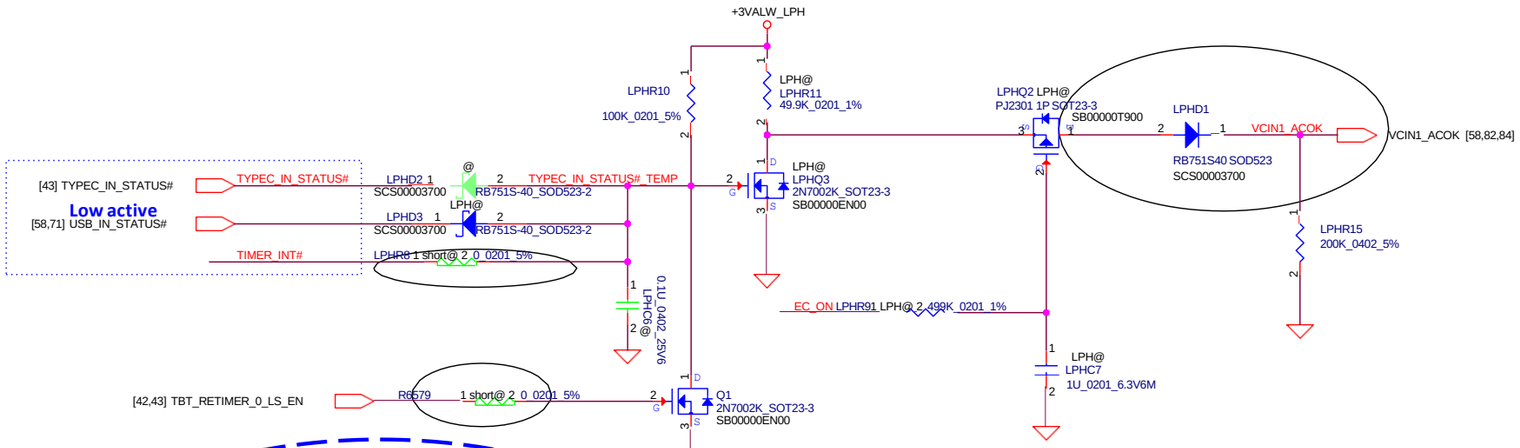
TOP
Lid Switch (Hall Effect Sensor)

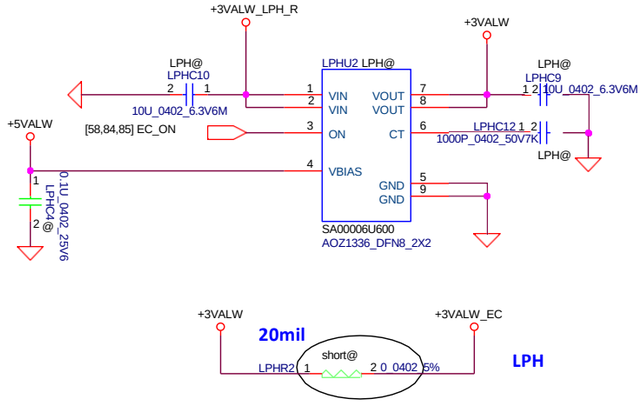


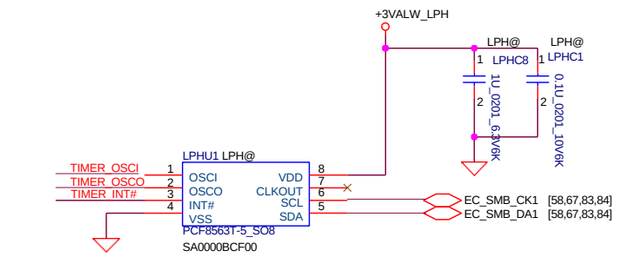
BOTTOM
Lid Switch (Hall Effect Sensor)





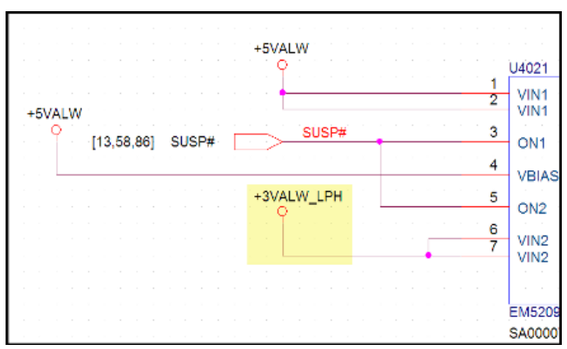




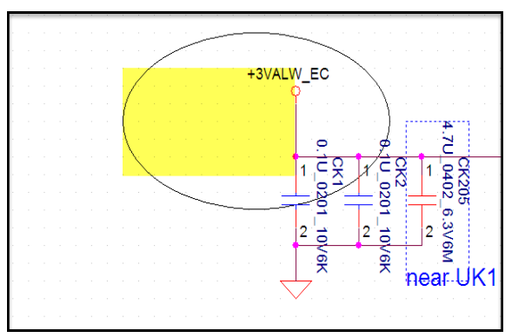


	LPHR1	LPHR2	JPLPH1	JPLPH2	LPHU2	LPHD1
	+3VL to EC_VCC	+3VALW to EC_VCC	Load SW input	Bypass Load SW	SW input	
non-LPH	V			V		
LPH		V	V		V	V

+3VS Source need change to +3VALW_LPH



Remove the bypass resistor at EC page.



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Issued Date	2019/07/17	Deciphered Date	2019/07/17

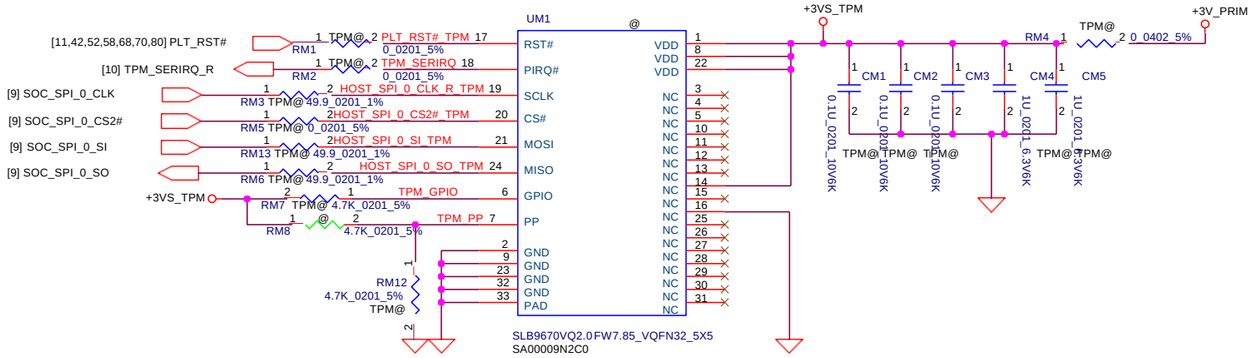
Compal Electronics, Inc.

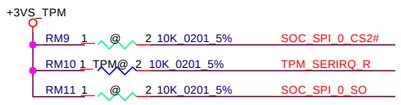
Title: LID

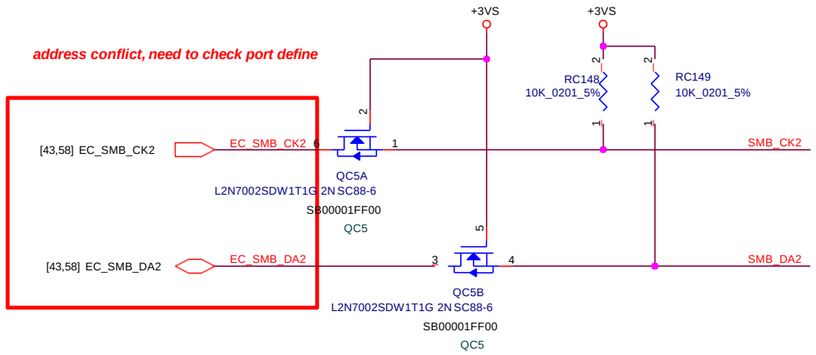
Size: C | Document Number: LA-J471PR01 | Rev: V0.1

Date: Friday, August 14, 2020 | Sheet 64 of 99

TPM2.0

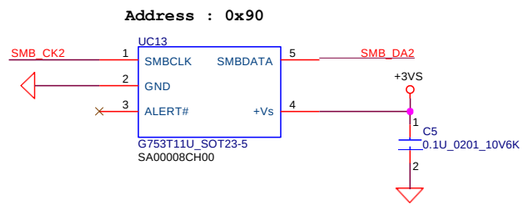




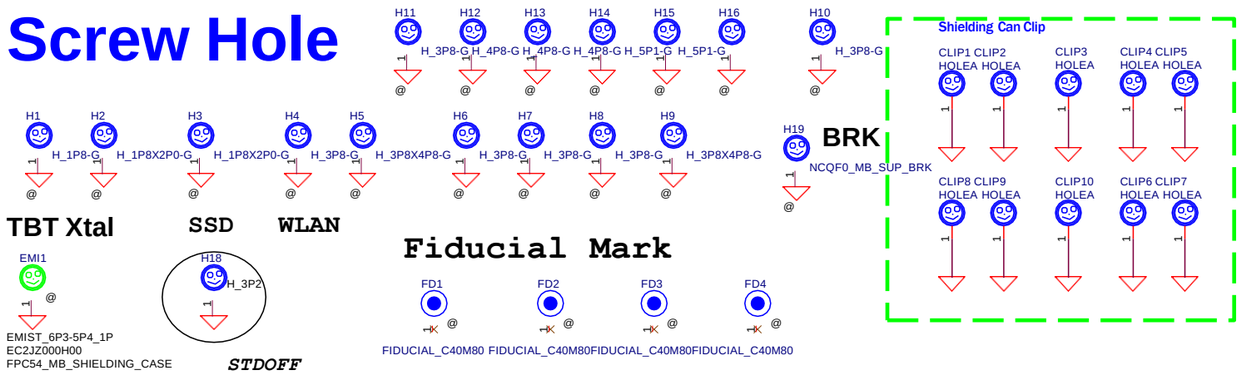


CPU THERMAL SENSOR

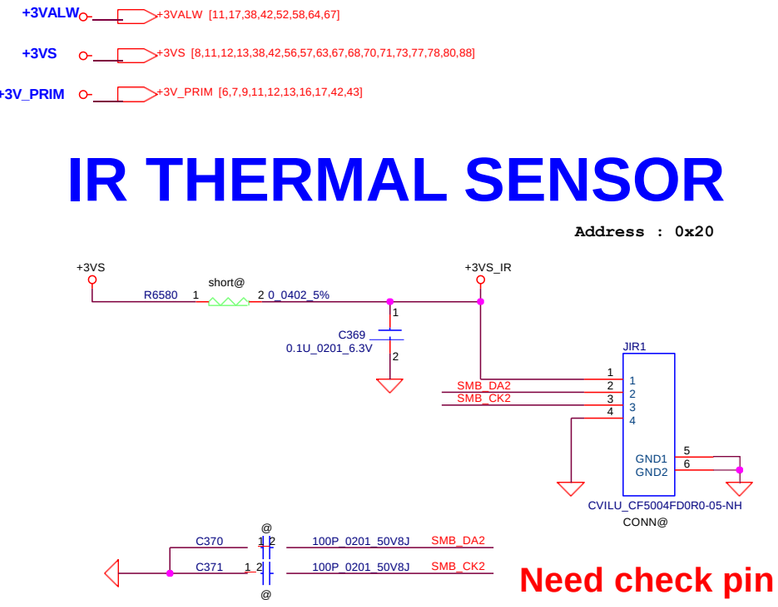
CPU THERMAL SENSOR



Screw Hole

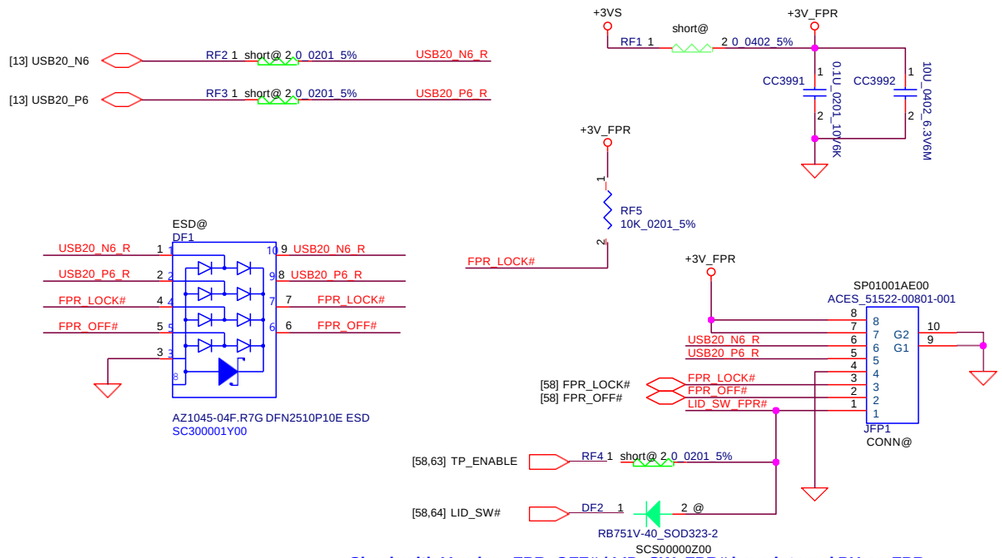


IR THERMAL SENSOR



Need check pin define

Finger Printer



Check with Vendor , FPR_OFF# / LID_SW_FPR# have internal PH on FPR

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: **TPM/Screw**

Document Number: LA-K261P

Rev: 0.3

Date: Friday, August 14, 2020

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ACCELEROMETER FOR G-sensor
ST Micro HP2DC

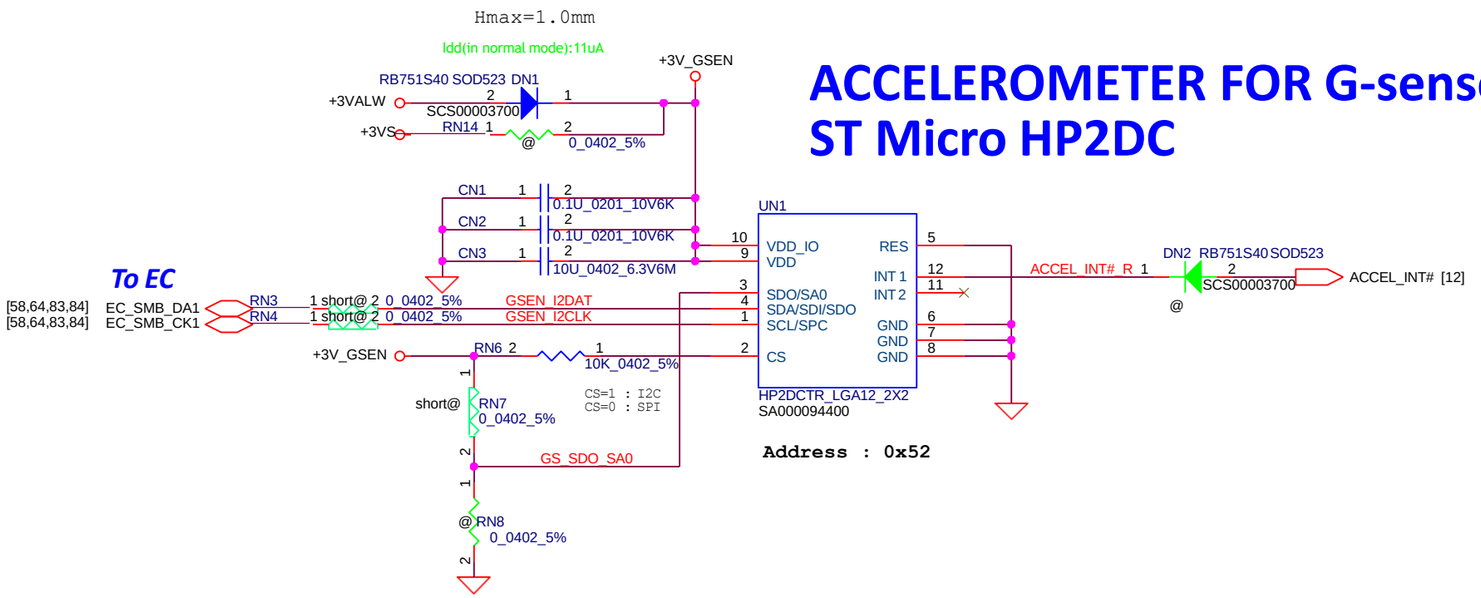
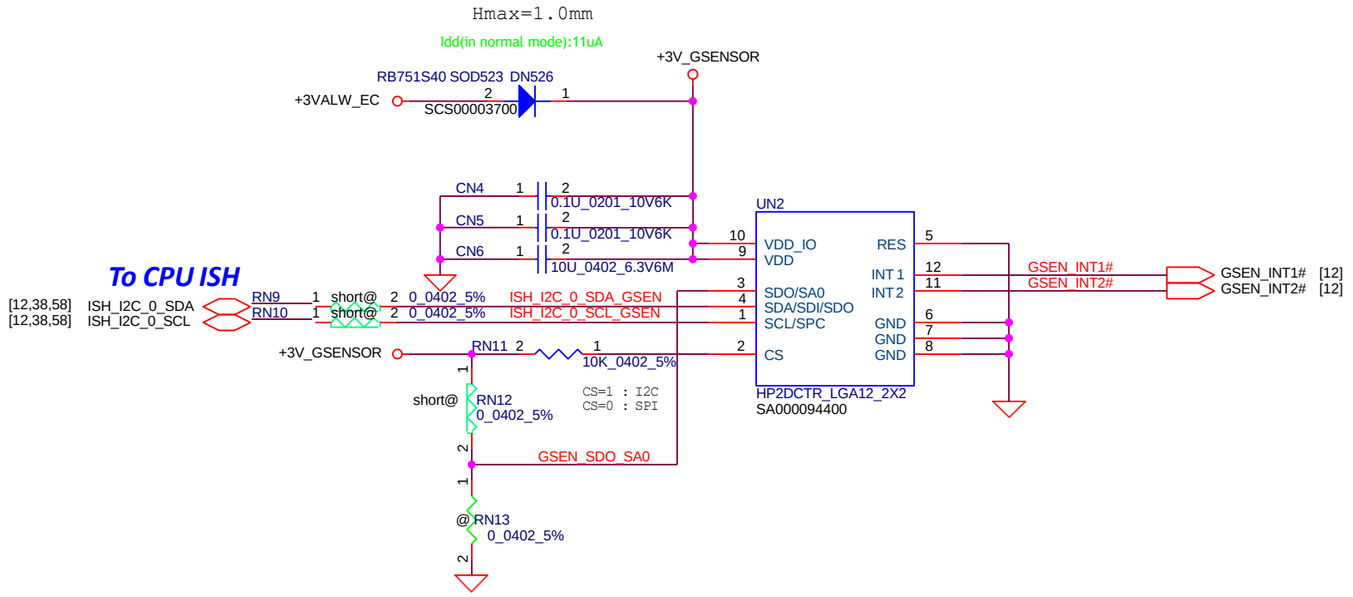


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

ACCELEROMETER
ST Micro HP2DC



Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

Title: HDD/ODD Conn

Size: Custom | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 67 of 100

[8,11,12,13,38,42,56,57,63,66,67,70,71,73,77,78,80,88] +3VS

+3VS

It inverted the PCIe lane polarity of pin41 and pin43 for PCIe/SATA auto switchable.

JSSD1

1	GND	3P3VAUX	2
3	GND	3P3VAUX	4
5	PETp3	NC	6
7	PETn3	NC	8
9	GND	DAS/DSS#	10
11	PERn3	3P3VAUX	12
13	PERp3	3P3VAUX	14
15	GND	3P3VAUX	16
17	PETp2	3P3VAUX	18
19	PETn2	NC	20
21	GND	NC	22
23	PERn2	NC	24
25	PERp2	NC	26
27	GND	NC	28
29	PETn1	NC	30
31	PETp1	NC	32
33	GND	NC	34
35	PERn1	NC	36
37	PERp1	DEVSLP	38
39	GND	NC	40
41	PETn0/SATA-B+	NC	42
43	PETp0/SATA-B-	NC	44
45	GND	NC	46
47	PERn0/SATA-A	NC	48
49	PERp0/SATA-A+	PERST#	50
51	GND	CLKREQ#	52
53	REFCLKN	PEWake#	54
55	REFCLKP	NC	56
57	GND	NC	58
67	NC	SUSCLK(32kHz)	68
69	PEDET	3P3VAUX	70
71	GND	3P3VAUX	72
73	GND	3P3VAUX	74
75	GND	GND	76
		GND	77

FOX_AS0BC26-S20BM-7H
CONN@

[13] PCIE_CRX_DTX_N9 / [13] PCIE_CRX_DTX_P9 — PCIE_CRX_DTX_N9 / PCIE_CRX_DTX_P9

[13] PCIE_CTX_DRX_N9 / [13] PCIE_CTX_DRX_P9 — CS1 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_N9; CSS3 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_P9

[13] PCIE_CRX_DTX_N10 / [13] PCIE_CRX_DTX_P10 — PCIE_CRX_DTX_N10 / PCIE_CRX_DTX_P10

[13] PCIE_CTX_DRX_N10 / [13] PCIE_CTX_DRX_P10 — CSS2 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_N10; CSS4 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_P10

[13] PCIE_CRX_DTX_N11 / [13] PCIE_CRX_DTX_P11 — PCIE_CRX_DTX_N11 / PCIE_CRX_DTX_P11

[13] PCIE_CTX_DRX_N11 / [13] PCIE_CTX_DRX_P11 — CSS6 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_N11; CSS7 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_P11

[13] PCIE_CRX_DTX_P12 / [13] PCIE_CRX_DTX_N12 — PCIE_CRX_DTX_P12 / PCIE_CRX_DTX_N12

[13] PCIE_CTX_DRX_N12 / [13] PCIE_CTX_DRX_P12 — CSS8 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_N12; CSS9 1 2 0.22U_0201_6.3V6M PCIE_CTX_C_DRX_P12

[11] CLK_PCIE_N3 / [11] CLK_PCIE_P3 — CLK_PCIE_N3 / CLK_PCIE_P3

+3VS_SSD

DEVSLP1 1 @ 2 RSS1 10K_0201_5%

CLKREQ_PCIE#3 CSS5 1 RF@ 2 10P_0201_25V8

DEVSLP1 — DEVSLP1 [13]

PLT_RST#_SSD 0_0201_5% 2 Rshort@ 1 RSS2 — PLT_RST# [11,42,52,58,66,70,80]

CLKREQ_PCIE#3 — CLKREQ_PCIE#3 [11]

PEDET: SATA=GND PCI-E=NC

12/25 SATA_GP2-->SATA_GP1

+3VS_SSD

RSS4 1 2 100K_0201_5%

RSS5 100K_0201_5% @

SSD_PDET

[13] SATA_GP1

RSS6 1 @ 2 0_0201_5%

NGFF_SSD_PEDET
H : SATA Interface
L : PCIe Interface

QS3
PJE138K 1N SOT-523-3
SB00001KM00

@EMI@
DS1
CK0402101V05_0402-2

+3VS — +3VS_SSD

JUMP@ JP4 1 2
JUMP_43X79

+3VS_SSD

CSS10 1 RF@ 2 68P_0201_50V8J

CSS11 1 RF@ 2 68P_0201_50V8J

CSS12 1 2 10U_0402_6.3V6M

CSS13 1 2 0.1U_0201_10V6K

CSS14 1 2 1U_0201_6.3V6M

CSS15 1 RF@ 2 100P_0201_50V8J

CSS16 1 @RF@ 2 1U_0201_6.3V6M

CSS17 1 @RF@ 2 1U_0201_6.3V6M

0604 RF add

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

Security Classification	Compal Secret Data		
Issued Date	2018/7/31	Deciphered Date	2018/12/31

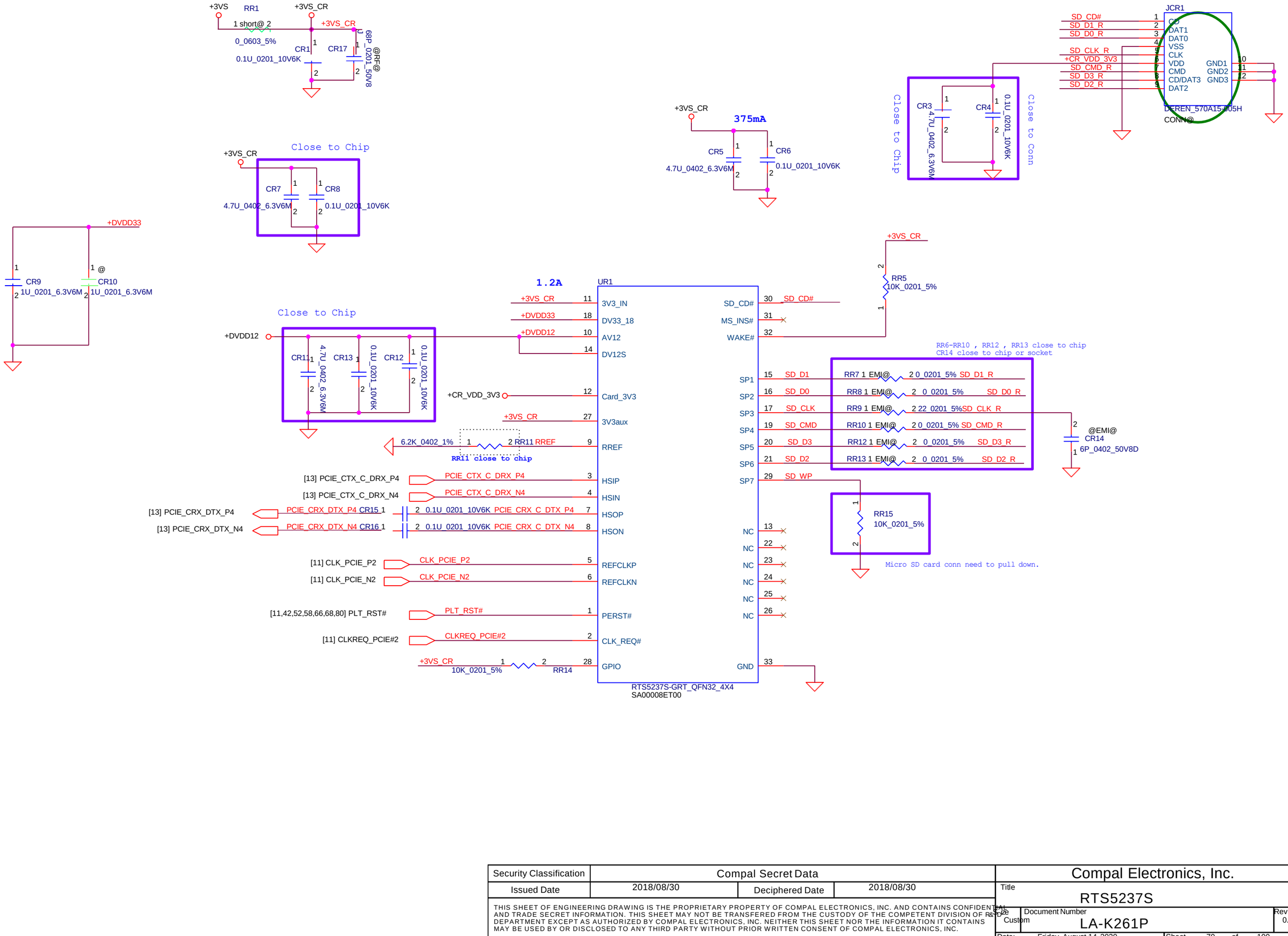
Compal Electronics, Inc.

Title: NGFF_M.2_SSD

Size: Custom | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 68 of 100

Card Reader Conn



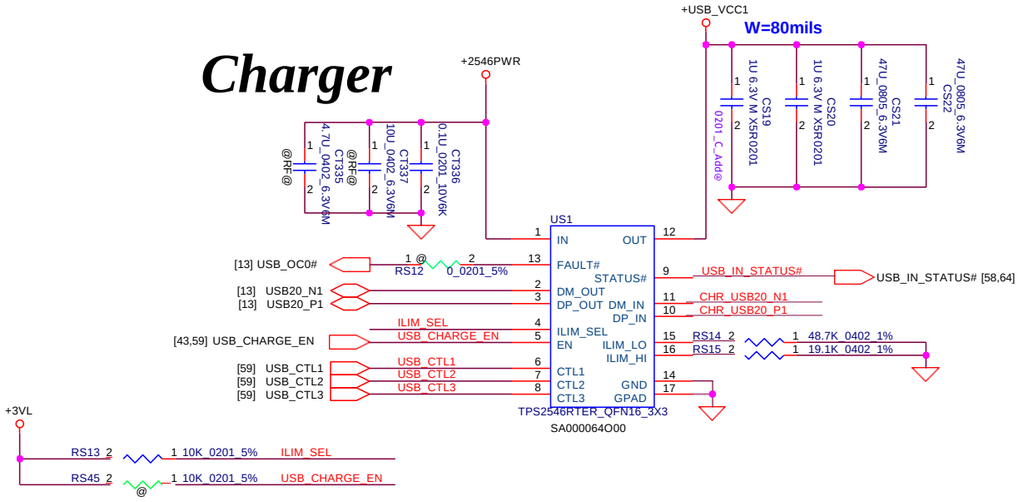
Compal Electronics, Inc.

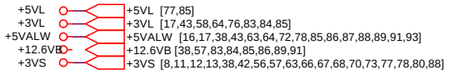
Title: RTS5237S

Size: Custom | Document Number: LA-K261P | Rev: 0.3

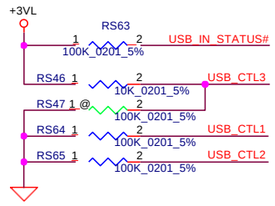
Date: Friday, August 14, 2020 | Sheet 70 of 100

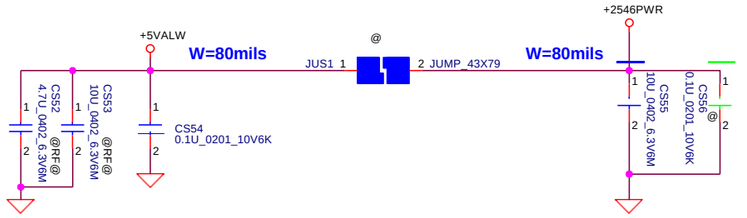
Charger

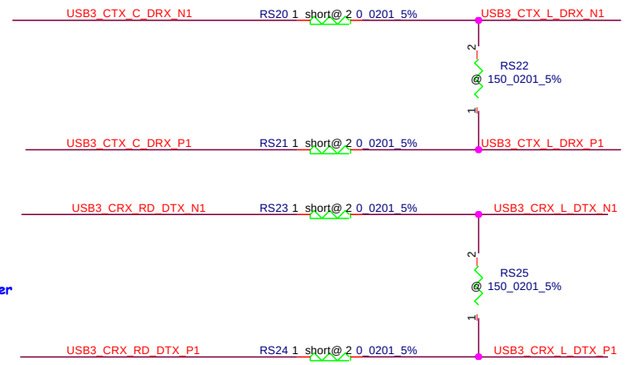


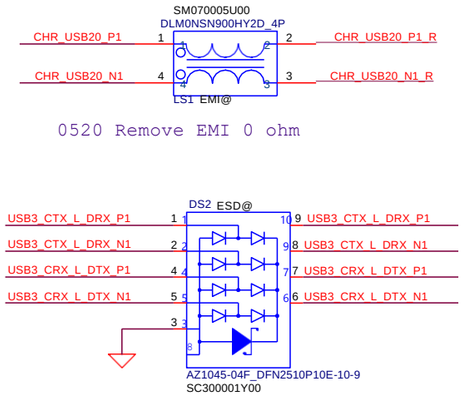


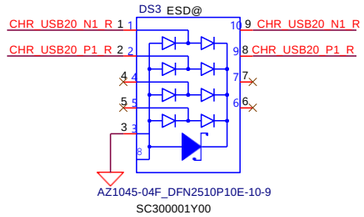
2013.01.07 Change MOS gate from +VL to B+ to preventleakage.
2014-10-13:Change Correct Power Net Name B+ => +19VB
2014-10-20: Change USB_IN_STATUS# PU to +3VL(same power level as EC)
2014-10-21: Change from single load switch back to MOS.
Load Swtich have body diode will leakage from out to in.



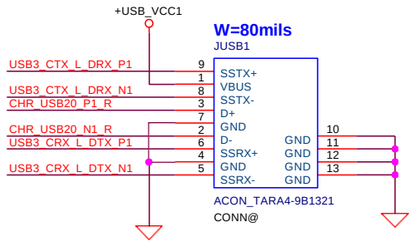


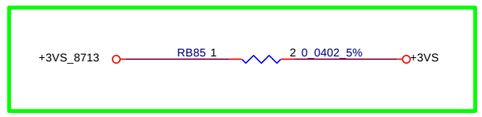




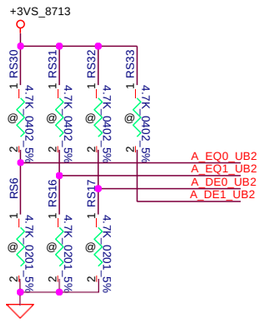


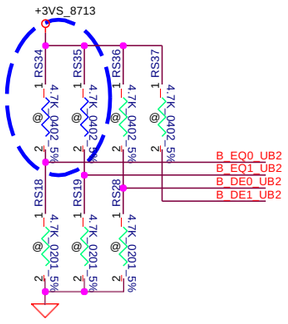
USB Charger port

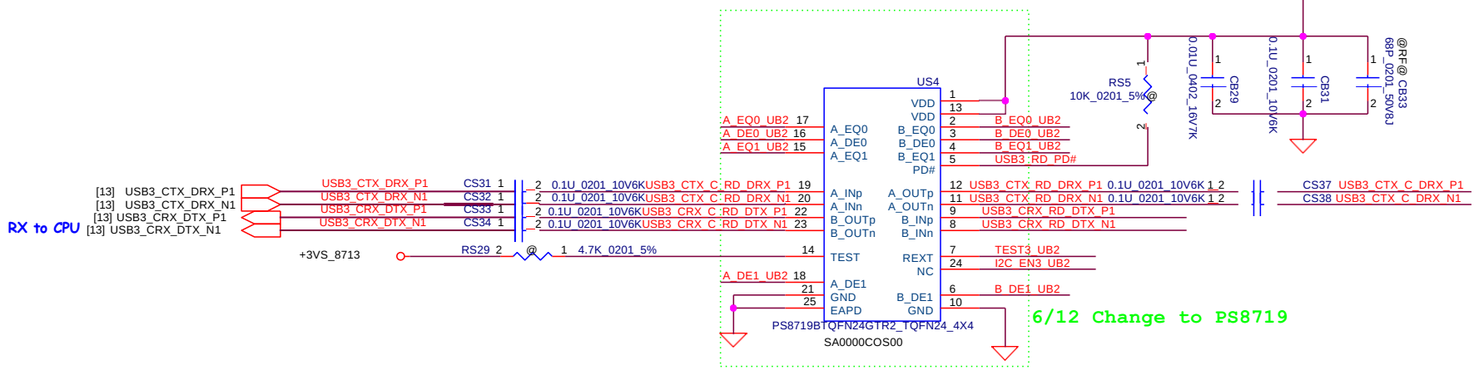


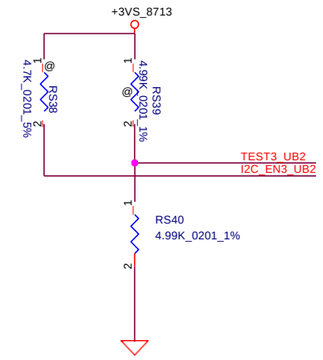


USB3 Gen1 Redriver









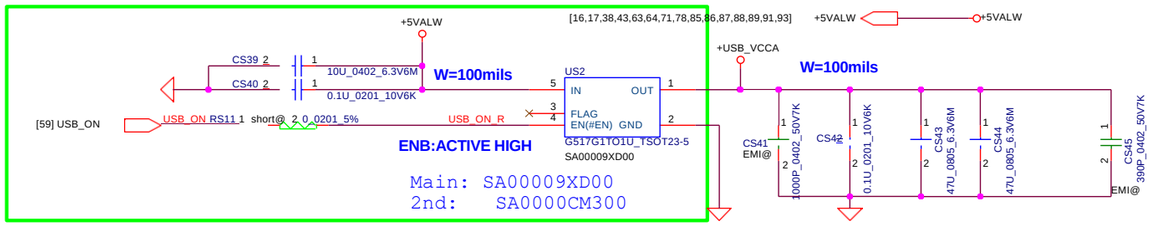
Security Classification	Compal Secret Data		
Issued Date	2019/04/02	Deciphered Date	2021/04/03

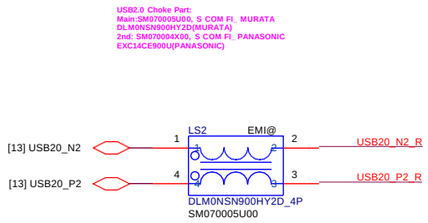
Compal Electronics, Inc.

Title: USB Charger

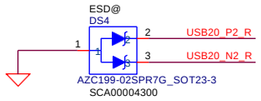
Size: Custom | Document Number: LA-K261P | Rev: 0.3

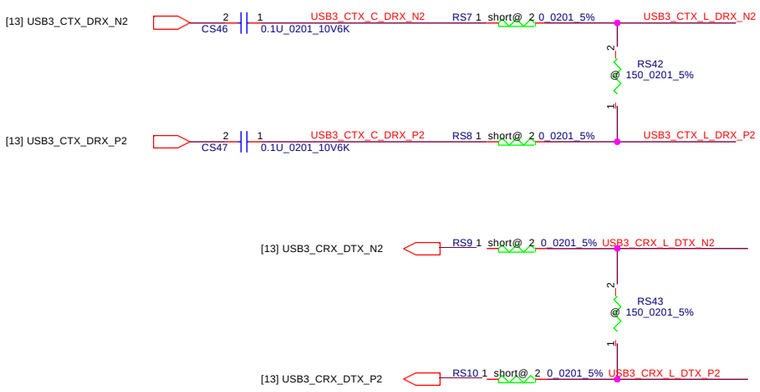
Date: Friday, August 14, 2020 | Sheet 71 of 100

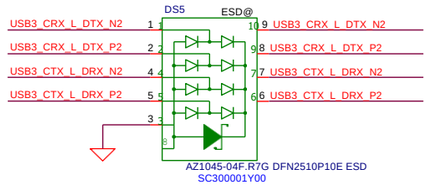


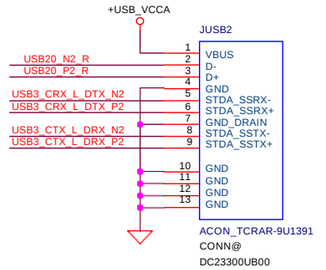


0520 Remove EMI 0 ohm









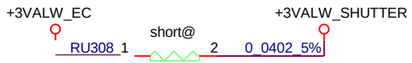
Security Classification	Compal Secret Data		
Issued Date	2018/01/08	Deciphered Date	2020/01/08

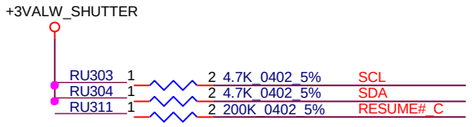
Compal Electronics, Inc.

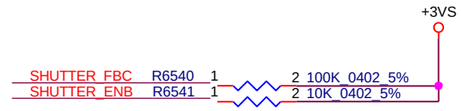
Title: USB 3.0/2.0 conn

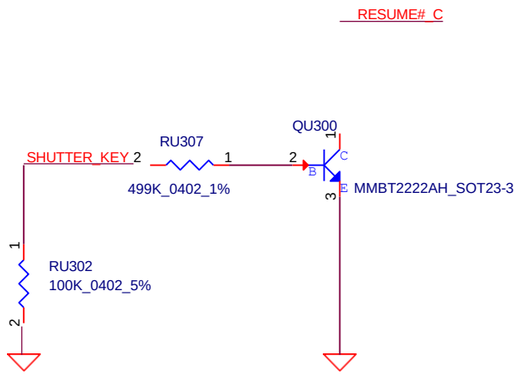
Size: Custom | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 72 of 100





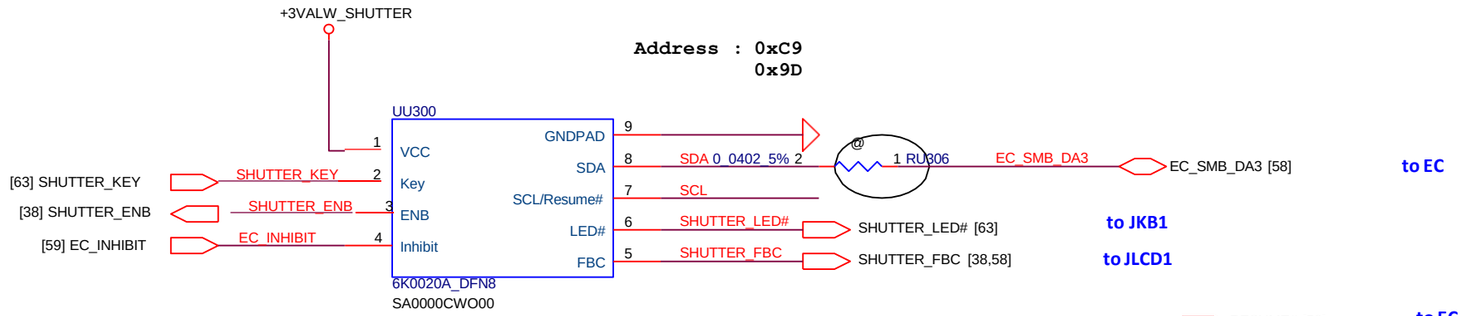




to JKB1

to JEDP1

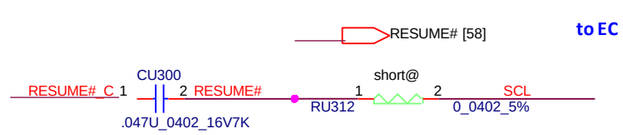
to EC



to EC

to JKB1

to JLCD1



to EC

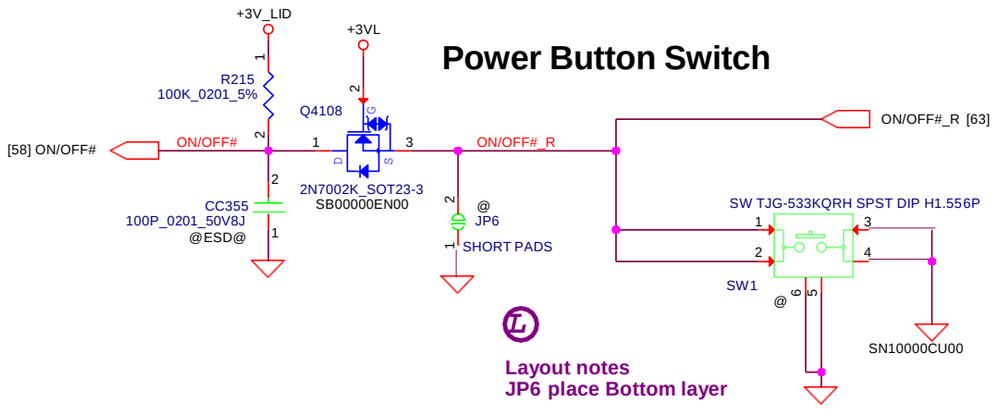
Compal Electronics, Inc.

Title: Shutter Camera_6K0020

Size: Custom | Document Number: LA-H465P | Rev: 0.1

Date: Friday, August 14, 2020 | Sheet 73 of 100

Power Button Switch



Layout notes
JP6 place Bottom layer

[17,43,58,64,71,83,84,85]	+3VL		+3VL
[16,17,38,43,63,64,71,72,78,85,86,87,88,89,91,93]	+5VALW		+5VALW
[8,11,12,13,38,42,56,57,63,66,67,68,70,71,73,77,78,80,88]	+3VS		+3VS
[17,58,64,83]	+3V_LID		+3V_LID
[58,64]	+3V_SMBUS		+3V_SMBUS

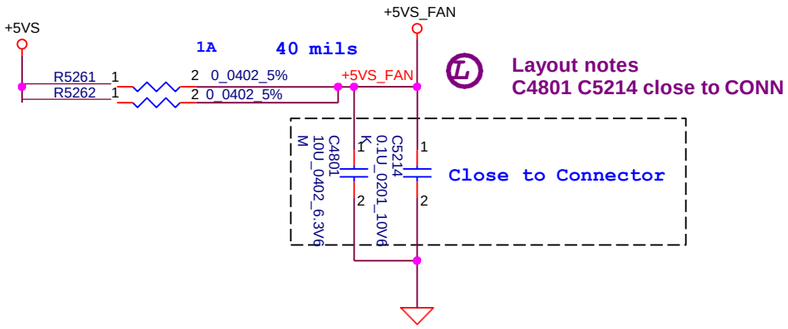
Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

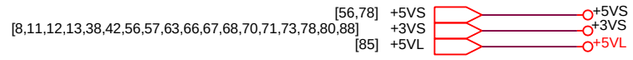
Compal Electronics, Inc.

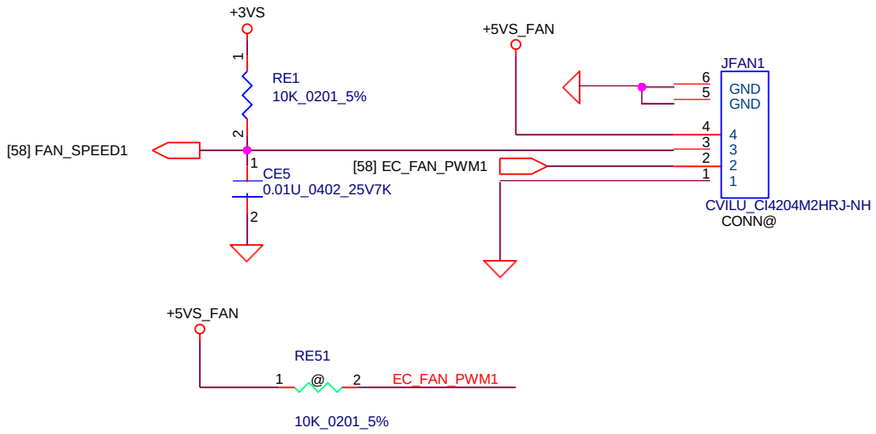
Title: IO CON

Size: Custom | Document Number: LA-K261P | Rev: 0.3

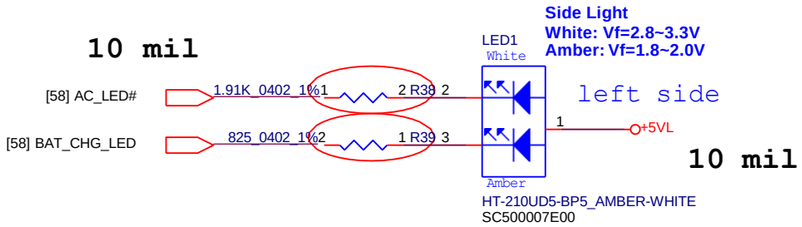
Date: Friday, August 14, 2020 | Sheet 76 of 100







Charger LED



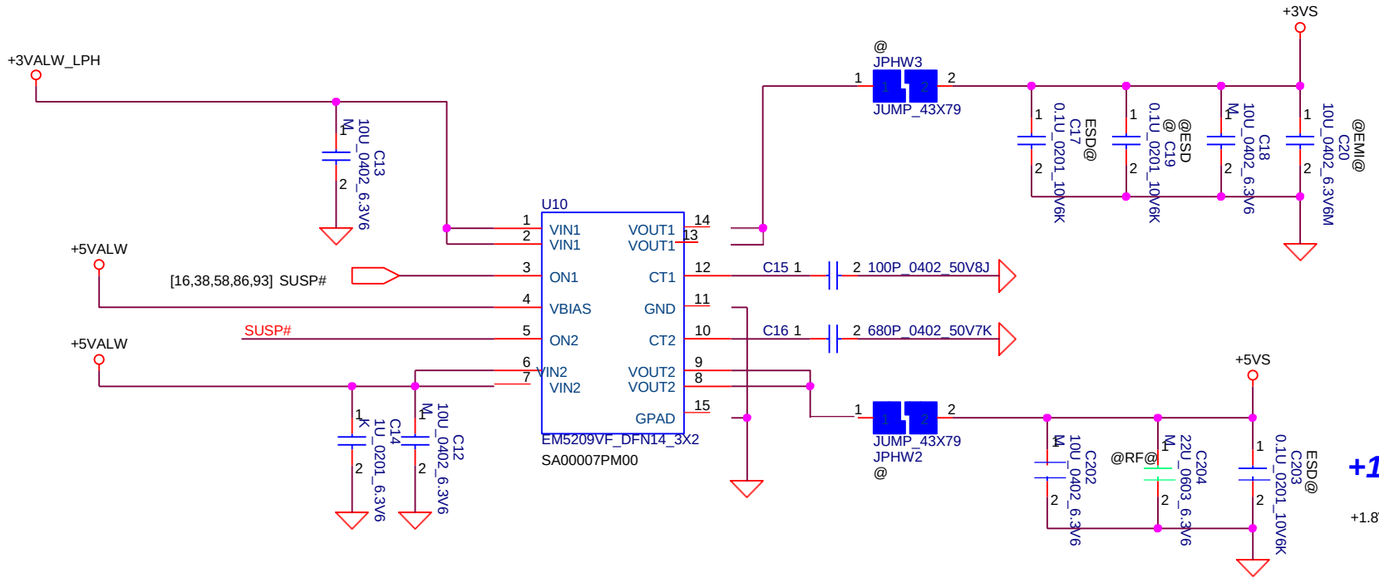
Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

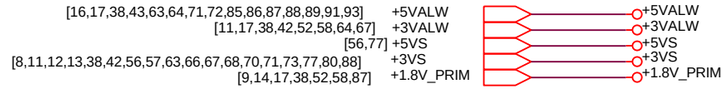
Compal Electronics, Inc.

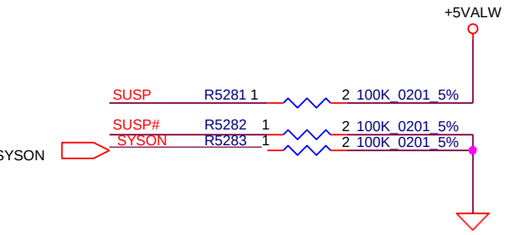
Title: FAN

Size: Custom | Document Number: LA-K261P | Rev: 0.3

Date: Friday, August 14, 2020 | Sheet 77 of 100

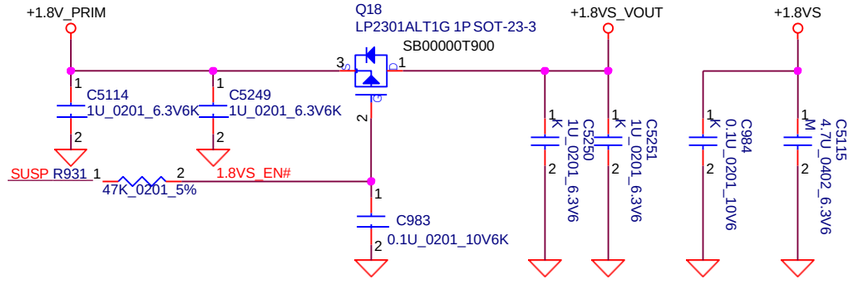




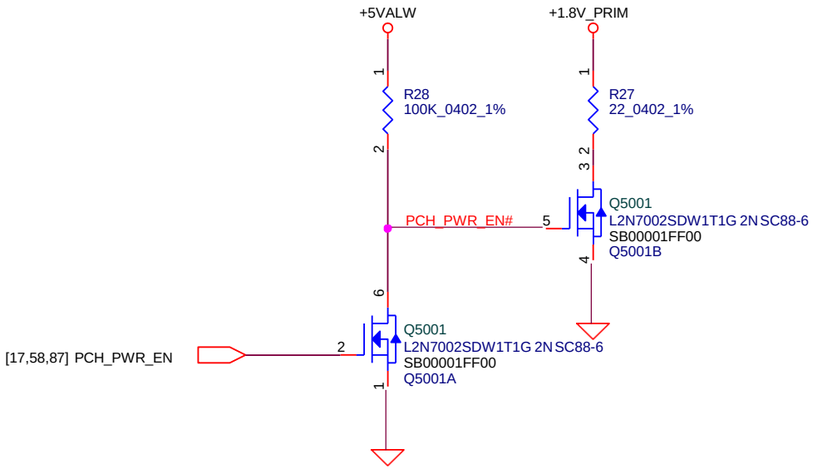


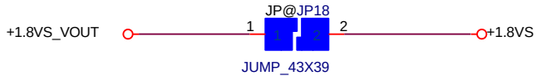
+1.8V_PRIM TO +1.8VS

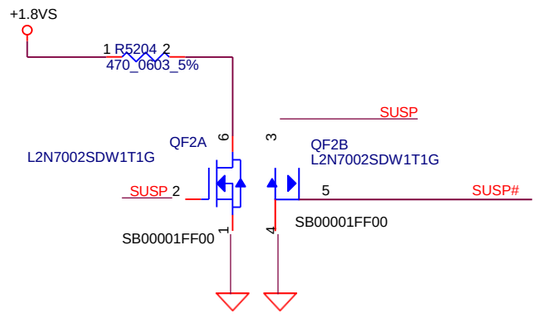
I (Max) : 0.2 A(Codec)
RDS(max) : 150 mohm
V drop : 0.03V



For +1.8V_PRIM Discharge







Add +1.8VS power down

Security Classification	Compal Secret Data		
Issued Date	2018/05/17	Deciphered Date	2021/05/17

Compal Electronics, Inc.

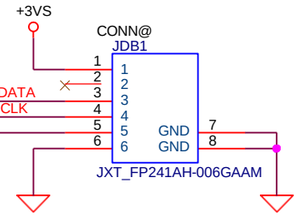
Title: DC Interface

Size	Document Number	Rev
Custom	LA-K261P	0.3

Date: Friday, August 14, 2020 | Sheet 78 of 100

12/25 EC_TX-->E51TXD_P80DATA
12/25 EC_RX-->E51RXD_P80CLK

[58] E51TXD_P80DATA
[58] E51RXD_P80CLK
[11,42,52,58,66,68,70] PLT_RST#



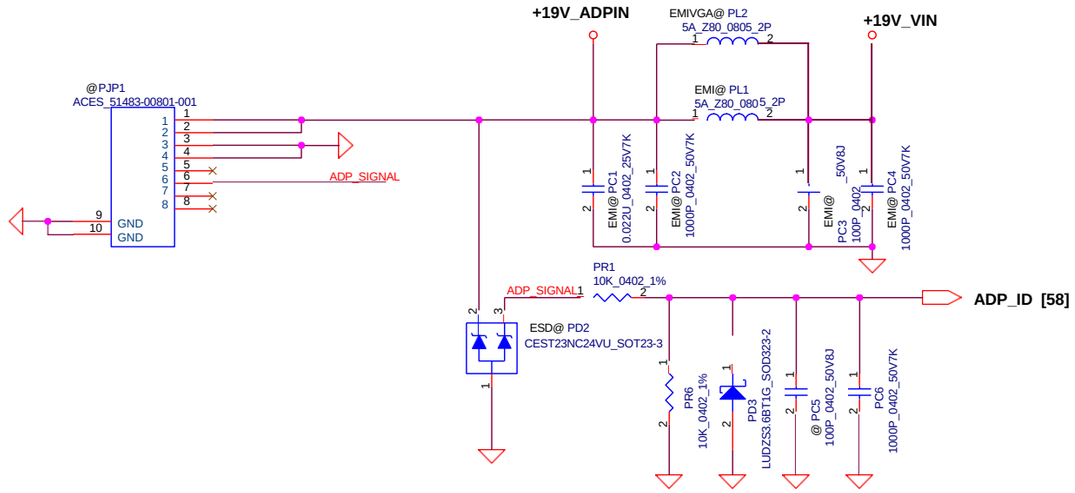
Security Classification	Compal Secret Data		
Issued Date	2018/01/08	Deciphered Date	2020/01/08

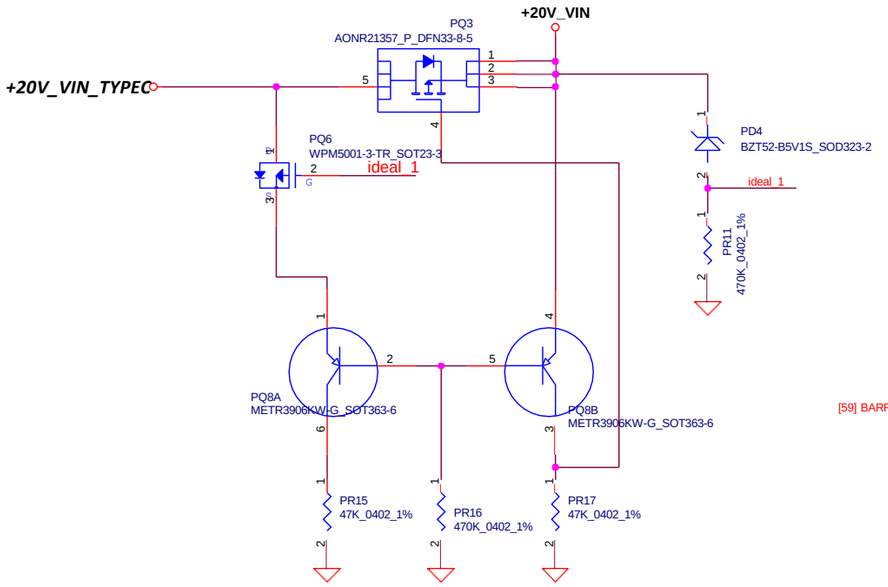
Compal Electronics, Inc.

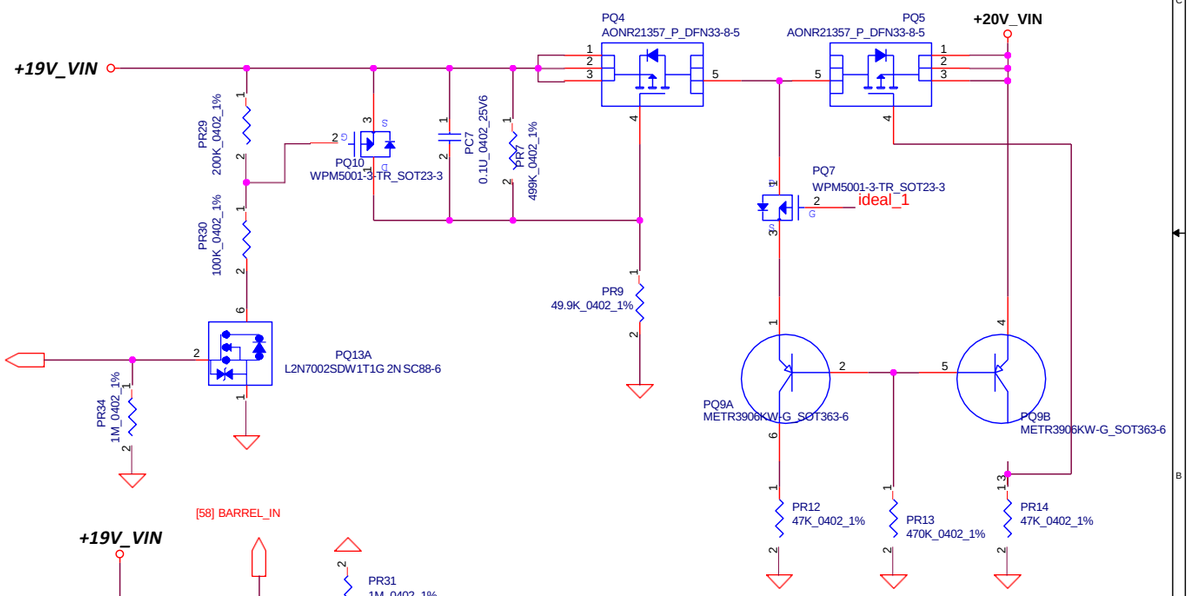
Title: HW Reserve

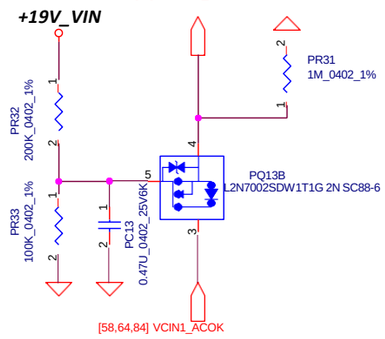
Size: Custom | Document Number: LA-K261P | Rev: 0.3

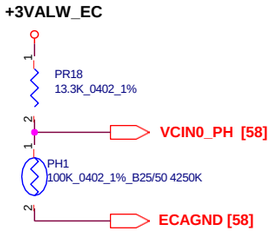
Date: Friday, August 14, 2020 | Sheet 80 of 100

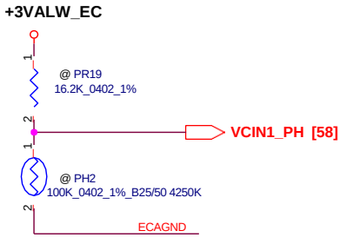












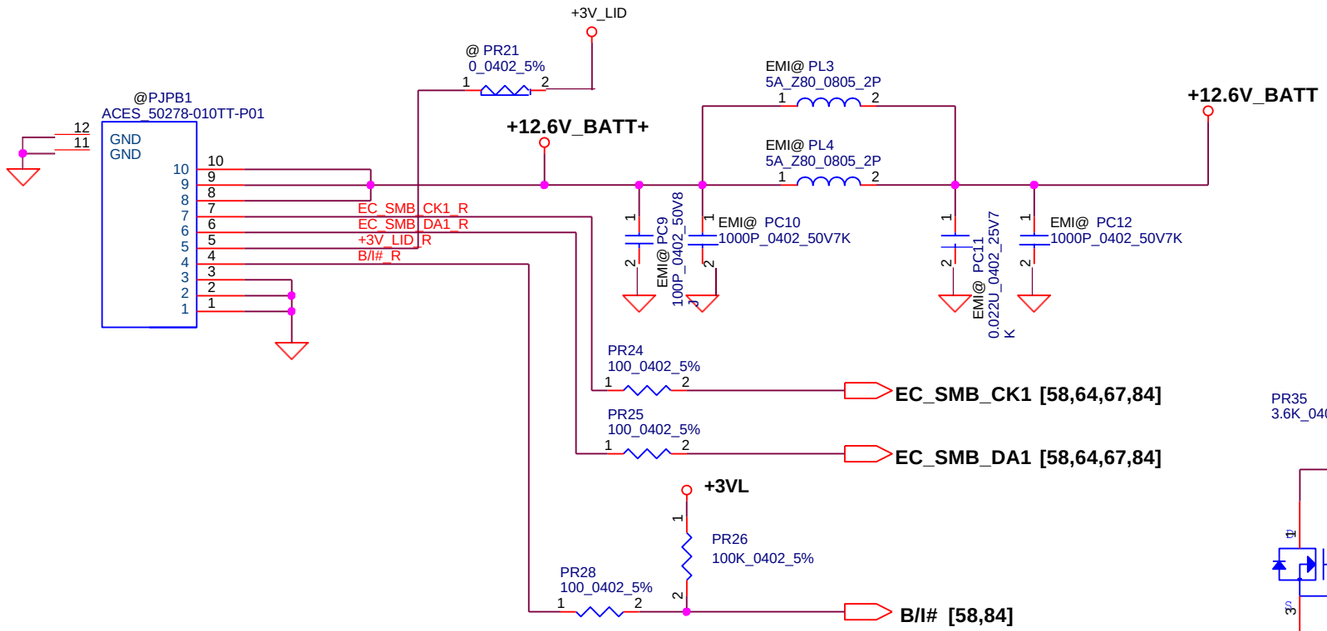
Security Classification	Compal Secret Data		
Issued Date	2019/06/20	Deciphered Date	2021/09/30

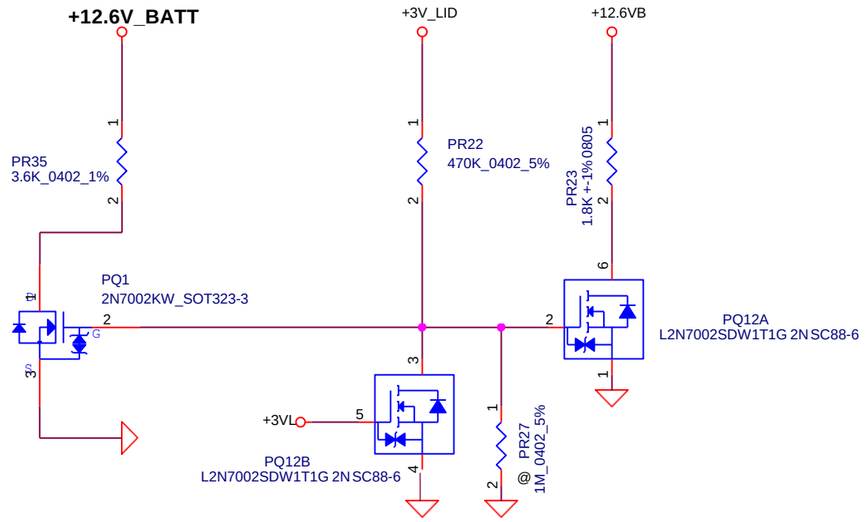
Compal Electronics, Inc.

Title: ***DC Conn***

Size: Document Number: **LAH** Rev: v0.1

Date: Friday, August 14, 2020 Sheet 82 of 99





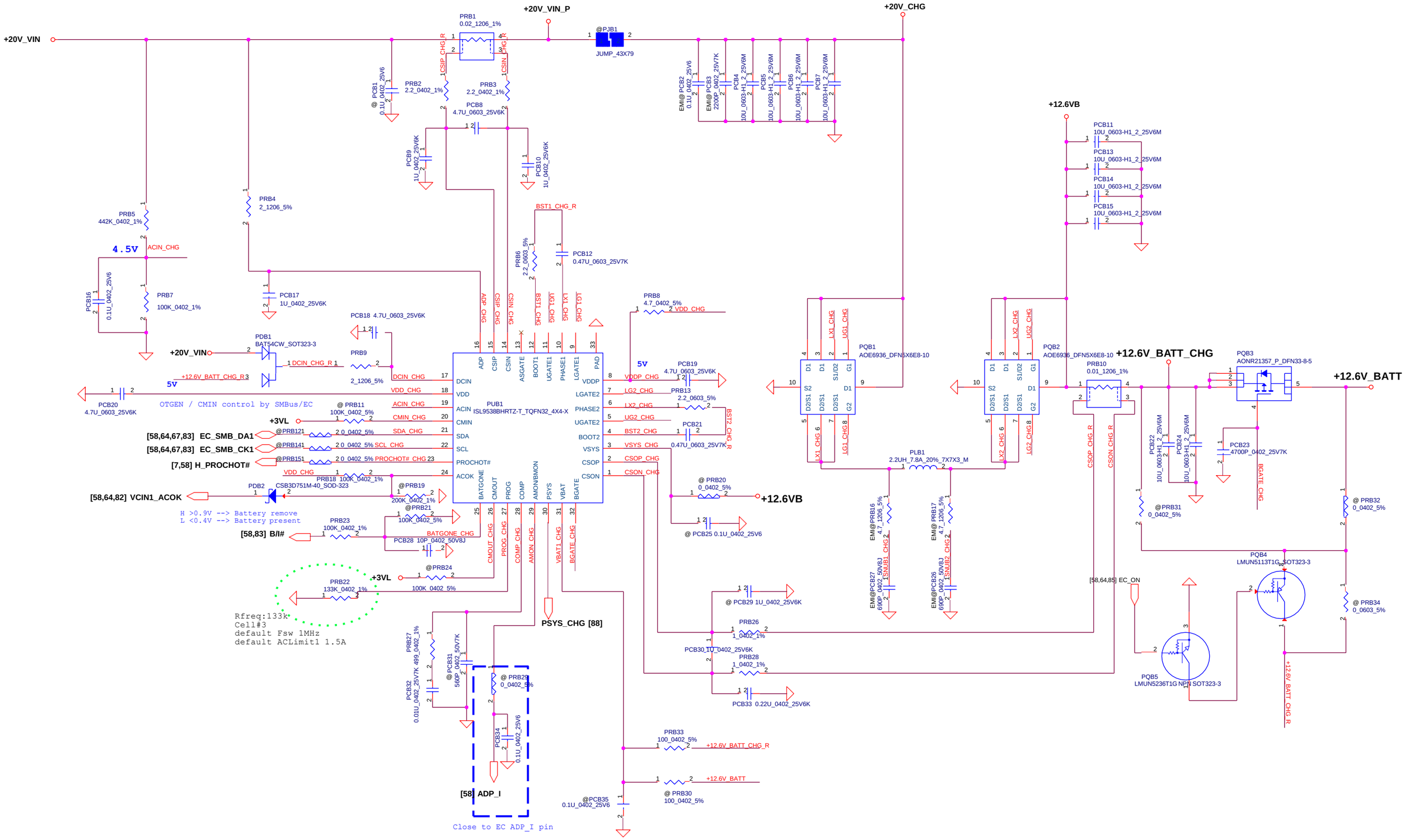
Security Classification	Compal Secret Data		
Issued Date	2019/07/17	Deciphered Date	2019/07/17

Compal Electronics, Inc.

Title: ***BATT Conn***

Size	Document Number	Rev
	LA-J471PR01	V0.1

Date: Friday, August 14, 2020 Sheet 83 of 99



$V_{AMON}=18x(V_{CSIP}-V_{CSIN})$; $V_{BMON}=18x(V_{CSON}-V_{CSOP})$

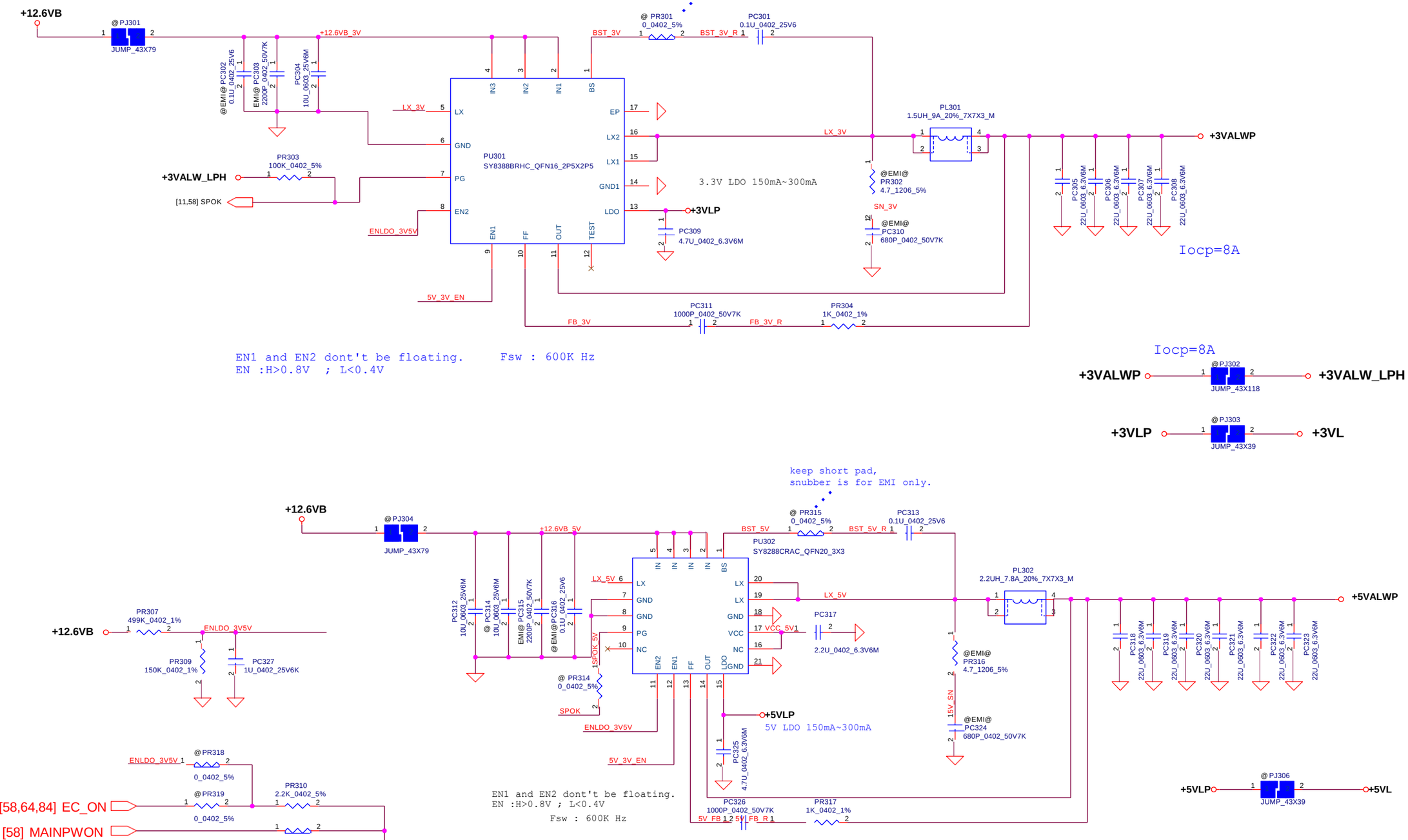
Security Classification	Compal Secret Data		
Issued Date	2019/06/20	Deciphered Date	2021/09/30

Compal Electronics, Inc.

Title: *CHARGER*

Size: Custom | Document Number: LAH | Rev: v0.1

Date: | Sheet 84 of 99



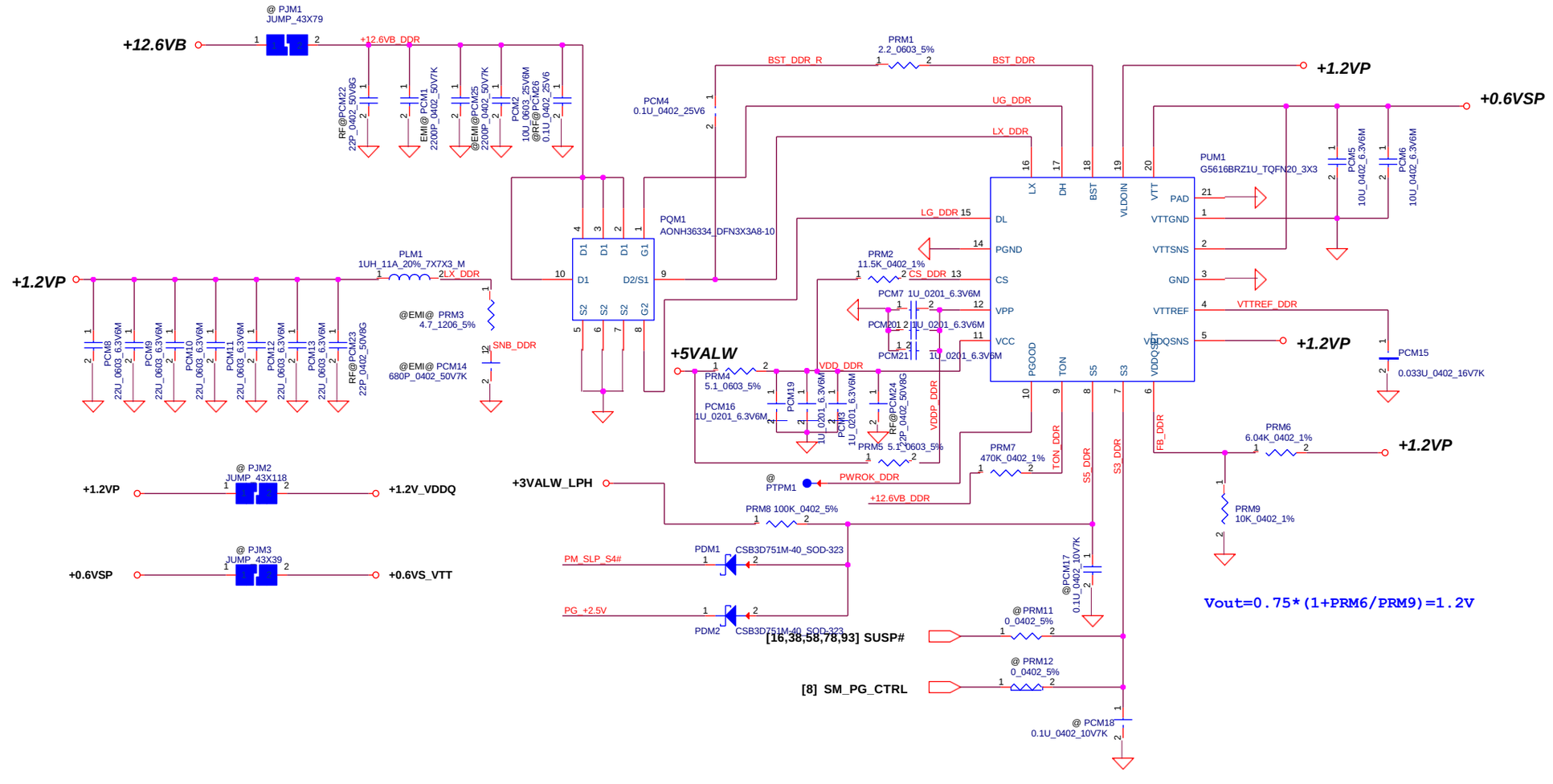
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size	Document Number	Rev
Custom	LAH323P	v0.3

Date: Friday, August 14, 2020 Sheet 85 of 99



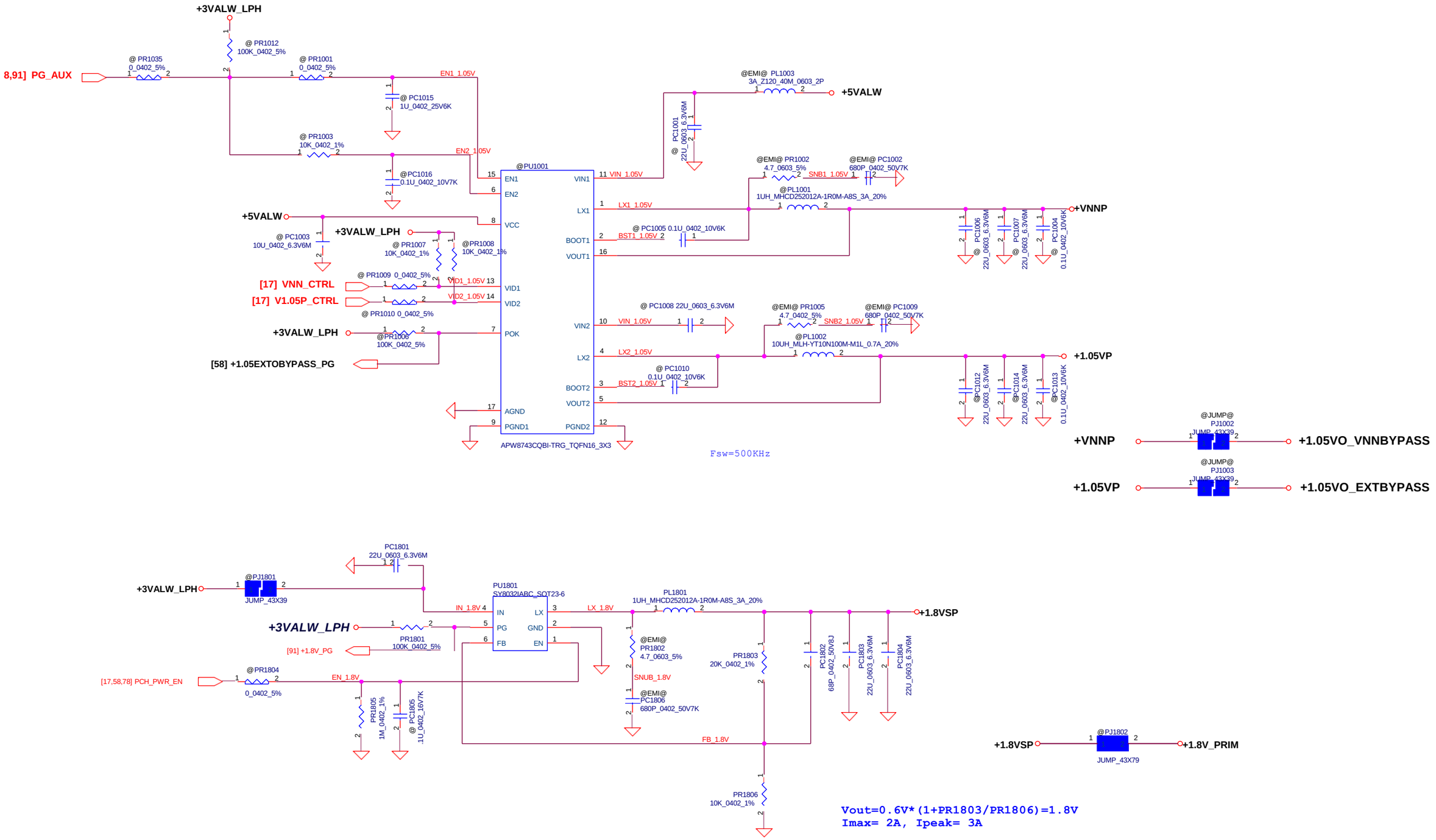
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: **1.2VP/0.6VSP/2.5VP**

Size: Custom | Document Number | Rev: 0.1

Date: Friday, August 14, 2020 | Sheet 86 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: 1.05V_EXTBYPASS/1.8V_PRIM

Size: C | Document Number | Rev: 0.1

Date: Friday, August 14, 2020 | Sheet 87 of 100

RT3613EEGQW-02 is not MP part

Pull High in HW site.

High: > 0.7V
Low: < 0.3V

VR_HOT# 100 degreeC
ALERT# 97 degreeC

remote sense in HW site.

31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable
Low:(0V): disable
this pin can dynamic change state.

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

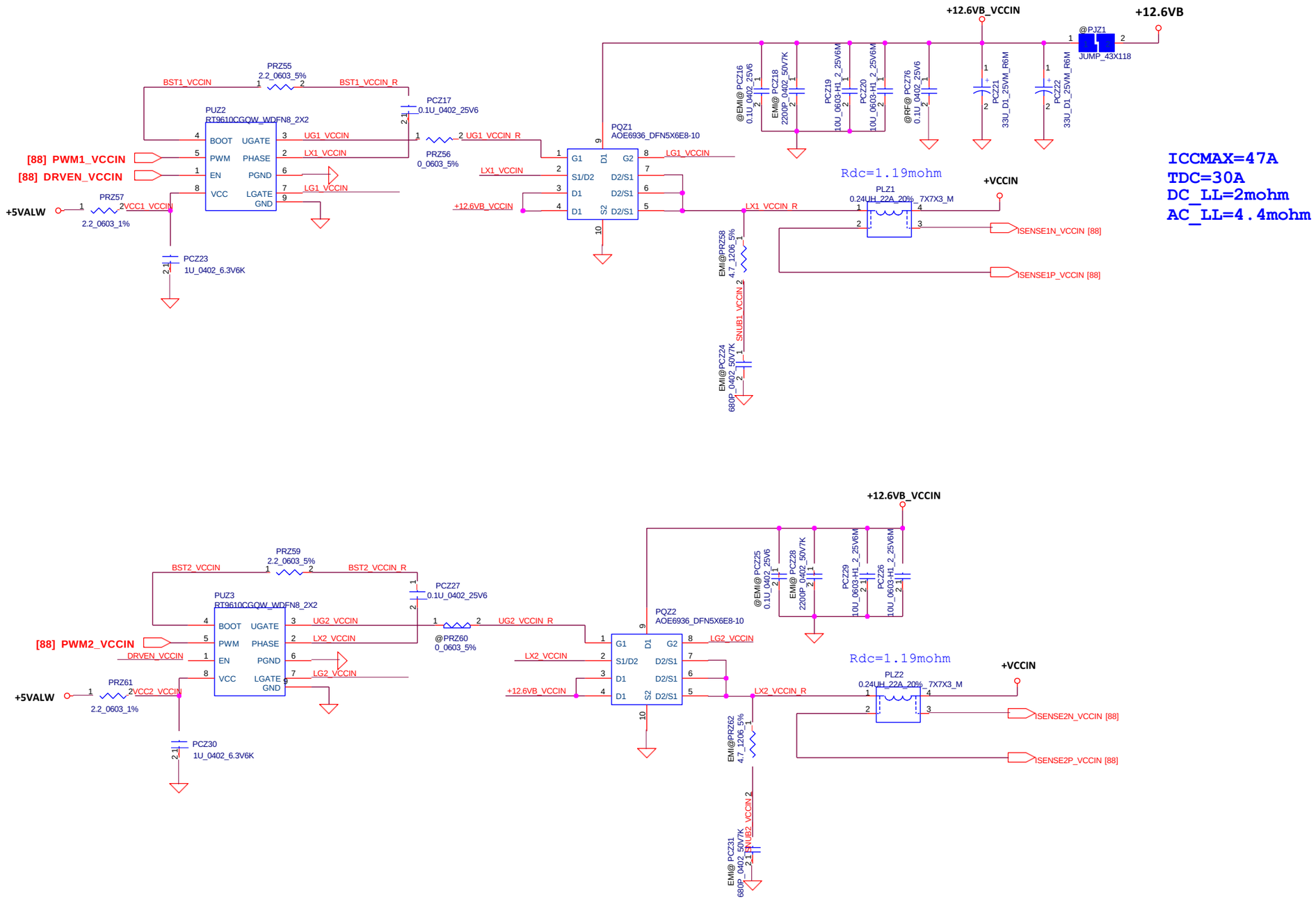
Title: VCORE

Size: D | Document Number: 2019OPP ICL | Rev: 0.1

Date: Friday, August 14, 2020 | Sheet 88 of 100

AOE6936

	Q1	Q2
I D (at V GS =10V)	55A	85A
R DS(ON) (at V GS =10V)	<5m ohm	<2m ohm
R DS(ON) (at V GS =4.5V)	<8m ohm	<3m ohm



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *VCORE_SW*

Size: A | Document Number: **2019OPP ICL** | Rev: 0.1

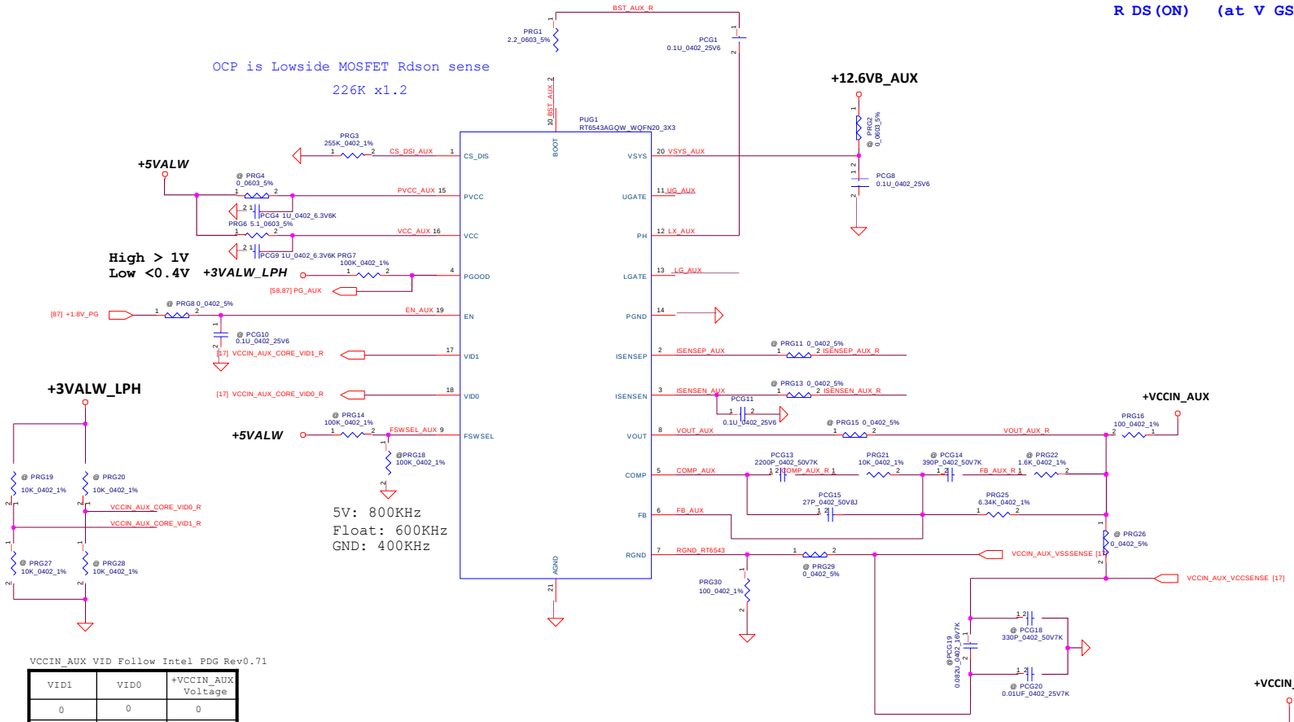
Date: Friday, August 14, 2020 | Sheet 89 of 100

AON6380
R DS(ON) (at V GS =10V) < 6.8mohm
R DS(ON) (at V GS =4.5V) < 10.5mohm

AON6314
R DS(ON) (at V GS =10V) < 2.8mohm
R DS(ON) (at V GS =4.5V) < 3.5mohm

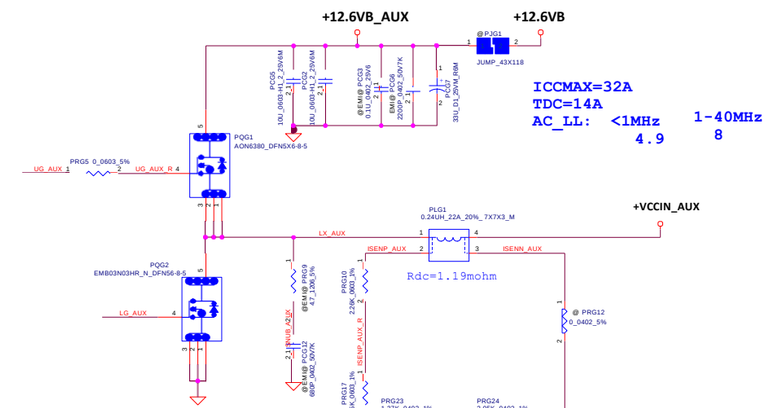
OCP is Lowside MOSFET Rdson sense

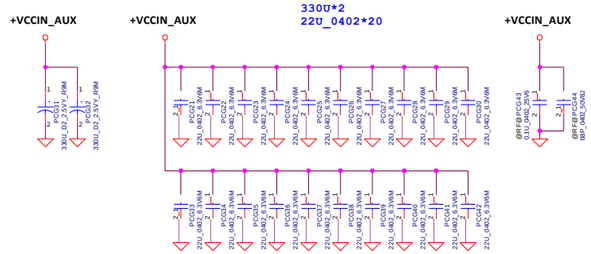
226K x1.2



VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title VCCINAUX
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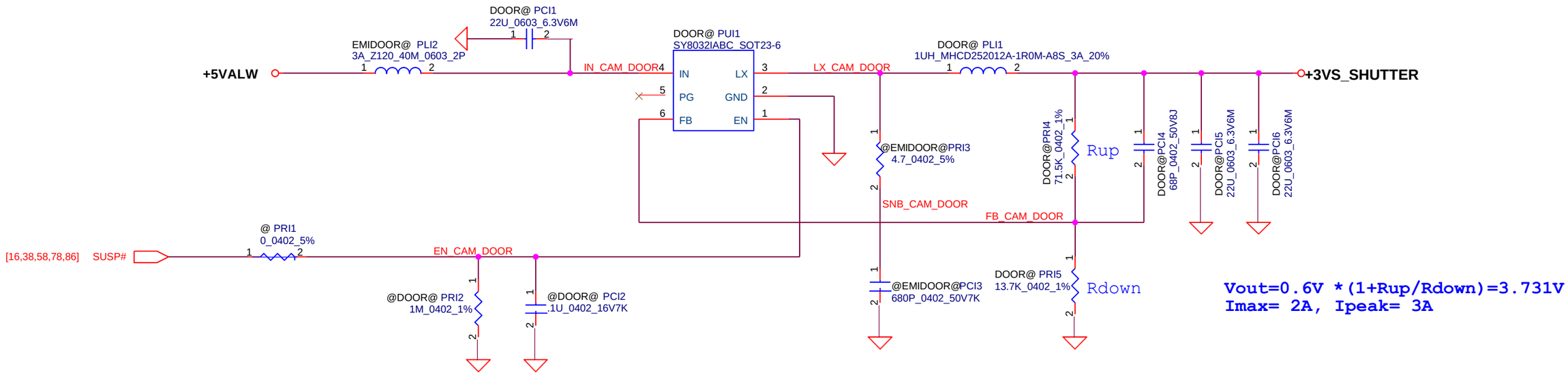
			Date: Friday, August 14, 2020 Sheet 91 of 100



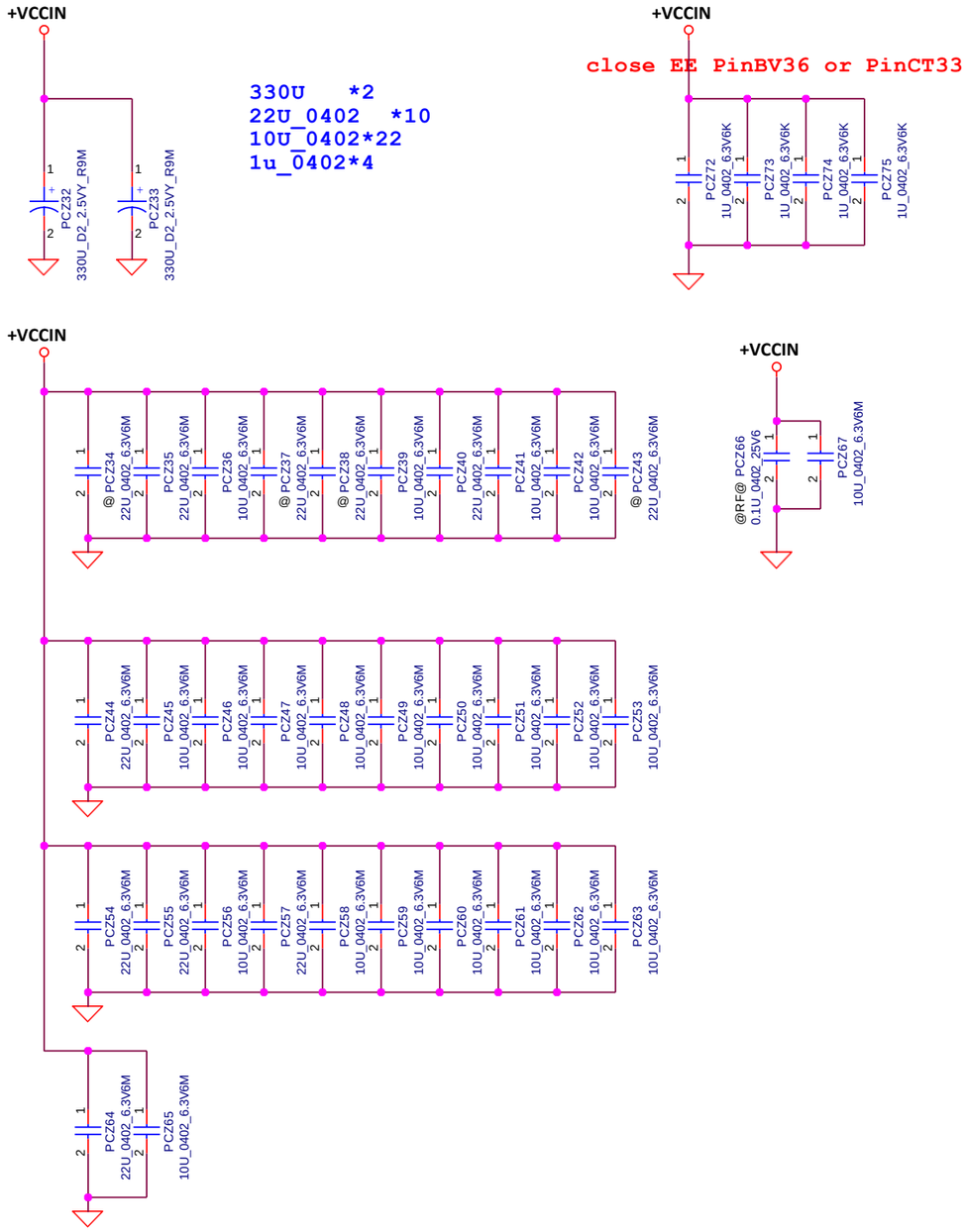
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title

Size | Document Number | Rev 0.1

Date: Friday, August 14, 2020 | Sheet 93 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: ***VCORE_DECOUPLING***

Size: D | Document Number: **2019OPP ICL** | Rev: 0.1

Date: Friday, August 14, 2020 | Sheet 90 of 100

Version change list (P.I.R. List)

Item	Page#	Date	Title	Issue Description	Request Owner	Solution Description	Rev.
1	P84	2020/03/27	Change to	Down size	PWR	PCB26 & PCB27 from SE024681J80 to SE00000PS00 PCB30 from SE000006900 to SE000010V00 (down size) PCB17 from SE000009RY0 to SE000010V00 (down size)	SI
2	P87 P86 P93	2020/03/27	Change to	X1 Code	PWR	PL1001 PL1801 PL2501 PLI1 from SH00001KJ00 to SH00001NF00	SI
3	P88	2020/04/01	Change to	psys Reserve	PWR	add PRZ63 reserve	SI
4 5	P88	2020/04/07	Change to	Charger Ipsys	PWR	PRZ49 from (SD034162280) 16.2K 0402to (SD034931180)9.31K 0402	SI
6	P87	2020/04/06	Change to	VID pull high change to +3VALW_LPH	PWR	PR1007 PR1008 VID pull high change to +3VALW_LPH	SI
7	P88	2020/04/13	Change to	CPU Transient	PWR	PRZ52 = from 21.5K +-1% 0402 (SD034215280) to 19.6K +-1% 0402kohm (SD000003580) PRZ19 = from 12.4K +-1% 0402 (SD00000AJ80) to 78.7K +-1% 0402 (SD034787280), PRZ11 =from 12.1K +-1% 0402 (SD034121280) to 8.87K +-1% 0402 SD034887180, PRZ29 = from19.6K +-1% 0402 (SD000003580) to 10K +-1% 0402(SD034100280) PRZ30 = from 24.9K +-1% 0402 (SD034249280) to 110K +-1% 0402 (SD034110380)	SI
8 9	P90	2020/04/13	Change to	CPU Transient	PWR	PCZ44, PCZ54, PCZ57, PCZ55, PCZ64 from 10U 0402 (SE00000UD00) TO 22U 0402 (SE00001 4600) PCZ39, PCZ36, PCZ41, PCZ42, PCZ67, to 10U 0402 (SE00000UD00) PCZ38, PCZ37, PC34 unPOP	SI
10	P88	2020/04/13	Change to	IMON	PWR	PRZ52 from (SD000003580) 19.6K 0402 to (SD034210280)21K 0402	SI
11	P88	2020/05/18	Change to	Psys POP	PWR	PRZ63 0_0402_5% pop	PV
12 13 14	P85 P87 P88 P91 P93	2020/05/19	Change to	short pad	PWR	PR1804 PR318 PRG15 PRG26 PRG29 PRG8 PRI1 PRZ39 PRZ41 PRZ44 PRZ45 PRZ50 0 0402 ohm to Short pad	PV
15	P84	2020/06/01	Change to	Acoustics Change low noise	PWR	PCB13 PCB15 PCB24 change to SE00000X210	PV
16	P91	2020/06/03	Change to	AUX LL	PWR	PCG16, PHG1,PRG12 POP PRG24 Change to 2.05K_0402 PRG23 Change to 1.37K 0402 PRG11 PRG13 Change to 0 ohm	PV
17	P84	2020/06/09	Change to	Charger Fsw 1MHz	PWR	PRB22 Change to SD034133380 (133K +-1% 0402)	PV
	P84	2020/06/10	Change to	Charger OCP	PWR	PQB2 Change to AOE6936	PV
	P91	2020/06/12	Change to	AUX LL	PWR	PRG17 Change to SD014365180 S RES 1/10W 3.65K +-1% 0603 PRG10 Change to SD014226180 S RES 1/10W 2.26K +-1% 0603	PV
	P84 P86 P87 P89 P91	2020/07/22	Change to	short pad	PWR	PRG11,PRG12,PRG13,PR1001,PR1009,PR1010,PR1035,PRB15,PRM12. 0_0402 ohm to Short pad PRZ60 0_0603 ohm to Short pad	MV
	P87	2020/08/07	Change to	VNNBYPASS and 1.05VBYPASS UNPOP	PWR	VNNBYPASS and 1.05VBYPASS UNPOP	MV

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