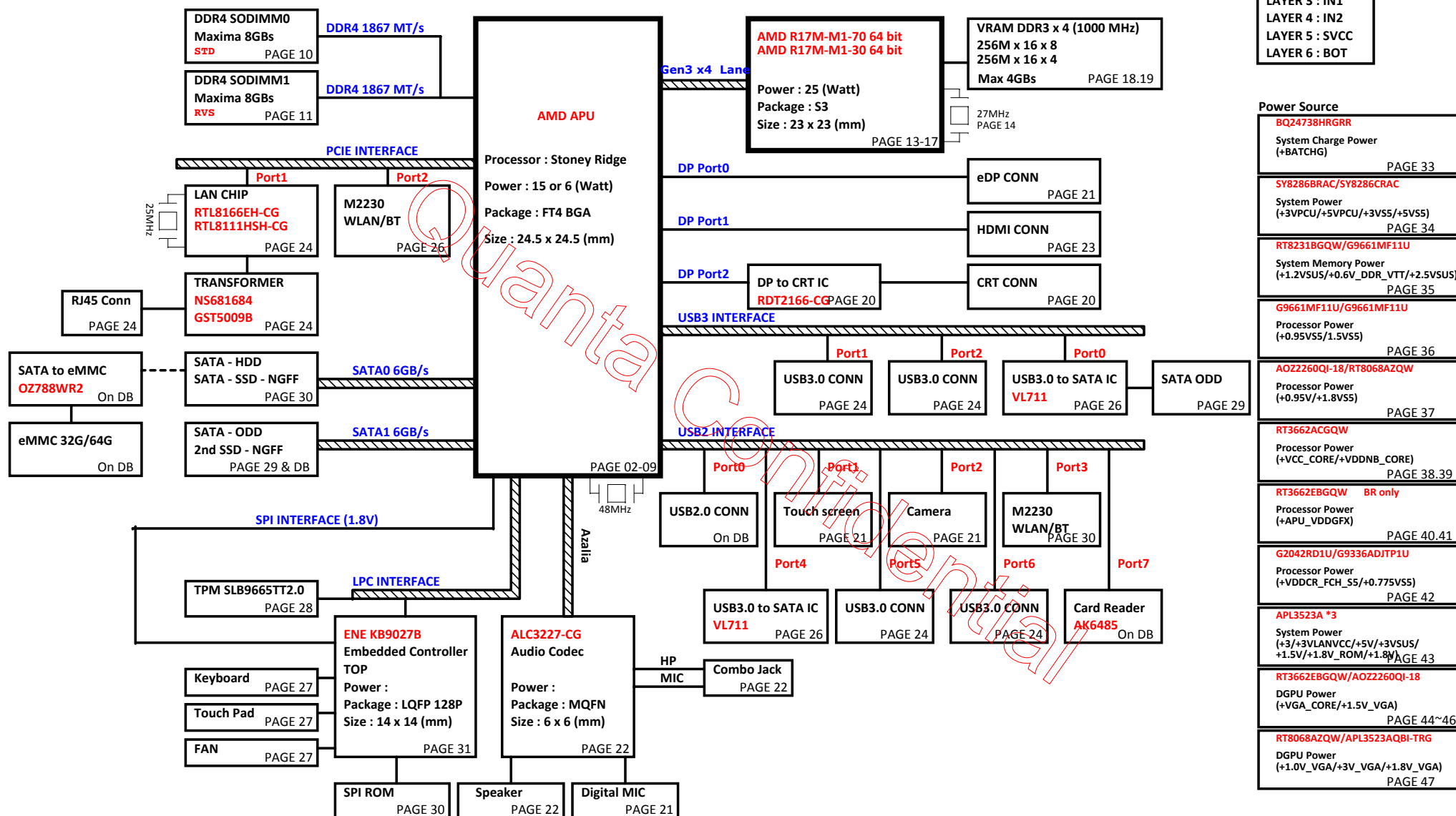
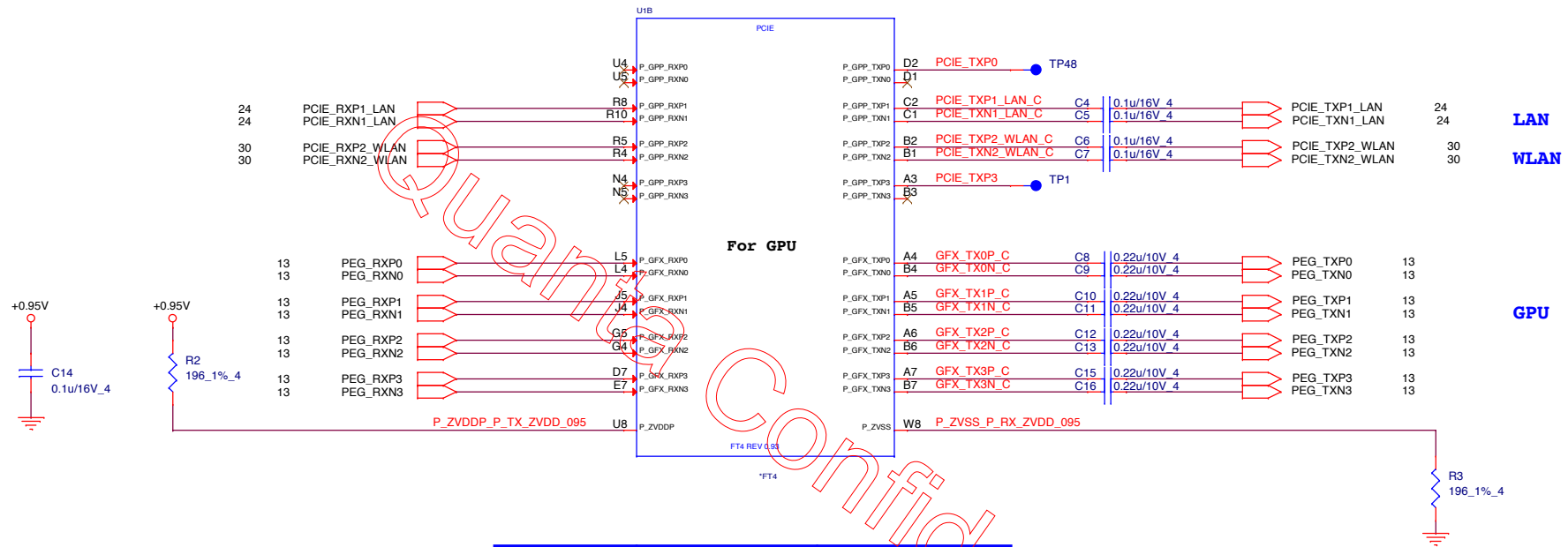


NFL-C 14" AMD SR FT4 DIS/UMA Block Diagram



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



	QBCON PN	TOP BSO
A9-9420	AJ094208T02	AJ094208T01
A6-9220	AJ09220RT01	AJ09220RT00
A4-9120	AJ09120UT01	AJ09120UT00
A6-9200e	AJ00920UT01	AJ00920UT00
E2-9000e	AJ900EAVT01	AJ900EAVT00

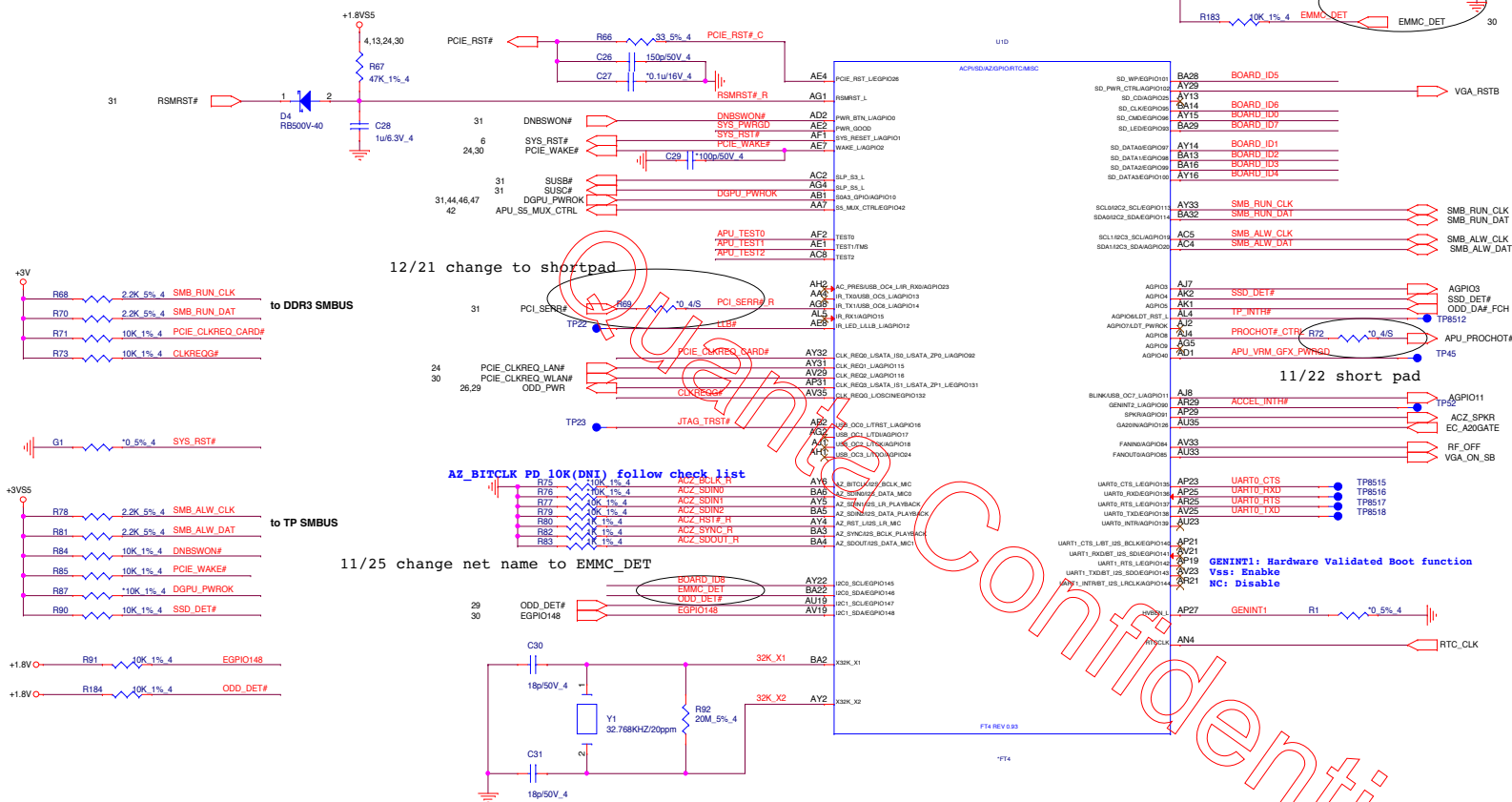


PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

Size	Document Number	Rev
	ST 17(PCIE)	1A

Date: Wednesday, March 08, 2017 Sheet 2 of 48





Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14 "
01	Reserve
10	Reserve
11	Reserve

Board ID [4:3]	Definition
00	Reserve
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0	BR
1	SR

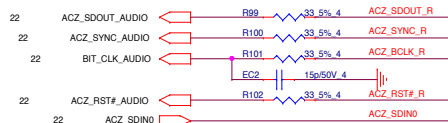
Board ID [6]	Definition
0	VRAM x8
1	VRAM x4

Board ID [7]	Definition
0	R17M-M1-70
1	R17M-M1-30

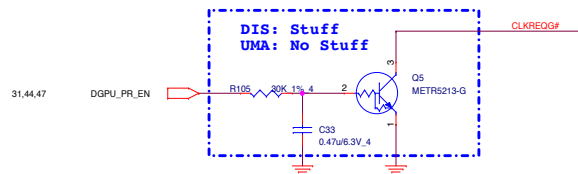
Board ID [8]	Definition
0	6W CPU
1	15W CPU

12/21 add CPU Watt.

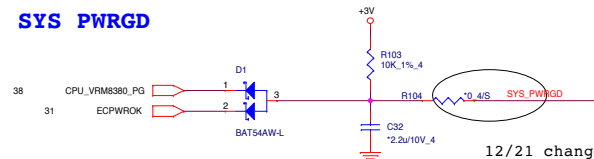
HDA INTERFACE



GPU CLK REQ



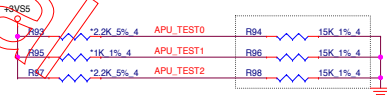
SYS PWRGD



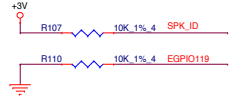
12/21 change to shortpad

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
ad0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAC pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAC enabled

Follow AMD checklist 55347 suggestion.



Follow Checklist



12/21 change to shortpad

HDD

ODD or SSD

BT_OFF

CLK GFX_P

CLK GFX_N

CLK POE_LAMP

CLK POE_LANN

CLK POE_WLANP

CLK POE_WLANN

CLK_33M_KBC

CLK_PCL_TPM

CLK_33M_DEBUG

KBC_RST#

R115

R116

R117

R118

R119

R120

R121

R122

R123

R124

R125

R126

R127

R128

R129

R130

R131

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R425

R426

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R428

R429

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R438

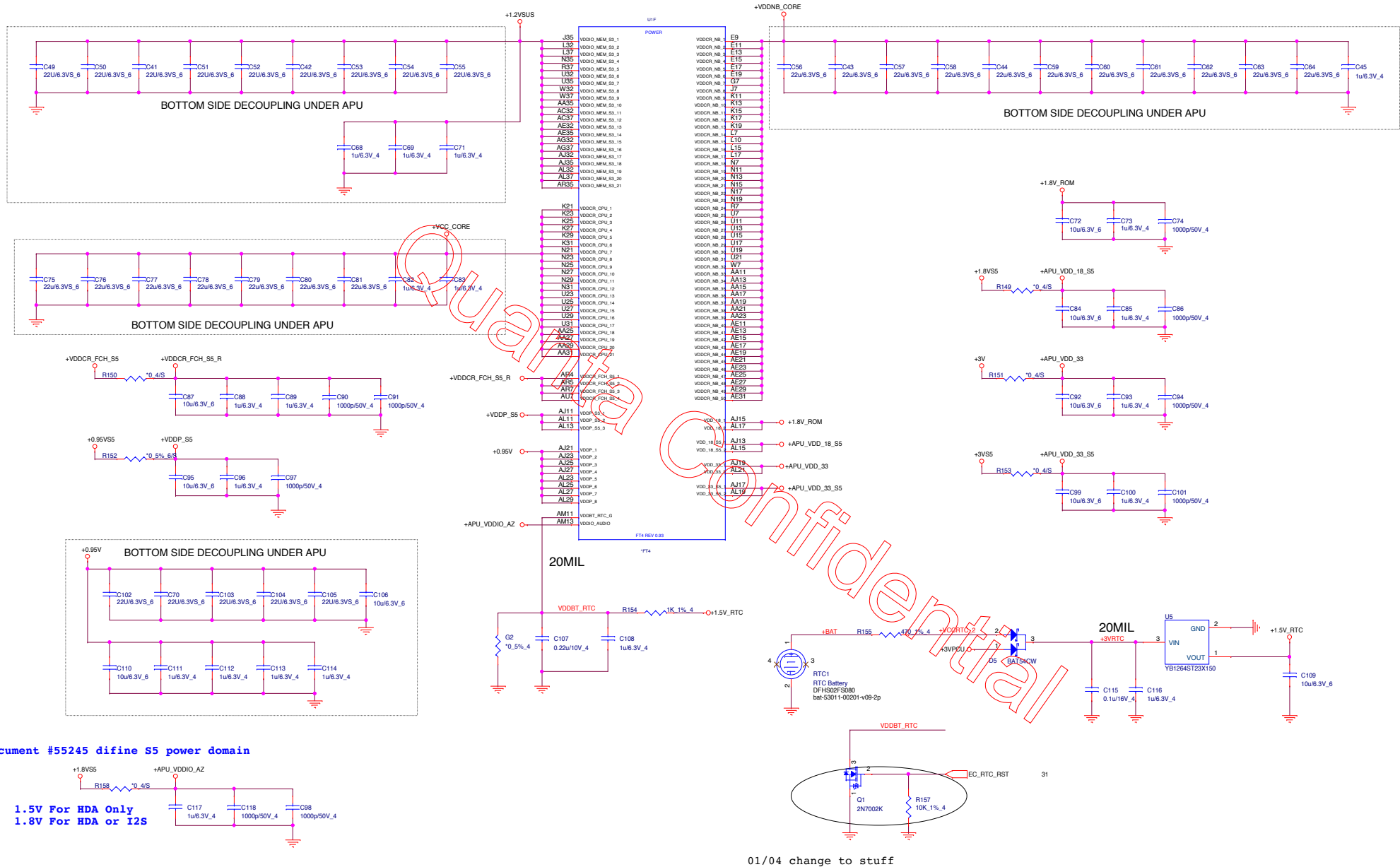
R439

R440

R441

R442

Power Decoupling follow Check list by AMD suggestion



01/04 change to stuff




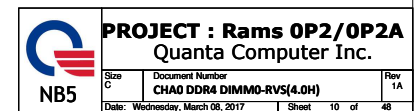
PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

Size	Document Number	Rev
	ST 717 (GND)	1A
Date: Wednesday, March 08, 2017 Sheet 8 of 48		

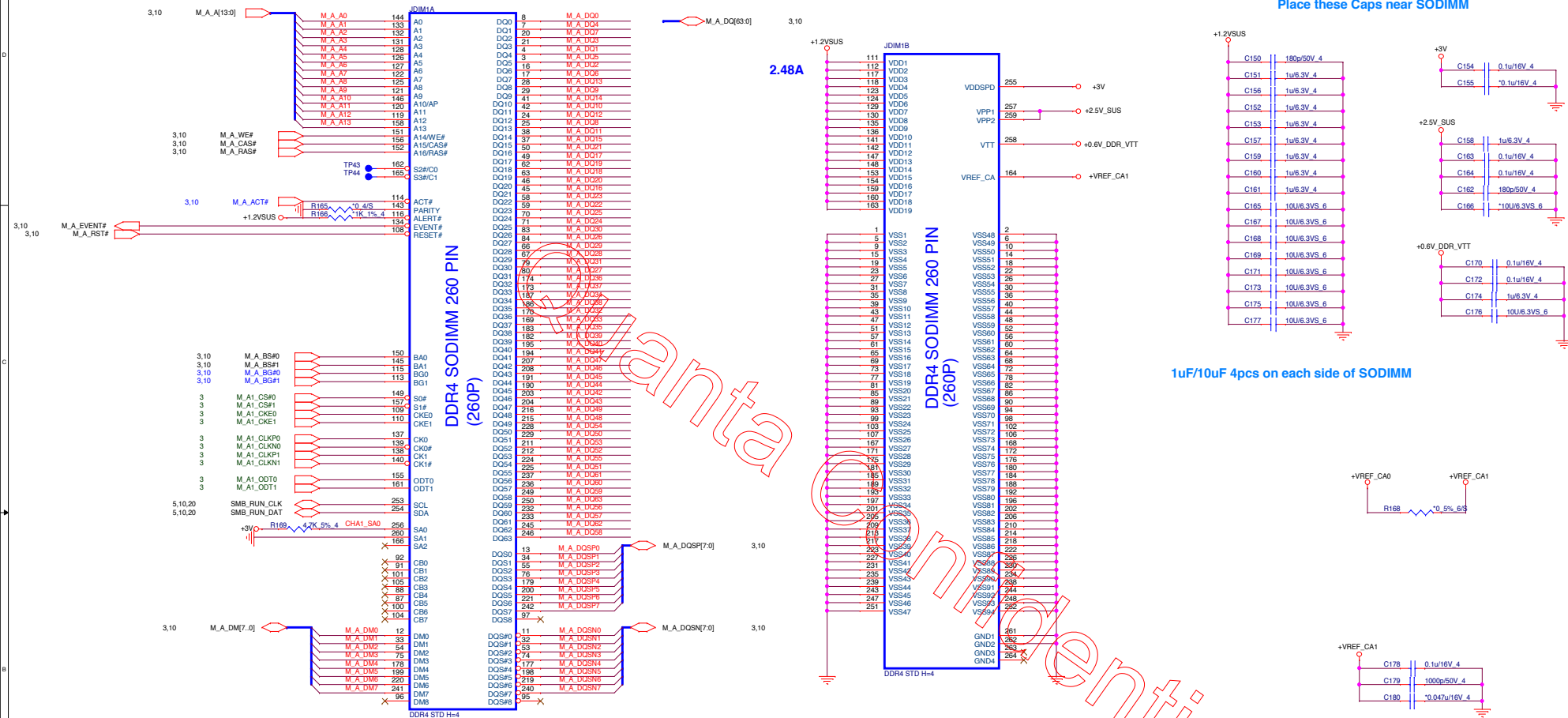
Quanta Confidential

<Reserved>

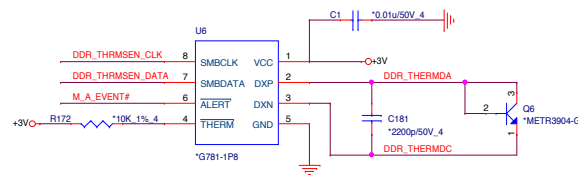
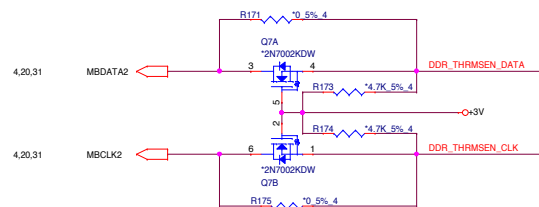
 NB5	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 9 of 48		



Place these Caps near SODIMM

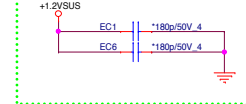


Local Thermal Sensor




Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

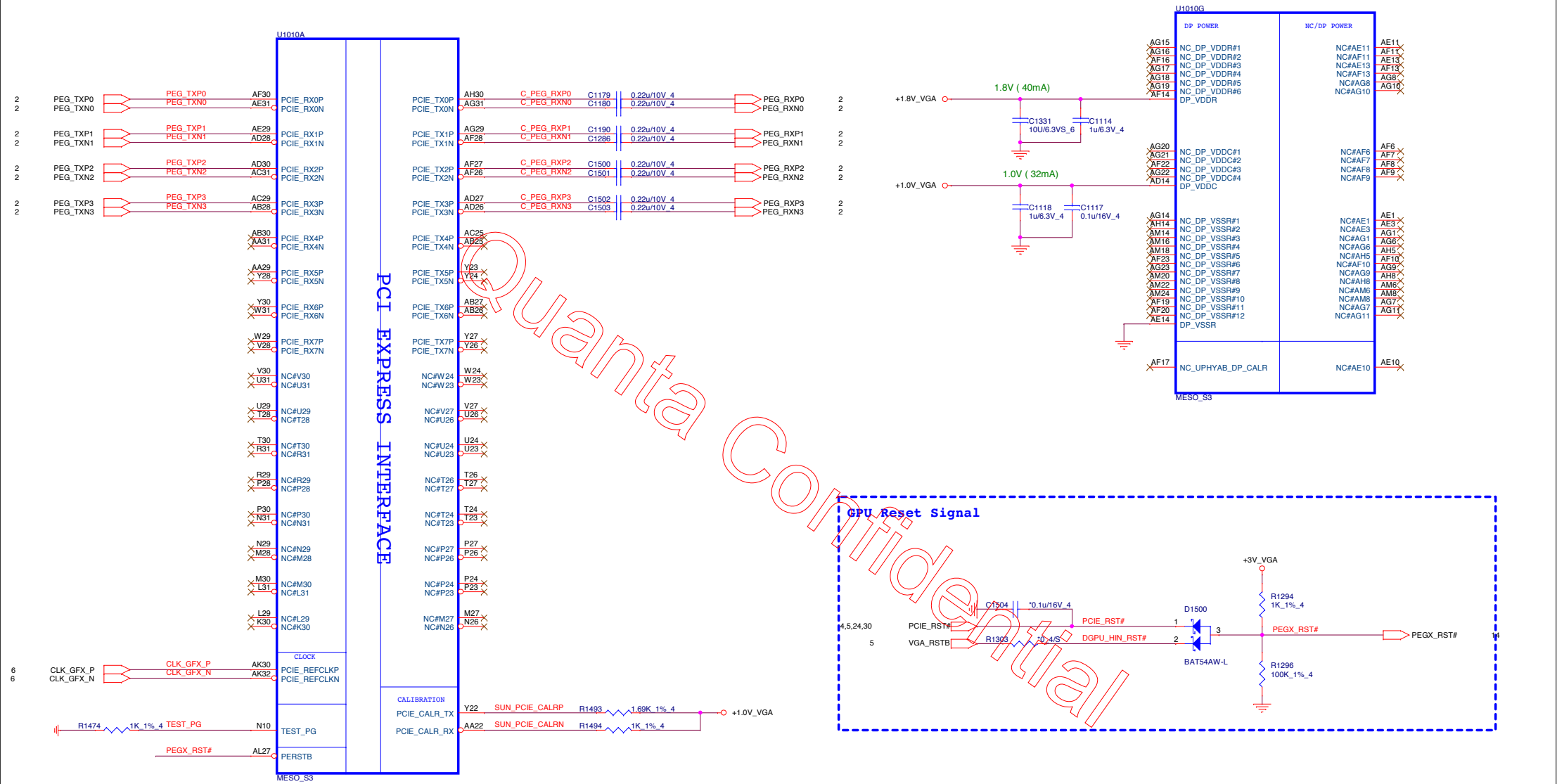
For EMI CAP



<Reserved>

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 NB5	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 12 of 48		



PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_PCIE/DP POWER	1A
Date: Wednesday, March 08, 2017	Sheet	13 of 48

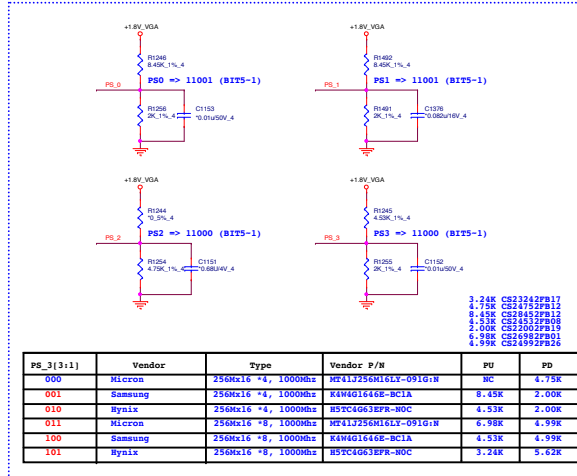
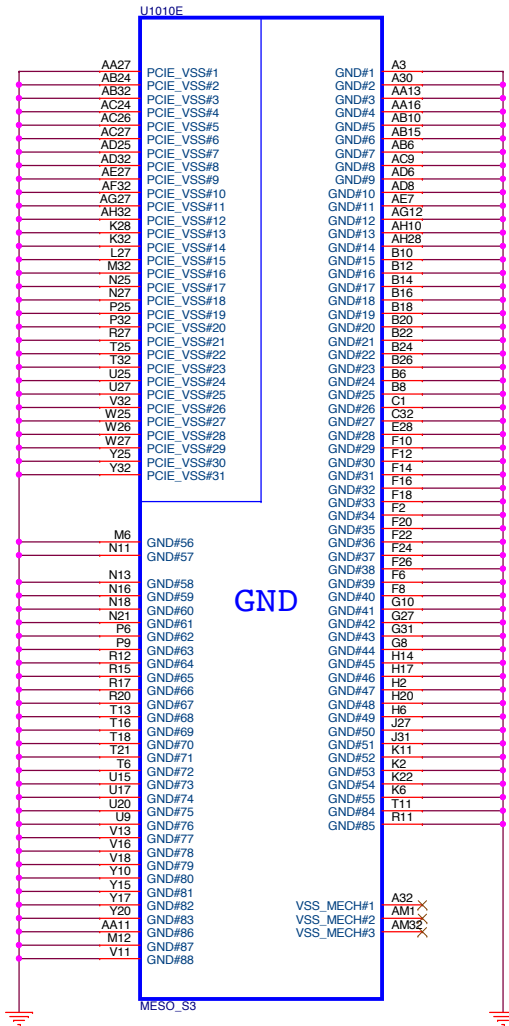


Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

VRP ID#	Strap Name	Description	Recommended Settings
PS_0101	N/A	IF STRAP_BIOS_ROM_EN = 1, N/A, CONFIG01-01 forces the ROM type	
PS_0102	STRAP_CONFIG01	IF STRAP_BIOS_ROM_EN = 0, N/A, CONFIG01 defines the primary recovery operation state. See Factory Recovery Operation state. See Factory Recovery Operation state. See	Design dependent, see the description.
PS_0103	STRAP_CONFIG02		
PS_0104	N/A	Reserved for internal use only. Must be 0 at start.	1
PS_0105	N/A	Reserved	1
PS_1111	STRAP_BIF, GENI_EN_A	1 = PC GENI capability. 0 = PC GENI is supported. 0 = PC GENI is supported. Determines whether or not the PC reference clock or power management capability is reported in the PC GENI capability (see reference to GENI in CLARIFIE). 0 = The CLARIFIE power management capability is disabled 1 = The CLARIFIE power management capability is enabled	Design dependent, see the description.
PS_1121	STRAP_BIF_CLK_PUL_IN		0
PS_1122	N/A	Reserved for internal use only. Must be 0 at start.	0
PS_1141	STRAP_T1_EXP_FULL_SYNC	Control the transmitter full-half wave mode 0 = The transmitter half-wave is enabled 1 = The transmitter full-wave is enabled	1
PS_1151	STRAP_T1_DISABLEPHN_EN	PC1EXRESS transmitter, disable-external. 0 = Tx disable-external disabled. 1 = Tx disable-external disabled.	Design dependent, see the description.
PS_2101	N/A	Reserved.	0
PS_2102	N/A	Reserved.	0
PS_2103	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2141	N/A	Reserved.	1
PS_2151	N/A	Reserved	1
PS_3101	BOARD_CONFIG01	Board configuration related booting, such as the memory ID	Design dependent, see the description.
PS_3102	BOARD_CONFIG01		
PS_3103	BOARD_CONFIG02		
PS_3141	N/A	Reserved.	1
PS_3151	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

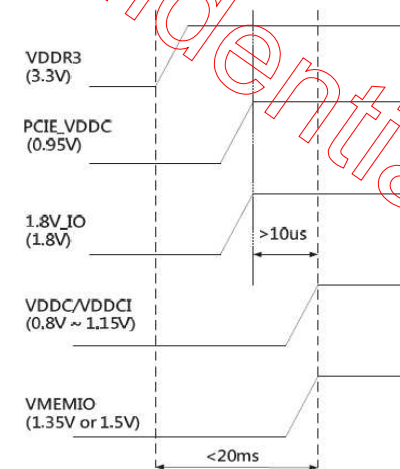
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

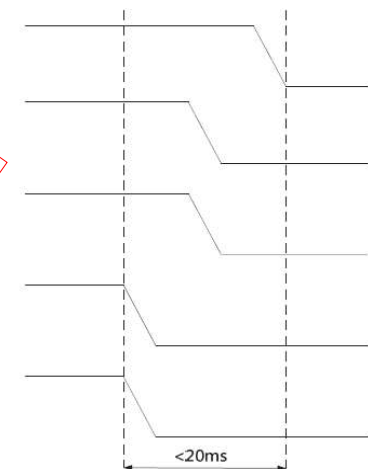
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

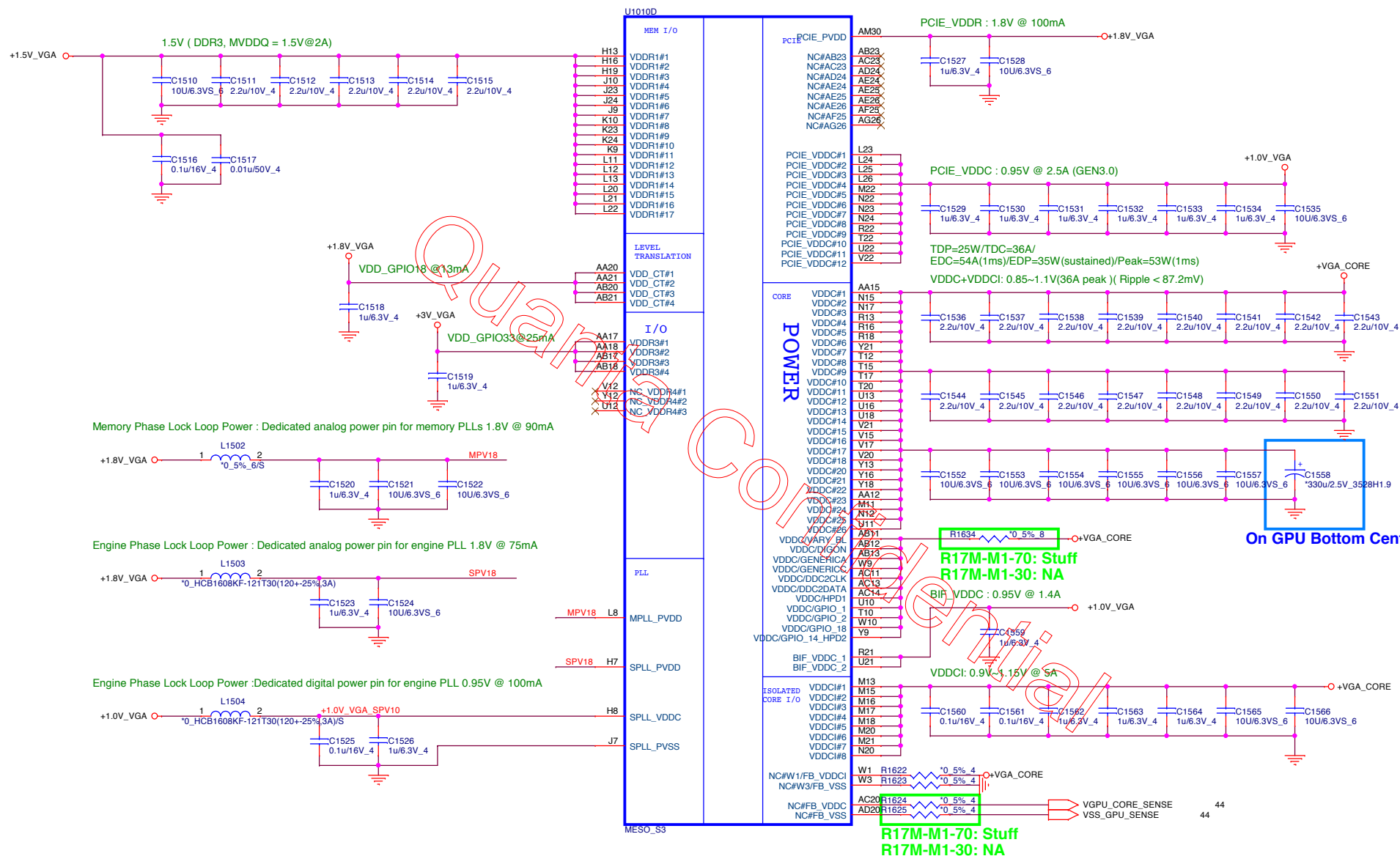


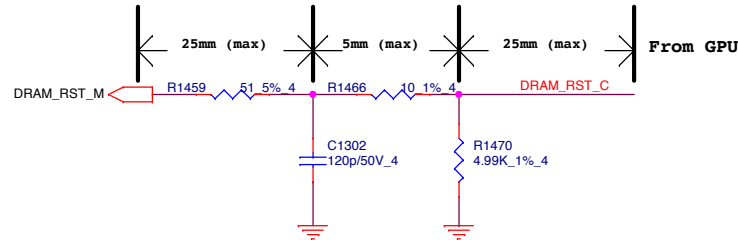
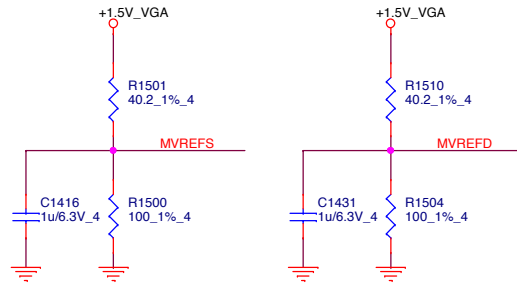
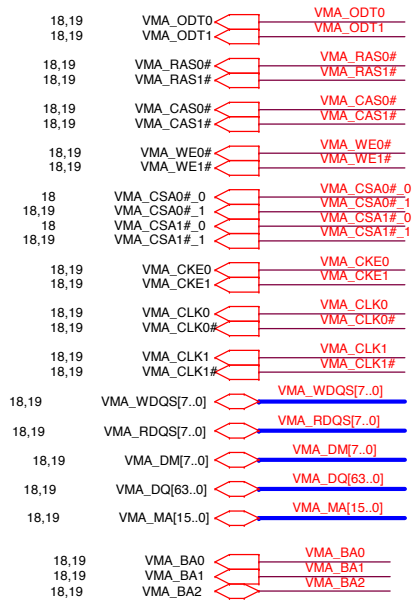
POWER DOWN



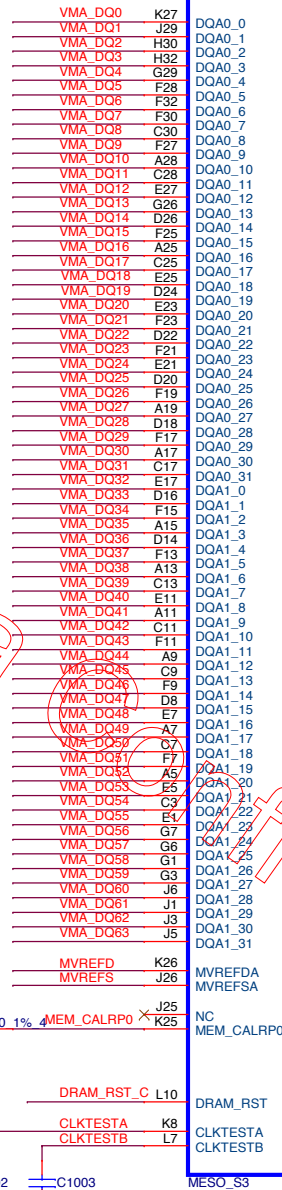
PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

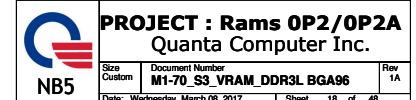
Size Document Number
M1-70_S3_GND/LVDS/Strap Rev 1A
 Date: Wednesday, March 08, 2017 Sheet 15 of 48

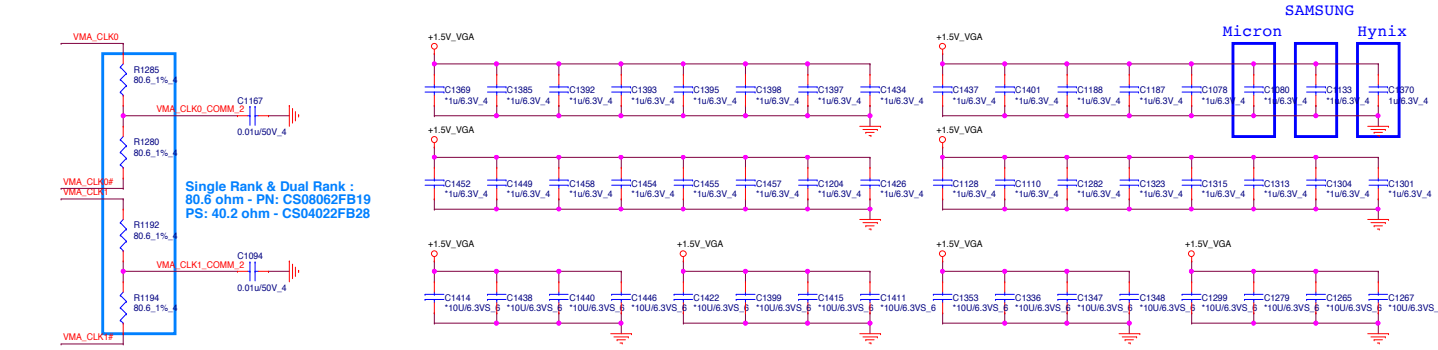




Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)
This basic topology should be used for DRAM_RST for DDR3/GDDR5.

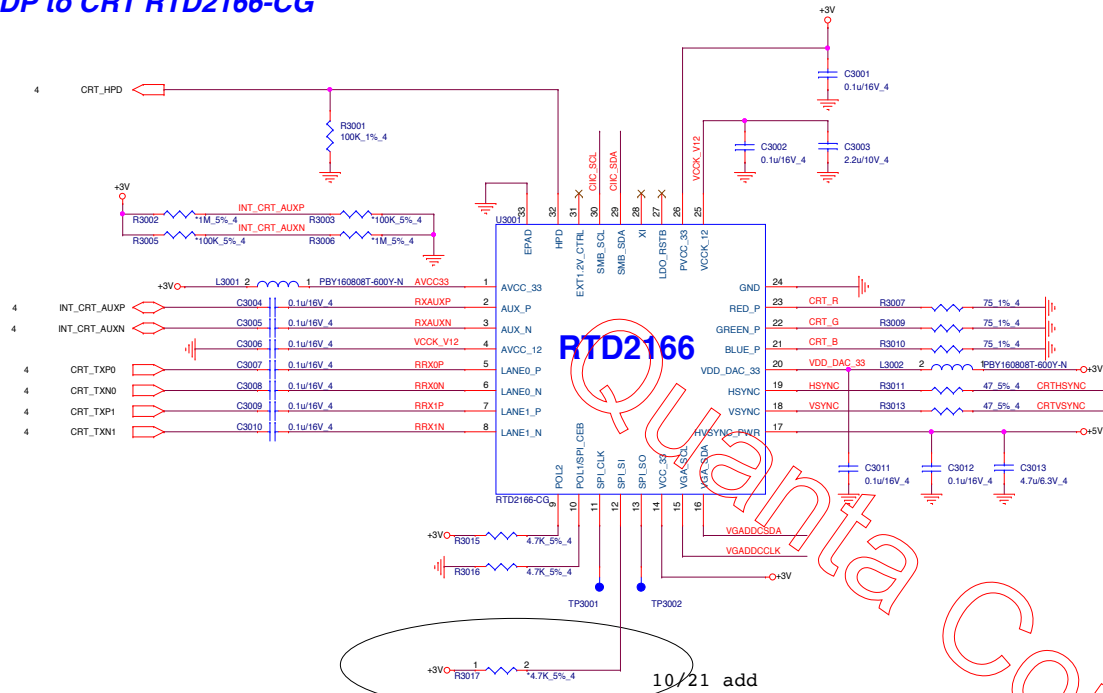






	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PFDTW02	AKD5PFDTW01

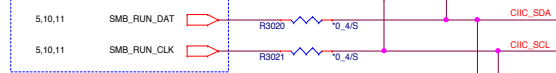
DP to CRT RTD2166-CG



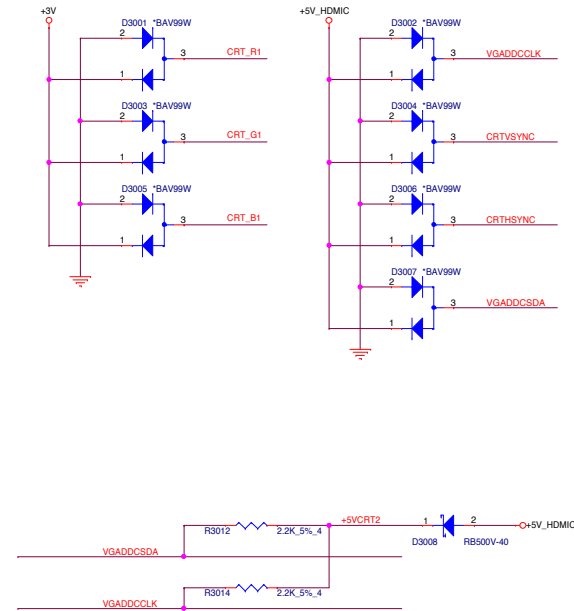
CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
 ROM or EEPROM mode: connect to PCH SMBUS
 IIC Protocol is used

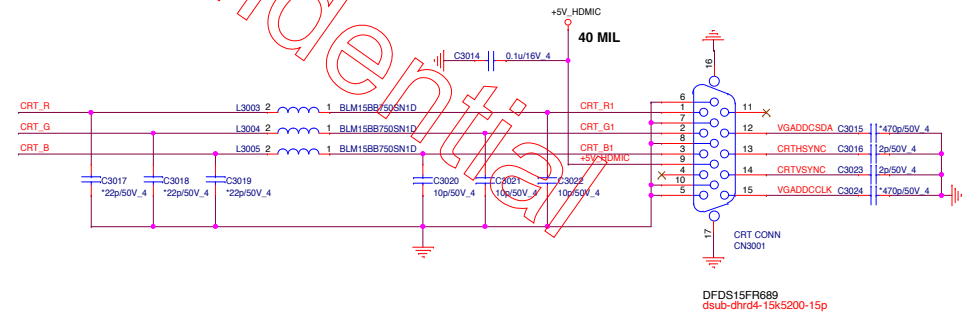
From PCH



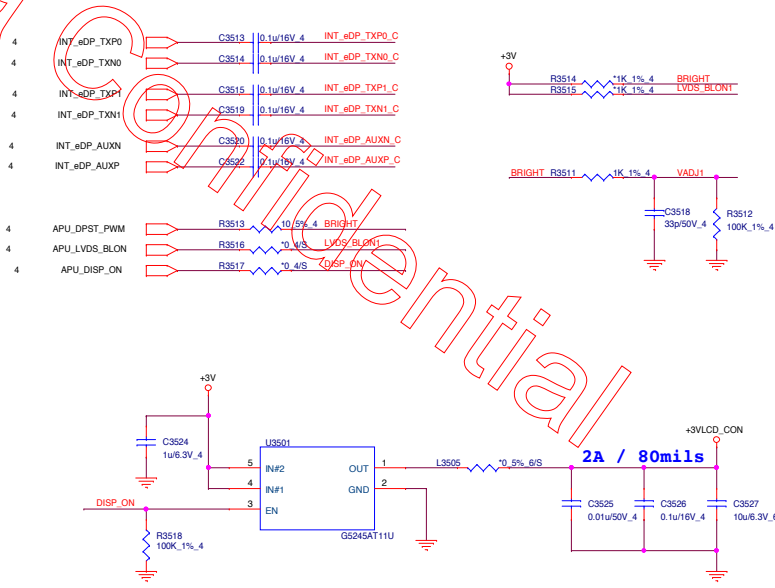
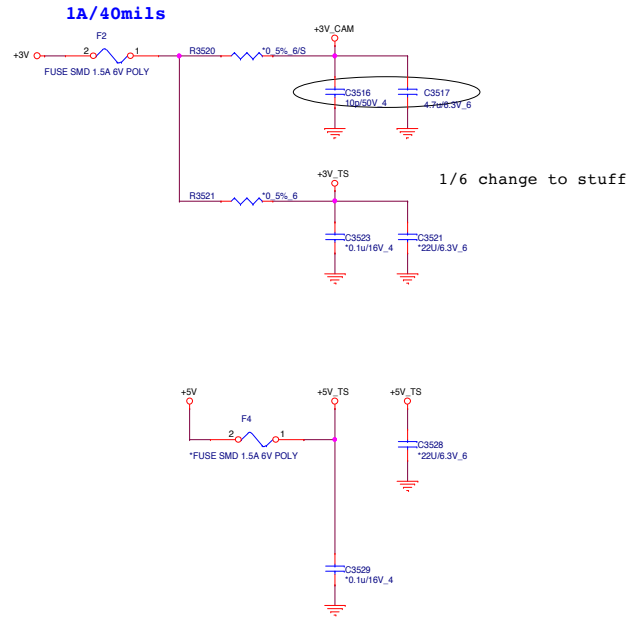
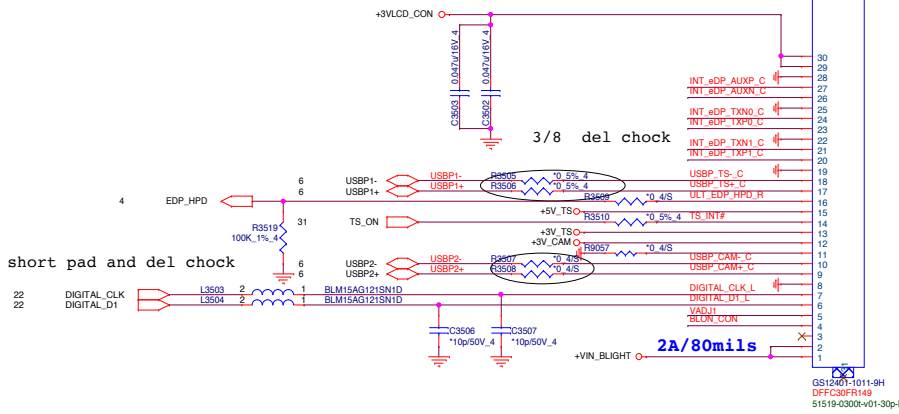
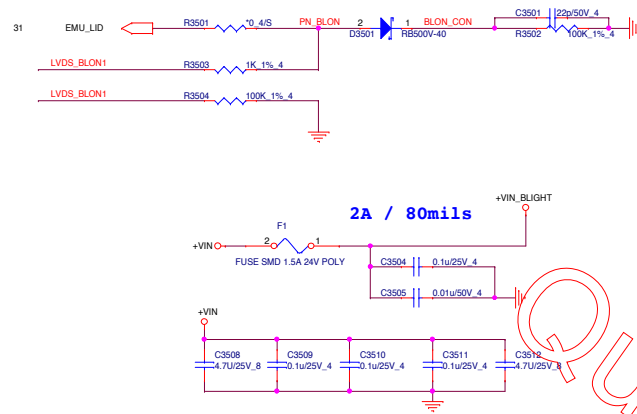
From EC



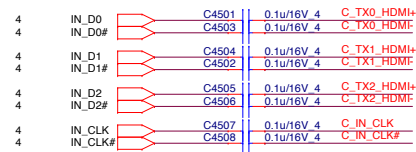
Confidential



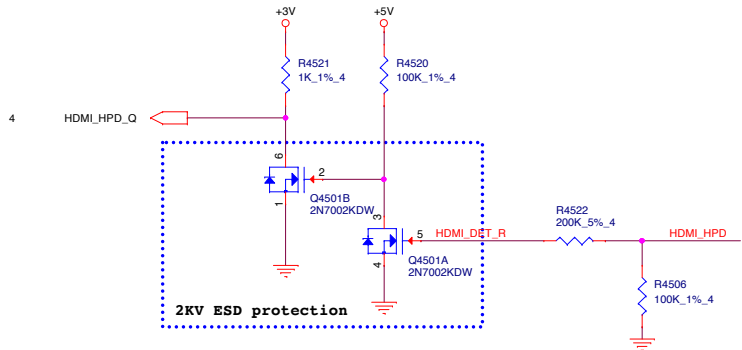
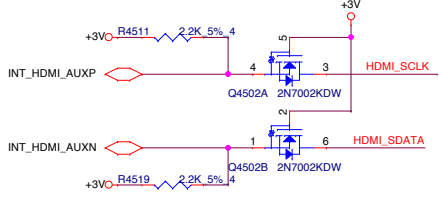
LID Switch



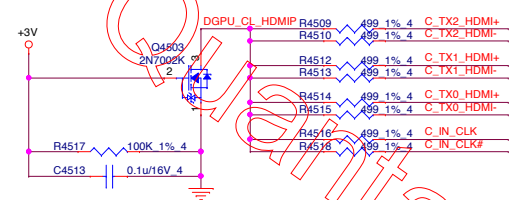




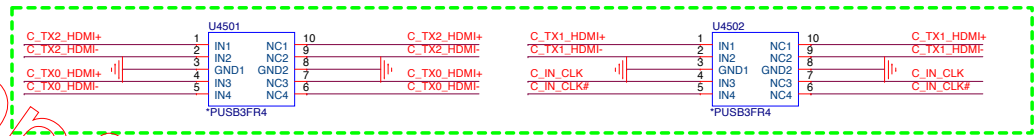
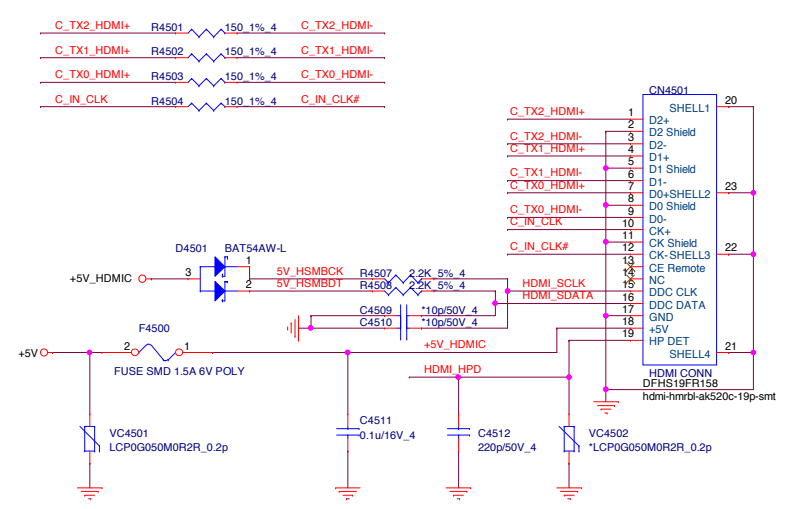
HDMI SMBus Isolation

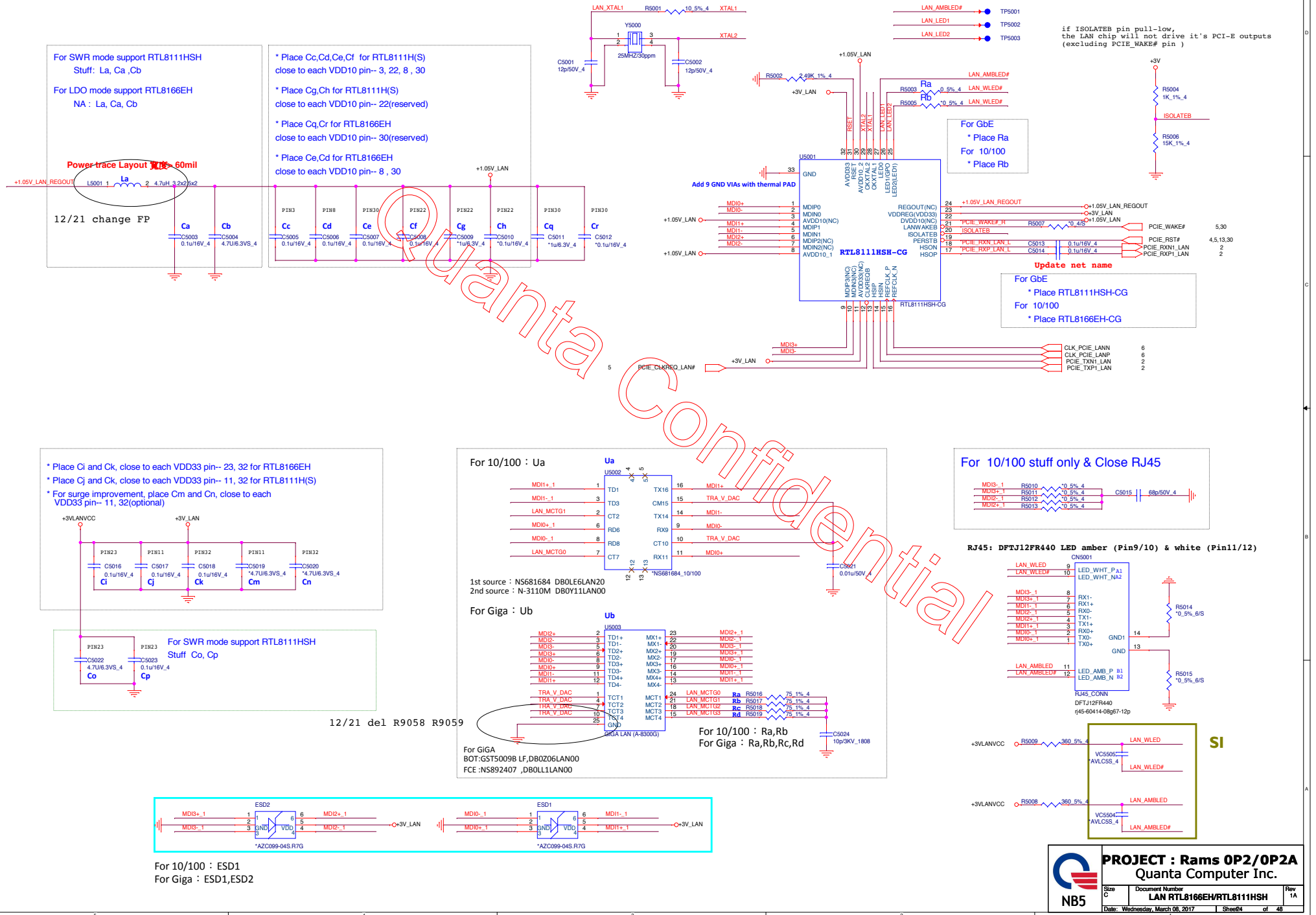


Close to HDMI connector

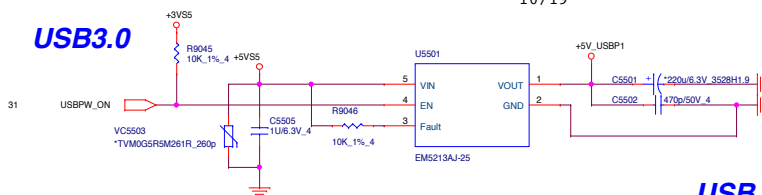


EMI Solution

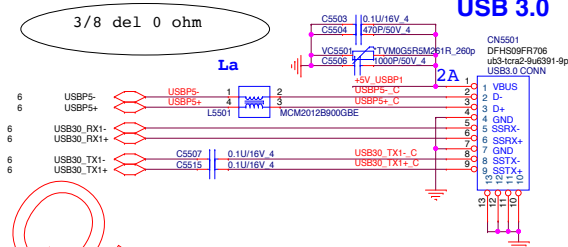




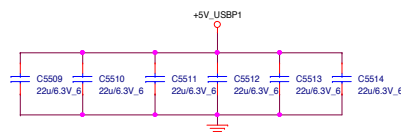
USB3.0



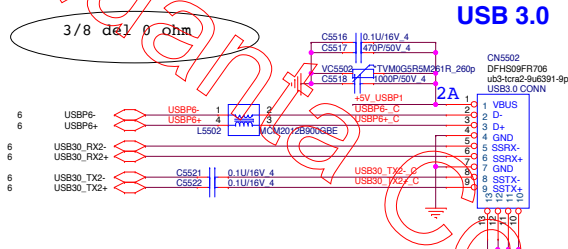
USB 2.0/3.0 Combo



USB 3.0

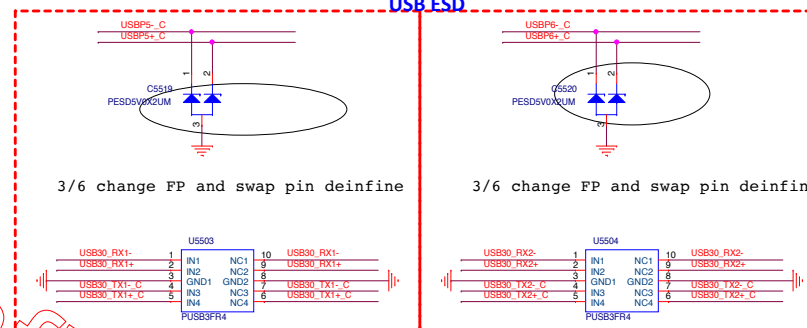


USB 2.0/3.0 Combo



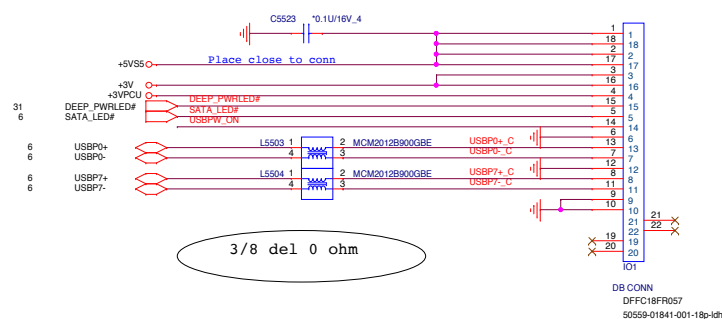
USB 3.0

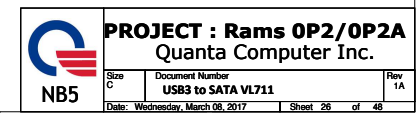
USB ESD



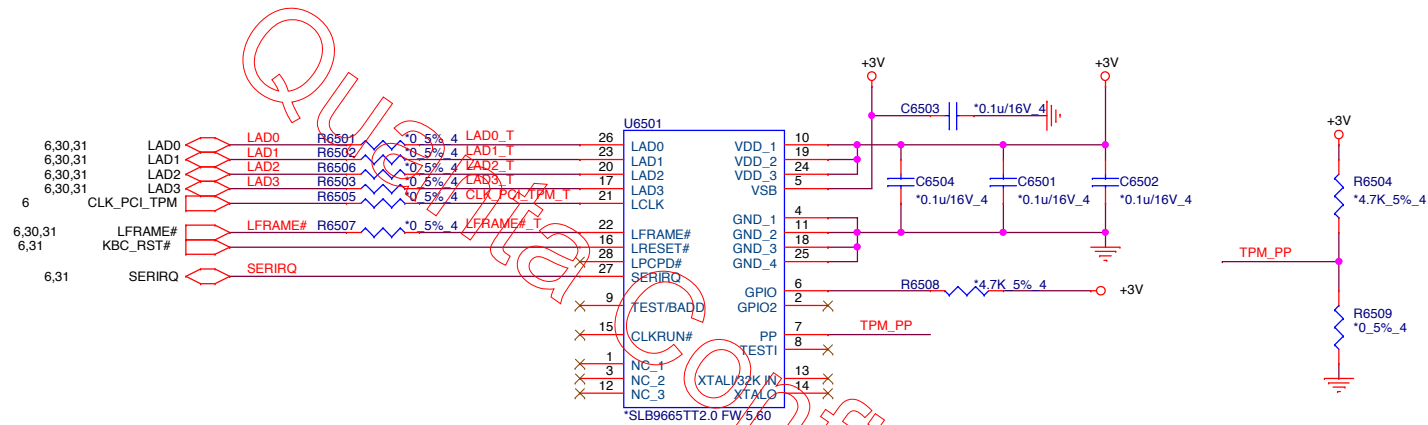
Daughter Board

USB2.0 CONN ON DB
Card Reader





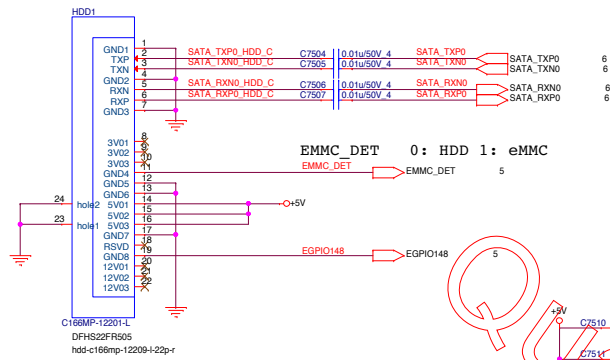
TPM



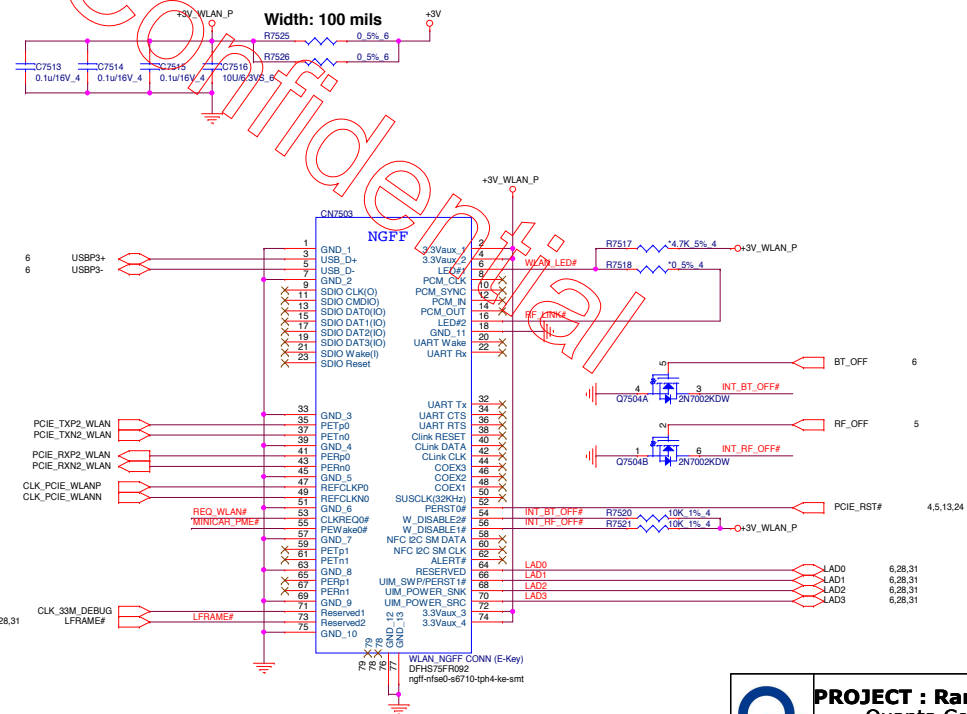
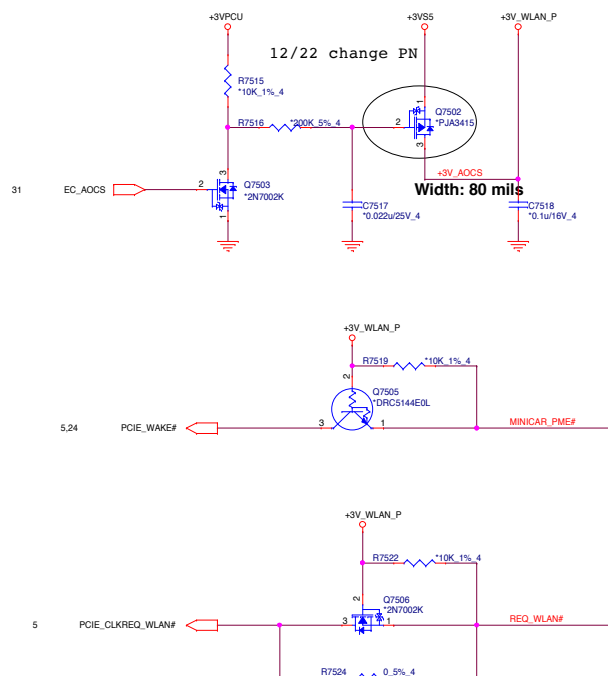
PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

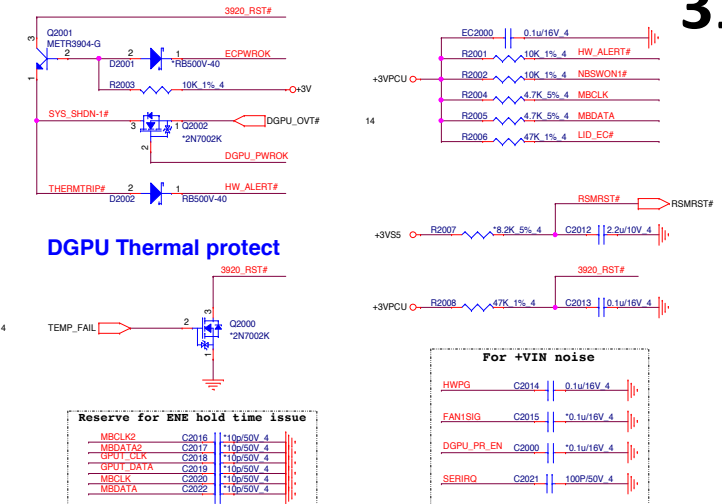
Size B	Document Number	Rev 1A
	TPM	
Date: Wednesday, March 08, 2017	Sheet 28	of 48

SATA HDD

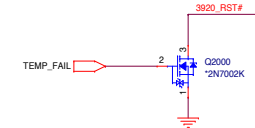


WLAN & BT





DGPU Thermal protect



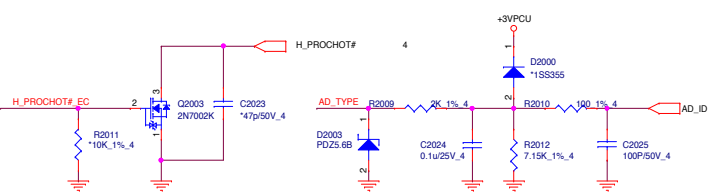
Reserve for ENE hold time issue

MBCLK2	C2016	*10p/50V 4
MBDATA2	C2017	*10p/50V 4
GPOT_CLK	C2018	*10p/50V 4
GPOT_DATA	C2019	*10p/50V 4
MBCLK	C2020	*10p/50V 4
MBDATA	C2022	*10p/50V 4

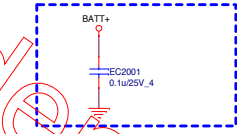
For +VIN noise

The timing diagram shows four digital signals over time. The signals are: HWPG (C2014), FAN1SIG (C2015), DGPU_PR_EN (C2000), and SERIRQ (C2021). The voltage levels are indicated as 0.1u/16V_4 for the first three signals and 100P/50V_4 for SERIRQ. The signals are shown as red lines with blue vertical markers indicating transitions.

Smart Adapter Type Check



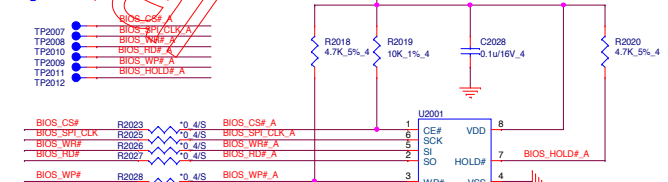
Close Battery CONN



Adapter Select

GPIO 42	adapter
R2014 stuff	65W
R2015 stuff	45W
R2014 & R2015 stuff	90W

TPs need place to all TOP or all BOT

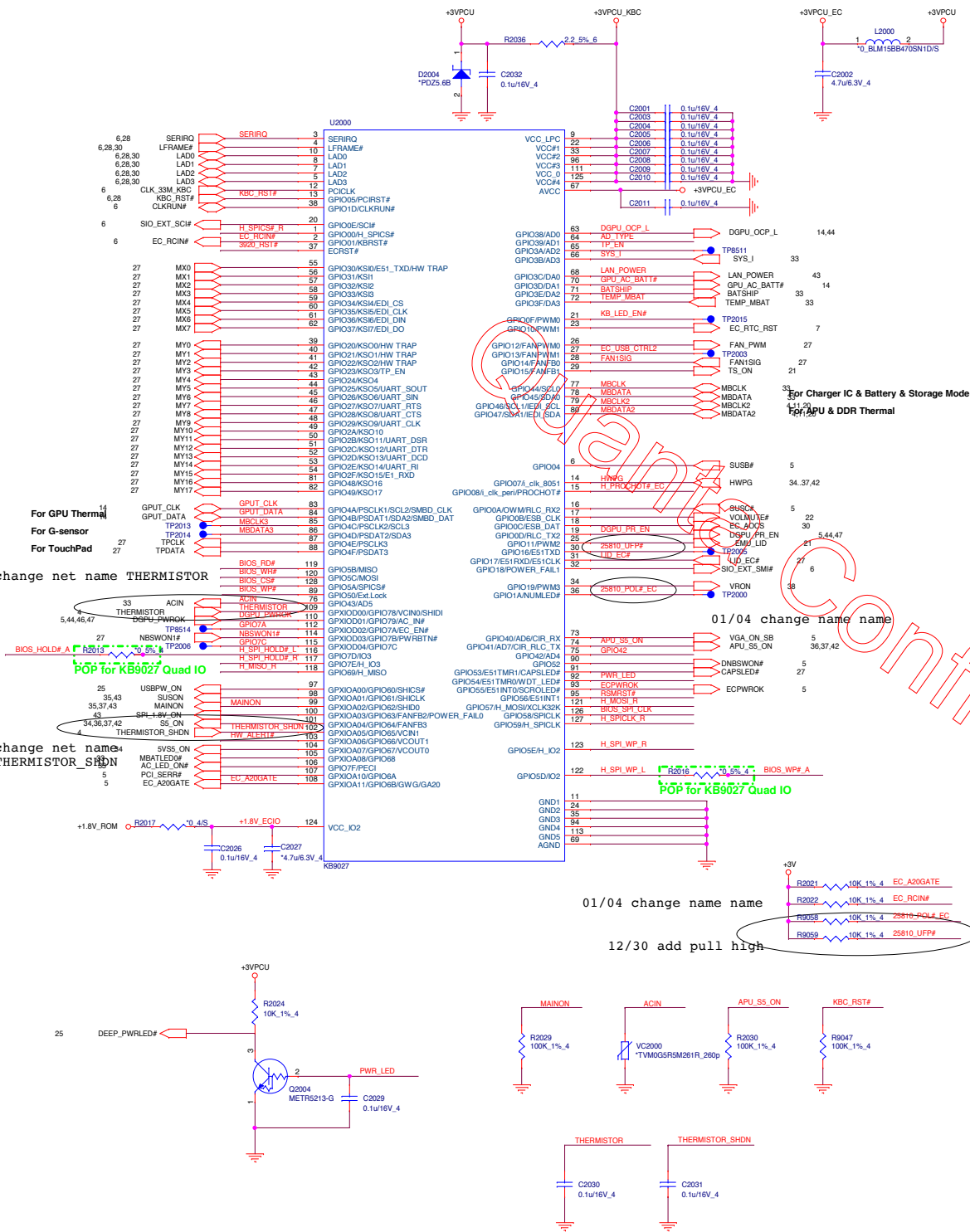


Vender	Size	P/N (3.3V)
WND	8M	AKE3EFP0N07
GGD	8M	AKE2EZNOQ00
AEO	8M	AKE3GZNO0S01
Socket	DFHS08FS023	



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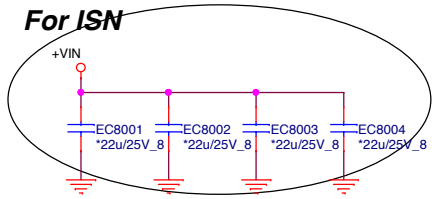


```
01/04 change name name
```

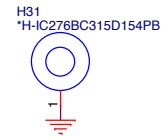
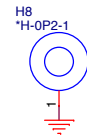
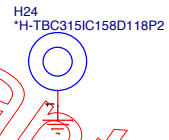
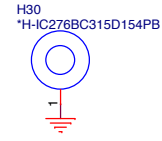
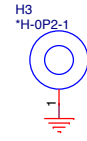
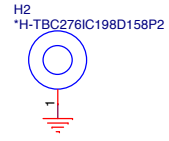
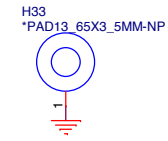
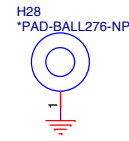
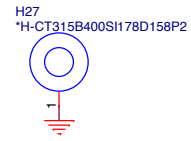
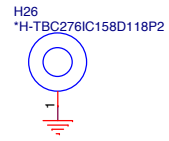
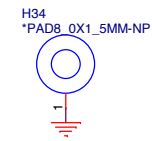
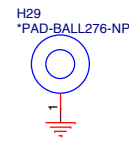
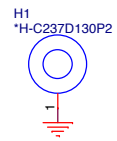
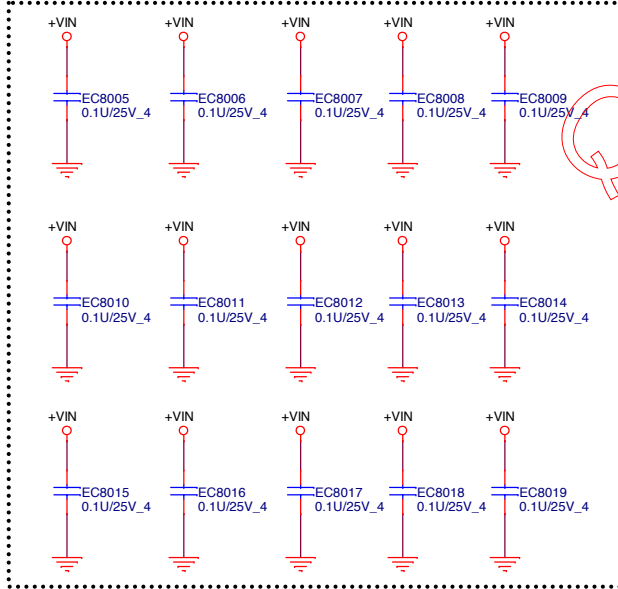
12/30 add pull high

POP for KB9027 Quad IC

For ISN




Place on +VIN Path



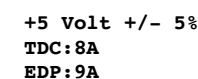
PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

Size B	Document Number EMI CAP/HOLES	Rev 1A
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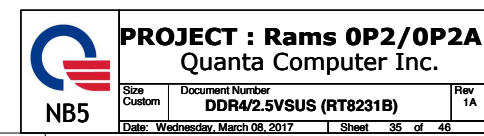
 NB5	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size Custom	Document Number Charger (BQ24728H)	Rev 1A
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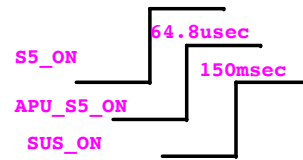
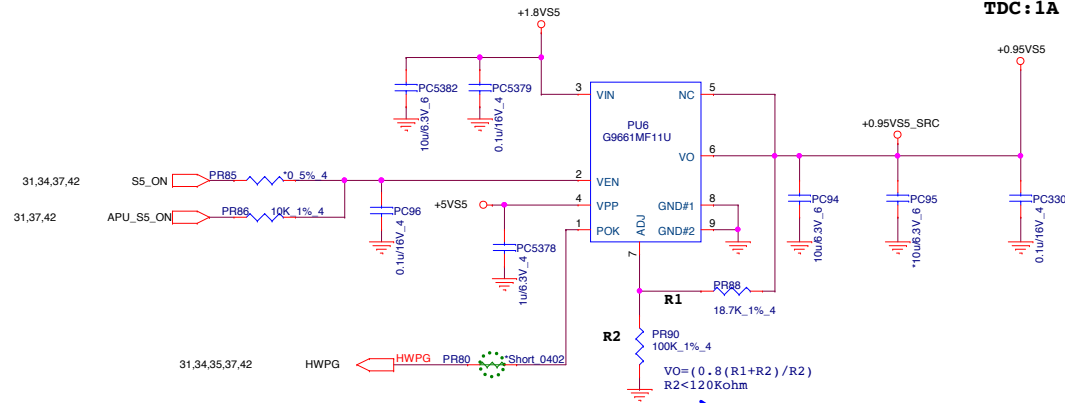
$V_{ih} = 0.8V$



Do Not add test pad on VCC & LDO pin

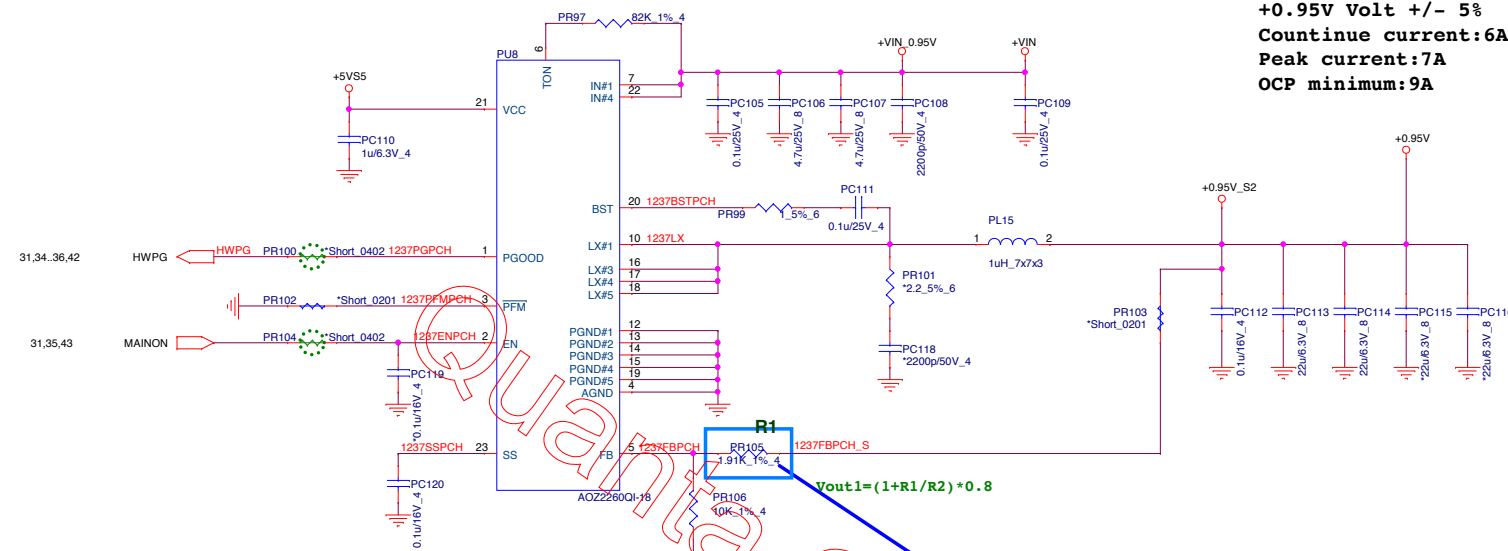


+0.95V +/- 5%
TDC: 1A



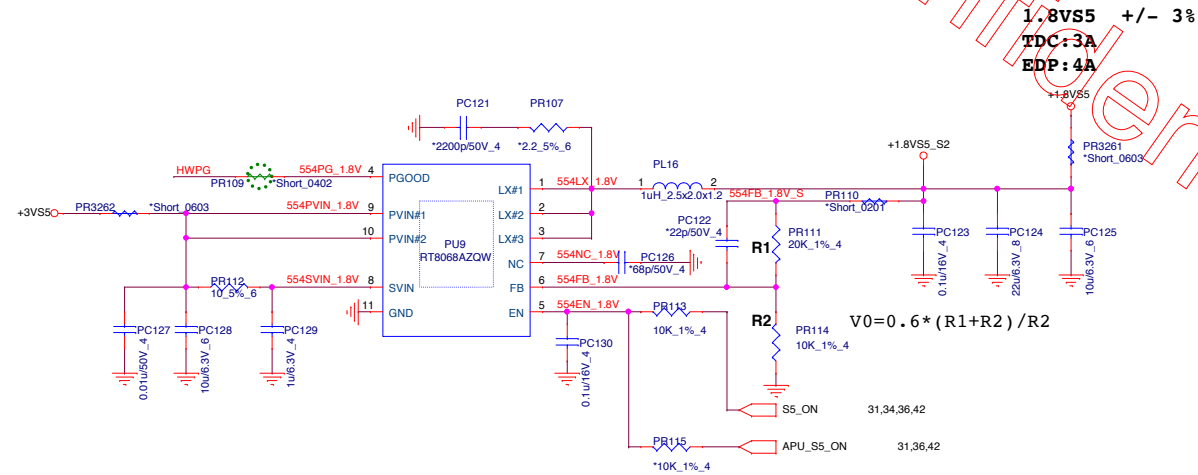
R1			
	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

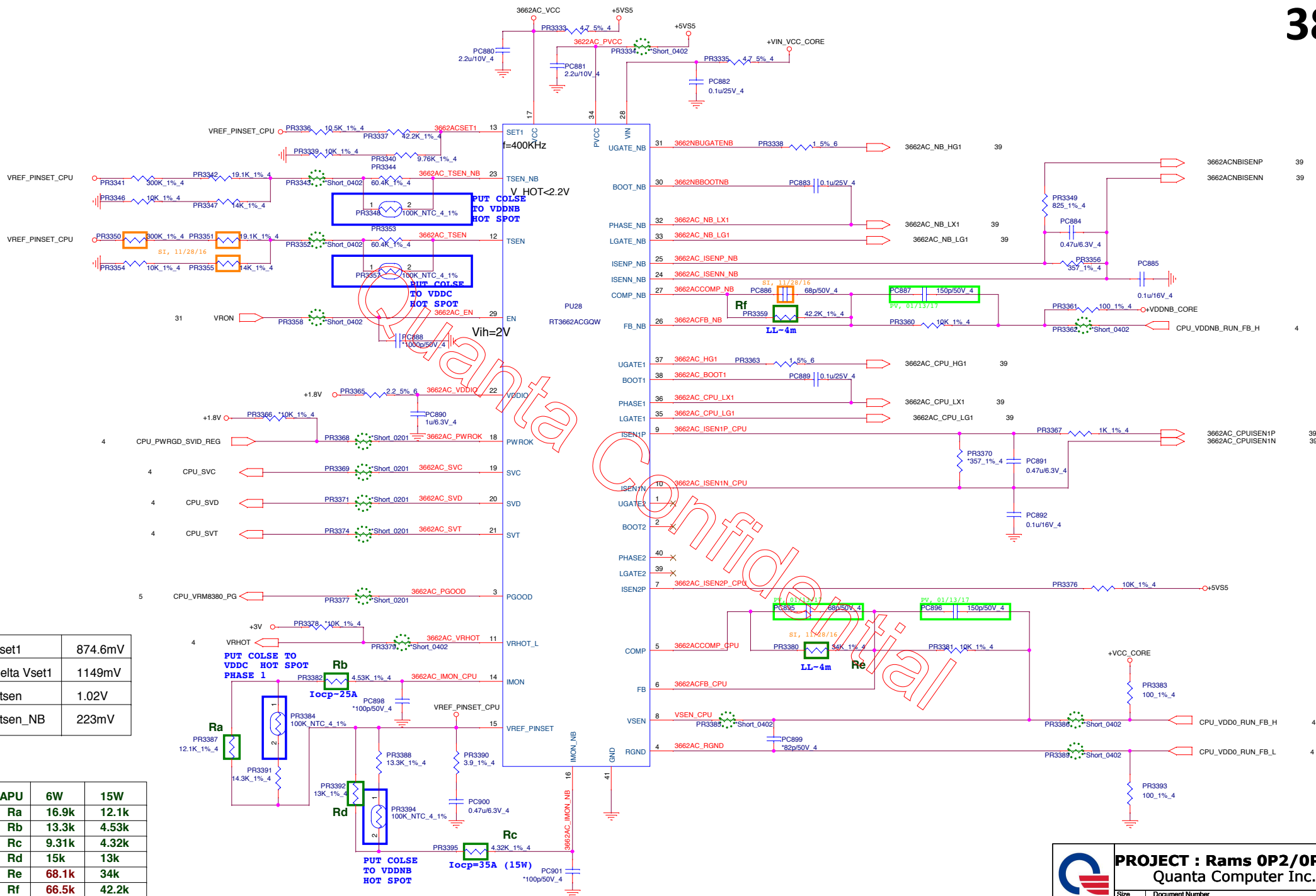
Bristol VDDP=1.05V
Stoney VDDP=0.95V



Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

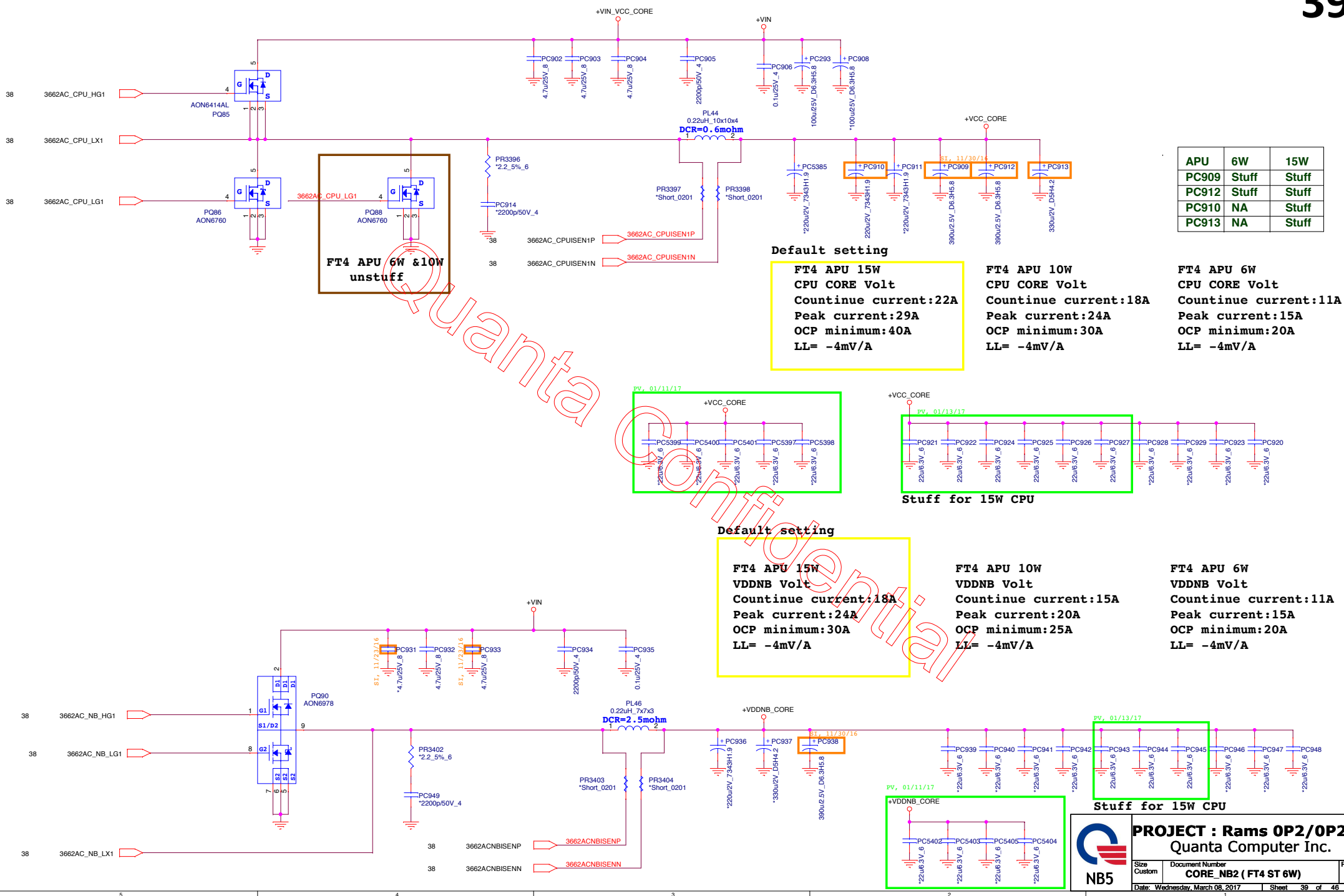
	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V






Vset1	874.6mV
Delta Vset1	1149mV
Vtsen	1.02V
Vtsen_NB	223mV

APU	6W	15W
Ra	16.9k	12.1k
Rb	13.3k	4.53k
Rc	9.31k	4.32k
Rd	15k	13k
Re	68.1k	34k
Rf	66.5k	42.2k

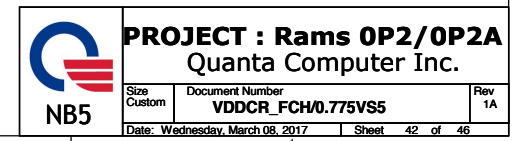
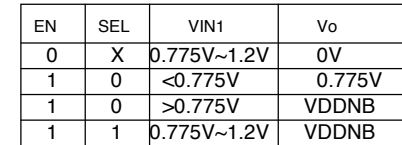


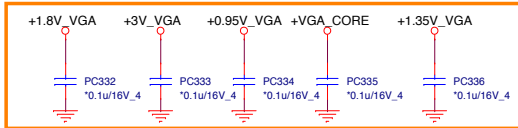
Quanta Confidential

 NB5	PROJECT : Rams OP2/OP2A Quanta Computer Inc.				
	Size Custom	Document Number GFX1 (Stonlry N/A)			Rev 1A
	Date: Wednesday, March 08, 2017			Sheet	40 of 46

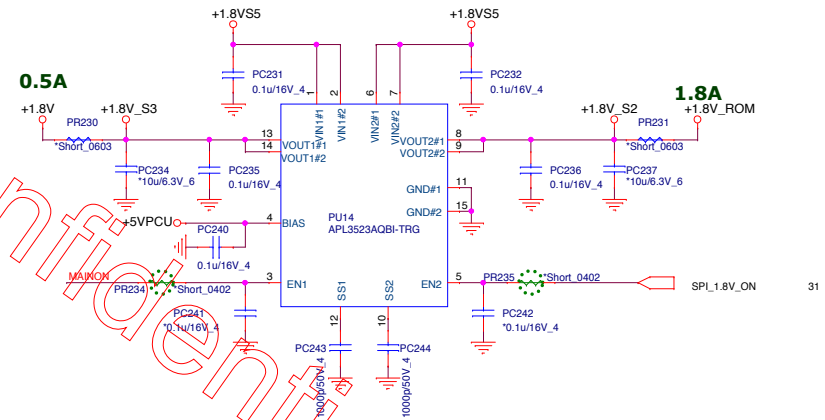
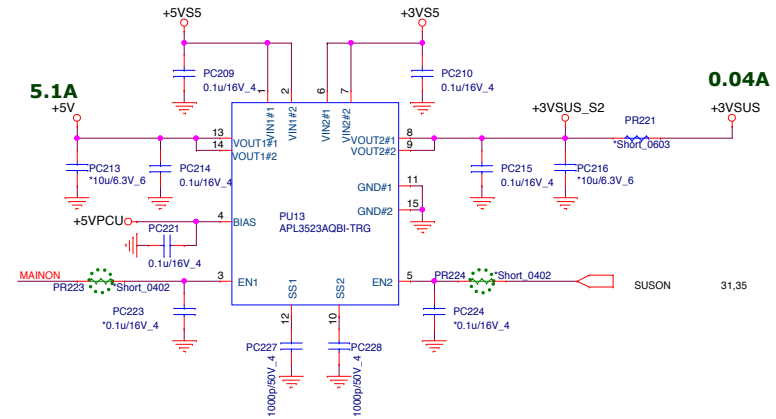
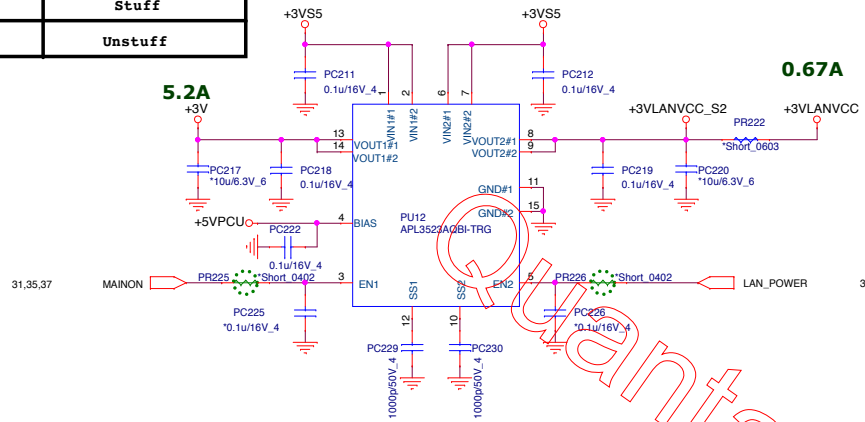
CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff

Quanta Confidential



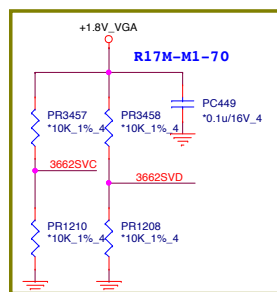


UMA only	Stuff
discrete	Unstuff



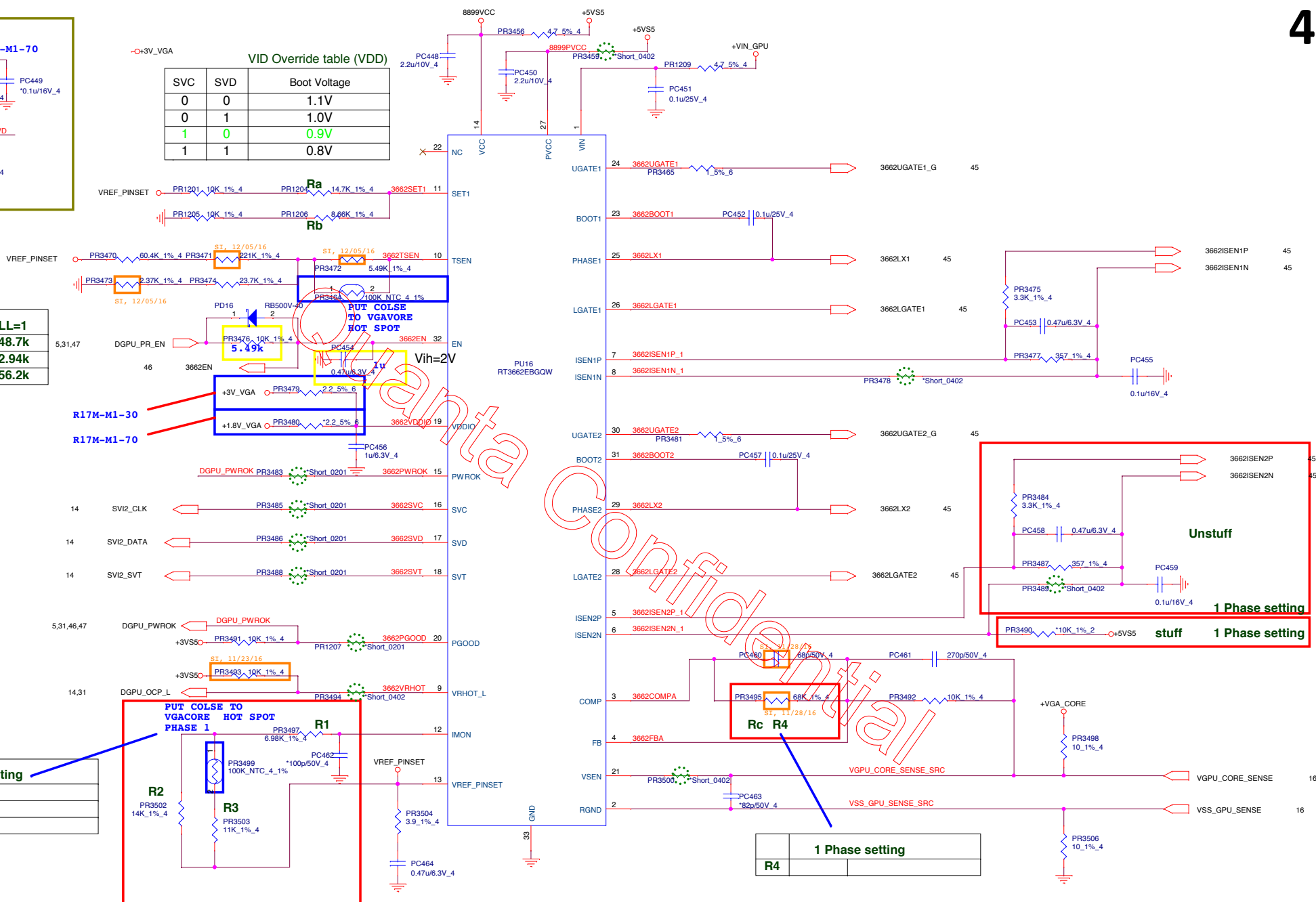
PROJECT : Rams 0P2/0P2A
Qanta Computer Inc.

Size Custom Document Number Load switch IC (APL3523A) Rev 1A
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SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

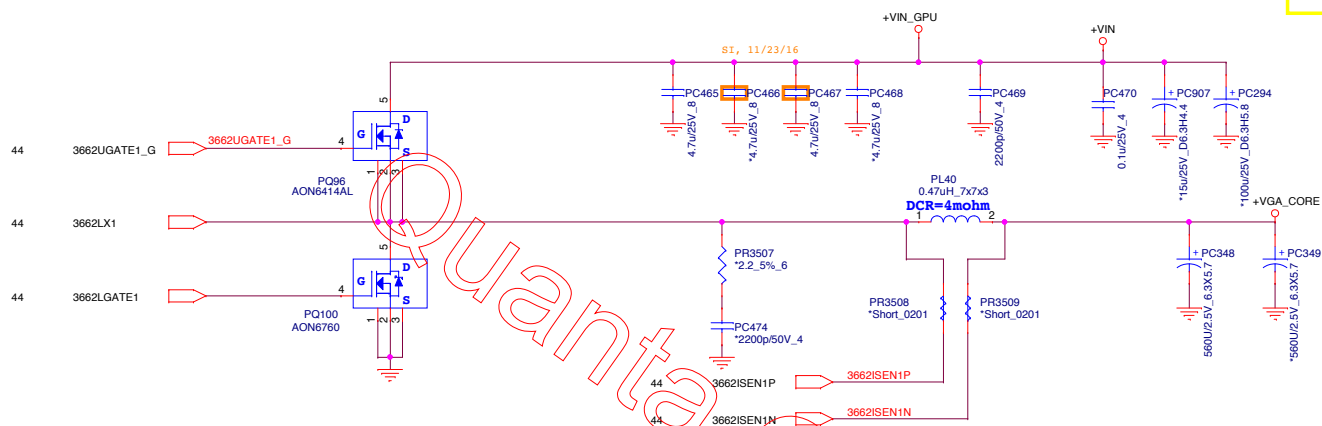
	LL=0	LL=1
Ra	14.7k	48.7k
Rb	8.66k	2.94k
Rc	27.4k	56.2k



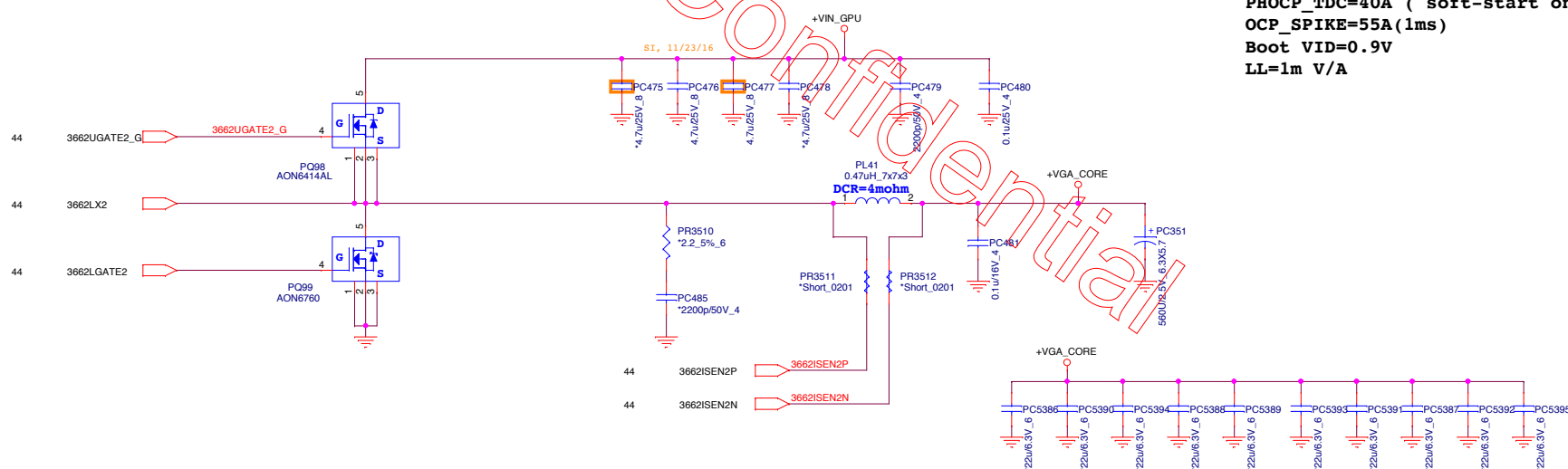
	1 Phase setting	
R1		
R2		
R3		

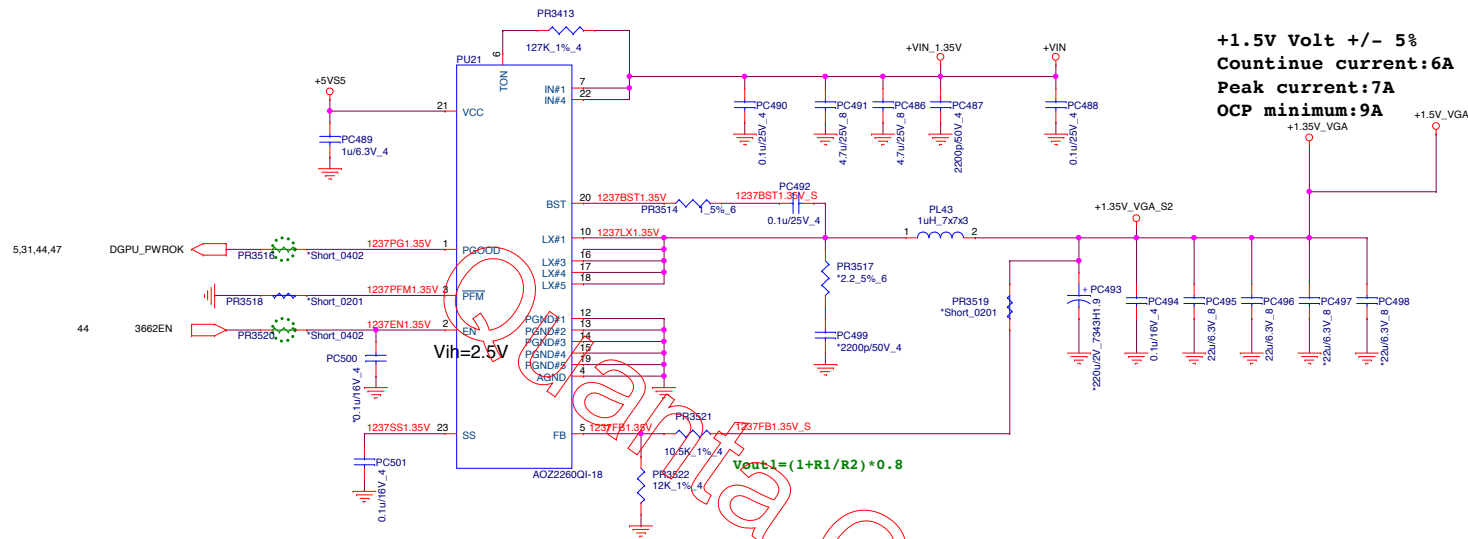
	1 Phase setting	
R4		

Default M1-30
 VGACORE (R17M-M1-30_18W/25W(1ms))
Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=0m V/A

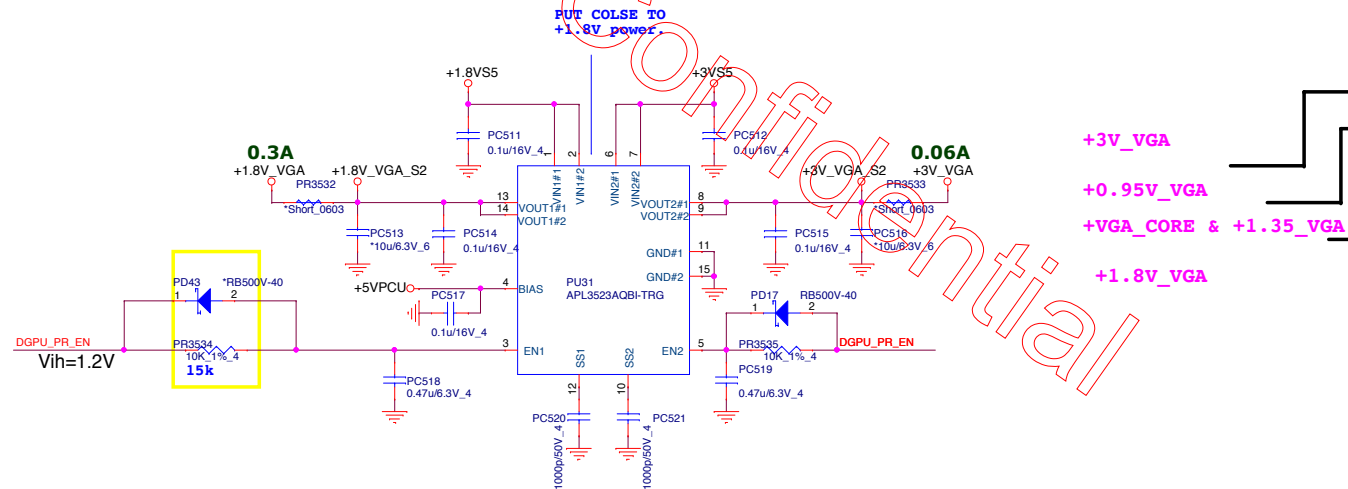
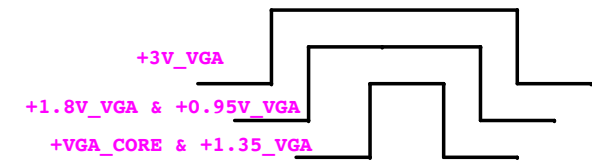
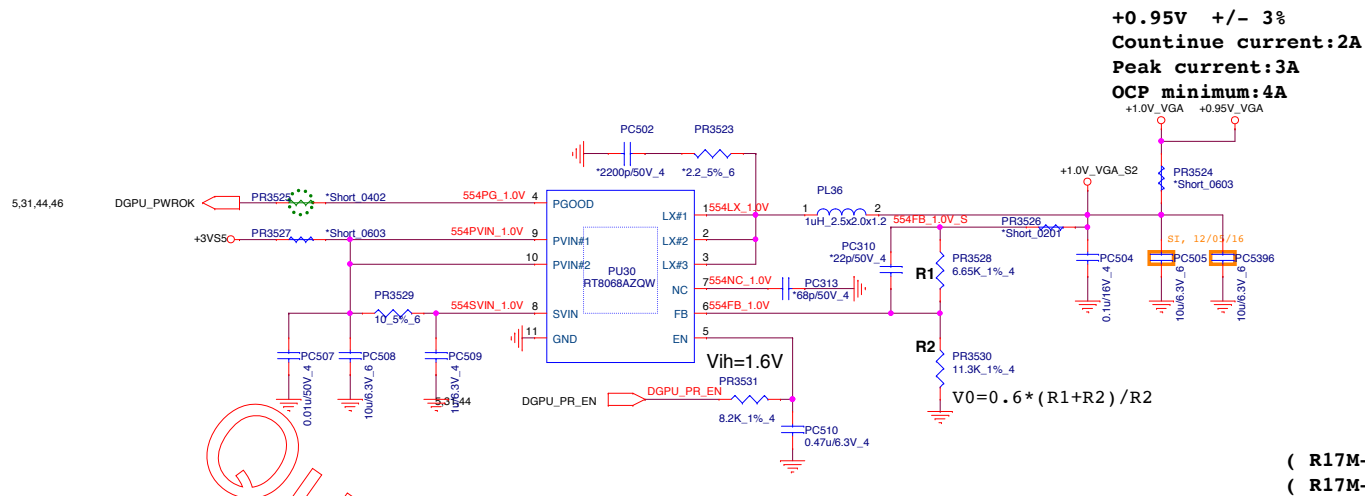


VGACORE (R17M-M1-70_25W/38W(1ms))
Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=1m V/A






Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



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 NB5	PROJECT : Rams OP2/OP2A Quanta Computer Inc.		
	Size Custom	Document Number Storage Mode/NA	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 48 of 48		