Hadley14" Schematics Document

Haswell ULT

2013-08-14
REV : A00

DY : None Installed

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
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Hadley 14 Block Diagram

Project code : 91.46L01.001
PCB P/N : 12310
Revision : SB

14" eDP LCD
FHD(1920 x 1080)
HD(1366 x 768) 52

HDMI CONN 54

HDMI Repeater
Prade
PS8171C 54

USB 3.0 / Power share 34

USB PowerShare
PERICOM
PI5USB1458AZAEX 35

USB 3.0 CONN 34

USB3.0 Redriver
TI
SN65LVPE502ARGER 34

SD Card Connector
(SD, SDHC,
SDXC w/ UHS) 33

CardReader
Realtek
RTS5227E 32

Internal Digital MIC
Universal Jack

Audio Codec
Realtek
ALC3223 27

2CH SPEAKER
1W , 8ohm / channel

Tweeter SPEAKER
0.5W , 8ohm

AMP 28

eDP
HDMI
HDMI
USB 2.0
USB 2.0
USB 3.0
USB 2.0
USB 3.0
USB 3.0
PCIE
HDA

Intel CPU
Haswell ULT
15W

Lynx Point-LP
8 USB 2.0/1.1 ports
2-4 USB 3.0 ports
High Definition Audio
4 SATA ports
8-12 PCIE ports
LPC I/F
ACPI 4.0a

DDR3L Channel A
DDR3L Channel B
PCI-E
USB 2.0
SATA3
USB 2.0
USB 2.0
SATA3
SATA3
SPI
SPI
LPC
SMBus
PS2
SMBus

DDR3L 1600 Memory Down 1
4GB (4*16*512M) 12

DDR3L 1600 Memory Down 2
4GB (4*16*512M) 13

Mini-Card
802.11a/b/g/n
BT 58

Mini-Card
mSATA 60

Touch Screen 52

Camera 52

SATA Repeater
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SN75LVCP601 56

HDD Board

LPC debug port 65

Flash ROM
8MB 25

KBC
Nuvoton
PCE985PA0BX (BGA) 24

PWM Fan1
Module 26

PWM Fan2
Module 26

Touch
Pad 62

Int.
KB (Backlight Option) 62

Thermal
Nuvoton
NCT7718W 26

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_CHARGER 3D3V_PWR

CPU DC/DC MAX15567 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT9025 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0

SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51367 & TPS51206 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

Switches 36	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0 3D3V_S5_PCH

PCB LAYER
L1 : TOP
L2 : GND
L3 : Signal
L4 : GND
L5 : Signal
L6 : Signal
L7 : GND
L8 : Signal
L9 : GND
L10 : Bottom

<Core Design>

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(Blanking)

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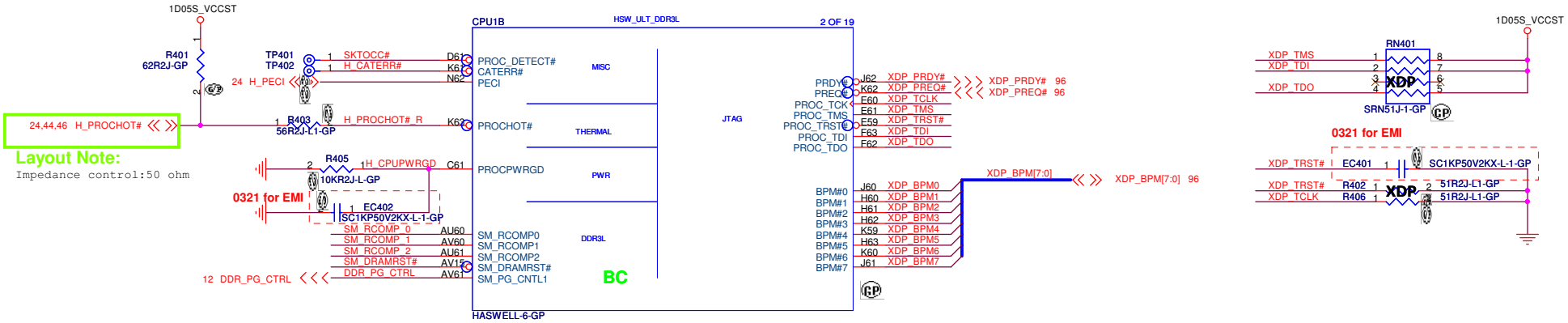
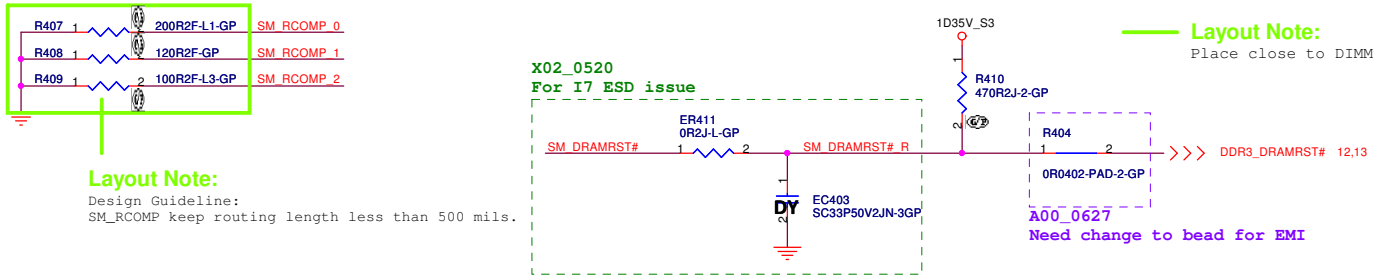
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Hadley 14"*	*A00*

Date: Wednesday, August 14, 2013 Sheet 3 of 107

SSID = CPU





<Core Design>

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Title: CPU (THERMAL/CLOCK)

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 4 of 107

SSID = CPU

<core_design>

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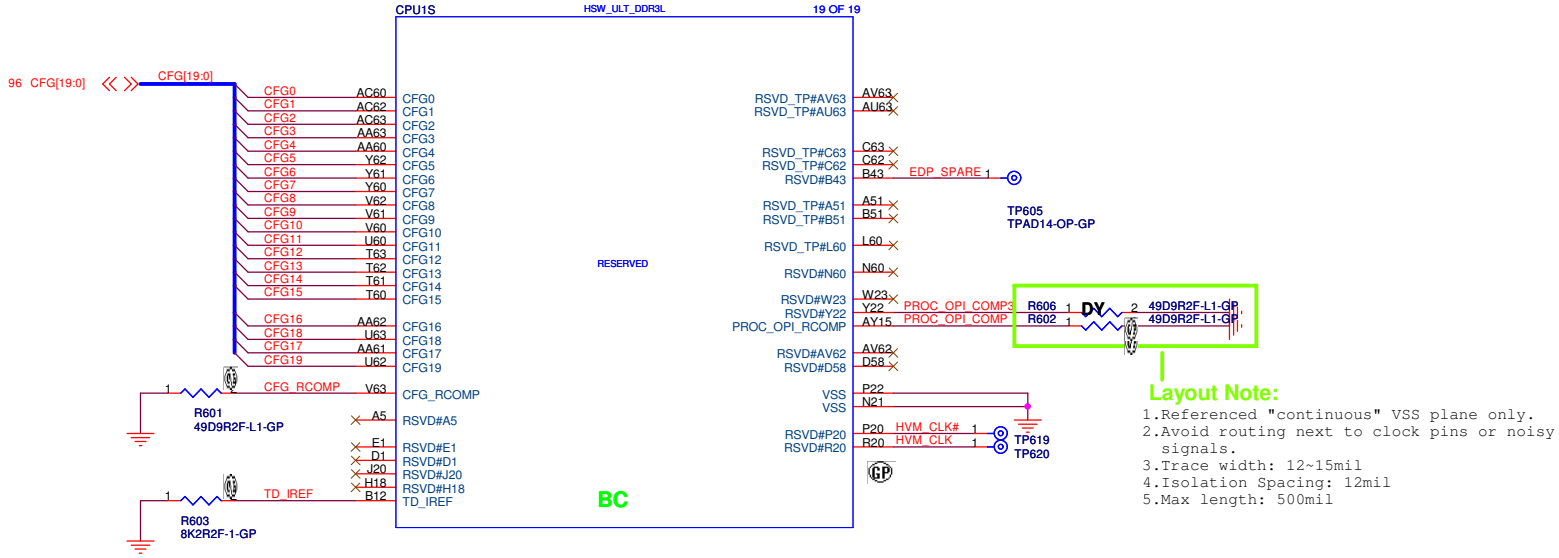
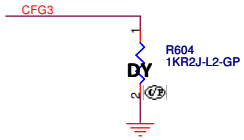
Title: CPU (DDR)		
Size: Custom	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 5 of 107	
</core_design>

SSID = CPU

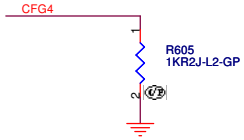


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>

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Title: CPU (RESERVED)

Size: A3 | Document Number: Hadley 14" | Rev: A00

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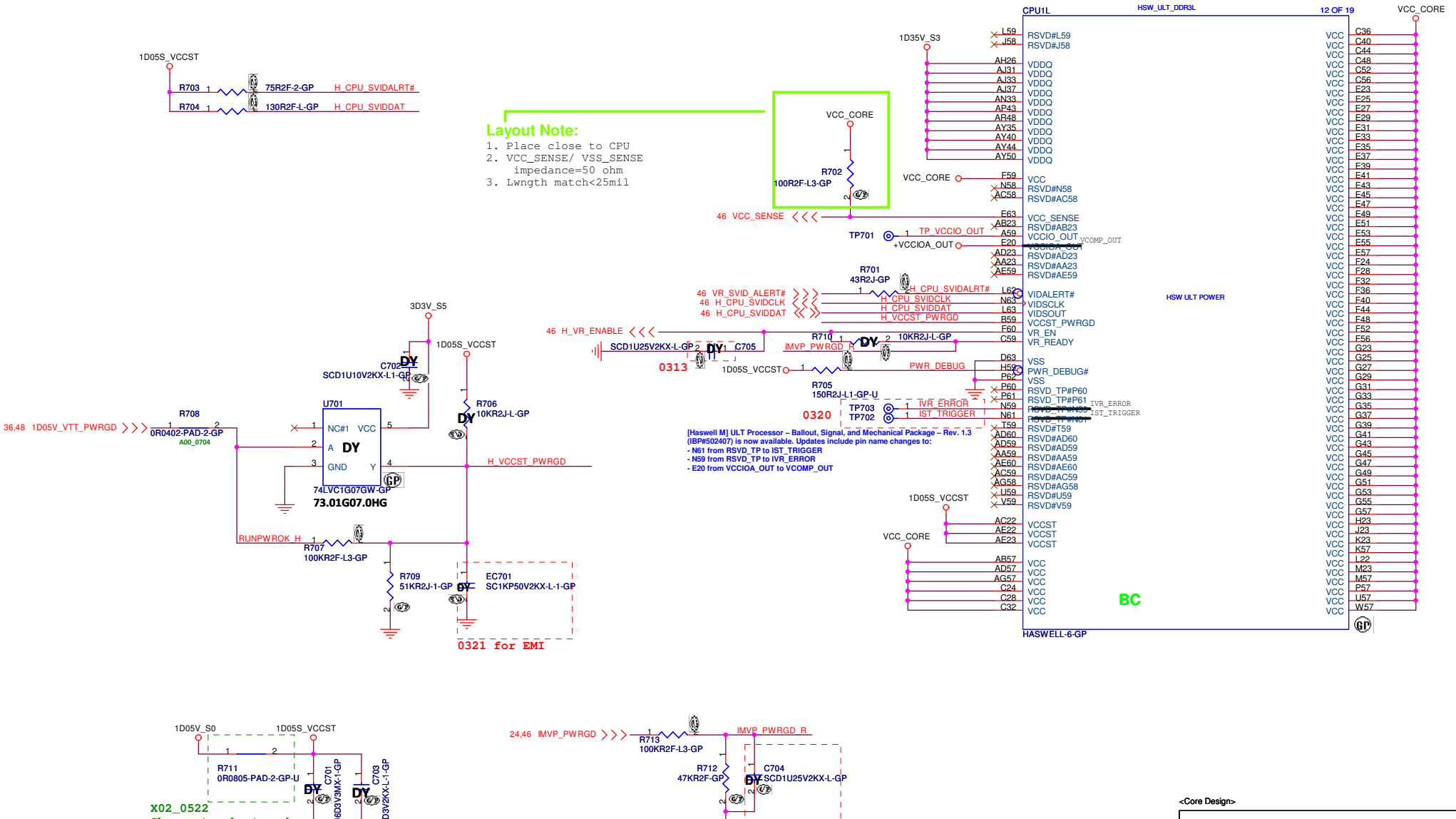
SSID = CPU



<core_design>

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Title: CPU (VCC_CORE)		
Size: A3	Document Number: Hadley 14"	Rev: A00
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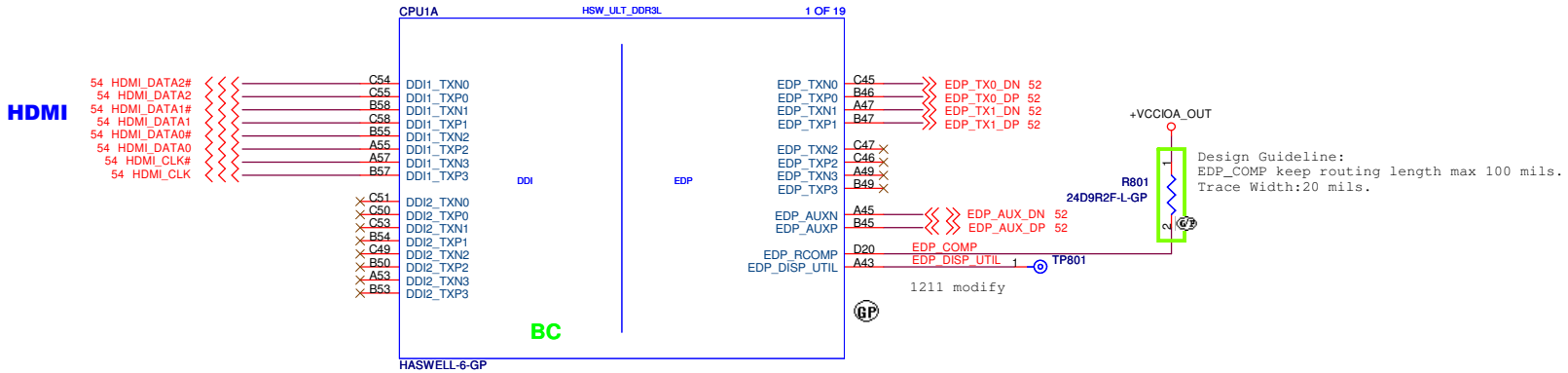
</core_design>

SSID = CPU



<Core Design>

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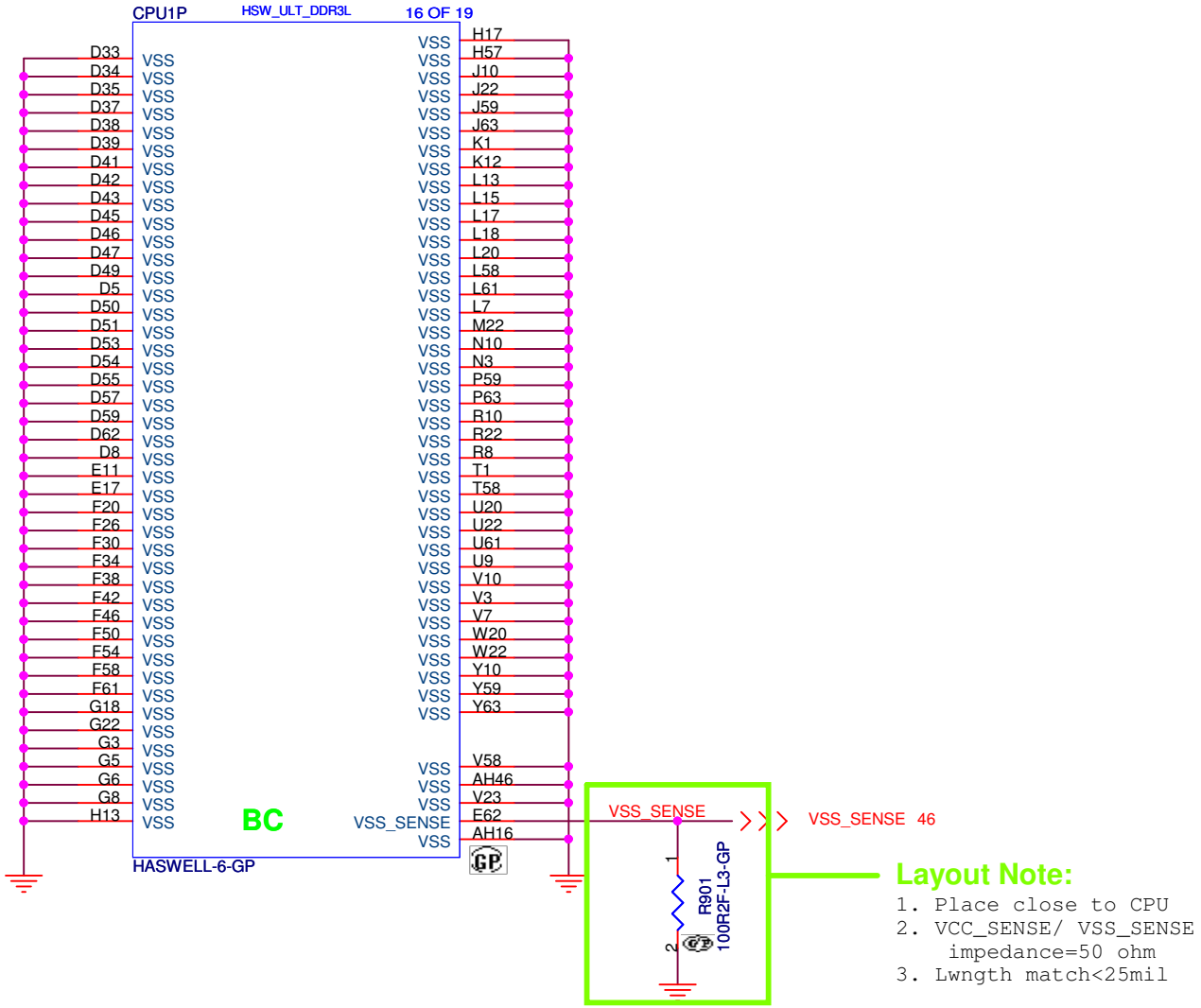
Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 8 of 107

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil

<Core Design>

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	***Hadley 14"***	***A00***

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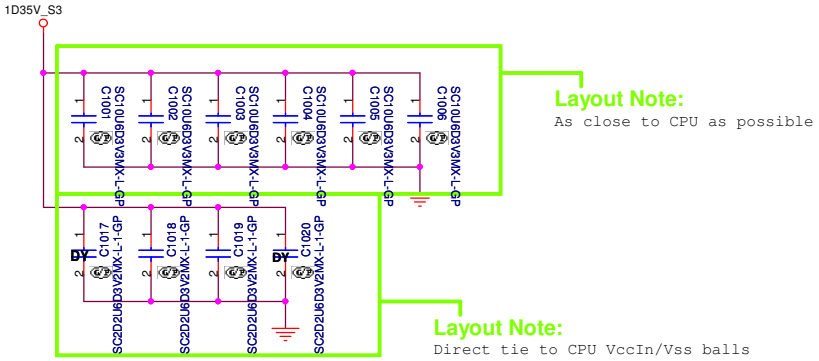
SSID = CPU



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Title	CPU(Power CAP1)	
Size: A3	Document Number: Hadley 14"	Rev: A00
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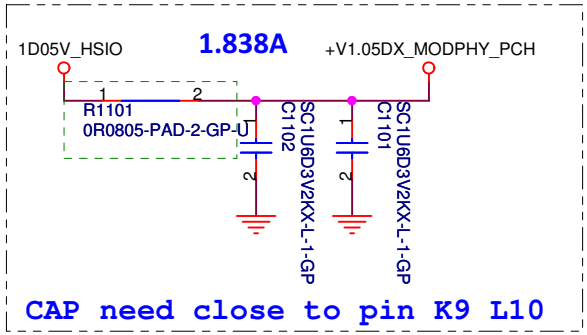
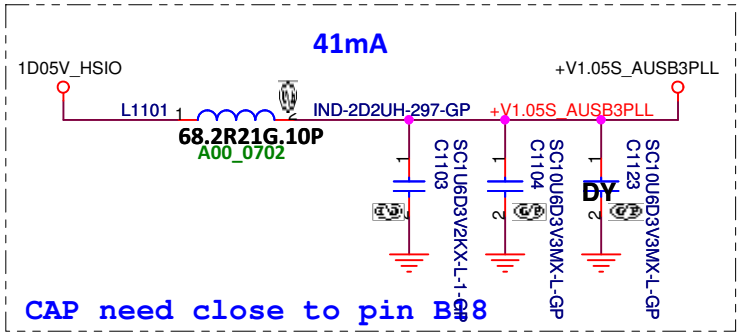
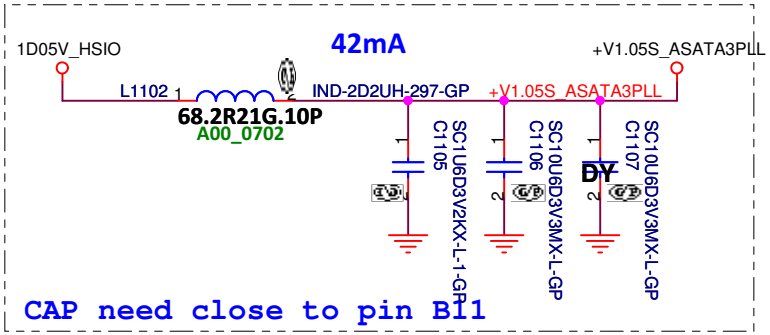
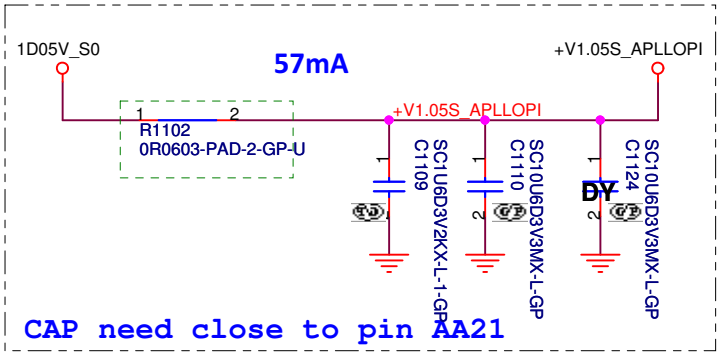
SSID = CPU

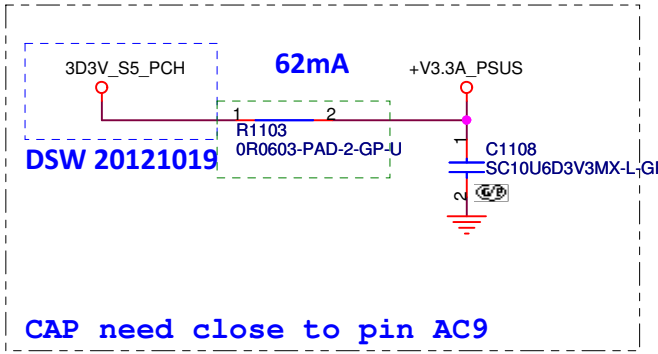
MAX: 1.92A

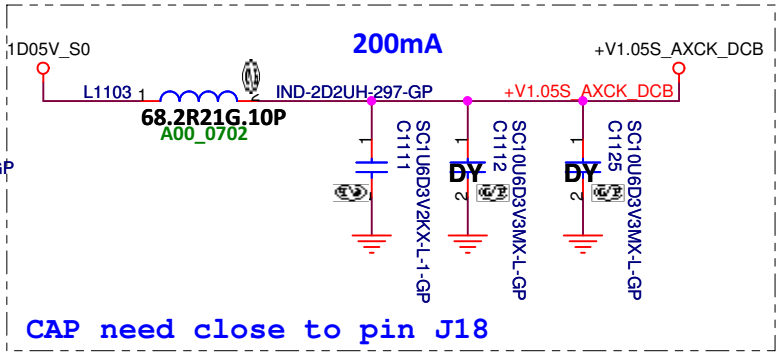


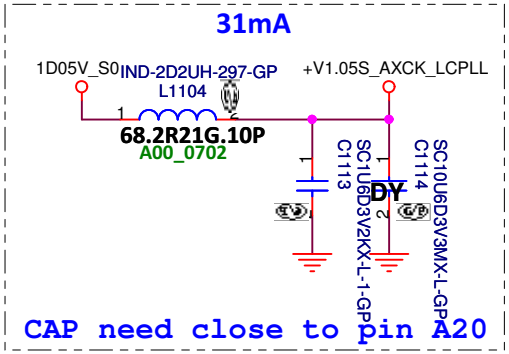


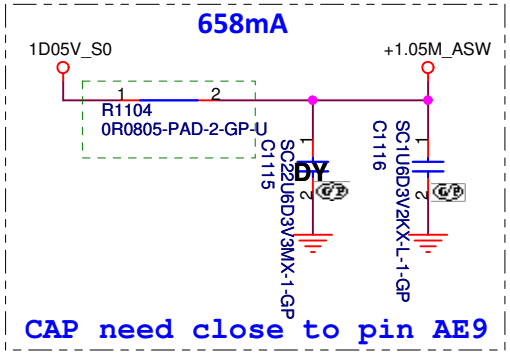


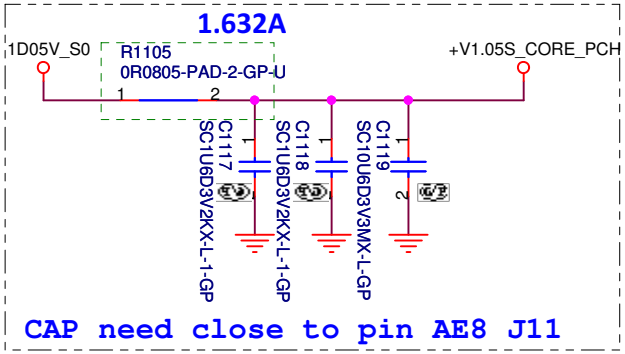


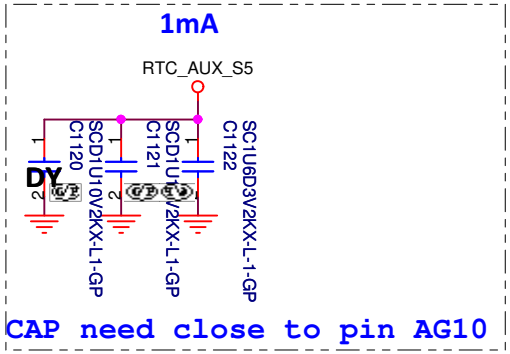












X02_0522
Change R1101~ R1105 to short pad

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Title	CPU(Power CAP2)	
Size A4	Document Number Hadley 14"	Rev A00
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SSID = MEMORY

DDR3L Channel-A Termination

CRB WhiteTip Mountain2 U4E2

CRB WhiteTip Mountain2 U4E1

CRB WhiteTip Mountain2 U5E2

CRB WhiteTip Mountain2 U5E1

DIMM Vref Filter Caps

0920 PDG1.0 change

X02_0522
Change to short pad

Q1402 Need check Vth=1V

84.00301.A31

Layout Note:
Place Close SO-DIMMA.

Intel CRB
10uF 0603: 4/6
470uF: 1/1

Hadley14
10uF 0402: 4/6
330uF: 0/1

Intel CRB
1uF 0402: 12/24

Hadley14
1uF 0201: 12/24

Intel CRB
10uF 0805: 1/2
1uF 0402: 4/8

Hadley14
10uF 0402: 1/2
1uF 0201: 4/8

<Core Design>

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Title: DDR3L-Memorydown1

Size: A2 | Document Number: Hadley 14" | Rev: A00

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SSID = MEMORY

5 M_B_A[15:0]
5 M_B_DQ[63:0]
5 M_B_DQS#[7:0]
5 M_B_DQS[7:0]

DDR3L Channel-B Termination

0D675V_S0

R1301 1	34D8R2F-GP	M_B_A0
R1302 1	34D8R2F-GP	M_B_A1
R1303 1	34D8R2F-GP	M_B_A2
R1304 1	34D8R2F-GP	M_B_A3
R1305 1	34D8R2F-GP	M_B_A4
R1306 1	34D8R2F-GP	M_B_A5
R1307 1	34D8R2F-GP	M_B_A6
R1309 1	34D8R2F-GP	M_B_A7
R1311 1	34D8R2F-GP	M_B_A8
R1313 1	34D8R2F-GP	M_B_A9
R1314 1	34D8R2F-GP	M_B_A10
R1315 1	34D8R2F-GP	M_B_A11
R1316 1	34D8R2F-GP	M_B_A12
R1317 1	34D8R2F-GP	M_B_A13
R1318 1	34D8R2F-GP	M_B_A14
R1319 1	34D8R2F-GP	M_B_A15
R1320 1	34D8R2F-GP	M_B_DIMB_CS#0
R1321 1	34D8R2F-GP	M_B_DIMB_CKE0
R1323 1	34D8R2F-GP	M_B_CAS#
R1324 1	34D8R2F-GP	M_B_RAS#
R1325 1	34D8R2F-GP	M_B_WE#
R1326 1	34D8R2F-GP	M_B_BS0
R1327 1	34D8R2F-GP	M_B_BS1
R1328 1	34D8R2F-GP	M_B_BS2

1D35V_S3

R1322 1	30R2J-1-GP	M_B_DIMB_ODT0

0D675V_S0

R1308 1	26D1R2F-GP	M_B_DIMB_CLK_DDR0
R1310 1	26D1R2F-GP	M_B_DIMB_CLK_DDR#0

0D675V_S0

R1329 1	34D8R2F-GP	M_B_DIMB_CS#1
R1330 1	34D8R2F-GP	M_B_DIMB_CKE1

CRB WhiteTip Mountain2 U6E1

1D35V_S3 — RAM6

M_VREF_DQ_DIMMB, M_VREF_CA_DIMMB — VRAM_CH_B_ZQ_1 — R1312 240R1F-GP

M_B_A[0:15] → A0–A14, A10/AP, A12/BC#

M_B_BS0, M_B_BS1, M_B_BS2 → BA0, BA1, BA2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0 → CK, CK#

5 M_B_DIMB_CKE0 → CKE

M_B_DQ[63:0] → DQ0–DQ63

M_B_DQS[7:0], M_B_DQS#[7:0] → UDQS, UDQS#, LDQS, LDQS#

M_B_DIMB_ODT0 → ODT

M_B_DIMB_CS#0 5, DDR3_DRAMRST# 4,12 → CS#, RESET#

M_B_A15 — NC#M7, NC#L9, NC#L1, NC#J9, NC#J1 — VRAM_CH_B_ZQT_1 — M_B_DIMB_CS#1 5, M_B_DIMB_CKE1 5, M_B_DIMB_CKE1, M_B_DIMB_ODT0 — R1334 240R1F-GP

5 M_B_BS0, 5 M_B_BS1, 5 M_B_BS2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0

5 M_B_DIMB_CKE0

5 M_B_WE#, 5 M_B_CAS#, 5 M_B_RAS#

UDM, LDM

VDD, VDDQ, VSS, VSSQ

BC

H5TC4G63AFR-PBA-1-GP-U

72.05463.F0U

0318

L GROUP / U GROUP / U GROUP / L GROUP

CRB WhiteTip Mountain2 U6E2

1D35V_S3 — RAM5

M_VREF_DQ_DIMMB, M_VREF_CA_DIMMB — VRAM_CH_B_ZQ_2 — R1332 240R1F-GP

M_B_A[0:15] → A0–A14, A10/AP, A12/BC#

M_B_BS0, M_B_BS1, M_B_BS2 → BA0, BA1, BA2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0 → CK, CK#

5 M_B_DIMB_CKE0 → CKE

M_B_DQ[63:0] → DQ0–DQ63

M_B_DQS[7:0], M_B_DQS#[7:0] → UDQS, UDQS#, LDQS, LDQS#

M_B_DIMB_ODT0 → ODT

M_B_DIMB_CS#0 5, DDR3_DRAMRST# 4,12 → CS#, RESET#

M_B_A15 — NC#M7, NC#L9, NC#L1, NC#J9, NC#J1 — VRAM_CH_B_ZQT_2 — M_B_DIMB_CS#1, M_B_DIMB_CKE1, M_B_DIMB_ODT0 — R1335 240R1F-GP

5 M_B_BS0, 5 M_B_BS1, 5 M_B_BS2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0

5 M_B_DIMB_CKE0

5 M_B_WE#, 5 M_B_CAS#, 5 M_B_RAS#

UDM, LDM

VDD, VDDQ, VSS, VSSQ

BC

H5TC4G63AFR-PBA-1-GP-U

72.05463.F0U

0318

L GROUP / U GROUP / U GROUP / L GROUP

CRB WhiteTip Mountain2 U7E1

1D35V_S3 — RAM8

M_VREF_DQ_DIMMB, M_VREF_CA_DIMMB — VRAM_CH_B_ZQ_3 — R1333 240R1F-GP

M_B_A[0:15] → A0–A14, A10/AP, A12/BC#

M_B_BS0, M_B_BS1, M_B_BS2 → BA0, BA1, BA2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0 → CK, CK#

5 M_B_DIMB_CKE0 → CKE

M_B_DQ[63:0] → DQ0–DQ63

M_B_DQS[7:0], M_B_DQS#[7:0] → UDQS, UDQS#, LDQS, LDQS#

M_B_DIMB_ODT0 → ODT

M_B_DIMB_CS#0 5, DDR3_DRAMRST# 4,12 → CS#, RESET#

M_B_A15 — NC#M7, NC#L9, NC#L1, NC#J9, NC#J1 — VRAM_CH_B_ZQT_3 — M_B_DIMB_CS#1, M_B_DIMB_CKE1, M_B_DIMB_ODT0 — R1336 240R1F-GP

5 M_B_BS0, 5 M_B_BS1, 5 M_B_BS2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0

5 M_B_DIMB_CKE0

5 M_B_WE#, 5 M_B_CAS#, 5 M_B_RAS#

UDM, LDM

VDD, VDDQ, VSS, VSSQ

BC

H5TC4G63AFR-PBA-1-GP-U

72.05463.F0U

0318

L GROUP / U GROUP / U GROUP / L GROUP

CRB WhiteTip Mountain2 U7E2

1D35V_S3 — RAM7

M_VREF_DQ_DIMMB, M_VREF_CA_DIMMB — VRAM_CH_B_ZQ_4 — R1331 240R1F-GP

M_B_A[0:15] → A0–A14, A10/AP, A12/BC#

M_B_BS0, M_B_BS1, M_B_BS2 → BA0, BA1, BA2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0 → CK, CK#

5 M_B_DIMB_CKE0 → CKE

M_B_DQ[63:0] → DQ0–DQ63

M_B_DQS[7:0], M_B_DQS#[7:0] → UDQS, UDQS#, LDQS, LDQS#

M_B_DIMB_ODT0 → ODT

M_B_DIMB_CS#0 5, DDR3_DRAMRST# 4,12 → CS#, RESET#

M_B_A15 — NC#M7, NC#L9, NC#L1, NC#J9, NC#J1 — VRAM_CH_B_ZQT_4 — M_B_DIMB_CS#1, M_B_DIMB_CKE1, M_B_DIMB_ODT0 — R1337 240R1F-GP

5 M_B_BS0, 5 M_B_BS1, 5 M_B_BS2

5 M_B_DIMB_CLK_DDR0, 5 M_B_DIMB_CLK_DDR#0

5 M_B_DIMB_CKE0

5 M_B_WE#, 5 M_B_CAS#, 5 M_B_RAS#

UDM, LDM

VDD, VDDQ, VSS, VSSQ

BC

H5TC4G63AFR-PBA-1-GP-U

72.05463.F0U

0318

L GROUP / U GROUP / U GROUP / L GROUP

DIMM Vref Filter Caps

M_VREF_CA_DIMMB — C1301, C1302, C1303, C1304 — SC2004U7U0X2KX-2GP

M_VREF_DQ_DIMMB — C1305, C1306, C1307, C1308 — SC2004U7U0X2KX-2GP

0920 PDG1.0 change

Layout Note:

Place Close SO-DIMMA.

5 DDR_WR_VREF02

1D35V_S3 — R1341 1K8R2F-GP — DY — R1343 0R2J-L-GP — 0D675V_VTTREF

R1339 5D1R2F-GP — M_VREF_DQ_DIMMB_R — R1340 0R0402-PAD-2-GP — M_VREF_DQ_DIMMB

C1333 SCD022U16V2JX-GP — +V_VREF_PATH2 — R1338 1K8R2F-GP

R1342 24D9R2F-L-GP

SODIMM B DECOUPLING

Intel CRB 10uF 0603: 4/6

Hadley14 10uF 0402: 4/6

Intel CRB 1uF 0402: 12/24

Hadley14 1uF 0201: 12/24

Layout Note:

Place these Caps near SO-DIMMB.

1D35V_S3 — C1307, C1311, C1312, C1313, C1314, C1315, C1316, C1317, C1318, C1319, C1320, C1321, C1322, C1323, C1324, C1325, C1326, C1327, C1328, C1329, C1330, C1331, C1332, C1333, C1334, C1335, C1336, C1337 — SC1U6D3V2MX-GP / SC1U6D3V2MX-GP-U — DY

1D35V_S3 — C1309, C1310, C1338, C1339, C1340, C1341, C1342, C1343, C1344, C1345, C1346, C1347, C1348, C1349, C1350, C1351, C1352, C1353, C1354, C1355, C1356, C1357, C1358, C1359, C1360, C1361, C1362, C1363, C1364, C1365, C1366, C1367, C1368, C1369, C1370, C1371, C1372, C1373, C1374, C1375, C1376, C1377, C1378, C1379, C1380, C1381, C1382, C1383, C1384, C1385, C1386, C1387, C1388, C1389, C1390, C1391, C1392, C1393, C1394, C1395, C1396, C1397, C1398, C1399, C1400, C1401, C1402, C1403, C1404, C1405, C1406, C1407, C1408, C1409, C1410, C1411, C1412, C1413, C1414, C1415, C1416, C1417, C1418, C1419, C1420, C1421, C1422, C1423, C1424, C1425, C1426, C1427, C1428, C1429, C1430, C1431, C1432, C1433, C1434, C1435, C1436, C1437 — SC1U6D3V2MX-GP / SC1U6D3V2MX-GP-U — DY

Intel CRB 10uF 0805: 1/2 1uF 0402: 4/8

Hadley14 10uF 0402: 1/2 1uF 0201: 4/8

0D675V_S0 — C1438, C1439, C1440, C1441, C1442, C1443, C1444, C1445, C1446, C1447, C1448, C1449, C1450, C1451, C1452, C1453, C1454, C1455, C1456, C1457, C1458, C1459, C1460, C1461, C1462, C1463, C1464, C1465, C1466, C1467, C1468, C1469, C1470, C1471, C1472, C1473, C1474, C1475, C1476, C1477, C1478, C1479, C1480, C1481, C1482, C1483, C1484, C1485, C1486, C1487, C1488, C1489, C1490, C1491, C1492, C1493, C1494, C1495, C1496, C1497, C1498, C1499, C1500, C1501, C1502, C1503, C1504, C1505, C1506, C1507, C1508, C1509, C1510, C1511, C1512, C1513, C1514, C1515, C1516, C1517, C1518, C1519, C1520, C1521, C1522, C1523, C1524, C1525, C1526, C1527, C1528, C1529, C1530, C1531, C1532, C1533, C1534, C1535, C1536, C1537 — SC1U6D3V2MX-GP / SC1U6D3V2MX-GP-U — DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3L-Memorydown2

Size: A2 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 13 of 107

<Core Design>

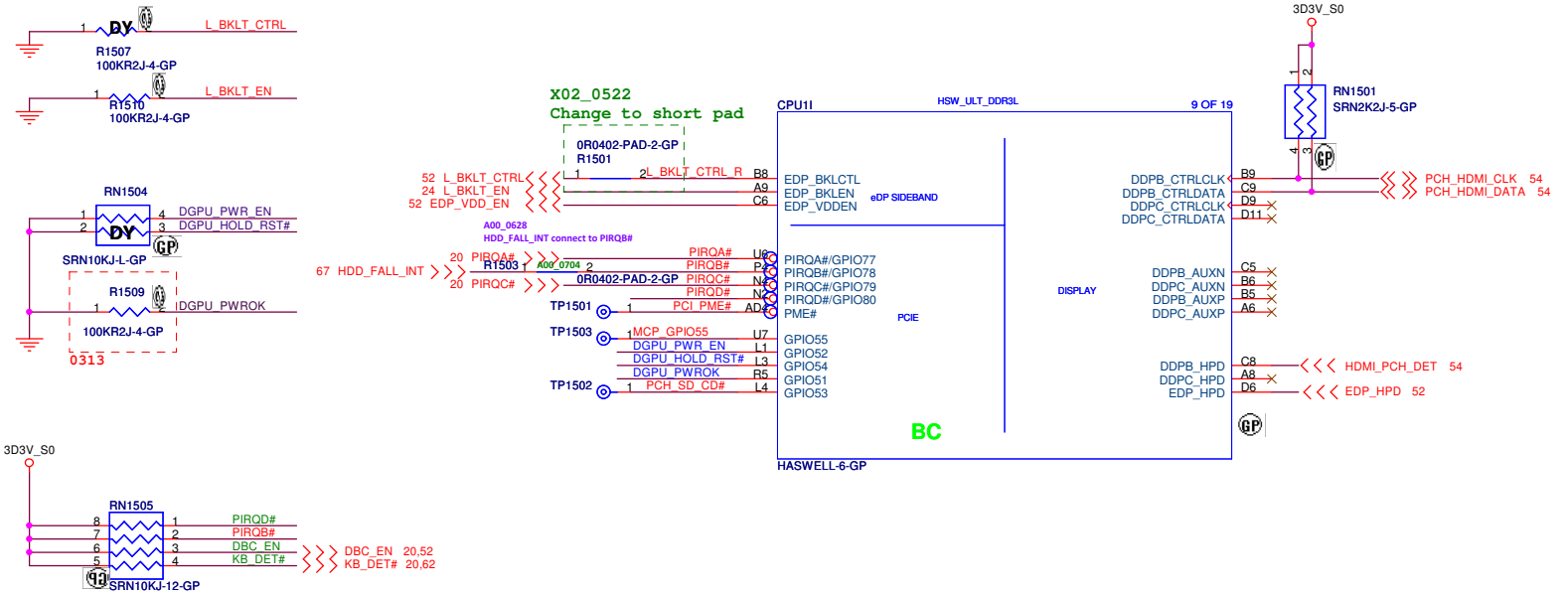
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M1&M3

Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 14 of 107

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (EDP SIDEBAND/GPIO/DDI)**

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 15 of 107

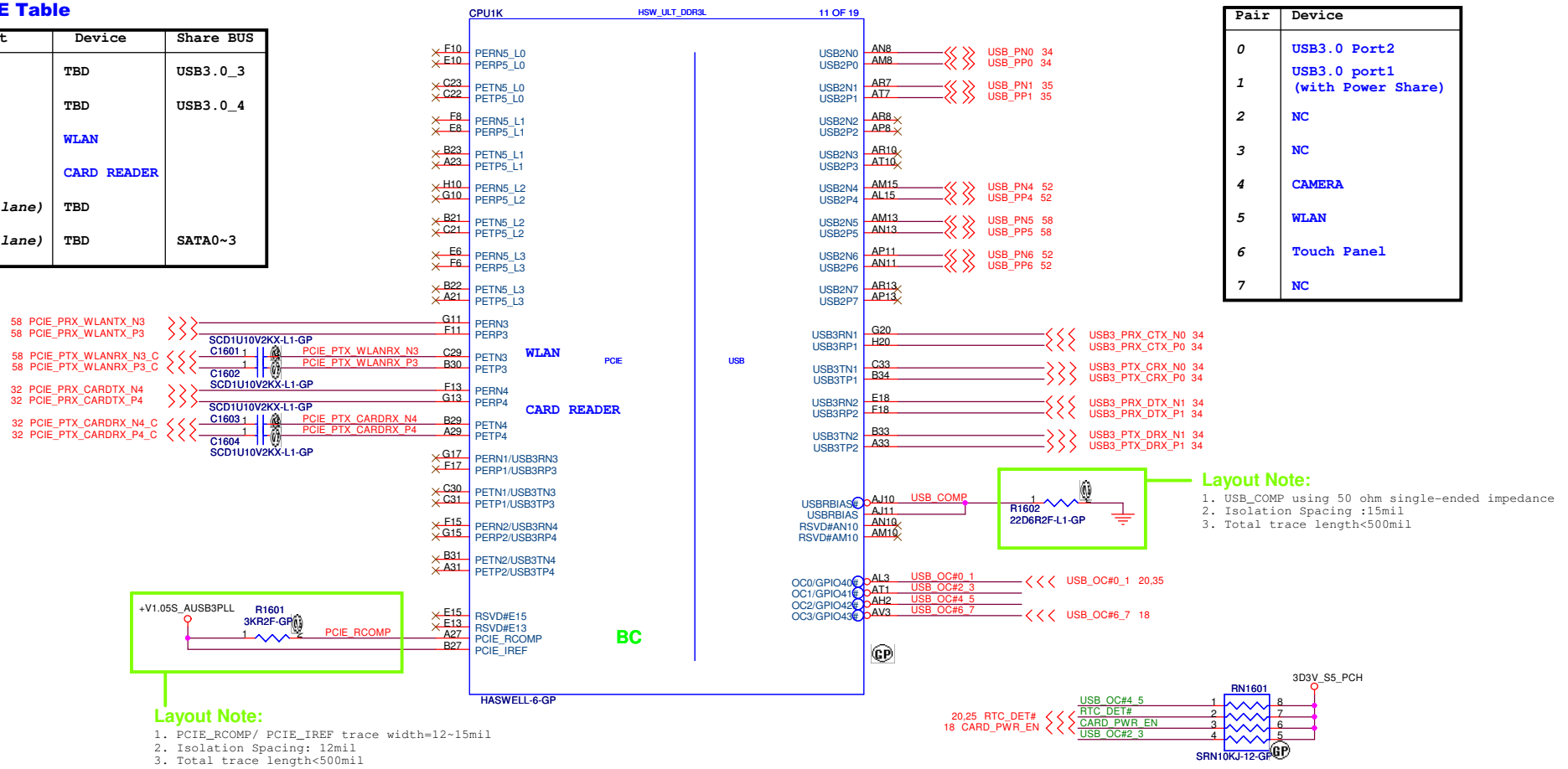
SSID = CPU

PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	CARD READER	
5(4lane)	TBD	
6(4lane)	TBD	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	NC
3	NC
4	CAMERA
5	WLAN
6	Touch Panel
7	NC



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/USB)

Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 16 of 107

SSID = CPU

PCH strap pin:

On Die DSW VR Enable	
DSWODVREN	Low = Disable High = Enable (default) *

R1717 2 DY 1 10KR2J-L-GP SYS_PWROK

RN1703 1 2 4 3 SRN10KJ-L-GP PM_PCH_PWROK PM_RSMRST#

R1720 330KR2J-L-GP RTC_AUX_S5

DSWODVREN 1 DY 2 R1721 330KR2J-L-GP

RN1704 3D3V_S0

PM_CLKRUN# XDP_DBRESET# SRN8K2J-6-GP

CPU1H HSW_ULT_DDR3L 8 OF 19

SYSTEM POWER MANAGEMENT

24,96 SYS_PWROK
24,26,36 PCH_PWROK
R1706 A00_0704 0R0402-PAD-2-GP
R1707 0R0402-PAD-2-GP

PM_SUSACK# XDP_DBRESET# SYS_PWROK PM_PCH_PWROK MPWROK PCI_PLTRST#

SUSACK# SYS_RESET# SYS_PWROK PCH_PWROK APWROK PLTRST#

24,96 PM_PWRBTN#
24 AC_PRESENT
48 PCH_SLP_S0#
TP1705

PM_RSMRST# PM_SUSWARN#_R PM_PWRBTN# AC_PRESENT BATLOW# PCH_SLP_S0# PCH_SLP_WLAN#

RSMRST# SUSWARN#/SUSPWRDNACK#/GPIO30 PWRBTN# ACPRESENT/GPIO31 BATLOW#/GPIO72 SLP_S0# SLP_WLAN#/GPIO29

BC

HASWELL-6-GP

DSWVRMEN DPWROK WAKE#

DSWODVREN PCH_DPWROK PCH_WAKE#

R1704 0R2J-L-GP A00_0708 DY R1705 1KR2J-L2-GP PM_RSMRST# 3D3V_S5

0313

CLKRUN#/GPIO32 SUS_STAT#/GPIO61 SUSCLK/GPIO62 SLP_S5#/GPIO63

PM_CLKRUN# PM_SUS_STAT# SUS_CLK PM_SLP_S5#

R1709 0R0402-PAD-2-GP TP1702 R1710 0R2J-L-GP TP1703

PM_CLKRUN#_EC 24
PCH_SUSCLK_KBC 24

SLP_S4# SLP_S3# SLP_A# SLP_SUS# SLP_LAN#

PM_SLP_S4# PM_SLP_S3# PM_SLP_A# PM_SLP_SUS# PM_SLP_LAN#

TP1704 TP1707

PM_SLP_S4# 24,49
PM_SLP_S3# 24,36,48,49,51
PM_SLP_SUS# 24,38

PCH_SUSCLK_KBC

EC1701 SC4D7P50V2CN-1GP

X02_0520
For I7 ESD issue

PM_PWRBTN# EC1707 SC220P50V2JN-1-GP

Layout Note:
Place near CPU

24,32,58,65 PLT_RST#
R1713 A00_0708 0R2J-L-GP PCI_PLTRST#
R1715 100KR2J-4-GP C1701 SC220P50V2KX-3GP

3D3V_S5 0313 RN1701 BATLOW# AC_PRESENT SRN10KJ-L-GP

24 PM_SUSACK#
24 PM_SUSWARN#
RN1702 A00_0708 0R4P2R-PAD PM_SUSACK#_R PM_SUSWARN#_R

PCH_DPWROK A00_0708 R1718 0R0402-PAD-2-GP KBC_DPWROK 24

R1725 100KR2F-L3-GP EC1706 SCD1U10V2KX-1-GP

Layout Note:
Place near R1725

X02_0520
For I7 ESD issue

3D3V_S5_PCH

R1724 DY PM_SUS_STAT# 10KR2J-L-GP
R1727 PM_SUSWARN# 10KR2J-L-GP

3D3V_AUX_S5

A00_0708 R1708 DY 100KR2J-4-GP
R1726 10KR2J-L-GP

0314 for EMI

EC1702 SC820P50V2KX-1GP DY R1702 1KR2J-L2-GP

Q1701 2N7002KDW-GP

3V_5V_POK#
PM_RSMRST#
3V_5V_POK_C R1728 0R2J-L-GP A00_0708

RSMRST#_KBC 24
3V_5V_POK 45

R1729 0R0402-PAD-2-GP A00_0708 PM_SLP_SUS#

84.2N702.A3F

X02_0520
For I7 ESD issue

XDP_DBRESET#
SYS_PWROK
PCI_PLTRST#
PCH_PWROK

EC1708 EC1703 EC1704 EC1705 SCD1U10V2KX-1-GP

Layout Note:
Place near cpu side

Layout Note:
Place near R1706

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (PM)		
Size: A3	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 17 of 107	

SSID = CPU

PCIE Mapping Table		
PCIE Port	PCIE CLK	REQ#
Port 3 WLAN	Port 2 WLAN	Port 2 WLAN
Port 4 CARD READER	Port 3 CARD READER	Port 3 CARD READER

0321

0321 for EMI

X02_0522
Change to short pad

X02_0522
Change R1807 to short pad

X02_0520
For I7 ESD issue

Layout Note:
Place near R1801

0315

0313

0329

<Core Design>

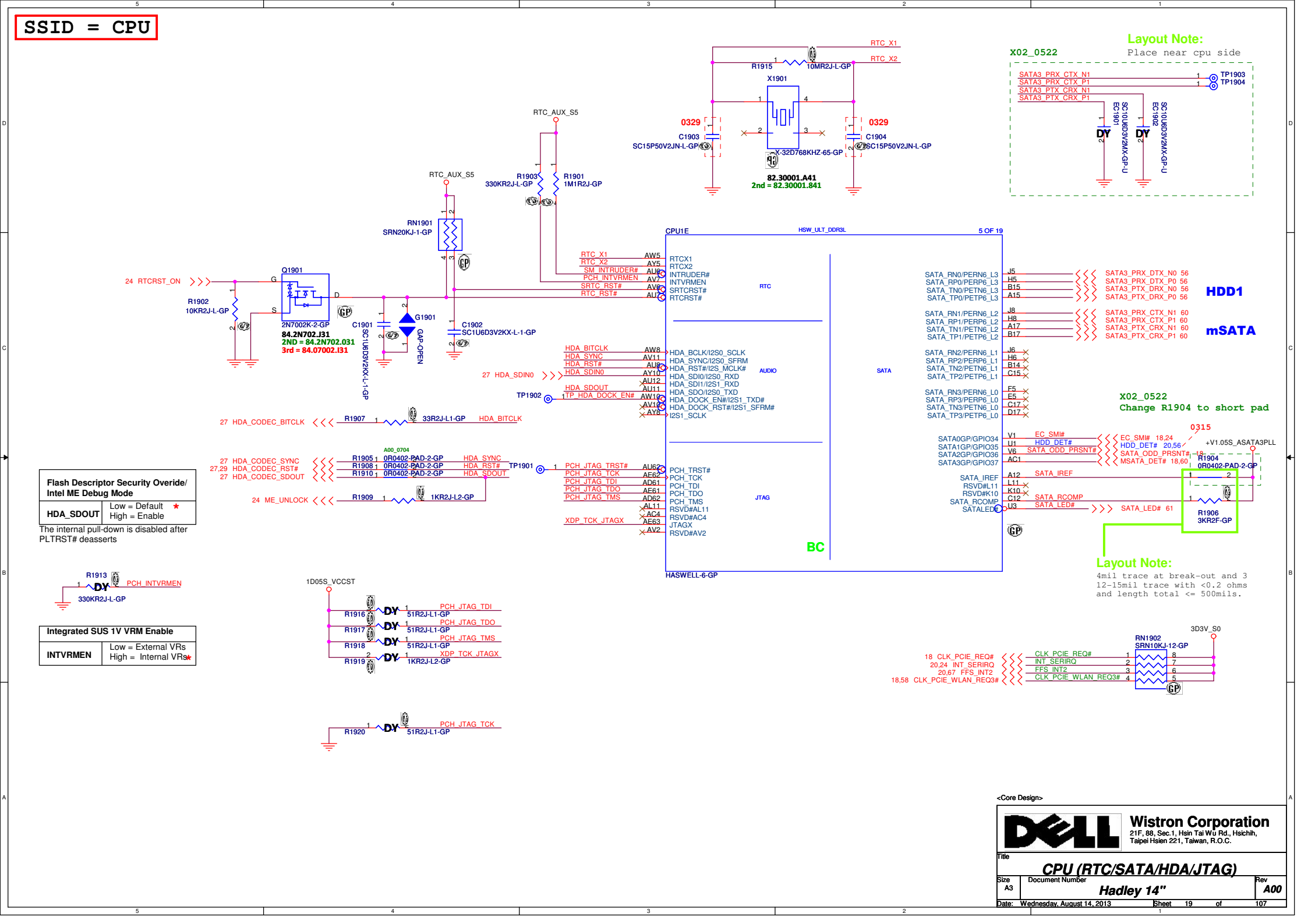
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SMB/LPC/SPI)

Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 18 of 107

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/SATA/HDA/JTAG)

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 19 of 107

SSID = CPU

SSI Memory Matrix Table

Vendor	Size	MS3 GPIO47	MS2 GPIO46	MS1 GPIO45	MS0 GPIO44
Hynix	4	0	0	0	0
Hynix	6	0	0	0	1
Hynix	8	0	0	1	0
Samsung	4	0	0	1	1
Samsung	6	0	1	0	0
Samsung	8	0	1	0	1
Micron	4	0	1	1	0
Micron	6	0	1	1	1
Micron	8	1	0	0	0
Hadley 15/17 SODIMM		1	1	1	1

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

it is for "A1" stepping.	
Top-Block Swap Override mode	
SDIO_D0 / GPIO66	*Low = Disable "Top-Block swap" mode (Default) High = Enable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	*Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

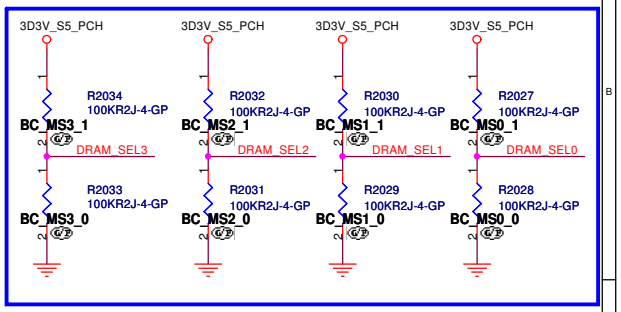
BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

Memory Matrix Define



<Core Design>

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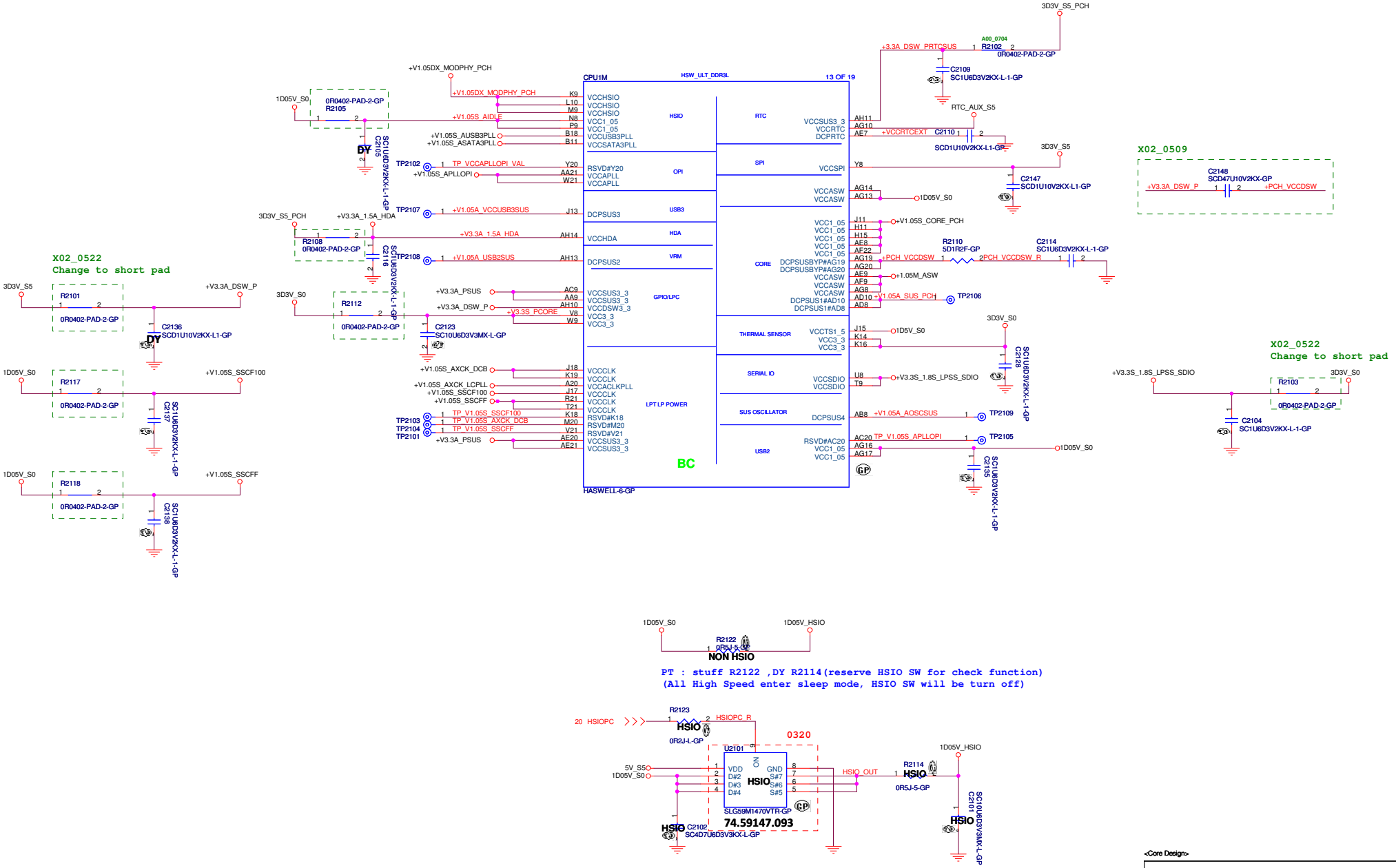
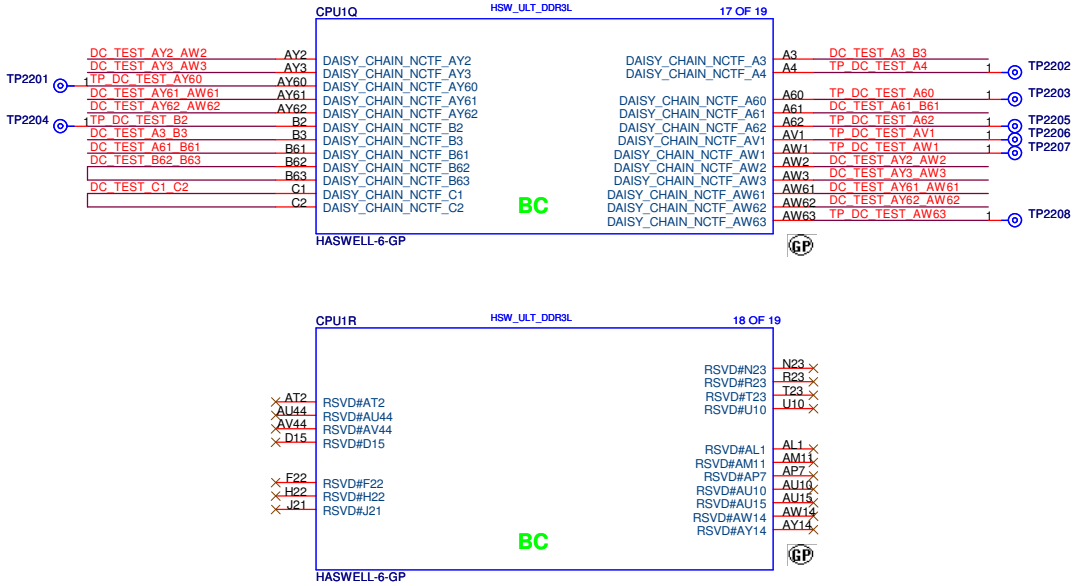
Title: CPU (GPIO)
Size: A3 | Document Number: Hadley 14" | Rev: A00
Date: Wednesday, August 14, 2013 | Sheet 20 of 107

SSID = CPU


CPU1M
HSW_ULT_DDR3L
13 OF 19
HASWELL-6-GP
BC
X02_0522
Change to short pad
X02_0509
NON HSIO
PT : stuff R2122 ,DY R2114(reserve HSIO SW for check function)
(All High Speed enter sleep mode, HSIO SW will be turn off)
0320
74.59147.093
SLG59M1470VTR-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (POWER2)
Hadley 14"
A00
Wednesday, August 14, 2013
Sheet 21 of 107

SSID = CPU



<Core Design>

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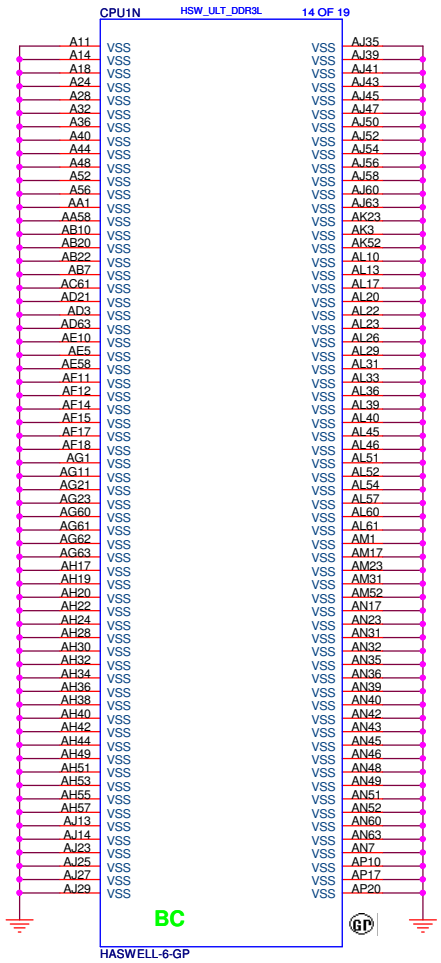
Taipei Hsien 221, Taiwan, R.O.C.

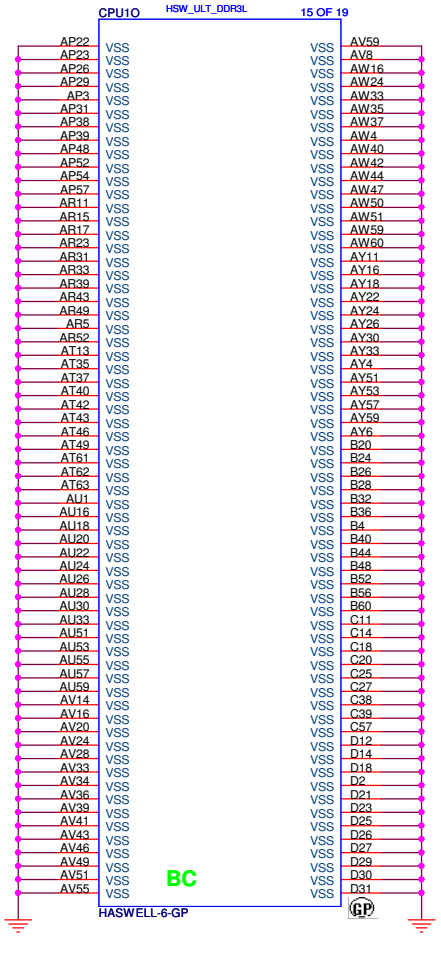
Title: RSVD

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 22 of 107

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	***Hadley 14"***	***A00***

Date: Wednesday, August 14, 2013 Sheet 23 of 107

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
UMA/eDP	100.0K	10.0K(64.10025.6DL)	3.0V
TBD	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
TBD	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
TBD	100.0K	49.9K(64.49925.6DL)	2.201V
TBD	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

X02_0522 Change to short pad

X02_0520 For I7 ESD issue

Layout Note: Need very close to EC

Layout Note: Place near KBC

Layout Note: Need very close to EC 1203 R2419,20,22 change to 0R

Layout Note: Need very close to EC C2422 PDG is 47p

Layout Note: Connect GND and AGND planes via either 0R resistor or connect directly.

Layout Note: Design Guide: The purpose of the capacitor, C, in the topology following figure is to mitigate the undershoots on the PROCHOT# signal.

Charger / PCH/thermal / TP

Power Switch Logic(PSL)

AOAC Ambient temperature detect

EC_GPIO47 High Active

Update P/N to Version B : 71.00985.A0U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

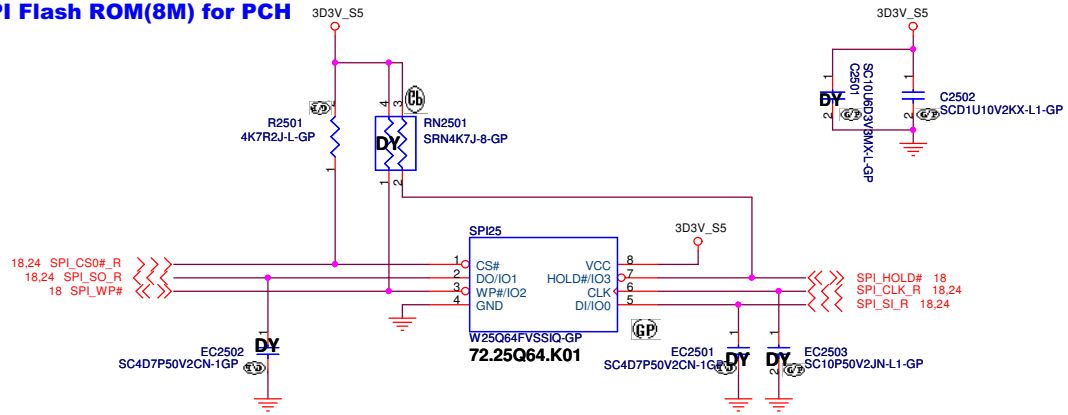
Title: KBC Nuvoton NPCE985

Size: A2 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 24 of 107

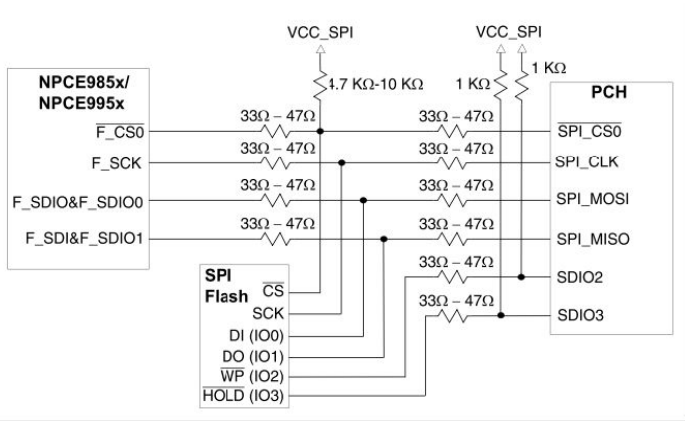
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



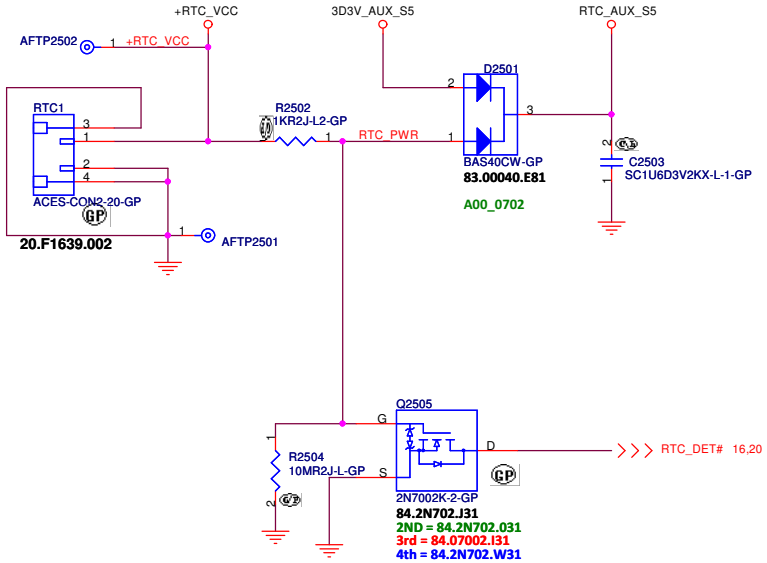
0313

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT

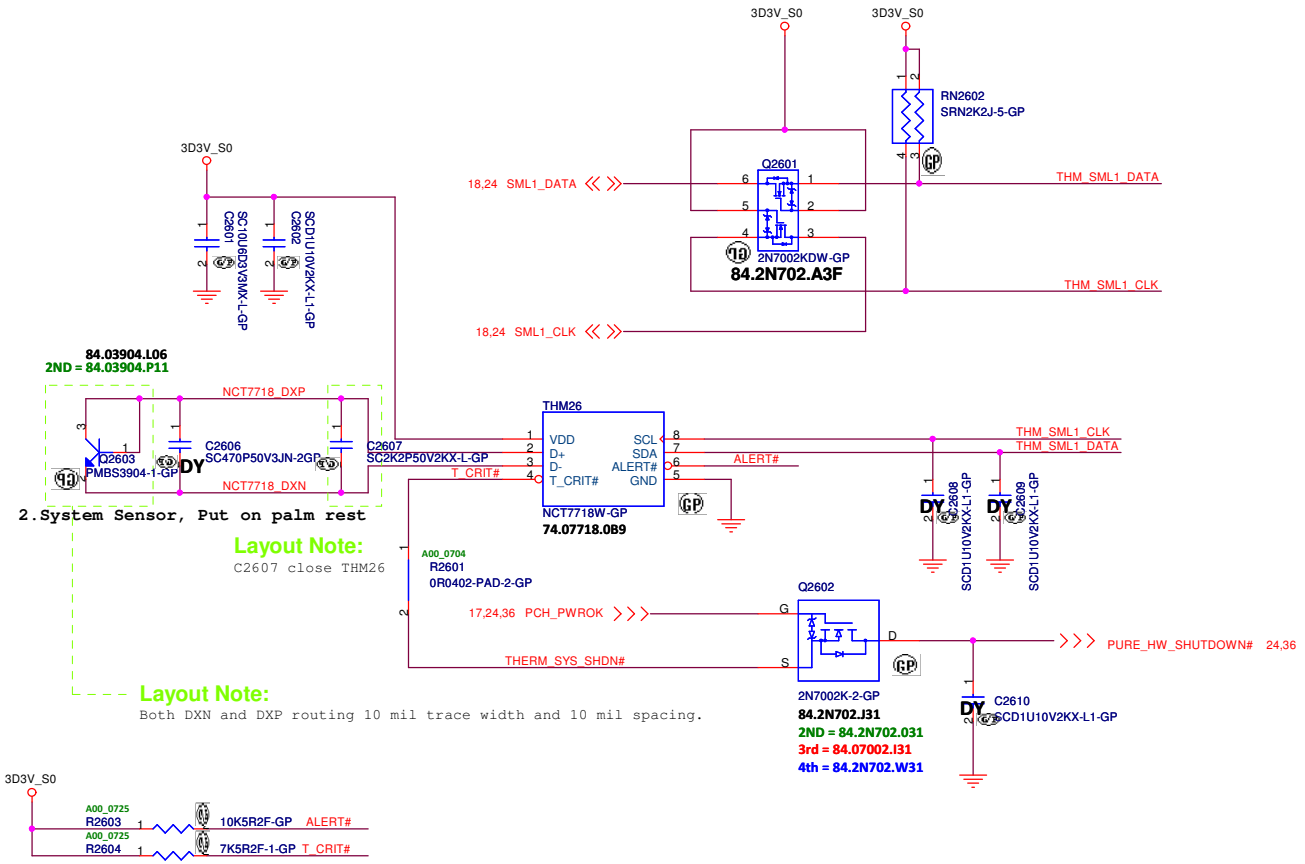


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

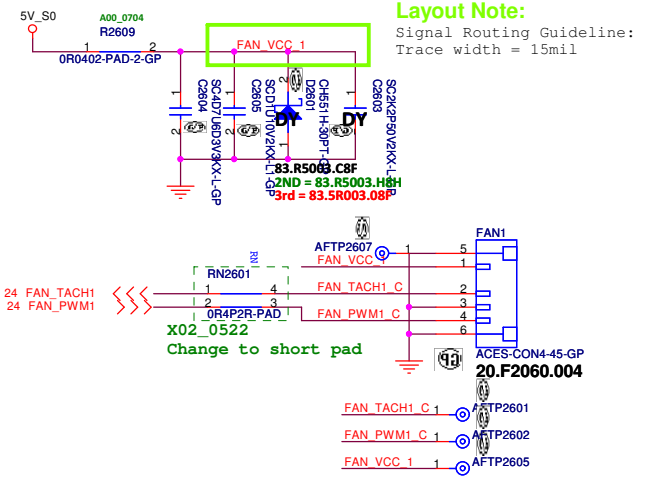
Title: Flash/RTC		
Size: A3	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 25 of 107	

SSID = Thermal

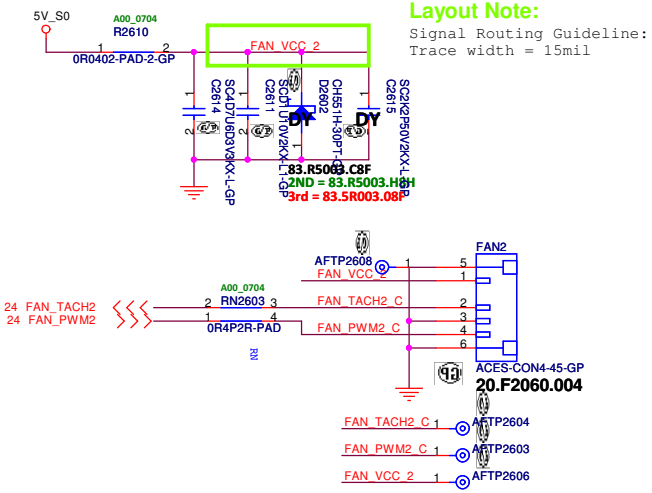


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



PWM FAN2



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan

Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 26 of 107

SSID = AUDIO

25mA

1.5A

Close pin36

Close pin41

Close pin46

Close pin40

Close pin3

Layout Note: Place close to Pin 26

Layout Note: Tied at point only under Codec or near the Codec

Layout Note: Width>40mil, to improve Headphone Crosstalk noise

Layout Note: Place close to Pin 13

X02_0522 Change to short pad

0321 for EMI

0313

71.03223.003

Azalia I/F EMI

X02_0527
Change EC2723, EC2724, EC2701, EC2702 to 5.6pF for RF request

X02_0522
Change to short pad

X02_0522
Change R2718 to short pad

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

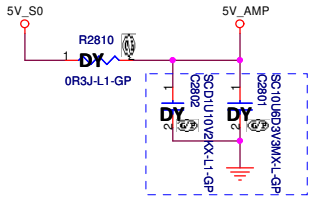
Title: Audio Codec ALC3223

Size: Custom | Document Number: Hadley 14" | Rev: X02

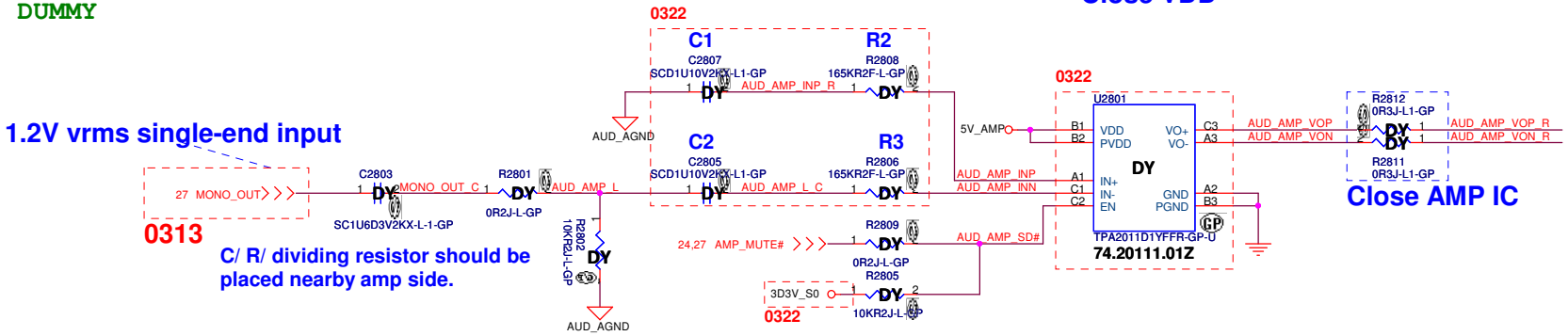
Date: Wednesday, August 14, 2013 | Sheet 27 of 107

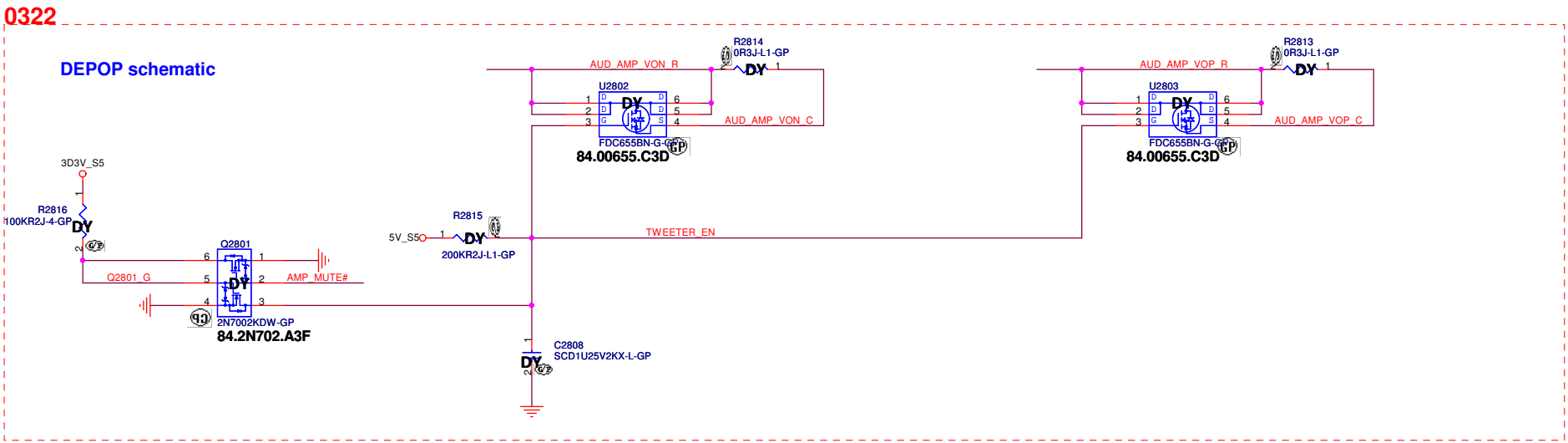
SSID = AUDIO

X02_0515
DUMMY



1.2V vrms single-end input





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

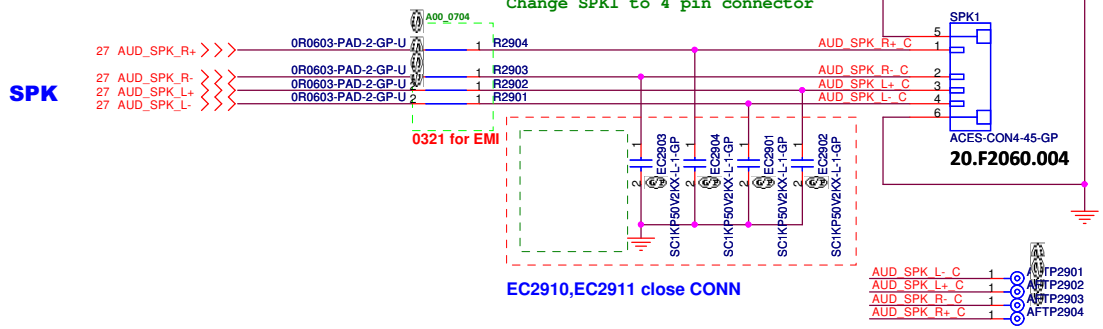
Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 28 of 107

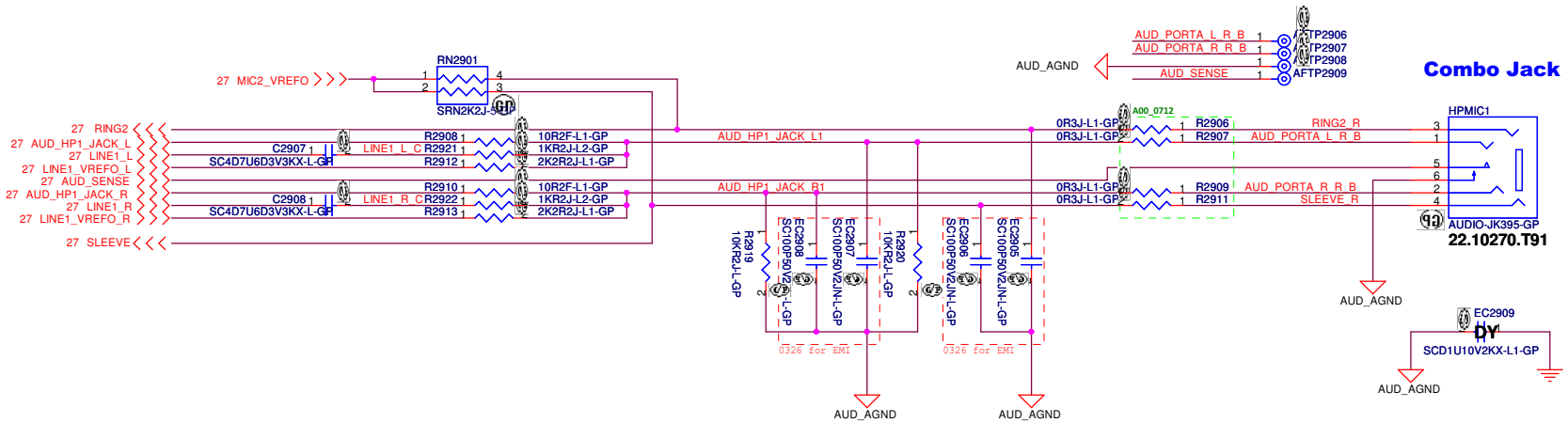
SSID = AUDIO

Speaker

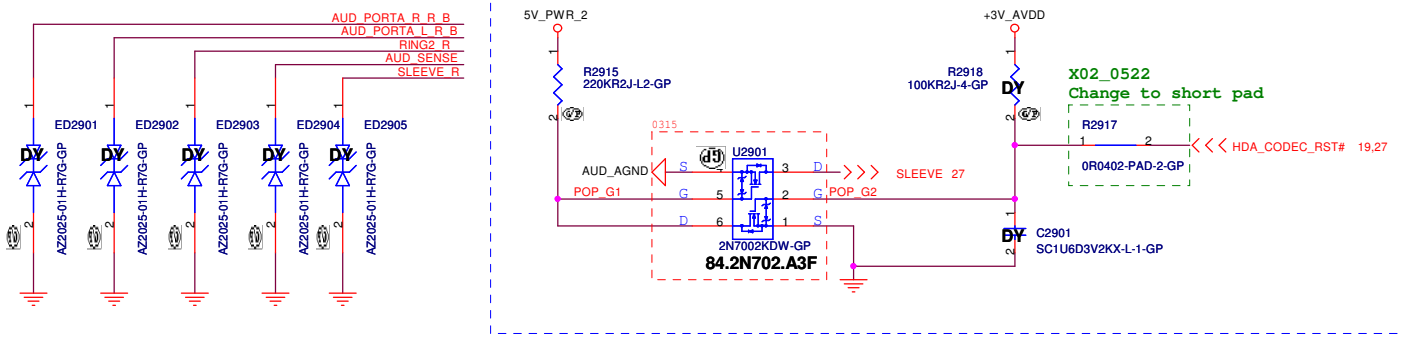
X02_0515
Remove EC2911 and EC2910
Change SPK1 to 4 pin connector



Combo Jack



Grounding circuit for combo jack SLEEVE pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 29 of 107

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

Date: Wednesday, August 14, 2013 | Sheet 30 of 107

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

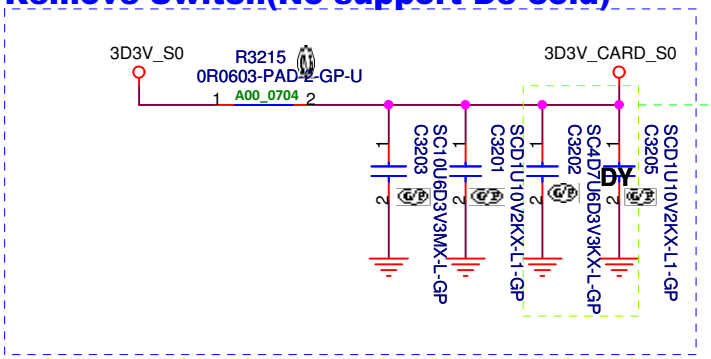
Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

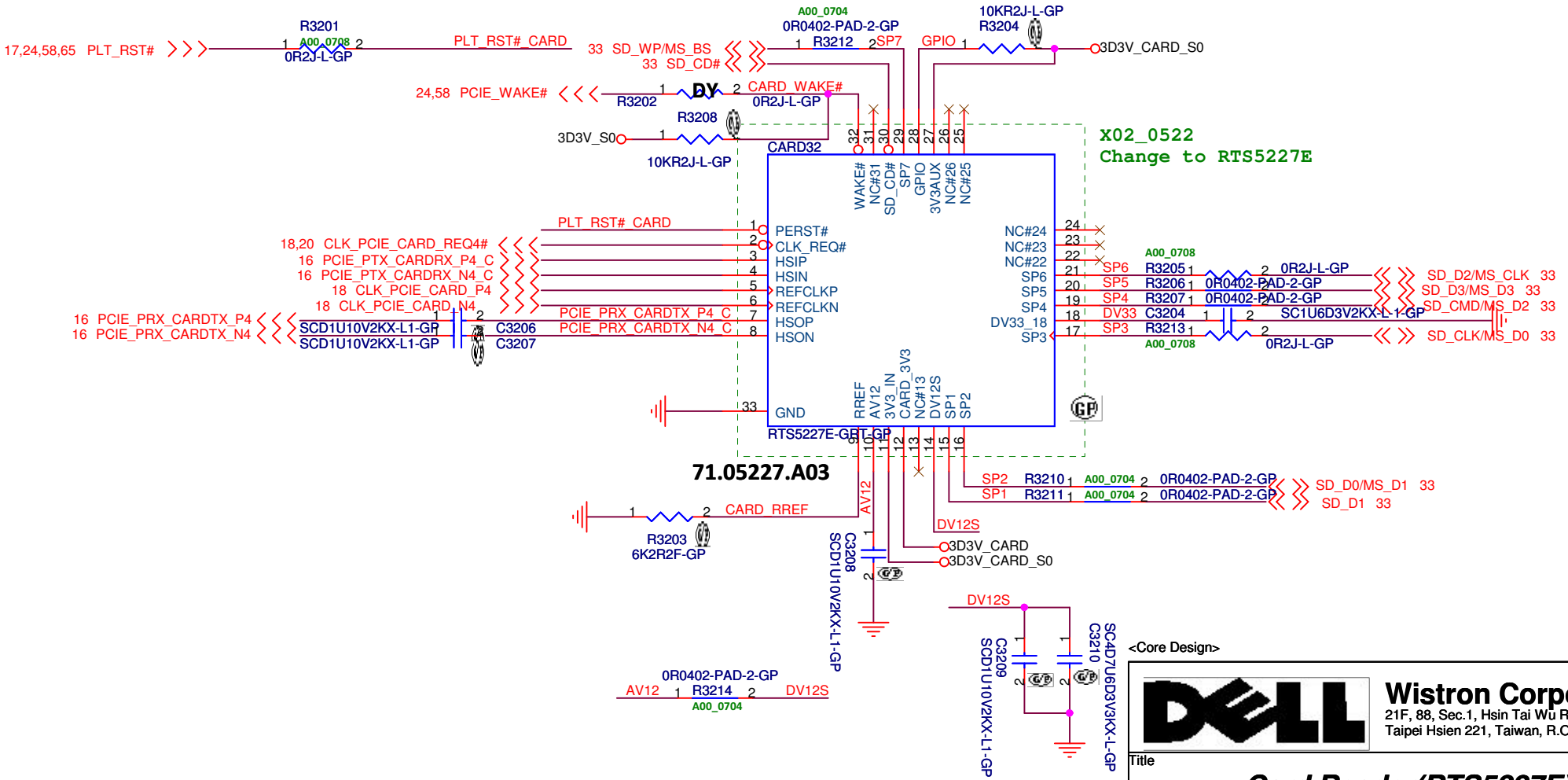
Date: Wednesday, August 14, 2013 | Sheet 31 of 107

SSID = SDIO

Remove Switch(No support D3 cold)



Layout Note:
closed to pin27



<Core Design>

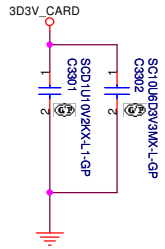
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader(RTS5227E)***

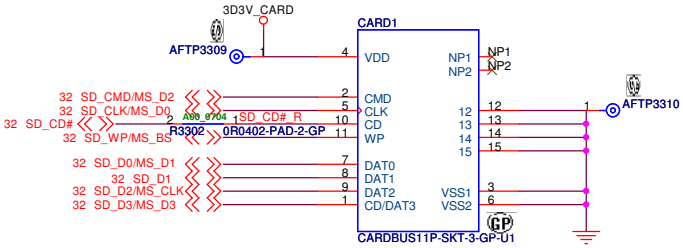
Size	Document Number	Rev
A4	***Hadley 14"***	***A00***

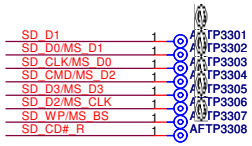
Date: Wednesday, August 14, 2013 Sheet 32 of 107

SSID = SDIO

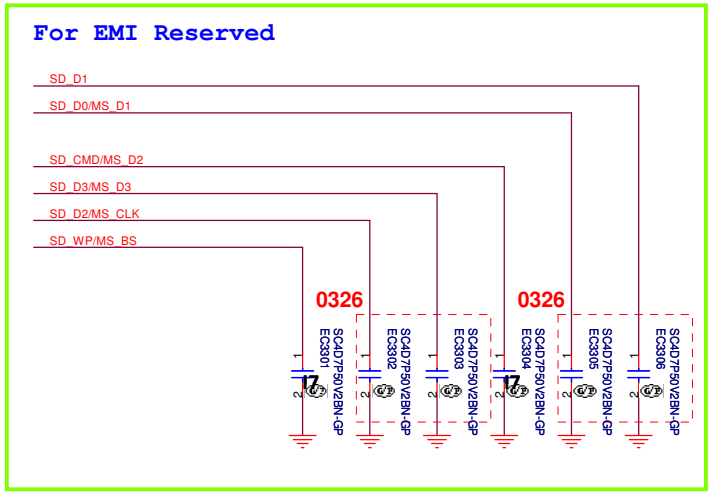


Card Connector

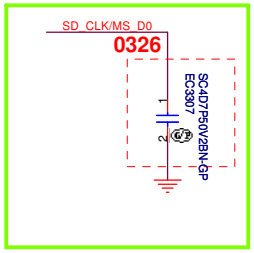




Layout Note:
Close to Card Reader CONN



Layout Note:
closed to chip side



<Core Design>

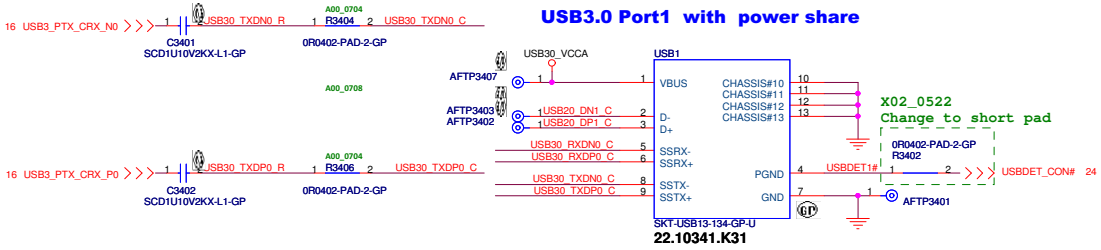
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader CONN		
Size: A3	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 33 of 107	

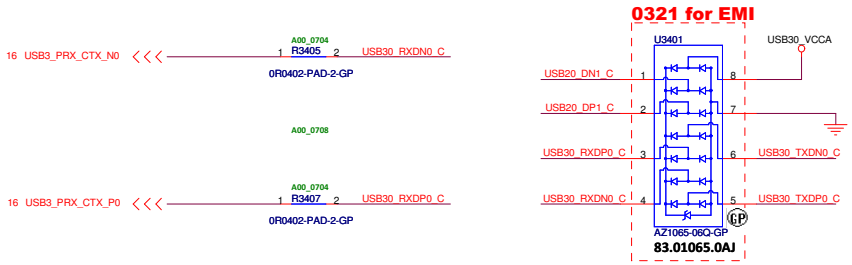
SSID = USB

USB Port1 with power share

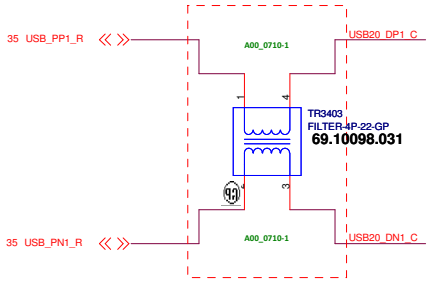
USB3.0 Port1 with power share



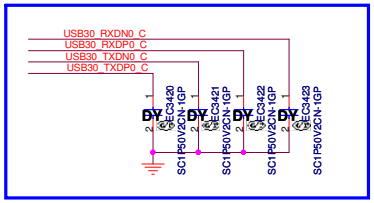
0321 for EMI



0321 for EMI

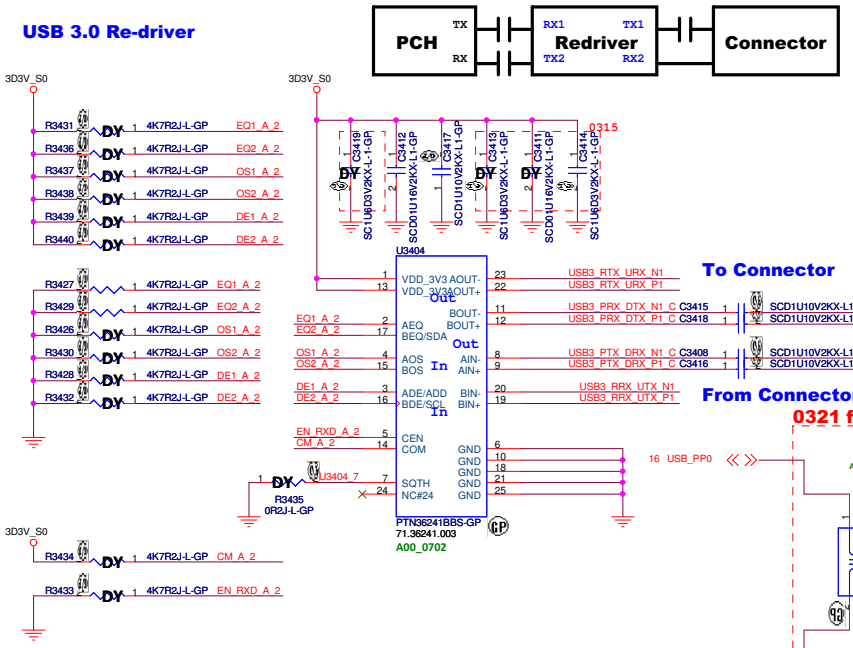


Reserve For RF

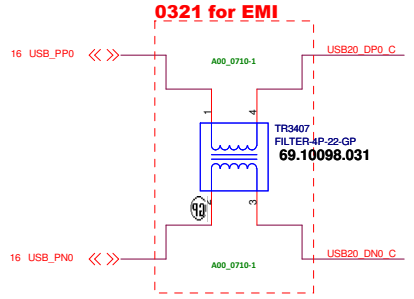


USB Port2

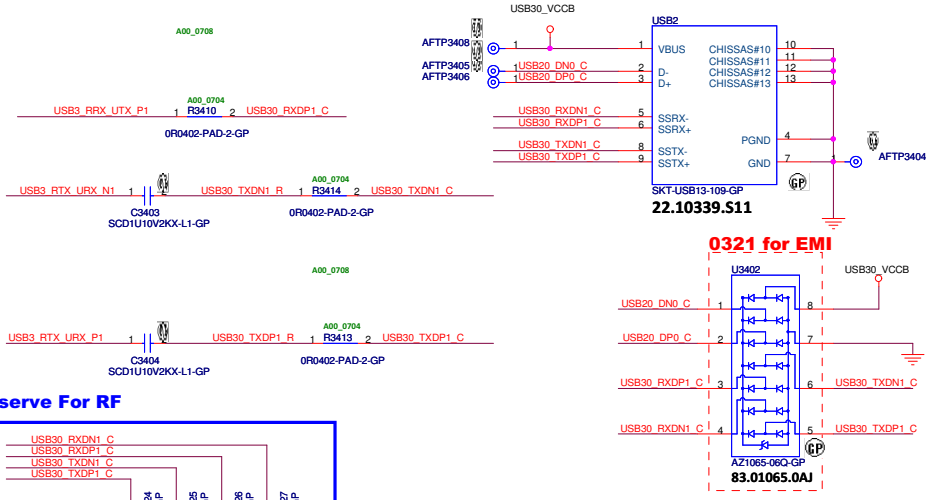
USB 3.0 Re-driver



0321 for EMI

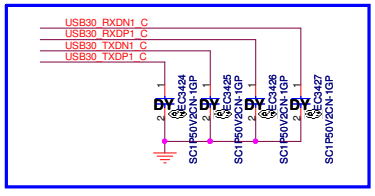


USB3.0 Port2



0321 for EMI

Reserve For RF



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0(1)

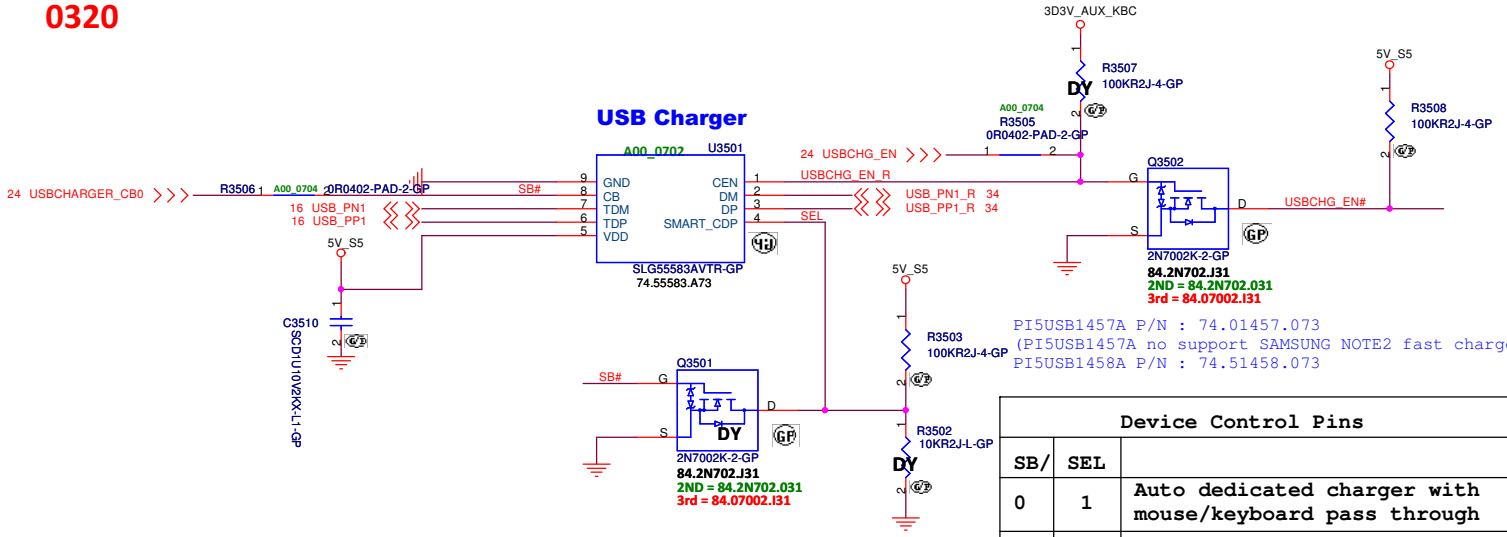
Size	Document Number	Rev
Custom	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 34 of 107

SSID = USB

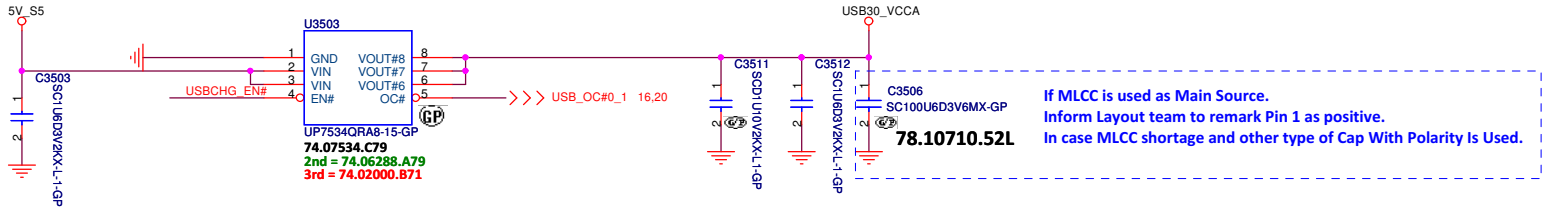
0320

USB Charger

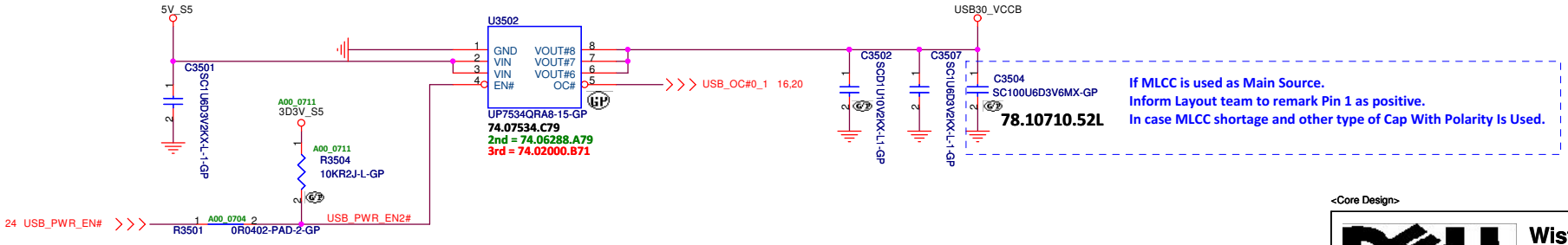


PI5USB1457A P/N : 74.01457.073
(PI5USB1457A no support SAMSUNG NOTE2 fast charge)
PI5USB1458A P/N : 74.51458.073

Device Control Pins		
SB/	SEL	
0	1	Auto dedicated charger with mouse/keyboard pass through
1	1	S0 charging with CDP or SDP only (depending on external device)



If MLCC is used as Main Source.
Inform Layout team to remark Pin 1 as positive.
In case MLCC shortage and other type of Cap With Polarity Is Used.



If MLCC is used as Main Source.
Inform Layout team to remark Pin 1 as positive.
In case MLCC shortage and other type of Cap With Polarity Is Used.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

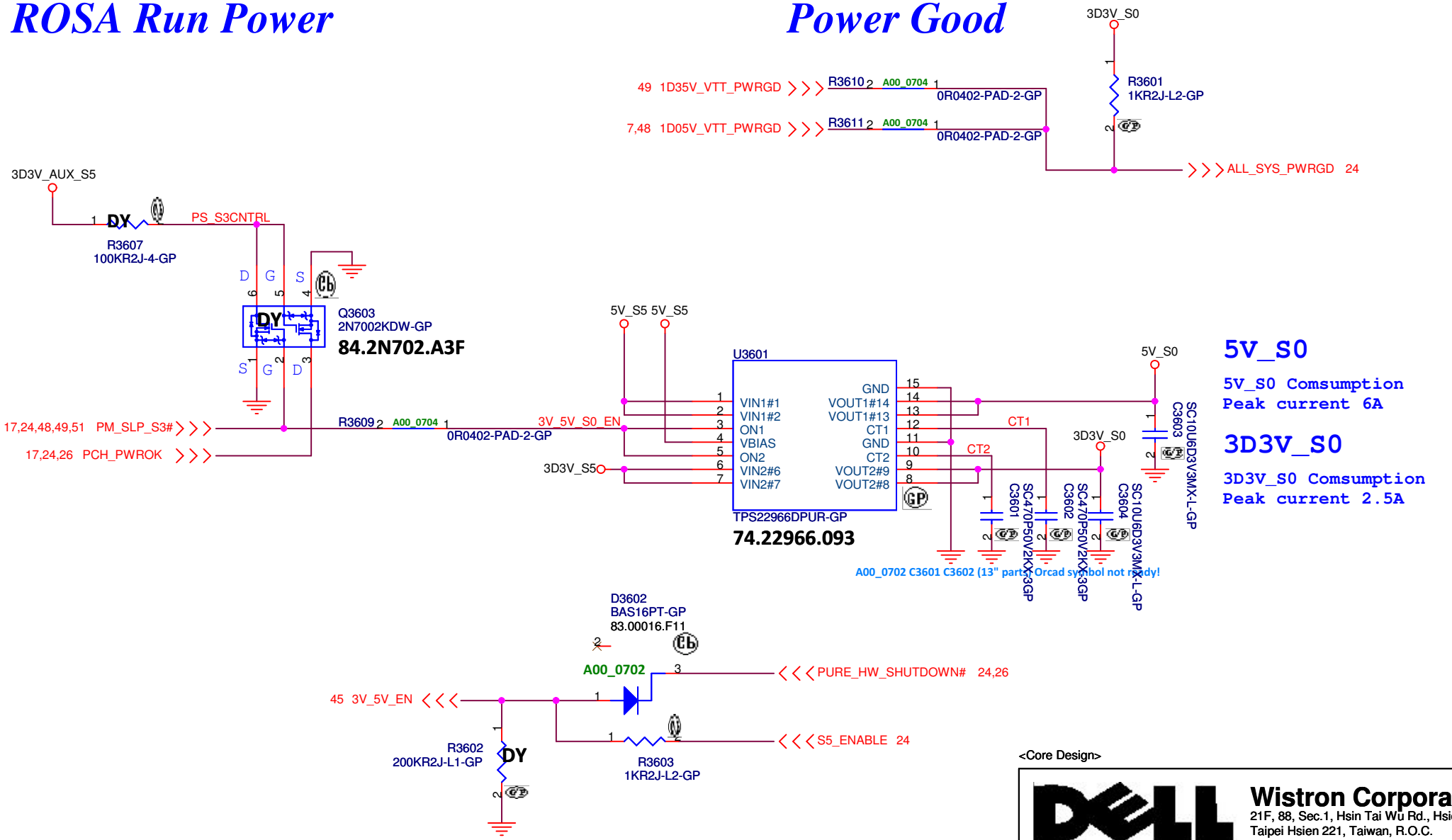
Size | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 35 of 107

SSID = Reset.Suspend

ROSA Run Power

Power Good



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

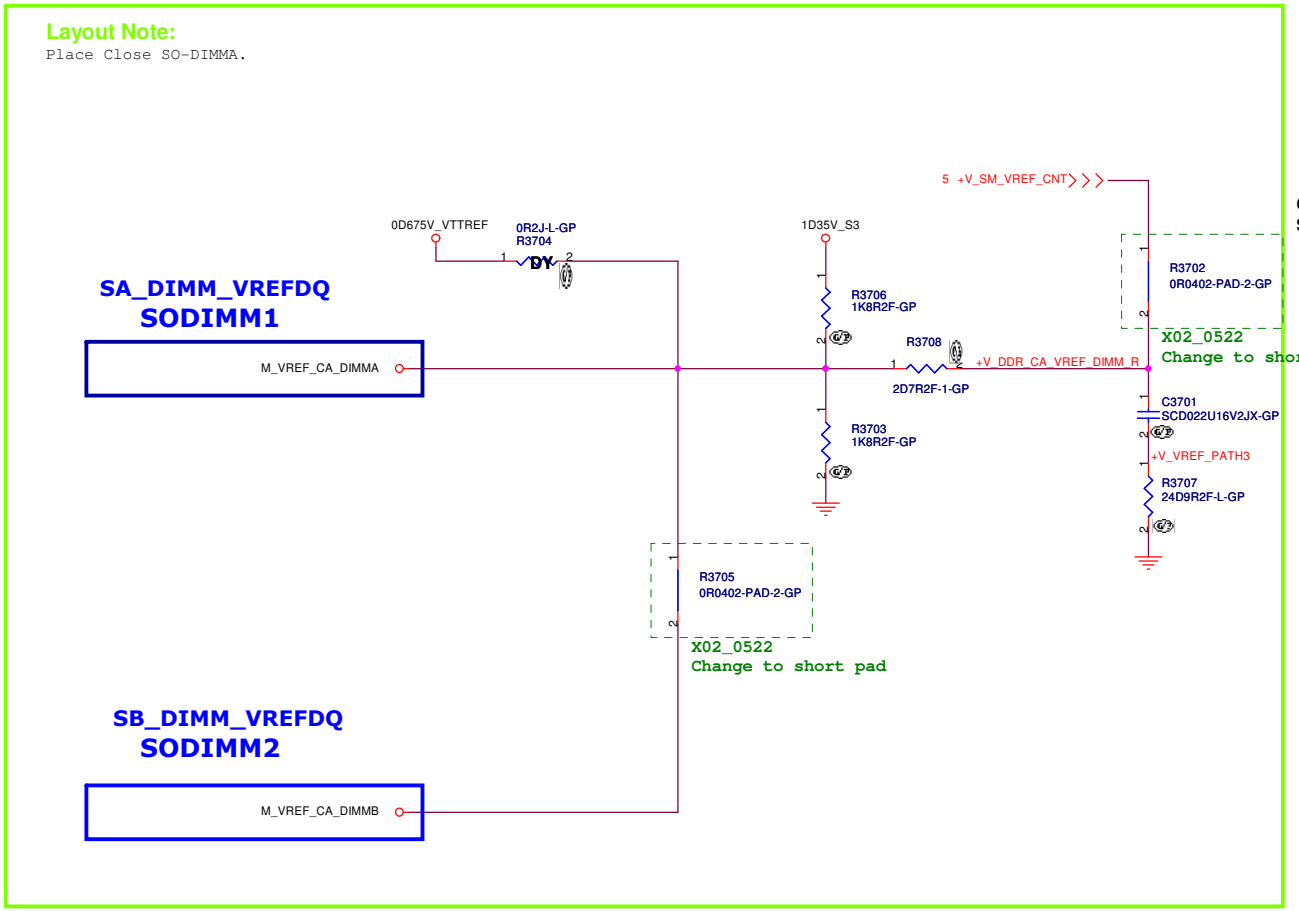
Title: **Power Plane Enable**

Size	Document Number	Rev
A4	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 36 of 107

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.



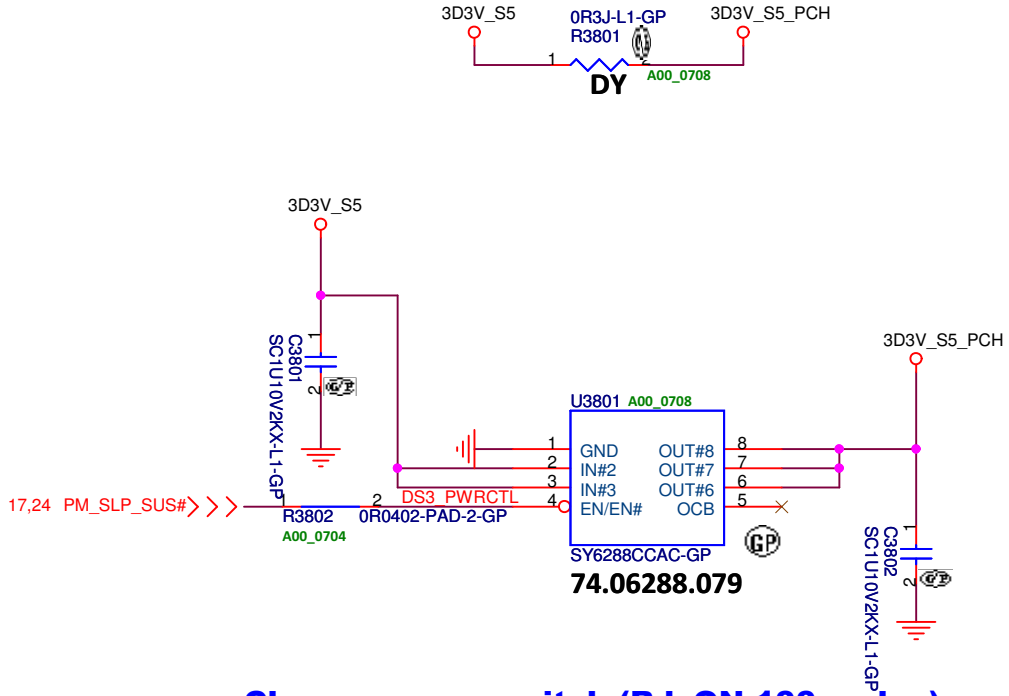
Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S3 Power Reduction*		
Size: A3	Document Number: *Hadley 14"*	Rev: *A00*
Date: Wednesday, August 14, 2013	Sheet 37 of 107	

SSID = Reset.Suspend



Change power switch (RdsON:100m ohm)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DSW***

Size	Document Number	Rev
A4	***Hadley 14"***	***A00***

Date: Wednesday, August 14, 2013 Sheet 38 of 107

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

Date: Wednesday, August 14, 2013 | Sheet 39 of 107

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

Date: Wednesday, August 14, 2013 | Sheet 40 of 107

(Blanking)

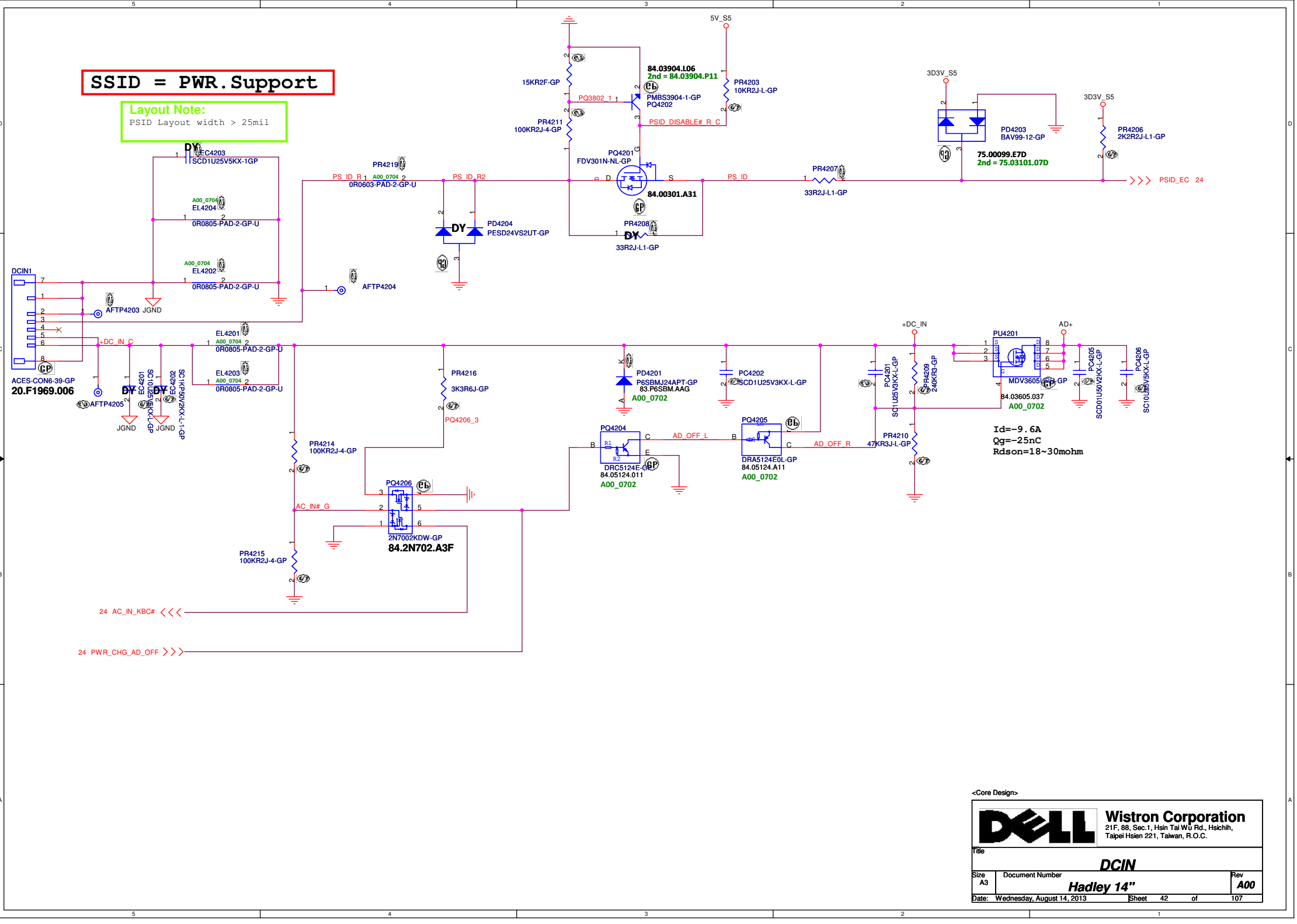
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

Date: Wednesday, August 14, 2013 | Sheet 41 of 107

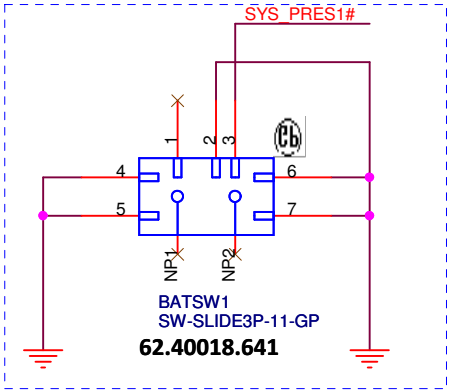


<Core Design>

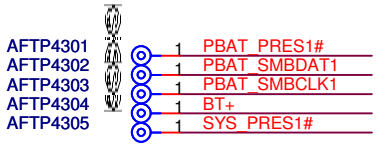
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

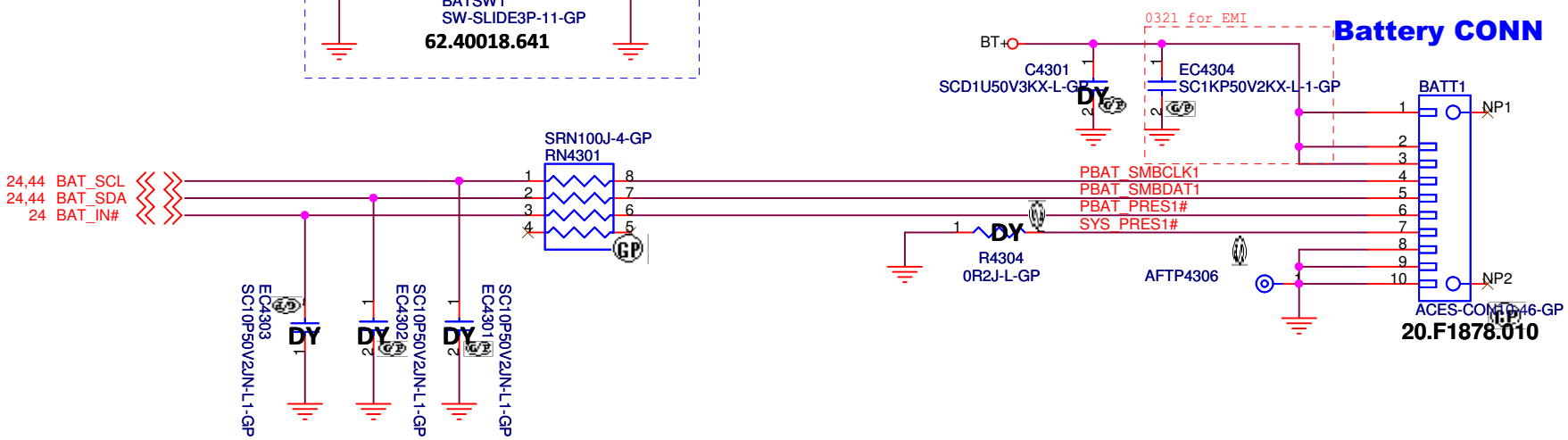
Title		
DCIN		
Size: A3	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 42 of 107	

SSID = PWR.Support

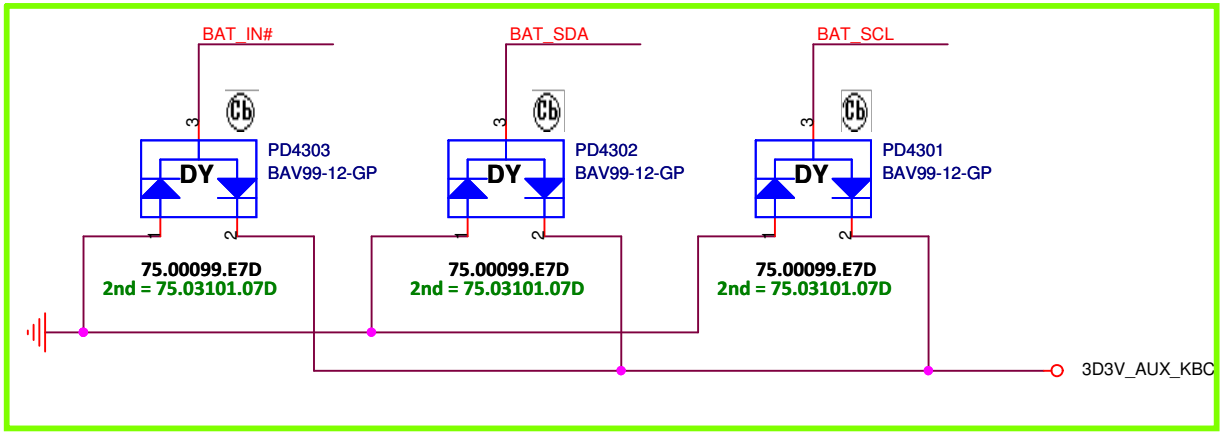


If non-removable battery ,
BATSW1 need stuff





Layout Note: Place near Battery CONN



If battery is Detachable ,
PD4301~4303 need stuff

<Core Design>

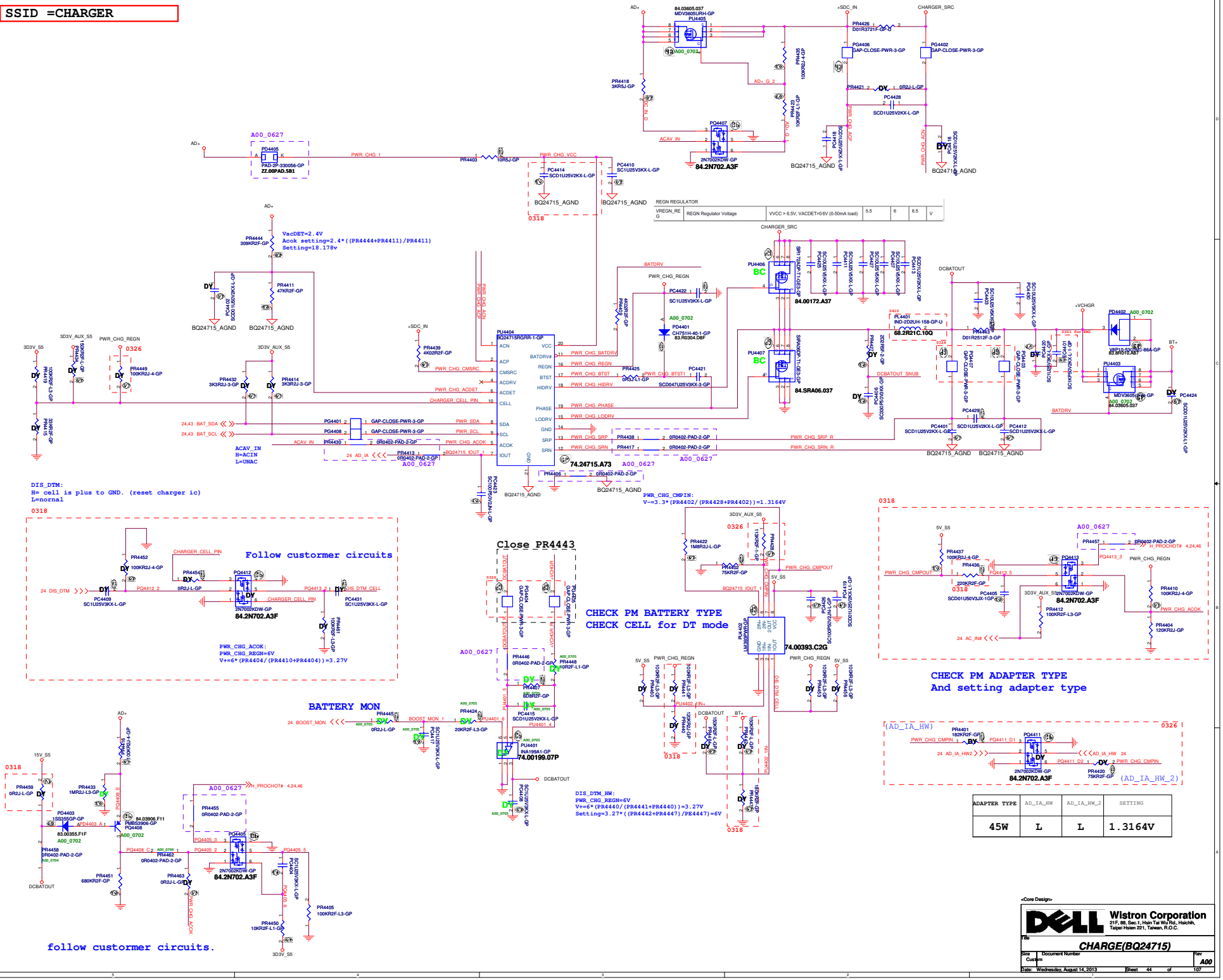
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A4	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 43 of 107

SSID =CHARGER



ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
45W	L	L	1.3164V

<Core Design>

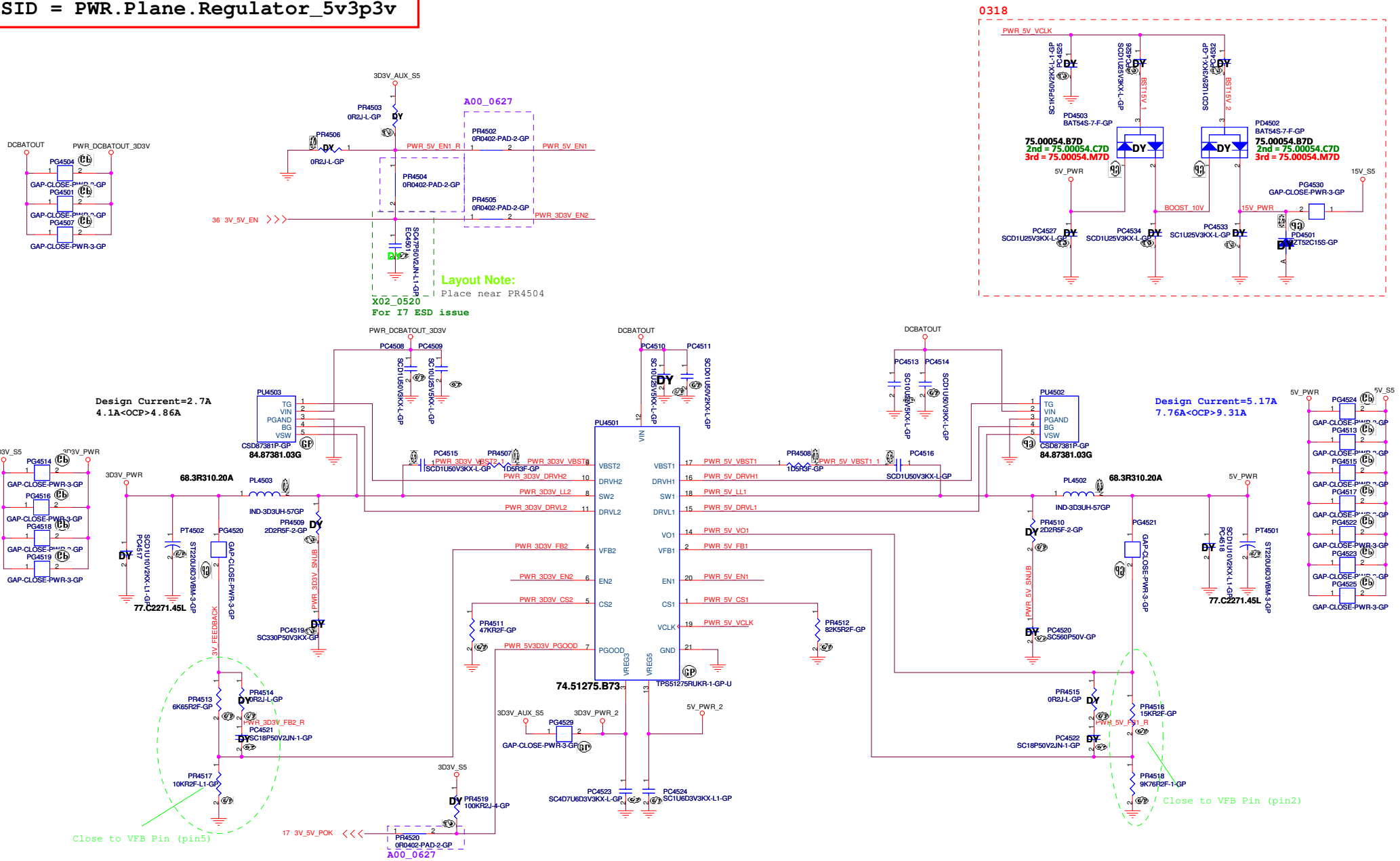
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)

Size	Document Number	Rev
Custom		A00

Date: Wednesday, August 14, 2013 Sheet 44 of 107

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP T 220U 6.3V M3528 PSL /NEC-TOKIN/ 25mOhm / 77.C2271.45L
H/S,L/S: FET MOS CSD87381P SON 5P/ 15.3m ohm@4.5Vgs/ 7 mohm@ 4.5Vgs / 84.87381.03G

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP T 220U 6.3V M3528 PSL /NEC-TOKIN/ 25mOhm / 77.C2271.45L
H/S,L/S: FET MOS CSD87381P SON 5P/ 15.3m ohm@4.5Vgs/ 7 mohm@ 4.5Vgs / 84.87381.03G

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51275

Size: Custom | Document Number: Hadley 14" | Rev: A00

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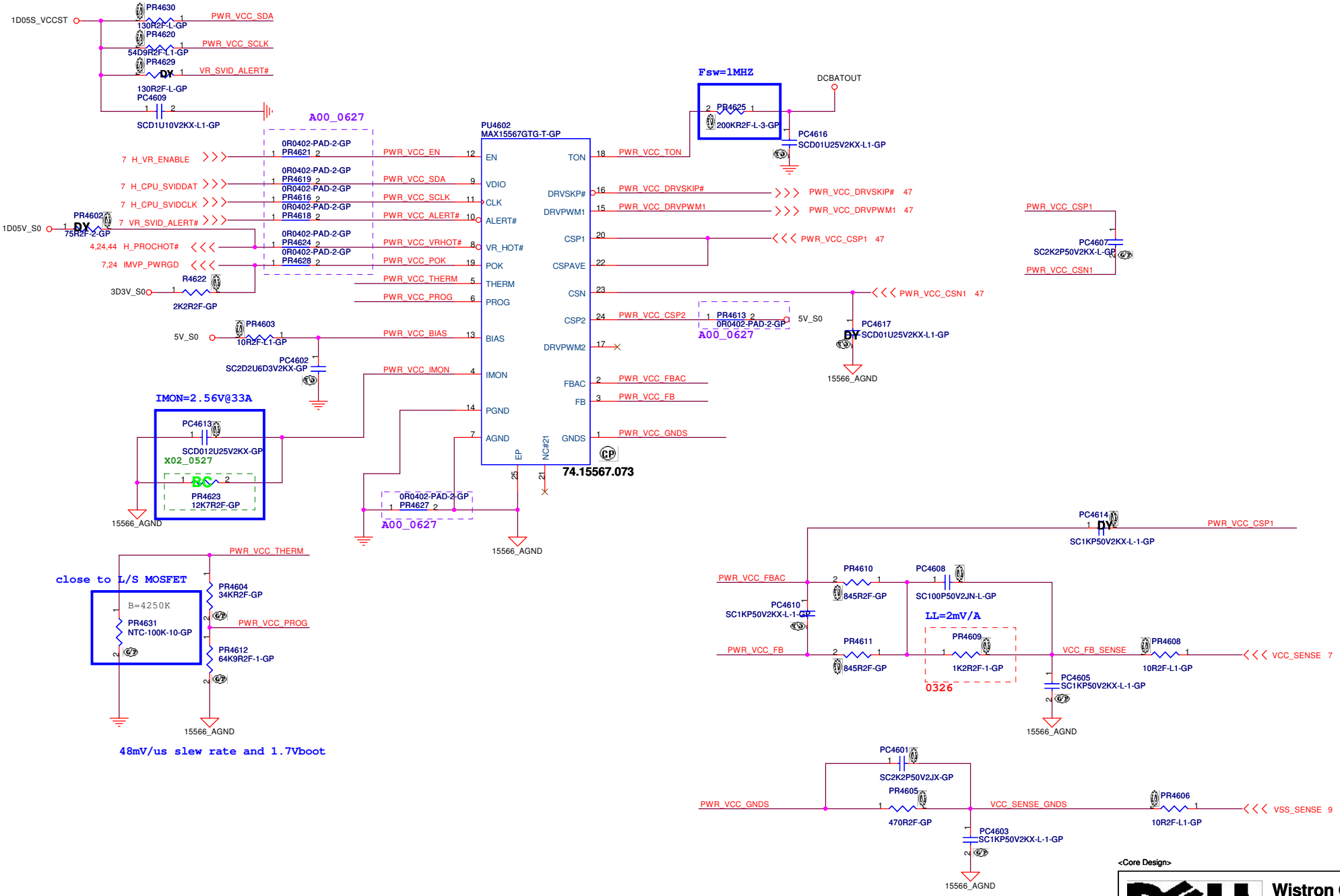
SSID = CPU.Regulator



<Core Design>

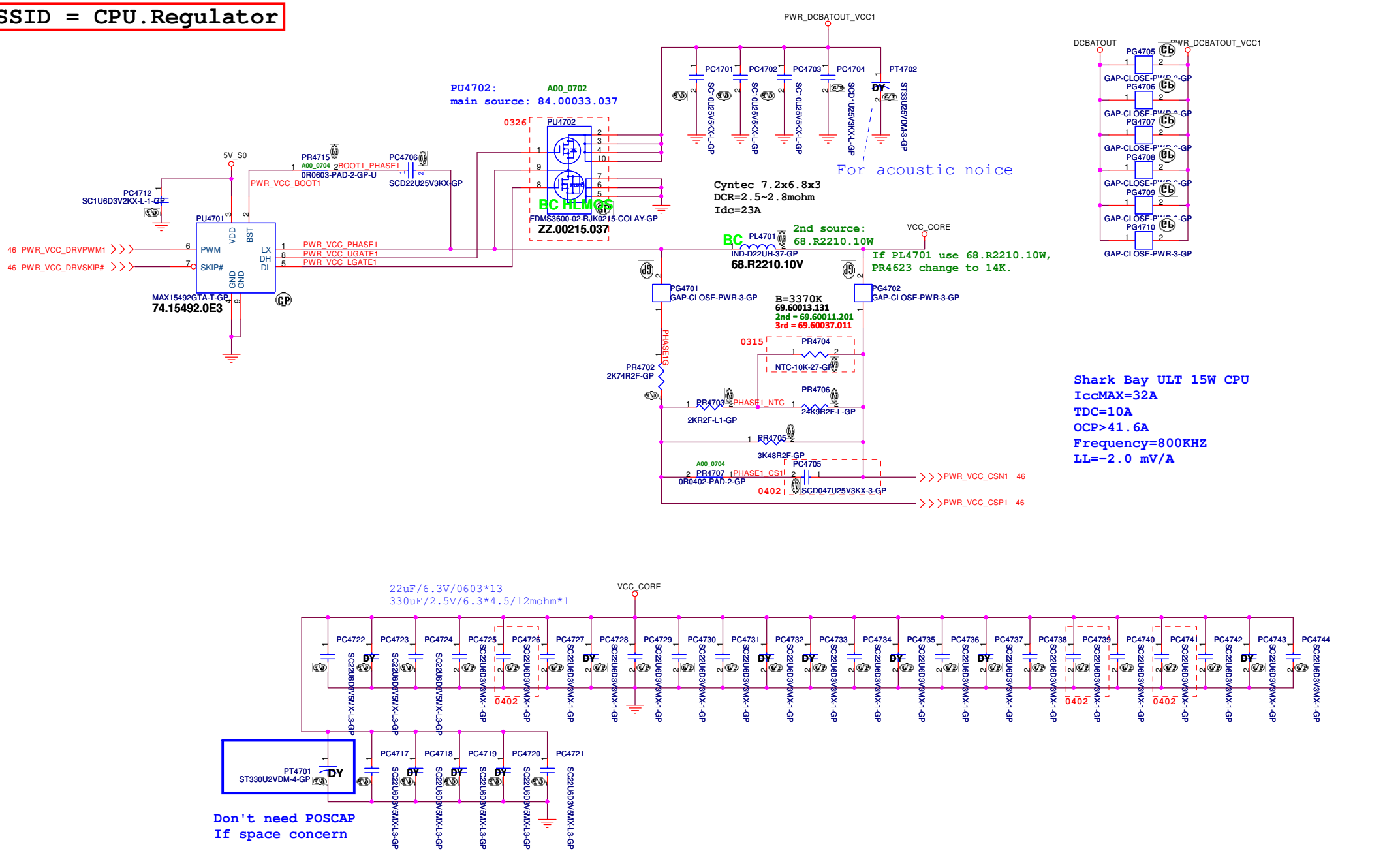
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MAX15567GTG_CPUCORE(1/2)

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 46 of 107

SSID = CPU.Regulator



<Core Design>

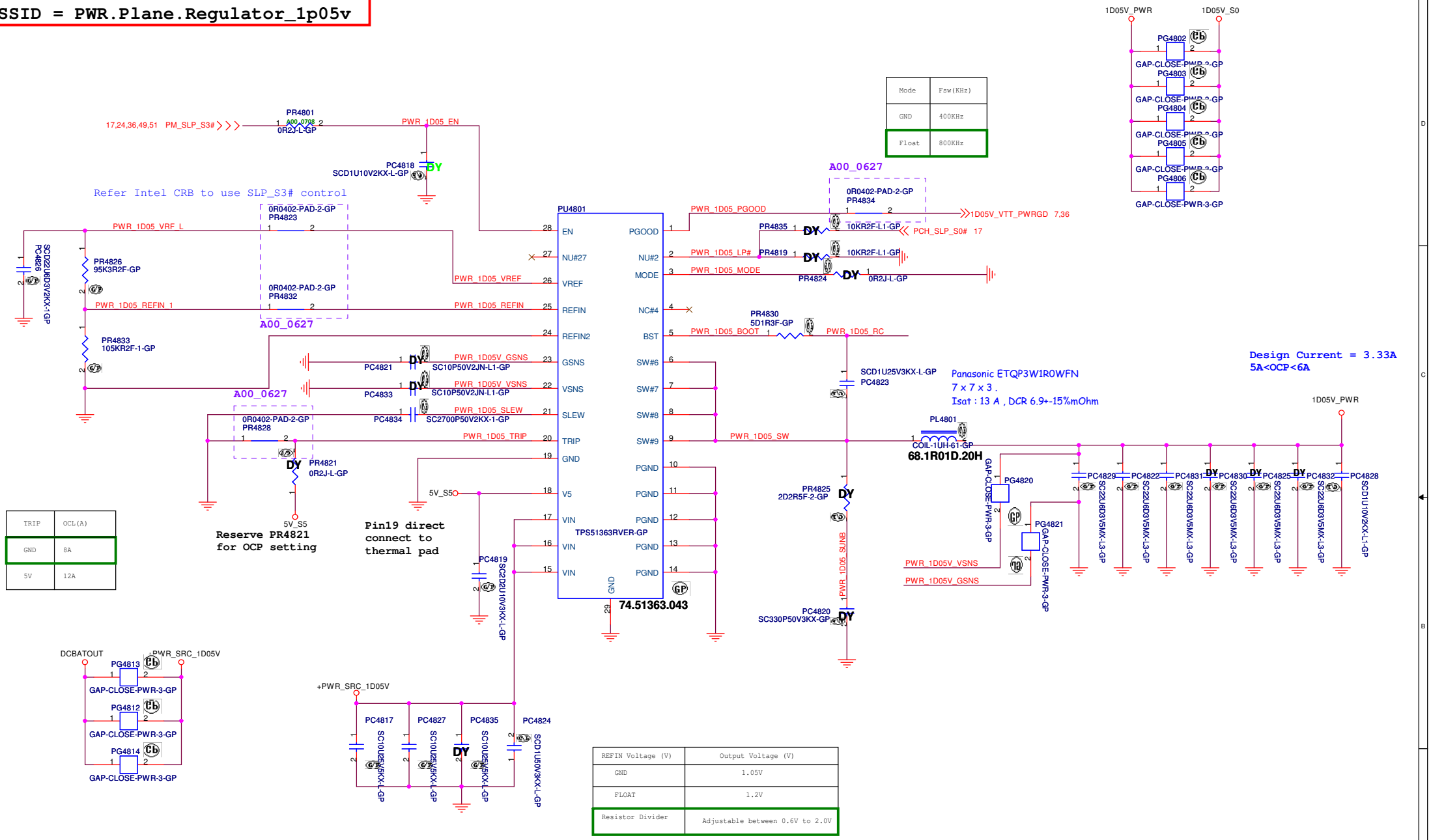
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MAX15567GTG_CPUCORE(2/2)*

Size	Document Number	Rev
A3	*Hadley 14"*	*A00*

Date: Wednesday, August 14, 2013 Sheet 47 of 107

SSID = PWR.Plane.Regulator_1p05v



Mode	Fsw(KHz)
GND	400KHz
Float	800KHz

TRIP	OCL(A)
GND	8A
5V	12A

REFIN Voltage (V)	Output Voltage (V)
GND	1.05V
FLOAT	1.2V
Resistor Divider	Adjustable between 0.6V to 2.0V

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

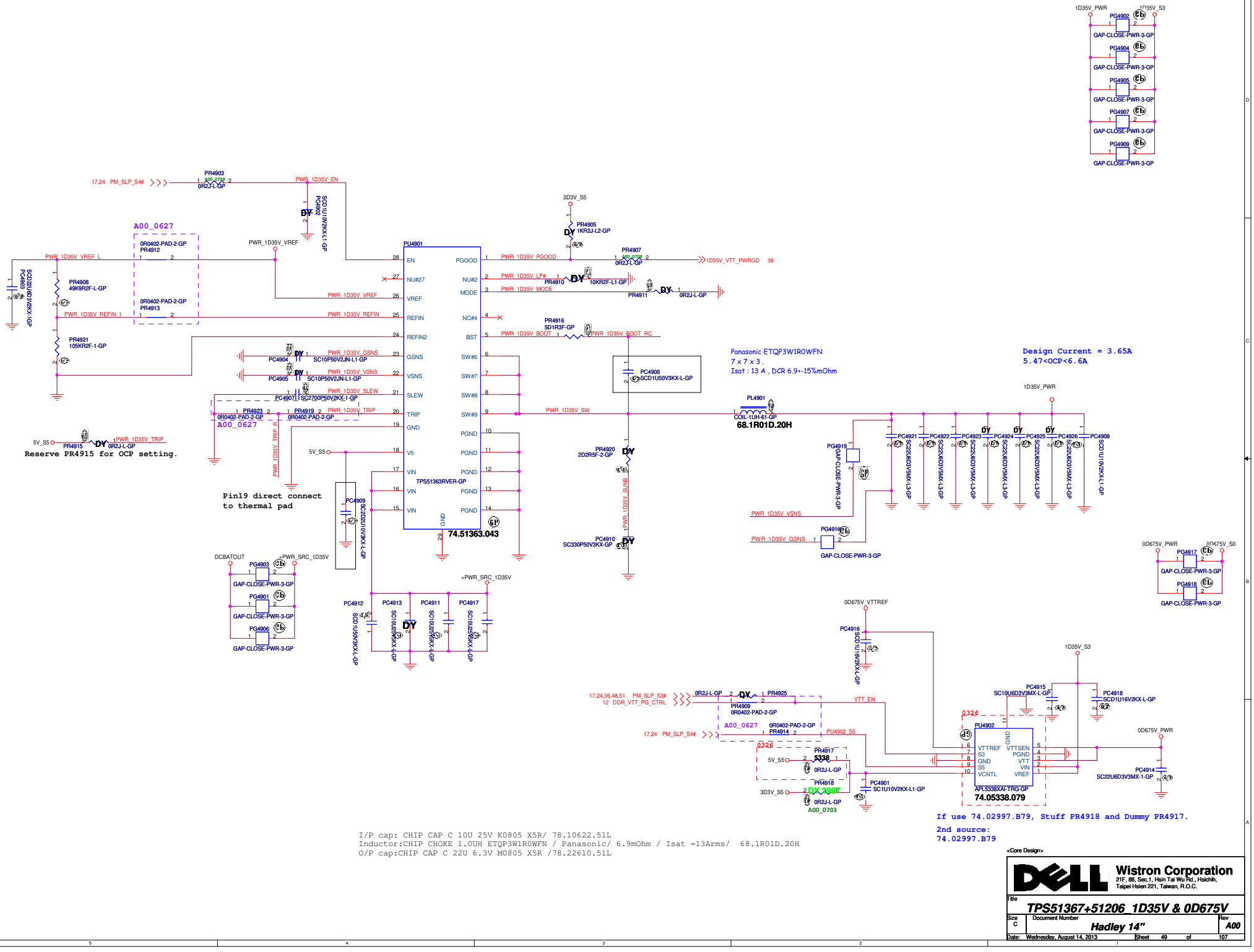
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363 1D05V

Size	Document Number	Rev
A3	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 48 of 107

SSID = PWR.Plane.Regulator_1p35v0p675v



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51367+51206_1D35V & 0D675V

Size	Document Number	Rev
C	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 49 of 107

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

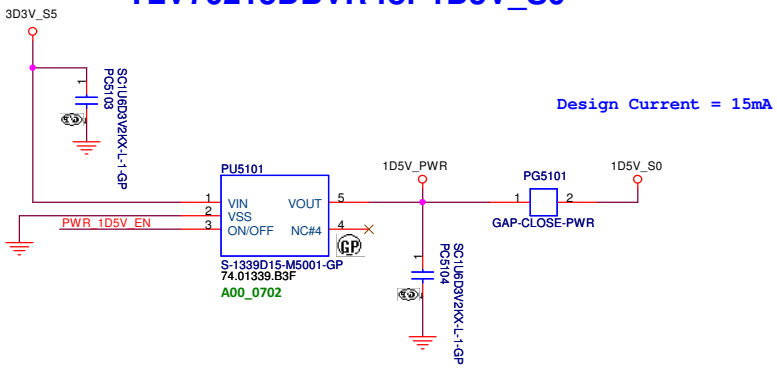
Title: (Reserved)TPS51312 1D8V

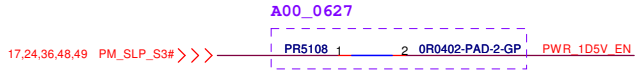
Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 50 of 107

SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

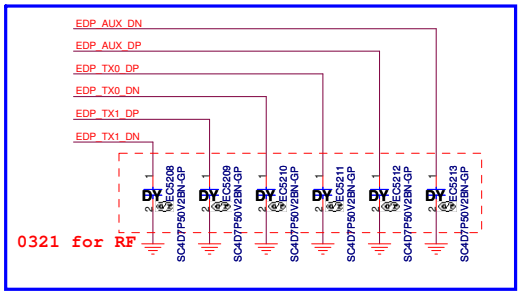
Title: RT9198-15PU5R_1D5V

Size: A3 | Document Number: Hadley 14" | Rev: A00

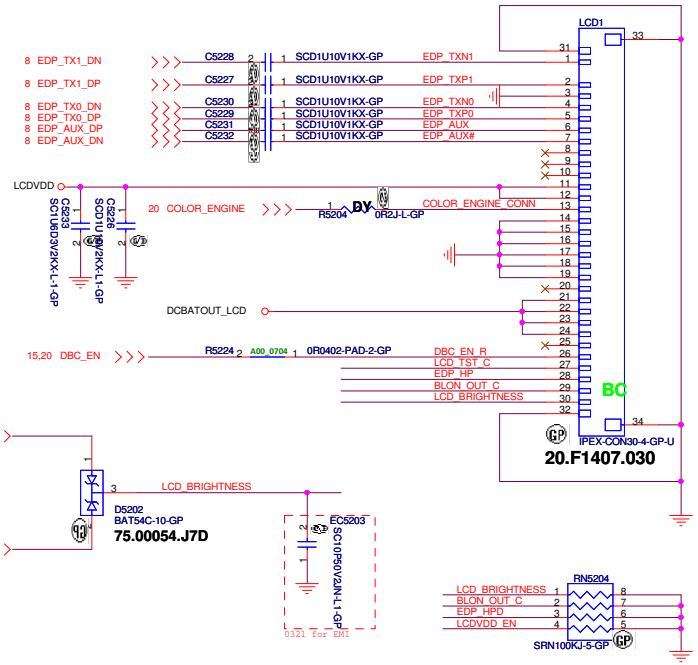
Date: Wednesday, August 14, 2013 | Sheet 51 of 107

SSID = VIDEO

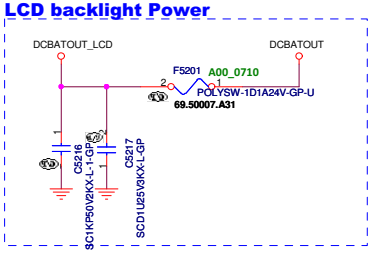
Reserve For RF

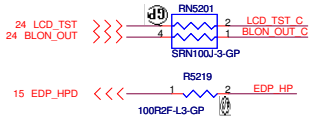


Panel CONN



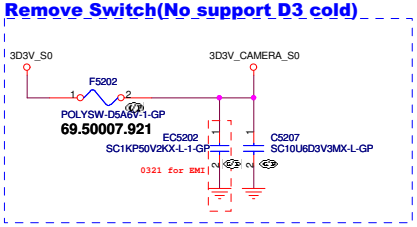
LCD backlight Power

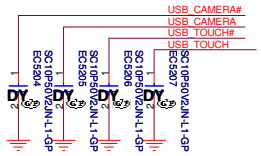


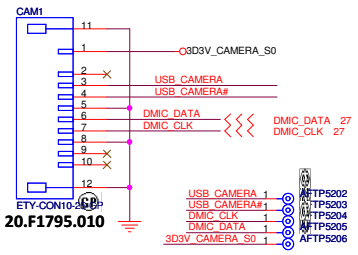


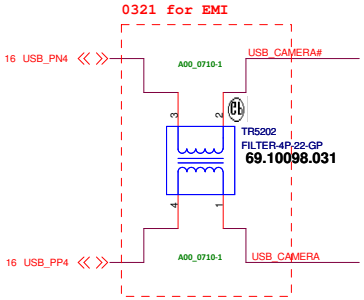
CAMERA

Camera Power
Remove Switch(No support D3 cold)



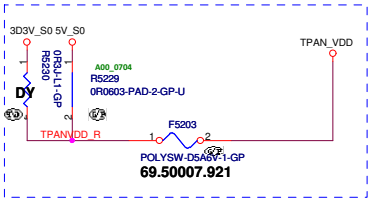


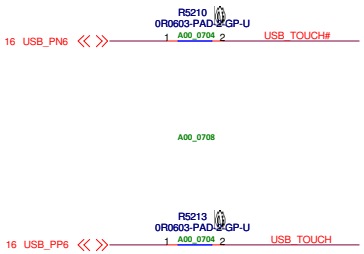


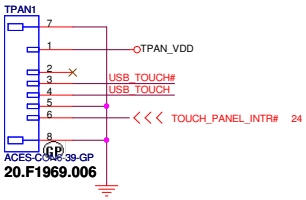


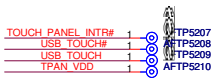
TPNL

Touch Panel Power
Remove Switch(No support D3 cold)

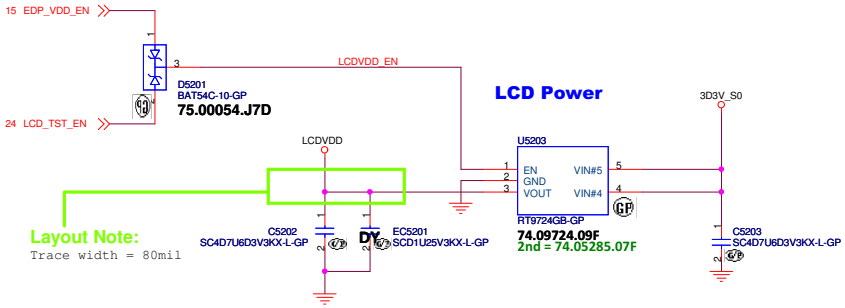








LCDVDD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
Custom	Hadley 14"	A00

Date: Wednesday, August 14, 2013 Sheet 52 of 107

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***Hadley 14"***	***A00***

SSID = VIDEO

8 HDMI_CLK#
8 HDMI_CLK
C5401 C5402 SCD1U10V2KX-L1-GP
HDMI_CLK_R# HDMI_CLK_R

8 HDMI_DATA0#
8 HDMI_DATA0
C5403 C5404 SCD1U10V2KX-L1-GP
HDMI_DATA0_R# HDMI_DATA0_R

8 HDMI_DATA1#
8 HDMI_DATA1
C5405 C5406 SCD1U10V2KX-L1-GP
HDMI_DATA1_R# HDMI_DATA1_R

8 HDMI_DATA2#
8 HDMI_DATA2
C5407 C5408 SCD1U10V2KX-L1-GP
HDMI_DATA2_R# HDMI_DATA2_R

PS8171: strap pin
PS8171C : vcc pin

3D3V_S0
R5430 DY 4K7R2J-L-GP PS8171_APD
R5431 DY 4K7R2J-L-GP

0327
R5428 DY 4K7R2J-L-GP PS8171_PRE
R5427 DY 4K7R2J-L-GP

R5412 DY 4K7R2J-L-GP PS8171_PEQ
R5413 DY 4K7R2J-L-GP

R5414 DY 4K7R2J-L-GP PS8171_PIO
R5415 DY 4K7R2J-L-GP

R5426 DY 4K7R2J-L-GP PS8171_EMI0
R5425 DY 4K7R2J-L-GP

R5417 DY 4K7R2J-L-GP PS8171_EMI1
R5419 DY 4K7R2J-L-GP

3D3V_S0
C5425 C5424 C5427 C5428 C5429 C5431 SCD1U10V2KX-L1-GP DY
PS8171_APD

R5429 4K7R2J-L-GP DY
A00_0704 R5433 0R0402-PAD-2-GP
C5430 SCD1U10V2KX-L1-GP DY

U5401
VCC x7
DDC_EN DDCBUF
OE#
PS8171_DDCEN PS8171_DDCBUF

RESERVED0 NC#12
EMI0 EMI1
PRE
IN_D1- IN_D1+ IN_D2- IN_D2+ IN_D3- IN_D3+ IN_D4- IN_D4+
PS8171_ASQ1 PS8171_EMI0 PS8171_EMI1 PS8171_APD PS8171_PRE
HDMI_CLK_R# HDMI_CLK_R HDMI_DATA0_R# HDMI_DATA0_R HDMI_DATA1_R# HDMI_DATA1_R HDMI_DATA2_R# HDMI_DATA2_R

HPDX SDA SCL
SCL_SINK SDA_SINK HPD_SINK
DDC_CLK_HDMI DDC_DATA_HDMI HPD_HDMI_CON
HDMI_PCH_DET 15
PCH_HDMI_DATA 15
PCH_HDMI_CLK 15

OUT_D1- OUT_D1+ OUT_D2- OUT_D2+ OUT_D3- OUT_D3+ OUT_D4- OUT_D4+
HDMI_CLK_R_C#_CON HDMI_CLK_R_C_CON HDMI_DATA0_R_C#_CON HDMI_DATA0_R_C_CON HDMI_DATA1_R_C#_CON HDMI_DATA1_R_C_CON HDMI_DATA2_R_C#_CON HDMI_DATA2_R_C_CON

PEQ PIO REXT CEXT GND x7
PS8171_PEQ PS8171_PIO PS8171_REXT PS8171_CEXT

PS8171CQFN48GTR2-A1-GP
71.08171.B03
PS8171 P/N : 71.08171.003
PS8171C P/N : 71.08171.B03

0327
R5410 390R2F-2GP
C5426 SC2D2U6D3V2MX-L-1-GP
X02_0522

0327

5V_S0 0326 5V_HDMI_S0
F5401 POLYSW-1D1A8V-5-GP
69.50007.691

5V_HDMI_S0 0315
D5401 BAW56-11-GP
75.00056.B7D
2nd = 75.00056.A7D
D5102_2 D5102_1
SRN2K2J-5-GP RN5401

5V_HDMI_S0
C5417 SCD1U10V2KX-L1-GP

X02_0509
HDMI CONN
HDMI1
+5V_POWER
SCL SDA
DDC_CLK_HDMI DDC_DATA_HDMI
TMDS_DATA0+ TMDS_DATA0- TMDS_DATA1+ TMDS_DATA1- TMDS_DATA2+ TMDS_DATA2-
HDMI_DATA0_R_C_CON HDMI_DATA0_R_C#_CON HDMI_DATA1_R_C_CON HDMI_DATA1_R_C#_CON HDMI_DATA2_R_C_CON HDMI_DATA2_R_C#_CON
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
HPD_HDMI_CON
RESERVED#14
TMDS_DATA0_SHIELD TMDS_DATA1_SHIELD TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+ TMDS_CLOCK-
HDMI_CLK_R_C_CON HDMI_CLK_R_C#_CON
CHASSIS#20 CHASSIS#21 CHASSIS#22 CHASSIS#23
SKT-HDMI23-101-GP-U
22.10296.A61

R5409 DY 20KR2J-L3-GP

0327 HDMI_CLK_R_C_CON → 0321 for EMI ER5442 150R2F-4-L-GP → HDMI_CLK_R_C#_CON
0327 HDMI_DATA0_R_C_CON → 0321 for EMI ER5444 150R2F-4-L-GP → HDMI_DATA0_R_C#_CON
0327 HDMI_DATA2_R_C_CON → 0321 for EMI ER5443 150R2F-4-L-GP → HDMI_DATA2_R_C#_CON
0327 HDMI_DATA1_R_C_CON → 0321 for EMI ER5445 150R2F-4-L-GP → HDMI_DATA1_R_C#_CON

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Repeater/Connector
Size: A3
Document Number: Hadley 14"
Rev: A00
Date: Wednesday, August 14, 2013
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Hadley 14"*	*A00*

Date: Wednesday, August 14, 2013 Sheet 55 of 107

SSID = SATA

HDD CONN

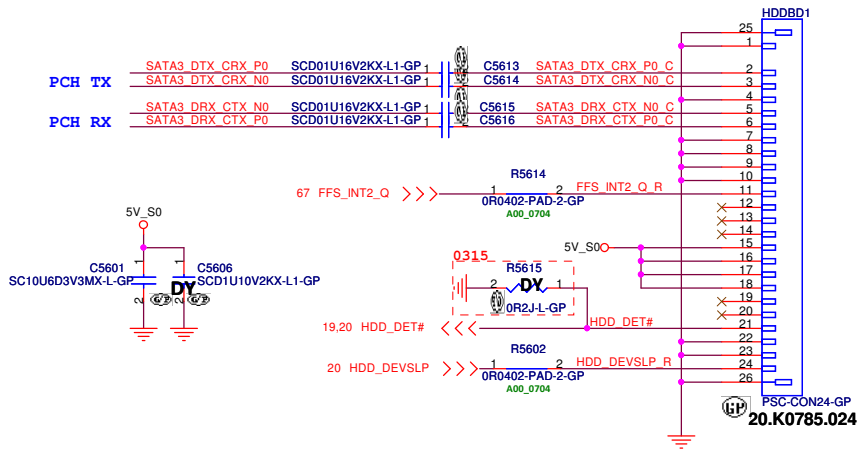


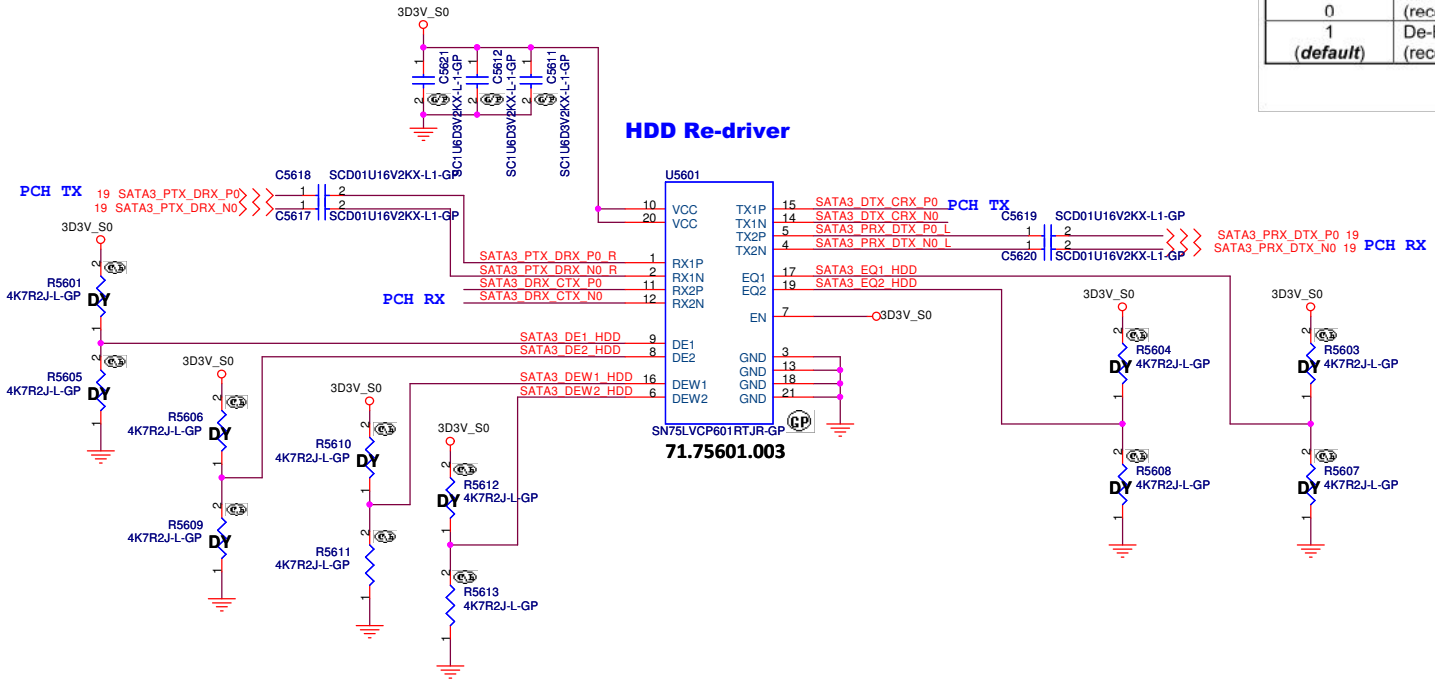
Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps
NC (*default*)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (*default*)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (*default*)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

HDD Re-driver



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

Size: A3 | Document Number: Hadley 14" | Rev: A00

Date: Wednesday, August 14, 2013 | Sheet 56 of 107

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 14"* | Rev: *A00*

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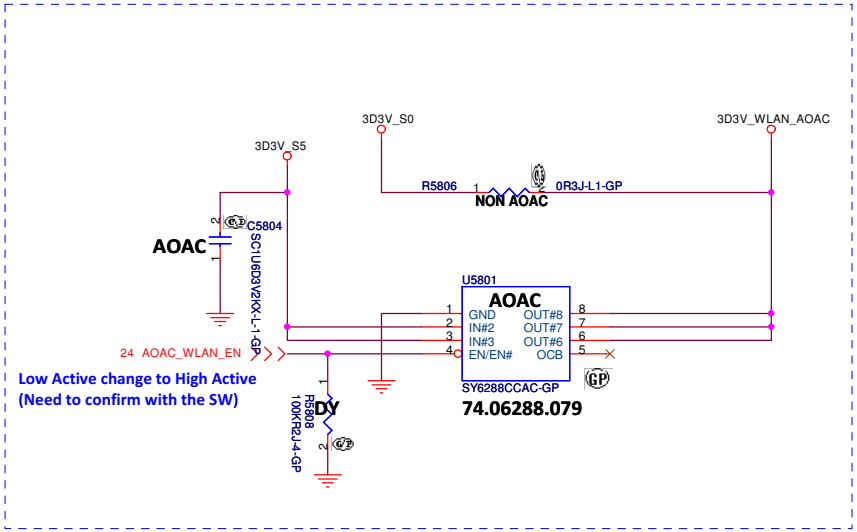
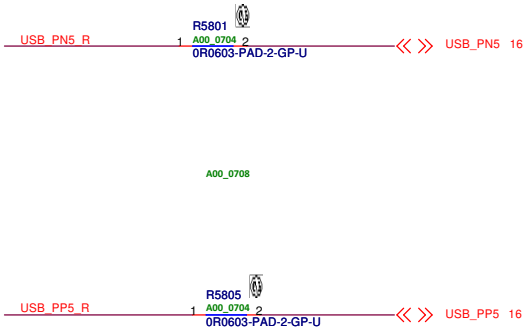
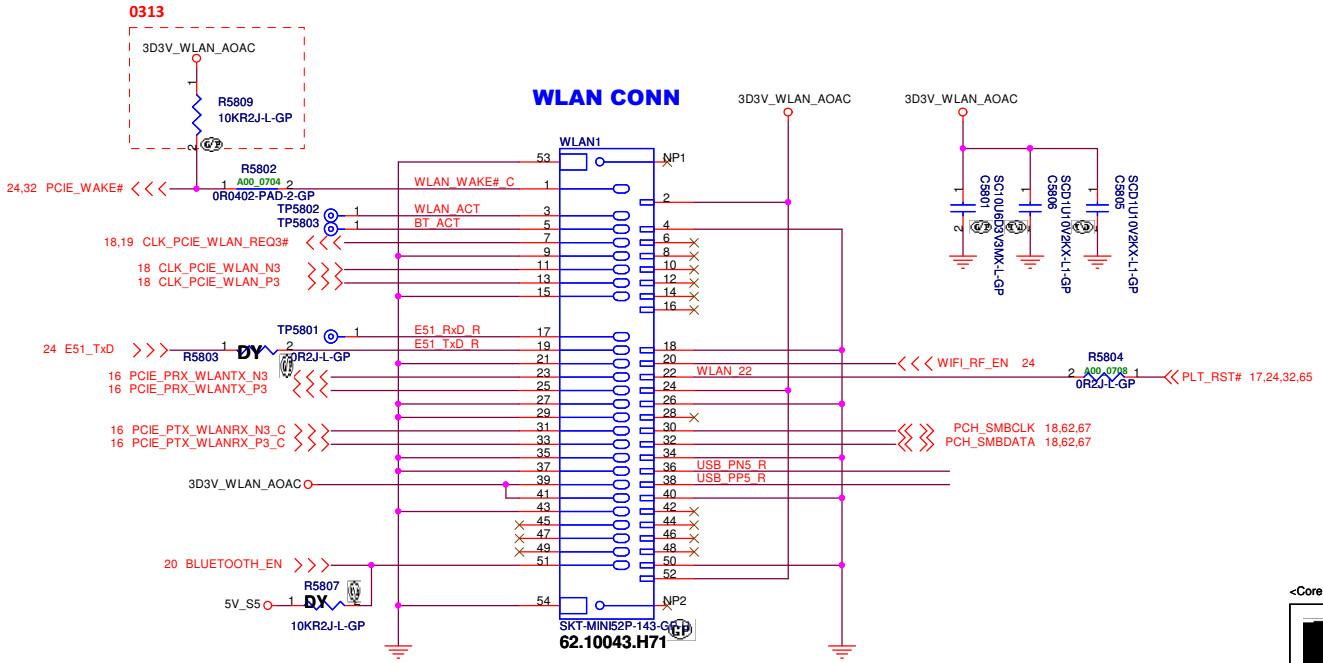
SSID = Wireless

Change power switch(Active High)







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	WLAN/BT	
Size: A3	Document Number: Hadley 14"	Rev: A00
Date: Wednesday, August 14, 2013	Sheet 58 of 107	

<Core Design>

Wistron Corporation
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Title

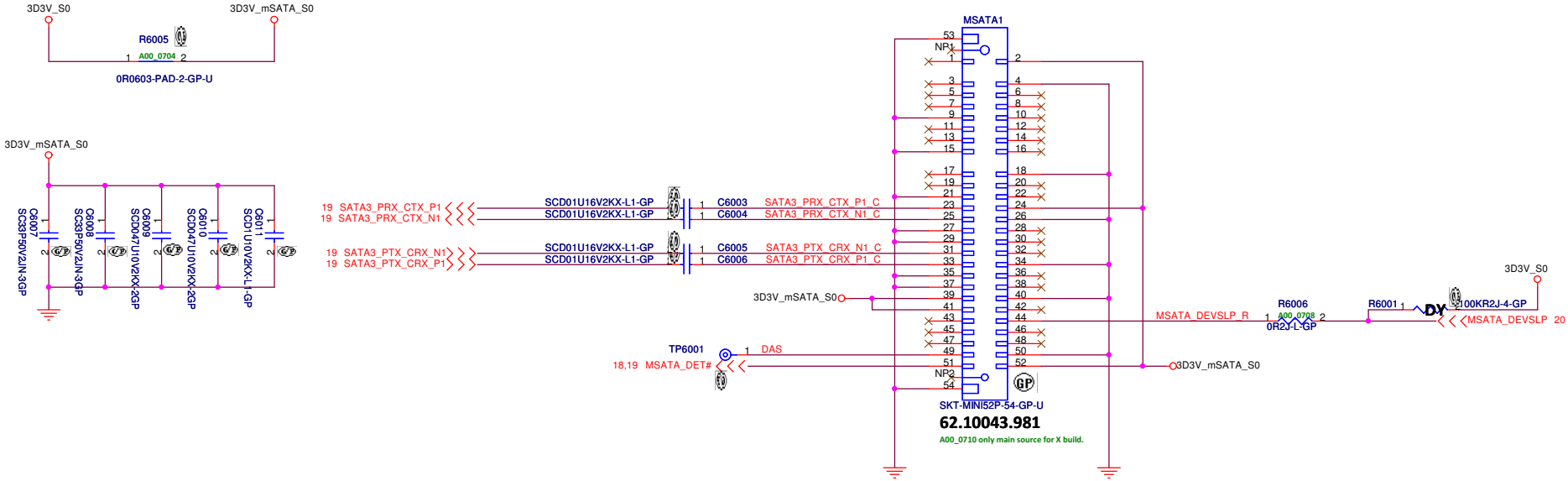
(Reserved)

Size	Document Number	Rev
A4	***Hadley 14"***	***A00***

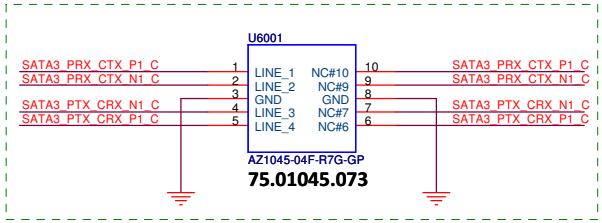
Date: Wednesday, August 14, 2013 Sheet 59 of 107

SSID = mSATA

MSATA CONN



X02_0515



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

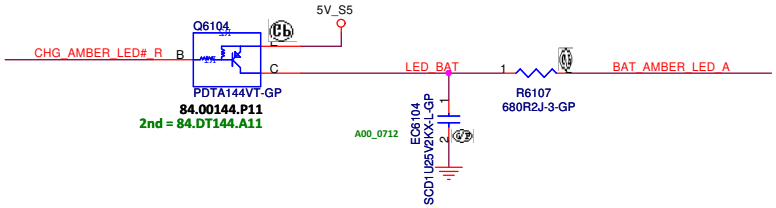
Title: Reserved

Size: A3 | Document Number: Hadley 14" | Rev: A00

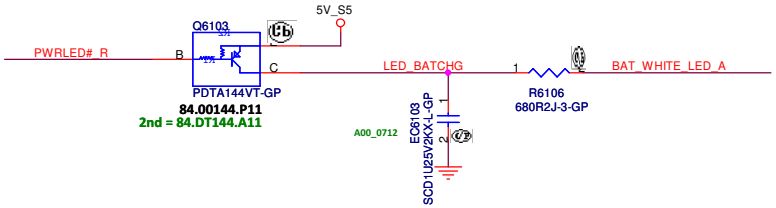
Date: Wednesday, August 14, 2013 | Sheet 60 of 107

SSID = User.Interface

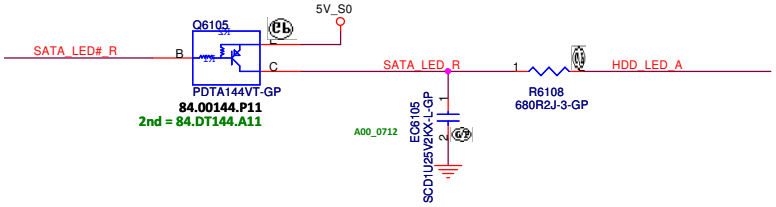
Battery LED1(Amber_LED)
LOW actived from KBC GPIO

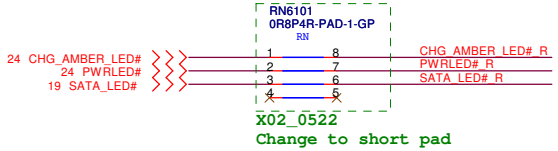


Battery LED2(White_LED)
LOW actived from KBC GPIO



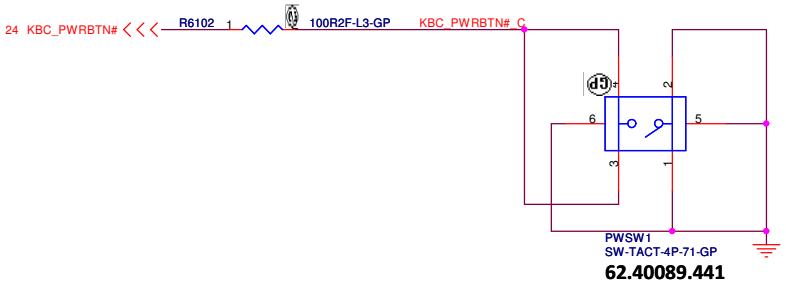
SATA HDD LED
LOW actived from PCH GPIO



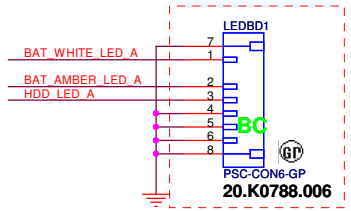


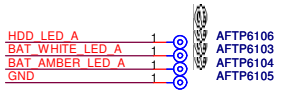
X02_0522
Change to short pad

PWRBTN



LED board CONN
0313





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bar/Power Button

Size: A3 | Document Number: Hadley 14" | Rev: A00

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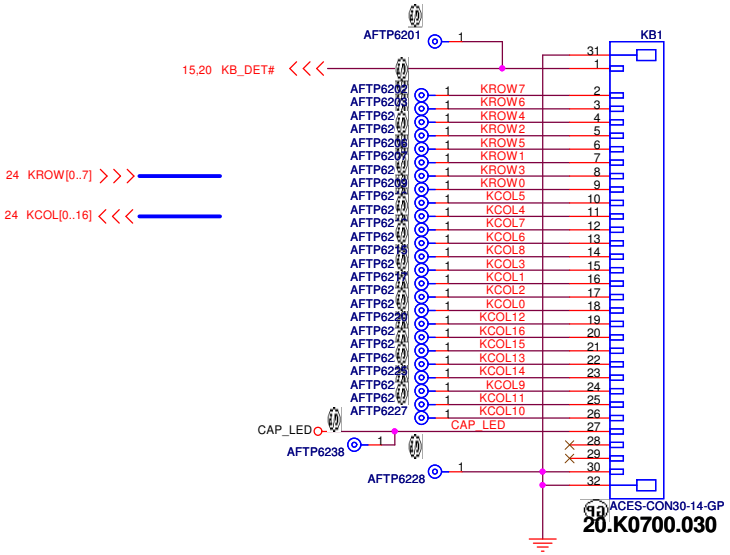
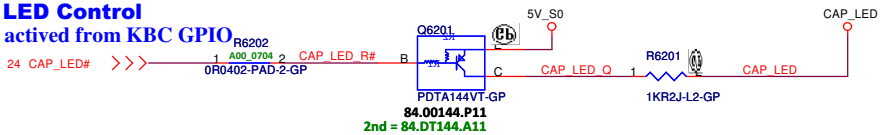
SSID = KBC

Internal Keyboard Connector

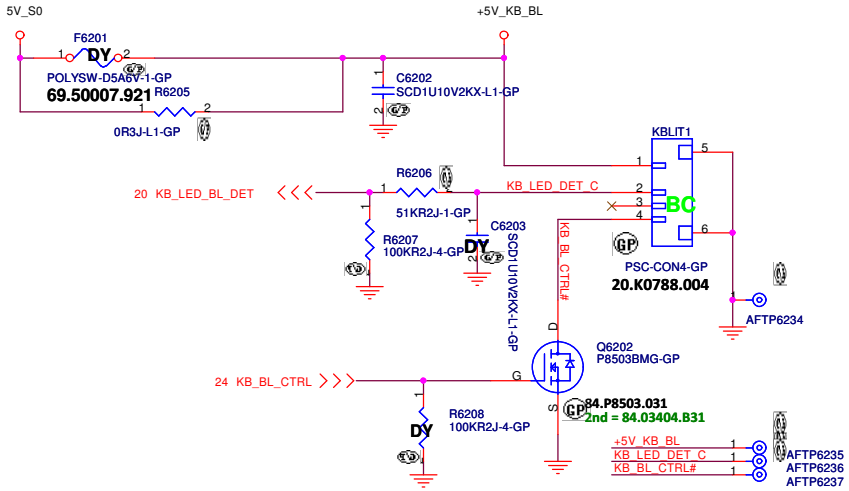


CAP LED Control

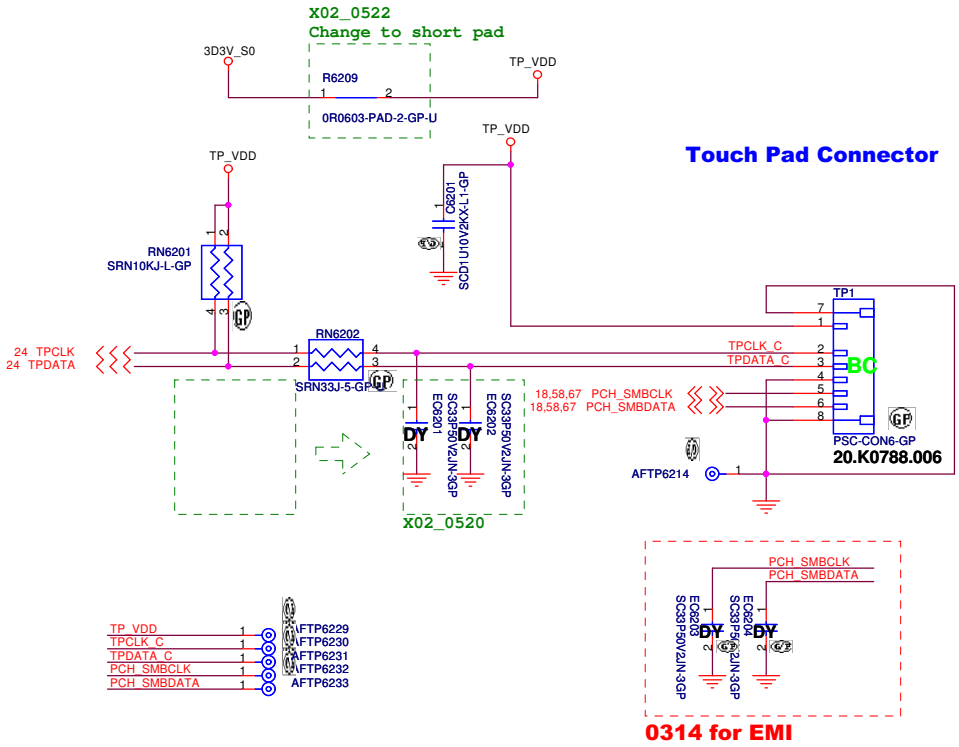
LOW actived from KBC GPIO



1109 Add KB backlit



SSID = Touch.Pad



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Title: **Reserved**

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SSID = User.Interface

<Core Design>

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Title: *IO Board Connector*

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A4	*Hadley 14"*	*A00*

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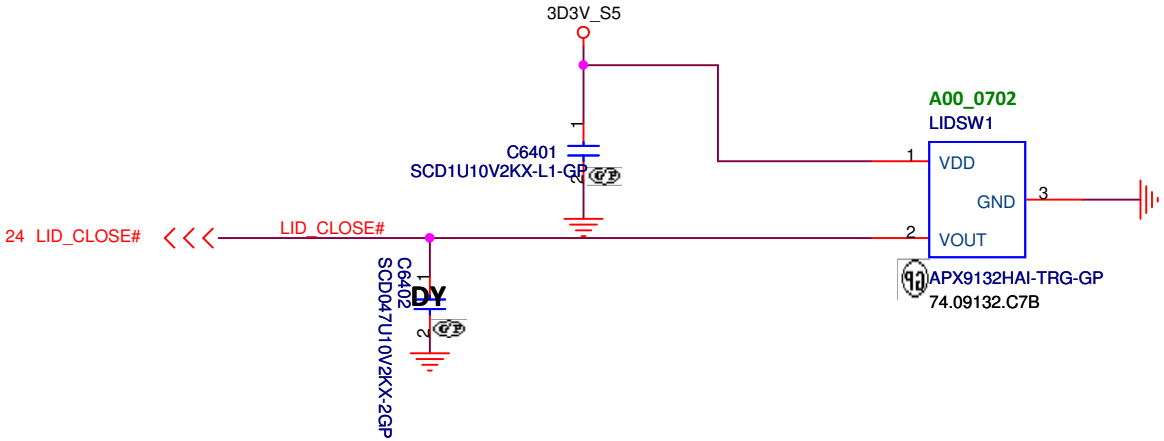
SSID = User.Interface



<Core Design>

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Title: ***Hall Sensor***

Size	Document Number	Rev
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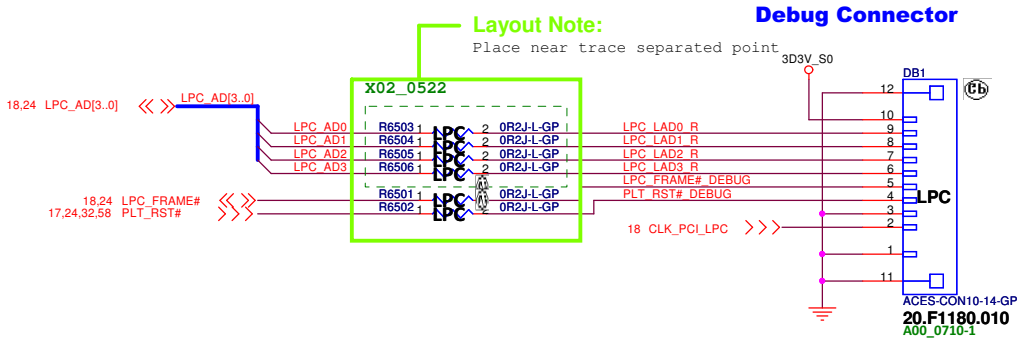
SSID = DEBUG PORT



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Title: ***Dubug connector***

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Title

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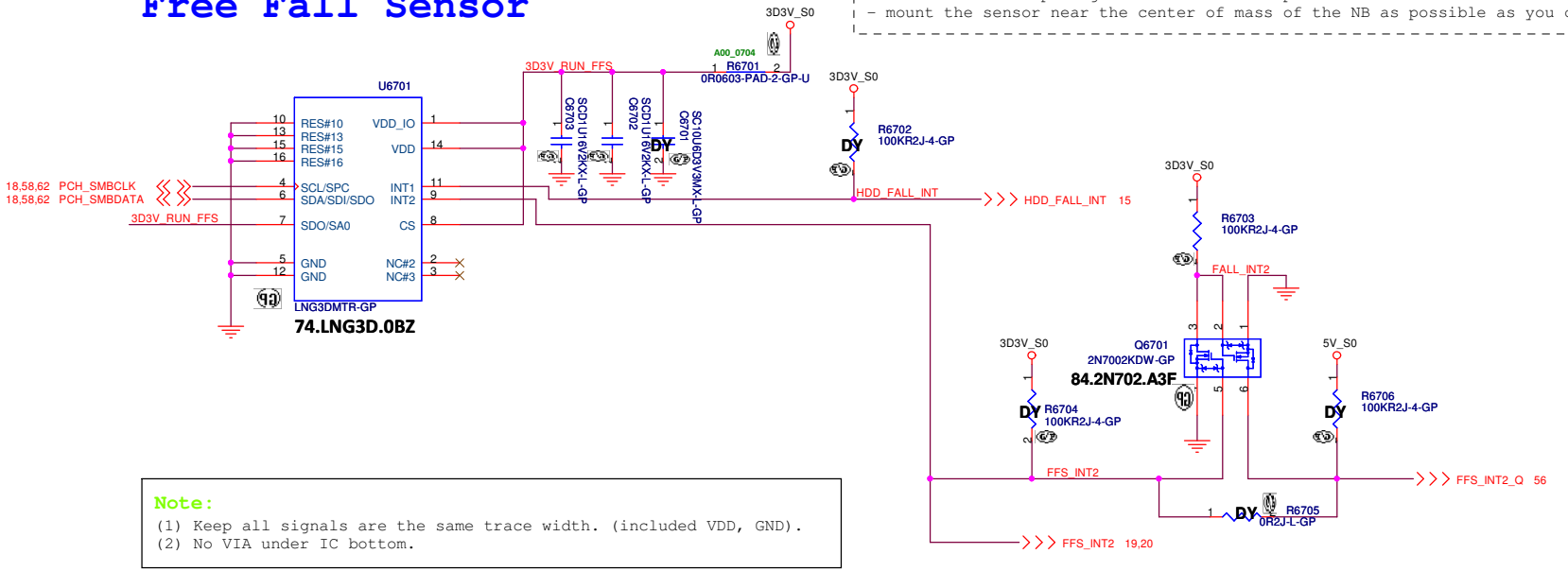
SSID = User.interface

Free Fall Sensor

Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title	Free Fall Sensor	
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Title: Reserved

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Title: ***Reserved***

Size	Document Number	Rev
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SSID = User.Interface

HS1 STF237R128H42-1-GP — 34.4GD01.001
HS2 STF237R128H42-1-GP — 34.4GD01.001
HS3 STF237R128H42-1-GP — 34.4GD01.001
HS4 STF237R148H67-GP — 34.4K501.001

PAD1 HT8BE9R24-U-45-GP — ZZ.00PAD.941
PAD2 HOLE237R95-GP — ZZ.00PAD.921
PAD3 HOLE237R95-GP — ZZ.00PAD.921

PAD4 HTE10BE10R32-R-55-GP — ZZ.00PAD.K91
PAD5 HTE10BE10R32-R-55-GP — ZZ.00PAD.K91
PAD8 HTE10BE10R32-R-55-GP — ZZ.00PAD.K91

0318 for EMI

HS5 SPRING-16-GP — 34.43E28.001
HS6 SPRING-28-GP — 34.41T19.001
HS7 SPRING-16-GP — 34.43E28.001
HS12 SPRING-16-GP — 34.43E28.001

PAD6 HT8BE9R24-U-45-GP — ZZ.00PAD.941
PAD7 HT8BE9R24-U-45-GP — ZZ.00PAD.941

For EMI

X02_0527
EC8603 change to 1000p for EMI

0314 for EMI
+DC_IN
+SDC_IN
0326 for EMI
EC8601 SCD1U25V2KX-L-GP
EC8603 SC1KP50V2KX-L-1-GP

DCBATOUT
EC8604 SCD1U25V2KX-L-GP
0321 for EMI
EC8605 SCD1U25V2KX-L-GP
EC8606 SC1KP50V2KX-L-1-GP
EC8607 SCD1U25V2KX-L-GP
EC8608 SC1KP50V2KX-L-1-GP
EC8609 SC1KP50V2KX-L-1-GP
EC8610 SCD1U25V2KX-L-GP

X02_0520
For I7 ESD issue
DCBATOUT
5V_S5
SC10U25V3MX-GP
EC8635
EC8636
EC8637

X02_0627
EC8614 change to 1000p for EMI

5V_S5
EC8611 SCD1U25V2KX-L-GP
EC8612 SC1KP50V2KX-L-1-GP
EC8613 SCD1U25V2KX-L-GP
0321 for EMI
0314 for EMI
EC8614 SC1KP50V2KX-L-1-GP
EC8615 SCD1U25V2KX-L-GP
EC8616 SCD1U25V2KX-L-GP
EC8638 SC10U6D3V2MX-GP-U
EC8639
EC8640 SC10U6D3V2MX-GP-U
EC8641 SC10U6D3V2MX-GP-U
EC8642 SC10U6D3V2MX-GP-U

X02_0520
For I7 ESD issue

1D35V_S3
EC8643 SC10U6D3V2MX-GP-U
EC8644
EC8645
EC8646 SC47U4V3MX-GP
0D675V_S0
EC8647 SC47U4V3MX-GP
EC8648 SC10U6D3V2MX-GP-U
EC8649 SC10U6D3V2MX-GP-U

X02_0520
For I7 ESD issue

A00_0627
EC8647 change to 47u

For RF

X02_0527
EC8617 change to 1000p for EMI

+DC_IN
0314 for RF
EC8617 SC1KP50V2KX-L-1-GP
0D675V_S0
EC8628 SCD1U25V2KX-L-GP
EC8629 SCD1U25V2KX-L-GP
3D3V_S5
EC8630 SCD1U25V2KX-L-GP

DCBATOUT
0326 for RF
0321 for EMI
EC8618 SC1KP50V2KX-L-1-GP
0326 for RF

5V_S5
EC8624 SCD1U25V2KX-L-GP
0326 for RF
0321 for EMI
EC8626 SC1KP50V2KX-L-1-GP
EC8627 SC1KP50V2KX-L-1-GP
VCC_CORE
EC8631 SCD1U25V2KX-L-GP
EC8632 SCD1U25V2KX-L-GP
EC8633 SCD1U25V2KX-L-GP
EC8634 SCD1U25V2KX-L-GP

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Title: UNUSED PARTS/EMI Capacitors
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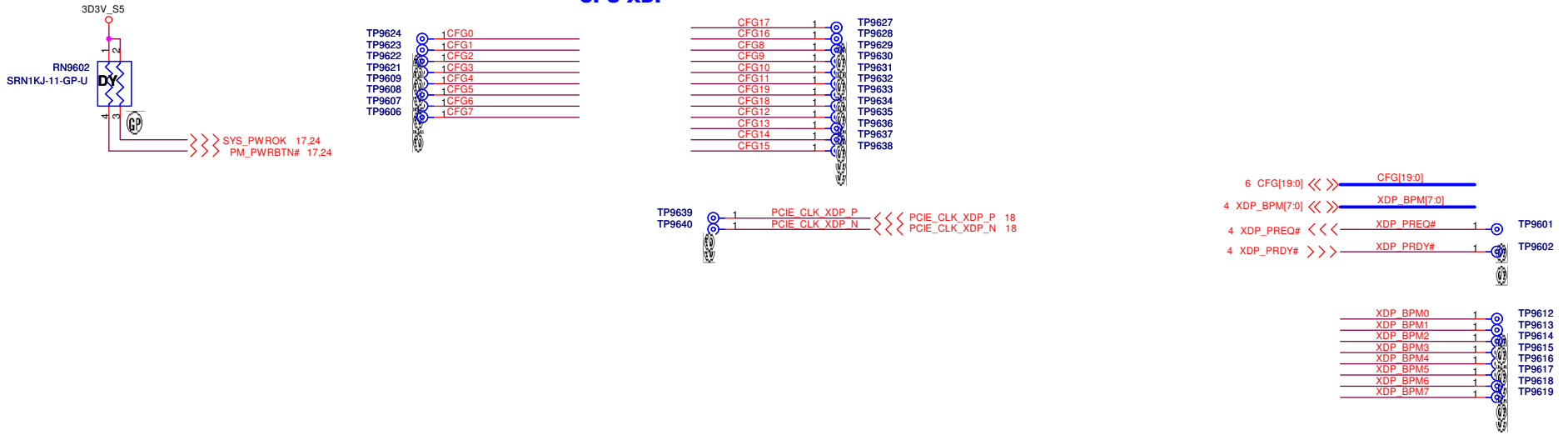
SSID = XDP

CPU XDP



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Title	CPU XDP	
Size A3	Document Number Hadley 14"	Rev A00
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PCH Strapping

Name	Schematics Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION

SMBus ADDRESSES

I²C / SMBus Addresses	CHIEF RIVER ORB	
Device	Address	Bus
EC SMBus 1		
Battery 0	0x16	BAT_SCL/BAT_SDA
CHARGER	0x12	BAT_SCL/BAT_SDA
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA
EC SMBus 2		
Battery 1	0x16	SML1_CLK/SML1_DATA
PCH	0x96 & 0x94	SML1_CLK/SML1_DATA
Discrete VGA Thermal	0x9C or 0x9E	SML1_CLK/SML1_DATA
PS8321 HDMI level shifter	0x96 & 0X97	SML1_CLK/SML1_DATA
NCT7718W	0x98 or 0x99	SML1_CLK/SML1_DATA
EC SMBus 3		SMB2_CLK/SMB2_DATA
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA
PCH SMBus		
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK
G-Sensor		PCH_SMBDATA/PCH_SMBCLK
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	

USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

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Title: Table of Content

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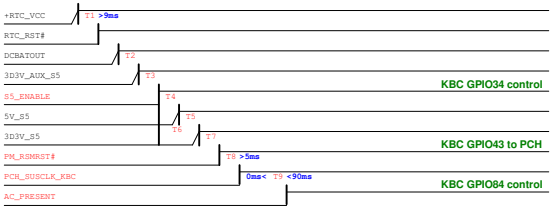
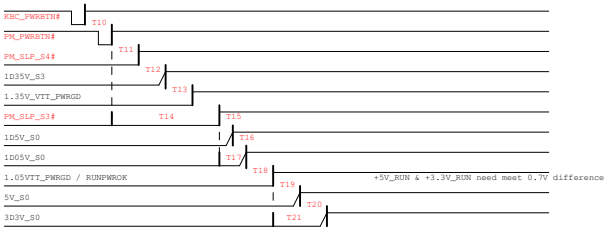
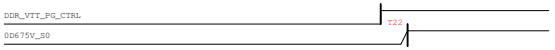
Intel-Power Up Sequence

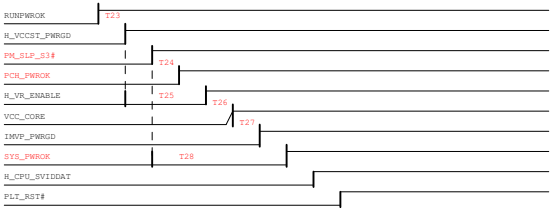
(AC mode)

Red printings:KBC GPIO involved



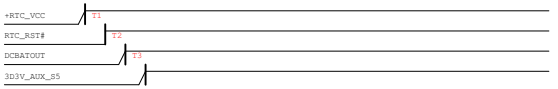


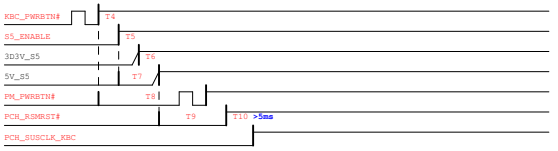


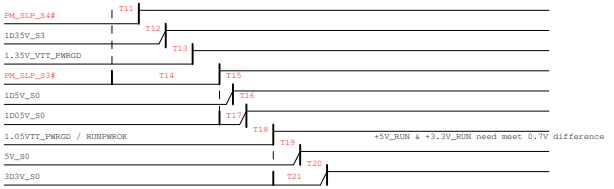


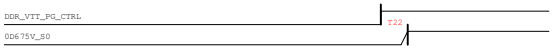
(DC mode)

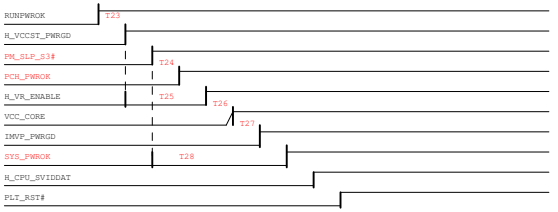
Red printings:KBC GPIO involved



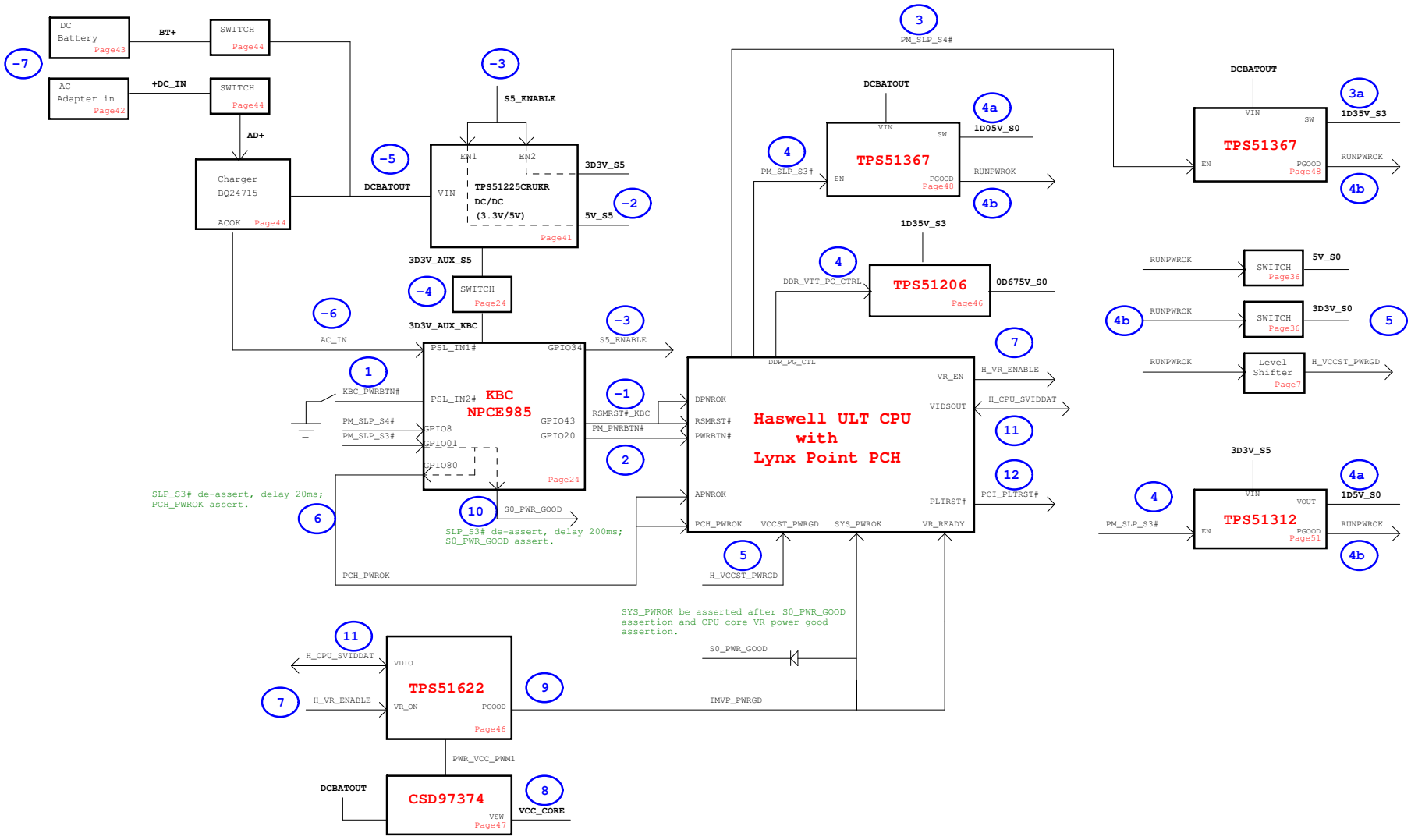








Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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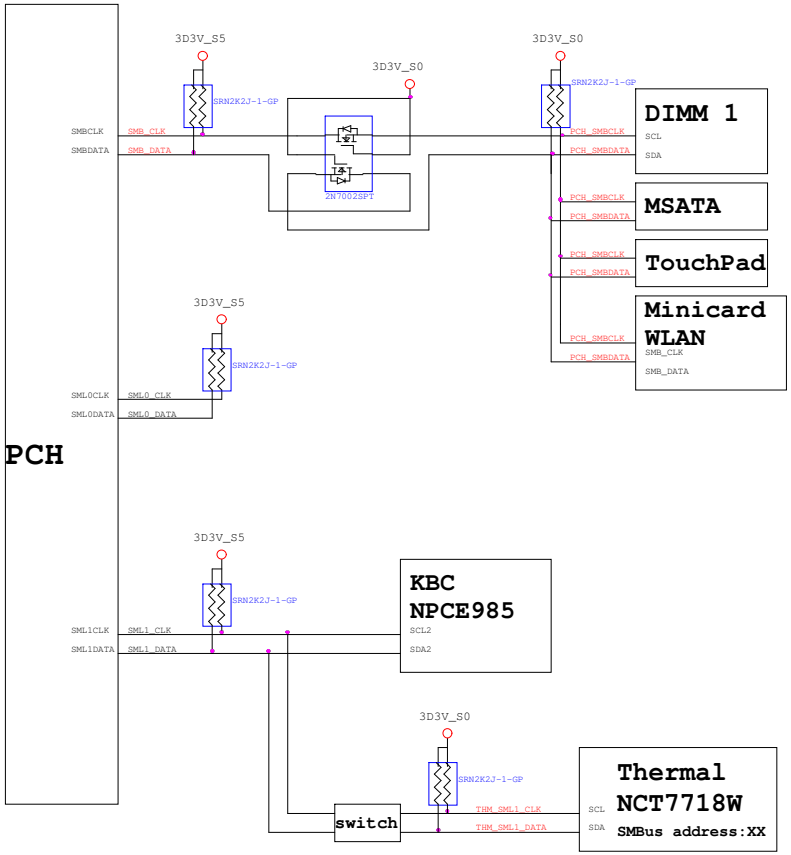
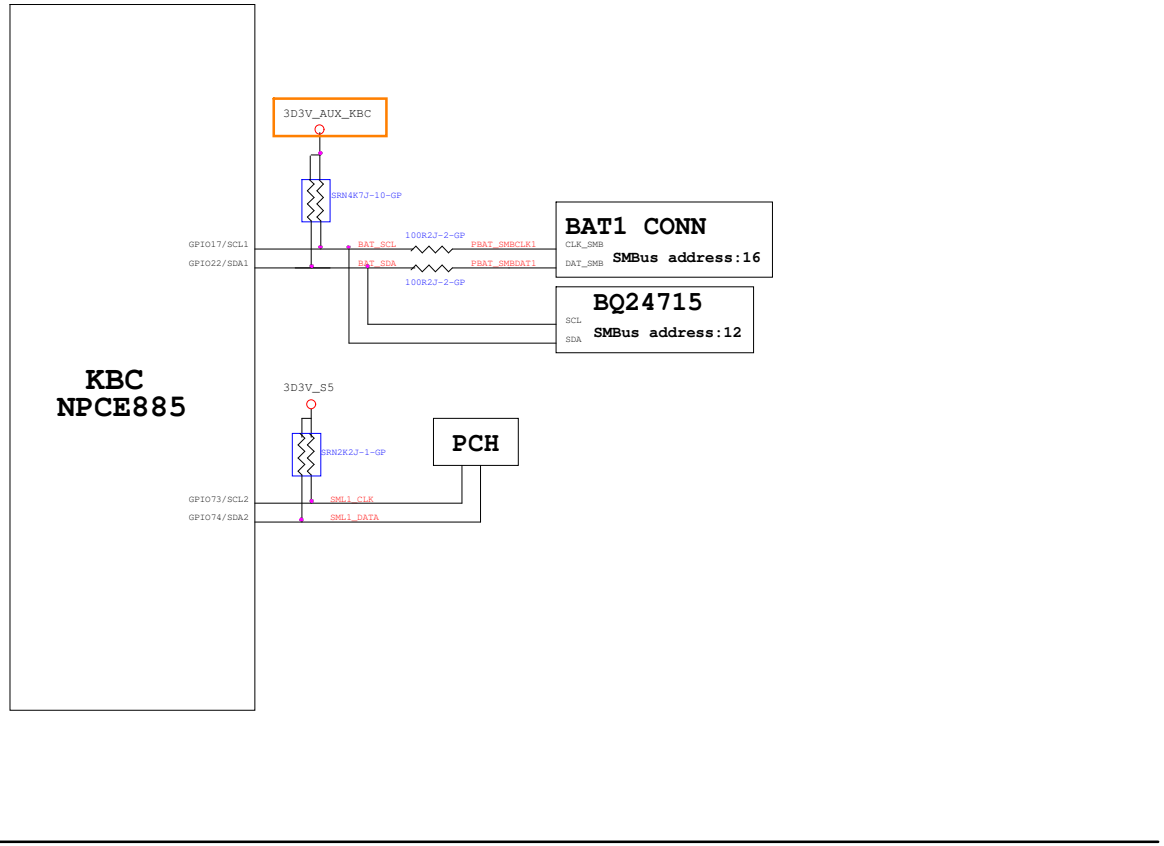
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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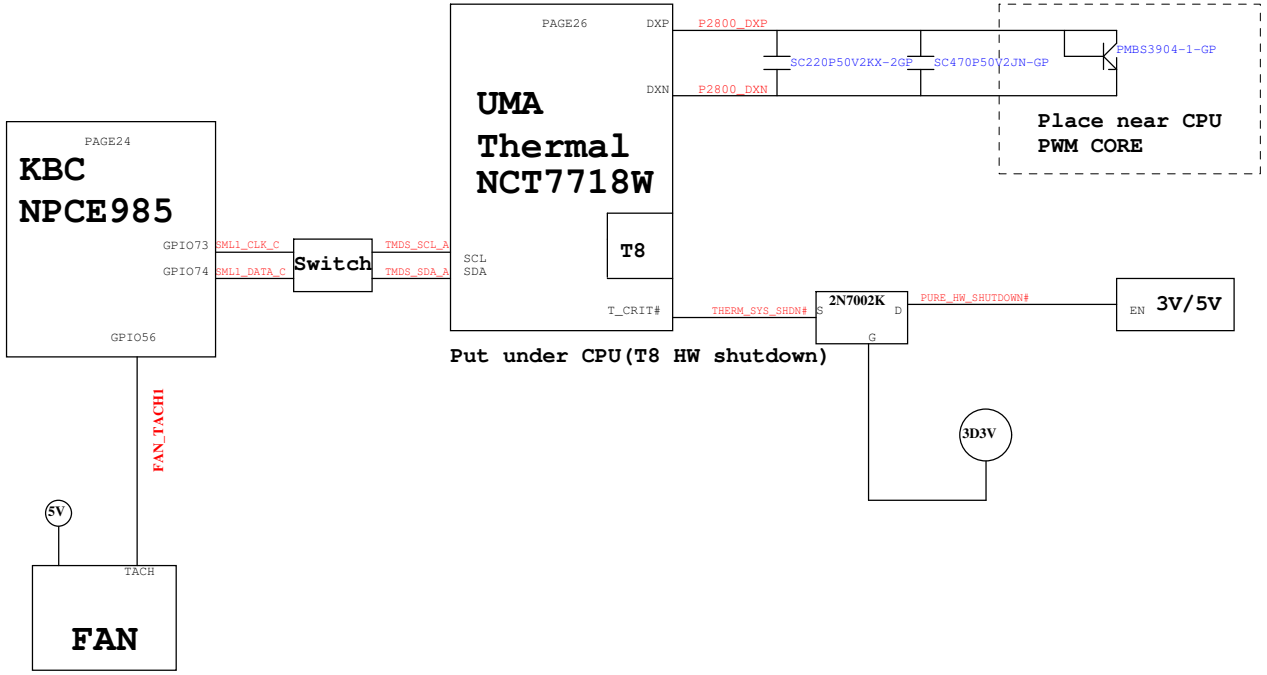
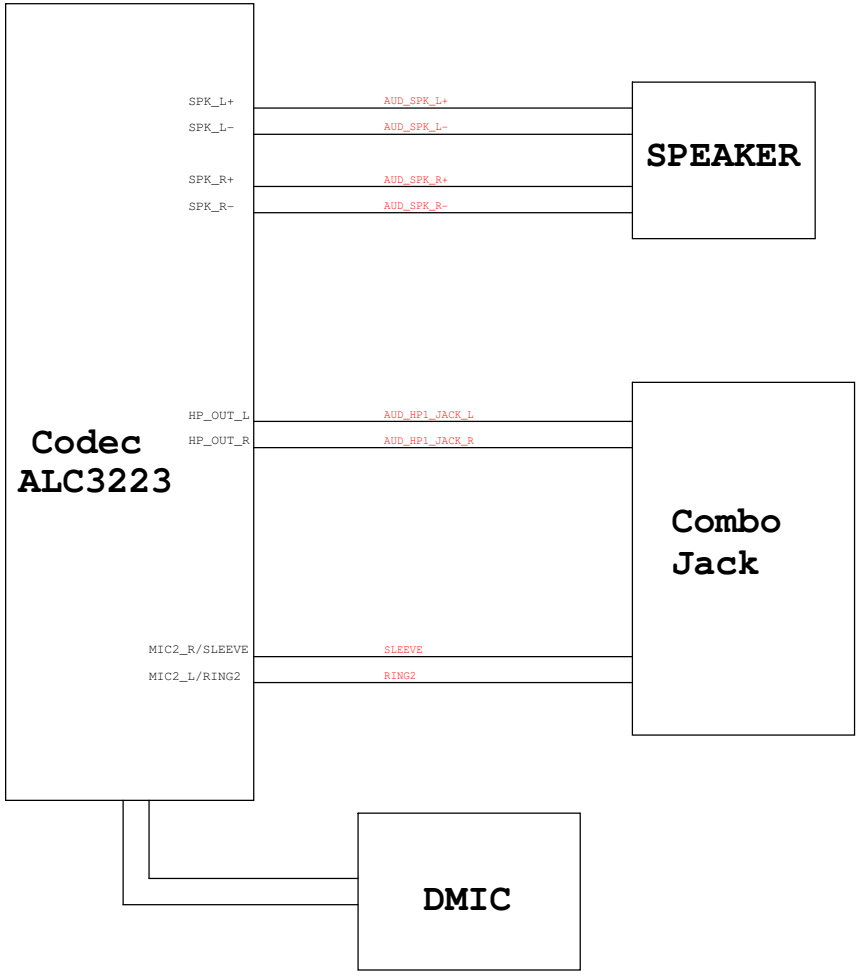
Thermal Block Diagram



Audio Block Diagram



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Item	Pg.	Date	Description	Owner
CPU	7	0313	1.Add C704,C705 D1U cap PD (need close to CPU side)	EE
PCH	20	0313	2.Change R2001,R2007,R2015,R2017,R2019,R2020,R2021,R2023 short pad to 0 ohm.	EE
PCH	15	0313	3.follow DOH50 change R1509 from 10K to 100K	EE
FFS	15,56	0313	4.stuff R1503,R5614 for FFS	EE
KBC	24	0313	5.change R2404 from 10K to 20k for PT config	EE
PCH	18	0313	6.RN1805 8P4R change to 4P2R(RN1808,RN1805) by power well different	EE
SPI	25	0313	7.Remove SKT25 colay	EE
PCH	17	0313	8.change PCH_WAKE# PH R1705 to 1K ohm and change RN1701 to 4P2R 10K	EE
WLAN	58	0313	9.Add R5809 pull high 10k for wifi wake	EE
AUDIO	27,28	0313	10.Delet LINE2_L trace and change to mono_out for tweeter by vendor	EE
LED	61	0313	11.change LEDBD1 P/N to 20.K0788.006 for 6 pin by ME	ME
	17,62, 86	0314	12.Add CAP EC6204, EC6203, EC1702, EC8619, EC8620, EC8621, EC8622, EC8623, EC8604, EC8605, EC8606, EC8609, EC8610, EC8617, EC8601, EC8602, EC8603, EC8614, EC8616, EC8615 ,EC8613, EC8612, EC8611, EC8627, EC8626, EC8625 for EMI	EMI
	18,26	0315	13.SWAP RN2603 and RN1808 net by layout	Layout
LCD	52	0315	14.change TOUCH_PANEL_INTR# to input direction	EE
LCD	24	0315	15.change R2445 to D2402 and dummy for TOUCH_PANEL_INTR#	EE
USB	34	0315	16.DUMMY C3419,C3413,C3411 and change C3414 to 1u by layout location	EE
KBC	24	0315	17.Reserve R2445 for PSL_IN2# Issue	EE
HDMI	54	0315	18.follow DOH50 to change D5401 P/N	EE
	29,44, 47	0315	19.change PR4704,U2901,PQ4408 P/N for BOM merge	EE
HDD	19,20, 56	0315	20.Reserve R5615 to GND and change MCP_GPIO35 to HDD_DET# for sku option	EE
LCD	24	0315	21.Dummy R2443 for panel site have pull high by vendor	EE

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Item	Pg.	Date	Description	Owner
PCH	18	0318	1.change CLK_PCIE_REQ port by intel EDS	EE
	86	0318	2.HS5, HS6, HS7, HS12 add EMI spring	EMI
Charger	44	0318	3.Dummy PR4459 and stuff PR4458 for 15V_S5 schematic	POWER
Charger	44	0318	4.Dummy PR4441, PR4440, PR4442, PR4447 for DOH40 BATT not unplug	POWER
Charger	44	0318	5.Dummy PQ4412, PR4452, PR4454, PC4409 and PC4431 for DOH40 BATT not unplug	POWER
Charger	44	0318	6.Combin Charger cell pin schematic in PQ4412 and combin AC_IN# and H_PROCHOT# schematic in PQ4413	POWER
Charger	44	0318	7.Add PC4414 by power	POWER
Charger	44	0318	8.PR4436 change to 220K by power	POWER
3V/5V	45	0318	9.Dummy PC4525, PC4526, PC4532, PC4533, PC4534, PC4527, PD4502 and PD4503 for 15V_S5 schematic	POWER
memory	12,13	0318	10.update RAM1~RAM8 P/N and PCBfootprint for memory size	EE
PCH	21	0320	11.Change U2101 part number from 74.22965.093 to 74.59147.093 by meet intel SPEC; remove C2140	EE
USB	35	0320	12.Change USB charger solution and add USB SW	EE
CPU	7	0320	13.Add TP for N61,N59 by MOW update	EE
AUDIO	28	0320	14.Change tweeter speaker AMP solution for POP noise	EE
PCH	18	0322	15.Change PCIE CLK and REQ# Port mapping	EE
HDMI	54	0322	16.Stuff R5427,R5428 and change R5410 to 487ohm for HDMI fine tune	EE
AUDIO	28	0322	17.Change U2801 to TPA2011D1 for POP noise Change R2805 to 3D3v_S0 and DY Change R2808/R2806 to 165Kohm by vendor Change C2805/C2807 to 0.1u by vendor Add R2813,R2814,R2815,R2816,C2808,U2802,U2803,Q2801 for depop	EE
	52,86	0322	18.Add EC8631~EC8634 0.1u on VCC_CARE and change EC5208~EC5213 to 0402 SIZE for RF	RF
	34,52	0322	19.Stuff TR3403,TR3407,TR5202 CMC,U3401,U3402 TVS and DY R3409,R3411,R3403,R3403,R5214 ,R5217 for EMI	EMI

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Item	Pg.	Date	Description	Owner
	54	0322	1.Change R5442,R5443,R5444,R5445 to ER5442,ER5443,ER5444,ER5445 150ohm and stuff for EMI	EMI
	54	0322	2.Remove TR5402,TR5403,TR5404,TR5405 for EMI	EMI
	27	0322	3.Change R2714,R2716,C2723,C2724 to ER2714,ER2716 33ohm ,EC2723,EC2724 22p and stuff for EMI	EMI
	29	0322	4.Stuff EC2901, EC2902, EC2903, EC2904, EC2910, EC2911 1000p for EMI	EMI
	44	0322	5.Add EC4401 1000p on +VCHGR for EMI	EMI
	43	0322	6.Stuff EC4304 1000p on BT+ for EMI	EMI
	86	0322	7.Stuff EC8609,EC8606,EC8618,EC8608 1000p on DCBATOUT for EMI	EMI
	86	0322	8.Stuff EC8610,EC8605 0.1u on DCBATOUT for EMI	EMI
	27	0322	9.Add EC2710~EC2714 0.1u AGND to GND for EMI	EMI
	52	0322	10.Stuff EC5203 10p on LCD_BRIGHTNESS for EMI	EMI
	18	0322	11.Stuff EC1803 22p on SPI_CLK for EMI	EMI
	18	0322	12.Stuff EC1801 22p and R1805 33 ohm on CLK_PCI_KBC for EMI	EMI
	4	0322	13.Reserve EC401 1000p on XDP_TRST# for EMI	EMI
	4	0322	14.Reserve EC402 1000p on H_CPUPWRGD for EMI	EMI
	7	0322	15.Reserve EC701 1000p on H_VCCST_PWRGD for EMI	EMI
	86	0322	16.Stuff EC8626,EC8627,EC8612 1000p on 5V_S5 for EMI	EMI
	86	0322	17.Stuff EC8611 0.1u on 5V_S5 for EMI	EMI
	52	0322	18.Stuff EC5202 1000p on 3D3V_CAMERA_S0 for EMI	EMI
	44,54	0326	19.change F5401,PD4402 symbol by net file check	EE
	86	0326	20.Remove EC8625, EC8623, EC8622, EC8621, EC8620, EC8619 by RF	RF
	86	0326	21.Audio codec: ER2716 change to 100 ohm; ER2714 change to 0 ohm; EC2723, EC2724 dummy EC2905, EC2906, EC2907, EC2908 change to 100pF	EMI

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Item	Pg.	Date	Description	Owner
	33	0326	1.Card reader: EC3302, EC3303, EC3305,EC3306, EC3307 change to 4.7pF	EMI
Charger	44	0326	2.Charger:Dummy PR4401, PR4420 and PQ4411 for DOH40 only 45W adapter Change PR4428 change to 113K by power Dummy PR4449 by power PG4407, PG4403, PG4404 and PG4405 change to ZZ.CLOSE.001 by power PU4405 chnage main source to 84.06675.030	POWER
VCORE	46,47	0326	3.Vcore:PR4609 change to 1.2K and PR4623 change to 11.8K by power PU4702 main source change to 84.03664.037 by power	POWER
0.675V	49	0326	4.0.675V:PU4902 change main source to 74.05338.079 by power Stuff PR4917 and Dummy PR4918 by power	POWER
DCIN	42	0326	5.DCIN:PU4201 chnage main source to 84.06675.030	POWER
PCH	18	0327	6.Change C1801 and C1802 to 15P by vendor	EE
HDMI	54	0327	7.HDMI:Remove R5434~R5441 0402 0 ohm and R5401~R5408 0603 0 ohm by HDMI vendor DY R5427,R5428 by EA test	EE
	86	0327	8.Delet EC8602 by EMI	EMI
CPU	18	0329	9.Change RN1803,RN1804 to R1813~R1816 10K ohm by Intel EDS	EE
CPU	19	0329	10.Change C1903 and C1904 to 15P by vendor	EE
VCORE	45	0402	11.Stuff PC4741, PC4726 and PC4739 and change PC4705 to 78.47322.2BL by power	POWER
Charger	44	0410	12.Change PL4401 to 68.2R21C.10Q by HALT test	EE
CPU	21	0509	13.Add C2148 0.47uF for VccDSW3_3 and DcpSusByp to address temporary inrush currents.	EE
HDMI	54	0509	14.Change HDMI1 to 22.10296.A61 by ME	EE
MSATA	60	0514	15.Reserved U6001 for EMI test	EMI
MSATA	60	0515	16.Change U6001 P/N to 75.01045.073 by EMI	EMI
KBC	24	0515	17.DUMMY RSTSW1	EE
AUDIO	28,29	0515	18.DUMMY Twitter function and remove EC2910, EC2911	EE
AUDIO	29	0515	19.Change SPK1 P/N to 20.F2060.004	ME

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Item	Pg.	Date	Description	Owner
KBC	24	0515	1.Change R2404 from 20K to 33k for ST config	EE
CPU	17,19	0520	2.Add D1901~D1904, EC1703~EC1708 for EMI	EMI
	24,45	0520	3.Add EC2423, EC2424, EC4501 for EMI	EMI
CPU	4,18	0520	4.Add ER411, EC403, EC1804 for EMI	EMI
TPAD	62	0520	5.Shift EC6201 and EC6202 to TPCLK_C and TpDATA_C for EMI	EMI
	86	0520	6.Add EC8635~EC8649 for EMI	EMI
CPU	17,19	0522	7.Remove D1901~D1904 and reserved EC1901~EC1904	EMI
	32	0522	8.CARD32 Change to RTS5227E	EE
HDMI	54	0522	9.Change R5410 to 390ohm	EE
		0522	10.Change R404, R711, R1101, R1102, R1103, R1104, R1105 R1238, R1501, R1807 , RN1806, R1904, R2101, R2103, R2105, R2108, R2112, R2117, R2118, R2401, R2402, R2408, R2409, R2410, R2417, R2427, R2428, R2430, R2440, RN2601, R2706, R2708, R2711, R2718, R2917, R3402, R3702, R3705, RN6101, R6209 to short pad	EE
	65	0522	11.Remove RN6501 and add R6503~R6506 for EE	EE
	19	0523	12.Remove EC1903, EC1904 and add TP1903, TP1904	EMI
CPU	11	0523	13.Change R1102 and R1103 P/N to ZZ.00PAD.M21	EE
	86	0527	14.Change EC8614, EC8617, EC8603 to 1000p for EMI	EMI
	4	0527	15.EC402, EC401 add 1KP for EMI	EMI
	86	0527	16.EC8635, EC8636, EC8637, EC8638, EC8640, EC8642, EC8643, EC8644, EC8645, EC8648, EC8649 add 10uF for EMI, just for I7 config	EMI
	86	0527	17.EC8646, EC8647 add 47uF for EMI, just for I7 config	EMI
	27	0527	18.Change EC2723, EC2724, EC2701, EC2702 to 5.6pF for RF request	RF
	46	0527	19.PR4623 change to 12.7K for power	EE
	44,45 46,48 49,51	0627	20.Change PR4430, PR4413, PR4406, PR4438, PR4417, PR4457, PR4455, PR4446, PR4520, PR4504, PR4502, PR4505, PR4621, PR4619, PR4616, PR4618, PR4624, PR4628, PR4627, PR4613, PR4801, PR4823, PR4832, PR4828, PR4834, PR4903, PR4912, PR4913, PR4923, PR4907, PR4919, PR4909, PR4914, PR5108 to short pad	EE

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Item	Pg.	Date	Description	Owner
	44	0627	1.Change PD4405 to short pad	EE
	24	0627	2.Change R2404 to 64.9K	EE
	15	0628	3.HDD_FALL_INT connect to PIRQB#	EE
	20	0814	4. Add Micron into memory matrix	EE

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