Selek 15" Schematic

CFL-H refresh

NVIDIA N18P-G0

(4GB) N17P-G0-K1 (3GB)

2019/04/03

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

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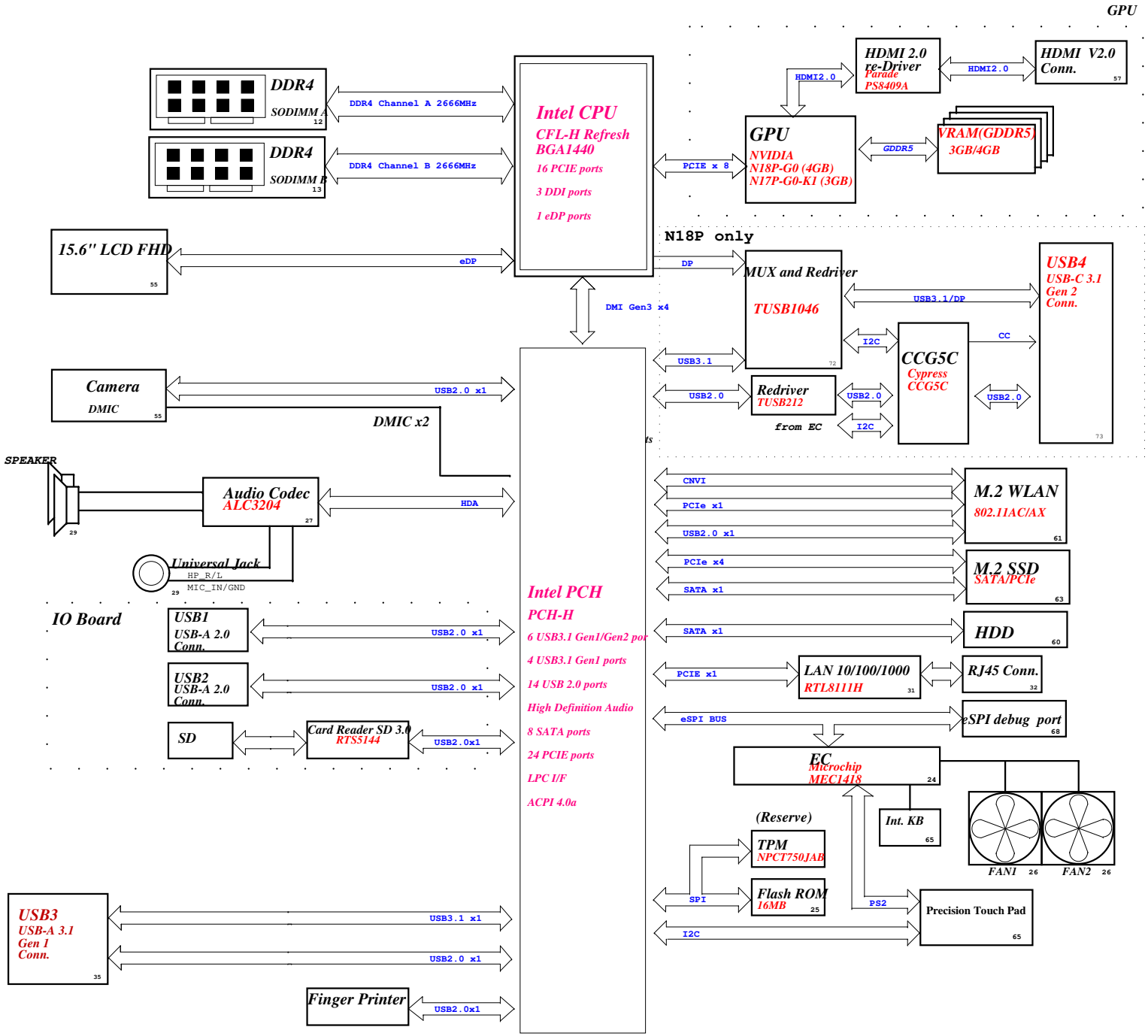
Project Code : 4PD0H7010001
PCB P/N : 18825-1
Revision : A00

Selek CFL-H refresh Block Diagram



CHARGER	
ISL88739	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power	
NCP81208MNTXG	46~50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS	
RT8231AGQW-GP APL5930KAI-TRG	51
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 DD6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V	
	11
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A	
AOZ2262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE	
ISL62771HRTZ-GP-U	85
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

Selek CFLH N17P

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Title: Block Diagram

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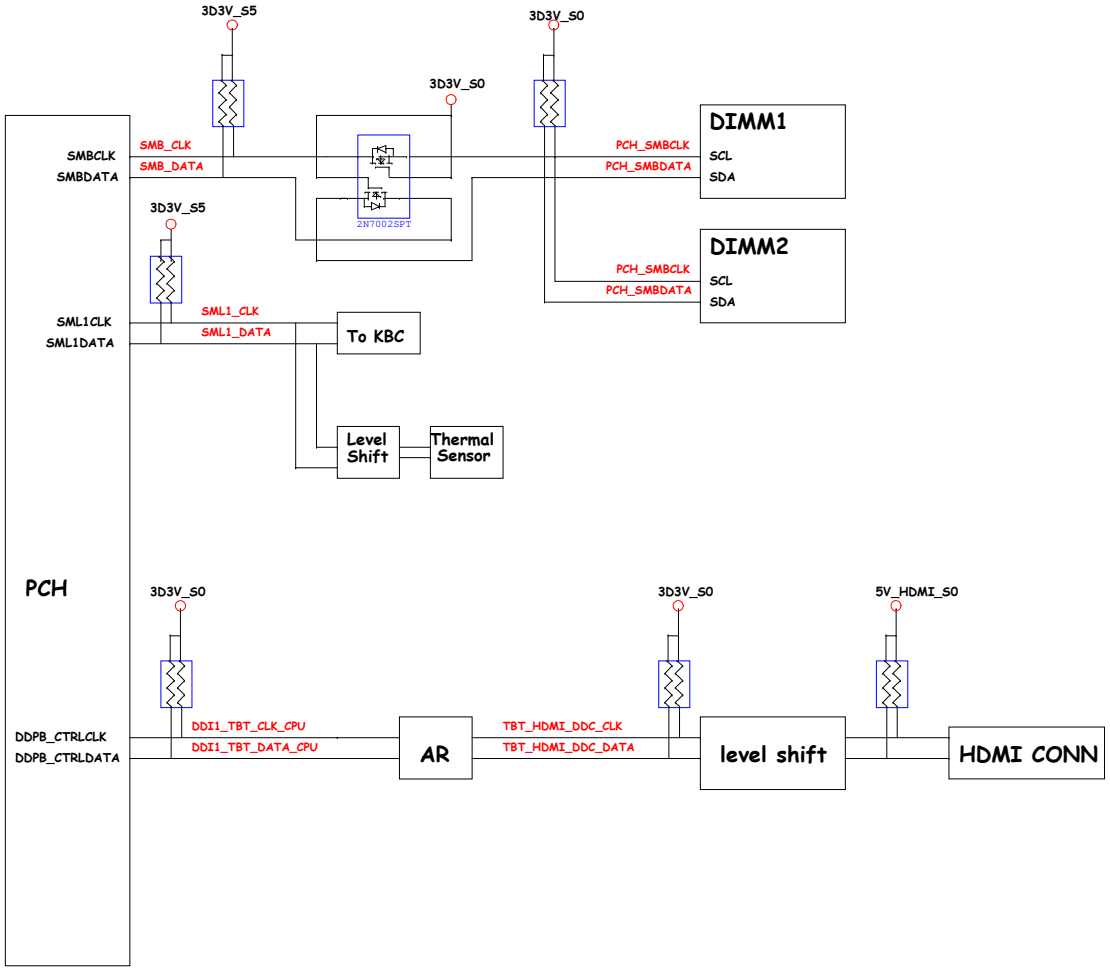
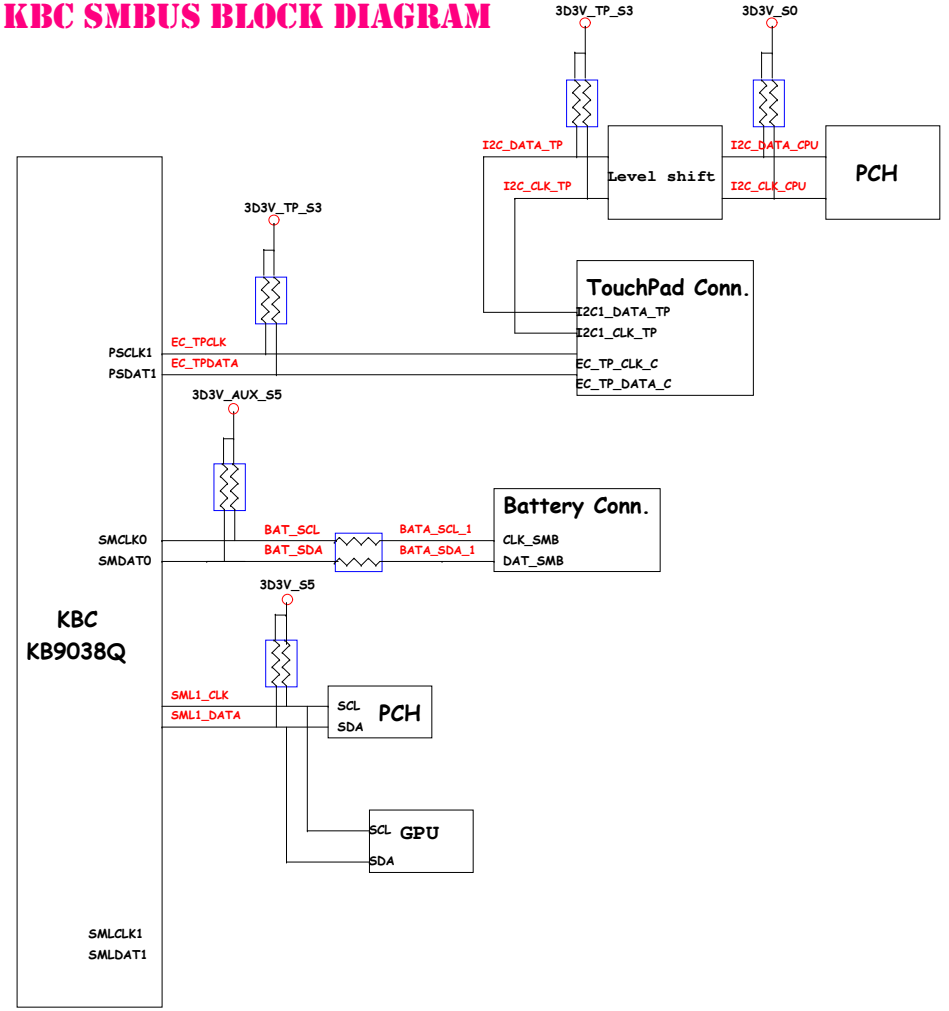
PCH SMBUS BLOCK DIAGRAM



KBC SMBUS BLOCK DIAGRAM



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Title: SMBUS BLOCK DIAGRAM

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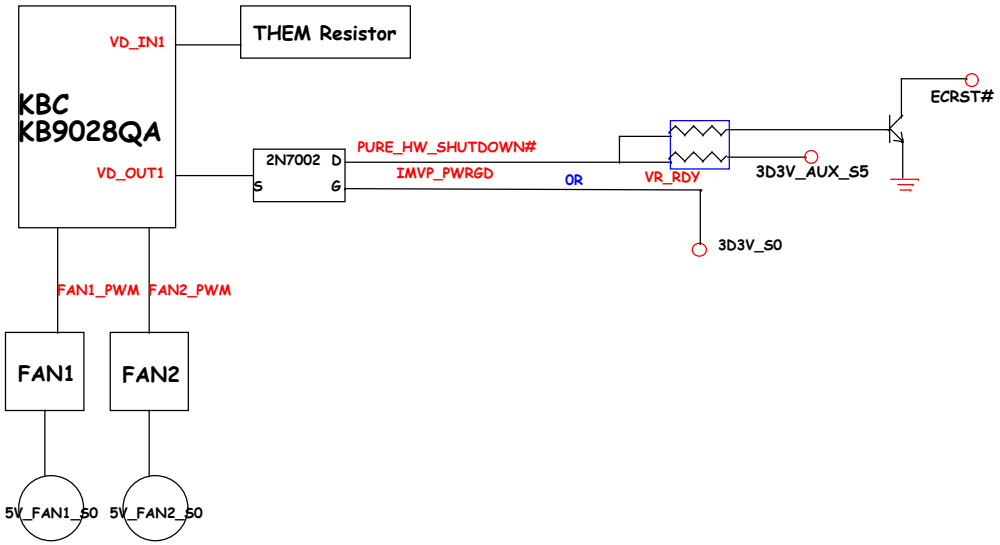
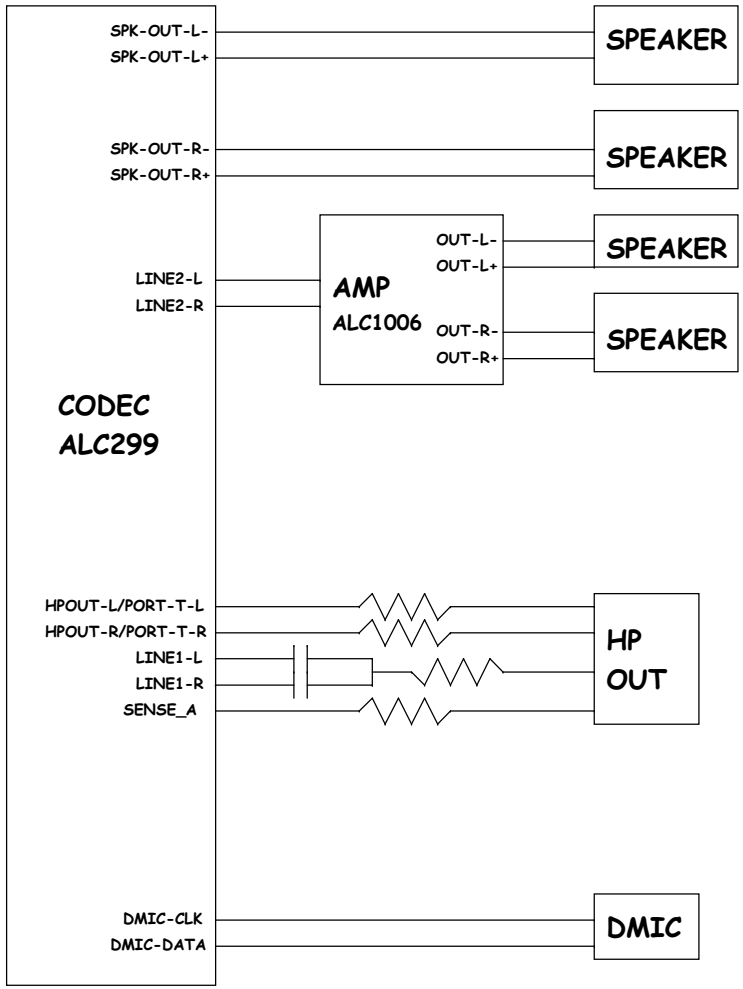
THERMAL BLOCK DIAGRAM



AUDIO BLOCK DIAGRAM



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Title	Thermal /AUDIO Block Diagram	
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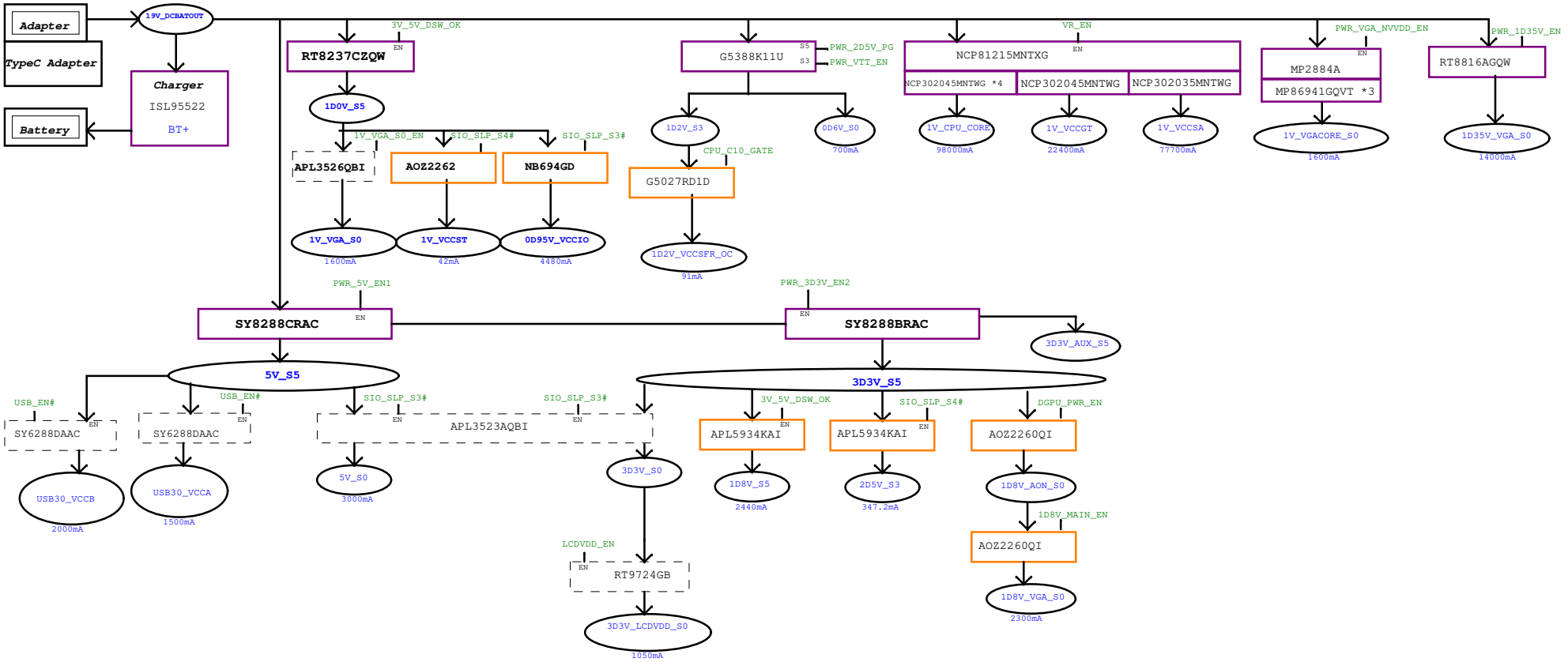

Power Shape

Regulator | LDO | Switch

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Title: Power Block Diagram

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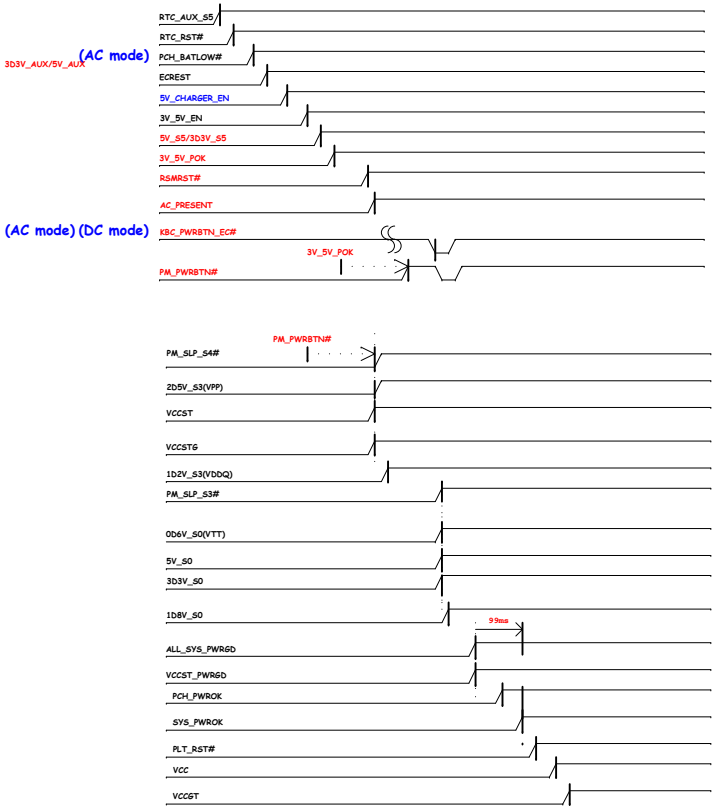
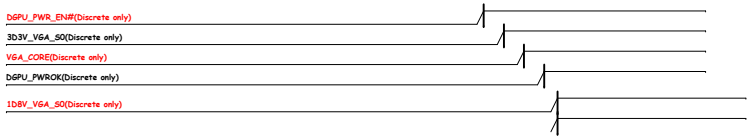
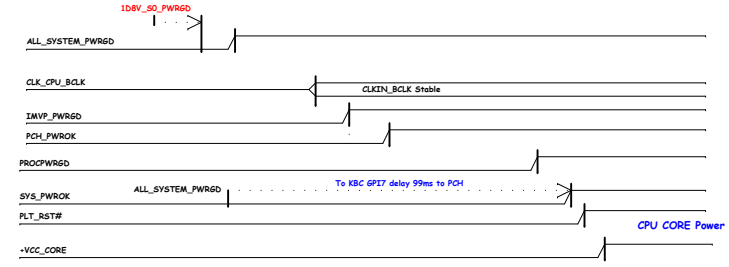
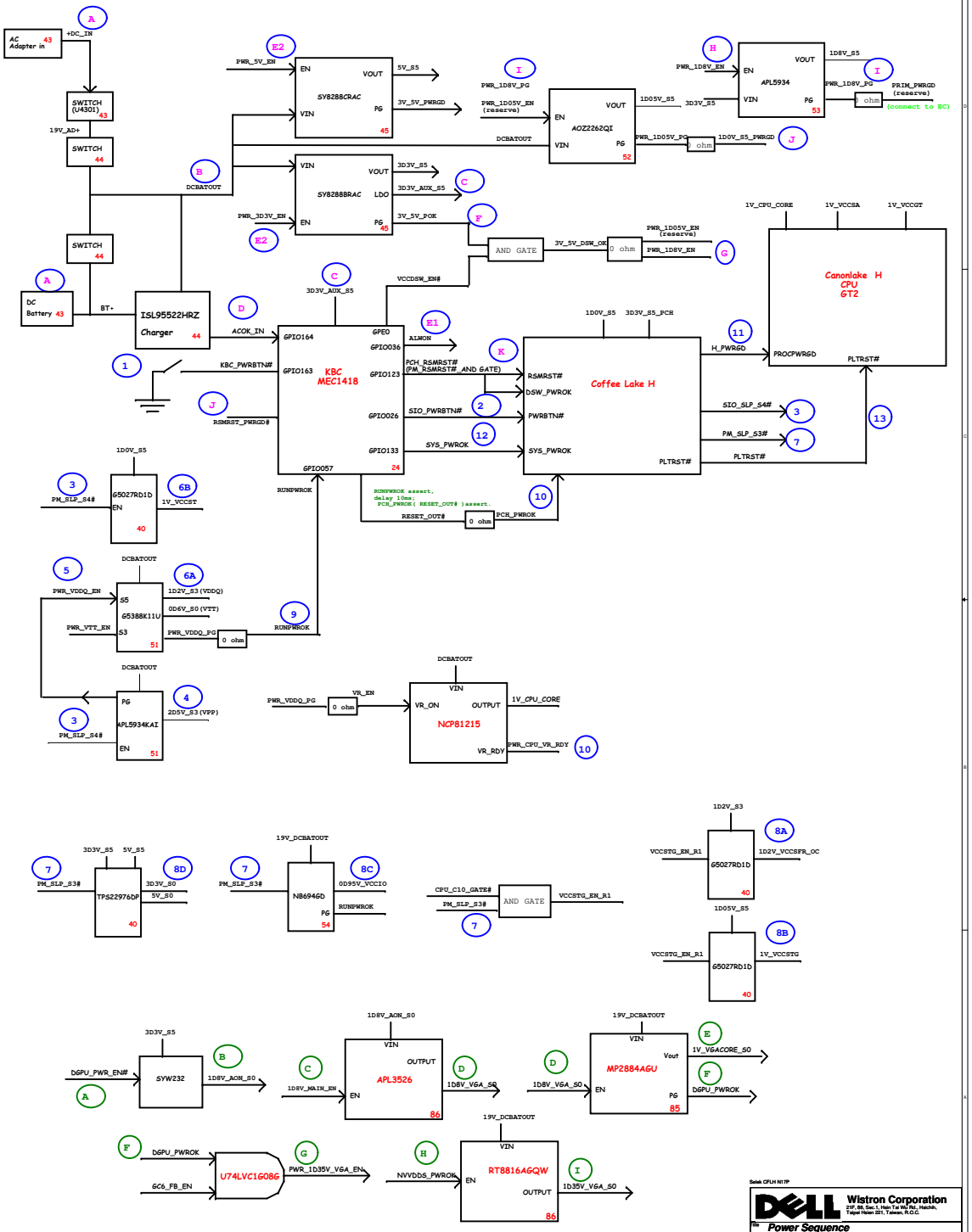
Intel-Power Up Sequence









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Title: Power Sequence

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HDMI

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N3

55 eDP_AUX_CPU_P
55 eDP_AUX_CPU_N

Soc AUD

15 AUD_AZACPU_SCLK
15 AUD_AZACPU_SDO
15 AUD_AZACPU_SDI_R

71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N0

71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N1

71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N2

71 DP1_DDI_TX_P3
71 DP1_DDI_TX_N3

71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P

PEG

76 GFX_PCIE_RX_P7
76 GFX_PCIE_RX_N7

76 GFX_PCIE_RX_P6
76 GFX_PCIE_RX_N6

76 GFX_PCIE_RX_P5
76 GFX_PCIE_RX_N5

76 GFX_PCIE_RX_P4
76 GFX_PCIE_RX_N4

76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3

76 GFX_PCIE_RX_P2
76 GFX_PCIE_RX_N2

76 GFX_PCIE_RX_P1
76 GFX_PCIE_RX_N1

76 GFX_PCIE_RX_P0
76 GFX_PCIE_RX_N0

76 GFX_PCIE_TX_CON_P7
76 GFX_PCIE_TX_CON_N7

76 GFX_PCIE_TX_CON_P6
76 GFX_PCIE_TX_CON_N6

76 GFX_PCIE_TX_CON_P5
76 GFX_PCIE_TX_CON_N5

76 GFX_PCIE_TX_CON_P4
76 GFX_PCIE_TX_CON_N4

76 GFX_PCIE_TX_CON_P3
76 GFX_PCIE_TX_CON_N3

76 GFX_PCIE_TX_CON_P2
76 GFX_PCIE_TX_CON_N2

76 GFX_PCIE_TX_CON_P1
76 GFX_PCIE_TX_CON_N1

76 GFX_PCIE_TX_CON_P0
76 GFX_PCIE_TX_CON_N0

DMI

18 DMI_RX_CPU_P0
18 DMI_RX_CPU_N0

18 DMI_RX_CPU_P1
18 DMI_RX_CPU_N1

18 DMI_RX_CPU_P2
18 DMI_RX_CPU_N2

18 DMI_RX_CPU_P3
18 DMI_RX_CPU_N3

18 DMI_TX_CPU_P0
18 DMI_TX_CPU_N0

18 DMI_TX_CPU_P1
18 DMI_TX_CPU_N1

18 DMI_TX_CPU_P2
18 DMI_TX_CPU_N2

18 DMI_TX_CPU_P3
18 DMI_TX_CPU_N3

DP to Type-C

CPU1D 4 OF 13

DP1_DDI_TX_P0 K36 DDI1_TXP_0 EDP_TXP_0 D29 eDP_TX_CPU_P0
DP1_DDI_TX_N0 K37 DDI1_TXN_0 EDP_TXN_0 E29 eDP_TX_CPU_N0
DP1_DDI_TX_P1 J35 DDI1_TXP_1 EDP_TXP_1 F28 eDP_TX_CPU_P1
DP1_DDI_TX_N1 J34 DDI1_TXN_1 EDP_TXN_1 E28 eDP_TX_CPU_N1
DP1_DDI_TX_P2 H37 DDI1_TXP_2 EDP_TXP_2 A26 eDP_TX_CPU_P2
DP1_DDI_TX_N2 H36 DDI1_TXN_2 EDP_TXN_2 B29 eDP_TX_CPU_N2
DP1_DDI_TX_P3 J37 DDI1_TXP_3 EDP_TXP_3 C26 eDP_TX_CPU_P3
DP1_DDI_TX_N3 J38 DDI1_TXN_3 EDP_TXN_3 B28 eDP_TX_CPU_N3

Port B

DP1_AUX_CPU_P D27 DDI1_AUXP EDP_AUXP C26 eDP_AUX_CPU_P
DP1_AUX_CPU_N E27 DDI1_AUXN EDP_AUXN B26 eDP_AUX_CPU_N

H34 DDI2_TXP_0
H33 DDI2_TXN_0
F37 DDI2_TXP_1 EDP_DISP_UTIL A33
G38 DDI2_TXN_1
F34 DDI2_TXP_2 EDP_RCOMP D37
F35 DDI2_TXN_2 DISP_RCOMP
E37 DDI2_TXP_3
E36 DDI2_TXN_3
F26 DDI2_AUXP
E26 DDI2_AUXN

Port C

C34 DDI3_TXP_0
D34 DDI3_TXN_0
B36 DDI3_TXP_1
B34 DDI3_TXN_1
F33 DDI3_TXP_2
E33 DDI3_TXN_2
C33 DDI3_TXP_3
B33 DDI3_TXN_3
A27 DDI3_AUXP
B27 DDI3_AUXN

Port D

G27 AUD_AZACPU_SCLK
G26 AUD_AZACPU_SDO
G29 AUD_AZACPU_SDI

PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO

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Do Not Stuff

0D95V_VCCIO

R301 2 1 24D9R2F-L-GP

AUD_AZACPU_SDI_R

R302 20R2J-3-GP

Do Not Stuff

Layout Note:
Trace Width:12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

Layout Note:
Trace Width:12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)

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E25 PEG_RXP_0 PEG_TXP_0 B25
D25 PEG_RXN_0 PEG_TXN_0 A25
E24 PEG_RXP_1 PEG_TXP_1 B24
F24 PEG_RXN_1 PEG_TXN_1 C24
E23 PEG_RXP_2 PEG_TXP_2 B23
D23 PEG_RXN_2 PEG_TXN_2 A23
E22 PEG_RXP_3 PEG_TXP_3 B22
F22 PEG_RXN_3 PEG_TXN_3 C22
E21 PEG_RXP_4 PEG_TXP_4 B21
D21 PEG_RXN_4 PEG_TXN_4 A21
E20 PEG_RXP_5 PEG_TXP_5 B20
F20 PEG_RXN_5 PEG_TXN_5 C20
E19 PEG_RXP_6 PEG_TXP_6 B19
D19 PEG_RXN_6 PEG_TXN_6 A19
E18 PEG_RXP_7 PEG_TXP_7 B18
F18 PEG_RXN_7 PEG_TXN_7 C18

GFX_PCIE_RX_P7 D17 PEG_RXP_8 PEG_TXP_8 A17 GFX_PCIE_TX_P7 C323 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P7
GFX_PCIE_RX_N7 E17 PEG_RXN_8 PEG_TXN_8 B17 GFX_PCIE_TX_N7 C324 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N7
GFX_PCIE_RX_P6 F16 PEG_RXP_9 PEG_TXP_9 C16 GFX_PCIE_TX_P6 C321 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P6
GFX_PCIE_RX_N6 E16 PEG_RXN_9 PEG_TXN_9 B16 GFX_PCIE_TX_N6 C322 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N6
GFX_PCIE_RX_P5 D15 PEG_RXP_10 PEG_TXP_10 A15 GFX_PCIE_TX_P5 C318 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P5
GFX_PCIE_RX_N5 E15 PEG_RXN_10 PEG_TXN_10 B15 GFX_PCIE_TX_N5 C320 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N5
GFX_PCIE_RX_P4 F14 PEG_RXP_11 PEG_TXP_11 C14 GFX_PCIE_TX_P4 C307 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P4
GFX_PCIE_RX_N4 E14 PEG_RXN_11 PEG_TXN_11 B14 GFX_PCIE_TX_N4 C316 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N4
GFX_PCIE_RX_P3 D13 PEG_RXP_12 PEG_TXP_12 A13 GFX_PCIE_TX_P3 C314 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P3
GFX_PCIE_RX_N3 E13 PEG_RXN_12 PEG_TXN_12 B13 GFX_PCIE_TX_N3 C304 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N3
GFX_PCIE_RX_P2 F12 PEG_RXP_13 PEG_TXP_13 C12 GFX_PCIE_TX_P2 C303 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P2
GFX_PCIE_RX_N2 E12 PEG_RXN_13 PEG_TXN_13 B12 GFX_PCIE_TX_N2 C313 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P1 D11 PEG_RXP_14 PEG_TXP_14 A11 GFX_PCIE_TX_P1 C312 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P1
GFX_PCIE_RX_N1 E11 PEG_RXN_14 PEG_TXN_14 B11 GFX_PCIE_TX_N1 C302 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P0 F10 PEG_RXP_15 PEG_TXP_15 C10 GFX_PCIE_TX_P0 C310 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P0
GFX_PCIE_RX_N0 E10 PEG_RXN_15 PEG_TXN_15 B10 GFX_PCIE_TX_N0 C311 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N0

0D95V_VCCIO

R303 1 2 24D9R2F-L-GP

PEG_RCOMPO G2 PEG_RCOMP

DMI_RX_CPU_P0 D8 DMI_RXP_0 DMI_TXP_0 B8 DMI_TX_CPU_P0
DMI_RX_CPU_N0 E8 DMI_RXN_0 DMI_TXN_0 A8 DMI_TX_CPU_N0
DMI_RX_CPU_P1 E6 DMI_RXP_1 DMI_TXP_1 C6 DMI_TX_CPU_P1
DMI_RX_CPU_N1 F6 DMI_RXN_1 DMI_TXN_1 B6 DMI_TX_CPU_N1
DMI_RX_CPU_P2 D5 DMI_RXP_2 DMI_TXP_2 B5 DMI_TX_CPU_P2
DMI_RX_CPU_N2 E5 DMI_RXN_2 DMI_TXN_2 A5 DMI_TX_CPU_N2
DMI_RX_CPU_P3 J8 DMI_RXP_3 DMI_TXP_3 D4 DMI_TX_CPU_P3
DMI_RX_CPU_N3 J9 DMI_RXN_3 DMI_TXN_3 B4 DMI_TX_CPU_N3

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Do Not Stuff

Do Not Stuff

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Title: CPU (PCIE/DMI/FDI)

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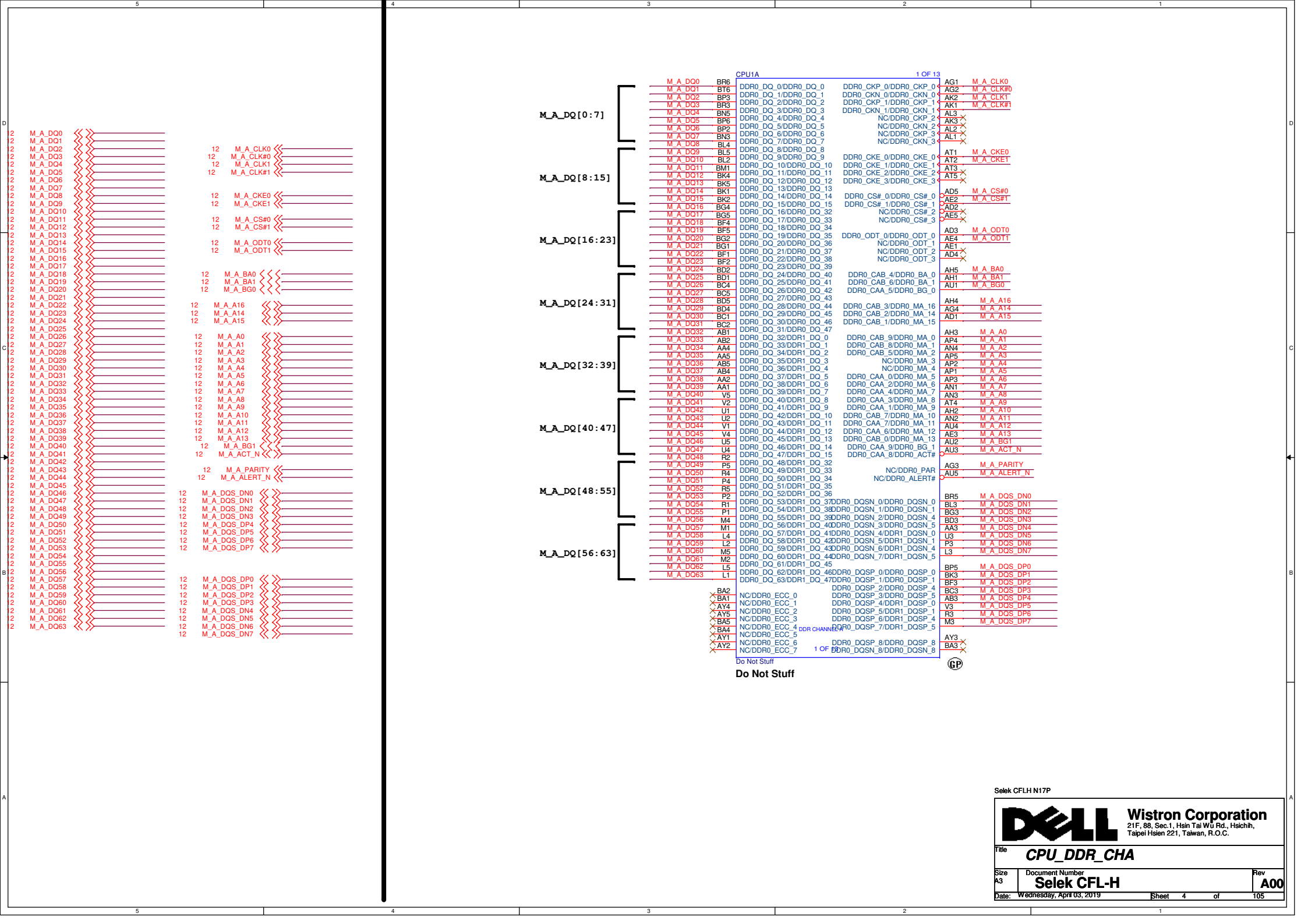

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Title: CPU_DDR_CHA

Size: A3 | Document Number: Selek CFL-H | Rev: A00

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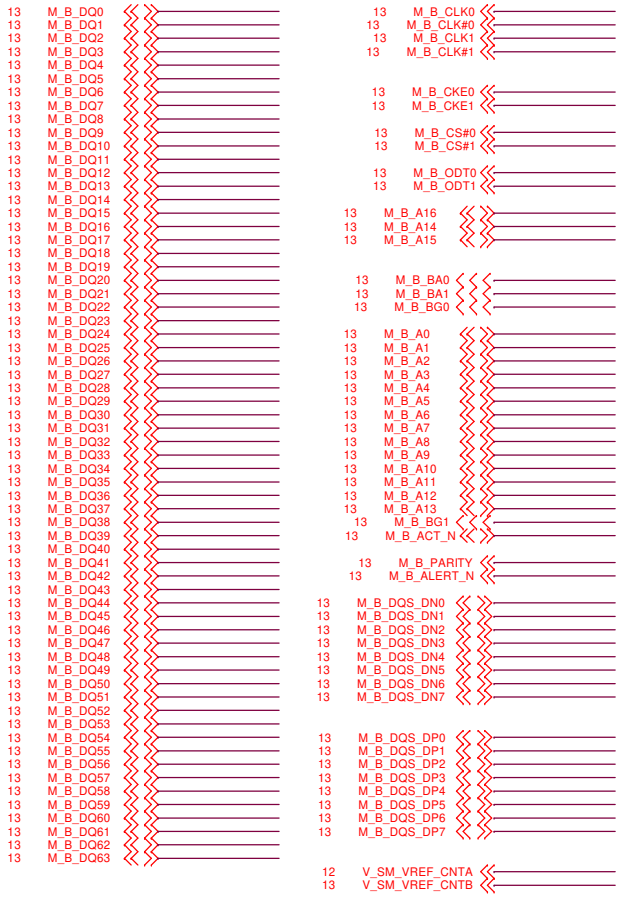
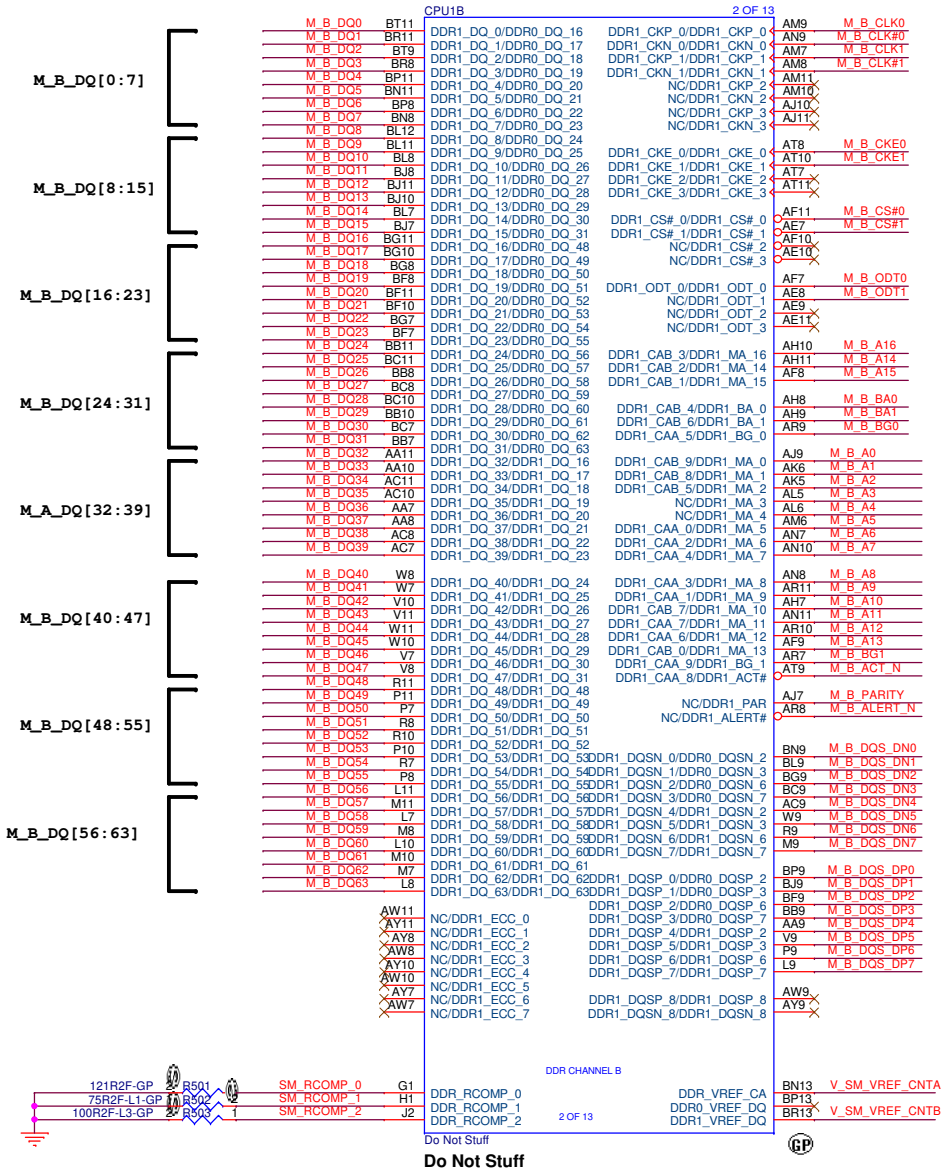
SSID = CPU





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Title	CPU_DDR_CHB	
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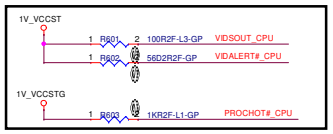
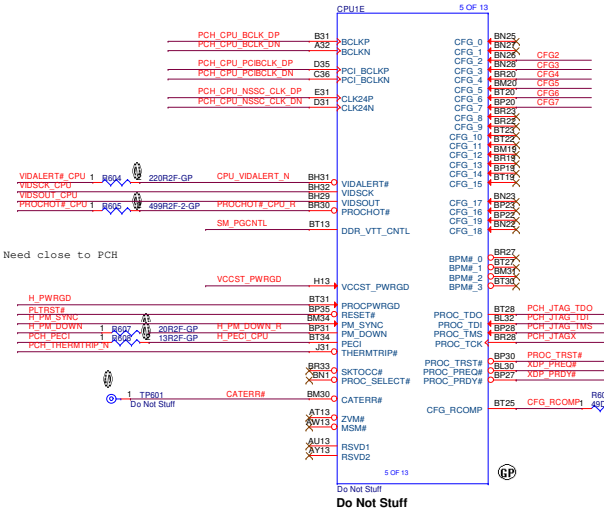
AROUND_CPU





R608 Need close to PCH

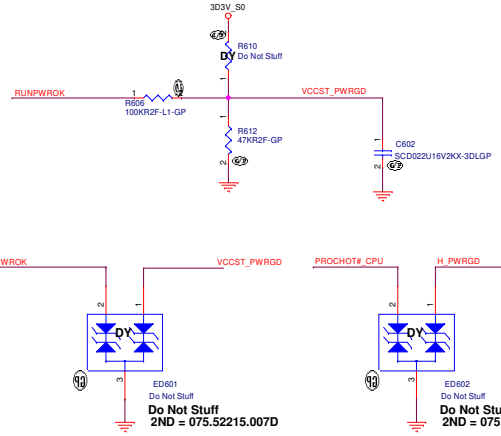
Table 13-14. SVID Bus Routing Guidelines

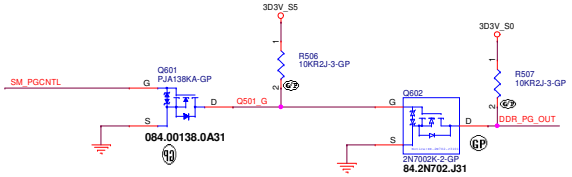
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	WS1 [inches]	WS2 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

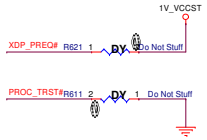
Note: For additional information regarding SVID and power management refer to *"Power Architecture Guide"* .

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

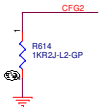




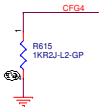


GPD11 pull high by Intel PDG1.3 request

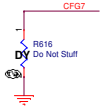
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



eDP Enable	
CFG4	1:Disable 0:Enable



PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.



Physical_Debug_Enabled (DFX privacy)	
CFG4	1:Disable 0:Enable (Set DXF enables bit in debug)

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	$V_{CC_{IO}}$	16-60 Ω
PREQ# |	Pull Up	$V_{CC_{ST}}$	3 kΩ
PROC_TDI	Pull Up	$V_{CC_{STG}}$[1]	3 kΩ
PROC_TMS	Pull Up	$V_{CC_{SGT}}$[1]	3 kΩ
CFG[19:0]	Pull Up	$V_{CC_{IO}}$	3 kΩ

Note:
1. For SKL-S it should be $V_{CC_{ST}}$

1208

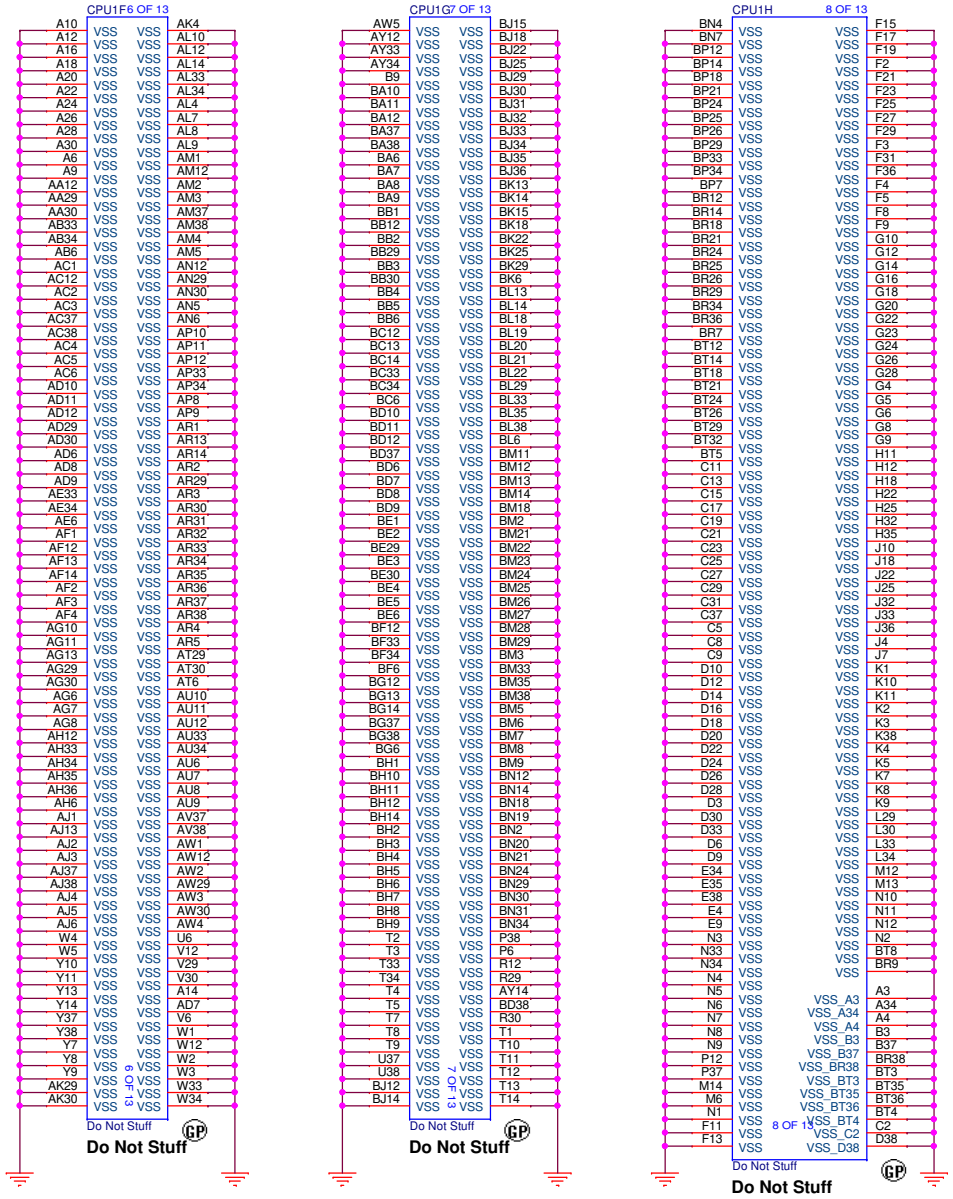
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_CFG_CFG STRAP

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 6 of 105



Selek CFLH N17P

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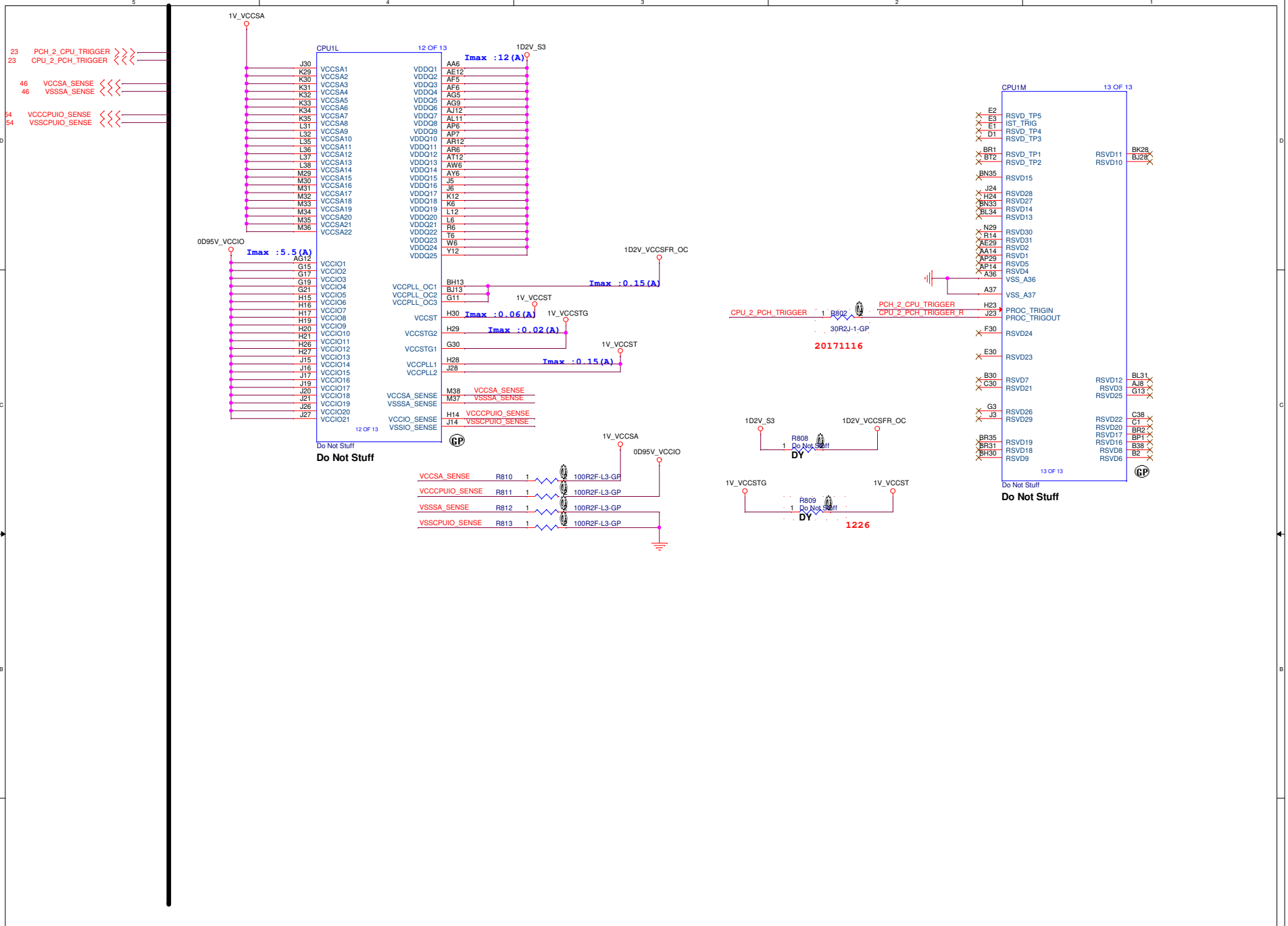
Title	*CPU_GND*	
Size A3	Document Number **Selek CFL-H**	Rev **A00**
Date: Wednesday, April 03, 2019	Sheet 7 of 105	



Selek CFLH N17P

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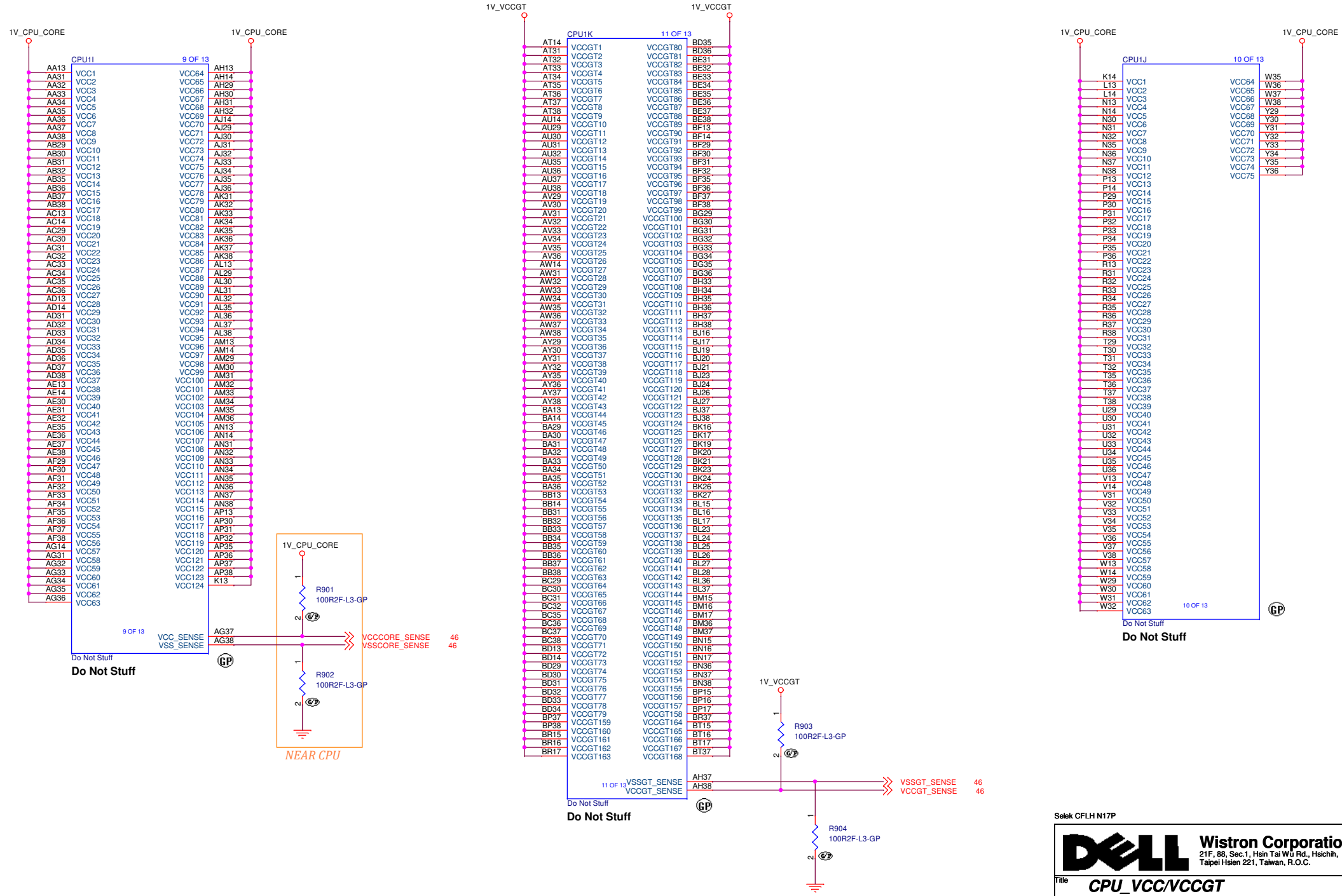
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_POWER(VCCSA/VCCIO/VDD)***

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 8 of 105

SSID = CPU



Selek CFLH N17P

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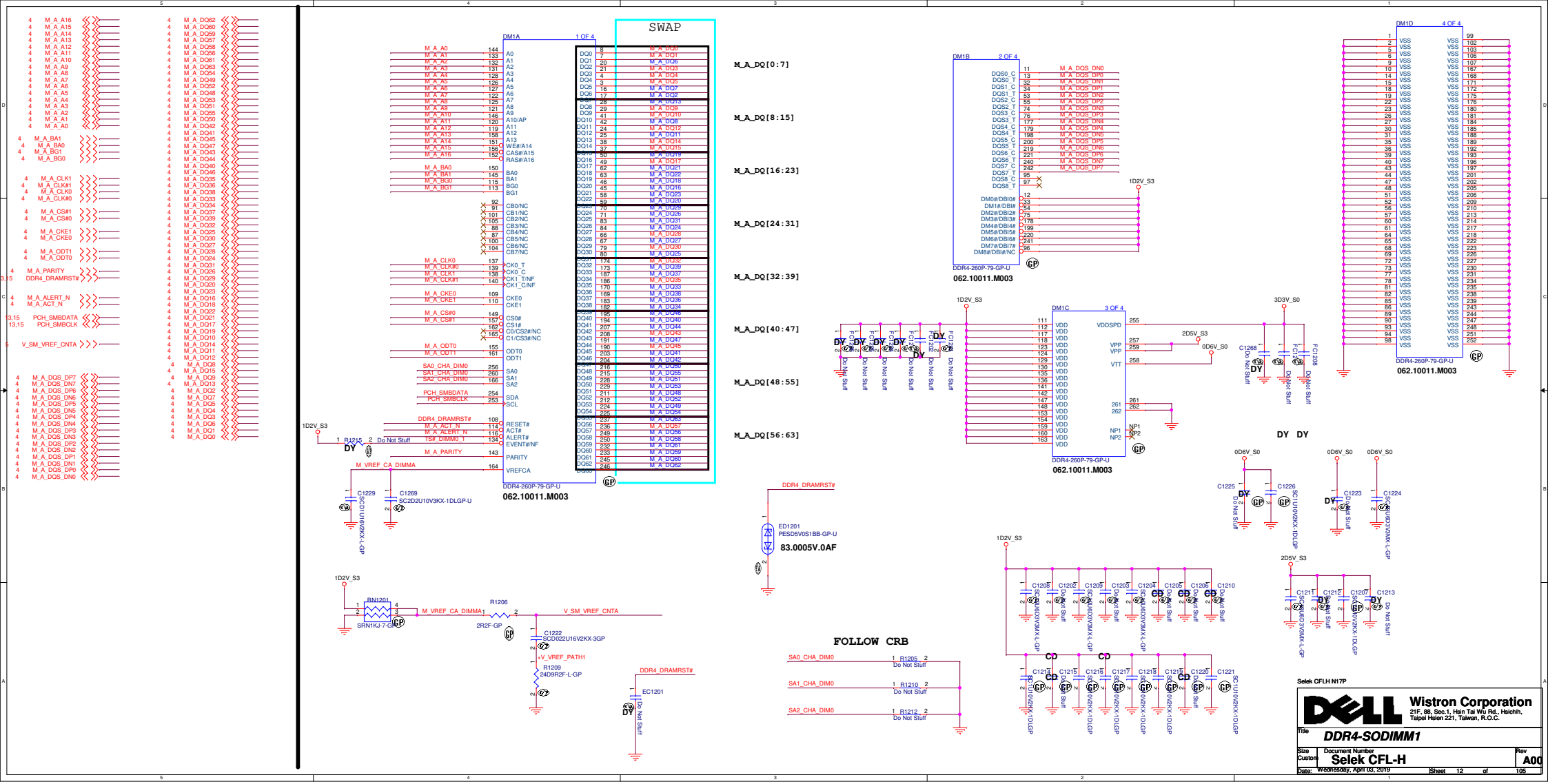
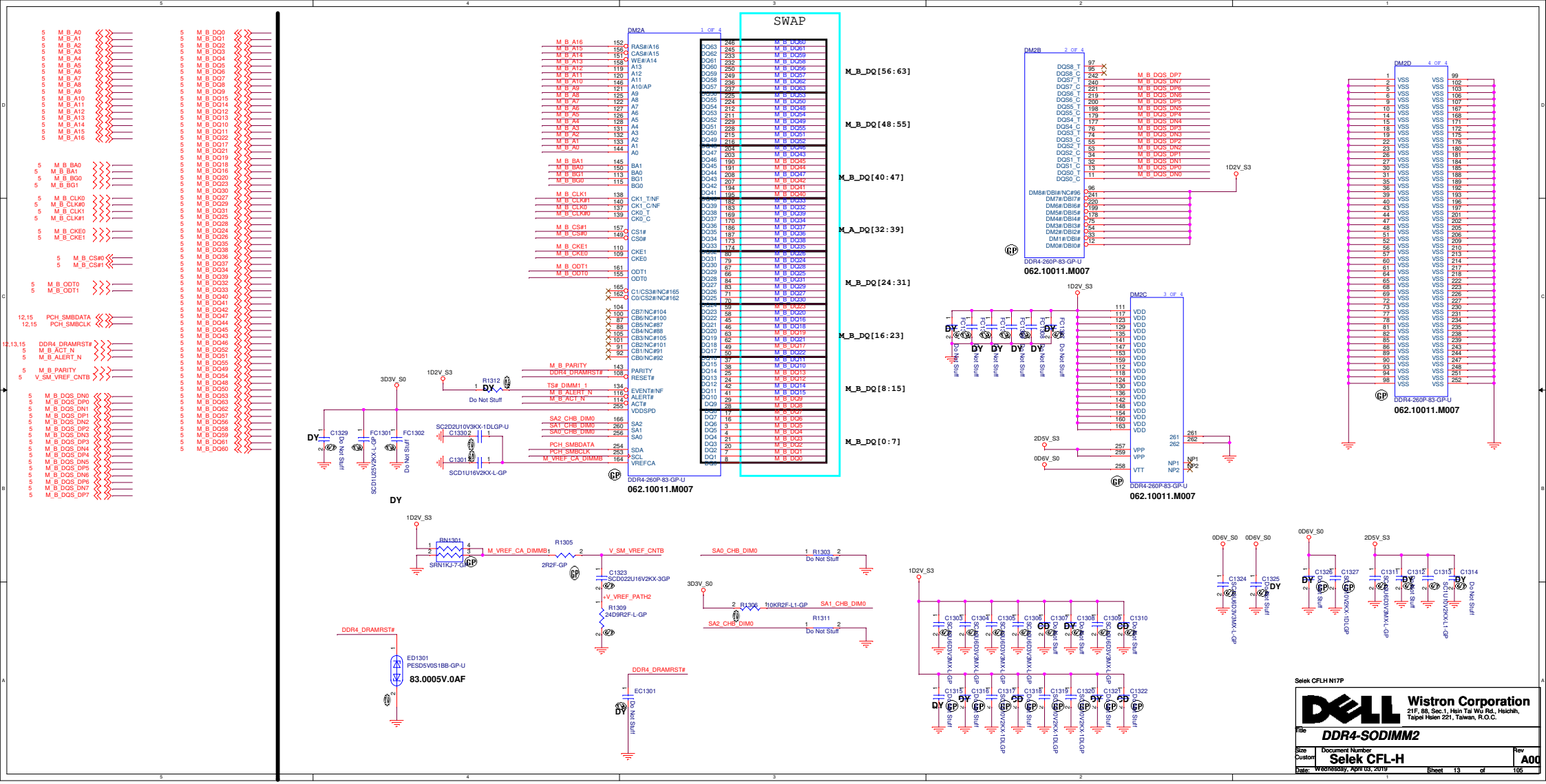
Title	CPU_VCC/VCCGT	
Size A3	Document Number Selek CFL-H	Rev A00
Date: Wednesday, April 03, 2019	Sheet 9 of 105	


SWAP
DM1A
1 OF 4
DM1B
2 OF 4
DM1C
3 OF 4
DM1D
4 OF 4
M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]
DDR4-260P-79-GP-U
062.10011.M003
FOLLOW CRB
DY DY
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR4-SODIMM1
Selek CFL-H
Wednesday, April 03, 2019


SWAP
DM2A
M_B_DQ[56:63]
M_B_DQ[48:55]
M_B_DQ[40:47]
M_A_DQ[32:39]
M_B_DQ[24:31]
M_B_DQ[16:23]
M_B_DQ[8:15]
M_B_DQ[0:7]
DDR4-260P-83-GP-U
062.10011.M007
DM2B
DM2C
DM2D
1D2V_S3
2D5V_S3
0D6V_S0
3D3V_S0
DY
Do Not Stuff
ED1301
PESD5V0S1BB-GP-U
83.0005V.0AF
EC1301
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR4-SODIMM2
Selek CFL-H
A00
Wednesday, April 03, 2019
13
105

SPI ROM

25,91 SPI_CLK_CPU
15,21,25,91 SPI_SO_CPU
15,21,25,91 SPI_SI_CPU
15,21,25 SPI_WP_CPU
15,21,25 SPI_HOLD_CPU
25 SPI_CS_ROM_N0
25 SPI_CS_ROM_N1

TPM

91 SPI_CS_CPU_N2
91 TPM_SPI_IRQ#

26,31,61,63,79,91 PLT_RST#
6 H_PWRGD
24 SIO_PWRBTN#
61 SUS_CLK
24 GC6_THM_DIS#
3 AUD_AZACPU_SDO
3 AUD_AZACPU_SDI
3 AUD_AZACPU_SCLK
6 PCH_JTAG_TMS
6 PCH_JTAG_TDO
6 PCH_JTAG_TDI
12,13 DDR4_DRAMRST#
21 CPU_SMB_ALERT#_P1
27 HDA_BITCLK_CODEC
27 HDA_SDI0_CPU
27 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
24 ME_FWP
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
24,31 LAN_WAKE#
21 GPP_H15
61 CNV_RF_RESET#
61 CLKREQ_CNV#

PCH Strap

21 CPU_SMB_ALERT#
21 CPU_SMB_ALERT#_P0

SIO

15,21,25 SPI_WP_CPU
15,21,25 SPI_HOLD_CPU
15,21,25,91 SPI_SI_CPU
15,21,25,91 SPI_SO_CPU

40,91 PM_SLP_S0#
27,40,54,57 PM_SLP_S3#
40,44,51,92 PM_SLP_S4#
24 PCH_WAKE_N
24,26,79 CPU_SMB_SCL_P1
24,26,79 CPU_SMB_SDA_P1
24,76,86 DGPU_PWROK
24 SYS_PWROK
24,65 TP_WAKE_KBC#
21,27 SPKR
24,26 RESET_OUT#
12,13 PCH_SMBDATA
12,13 PCH_SMBCLK
6 PCH_JTAGX
25,40,45 3V_5V_POK
24 PCH_RSMRST#
43,44 ACOK_IN_M
64 PM_RSMRST#

Azalia I/F EMI

Close to PCH

HDA_SDOUT_CODEC
HDA_SYNC_CODEC
EC1501 22P/50V/NPO/0402
EC1502 22P/50V/NPO/0402

SPI ROM

SIO_PME_N_R
SPI_SI_CPU
SPI_SO_CPU
SPI_CS_ROM_N0
SPI_CLK_CPU
SPI_CS_ROM_N1
SPI_WP_CPU
SPI_HOLD_CPU
SPI_CS_CPU_N2
TPM_SPI_IRQ#

TPM

PCH1A
GPP_A11/PME#/SD_VDD2_PWR_EN#
RSVD2
RSVD1
VSS
TP
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
GPP_D1/SPI1_CLK/SBK1_BK1
GPP_D2/SPI1_CS#/SBK0_BK0
GPP_D3/SPI1_MOSI/SBK3_BK3
GPP_D4/SPI1_MISO/SBK2_BK2
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
CANON-LAKE-GP
(071.CANNO.0001)

PCH_PLTRST#
R1503 0 Do Not Stuff
PLT_RST#
R1592 0 Do Not Stuff
C1515 Do Not Stuff
GPP_K16/GSXDCLK
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
Y45
Y46
W45
AA45
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
AM45
BF38
BC37
TOUCHPAD_INT1#
GCE_THM_DIS#
R1590 0 Do Not Stuff
TP_WAKE_KBC#
GPP_H15
GPP_H12
PCH_INTRUDER_N
R1507 1
1MR2J-1-GP
RTC_AUX_S5
1214
1DV_S3
R1580 10R2F-GP
SM_DRAMRST#
R1581 0 Do Not Stuff
DDR4_DRAMRST#

EMI 1229

PCH_PLTRST#
ED1501 PLT(15)-05S-R7G-GP
75.05125.07D
2nd = 075.00363.0A7D
3rd = 075.02215.007D

ME_FWP
R1569 1
1KR2J-1-GP
HDA_SDOUT_CPU

Close to PCH

HDA_BITCLK_CODEC
R1559 1
33R2J-2-GP
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SDOUT_CPU
HDA_SYNC_CPU
HDA_RST_N_CPU
TP1511 Do Not Stuff

Intel® Display Audio Interface To CPU

AUD_AZACPU_SDO
R1501 1
33R2J-1-GP
AUD_AZACPU_SDO_R
AUD_AZACPU_SDI_R
AUD_AZACPU_SCLK_R
R1522 1
33R2J-1-GP

PCH1D
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_RXD
HDA_SDI/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S1_SCLK
HDA_SDI/I2S1_RXD
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
GPP_D6/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D8/I2S2_TXD/MODEM_CLKREQ
GPP_D9/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_DATA1/SNDW3_DATA
GPP_D18/DMIC_DATA0/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A6/CLKRUN#
GPD11/LANPHYPC
GPD8/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD7/SLP_S0#
SUSCLK
GPD0/SUSCLK
GPD3/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
CANON-LAKE-GP
(071.CANNO.000U)

RTC_RST#
SRTC_RST#
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SMLOALERT#
GPP_C6/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C8/SML1CLK
GPP_C7/SML1DATA

RESET_OUT#
R1529 2 Do Not Stuff
PM_PCH_PWROK
PM_RSMRST#
R1531 2 Do Not Stuff
DSW_PWROK
R1532 100KR2J-1-GP

SYS_PWROK
R1533 1 Do Not Stuff
PCH_WAKE_N
SLP_S0#_R
R1535 1 Do Not Stuff
SLP_S0#
PM_SLP_S0#
R1536 1 Do Not Stuff
PM_SLP_S3#
R1537 1 Do Not Stuff
PM_SLP_S4#
R1538 1 Do Not Stuff
SUSCLK
R1579 2 Do Not Stuff
SUS_CLK
PCH_BATLOW#
R1534 1 Do Not Stuff
SUS_WARN#
R1556 1 Do Not Stuff
LAN_WAKE#
AC_PRESENT
R1539 1 Do Not Stuff
H_PWRGD
R1548 1 Do Not Stuff
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
P1513 Do Not Stuff
P1512 Do Not Stuff
P1507 Do Not Stuff
P1509 Do Not Stuff
P1508 Do Not Stuff
LAN_WAKE#
ME_SUS_PWR_ACK
SUS_CLK

CPU_SMB_SCL_P1
CPU_SMB_SDA_P1
C1505 Do Not Stuff
C1508 Do Not Stuff

SMBUS

3DV_S0
RN1503 10KR2J-8-GP
CPU_SMB_SDA
CPU_SMB_SCL
Q1502 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.06301.007C
PCH_SMBDATA
PCH_SMBCLK

PCH_RSMRST#
3V_5V_POK
U1501 U74LVC1G08G-AL5-R-GP-U
73.01G08.EHG
2nd = 73.7SZ08.DAH
VCC=2.3V~3.6V
VIL=<Min=2V
VIL=>Max=0.8V
3DV_AUX_S5
C1516 Do Not Stuff
PM_RSMRST#

RTC_AUX_S5
1214
CRB pull 30.1k , but PDG use 20k
RN1507 SRN20KJ-1-GP
SRTC_RST#
C1518
Q1501
C1517
SCLVLVSXX-1CLKP
Layout: Place at the open door area

3DV_AUX_S5
R1587 100KR2J-1-GP
PM_RSMRST#_M
Q1502 2N7002KDW-1-GP
PM_RSMRST#_R
R1583 0 Do Not Stuff
PM_RSMRST#
D1501 RB521S30-GP
B1.R2003.A8M
2ND = 083.S2030.008F
ACOK_IN_M
AC_PRESENT
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.06301.007C

Reserve by NON DS3 function 20150413

3DV_S5_PCH

GPP_H12
R1596 1 Do Not Stuff
SIO_PME_N_R
R1504 1 Do Not Stuff
CLKRUN#/GPP_A6
R1511 1 Do Not Stuff
CPU_SMB_SCL_P1
CPU_SMB_SDA_P1
RN1506 SRN10KJ-4-GP

PM_SLP_S0#
R1512 100KR2F-L1-GP
PM_SLP_S3#
R1513 100KR2F-L1-GP
PM_SLP_S4#
R1514 100KR2F-L1-GP
SIO_SLP_S0#
R1515 100KR2F-L1-GP

1DV_S5

SUS_WARN#
RN1501 10KR2J-4-GP
RTC_PWR_ACK

3DV_S5_PCH

PCH_WAKE_N
R1537 1 1KR2J-1-GP
PCH_BATLOW#
RN1502 SRN10KJ-4-GP
AC_PRESENT

3DV_S5_PCH

LAN_WAKE#
R1534 1 10KR2J-3-GP
XDP_DBRESET#
R1539 1 10KR2J-3-GP

3DV_S0

TOUCHPAD_INT1#
R1540 1 Do Not Stuff

1V_VCCST

PCH_JTAG_TDO
R1545 1 100R2J-2-GP
PCH_JTAG_TDI
R1546 1 51R2F-2-GP
PCH_JTAG_TMS
R1547 1 51R2F-2-GP

3DV_S5_PCH

CPU_SMB_SCL_P0
R1550 1 1KR2J-1-GP
CPU_SMB_SDA_P0
R1551 1 1KR2J-1-GP
PCH_JTAGX
R1544 1 51R2F-2-GP
SYS_PWROK
R1582 1 10KR2J-3-GP
PCH_JTAG_TCK
R1535 1 Do Not Stuff
PM_PCH_PWROK
R1552 1 10KR2J-3-GP

GPU_ID2
RN1504 SRN10KJ-4-GP
GPU_ID1
Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(Audio/SMBUS/JTAG/GPIO)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 15 of 105

TO CPU CLOCK

6 PCH_CPU_BCLK_DP
6 PCH_CPU_BCLK_DN

6 PCH_CPU_PCIBCLK_DP
6 PCH_CPU_PCIBCLK_DN

6 PCH_CPU_NSSC_CLK_DP
6 PCH_CPU_NSSC_CLK_DN

31 LAN_CLK_CPU_N
31 LAN_CLK_CPU_P
31 LAN_CLKREQ_CPU_N

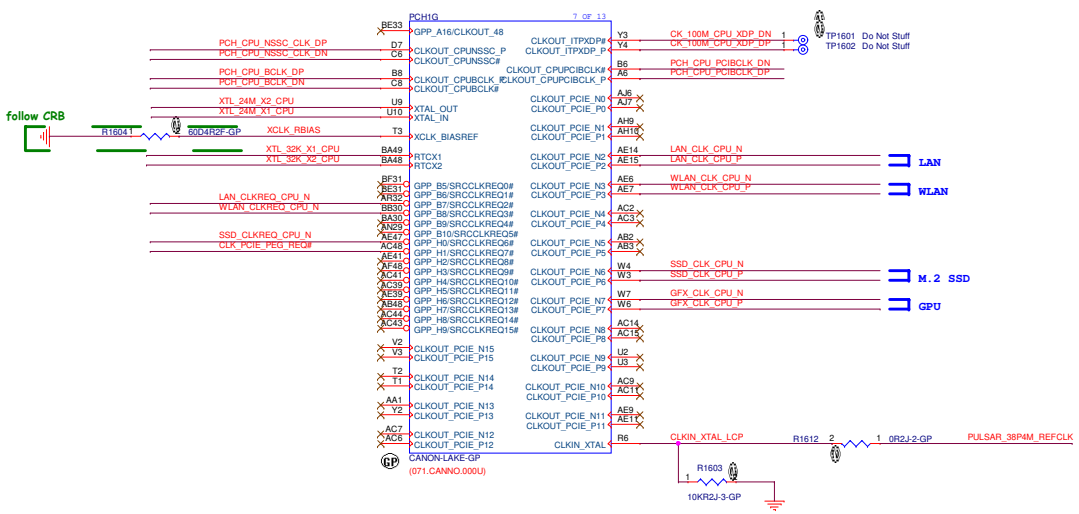
61 WLAN_CLK_CPU_N
61 WLAN_CLK_CPU_P
61 WLAN_CLKREQ_CPU_N

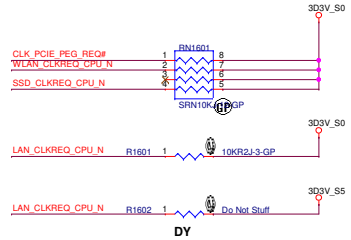
63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N

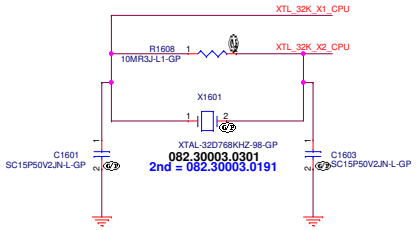
76 GFX_CLK_CPU_N
76 GFX_CLK_CPU_P
76 CLK_PCIE_PEG_REQ#

61 PULSAR_38P4M_REFCLK

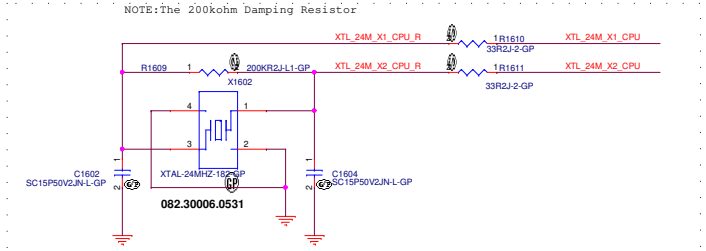
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







follow PDG
Frequecy: 32.768KHz
ESR: 50kohm
CL: 12pF



follow PDG
Frequecy: 24MHz
Series Resistance :< 30ohm MAX
CL: 12pF

24 MHz Crystal Specifications (Sheet 1 of 2)

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	

Parameter	Values	Units	Max/Min Range
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLK)
Size: Custom | Document Number: Selek CFL-H | Rev: A00
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M.2 SSD 1

63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1

63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2

63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3
63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P

HDD

60 HDD_SATA_RX_N
60 HDD_SATA_RX_P
60 HDD_SATA_TX_N
60 HDD_SATA_TX_P

WLAN

61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P
61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P

LAN

31 LAN_PCIE_TX_N
31 LAN_PCIE_TX_P
31 LAN_PCIE_RX_N
31 LAN_PCIE_RX_P

eDP

55 L_BKLT_CTRL
24 L_BKLT_EN
55 EDP_VDD_EN
64 PCH_SATA_LED#

6 PCH_THERMTRIP_N
6 H_PM_SYNC
6 PLTRST#
6 H_PM_DOWN

6 PCH_PECI

63 M2_SSD_PEDET

CNVI

61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLKN
61 CNV_WR_CLKP
61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLKN
61 CNV_WT_CLKP

61 CNV_BRI_RSP
21,61 CNV_RGI_DT
61 CNV_BRI_DT_CON
61 CNV_RGI_RSP
21 CNV_BRI_DT_PCH

21 GPP_J9

55 DBC_PANEL_EN

65 KB_BL_DET

40 CPU_C10_GATE#

PCH1C 3 OF 13

AR2 CL_CLK
AT5 CL_DATA
AU4 CL_RST#

P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11

L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3
N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7

AR42 GPP_F10/SATA_SCLOCK
AU47 GPP_F11/SATA_SLOAD
AU46 GPP_F13/SATA_SDATAOUT0
GPP_F12/SATA_SDATAOUT1

Lane 15: PCIE9_RXN G36, PCIE9_RXP F36, PCIE9_TXN C34, PCIE9_TXP D34
Lane 16: PCIE10_RXN K37, PCIE10_RXP J37, PCIE10_TXN C35, PCIE10_TXP B35
Lane 21: PCIE15_RXN/SATA2_RXN F44, PCIE15_RXP/SATA2_RXP E45, PCIE_15_SATA_2_TXN B40, PCIE15_TXP/SATA2_TXP C40
Lane 22: PCIE16_RXN/SATA3_RXN L41, PCIE16_RXP/SATA3_RXP M40, PCIE16_TXN/SATA3_TXN B41, PCIE16_TXP/SATA3_TXP C41
Lane 17: PCIE17_RXN/SATA4_RXN K43, PCIE17_RXP/SATA4_RXP K42, PCIE17_TXN/SATA4_TXN A42, PCIE17_TXP/SATA4_TXP B42
Lane 23: PCIE18_RXN/SATA5_RXN P41, PCIE18_RXP/SATA5_RXP M40, PCIE18_TXN/SATA5_TXN C42, PCIE18_TXP/SATA5_TXP D42
Lane 24: PCIE11_TXP/SATA0A_TXP C36, PCIE11_TXN/SATA0A_TXN B36, PCIE11_RXP/SATA0A_RXP F39, PCIE11_RXN/SATA0A_RXN G38
Lane 20: PCIE14_TXN/SATA1B_TXN C39, PCIE14_TXP/SATA1B_TXP D39, PCIE14_RXN/SATA1B_RXN D46, PCIE14_RXP/SATA1B_RXP C47
Lane 18: PCIE12_TXP/SATA1A_TXP E37, PCIE12_TXN/SATA1A_TXN D38, PCIE12_RXP/SATA_1A_RXP J41, PCIE12_RXN/SATA1A_RXN H42
Lane 26: PCIE20_TXN/SATA7_TXN B44, PCIE20_TXP/SATA7_TXP A44, PCIE20_RXN/SATA7_RXN R37, PCIE20_RXP/SATA7_RXP R35
Lane 25: PCIE19_TXN/SATA6_TXN C43, PCIE19_TXP/SATA6_TXP D43, PCIE19_RXN/SATA6_RXN N42, PCIE19_RXP/SATA6_RXP M44

GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E3/SATAXPCIE3/SATAGP_3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7

GPP_E8/SATA_LED#
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN

THRMTRIP#
PECI
PM_SYNC
PLTRST_CPU#
PM_DOWN

CANON-LAKE-GP
(071.CANNO.000U)

M.2 SSD 1 — SSD_PCIE_TX_P3, SSD_PCIE_TX_N3, SSD_PCIE_RX_P3, SSD_PCIE_RX_N3
LAN — LAN_PCIE_TX_N, LAN_PCIE_TX_P, LAN_PCIE_RX_N, LAN_PCIE_RX_P
HDD — HDD_SATA_TX_N, HDD_SATA_TX_P, HDD_SATA_RX_N, HDD_SATA_RX_P
M.2 SSD 1 — SSD_SATA_TX_P, SSD_SATA_TX_N, SSD_SATA_RX_P, SSD_SATA_RX_N

M.2 SSD 1 — SSD_PCIE_RX_N1, SSD_PCIE_RX_P1, SSD_PCIE_TX_N1, SSD_PCIE_TX_P1
M.2 SSD 1 — SSD_PCIE_RX_N2, SSD_PCIE_RX_P2, SSD_PCIE_TX_N2, SSD_PCIE_TX_P2
WLAN — WLAN_PCIE_RX_N, WLAN_PCIE_RX_P, WLAN_PCIE_TX_N, WLAN_PCIE_TX_P

PCH_SATA_LED#
M2_SSD_PEDET

3D3V_S0 — R1716 — PCH_SATA_LED# — 10KR2J-3-GP

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

eDP:
BIA_PWM_PCH — R1721 — Do Not Stuff — L_BKLT_CTRL
L_BKLT_EN_EC — R1720 — Do Not Stuff — L_BKLT_EN
ENVDD_PCH — R1719 — Do Not Stuff — EDP_VDD_EN
PCH_THERMTRIP_R_N — R1708 — 620R2F-GP — PCH_THERMTRIP_N
PCH_PECI
H_PM_SYNC_0 — R1710 — 30R2J-1-GP — H_PM_SYNC
PLTRST#
H_PM_DOWN

1V_VCCST
Close to PCH
PCH_THERMTRIP_N — R1702 — 1KR2J-3-GP

3D3V_S0 — R1705 — DY — Do Not Stuff — LCD_DBC
1D8V_S5 — R1703 — 20KR2J-L2-GP — CNV_BRI_RSP
R1704 — 20KR2J-L2-GP — CNV_RGI_RSP

TP1702 — Do Not Stuff — ELC_EN_PCH
DBC_PANEL_EN — R1727 — Do Not Stuff — KB_BL_DET
PROJECT_ID1
PROJECT_ID2
LCD_DBC
KB_BL_DET
TPM_ID

CPU_C10_GATE#

CNVI:
CNV_BRI_DT_PCH — R1730 — Do Not Stuff
CNV_BRI_DT_CON — R1701 — 33R2J-2-GP — CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_DT — R1706 — 33R2J-2-GP — CNV_RGI_DT_R
CNV_RGI_RSP
GPP_J9

PCH1M 13 OF 13

AW13 GPP_G0/SD_CMD
BF5 GPP_G1/SD_D0
BF9 GPP_G2/SD_D1
BC8 GPP_G3/SD_D2
BE5 GPP_G4/SD_D3
BD8 GPP_G5/SD_CD#
AV13 GPP_G6/SD_CLK
GPP_G7/SD_WP

AP3 GPP_I11/M2_SKT2_CFG0
AN2 GPP_I12/M2_SKT2_CFG1
AN4 GPP_I13/M2_SKT2_CFG2
AM7 GPP_I14/M2_SKT2_CFG3

AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_VCCIO_PWR_GATE#
AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10
AW3 GPP_J_2
AT10 GPP_J_3
AV4 GPP_J_4 CNV_BRI_DT_UART0_RTS#
AY2 GPP_J5/CNV_BRI_RSP/UART0_RXD
BA4 GPP_J6/CNV_RGI_DT/UART0_TXD
AV3 GPP_J7/CNV_RGI_RSP/UART0_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
AU9 GPP_J9/CNV_MFUART2_TXD

CNV_WR_CLKN BD4, CNV_WR_CLKP BE3
CNV_WR_DN0 BB3, CNV_WR_DP0 BB4
CNV_WR_DN1 BA3, CNV_WR_DP1 BA2
CNV_WT_CLKN BC5, CNV_WT_CLKP BB6
CNV_WT_DN0 BB6, CNV_WT_DP0 BD7
CNV_WT_DN1 BG6, CNV_WT_DP1 BF6
CNV_WT_RCOMP BA1 — R1712 — 150R2F-1-GP
PCIE_RCOMPN B12 — R1713 — 100R2F-L1-GP-U
PCIE_RCOMPP A13
SD_RCOMP_1P8 BE5
SD_RCOMP_3P3 BE4
GPPJ_RCOMP_1P81 BD1
GPPJ_RCOMP_1P82 BE1
GPPJ_RCOMP_1P83 BE2
SD_RCOMP — R1714 — 200R2F-L-GP

RSVD2 Y35
RSVD3 Y36
RSVD1 BC1 — PCH_RSVD1 — TP1701 — Do Not Stuff
TP AL35

CANON-LAKE-GP
(071.CANNO.000U)

CNVI

3D3V_S0 — R1728 — DY — Do Not Stuff — TPM_ID — R1729 — 10KR2J-3-GP

PROJECT ID

3D3V_S0 — R1723 — Do Not Stuff — DY — PROJECT_ID2 — R1725 — Do Not Stuff — DY
3D3V_S0 — R1724 — Do Not Stuff — DY — PROJECT_ID1 — R1726 — 10KR2J-3-GP

Selek CFLH N17P

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Title: PCH_(SATA/PCIE/HOST)
Size: Custom
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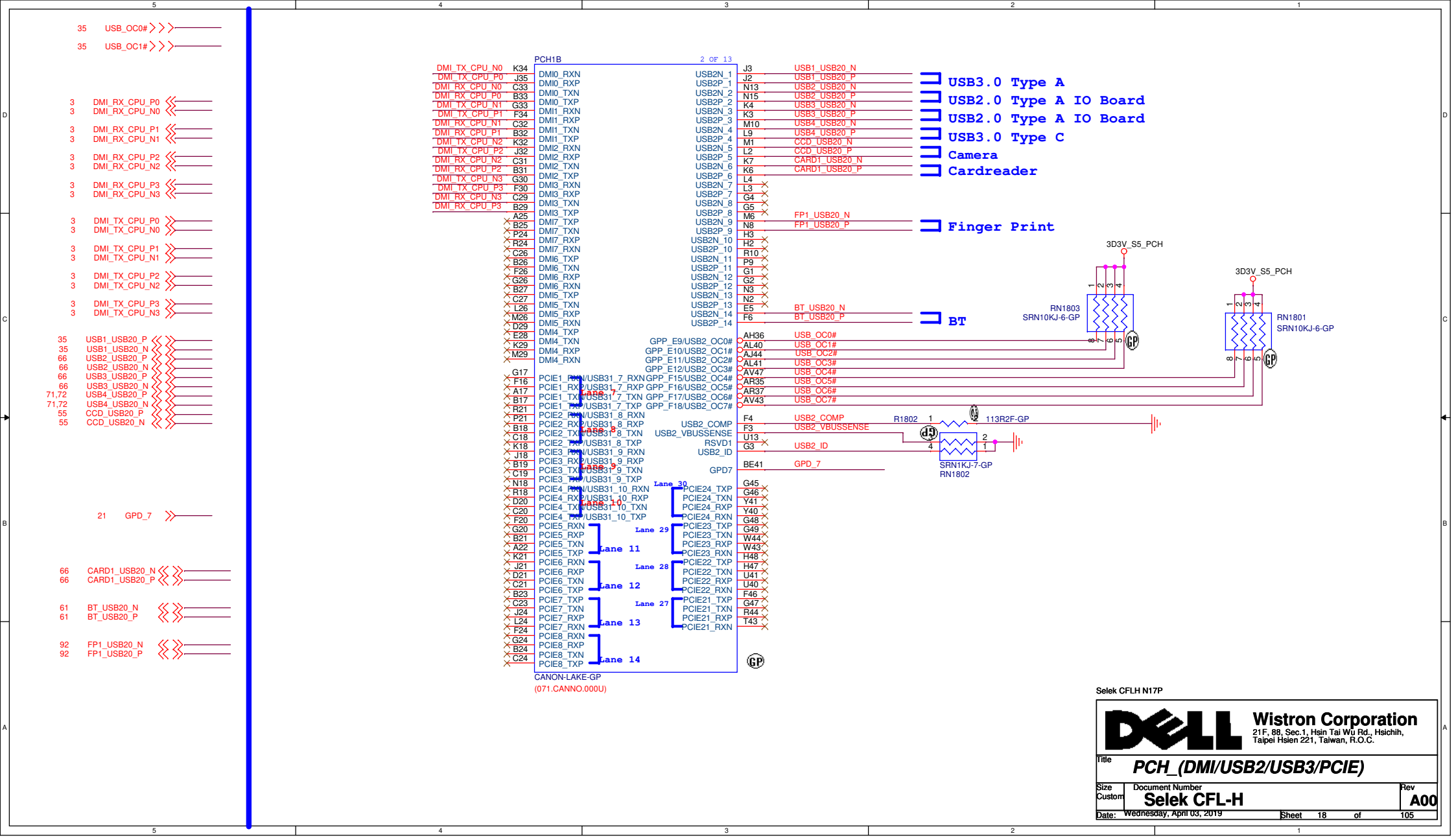

Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH_(DMI/USB2/USB3/PCIE)***

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91 PIRQA#

19,60 HDD_DEVSLP

71,72 CPU_DP_HPD_R

55 EDP_HPD

19,60 HDD_DEVSLP

19,63 mSATA_DEVSLP

19,63 mSATA_DEVSLP

24,68 ESPI_IO[3..0]

35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB30_RX_N
35 USB1_USB30_RX_P

71 USB4_USB30_TX_N
71 USB4_USB30_TX_P
71 USB4_USB30_RX_N
71 USB4_USB30_RX_P

24,68 ESPI_CS#

24,68 ESPI_RESET#

24,68 ESPI_CLK

3D3V_S0

CPU_DP_CTRL_CLK
CPU_DP_CTRL_DATA
RN2011
SRN2K2J-1-GP

Add RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH
R1906 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R1905 10KR2J-3-GP
RTC_RST
Q1901
CPU_DDI1HPD
CPU_DP_HPD_R
CPU_DP_HPD_P
RTC_RST
common part
2N7002KDW-3-GP
75.27002.F7C
2nd = 075.27002.0E7C
R1907 Do Not Stuff
DY

CPU_DDI1HPD
R1902 100KR2J-1-GP

PCH1E 5 OF 13
CPU_DDI1HPD AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DPPD_HPD2/DISP_MISC2
AL15 GPP_I3/DPPE_HPD3/DISP_MISC3
EDP_HPD AN6 GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK AL13 CPU_DP_CTRL_CLK
GPP_I6/DDPB_CTRLDATA AR8 CPU_DP_CTRL_DATA
GPP_I7/DDPC_CTRLCLK AN13
GPP_I8/DDPC_CTRLDATA AL10
GPP_I9/DDPD_CTRLCLK AL9
GPP_I10/DDPD_CTRLDATA AR3
GPP_F23/DDPF_CTRLDATA AN40
GPP_F22/DDPF_CTRLCLK AT49 PCIAUX_GATE
GPP_F14/EXT_PWR_GATE#/PS_ON# AP41 PROC_DETECT#
GPP_K23/IMGCLKOUT1 M45
GPP_K22/IMGCLKOUT0 L48
GPP_K21 T45
GPP_K20 T46
GPP_H23/TIME_SYNC0 AJ47
CANON-LAKE-GP
(071.CANNO.000U)
TP1901 Do Not Stuff

6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation

Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.

Note: When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPD) for HPD connectivity.

For eSPI

ESPI_IO[3..0]
ESPI_IO0 R1921 15R2F-2-GP ESPI_IO0_R
ESPI_IO1 R1922 15R2F-2-GP ESPI_IO1_R
ESPI_IO2 R1923 15R2F-2-GP ESPI_IO2_R
ESPI_IO3 R1924 15R2F-2-GP ESPI_IO3_R

3D3V_S5_PCH 1214
PROC_DETECT# R1920 20KR2J-L2-GP

3D3V_S0
PIRQA# R19111 10KR2J-3-GP
ESPI_ALERT1# R1912 DY Do Not Stuff

ESPI_RESET# R1919 DY Do Not Stuff

USB3.0 Type A

USB3.0 Type C(for N18P)

PCH1F 6 OF 13
USB1_USB30_TX_N F9 USB31_1_TXN
USB1_USB30_TX_P F7 USB31_1_TXP
USB1_USB30_RX_N D11 USB31_1_RXN
USB1_USB30_RX_P C11 USB31_1_RXP
Lane 1
C3 USB31_2_TXN
D4 USB31_2_TXP
B9 USB31_2_RXN
C9 USB31_2_RXP
Lane 2
C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
Lane 6
C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP
Lane 5
G12 USB31_3_TXP
F11 USB31_3_TXN
C10 USB31_3_RXP
B10 USB31_3_RXN
Lane 3
USB4_USB30_TX_P C14 USB31_4_TXP
USB4_USB30_TX_N B14 USB31_4_TXN
USB4_USB30_RX_P J15 USB31_4_RXP
USB4_USB30_RX_N K16 USB31_4_RXN
Lane 4
CANON-LAKE-GP
(071.CANNO.000U)

GPP_A1/LAD0/ESPI_IO0 BB39 ESPI_IO0_R
GPP_A2/LAD1/ESPI_IO1 AW37 ESPI_IO1_R
GPP_A3/LAD2/ESPI_IO2 AV37 ESPI_IO2_R
GPP_A4/LAD3/ESPI_IO3 BA38 ESPI_IO3_R
GPP_A5/LFRAME#/ESPI_CS0# BE38 ESPI_CS#
GPP_A6/SERIRQ/ESPI_CS1# AW35
GPP_A7/PIRQA#/ESPI_ALERT0# BA36 PIRQA#
GPP_A0/RCIN#/ESPI_ALERT1# BE39 ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET# BF38 ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK BB36 ESPI_CLK_R
GPP_A10/CLKOUT_LPC1 BB34
GPP_K19/SMI# T48
GPP_K18/NMI# T47
GPP_E6/SATA_DEVSLP2 AH40 mSATA_DEVSLP
GPP_E5/SATA_DEVSLP1 AH38
GPP_E4/SATA_DEVSLP0 AL48 HDD_DEVSLP
GPP_F9/SATA_DEVSLP7 AP47
GPP_F8/SATA_DEVSLP6 AN37
GPP_F7/SATA_DEVSLP5 AN46
GPP_F6/SATA_DEVSLP4 AR41
GPP_F5/SATA_DEVSLP3 AP48

ESPI_CLK_R R1914 33R2F-3-GP ESPI_CLK
DY Do Not Stuff ECI 1901

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(DDI/USB3/GPIO)

Size	Document Number	Rev
Custom	Selek CFL-H	A00

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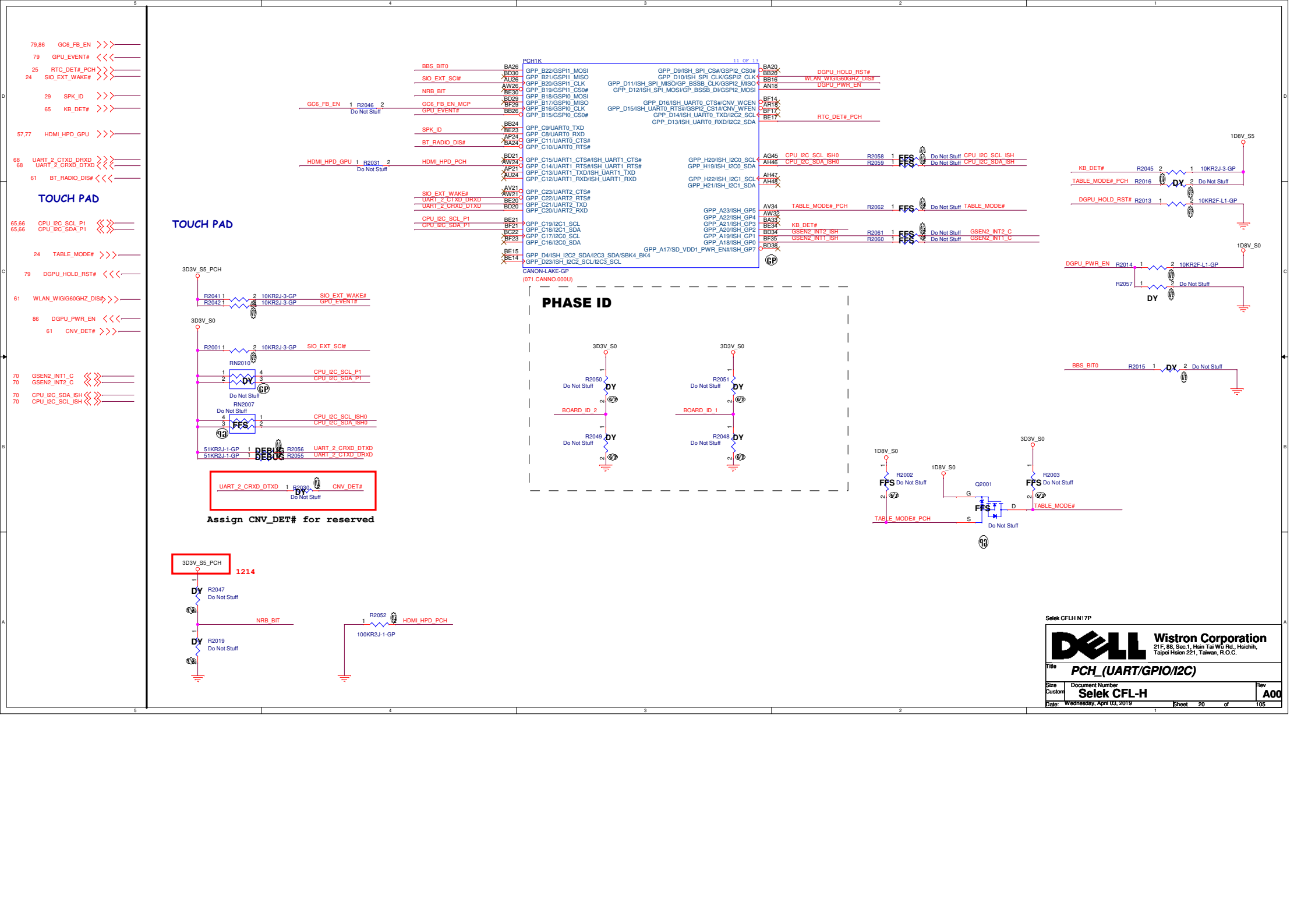
79,86 GC6_FB_EN
79 GPU_EVENT#
25 RTC_DET#_PCH
24 SIO_EXT_WAKE#
29 SPK_ID
65 KB_DET#
57,77 HDMI_HPD_GPU
68 UART_2_CTXD_DRXD
68 UART_2_CRXD_DTXD
61 BT_RADIO_DIS#
TOUCH PAD
65,66 CPU_I2C_SCL_P1
65,66 CPU_I2C_SDA_P1
24 TABLE_MODE#
79 DGPU_HOLD_RST#
61 WLAN_WIGIG60GHZ_DIS#
86 DGPU_PWR_EN
61 CNV_DET#
70 GSEN2_INT1_C
70 GSEN2_INT2_C
70 CPU_I2C_SDA_ISH
70 CPU_I2C_SCL_ISH
TOUCH PAD
PCH1K
11 OF 13
CANON-LAKE-GP
(071.CANNO.000U)
BBS_BIT0
SIO_EXT_SCI#
NRB_BIT
GC6_FB_EN
R2046
Do Not Stuff
GC6_FB_EN_MCP
GPU_EVENT#
SPK_ID
BT_RADIO_DIS#
HDMI_HPD_GPU
R2031
Do Not Stuff
HDMI_HPD_PCH
SIO_EXT_WAKE#
UART_2_CTXD_DRXD
UART_2_CRXD_DTXD
CPU_I2C_SCL_P1
CPU_I2C_SDA_P1
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DGPU_HOLD_RST#
WLAN_WIGIG60GHZ_DIS#
DGPU_PWR_EN
RTC_DET#_PCH
CPU_I2C_SCL_ISH0
CPU_I2C_SDA_ISH0
CPU_I2C_SCL_ISH
CPU_I2C_SDA_ISH
TABLE_MODE#_PCH
TABLE_MODE#
KB_DET#
GSEN2_INT2_ISH
GSEN2_INT1_ISH
GSEN2_INT2_C
GSEN2_INT1_C
PHASE ID
3D3V_S5_PCH
3D3V_S0
R2041
R2042
10KR2J-3-GP
RN2010
RN2007
Do Not Stuff
DEBUG
R2056
R2055
UART_2_CRXD_DTXD
UART_2_CTXD_DRXD
51KR2J-1-GP
R2030
CNV_DET#
Assign CNV_DET# for reserved
R2050
R2049
R2051
R2048
BOARD_ID_2
BOARD_ID_1
1D8V_S0
R2002
R2003
Q2001
1D8V_S5
R2045
R2016
R2013
10KR2J-3-GP
10KR2F-L1-GP
R2014
R2057
R2015
3D3V_S5_PCH
1214
R2047
R2019
NRB_BIT
R2052
100KR2J-1-GP
HDMI_HPD_PCH
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH_(UART/GPIO/I2C)
Size
Custom
Document Number
Selek CFL-H
Rev
A00
Date:
Wednesday, April 03, 2019
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of
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VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.

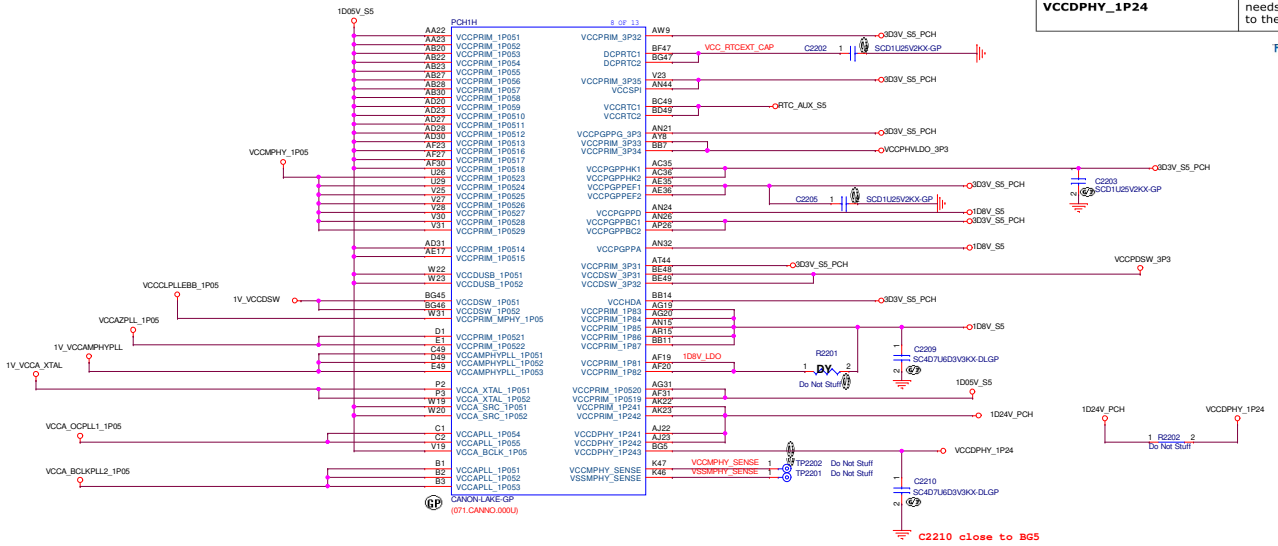
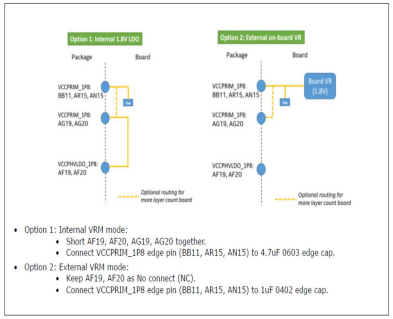
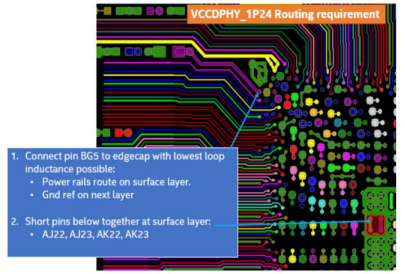


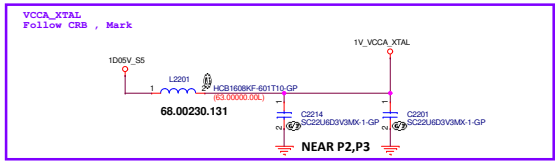
Figure 50-9. CFL PCH-H Power Rail VRM Recommendations

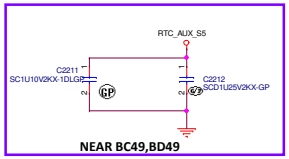


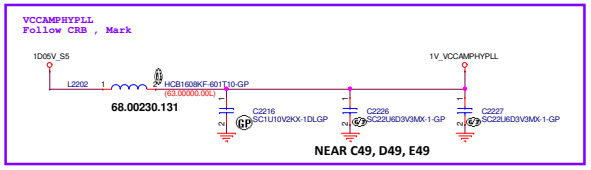
- Option 1: Internal VRM mode:
  - Short AF19, AF20, AG19, AG20 together.
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 4.7uF 0603 edge cap.
- Option 2: External VRM mode:
  - Keep AF19, AF20 as No connect (NC).
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 1uF 0402 edge cap.

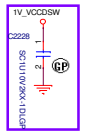
CFL PCH-H VCCDPHY_1P24 Routing

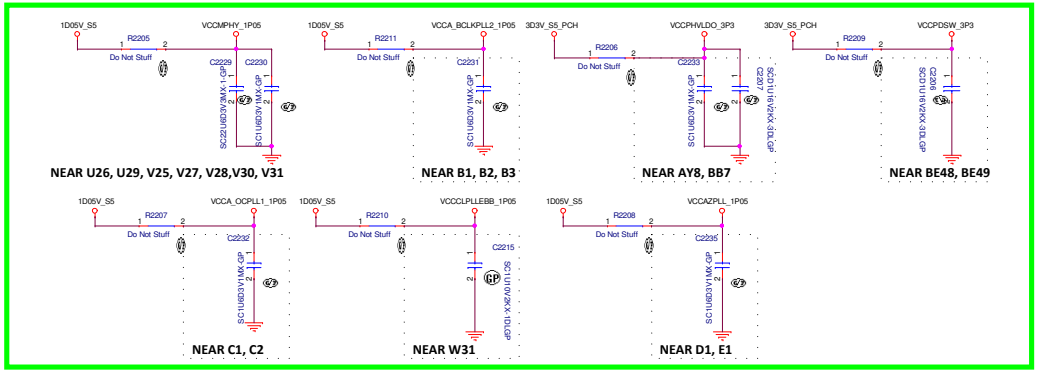












Selek CFLH N17P

Wistron Corporation
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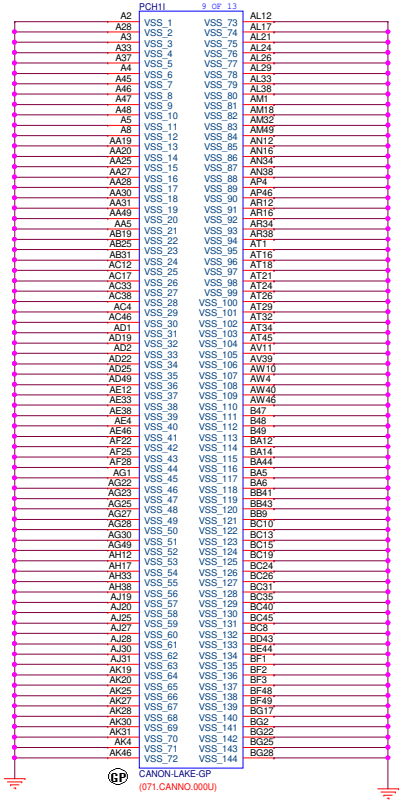
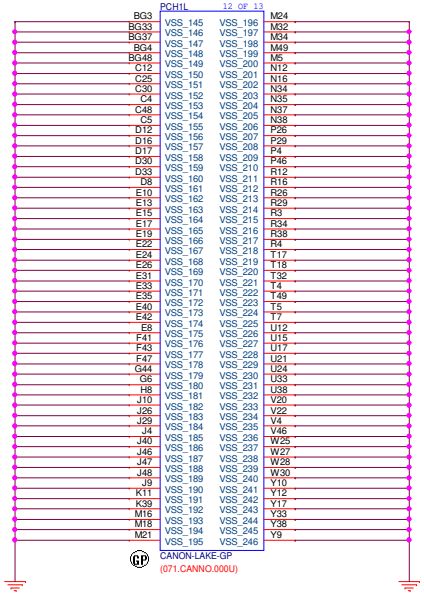
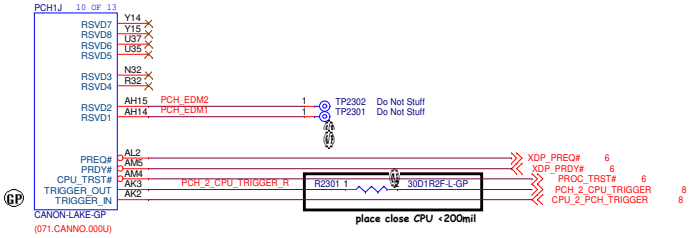
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_POWER
Size: Custom | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 22 of 105







Selek CFLH N17P

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS/GPIO)

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 23 of 105

Main Func = KBC

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTO	VOLTAGE
1	Nivida-N17P-G0-K1	100.0K	**10.0K**	3
2		100.0K	**17.8K**	2.801
3	Nivida-N18P-G0	100.0K	**27.0K**	2.598
4		100.0K	**37.4K**	2.402
5	Nivida-N18E-G0	100.0K	**49.9K**	2.201
6		100.0K	**64.9K**	2.001
7	Nivida-N18E-G1	100.0K	**82.5K**	1.808
8		100.0K	**107K**	1.594
9		100.0K	**154K**	1.299
10		100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

Layout Note:
Need very close to EC

X01 20161227 change

BATTER /CHARGER

CPU/ GPU/ Thermal
For I2C/USB Mux

Need very close to EC,
PDG: <0.5 inches.

ALL_SYS_PWRGD (RUNPWROK) assert,
delay 10ms; PCH_PWROK(RESET_OUT#) assert.

071.01416.000G

082.30003.0301
2nd = 082.30003.0191

Microchip: Use CL=9p Xtal - C - 9p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

For eSPI

GPIO102 (CR_STRAP) GPIO123 (BSS_STRAP)

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

75.00054.A7D

EC LCD test

DEBUG
20.K0691.006

For USB TypeC

For CCG5

Need check

Follow EV project circuit DY Q2417 (R013_20171026)

Power Switch Logic(PSL)

84.2N702.J31
2ND = 084.27002.0N31

2ND = 83.0005V.0AF

EMI i229

75.27002.F7C
2nd = 075.67002.007C
3rd = 075.06301.007C

180118

84.2N702.J31
2ND = 084.27002.0N31

Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC MEC1416
Size: A1 | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (32M byte) for PCH

15 SPI_CS_ROM_N0
15,21,91 SPI_SO_CPU
15,21 SPI_WP_CPU
15,21 SPI_HOLD_CPU
15,91 SPI_CLK_CPU
15,21,91 SPI_SI_CPU
15 SPI_CS_ROM_N1

3D3V_S5_PCH
C2501 SC10U6D3V3MX-DL-GP
C2502 SCD1U16V2KX-3DLGP
R2501 4K7R2J-2-GP
SPI25
CS# SO/SIO1 SIO2 GND
VCC SIO3 SCLK SI/SIO0
MX25L12872FMI-10G-GP
072.25128.0D61
R2518 R2517 33R2F-3-GP
R2519 R2520 R2521 33R2F-3-GP
SPI_CS_ROM_N0 SPI_SO_ROM SPI_WP_ROM
SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM
SPI_HOLD_CPU SPI_CLK_CPU SPI_SI_CPU

R2502 Do Not Stuff DY
SPI251
R2526 R2525 Do Not Stuff DY
R2522 R2523 R2524 Do Not Stuff DY
SPI_CS_ROM_N1
Do Not Stuff

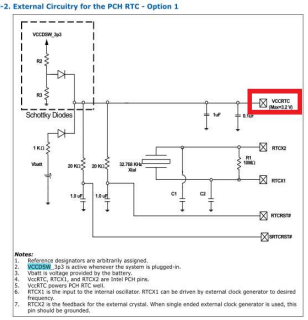
Main Func = RTC

BTY RTC CR2016_30MM KTS 2PIN
1st= 23.25212.011
-1 20161118

3D3V_AUX_S5
R2505 0R2J-GP
3D3V_RTC_SYS
3D3V_RTC_PWR
R2503 Do Not Stuff DY
D2501 BAT54C-12-GP
75.00054.A7D
3D3V_RTC_AUX
C2503 SCD47U25V3KX-1-DL-GP
RTC1 PWR GND NP1 NP2
BAT-560201-0ER-GP-U
062.70001.0101
R2506 1KR2J-1-GP

Q2505 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
20180102
R2504 10MR2J-L-GP
RTC_DET# D2504 1SS355T1G-GP
83.00355.G1F
RTC_DET#_PCH
R2040 10KR2J-3-GP RTC_DET#

Figure 28-2. External Circuitry for the PCH RTC - Option 1



Notes:
1. Reference designators are arbitrarily assigned.
2. VCCDSW_3p3 is active whenever the system is plugged-in.
3. Vbatt is voltage provided by the battery.
4. VccRTC, RTCX1, and RTCX2 are Intel PCH pins.
5. VccRTC powers PCH RTC well.
6. RTCX1 is the input to the internal oscillator. RTCX1 can be driven by external clock generator to desired frequency.
7. RTCX2 is the feedback for the external crystal. When single ended external clock generator is used, this pin should be grounded.

20 RTC_DET#_PCH
24 RTCRST_ON
24 VCCDSW_EN#
15,40,45 3V_5V_POK
52,53 3V_5V_DSW_OK

3D3V_RTC_AUX
R2515 NON_RTC_RST Do Not Stuff
Q2501 PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
RTC_AUX_S5
RTC_RST
R2514 4K7R2J-2-GP
RTC_3P3_EN_D
D2503 Do Not Stuff DY
2ND = 83.R5003.T8F
Q2502 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
RTCRST_ON
R2512 1MR2J-1-GP
RTC_3P3_EN_G
R2513 100KR2J-1-GP
C2504 SCD022U16V2KX-3DLGP

3D3V_S5
R2509 100KR2J-1-GP
VCCDSW_EN#
C2505 Do Not Stuff DY
R2508 NON_RTC_RST Do Not Stuff
R2510 10KR2J-3-GP
3V_5V_POK
3V_5V_DSW_OK
D2502 BAT54A-11-GP
RTC_RST
75.BAT54.07D
2ND = 75.00054.Q7D
U2502 SY6288C20AAC-GP
074.06288.007B
2nd = 074.03553.007F
R2516 Do Not Stuff
NON_RTC_RST

RTC GEN9

Selek CFLH N17P

Wistron Corporation
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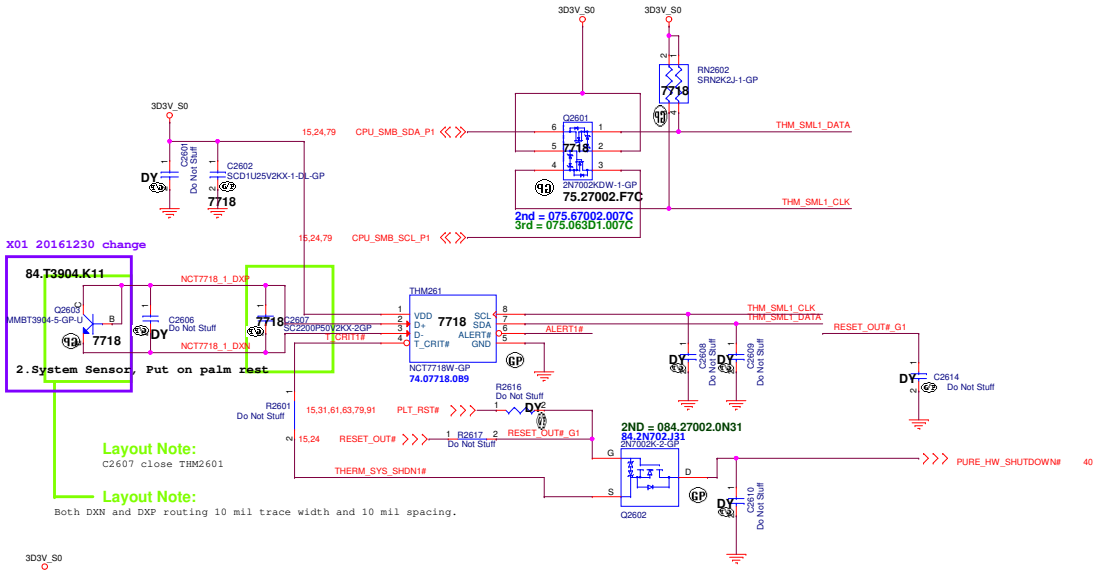
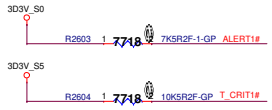
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC
Size: A2
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 25 of 105

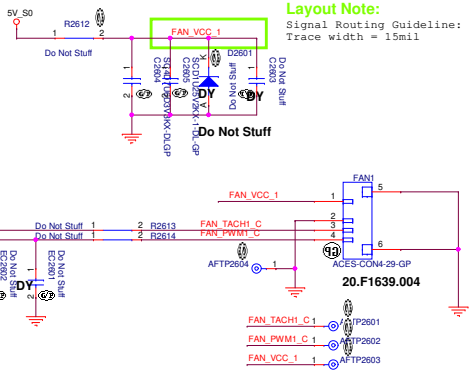
Main Func = Thermal Sensor



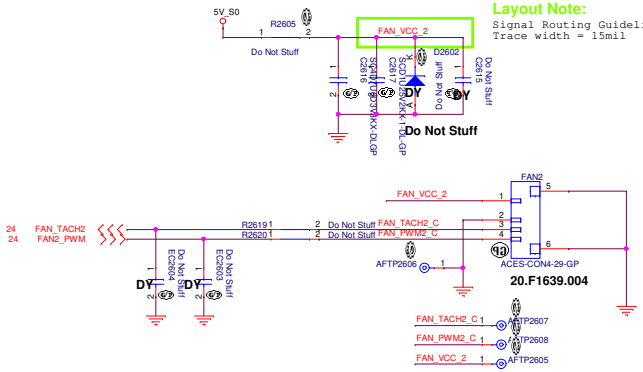


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



PWM FAN2



Selek CFLH N17P

Wistron Corporation
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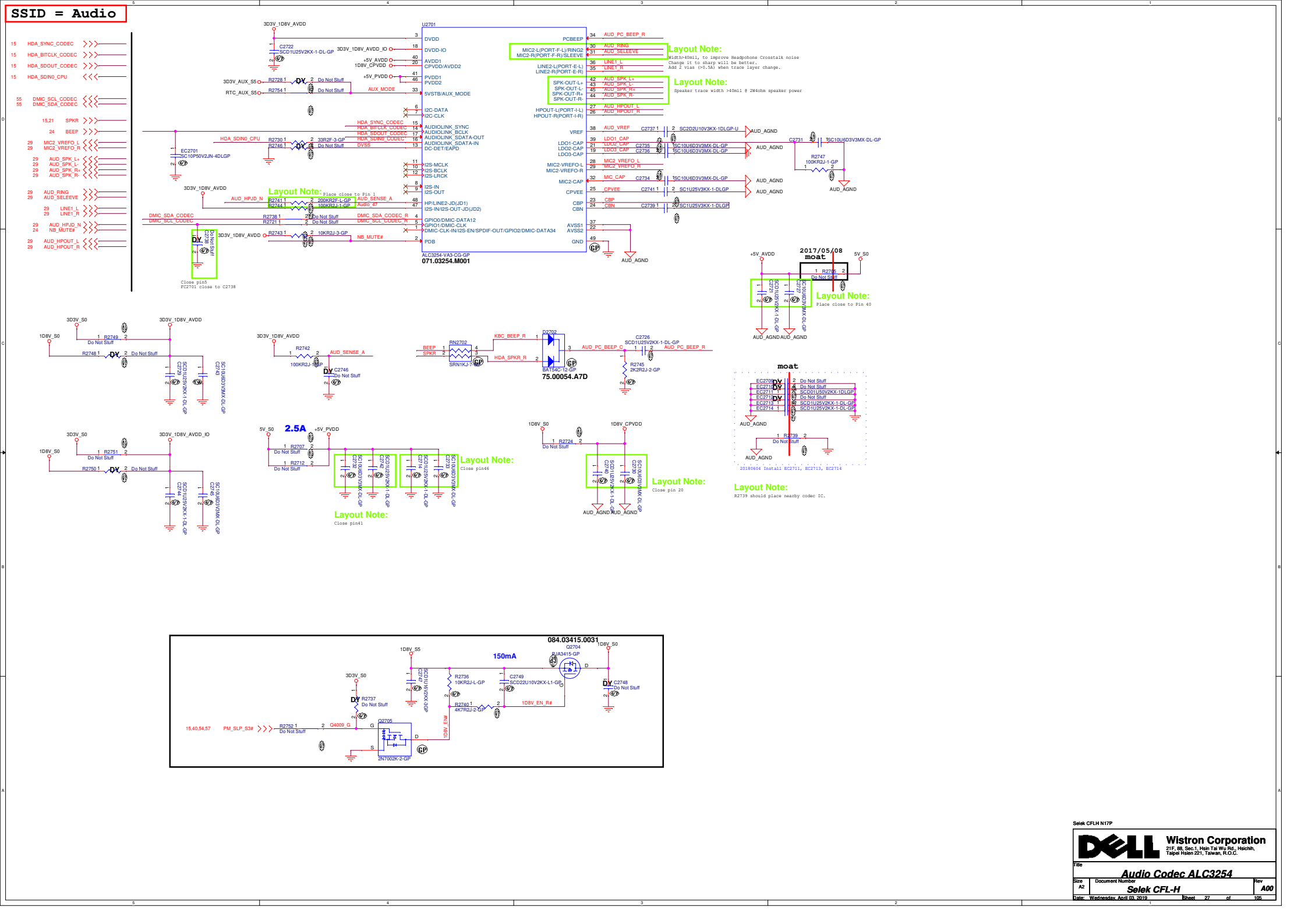
Title: THERMAL NCT7718W/Fan

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 26 of 105

SSID = Audio



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3254

Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 27 of 105

Main Func = Audio

20 SPK_ID

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

27 MIC2_VREFO_R
27 MIC2_VREFO_L
27 AUD_RING
27 AUD_HPOUT_L
27 LINE1_L
27 AUD_HPOUT_R
27 LINE1_R
27 AUD_SELEEVE
27 AUD_HPJD_N

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

3D3V_S0
R2915 10KR2J-3-GP
SPK1
ACES-CON6-20-GP-U
20.F1639.006
SC1KP50V2KX-1DLGP
AFTP2901
AFTP2902
AFTP2903
AFTP2904
12/17 Clark move close to connector

Universal Jack (Moved to I/O Board)

RN2901 SRN2K2J-1-GP
C2907 LINE1-L_C SC10U6D3V3MX-DL-GP
C2908 LINE1-L_R SC10U6D3V3MX-DL-GP
R2908 R2910 Do Not Stuff
R29111 R29121 10R2F-L-GP
20180223 Modify to 10R
SC680P50V2KX-2DLGP
JACK_PLUG_DET 10 mils
R2905 Do Not Stuff
AUD_AGND

Layout Note:
EC2908 EC2907 should place nearby codec IC.

CLOSS TO HPMIC1
ED2901 ED2902 ED2903
AZ5125-02S-R7G-GP
75.05125.07D

R2914 Do Not Stuff
10 mils
Delay circuit
(JACK_PLUG_DET: on IO Board)
DY C2909 Do Not Stuff

HPMIC1
AUDIO-JK440-GP
022.10002.0111

Selek CFLH N17P

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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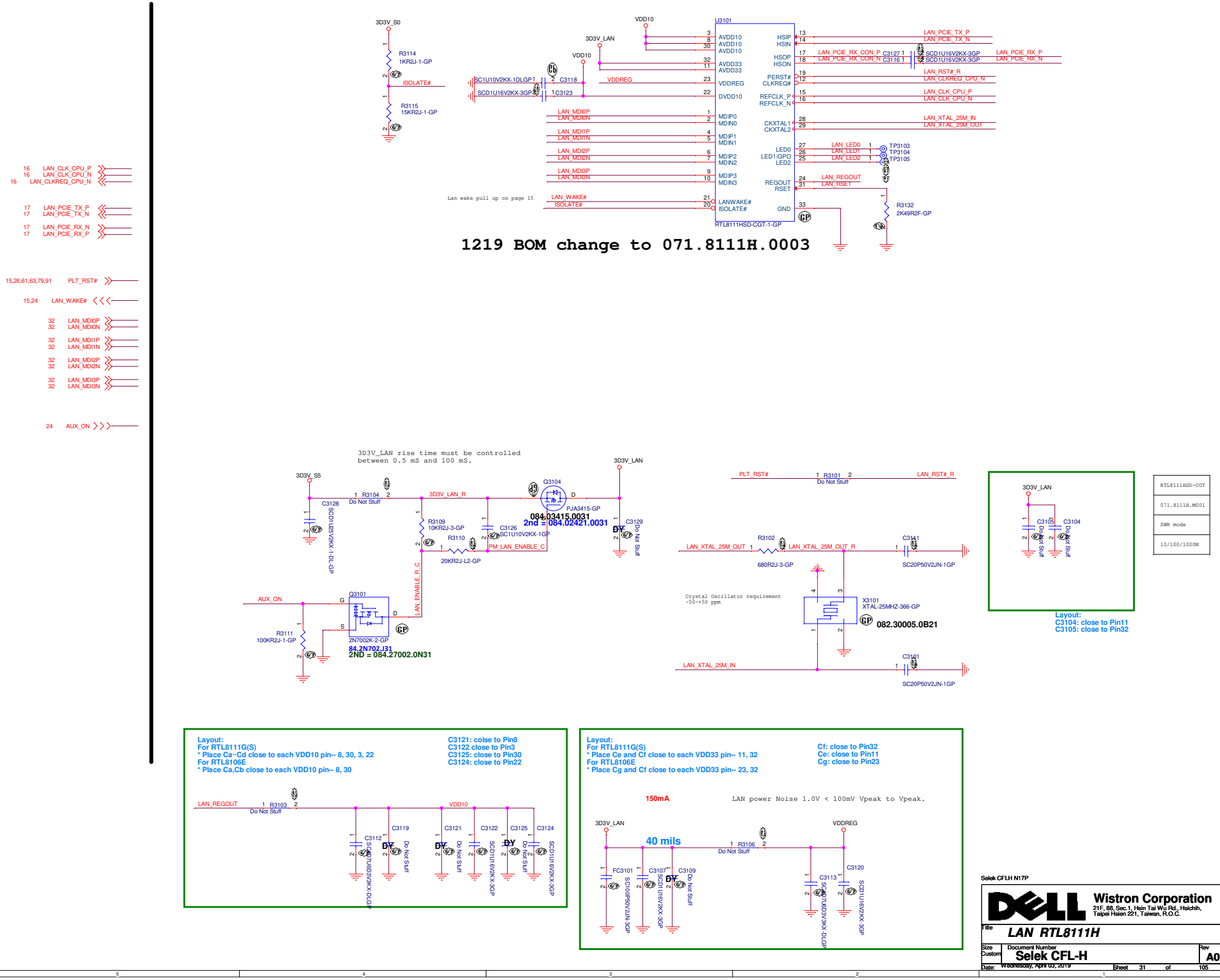
Title: Audio IO
Size: A3
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 29 of 105



Selek CFLH N17P

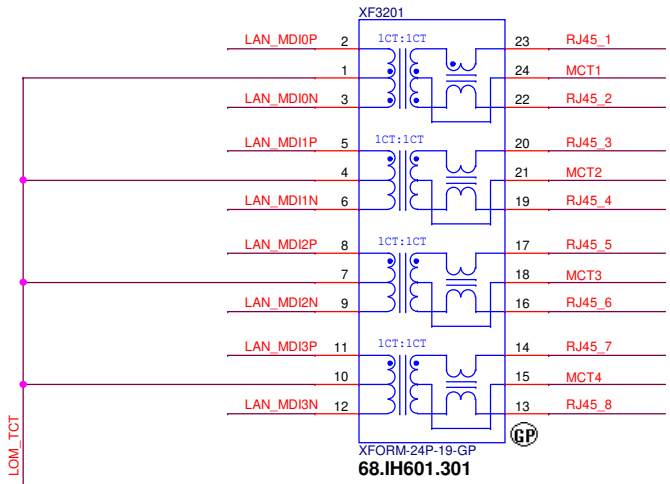
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

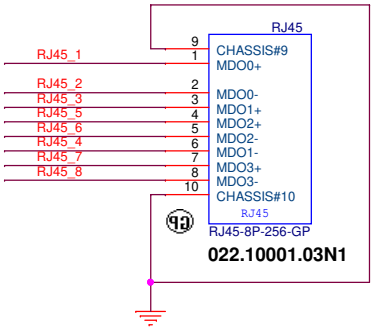
Title: LAN RTL8111H

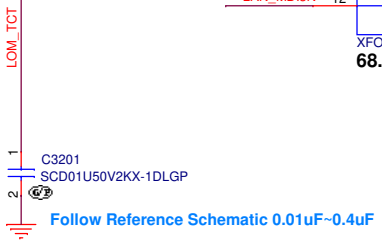
Size: Custom | Document Number: Selek CFL-H | Rev: A00

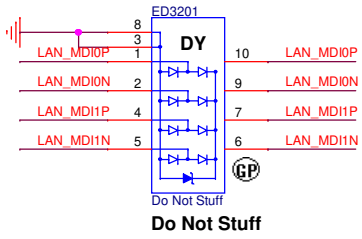
Date: Wednesday, April 03, 2019 | Sheet 31 of 105

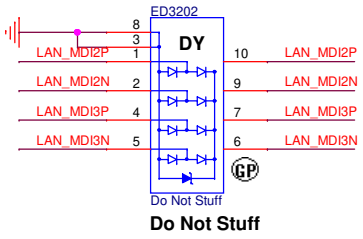
SSID = LAN

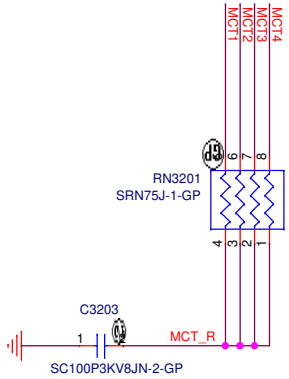












Selek CFLH N17P

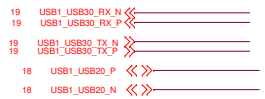
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

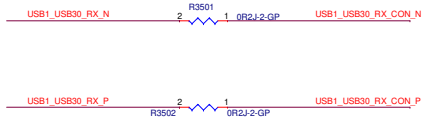
Title: ***RJ45+Transformer***

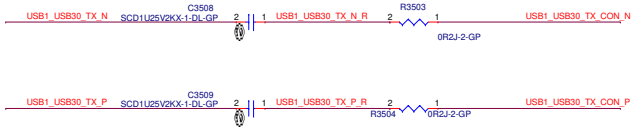
Size	Document Number	Rev
B	Selek CFL-H	A00

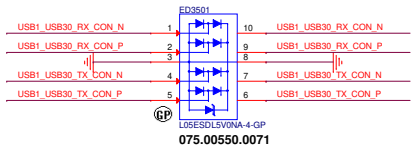
Date: Wednesday, April 03, 2019 Sheet 32 of 105

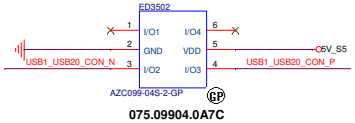
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

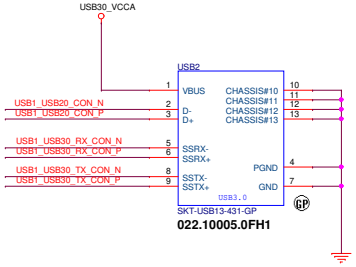


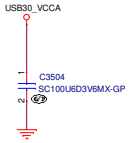




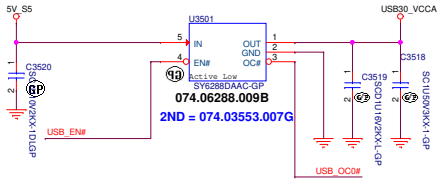


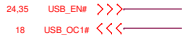




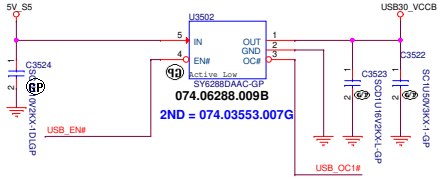


For USB3.0 port use





For IO USB2.0 port use



Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0*2 CONN	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 35 of 105	

Power Sequence

15,27,54,57 PM_SLP_S3# >>>

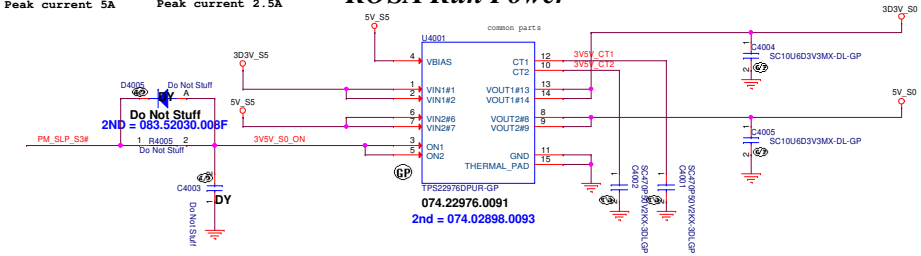
5V_S0

5V_S0 Comsumption
Peak current 5A

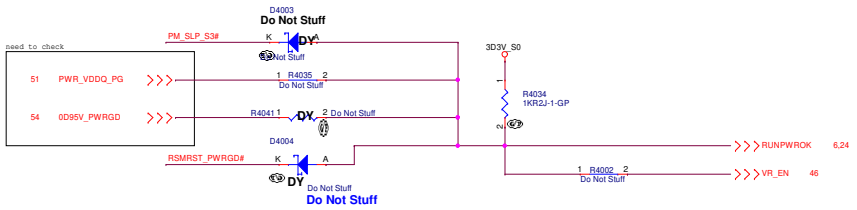
3D3V_S0

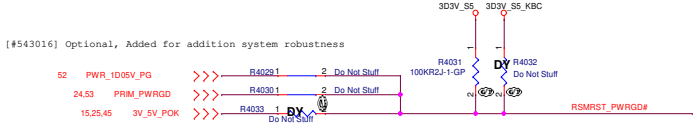
3D3V_S0 Comsumption
Peak current 2.5A

ROSA Run Power

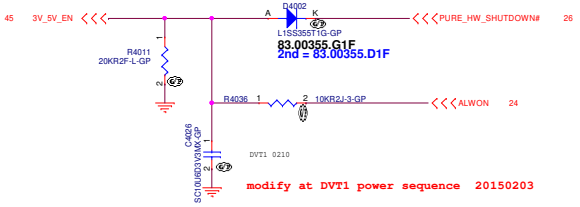


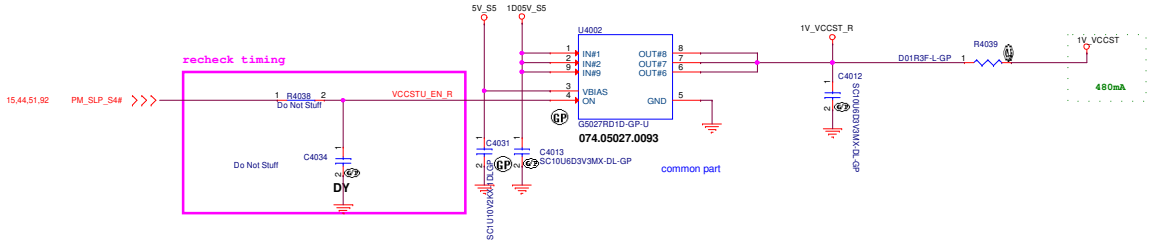
Power Good





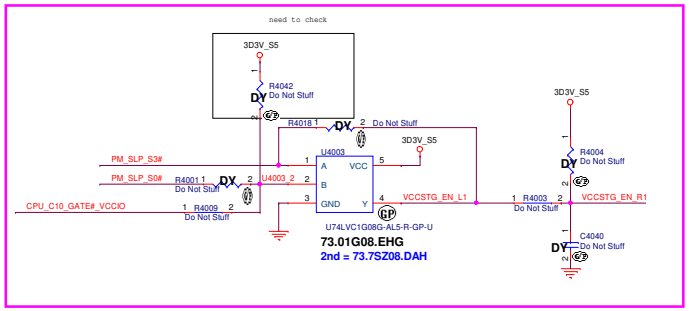
1V_VCCST



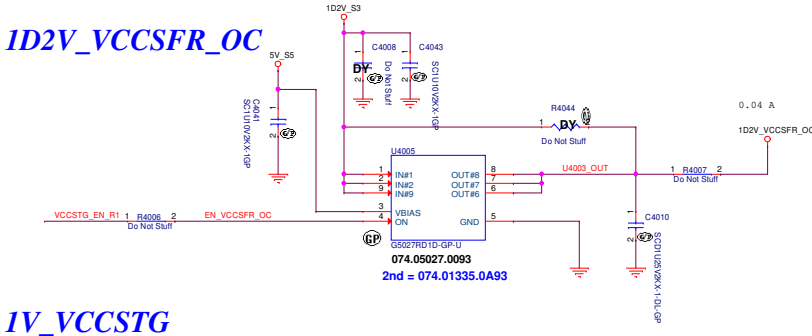


15,91 PM_SLP_S0#
17 CPU_C10_GATE#
54 CPU_C10_GATE#_VCCIO

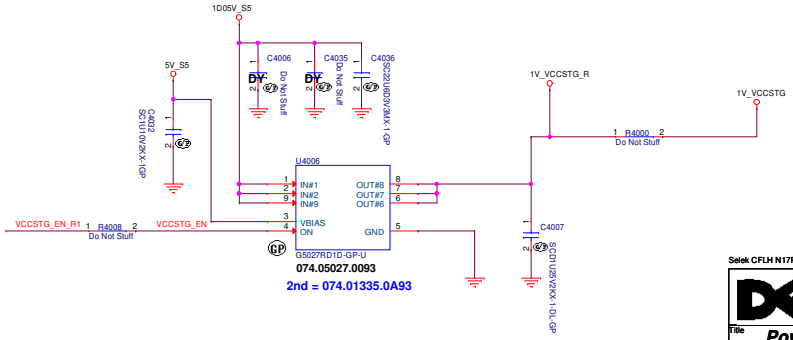
Sequence reserve

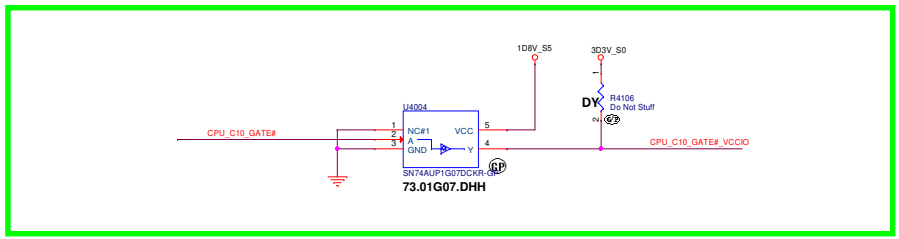


1D2V_VCCSFR_OC



1V_VCCSTG





Selek CFLH N17P

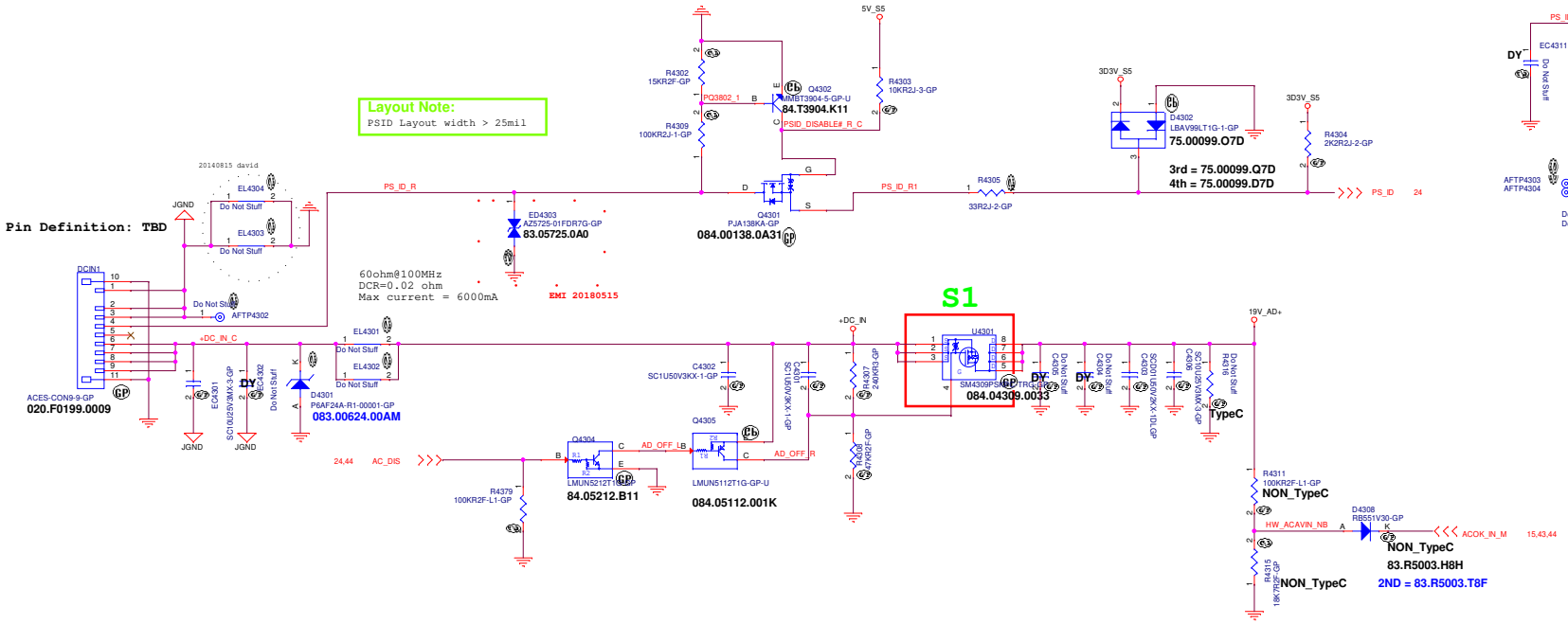
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Selek CFL-H | Rev: A00

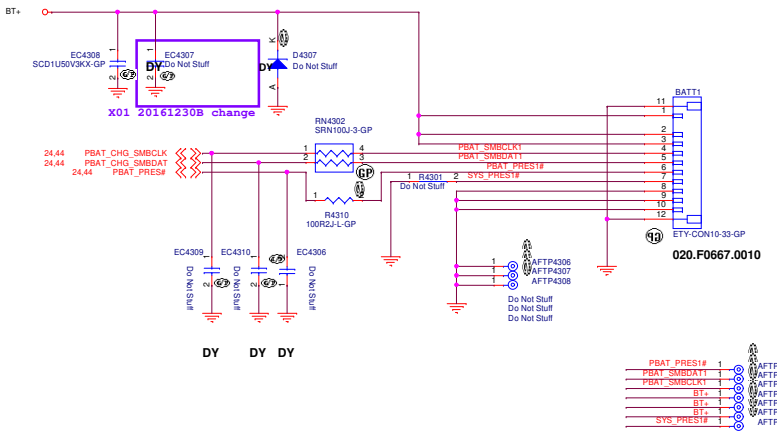
Date: Wednesday, April 03, 2019 | Sheet 40 of 105

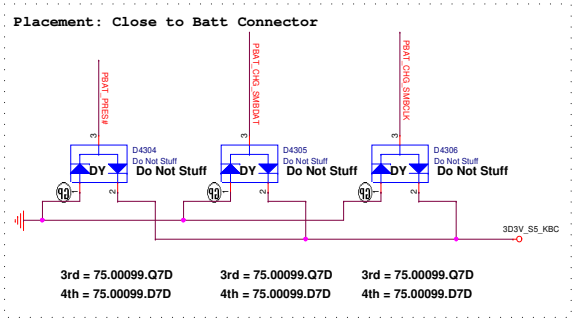
Main Func = ADT Input



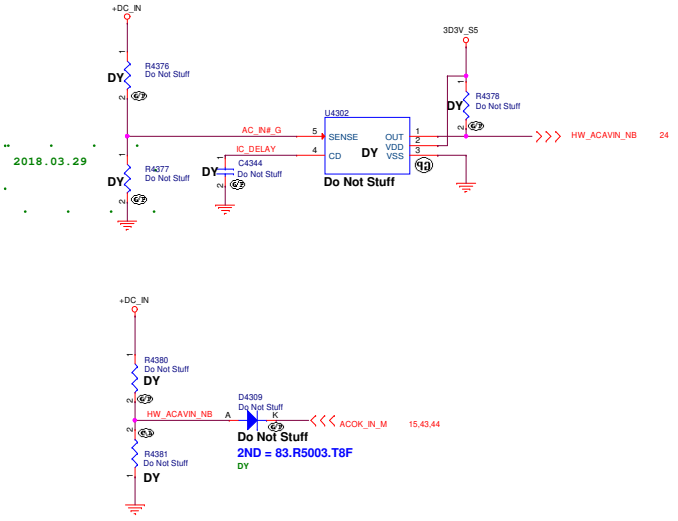
Main Func = M-BAT Input

Batt Connecter





Barrel Adapter Piug-in Detect



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
Size: A2	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 43 of 105	

Main Func = Charger

ISL95522 Hybrid Charger

OFF PAGE

need to check

24,64 HW_ACAV_IN — PR4403 1 2 Do Not Stuff — HW_ACAV_IN_M

24,43 AC_DS

15,40,51,92 PM_SLP_S4#

15,43 ACOK_IN_M

24,43 PBAT_CHG_SMBDAT

24,43 PBAT_CHG_SMBCLK

24,43 PBAT_PRES#

6,24,46 PROCHOT#_CPU

24 AD_IA

46 CHGR_PSYS_IMVP

24 boost_mon

E3

66 BT_PWR_IN+

66 BT_PWR_IN-

$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times PR4433}$$

$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times PR4436}$$

Power Team 0402

VAC DET
Greater than 2.633 V
Less than 3.5 V

AC_IN:3.35~3.75V

10*11.5*4
DCR=6.1~6.8mohm
Idc=15A, Isat=18A

68.2R210.20J

Need fine tune

Battery PROCHOT# Circuit

PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

CPU PROCHOT# Circuit

Selek CFL-H N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

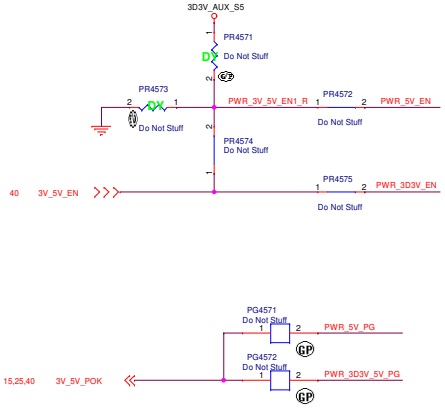
Title: Charger

Size: A1 | Document Number: Selek CFL-H | Rev: A00

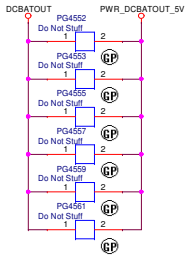
Date: Wednesday, April 03, 2019 | Sheet 44 of 105

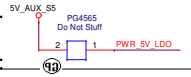
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

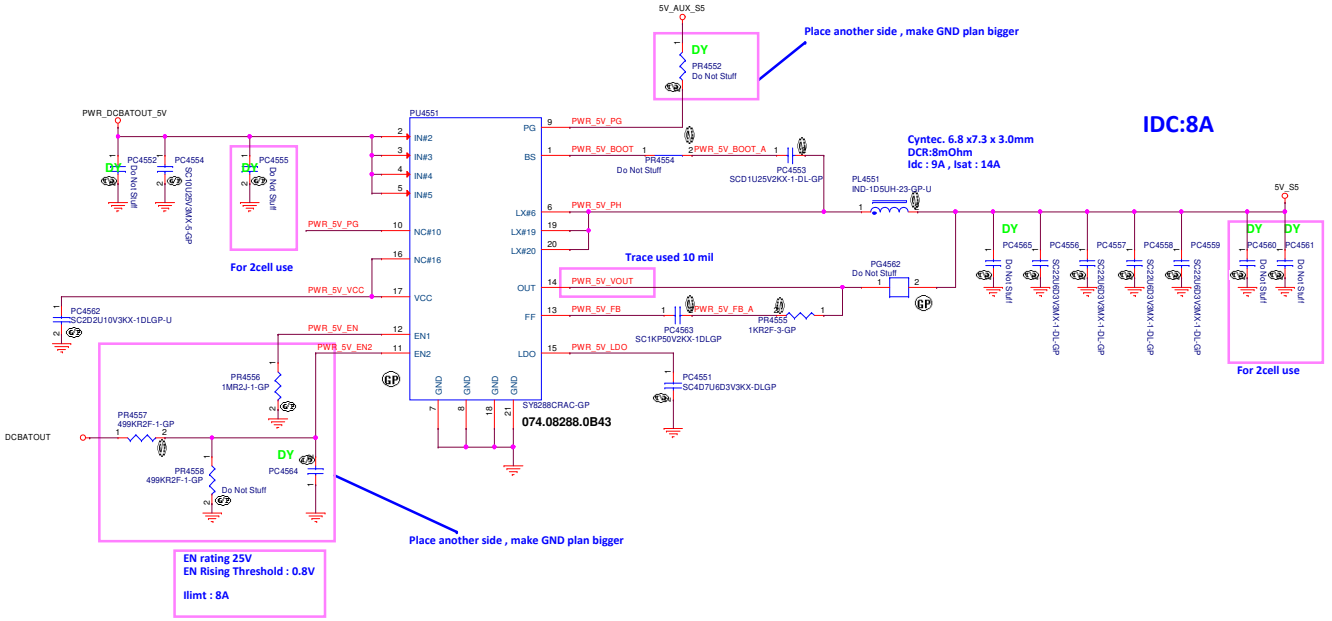


OFFPAGE-GAP





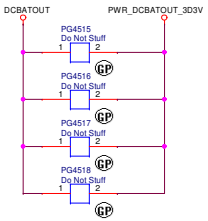
SY8288C For 5V

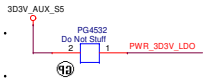


SSID = PWR.Plane.Regulator_3D3V

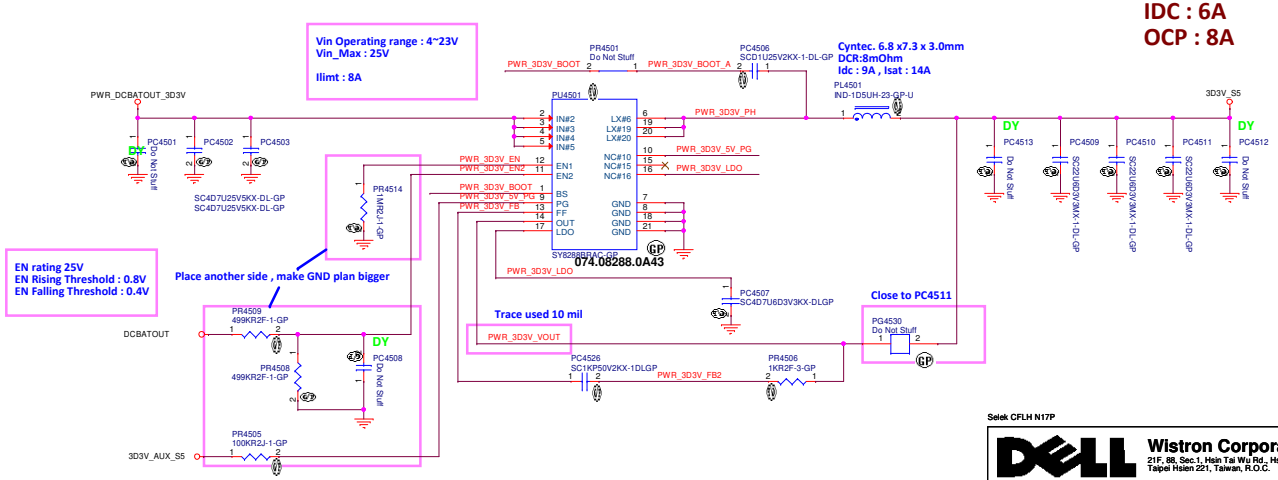
OFFPAGE-Signal

OFFPAGE-GAP





SY8286B For 3D3V



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size	Document Number	Rev
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OFFPAGE

VCCSA SENSE

VCCCORE SENSE

VCCGT_I SENSE

Close to VCCSA Choke

Close to Vcore Choke

Close to VCCGT_I Choke

VCCCORE Feedback

VCCGT Feedback

VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V

Close to VCORE Dr.MOS

Close to VCCGT_I Dr.MOS

Add : PWR GAP
change GND symbol on this page ALL GND

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC IMVP8

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 46 of 105

For acousaic noise 1228

DCBATOUT
PWR_DCBATOUT_VCCCORE
PL4711
PBY201209T-170Y-N-GP
PL4712
PBY201209T-170Y-N-GP
PT4711
SE33U25VM-11-GP
PL4701
DY
Do Not Stuff

EE 0401

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

PC4713 PC4714 PC4715 PC4716 PC4717
SC1U25V5KX-DL-GP
SCD1U25V2KX-1DL-GP

PU4702
NCP302045MNTWG-1-GP
074.30204.0AE3

VIN PHASE BOOT VCC VCCD
PWM DISB#
THWN SMOD#
PGND
GL#27 GL#33 NC#6 AGND CGND
VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22
VSW#26 VSW#25 VSW#24 VSW#23

PWR_CORE_BOOT_PH1
PR4703 3D9R3-GP
PC4702 SCD22U25V3KX-GP
PWR_CORE_BOOT_A_PH1
PWR_CORE_PHASED_PH1

PWR_CORE_VCCA
PR4704 2R2J-2-GP
PC4703 SC1U10V2KX-1GP
PC4704 SC1U10V2KX-1GP
5V_S5

PWR_CORE_DISB#_PH1
PR4705 Do Not Stuff
PWR_VCCCORE_PWM1 46
PWR_CORE_DRVON 46,47,48,49,50
PWR_CORE_THWN_PH1
PR4717 DY Do Not Stuff
5V_S5

PWR_CORE_PH1
PC4705 SC680P50V2KX-2DLGP
PWR_CORE_SNB_PH1
PR4708 2D2R3-1-U-GP

PL4701
COIL-D15UH-2-GP
68.R1510.20A
1V_CPU_CORE

PG4701 Do Not Stuff
PG4702 Do Not Stuff
PWR_CORE_ISEN1_N 46
PWR_CORE_ISEN1_P 46

CFL_H-45W
IMAX 96 A / TDC 75 A / OCP 120 A
PT4701 PT4702 PT4703 PT4704
SE330U2DM-4-GP
330uF 4 Pcs
1V_CPU_CORE

EE 0401

MLCCs must be placed symmetrically on Top and Bottom.

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

PC4757 PC4758 PC4759 PC4760 PC4761
SC1U25V5KX-DL-GP
SCD1U25V2KX-1DL-GP

PU4701
NCP302045MNTWG-1-GP
074.30204.0AE3

VIN PHASE BOOT VCC VCCD
PWM DISB#
THWN SMOD#
PGND
GL#27 GL#33 NC#6 AGND CGND
VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22
VSW#26 VSW#25 VSW#24 VSW#23

PWR_CORE_BOOT_PH2
PR4711 3D9R3-GP
PC4706 SCD22U25V3KX-GP
PWR_CORE_BOOT_A_PH2
PWR_CORE_PHASED_PH2

PWR_CORE_VCCB
PR4712 2R2J-2-GP
PC4707 SC1U10V2KX-1GP
PC4708 SC1U10V2KX-1GP
5V_S5

PWR_CORE_DISB#_PH2
PR4713 Do Not Stuff
PWR_VCCCORE_PWM2 46
PWR_CORE_DRVON 46,47,48,49,50
PWR_CORE_THWN_PH2
PR4718 DY Do Not Stuff
5V_S5

PWR_CORE_PH2
PC4774 SC680P50V2KX-2DLGP
PWR_CORE_SNB_PH2
PR4716 2D2R3-1-U-GP

PL4702
COIL-D15UH-2-GP
68.R1510.20A
1V_CPU_CORE

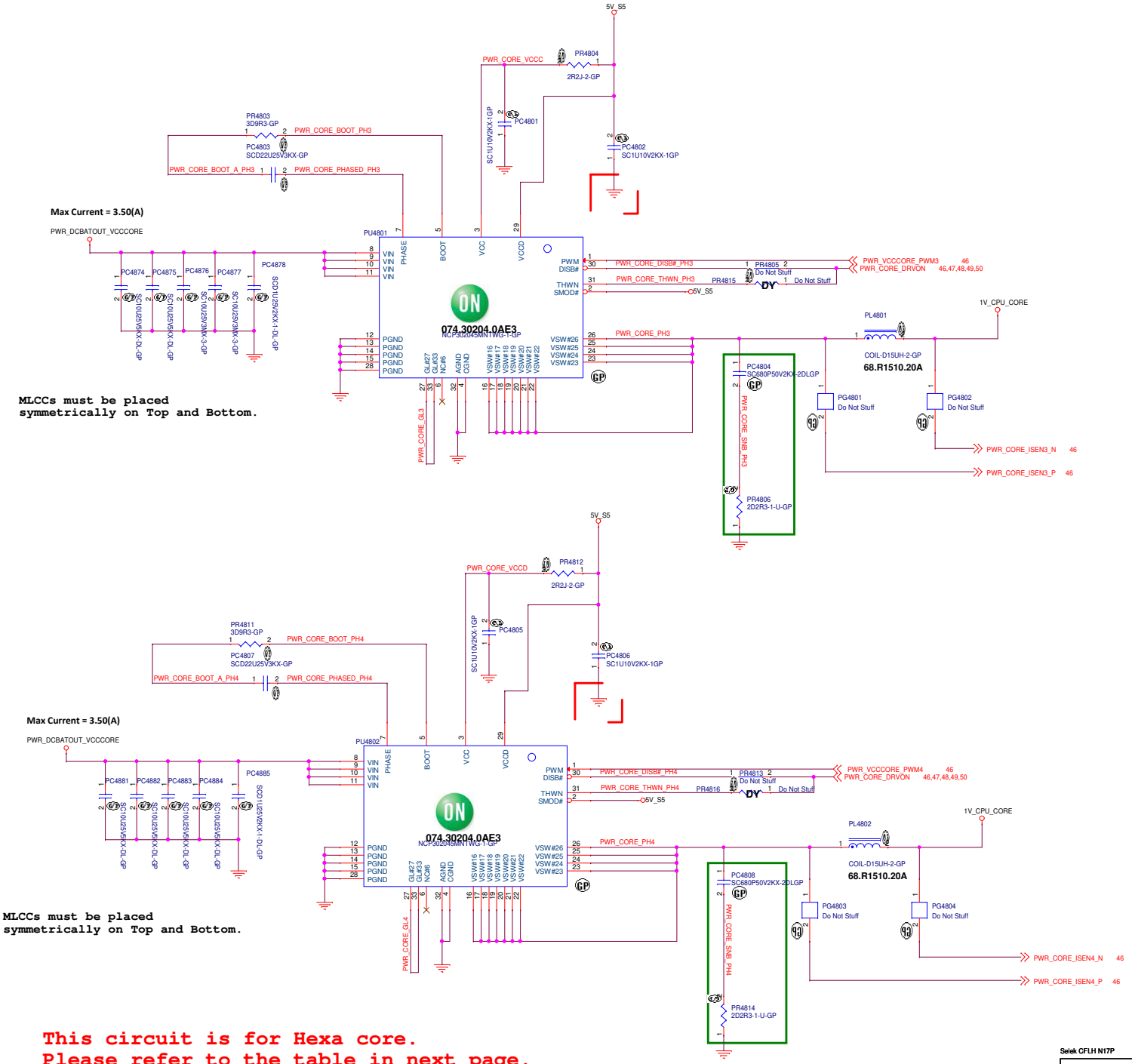
PG4703 Do Not Stuff
PG4704 Do Not Stuff
PWR_CORE_ISEN2_N 46
PWR_CORE_ISEN2_P 46

MLCCs must be placed symmetrically on Top and Bottom.

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCCPUCORE (1/2)
Size: C
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 47 of 105



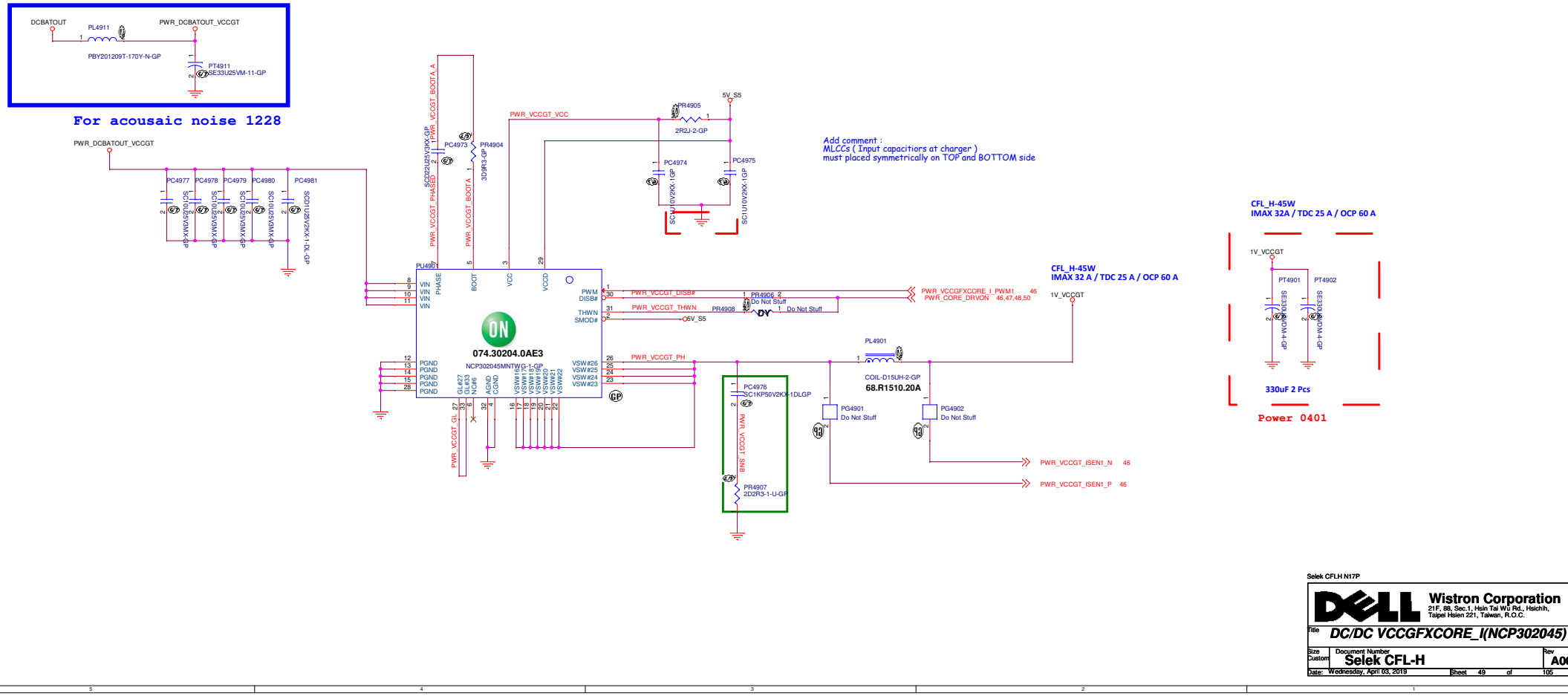
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCCPUCORE (2/2)

Size: C | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 48 of 105

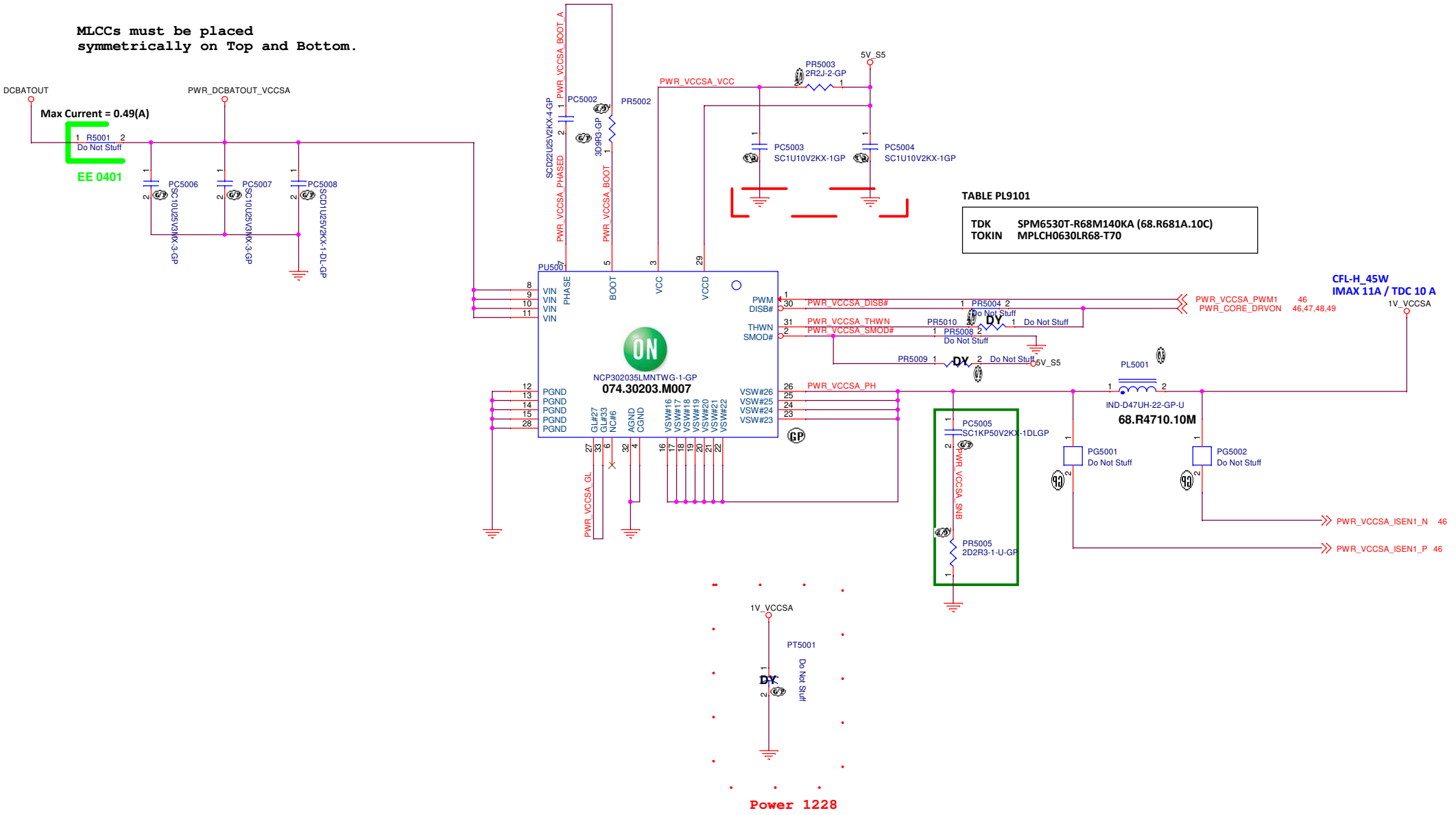


Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC VCCGFXCORE_I(NCP302045)	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 49 of 105	

MLCCs must be placed symmetrically on Top and Bottom.



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCSA(NCP302035)

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 50 of 105

SSID = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

S5

S3

6 DDR_PG_OUT >> DDR_PG_OUT

PH on EE Side

40 PWR_VDDQ_PG <<< PWR_VDDQ_PG

DDR_PG_OUT 1 R5102 2 PWR_VTT_EN
Do Not Stuff

OFFPAGE-GAP

DCBATOUT — PG5101 Do Not Stuff — PWR_DCBATOUT_VDDQ
PG5102 Do Not Stuff
PG5103 Do Not Stuff

1D2V_S3 — PG5105 Do Not Stuff — PWR_VDDQ
PG5106 Do Not Stuff
PG5107 Do Not Stuff
PG5108 Do Not Stuff
PG5109 Do Not Stuff
PG5110 Do Not Stuff
PG5112 Do Not Stuff
PG5114 Do Not Stuff

1D2V_S3 — PG5115 Do Not Stuff — PWR_VDDQ_VLDOIN
PG5116 Do Not Stuff

0D6V_S0 — PG5111 Do Not Stuff — PWR_VDDQ_VTT
PG5113 Do Not Stuff

G5388 For VDDQ/VTT

5V_S5 — PR5101 10R2J-L-GP — PWR_VDDQ_VCC
PC5104 SC1U10V2KX-1DLGP
PR5102 6K49R2F-1-GP
PC5102 DY Do Not Stuff
If 5V has droop Please mount it

PR5108 = 510K
Fs = 400~550KHz

3D3V_S5 — DY — PR5104 Do Not Stuff

PWR_DCBATOUT_VDDQ — PR5108 510KR2F-GP

PU5101 G5388K11U-GP

Pin	Name
10	CS
9	VCC
34	V+
23	V+
22	V+
21	V+
8	PGOOD
7	TON
6	S5
5	S3
28	VLDOIN
30	VTTGND
4	VTTGND
33	VTTGND
29	VTT
31	VTTSNS
26	NC/26
32	GND
1	VTTREF
27	BST
25	LX#25
17	LX#17
18	LX#18
19	LX#19
20	LX#20
35	LX#35
16	PGND
15	PGND
14	PGND
13	PGND
12	PGND
11	PGND
2	VDDQSNS
3	VDDQSET

PWR_VDDQ_PG
PWR_VDDQ_TON
PWR_VDDQ_EN
PWR_VTT_EN
PWR_VDDQ_VLDOIN
PWR_VDDQ_VTT
PWR_VDDQ_VTTREF
PWR_VDDQ_PH
PWR_VDDQ_BOOT
PWR_VDDQ_BOOTA
PWR_VDDQ_BOOTB
PWR_VDDQ_VDDQ
PWR_VDDQ_FB

PC5103 SC1U10V2KX-1DLGP
PC5111 DY — PC5112
Do Not Stuff SC10U6D3V3MX-DL-GP
PC5114 SCD1U25V2KX-1-DL-GP

PWR_DCBATOUT_VDDQ — for PU5101 2nd source: APW8861(074.08861.0043) request DY
PC5108 DY — PC5101 — PC5105
SC10U25V5KX-DL-GP SC10U25V5KX-DL-GP
PD5101 Do Not Stuff
PR5111 Do Not Stuff
PC5110 SCD1U25V2KX-1-DL-GP

Cyntec, 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
PL5101 COIL-1UH-34-GP-U1

TDC : 8A

PWR_VDDQ
PG5104 Do Not Stuff
PC5106 PC5107 PC5109 PC5113 — SC220U6D3VXMX-1DL-GP

R1 PR5105 6K2R2F-GP
R2 PR5106 10K2R2F-GP

PWR_VDDQ_PH — DY PR5110 Do Not Stuff — PWR_VDDQ_SNB
DY PC5115 Do Not Stuff

Vout= 0.75*(1+R1/R2) = 1.2

SSID = PWR.Plane.Regulator_2D5V

OFFPAGE-Signal

5,40,44,92 PM_SLP_S4# >>> PM_SLP_S4#

OFFPAGE-GAP

2D5V_S3 — PG5152 D01R5F-GP — PWR_2D5V

APL5934 For 2D5V

5V_S5 — PC5151 SC1U10V2KX-1DLGP
3D3V_S5 — PR5152 10KR2F-2-GP
3D3V_S5 — PC5155 SC10U6D3V3MX-DL-GP

PG5151 Do Not Stuff — PWR_VDDQ_EN
PM_SLP_S4# — PR5153 Do Not Stuff
PWR_2D5V_PG
PWR_2D5V_EN

PU5151 APL5934KAI-TRG-GP-U

Pin	Name
6	VCNTL
7	POK
8	EN
9	VIN#9
5	VIN#5
4	VOUT#4
3	VOUT#3
2	FB
1	GND

*PWR_2D5V_FB

PR5156 Do Not Stuff
PR5151 Do Not Stuff — PC5156 Do Not Stuff

Design current=700mA
PWR_2D5V
PR5154 28K4R2F-GP — PC5152 Do Not Stuff — PC5153 Do Not Stuff — PC5154 SC10U6D3V3MX-DL-GP

R1
R2 PR5155 13K7R2F-GP

Vout=0.8V*(R1+R2)/R2

Selek CFLH N17P

Wistron Corporation
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Title: Power (G5388_VDDQ_VTT_VPP)
Size: A2 | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 51 of 105

SSID = PWR.Plane.Regulator_1D05V

OFFPAGE-Signal

PH on EE Side

40 PWR_1D05V_PG

53 3V_5V_DSW_OK

53 PWR_1D8V_PG

OFFPAGE-GAP

DCBATOUT

PWR_DCBATOUT_1D05V

PG5201 Do Not Stuff

PG5202 Do Not Stuff

PG5203 Do Not Stuff

1D05V_S5

PWR_1D05V

PG5204 Do Not Stuff

PG5205 Do Not Stuff

PG5206 Do Not Stuff

PG5207 Do Not Stuff

PG5208 Do Not Stuff

PG5209 Do Not Stuff

PG5211 Do Not Stuff

PG5212 Do Not Stuff

PG5213 Do Not Stuff

PG5214 Do Not Stuff

COM \ IC	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 For 1D05V

Cyntec. 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC : 10A

5V_S5

PC5202 SC4D7U25V5KX-DL-GP

PU5201

VCC

IN#7 IN#8 IN#9

TON

PGOOD

EN

PFM#

SS

BST

FB

AGND

PGND

LX#18 LX#17 LX#16 LX#11 LX#10

AOZ2262QI-10-GP-U

PWR_DCBATOUT_1D05V

PC5208 DY Do Not Stuff

PC5209

PC5210

SC10U25V5KX-DL-GP

SC10U25V5KX-DL-GP

PR5201 88K7R2F-

PWR_1D05V_TON

PWR_1D05V_PG

PWR_1D05V_EN

PWR_1D05V_PFM

PWR_1D05V_SS

PC5214 SC1KP50V2KX-1DLGP

PR5203 100KR2F-L3-GP

PC5213 SCD01U50V2KX-1GP

PWR_1D05V_PH

PWR_1D05V_BT

PWR_1D05V_VFB

PL5201

COIL-1UH-34-GP-U1

PC5204 SCD1U25V2KX-1-DL-GP

PG5210 Do Not Stuff

PWR_1D05V_VFB_A

PR5202 3K16R2F-GP

R1

PC5212 Do Not Stuff

PR5204 10KR2F-L1-GP

R2

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

PWR_1D05V

DY

PC5201 PC5203 PC5205 PC5207 PC5206

SC22U6D3V3MX-1-DL-GP

SC22U6D3V3MX-1-DL-GP

SC22U6D3V3MX-1-DL-GP

SC22U6D3V3MX-1-DL-GP Do Not Stuff

3D3V_S5

PR5208 Do Not Stuff DY

PWR_1D05V_PG

3V_5V_DSW_OK R5202 DX Do Not Stuff PWR_1D05V_EN

PWR_1D8V_PG 1 R5205 2 Do Not Stuff

Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ2262_1D05V)

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 52 of 105

Main Func = 1D8V

OFFPAGE

25,52 3V_5V_DSW_OK

PH on EE Side

24,40 PRIM_PWRGD — R5304 1 DY 2 PWR_1D8V_PG — Do Not Stuff

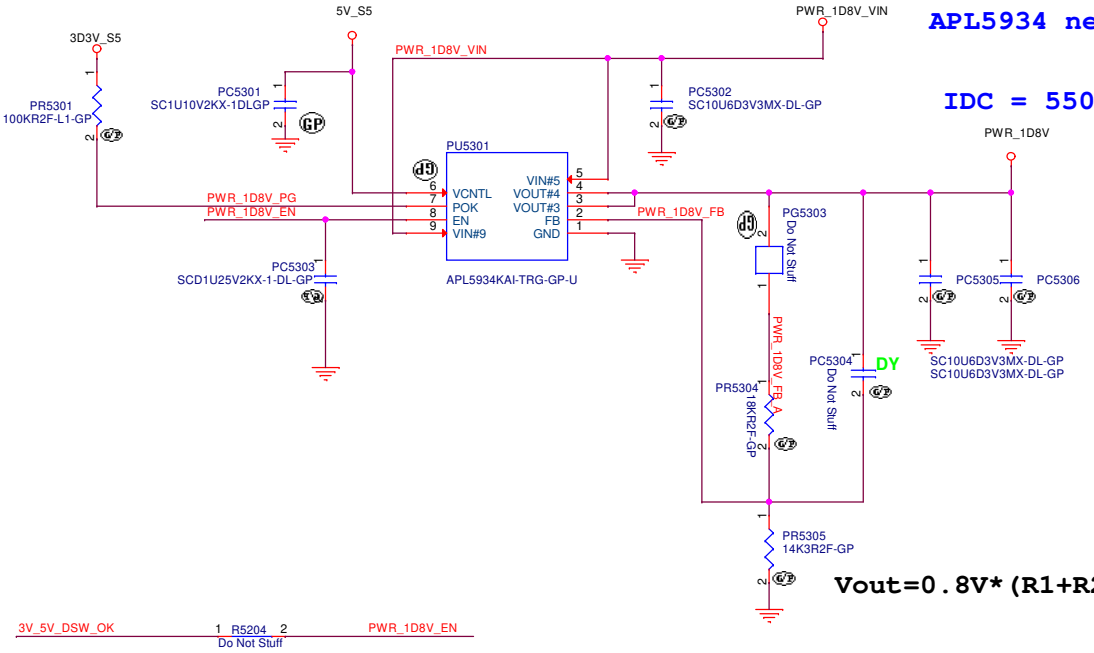
52 PWR_1D8V_PG

OFFPAGE_GAP

3D3V_S5 — PG5302 Do Not Stuff 2 1 — PWR_1D8V_VIN

1D8V_S5 — PG5301 Do Not Stuff 2 1 — PWR_1D8V

APL5934 for 1D8V



APL5934 need <1.8W

IDC = 550mA

Vout=0.8V*(R1+R2)/R2

Selek CFLH N17P

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Title	POWER (APL5934_1D8V)	
Size A3	Document Number Selek CFL-H	Rev A00
Date: Wednesday, April 03, 2019	Sheet of	

NB694 for VCCIO

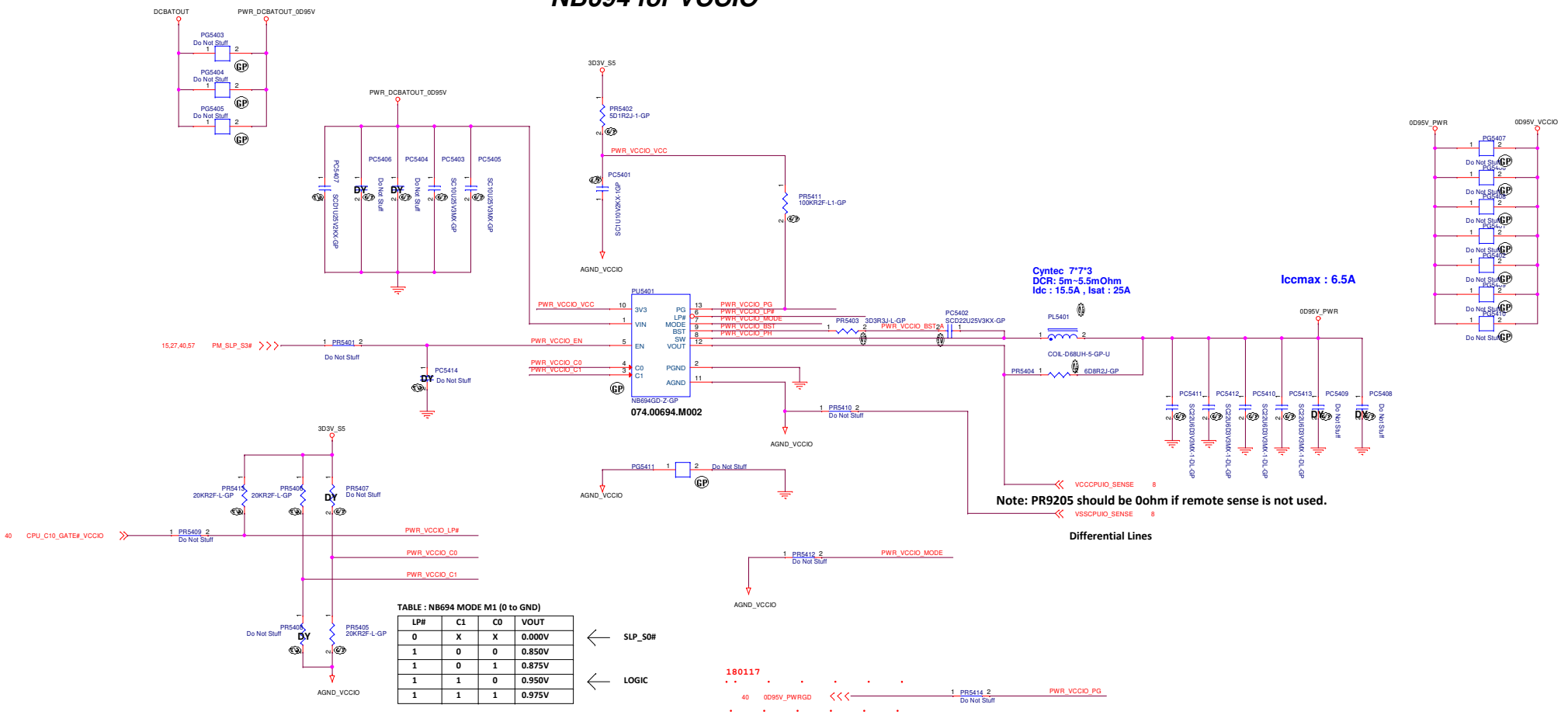

TABLE : NB694 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	
1	0	0	0.850V	SLP_S0#
1	0	1	0.875V	
1	1	0	0.950V	LOGIC
1	1	1	0.975V	

Selek CFLH N17P

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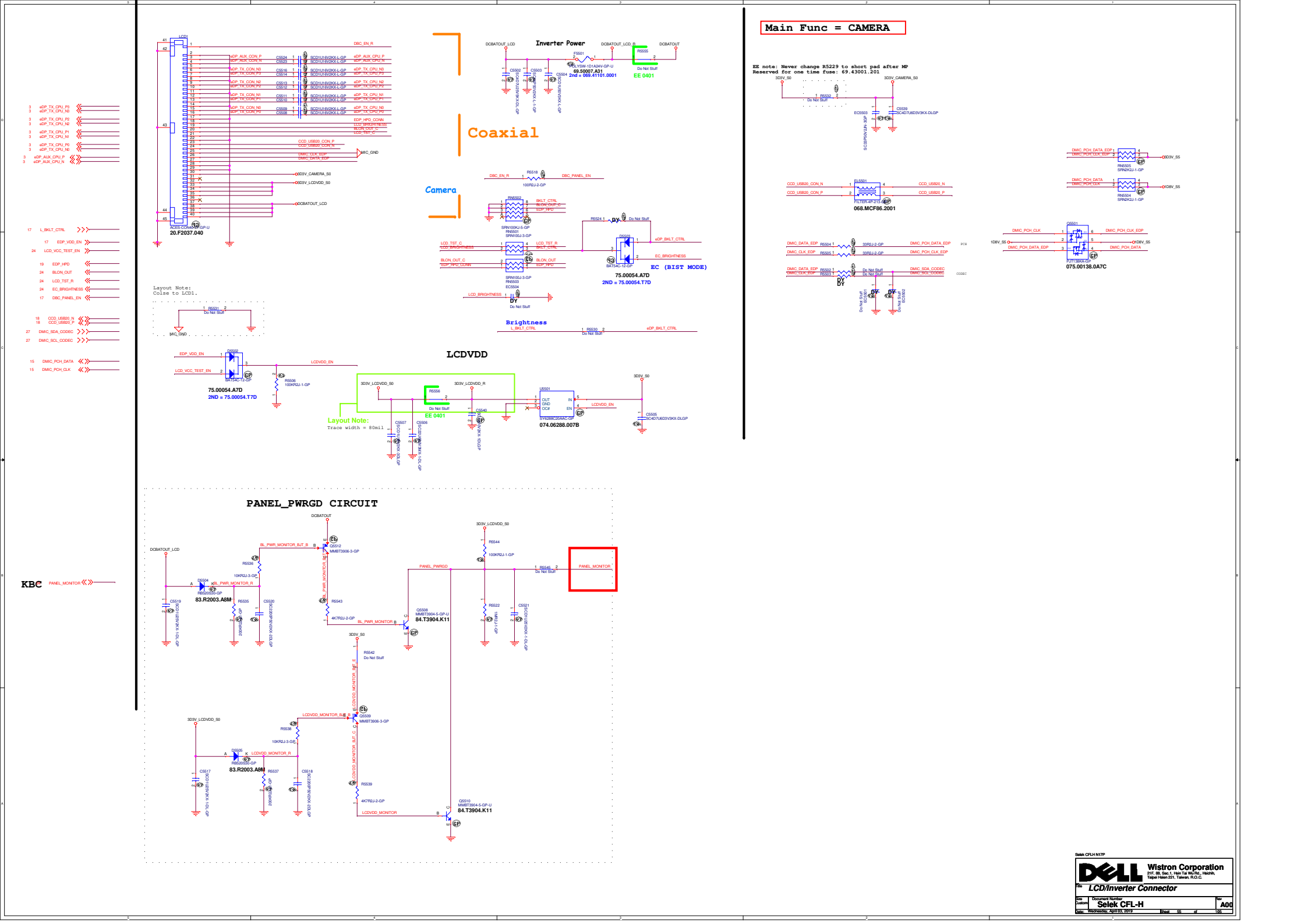
Taipei Hsien 221, Taiwan, R.O.C.

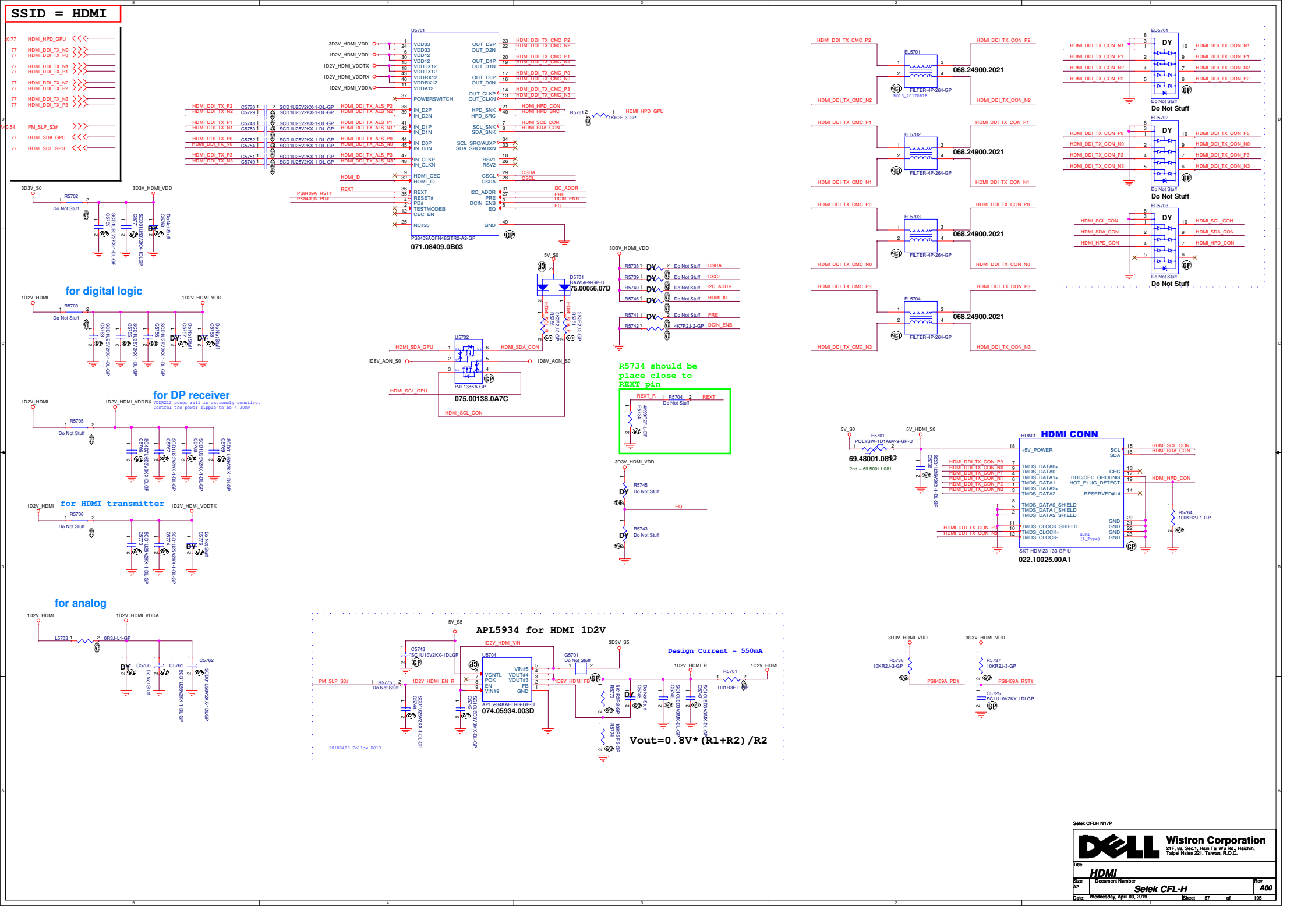
Title: NB964 for 0D95V

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 54 of 105


Main Func = CAMERA
EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201
Coaxial
Camera
Inverter Power
69.50007.A31
2nd = 069.41101.0001
EE 0401
EC (BIST MODE)
75.00054.A7D
2ND = 75.00054.T7D
Brightness
LCDVDD
Layout Note:
Colse to LCD1.
Layout Note:
Trace width = 80mil
074.06288.007B
PANEL_PWRGD CIRCUIT
83.R2003.A8M
84.T3904.K11
068.MCF86.2001
075.00138.0A7C
KBC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD/Inverter Connector
Selek-CFL-H
A00
Wednesday, April 03, 2013

SSID = HDMI


HDMI_HPD_GPU
HDMI_DDI_TX_N0
HDMI_DDI_TX_P0
HDMI_DDI_TX_N1
HDMI_DDI_TX_P1
HDMI_DDI_TX_N2
HDMI_DDI_TX_P2
HDMI_DDI_TX_N3
HDMI_DDI_TX_P3
PM_SLP_S3#
HDMI_SDA_GPU
HDMI_SCL_GPU
U5701
PS8409AQFN48GTR2-A2-GP
071.08409.0B03
3D3V_HDMI_VDD
1D2V_HDMI_VDD
1D2V_HDMI_VDDTX
1D2V_HDMI_VDDRX
1D2V_HDMI_VDDA
POWERSWITCH
HDMI_ID
REXT
PS8409A_RST#
PS8409A_PD#
HDMI_CEC
HDMI_ID
RESET#
PDI#
TESTMODEB
CEC_EN
NC#25
HPD_SNK
HPD_SRC
SCL_SNK
SDA_SNK
SCL_SRC/AUXP
SDA_SRC/AUXN
RSV1
RSV2
CSCL
CSDA
I2C_ADDR
PRE
DCIN_ENB
EQ
GND
HDMI_HPD_CON
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_GPU
1KR2F-3-GP
for digital logic
for DP receiver
VDDRX12 power rail is extremely senstive.
Control the power ripple to be < 30mV
for HDMI transmitter
for analog
5V_S0
D5701
BAW56-9-GP-U
075.00056.07D
U5702
PJT138KA-GP
075.00138.0A7C
R5734 should be
place close to
REXT pin
EL5701
EL5702
EL5703
EL5704
FILTER-4P-264-GP
068.24900.2021
ED5701
ED5702
ED5703
Do Not Stuff
F5701
POLYSW-1D1A6V-9-GP-U
69.48001.089
2nd = 69.50011.081
HDMI1
HDMI CONN
SKT-HDMI23-133-GP-U
022.10025.00A1
APL5934 for HDMI 1D2V
APL5934KAI-TRG-GP-U
074.05934.003D
Design Current = 550mA
Vout=0.8V*(R1+R2)/R2
20180409 Follow RO13
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI
Size
A2
Document Number
Selek CFL-H
Rev
A00
Date:
Wednesday, April 03, 2019
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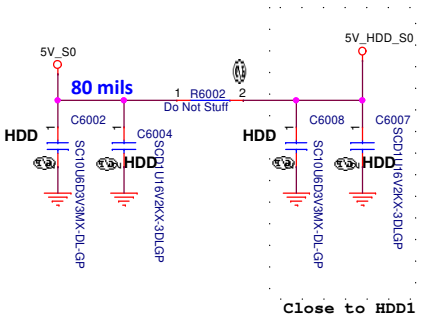
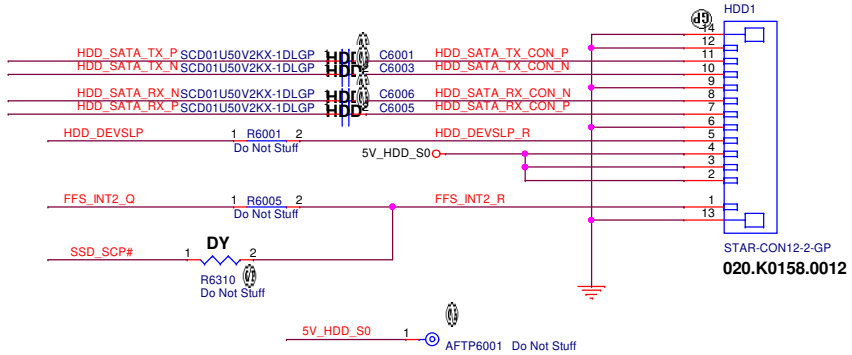
Main Func = HDD

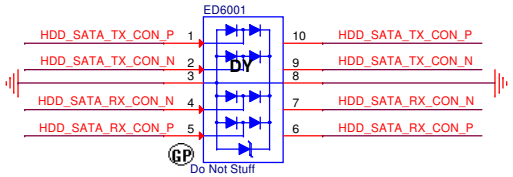
SATA HDD Connector

17 HDD_SATA_TX_P
17 HDD_SATA_TX_N
17 HDD_SATA_RX_N
17 HDD_SATA_RX_P
19 HDD_DEVSLP
70 FFS_INT2_Q
24,63 SSD_SCP#





Layout Note:
Place near HDD1



Do Not Stuff
2nd = 75.01045.073

Table 16-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

Notes:
1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Use a non-interleaved breakout to isolate Tx and Rx.

Selek CFLH N17P

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Title: SATA HDD
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
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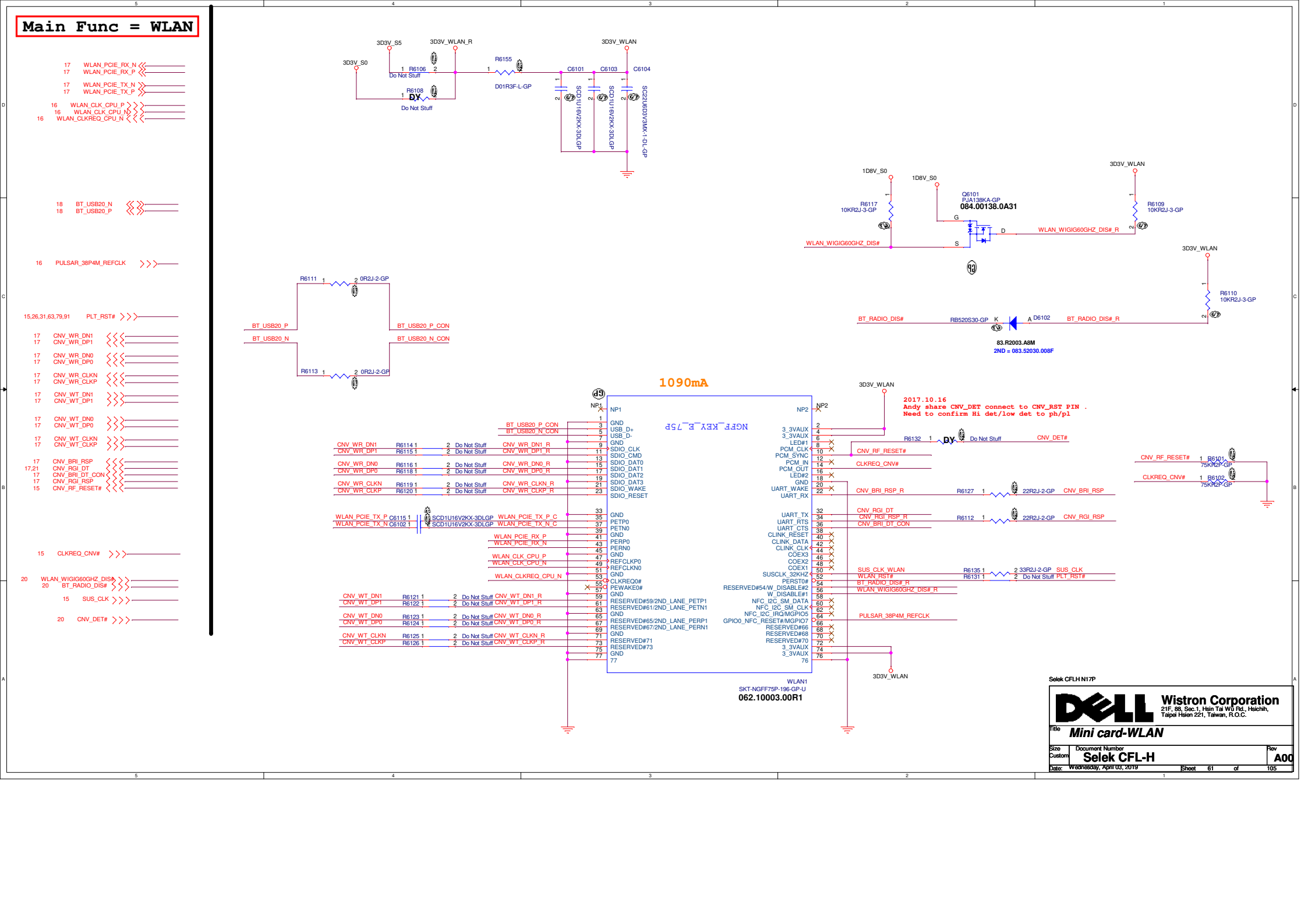
Main Func = WLAN



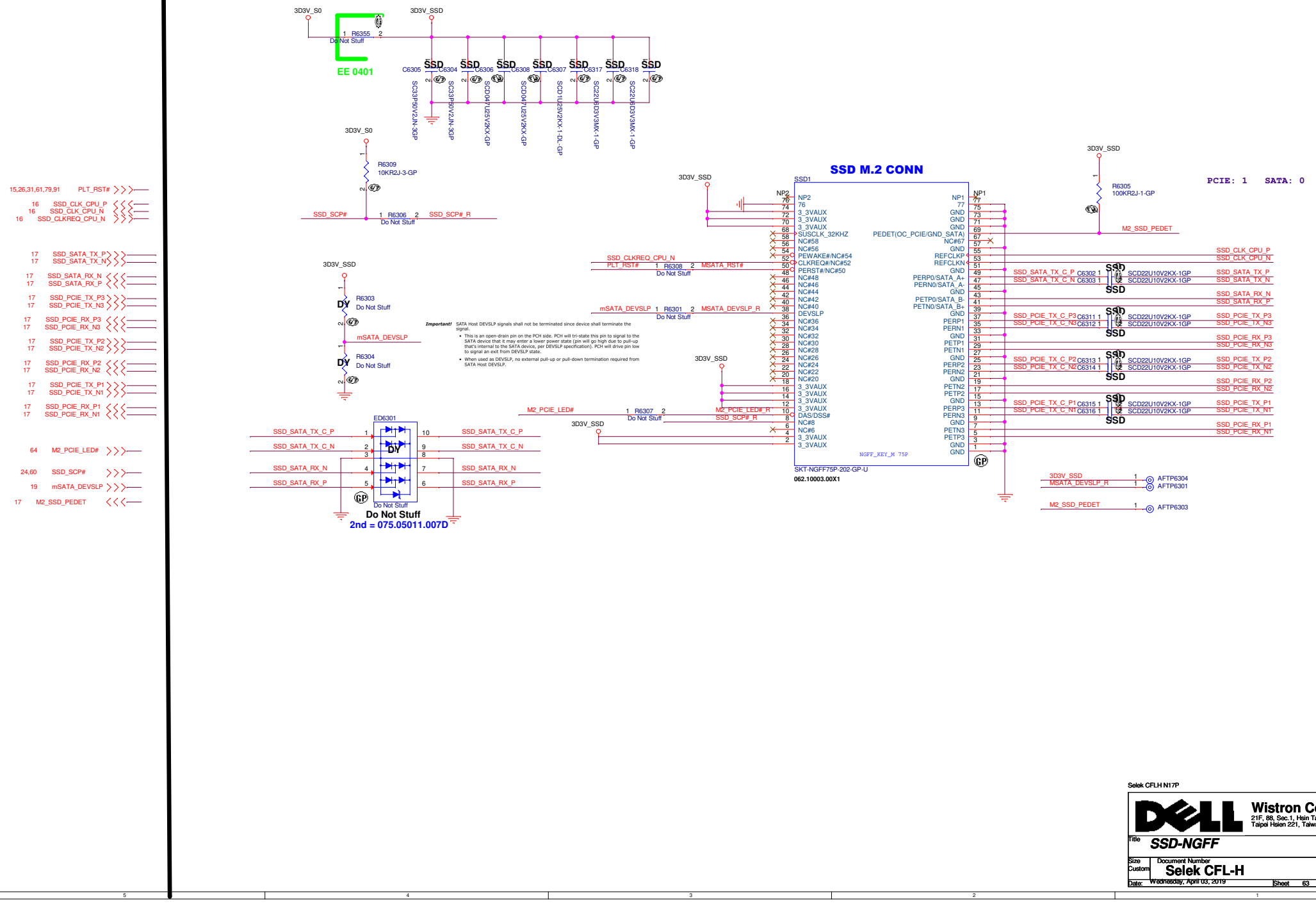
Selek CFLH N17P

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Mini card-WLAN*	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 61 of 105	

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



15,26,31,61,79,91 PLT_RST#
16 SSD_CLK_CPU_P
16 SSD_CLK_CPU_N
16 SSD_CLKREQ_CPU_N
17 SSD_SATA_TX_P
17 SSD_SATA_TX_N
17 SSD_SATA_RX_N
17 SSD_SATA_RX_P
17 SSD_PCIE_TX_P3
17 SSD_PCIE_TX_N3
17 SSD_PCIE_RX_P3
17 SSD_PCIE_RX_N3
17 SSD_PCIE_TX_P2
17 SSD_PCIE_TX_N2
17 SSD_PCIE_RX_P2
17 SSD_PCIE_RX_N2
17 SSD_PCIE_TX_P1
17 SSD_PCIE_TX_N1
17 SSD_PCIE_RX_P1
17 SSD_PCIE_RX_N1
64 M2_PCIE_LED#
24,60 SSD_SCP#
19 mSATA_DEVSLP
17 M2_SSD_PEDET

Selek CFLH N17P

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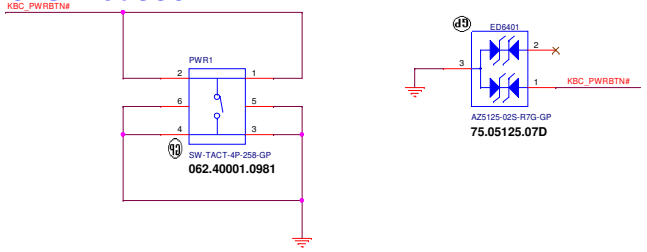
Taipei Hsien 221, Taiwan, R.O.C.

Title: SSD-NGFF		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 63 of 105	

SSID = User.Interface

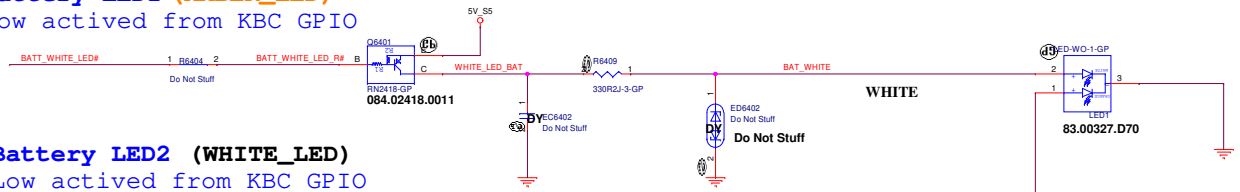
Power button

NONE FINGER PRINT 才會上件



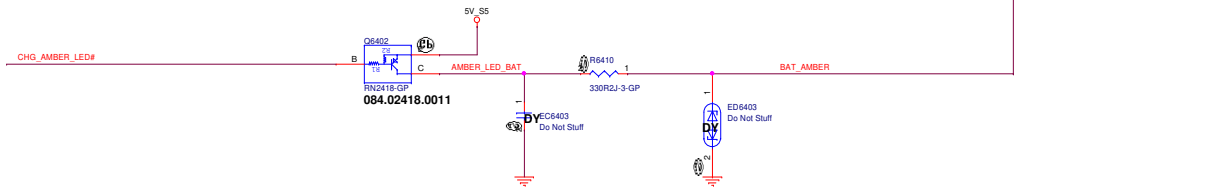
Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

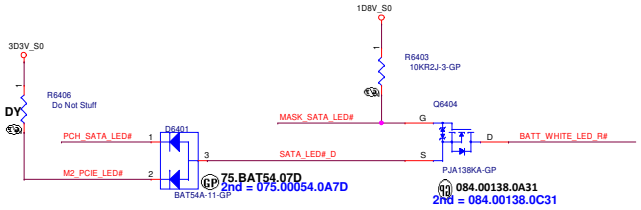


Battery LED2 (WHITE_LED)

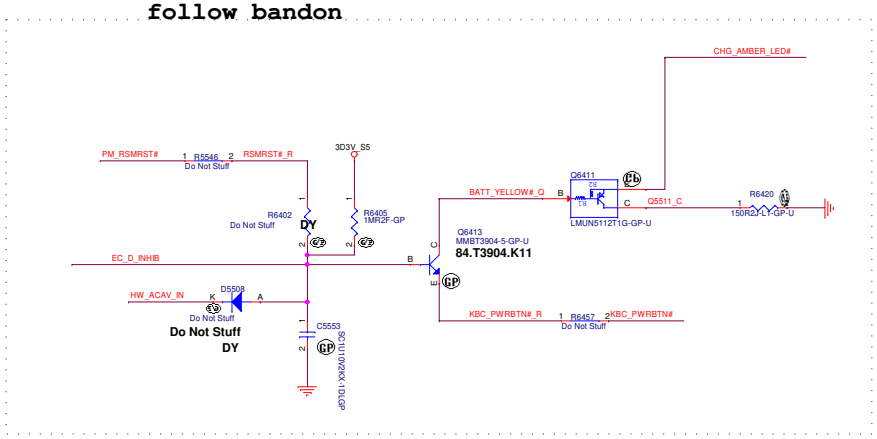
Low actived from KBC GPIO



SATA LED



M-BIST for G10 (Proposed schematic) follow bandon



KBC

- 24 EC_D_INHIB
- 24,64 CHG_AMBER_LED#
- 24,64,92 KBC_PWRBTN#
- 15 PM_RSMRST#
- 24,44 HW_ACAV_IN
- 24 MASK_SATA_LED#
- 63 M2_PCIE_LED#
- 17 PCH_SATA_LED#
- 24 BATT_WHITE_LED#
- 24,64 CHG_AMBER_LED#
- 8,92 LID_CL_SIO#
- 4,92 KBC_PWRBTN#

Selek CFLH N17P

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Light Bar/Power Button

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 64 of 105

Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

5V_S0 → F6502 POLYSW-1DI-A8V-9-GP → +5V_KB_BL

69.48001.081
2nd = 69.50011.081
KBBL

Q6501 SCZ01UB5VAX-1-DL-GP — KBBL

X01 20161228 change

+5V_KB_BL, KB_LED_DET_C, KB_BL_CTRL# → KBBL1 STM-CONN-2-GP 020.K0311.0004

D6502 BAT54S, D6503 BAT54S

24 KSI[0..7]
24 KSO[0..16]

20 KB_DET# → AFTP6542–AFTP6566 (KSI7–KSI0, KSO25–KSO0, CAP_LED) → KB1 STAR-CON30-2-GP 20.K0750.030

CAP_LED → AFTP6541

KB_BL_CTRL# → Q6501 AO3418L-GP 84.03418.A31

24 KB_LED_PWM → R6509 Do Not Stuff

17 KB_BL_DET → R6507 KBBL 51KR2J-1-GP → KB_LED_DET_C

KBBL R6508 109KR2J-1-GP, C6504 Do Not Stuff

+5V_KB_BL → AFTP6529
KB_BL_CTRL# → AFTP6530

X01 20170105 change

CAP LED Control
LOW actived from KBC GPIO

X02 0414

24 CAP_LED#_R → R6512 Do Not Stuff → CAP_LED_R# → Q6505 RN2418-GP 084.02418.0011 (5V_S5, CAP_LED_Q) → R6513 1KR2J-1-GP → CAP_LED

CAP_LED_Q → EC6507 Do Not Stuff

Main Func = TPAD

3D3V_S0 → R6502 NON TP_WAKE → TP_VDD
3D3V_S5 → R6514 Do Not Stuff → TP_WAKE

GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

EC I2C
I2C

24 DAT_TP_SIO_I2C_CLK, 24 CLK_TP_SIO_I2C_DAT → R6515, R6516 Do Not Stuff → I2C0_SCL_R, I2C0_SDA_R
20,66 CPU_I2C_SCL_P1, 20,66 CPU_I2C_SDA_P1 → R6505, R6506 Do Not Stuff → I2C0_SCL_R, I2C0_SDA_R

TP_VDD → RN6501 Do Not Stuff
EC6501 Do Not Stuff

NON TP_WAKE
NON TP_WAKE

TP_VDD → RN6503 SRN2K2J-1-GP

TP_VDD → C6505 0.1S,24 → SCZ01UB5VAX-1-DL-GP

I2C0_SCL_R, I2C0_SDA_R → TP_WAKE_KBC#, PTP_DISB → TP1 PTMO-CON8-16-GP 020.K0255.0008

AFTP6540

Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low
~~and check if there is PU~~ on TPAD side.

X02 0415

TP_VDD → R6511 10KR2J-3-GP → TP_WAKE_KBC#

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

TP_VDD → AFTP6531
I2C0_SCL_R → AFTP6534
I2C0_SDA_R → AFTP6535
TP_WAKE_KBC# → AFTP6536
PTP_DISB → AFTP6537

Selek CFLH NI 7P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: Key Board&Touch Pad

Size	Document Number	Rev
Custom	Selek CFL-H	A00

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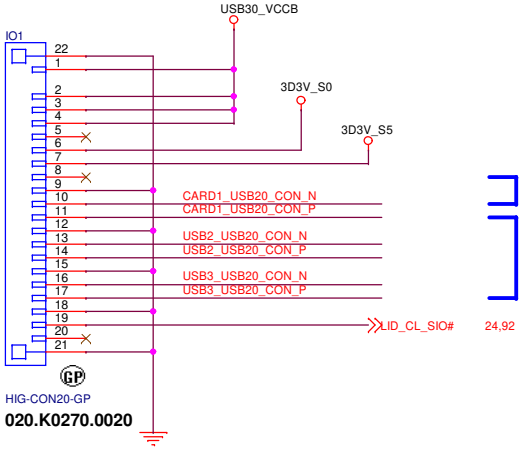
18 USB3_USB20_P
18 USB3_USB20_N
18 USB2_USB20_P
18 USB2_USB20_N

18 CARD1_USB20_N
18 CARD1_USB20_P

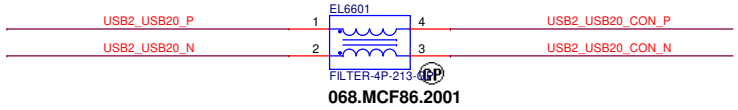
20,65 CPU_I2C_SCL_P1
20,65 CPU_I2C_SDA_P1

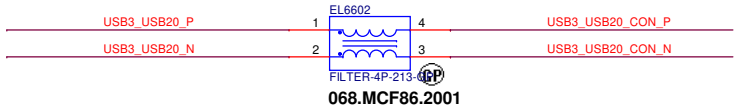
44 BT_PWR_IN-
44 BT_PWR_IN+

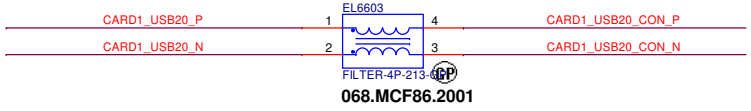


Cardreader

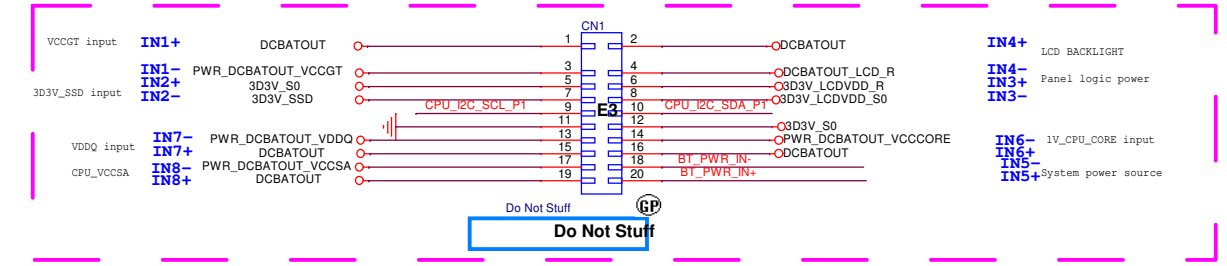
USB 2.0 Gen1 *2







E3 reserve



Do Not Stuff

Selek CFLH N17P

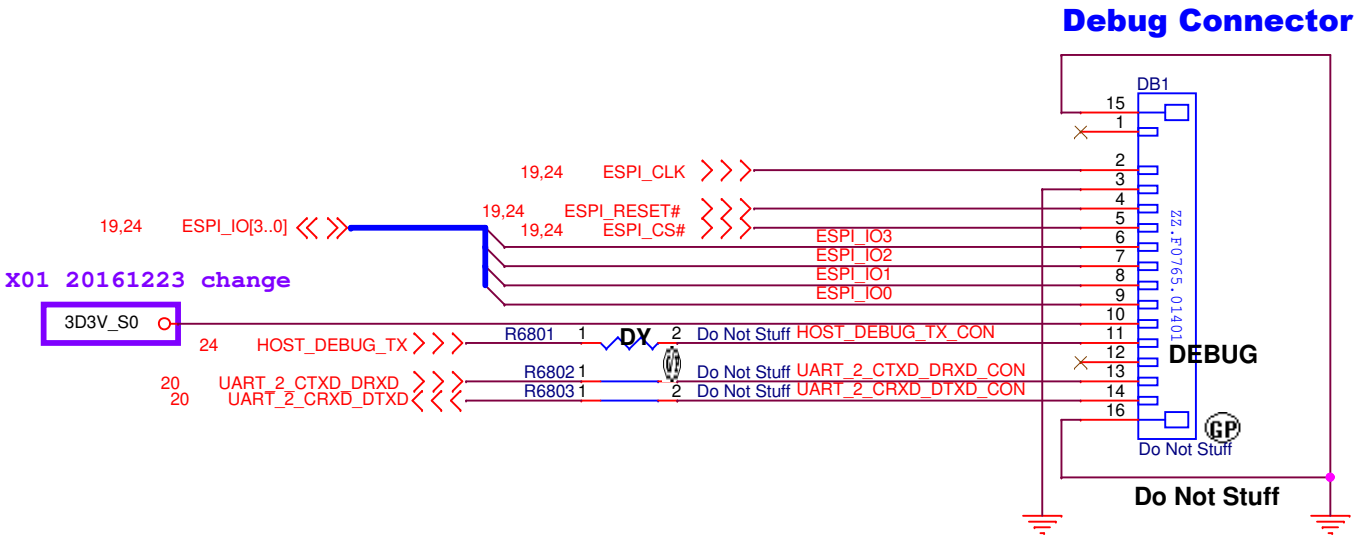
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 66 of 105

Main Func = Debug



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

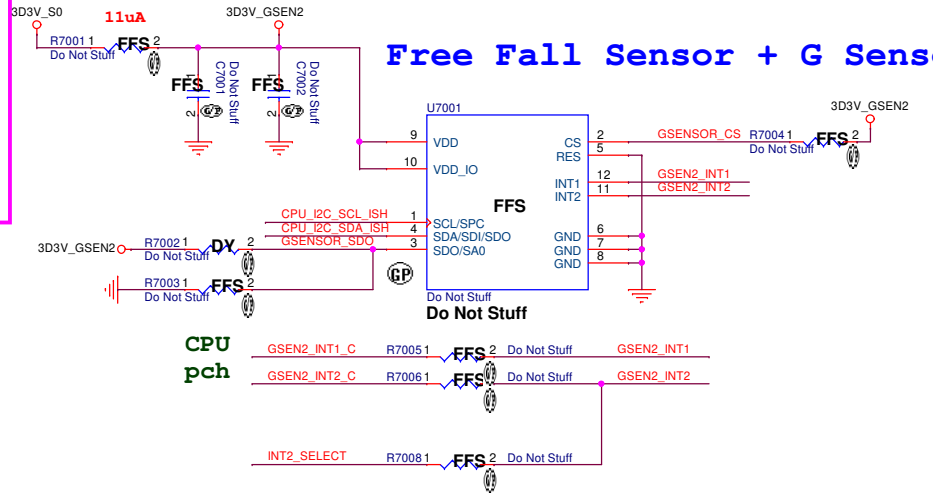
Title: *Dubug connector*		
Size: A4	Document Number: **Selek CFL-H**	Rev: **A00**
Date: Wednesday, April 03, 2019	Sheet 68 of 105	

SSID = Free Fall Sensor

20 GSEN2_INT1_C
20 GSEN2_INT2_C
20 CPU_I2C_SDA_ISH
20 CPU_I2C_SCL_ISH
60 FFS_INT2_Q

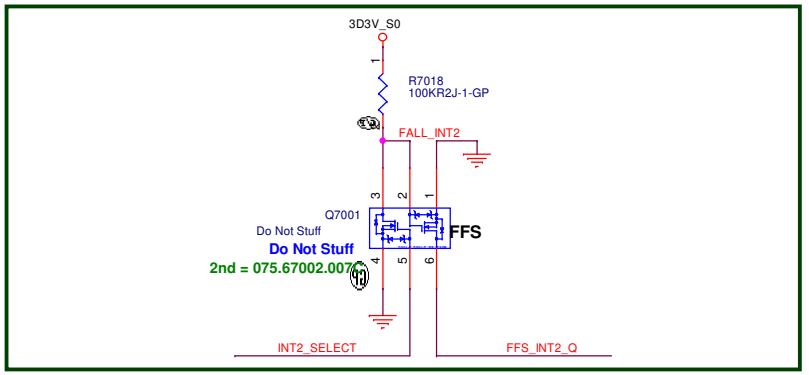
20180726 need DELL GPIO table

Free Fall Sensor + G Sensor



CPU pch

Please help to close with U6602



Selek CFLH N17P

Wistron Corporation
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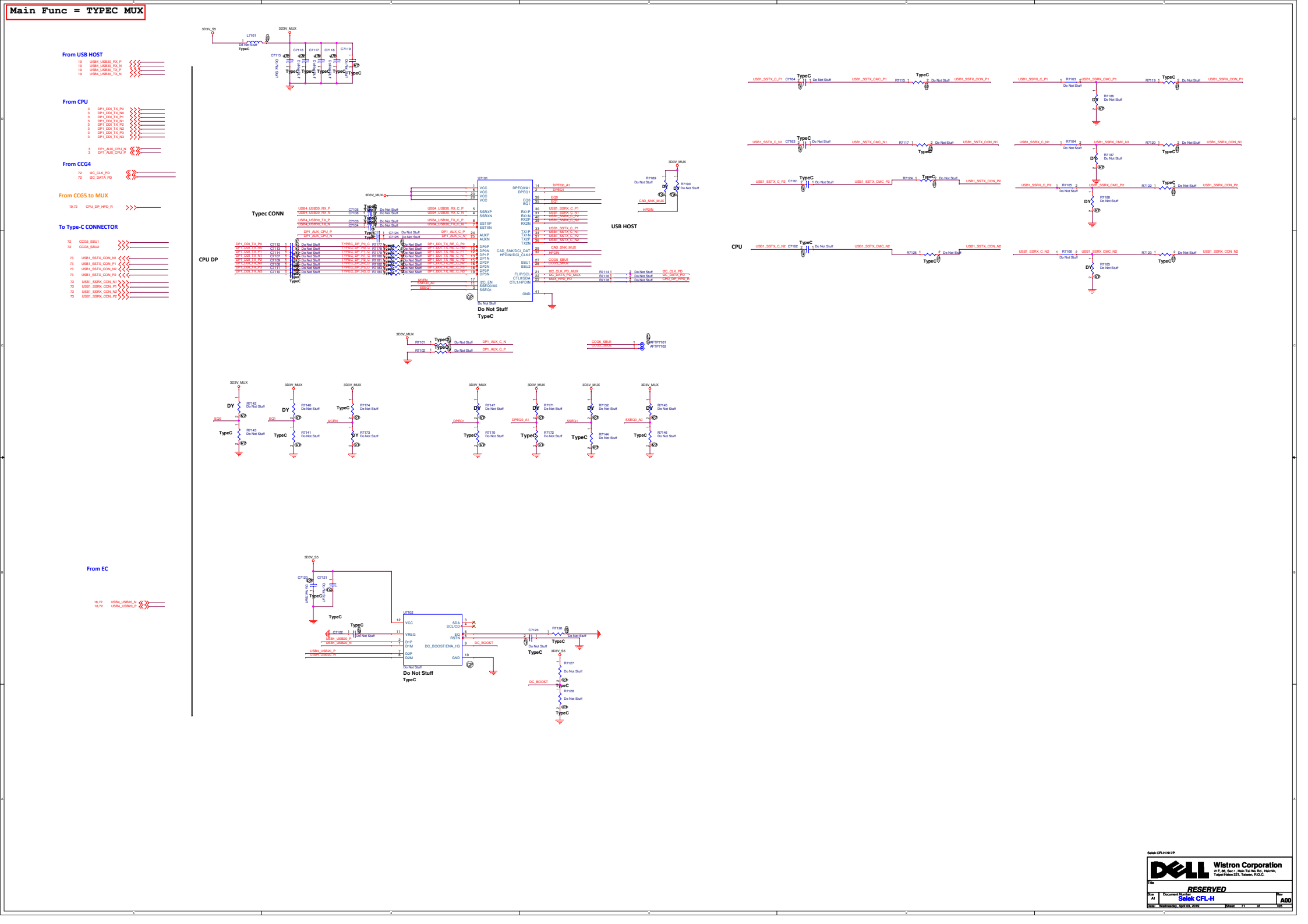
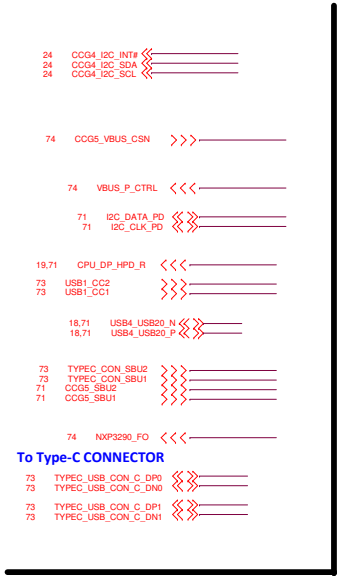
Taipei Hsien 221, Taiwan, R.O.C.

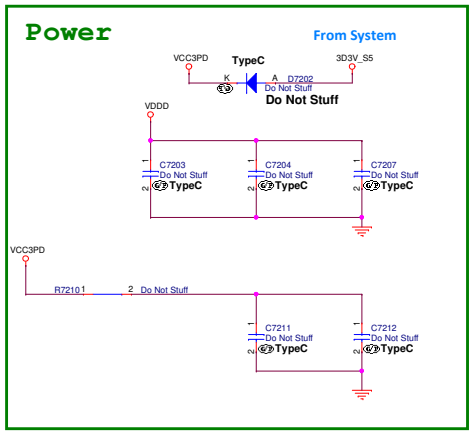
Title: (Reserved)
Size: A3
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 70 of 105

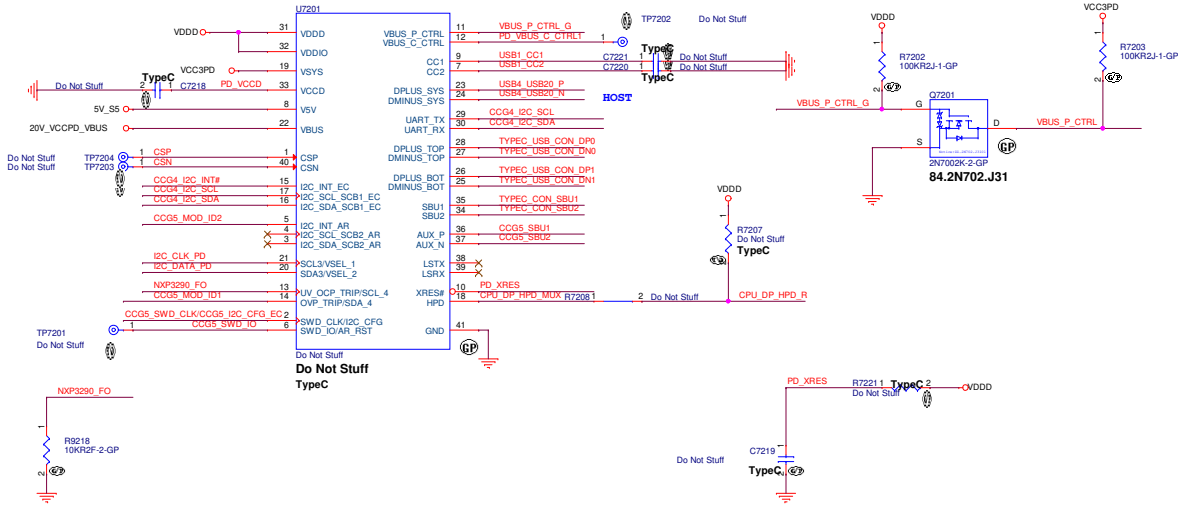
Main Func = TYPEC MUX

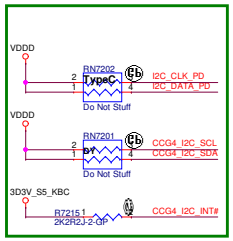


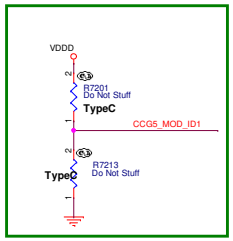
Main Func = TYPEC CONTROLLER

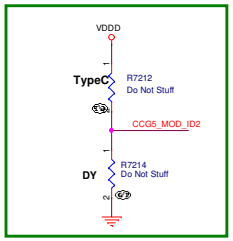


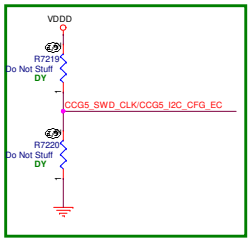


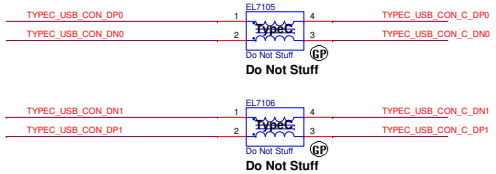












Selek CFLH N17P

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0 PORT**

Size	Document Number	Rev
Custom	Selek CFL-H	A00

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Main Func = TYPEC CONNECTOR

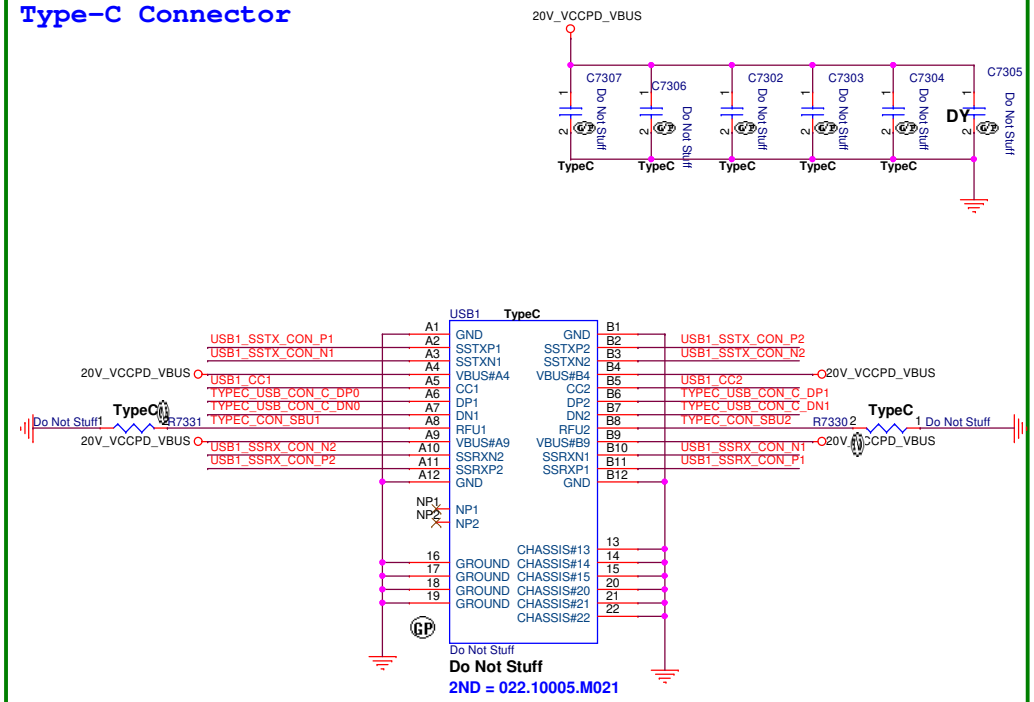
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2

72 TYPEC_CON_SBU1
72 TYPEC_CON_SBU2
72 USB1_CC1
72 USB1_CC2

From USB2.0/ I2C Mux

72 TYPEC_USB_CON_C_DP0
72 TYPEC_USB_CON_C_DN0
72 TYPEC_USB_CON_C_DP1
72 TYPEC_USB_CON_C_DN1

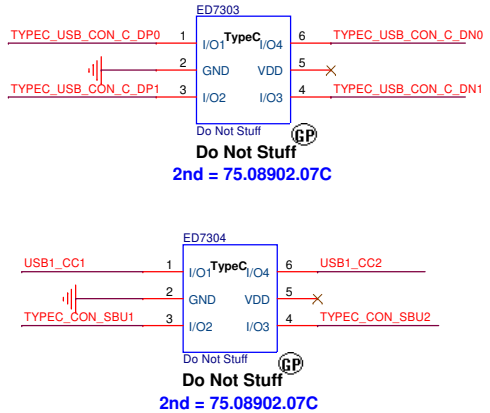
Type-C Connector



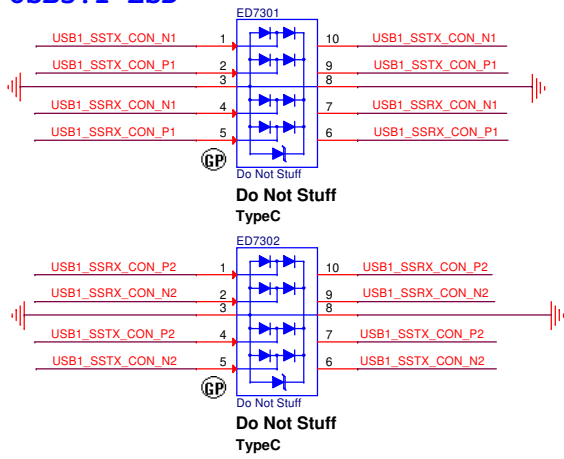
20V_VCCPD_VBUS 1 AFTP7301 Do Not Stuff

USB1_CC1 1 AFTP7303 Do Not Stuff
USB1_CC2 1 AFTP7304 Do Not Stuff

EMI



USB3.1 ESD



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

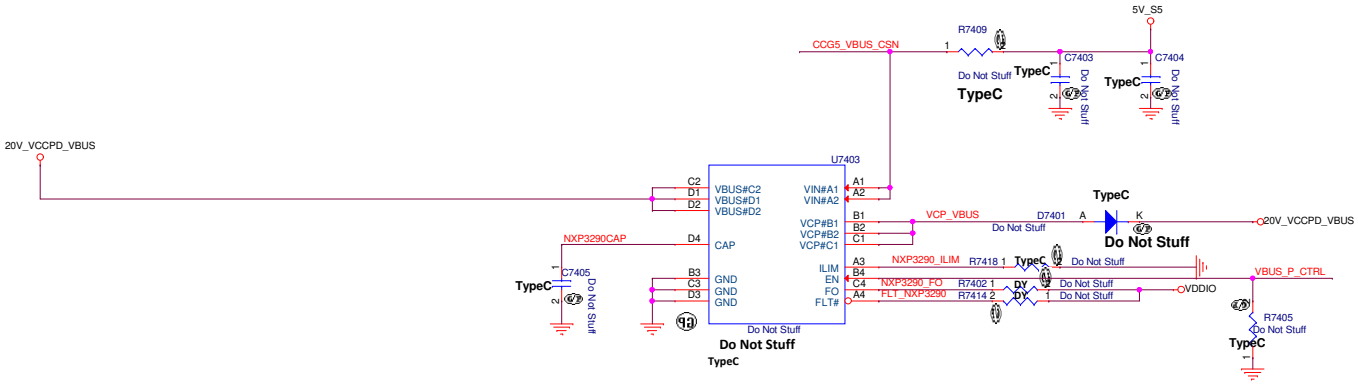
Title: TYPEC CONN		
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 73 of 105	

Main Func = LPS

72 VBUS_P_CTRL

72 NXP3290_FO

72 CCG5_VBUS_CSN



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPS

Size	Document Number	Rev
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- PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
PEX_DVDD Supply Rail					
GB4C-128, GB4D-128	1.0 µF[1]	X6S 0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S 0201W	12	0	Under GPU
	4.7 µF	X6S 0603	0	2	Near GPU
	4.7 µF	X6S 0603	3	0	Under GPU
	10 µF	X5R 0805	0	1	Midway between GPU and power supply
	10 µF	X6S 0805	3	0	Near GPU
	22 µF	X5R 0805	0	1	Midway between GPU and power supply
	22 µF	X6S 0805	2	0	Near GPU

PEX_HVDD Supply Rail					
GB4C-128, GB4D-128	1.0 µF	X6S 0402 or 0201W	0	4	Under GPU
	0.47 µF	X6S 0201W	13	0	Under GPU
	4.7 µF	X6S 0603	0	2	Near GPU
	4.7 µF	X6S 0603	3	0	Under GPU
	10 µF	X5R 0805	0	2	Midway between GPU and power supply
	10 µF	X6S 0805	3	0	Near GPU
	22 µF	X5R 0805	0	1	Midway between GPU and power supply
	22 µF	X6S 0805	2	0	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

EMI Reserved

VGA_RST#

EC7601 10n Do Not Stuff

15,24,86 DGPU_PWROK
16 CLK_PCIE_PEG_REQ#
79 VGA_RST#
16 GFX_CLK_CPU_P
16 GFX_CLK_CPU_N

3 GFX_PCIE_RX_P7 / 3 GFX_PCIE_RX_N7
3 GFX_PCIE_RX_P6 / 3 GFX_PCIE_RX_N6
3 GFX_PCIE_RX_P5 / 3 GFX_PCIE_RX_N5
3 GFX_PCIE_RX_P4 / 3 GFX_PCIE_RX_N4
3 GFX_PCIE_RX_P3 / 3 GFX_PCIE_RX_N3
3 GFX_PCIE_RX_P2 / 3 GFX_PCIE_RX_N2
3 GFX_PCIE_RX_P1 / 3 GFX_PCIE_RX_N1
3 GFX_PCIE_RX_P0 / 3 GFX_PCIE_RX_N0

3 GFX_PCIE_TX_CON_P7 / 3 GFX_PCIE_TX_CON_N7
3 GFX_PCIE_TX_CON_P6 / 3 GFX_PCIE_TX_CON_N6
3 GFX_PCIE_TX_CON_P5 / 3 GFX_PCIE_TX_CON_N5
3 GFX_PCIE_TX_CON_P4 / 3 GFX_PCIE_TX_CON_N4
3 GFX_PCIE_TX_CON_P3 / 3 GFX_PCIE_TX_CON_N3
3 GFX_PCIE_TX_CON_P2 / 3 GFX_PCIE_TX_CON_N2
3 GFX_PCIE_TX_CON_P1 / 3 GFX_PCIE_TX_CON_N1
3 GFX_PCIE_TX_CON_P0 / 3 GFX_PCIE_TX_CON_N0

1D8V_AON_S0
R7604 10KR2J-L-GP
DGPU_PWROK
CLK_PCIE_PEG_REQ#
Q7601 PJA138KA-GP 084.00138.0A31
MAX Vth=1V
VGA_RST#
PEG_CLKREQ_dGPU#
GFX_CLK_CPU_P
GFX_CLK_CPU_N

GPU1A 1 OF 17

AJ11	PEX_WAKE#		
AJ12	PEX_RST*		
AK12	PEX_CLKREQ#		
AL13	PEX_REFCLK		
AK13	PEX_REFCLK*		
AK14	PEX_TX0	GFX_PCIE_RX_P0 / GFX_PCIE_RX_N0	GFX_PCIE_RX_CON_P0 / GFX_PCIE_RX_CON_N0
AJ14	PEX_TX0*		
AN12	PEX_RX0	GFX_PCIE_TX_CON_P0 / GFX_PCIE_TX_CON_N0	
AM12	PEX_RX0*		
AH14	PEX_TX1	GFX_PCIE_RX_P1 / GFX_PCIE_RX_N1	GFX_PCIE_RX_CON_P1 / GFX_PCIE_RX_CON_N1
AG14	PEX_TX1*		
AN14	PEX_RX1	GFX_PCIE_TX_CON_P1 / GFX_PCIE_TX_CON_N1	
AM14	PEX_RX1*		
AK15	PEX_TX2	GFX_PCIE_RX_P2 / GFX_PCIE_RX_N2	GFX_PCIE_RX_CON_P2 / GFX_PCIE_RX_CON_N2
AJ15	PEX_TX2*		
AP14	PEX_RX2	GFX_PCIE_TX_CON_P2 / GFX_PCIE_TX_CON_N2	
AP15	PEX_RX2*		
AL16	PEX_TX3	GFX_PCIE_RX_P3 / GFX_PCIE_RX_N3	GFX_PCIE_RX_CON_P3 / GFX_PCIE_RX_CON_N3
AK16	PEX_TX3*		
AN15	PEX_RX3	GFX_PCIE_TX_CON_P3 / GFX_PCIE_TX_CON_N3	
AM15	PEX_RX3*		
AK17	PEX_TX4	GFX_PCIE_RX_P4 / GFX_PCIE_RX_N4	GFX_PCIE_RX_CON_P4 / GFX_PCIE_RX_CON_N4
AJ17	PEX_TX4*		
AN17	PEX_RX4	GFX_PCIE_TX_CON_P4 / GFX_PCIE_TX_CON_N4	
AM17	PEX_RX4*		
AH17	PEX_TX5	GFX_PCIE_RX_P5 / GFX_PCIE_RX_N5	GFX_PCIE_RX_CON_P5 / GFX_PCIE_RX_CON_N5
AG17	PEX_TX5*		
AP17	PEX_RX5	GFX_PCIE_TX_CON_P5 / GFX_PCIE_TX_CON_N5	
AP18	PEX_RX5*		
AK18	PEX_TX6	GFX_PCIE_RX_P6 / GFX_PCIE_RX_N6	GFX_PCIE_RX_CON_P6 / GFX_PCIE_RX_CON_N6
AJ18	PEX_TX6*		
AN18	PEX_RX6	GFX_PCIE_TX_CON_P6 / GFX_PCIE_TX_CON_N6	
AM18	PEX_RX6*		
AL19	PEX_TX7	GFX_PCIE_RX_P7 / GFX_PCIE_RX_N7	GFX_PCIE_RX_CON_P7 / GFX_PCIE_RX_CON_N7
AK19	PEX_TX7*		
AN20	PEX_RX7	GFX_PCIE_TX_CON_P7 / GFX_PCIE_TX_CON_N7	
AM20	PEX_RX7*		
AK20	PEX_TX8		
AJ20	PEX_TX8*		
AP20	PEX_RX8		
AP21	PEX_RX8*		
AH20	PEX_TX9		
AG20	PEX_TX9*		
AN21	PEX_RX9		
AM21	PEX_RX9*		
AK21	PEX_TX10		
AJ21	PEX_TX10*		
AN23	PEX_RX10		
AM23	PEX_RX10*		
AL22	PEX_TX11		
AK22	PEX_TX11*		
AP23	PEX_RX11		
AP24	PEX_RX11*		
AK23	PEX_TX12		
AJ23	PEX_TX12*		
AN24	PEX_RX12		
AM24	PEX_RX12*		
AH23	PEX_TX13		
AG23	PEX_TX13*		
AN26	PEX_RX13		
AM26	PEX_RX13*		
AK24	PEX_TX14		
AJ24	PEX_TX14*		
AP26	PEX_RX14		
AP27	PEX_RX14*		
AL25	PEX_TX15		
AK25	PEX_TX15*		
AN27	PEX_RX15		
AM27	PEX_RX15*		

Do Not Stuff

PCIE/PLL DIGITAL PWR 1V Interface

PEX_DVDD_1	AG21
PEX_DVDD_2	AG22
PEX_DVDD_3	AG24
PEX_DVDD_4	AH25
PEX_CVDD_1	AG19
PEX_CVDD_2	AH21

PCIE/PLL ANALOG PWR 1.8V Interface

PEX_HVDD_1	AG13
PEX_HVDD_2	AG15
PEX_HVDD_3	AG16
PEX_HVDD_4	AG18
PEX_HVDD_5	AG25
PEX_HVDD_6	AH15
PEX_HVDD_7	AH18
PEX_HVDD_8	AH26
PEX_HVDD_9	AH27
PEX_HVDD_10	AJ27
PEX_HVDD_11	AL27
PEX_HVDD_12	AM28
PEX_HVDD_13	AN28
PEX_HVDD_14	
PEX_PLL_HVDD	AH12
PEX_TERMP	AP29

R7607 Close to GPU
PEX_TERMP — R7607 2K49R2F-2-L-GP

1V_VGA_S0

1U*4 X6S Place under GPU
4.7U*2 X6S Place near GPU
10U*1 X5R Midway between GPU and VR
22U*1 X5R Midway between GPU and VR

0.47U*12 X6S Place under GPU
Change to 1uF 0201 X6S *6 use two 0201W 0.47uF X6s for each 0201W 1uF
C7627 C7628 C7629 C7630 C7631 C7632 — Do Not Stuff; SC1U6V1MX-1NF-GP; N17/N18

4.7U*3 X6S Place under GPU
10U*3 X6S Place near GPU
22U*2 X6S Place near GPU
C7633 C7634 C7635 C7636 C7637 C7638 C7639 C7640 C7641 C7642 C7643
SC4D7U6D3KX-5-GP-U; SC10U6D3VSKX-5DL-GP; N17/N18 CD; N18

1D8V_VGA_S0

1U*4 X6S Place under GPU
4.7U*2 X6S Place near GPU
10U*2 X5R Midway between GPU and VR
22U*1 X5R Midway between GPU and VR

0.47U*13 X6S Place under GPU
Change to 1uF 0201 X6S *6 use two 0201W 0.47uF X6s for each 0201W 1uF
C7644 C7645 C7646 C7647 C7648 C7649 C7650 C7651 C7652 C7653 C7654 C7655 C7656
SC1U6V1MX-1NF-GP; N17/N18; N18

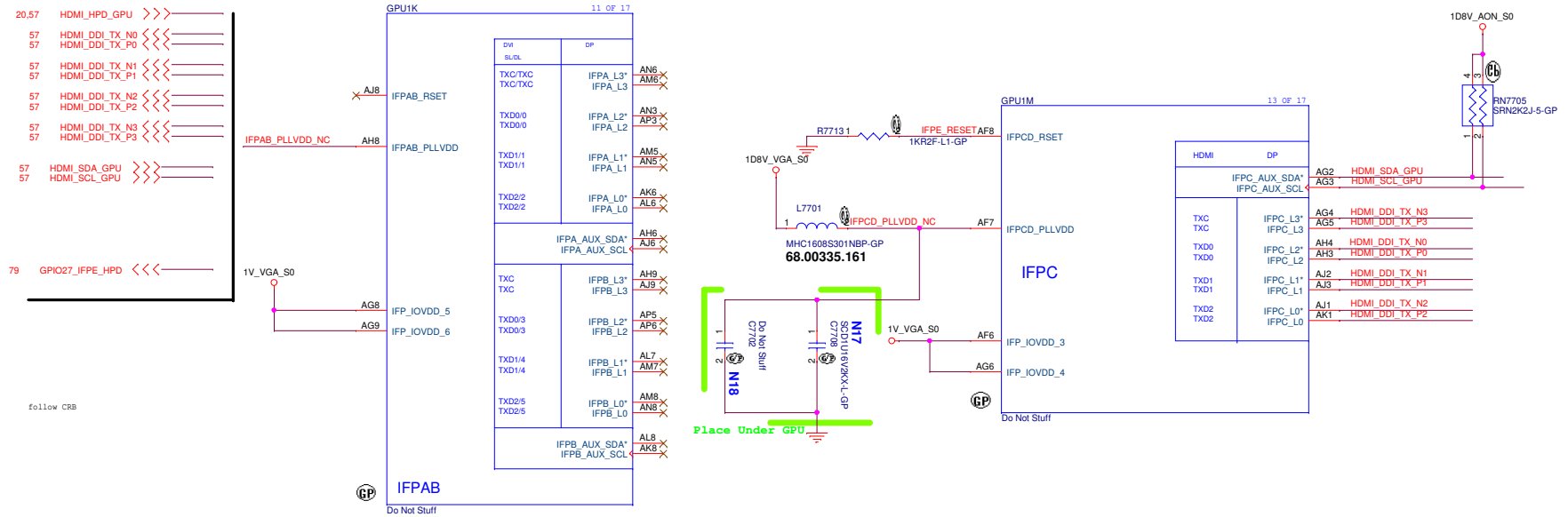
4.7U*3 X6S Place under GPU
10U*3 X6S Place near GPU
22U*2 X6S Place near GPU
C7657 C7658 C7659 C7660 C7661 C7662 C7663 C7664 C7665 C7666 C7667 C7668 C7669
SC4D7U6D3KX-5-GP-U; SC10U6D3VSKX-5DL-GP; SC22U6D3VSKX-5DL-GP; N17/N18; N18

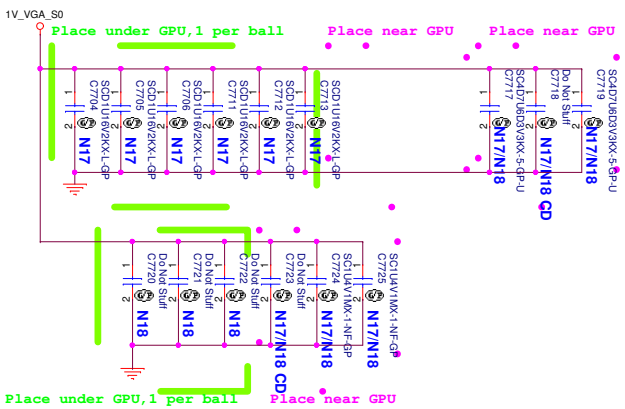
0.1U*1 X5R Place under GPU
0.47U*1 X6S Place under GPU
1D8V_VGA_S0
no 0201W 0.47uF X6s,so change to 1uF 0201W X6s
C7661 C7664 — SC01U16V2KX-L-GP; N17; N18

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_960M_PEG (1/5)
Size: A2 | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 76 of 105





Change to 1uF 0201 X6S *3 from 0201 X6S0.47u*6
use two 0201W 0.47uF X6s for each 0201W 1uF

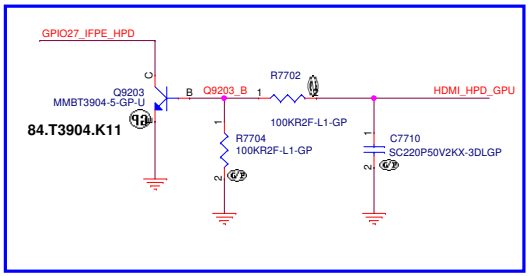


Table 7. IFPy_IOVDD Decoupling and Filtering

GPU	Type	Footprint	Population N18	Population N17	Location
IFP_IOVDD Supply Rails					
GB4C-128, GB4D-128	0.1 µF X7R	0402	0	6	Under GPU; 1 per ball
	0.47 µF X6S	0201W	6	0	Under GPU; 1 per ball
	1.0 µF X6S	0402 or 0201W	0	3	Near GPU
	0.47 µF X6S	0201W	6	0	Near GPU
	4.7 µF X6S	0603	3	3	Near GPU
	Bead Type				
	180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	0	0	Near GPU

Note:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0201W 1 µF.
2. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

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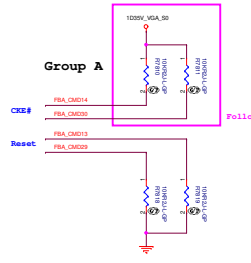
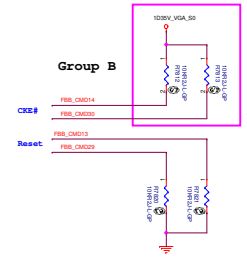
FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side



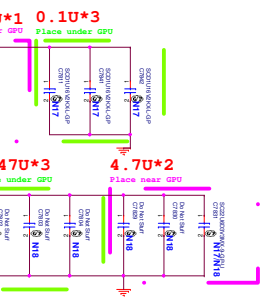
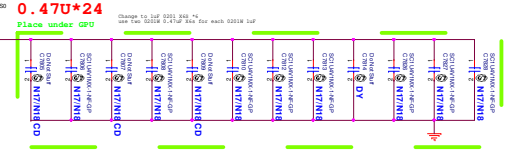
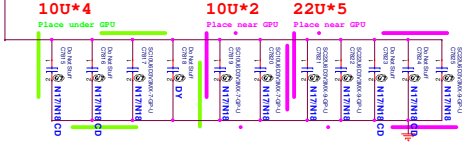


Table 4. Frame Buffer PLL3 Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
FB PLL Supply Rail for GDDR5					
G84C-128, G84D-128	0.1 uF	X7R 0402	0	3	Under GPU
	0.47 uF	X6S 0201W	3	0	Under GPU
	22 uF	X5R 0805	0	1	Near GPU
	22 uF	X6S 0805	1	0	Near GPU
	4.7 uF	X6S 0603	2	0	Near GPU
Bead Type					
	30 Ω (ESR@100 MHz)	0603	1	1	Near GPU

Notes:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0201W 1 µF.





GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
FBVDDQ Supply Rail for GDDR5					
G84C-128, G84D-128	0.47 µF	X6S 0201W	24	0	Under GPU
	1 µF	X6S 0402 or 0201W	0	12	Under GPU
	10 µF	X6S 0603	4	4	Under GPU
	10 µF	X6S 0603	2	2	Near GPU
	22 µF	X6S 0603	5	5	Near GPU

Notes:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

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A1	Selek CFL-H	A00

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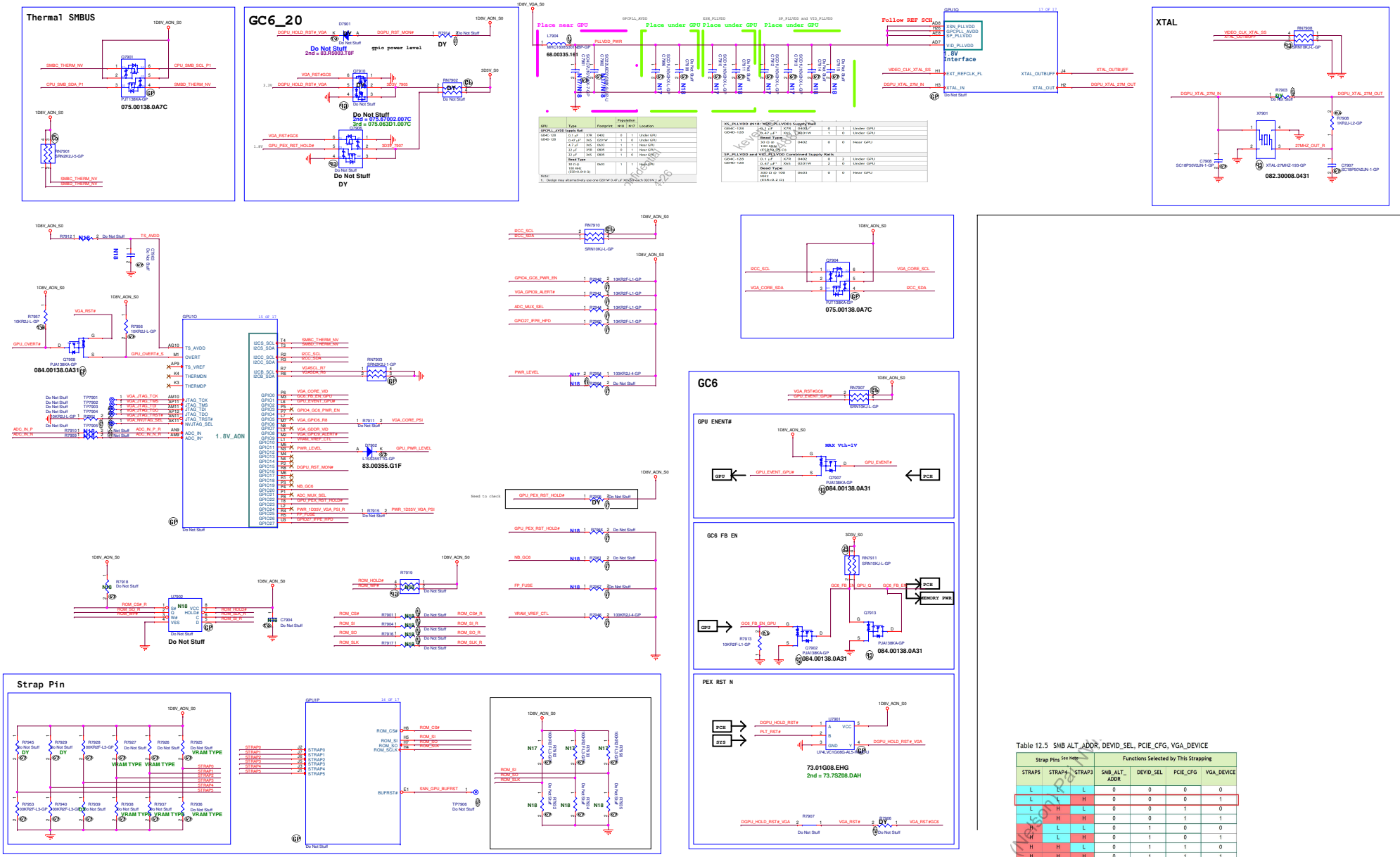

Strap2	Strap1	Strap0	vendor	vendor number	wistron P/N	strap	GPU
L	L	L	Samsung	K4G80325FB-HC28	N1MMH$AA	0x0	N17P
L	L	H	Micron	MT51J256M32HF-80:B	MHVDX$AA	0x1	N18P
L	H	L	Hynix	H5GC8H24AJR-R2C	GVK6K$AA	0x2	N18P
L	L	L	Samsung	K4G80325FC-HC25	J62CN$AA	0x0	N18P

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins (see Note)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 3. N17P-G1/G0/G0-K1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	N/A	Post production ready
			Hynix	H5GC8H24MJR-R2C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	M	1 (0x0001)
L	L	H	2 (0x0002)
L	M	L	3 (0x0003)
L	M	M	4 (0x0004)
L	M	H	5 (0x0005)
L	H	L	6 (0x0006)
L	H	M	7 (0x0007)
L	H	H	8 (0x0008)
M	L	L	9 (0x0009)
M	L	M	10 (0x000a)
M	L	H	11 (0x000B)
M	M	L	12 (0x000C)
M	M	M	13 (0x000D)
M	M	H	14 (0x000E)
M	H	L	15 (0x000F)
M	H	M	16 (0x0010)
M	H	H	17 (0x0011)
H	L	L	18 (0x0012)
H	L	M	19 (0x0013)
H	L	H	20 (0x0014)
H	M	L	21 (0x0015)
H	M	M	22 (0x0016)
H	M	H	23 (0x0017)
H	H	L	24 (0x0018)
H	H	M	25 (0x0019)
H	H	H	26 (0x001A)

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A1	Selek CFL-H	A00

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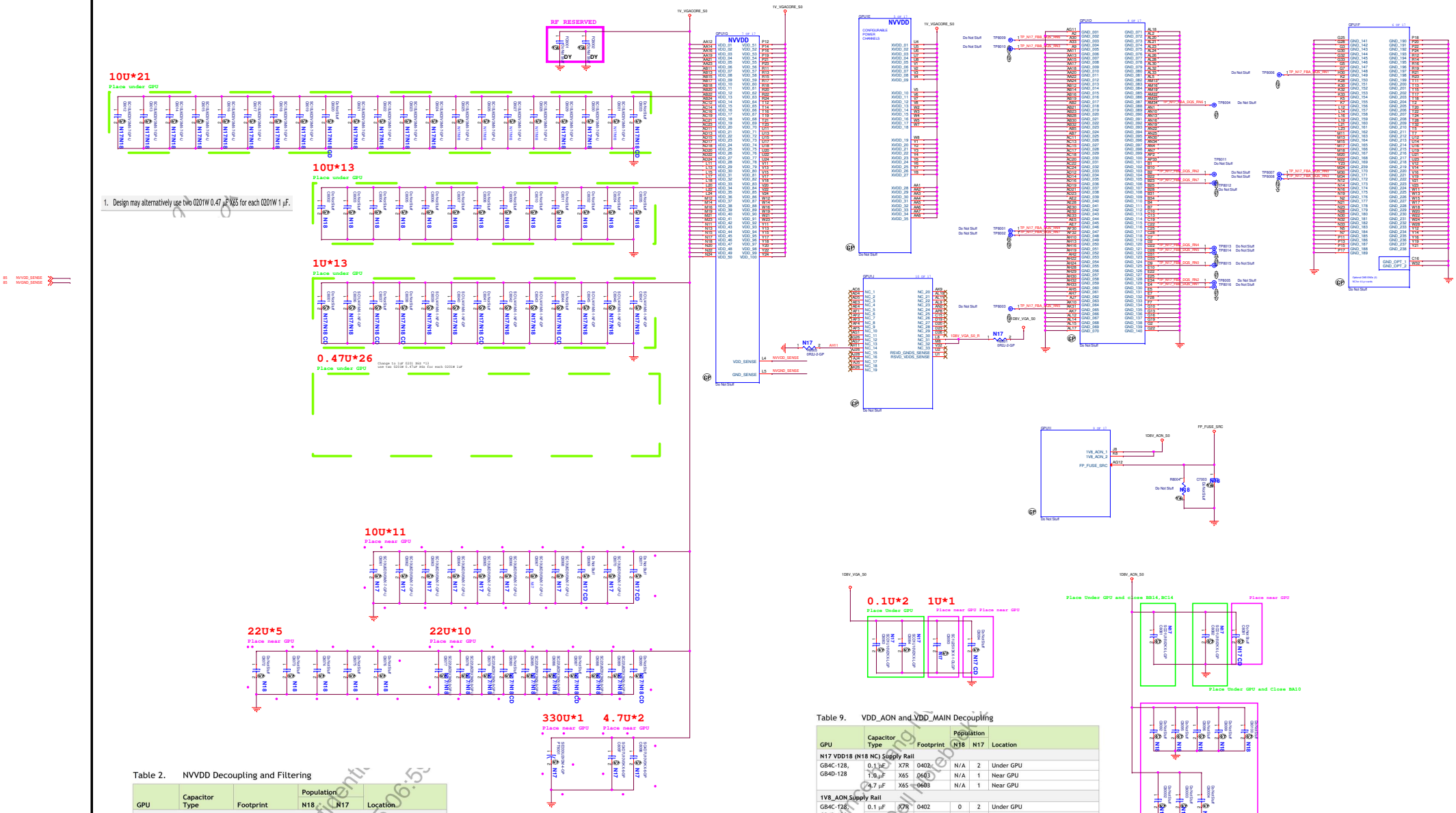

Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
NVVDD Supply Net						
GB4C-128, GB4D-128	10 µF	X6S	0603	34	21	Under GPU
	1 µF[1]	X6S	0402 or 0201W	0	13	Under GPU
	0.47 µF[1]	X6S	0402 or 0201W	26	0	Under GPU
	10 µF	X6S	0603	0	11	Near GPU
	22 µF	X6S	0805	15	10	Near GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	330 µF	POS	7343	0	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	N/A	2	Under GPU
	1.0 µF	X6S	0603	N/A	1	Near GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU
	0.47 µF[1]	X6S	0201W	4	0	Under GPU
	1.0 µF[1]	X6S	0402 or 0201W	0	1	Near GPU
	0.47 µF[1]	X6S	0201W	6	0	Near GPU
	4.7 µF	X6S	0603	3	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

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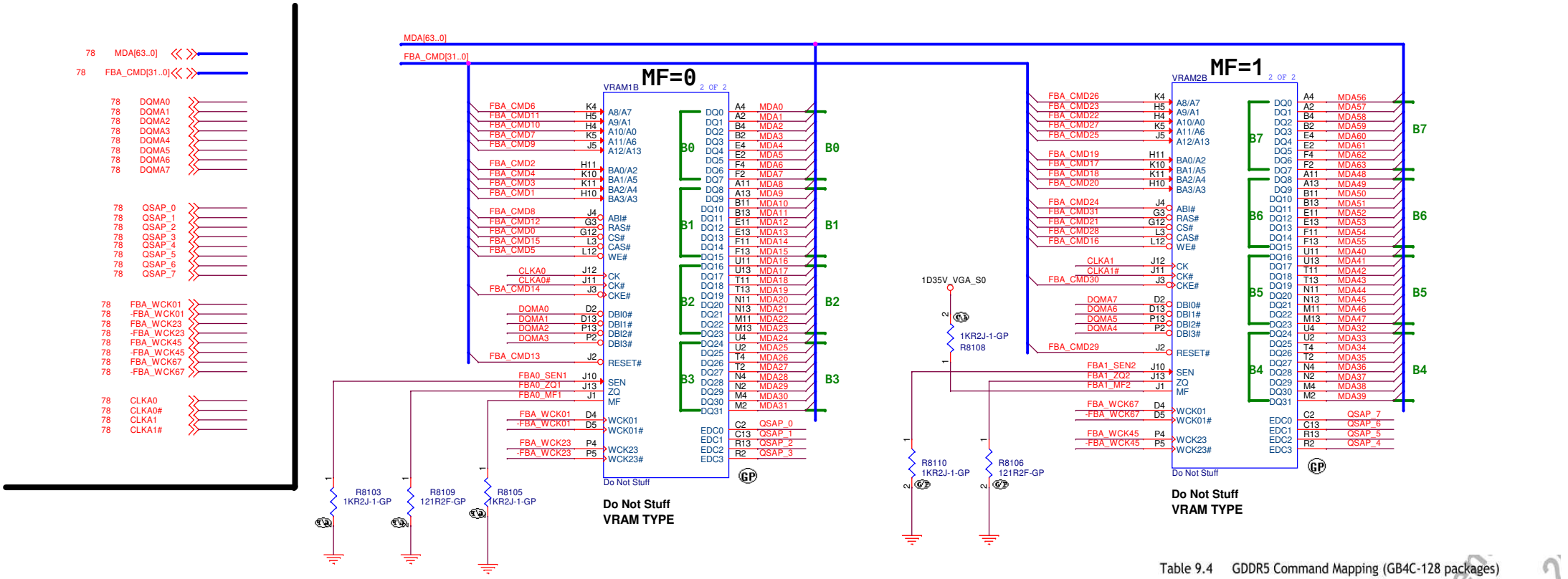

GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ		RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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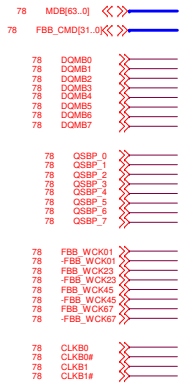

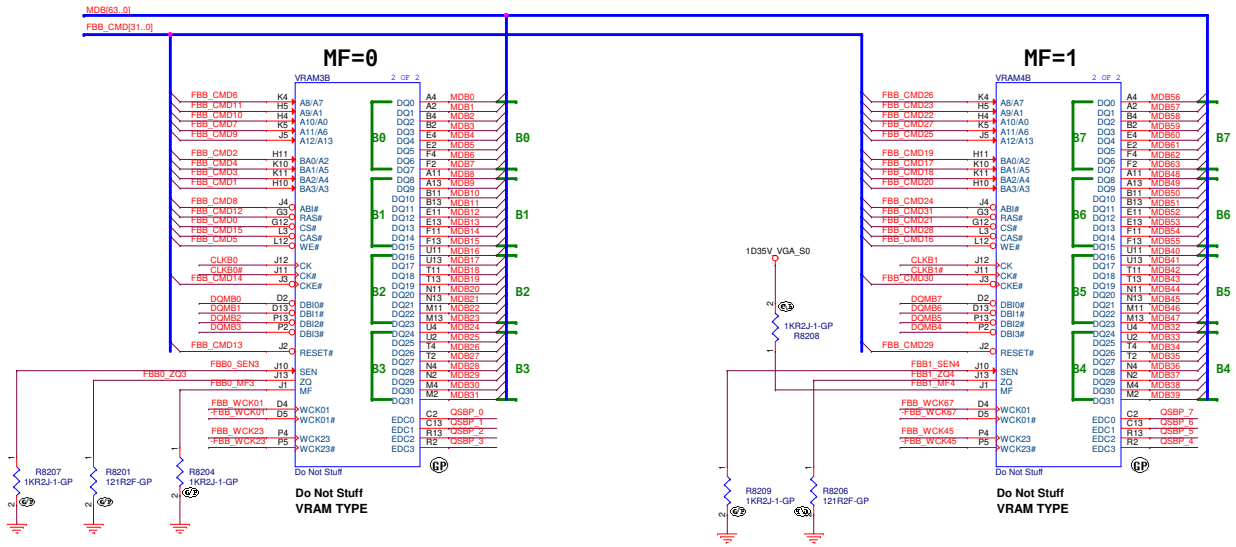

GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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Custom	Selek CFL-H	A00

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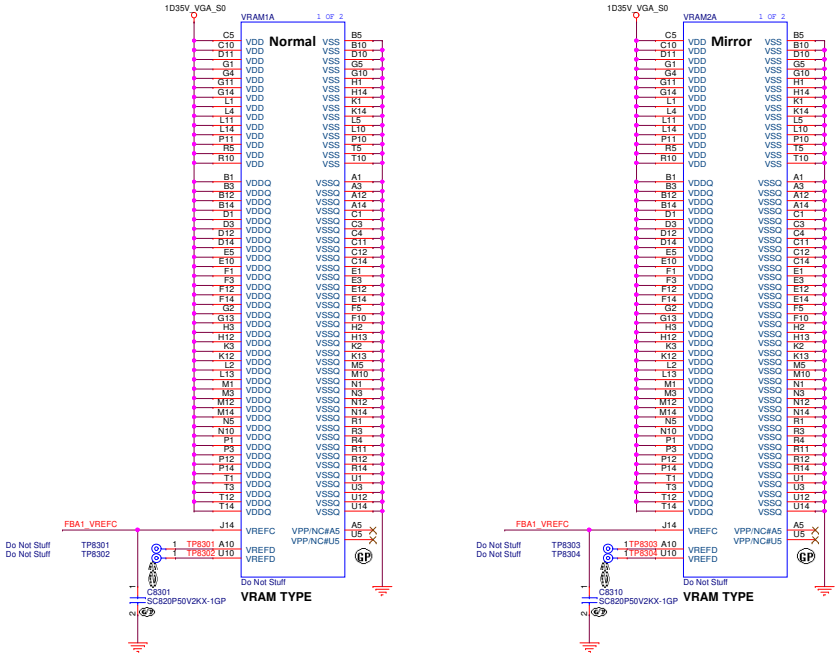

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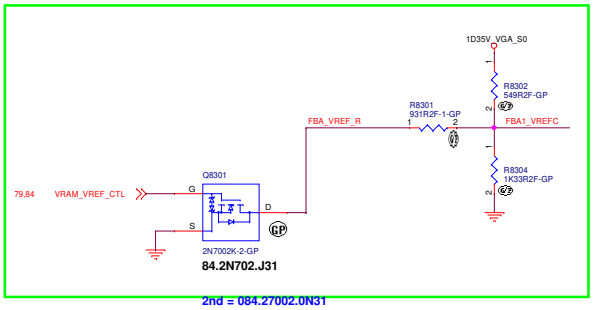

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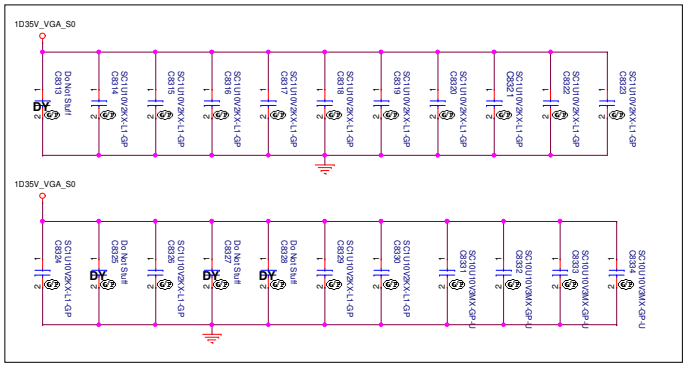
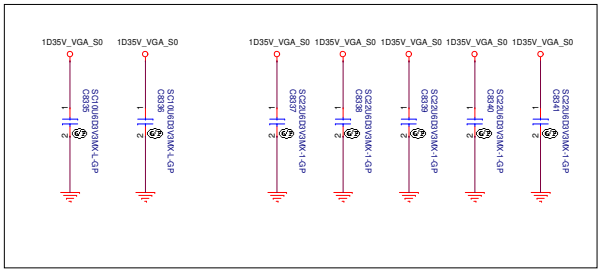


UNDER THE MEMORY

FOR VRAM1/ VRAM2



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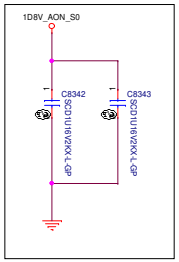

UNDER THE MEMORY

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Title: *VGA Power A*

Size: A2 | Document Number: Selek CFL-H | Rev: A00

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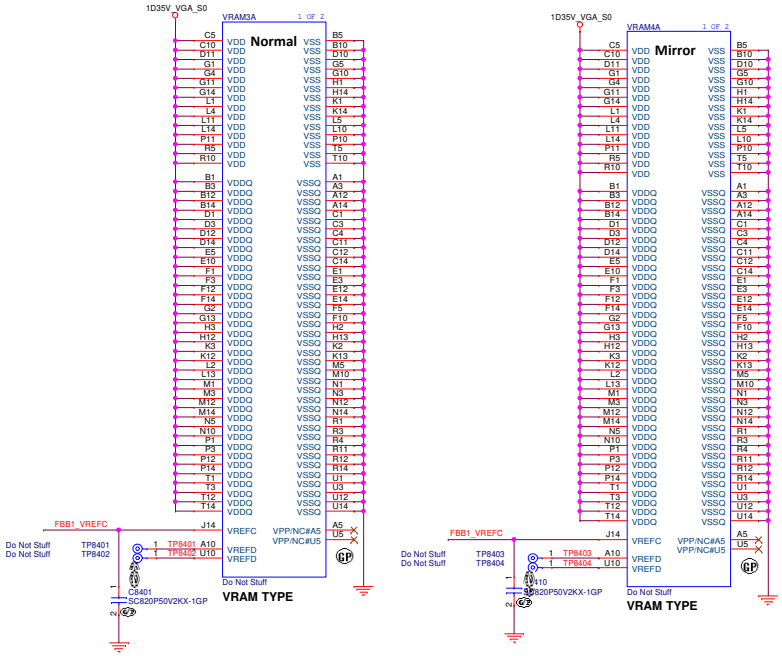

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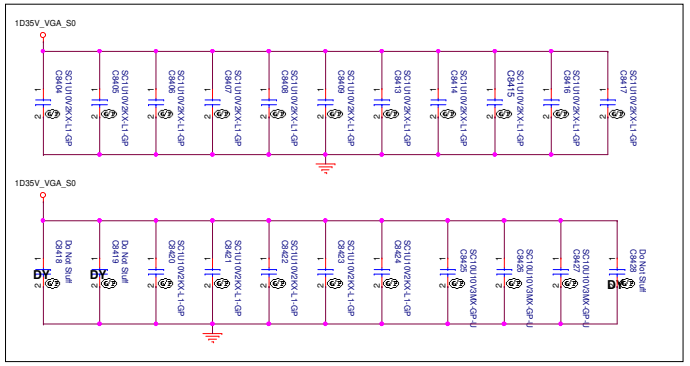

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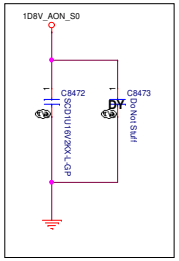
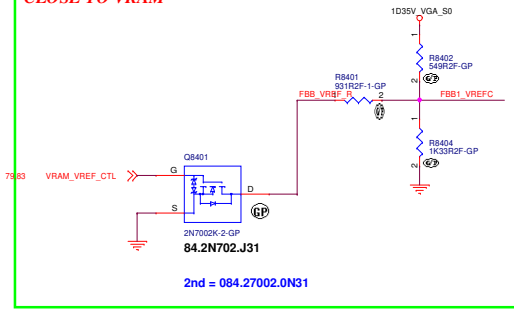
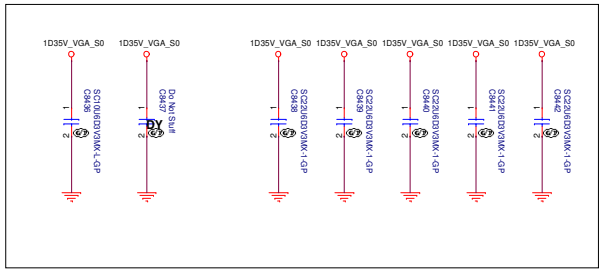


UNDER THE MEMORY

CLOSE TO VRAM





CLOSE TO THE MEMORY

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA Power B		
Size: A2	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet A4 of 105	

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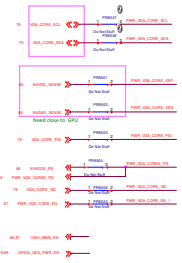


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	8.06
C	nF	0.1

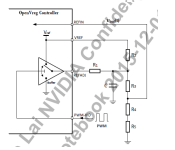
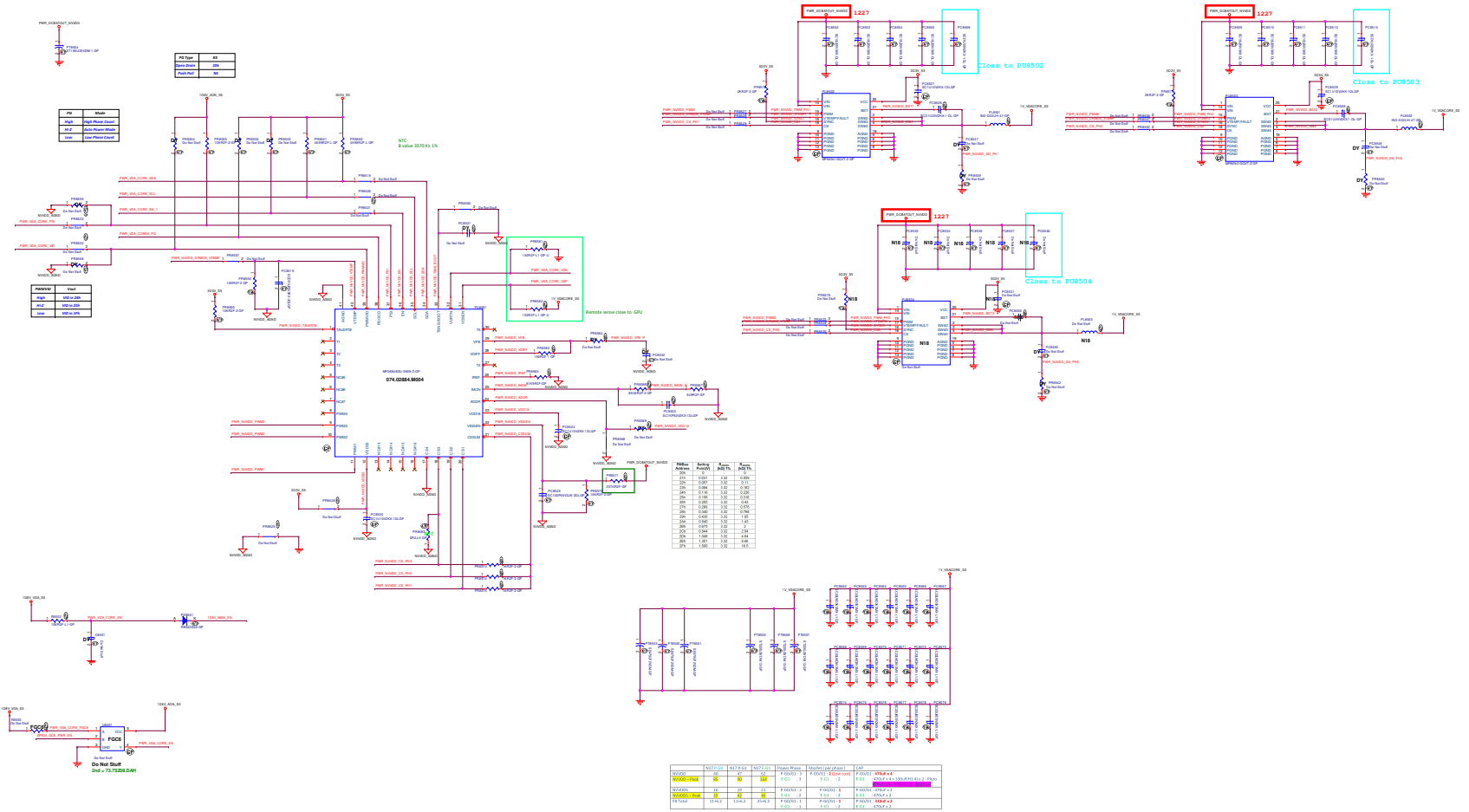


Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	8.06
C	nF	0.1



	NSTT=00	NSTT-01	NSTT-G1	Power Phase	MaxMet (per phase)	CAP
3V/VDD	48	47	52	P-VID/S1 - 5	P-VID/S1 - 3(Low cost)	P-VID/S1 - 470uF x 6
NVVDD - 7fmA	60	60	164	P-G1 - 3	P-G1 - 2	P-G1 - 470uF x 4 + 330uF(V) 41x2 - Poly
						330uF(V) 2.5V 7.3mΩ x 2
3V/VDD	16	20	23	P-VID/S1 - 2	P-VID/S1 - 1	P-VID/S1 - 470uF x 2
NVVDD - Fm8	30	30	30	P-G1 - 2	P-G1 - 2	P-G1 - 470uF x 2
FB Total	1+45-2	1+45-2	2+45-2	P-VID/S1 - 1 P-G1 - 1	P-VID/S1 - 1 P-G1 - 1	P-VID/S1 - 330uF x 2 P-G1 - 470uF x 2

Selek CFL-H BTP

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GPU VCORE POWER

Selek CFL-H

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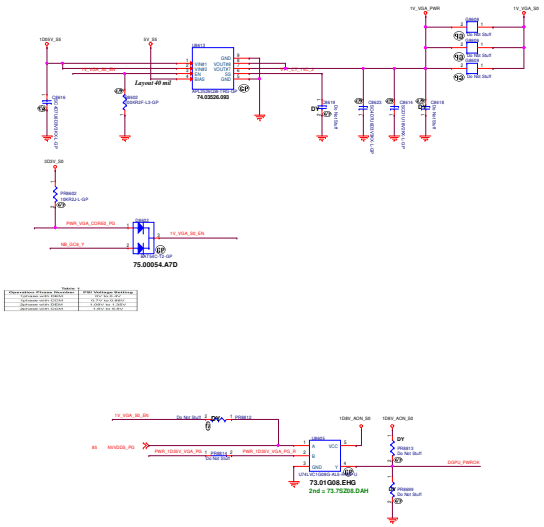
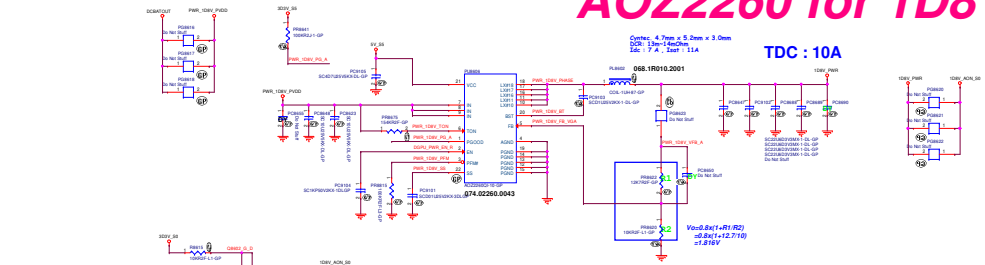
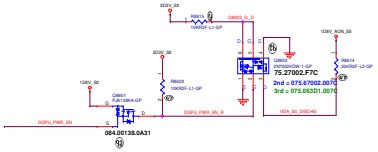
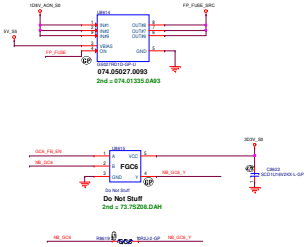
APL3526QB for 1V_VGA_S0



AOZ2260 for 1D8V_AON







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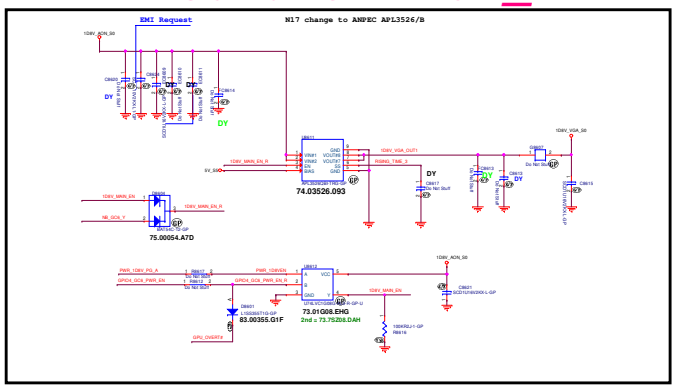

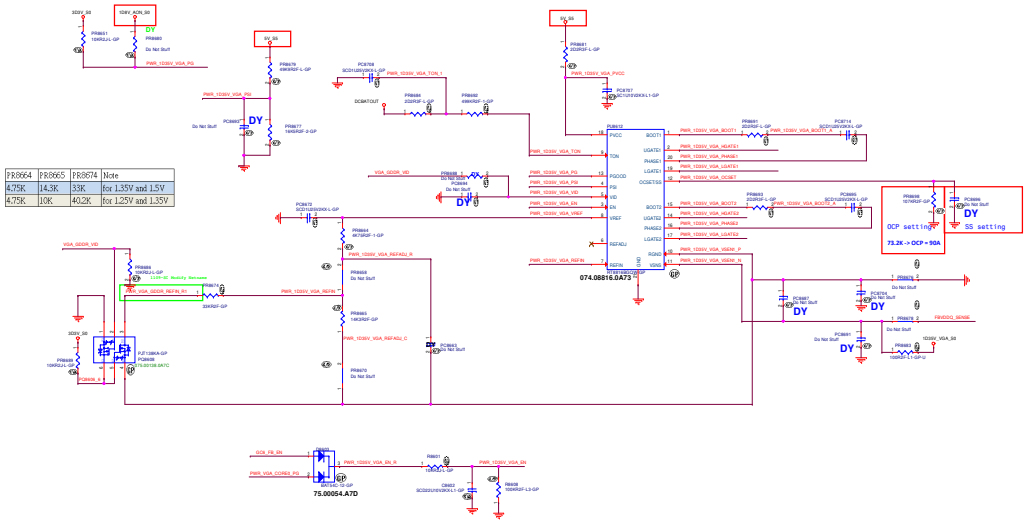

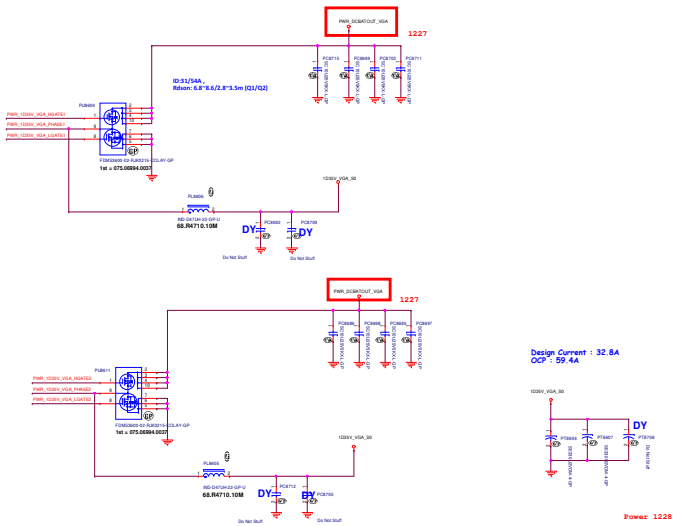

Selek CFLv0d13P

DELL	Wistron Corporation		
	GPU GDDR 1D35V		
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Custom	Selek CFL-H	A00	
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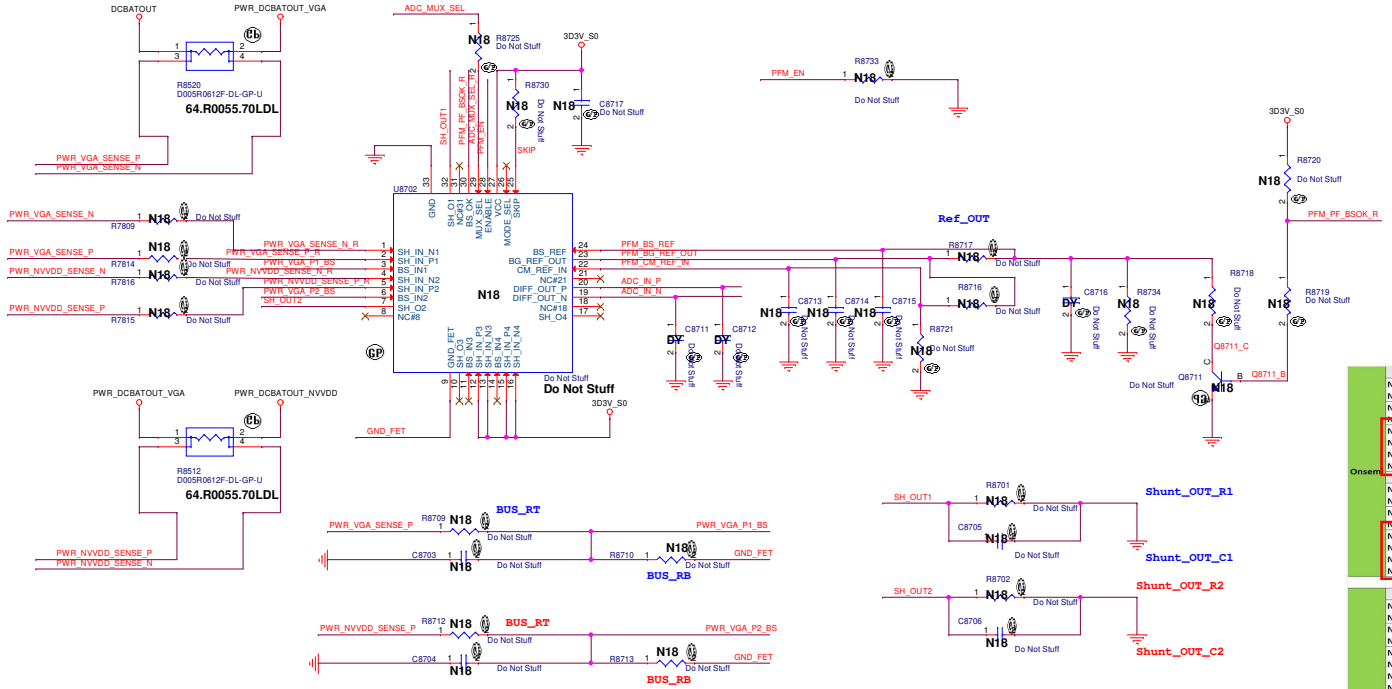
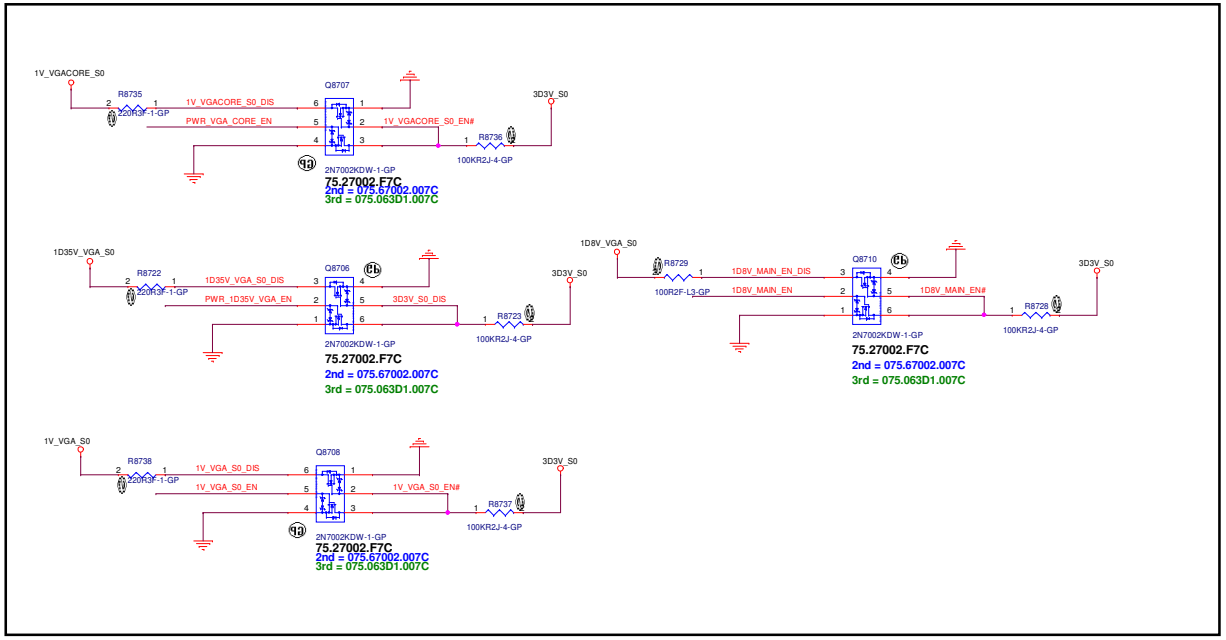


	TGP Current (GPU sku)	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
Onsem	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	169Ω	15nF	750K	6.49K	100pF	243K
	N18E-G2, N18E-G2 MAX-Q			191Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			287Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	169Ω	15nF	750K	6.49K	100pF	
	N18E-G2, N18E-G2 MAX-Q			191Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			287Ω					

	TGP Current (GPU sku)	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
upi	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	127Ω	15nF	750K	4.87K	100pF	324k
	N18E-G2, N18E-G2 MAX-Q			143Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			215Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	127Ω	15nF	750K	4.87K	100pF	
	N18E-G2, N18E-G2 MAX-Q			143Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			215Ω					

79 ADC_IN_P
79 ADC_IN_N
79 ADC_MUX_SEL

85 PWR_VGA_CORE_EN
86 1V_VGA_S0_EN
85,86 1D8V_MAIN_EN
86 PWR_1D35V_VGA_EN



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Discharge

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SSID = TPM

19 PIRQA#
15 TPM_SPI_IRQ#
26,31,61,63,79 PLT_RST#
15,40 PM_SLP_S0#
15 SPI_CS_CPU_N2
15,21,25 SPI_SO_CPU
15,21,25 SPI_SI_CPU
15,25 SPI_CLK_CPU

reserve RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH — R9148 — TPM — Do Not Stuff
3D3V_TPM_VHIO — R9140 — DY — Do Not Stuff
SPI_CS_CPU_N2 — R9130 — TPM — Do Not Stuff — SPI_CS2_TPM
SPI_SI_CPU — R9133 — TPM — Do Not Stuff — SPI_SI_TPM
SPI_SO_CPU — R9132 — TPM — Do Not Stuff — SPI_SO_TPM
SPI_CLK_CPU — R9138 — TPM — Do Not Stuff — SPI_CLK_TPM

Change to stuff vendor suggest 11/05

3D3V_TPM_VHIO — R9149 — DY — SPI_IRQ#_TPM2
Do Not Stuff

SPI_IRQ#_TPM2 — R9139 — DY — Do Not Stuff — TPM_SPI_IRQ#

3D3V_S0 — R9127 — TPM — Do Not Stuff
3D3V_S5 — R9126 — DY — Do Not Stuff
3D3V_TPM_VHIO
C9109 TPM Do Not Stuff
C9112 TPM Do Not Stuff
C9113 TPM Do Not Stuff

3D3V_S5 — R9143 — TPM — Do Not Stuff
3D3V_TPM_VSB
C9106 TPM Do Not Stuff
C9108 TPM Do Not Stuff

reserve for modern standby

U9102

8	VHIO	SDA/GPIO0	29 — TPM_GPIO0 — R9141 — DY — Do Not Stuff — PM_SLP_S0#
22	VHIO	SCL/GPIO1	30
1	VSB	PIRQ#/GPIO2	18 — SPI_IRQ#_TPM2 — R9137 — TPM — Do Not Stuff — PIRQA#
		GPIO3	6
		GPIO4	13
		PP/GPIO6	4
21	SPI_SI_TPM — MOSI/GPIO7	NC#7	7
24	SPI_SO_TPM — MISO	NC#9	9
20	SPI_CS2_TPM — SCS#/GPIO5	NC#10	10
19	SPI_CLK_TPM — SCLK	NC#11	11
	TPM	NC#12	12
17	PLT_RST# — R9136 — TPM — Do Not Stuff — PLT_RST#_Q_TPM2 — PLTRST#	NC#14	14
		NC#15	15
16	GND	NC#25	25
23	GND	NC#26	26
33	GND	NC#27	27
		NC#28	28
2	NC#2	NC#31	31
3	NC#3	NC#32	32
5	NC#5		

GP

Do Not Stuff

Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM2.0**

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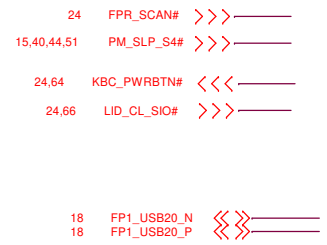
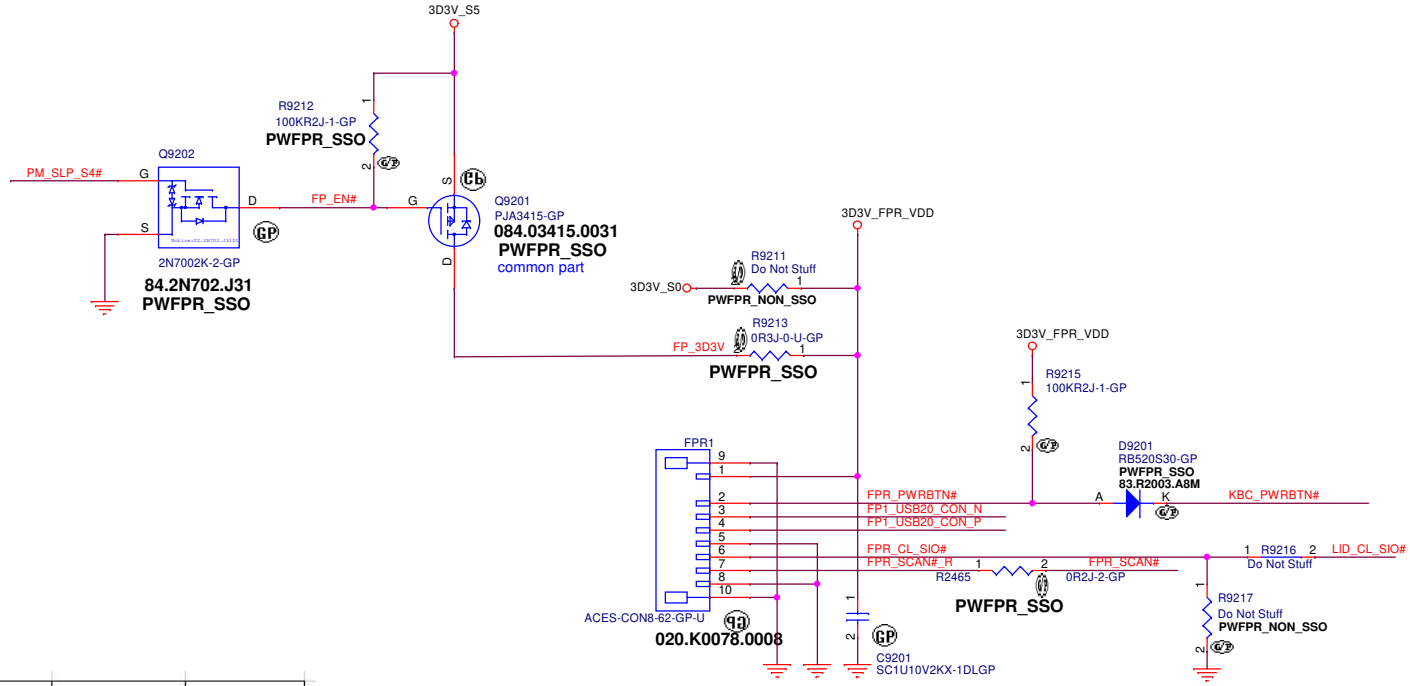
Main Func = FPR

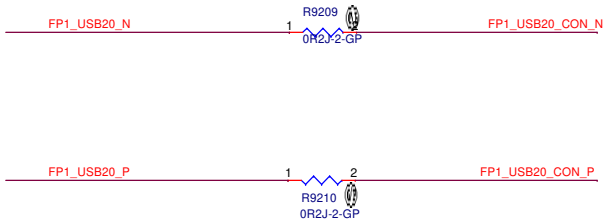
FBR(Botton side finger Print Sensor)

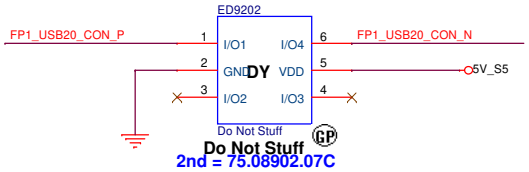
PWFPR_SSO: GOODIX module
PWFPR_NON_SSO: ELAN module(R9211 R9214 R9217)





	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0





GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Finger Print

Size: A3 | Document Number: Selek CFL-H | Rev: A00

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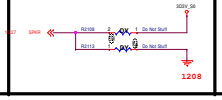
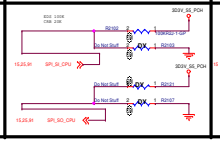
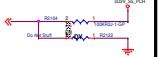
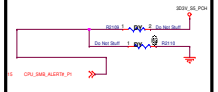
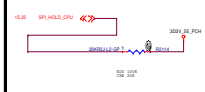
571182-cnl-pch-eds-h-vol1of2-rev2p1

CRB P.103 P.104

GPIO	GPP_B14 SPKR	GPP_B18 GSPIO_MOSI	GPP_C2 SMBALERT#	GPP_B22 GSPI1_MOSI	GPP_C5 SM0ALERT#	SPI0_MOSI SPI0_MISO	GPP_H15 SML3ALERT#
Schematic		default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side			

GPIO	GPP_B23 SML1ALERT# PCHHOT#	SPI0_IO2	SPI0_IO3	HDA_SDO/ I2S0_TXD	GPP_H12 SML2ALERT#	GPP_I6 DDPB_CTRLDATA	GPP_I8 DDPC_CTRLDATA
Schematic					internal pull down	Pull high at page 19	internal pull down

need check the latest CRB,PDG

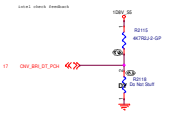
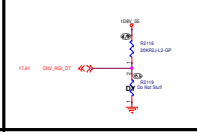
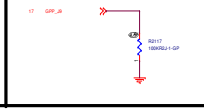
GPIO	GPP_I10	GPP_F23/ DPPF_CTRLDATA	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_J9	GPD7	
Schematic		internal pull down					

Table 9-1. Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address bit so that the upper 64-KB block in the PCH is where the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate number of bits for SPI. See the Top Swap section for more information. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DC4, bit 13). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel® ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel® ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS. **Notes:** 1. The internal pull-down is disabled after RSMRST# is de-asserted. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_B23 / GM7_MODE	Boot BIOS Destination	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DC5, bit 0). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If the strap is configured to LPC, BIOS may still be placed on SPI, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC is functional only. It is not validated. Platforms should not be shipped with accesses initiated to Intel® ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SM0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: If the strap is configured to '0' (eSPI Flash Sharing Mode) and no flash device is detected, the strap must be configured to '1' (eSPI Flash Sharing Mode is disabled).**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 20 kohm if pulled up to 3.3V or 1% kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2 / SML1ALERT# / PCHHOT#	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 1% kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3 / SML1ALERT# / PCHHOT#	eSPI or SMBus Used	Rising edge of RSMRST#	External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 1% kohm if pulled up to 1.8V. 0 = eSPI is selected (for EC). (Default) 1 = SMBus is selected (for EC). If eSPI is selected, SMBus is disabled. If SMBus is selected, eSPI is disabled. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 1% kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 1% kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is enabled).**
GPP_J0 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_J1 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-Down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
ITP_PMODE	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. Platforms that do not support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	A weak external pull-up is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. **Note:** When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down must be overridden and pull the strap load to enable CNVi interface.
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

Selek CFLH/H17P

Wistron Corporation
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Title: PCH_(Strap Pin)

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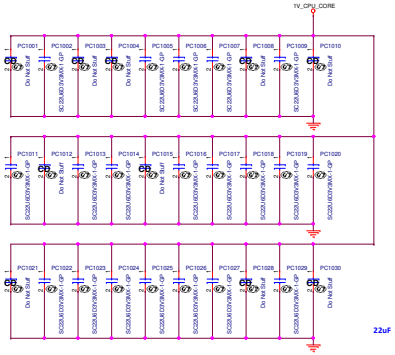
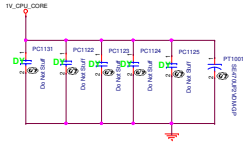
Main Func = CPU

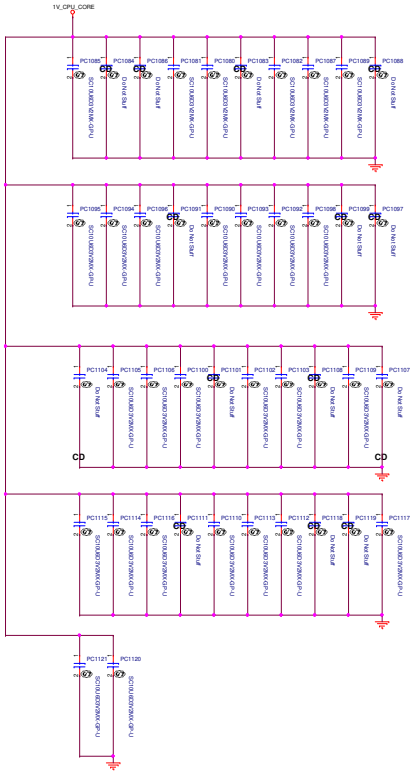
VCORE

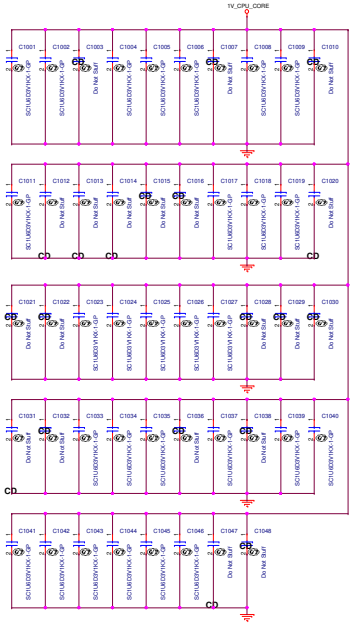
CFL-H_45W

H-line 45W
IccMax current-10ms max = 128A





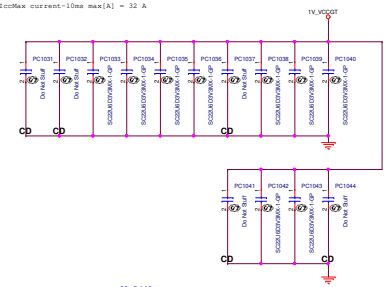


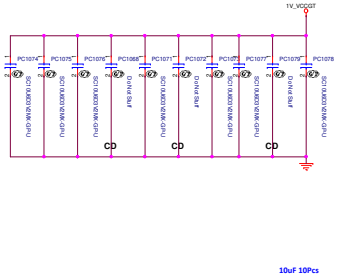


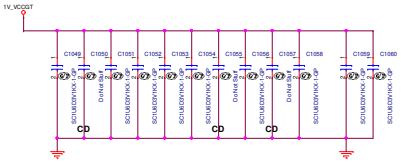
VCCGT

CFL-H_45W

IccMax current-10ms max[A] = 32 A



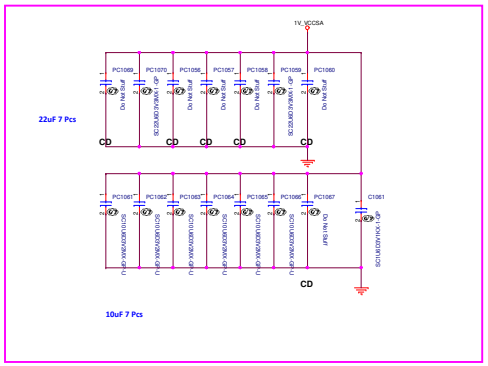


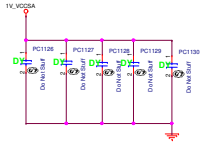


VCCSA

H-Line

IccMax current-10ms max[A] = 11.1 A





Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: A3 | Document Number: Selek CFL-H | Rev: A00

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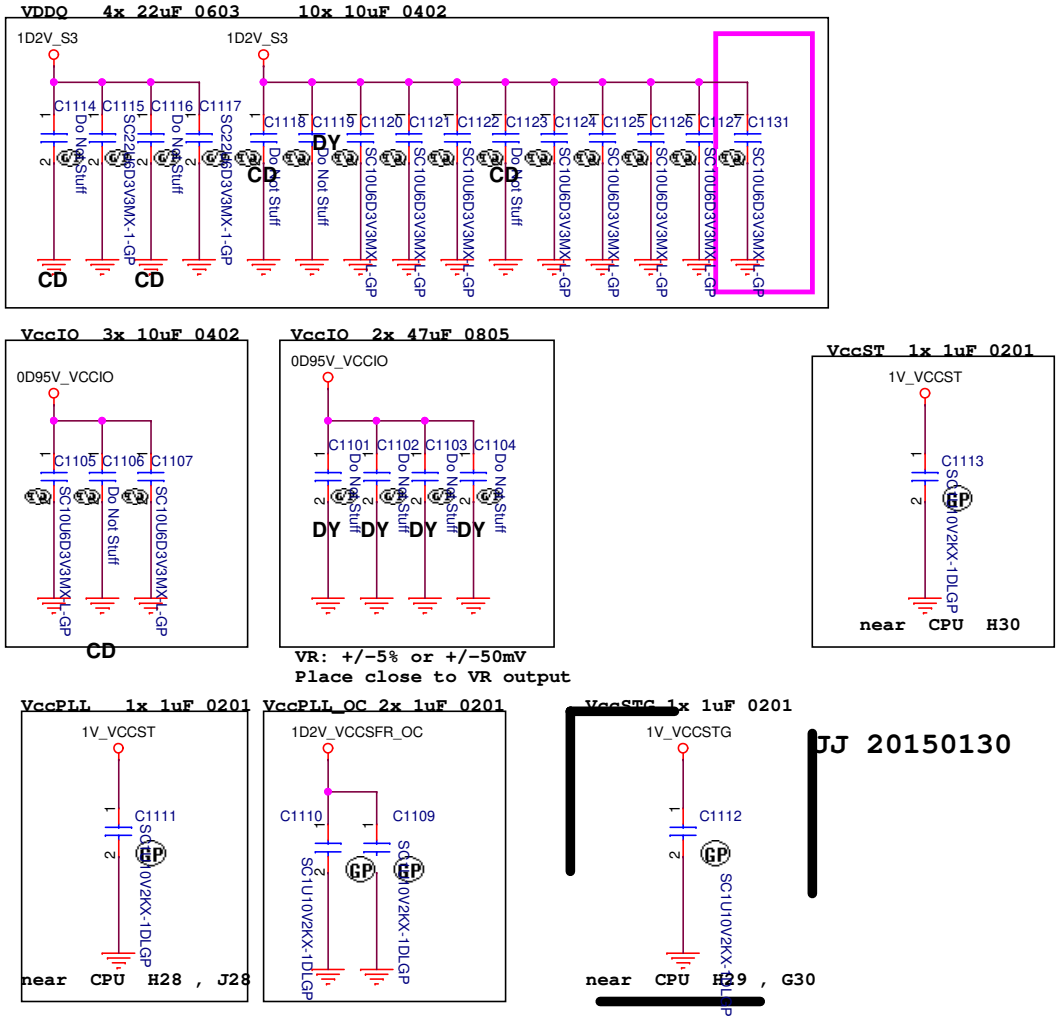

Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 1 of 2)

Domain	Board Edge cap	Backside cap	Notes
Vcc	2x 22uF 0603		
	8x 47uF 0805		
		48x 1uF 0201	
		42x 10uF 0402	
		10x 22uF 0603	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
Vcc_{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
	1x 22uF/47uF 0805 (placeholder)		*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.

Domain	Board Edge cap	Backside cap	Notes
Vcc_{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with V_{DDQ}. Board resistance from BGA to Power gate should be less than 86mOhm.

Note: High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.

Note: It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (Power CAP2)*

Size: Custom | Document Number: Selek CFL-H | Rev: A00

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HS1
STF236R128H101-3-GP
34.4YG18.001

HS2
STF237R113H184-GP
434.0H70B.0001

H16
Do Not Stuff
Do Not Stuff

H15
Do Not Stuff
Do Not Stuff

SPR1
Do Not Stuff
DY
Do Not Stuff

SPR2
SPRING-43-GP-U
34.15J03.001

SPR3
Do Not Stuff
DY
Do Not Stuff

SPR4
Do Not Stuff
DY
Do Not Stuff

H1
Do Not Stuff
Do Not Stuff

H2
Do Not Stuff
Do Not Stuff

H4
Do Not Stuff
Do Not Stuff

H5
Do Not Stuff
Do Not Stuff

H6
Do Not Stuff
Do Not Stuff

H9
Do Not Stuff
Do Not Stuff

H10
Do Not Stuff
Do Not Stuff

H11
Do Not Stuff
Do Not Stuff

H12
Do Not Stuff
Do Not Stuff

H13
Do Not Stuff
Do Not Stuff

H14
Do Not Stuff
Do Not Stuff

EMI Request

5V_S5

EC8938 EC8936 EC8937 EC8939 EC8940
DY DY
Do Not Stuff Do Not Stuff
SCD1U25V2KX-L-GP SCD1U25V2KX-L-GP SCD1U25V2KX-L-GP

SB 20160831

5V_S0

EC8943 EC8941 EC8942 EC8944 EC8945
DY DY
Do Not Stuff Do Not Stuff
SCD1U25V2KX-L-GP SCD1U25V2KX-L-GP SCD1U25V2KX-L-GP

EMI Request

DCBATOUT

EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910
DY
Do Not Stuff
SCD1U25V2KX-L-GP

EC8917 EC8914 EC8912 EC8915 EC8916 EC8911 EC8913
SCD1U25V2KX-L-GP

EMI Request

1D2V_S3

SB 20160822

EC8918 EC8919 EC8920 EC8921 EC8922 EC8923 EC8924 EC8925
DY
Do Not Stuff
SCD1U25V2KX-L-GP
SC100P50V2JN-1GR
SC1KP50V2KX-L-GP

EMI Request

1D35V_VGA_S0

SB 20160822

EC8932 EC8930 EC8927 EC8931 EC8929 EC8933 EC8926 EC8928 EC8934 EC8935
DY DY DY
Do Not Stuff Do Not Stuff Do Not Stuff
SCD1U25V2KX-L-GP
SC1KP50V2KX-L-GP

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Selek CFL-H	A00

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