

COMPAL CONFIDENTIAL

MODEL NAME : ZAM60

Board NO : LA-A893P

PCB NO : DA600146000

BOM P/N : 4319S031L01

GPIO MAP: 3.6C

Houston 12" UMA Entry M/B

Broadwell U Processor


2014-03-07

REV : 0.3 (X01)

- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component
- VPRO@ : VPRO Component
- DIMMB@ : DIMMB Component

Part Number	Description
DA600146000	PCB 130 LA-A893P REV0 M/B UMA W/O DOCK 1

Layout Dell logo



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REV: X01
PWB: 84J8X
DATE: 1351-02

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Cover Sheet

LA-A893P

Friday, March 07, 2014

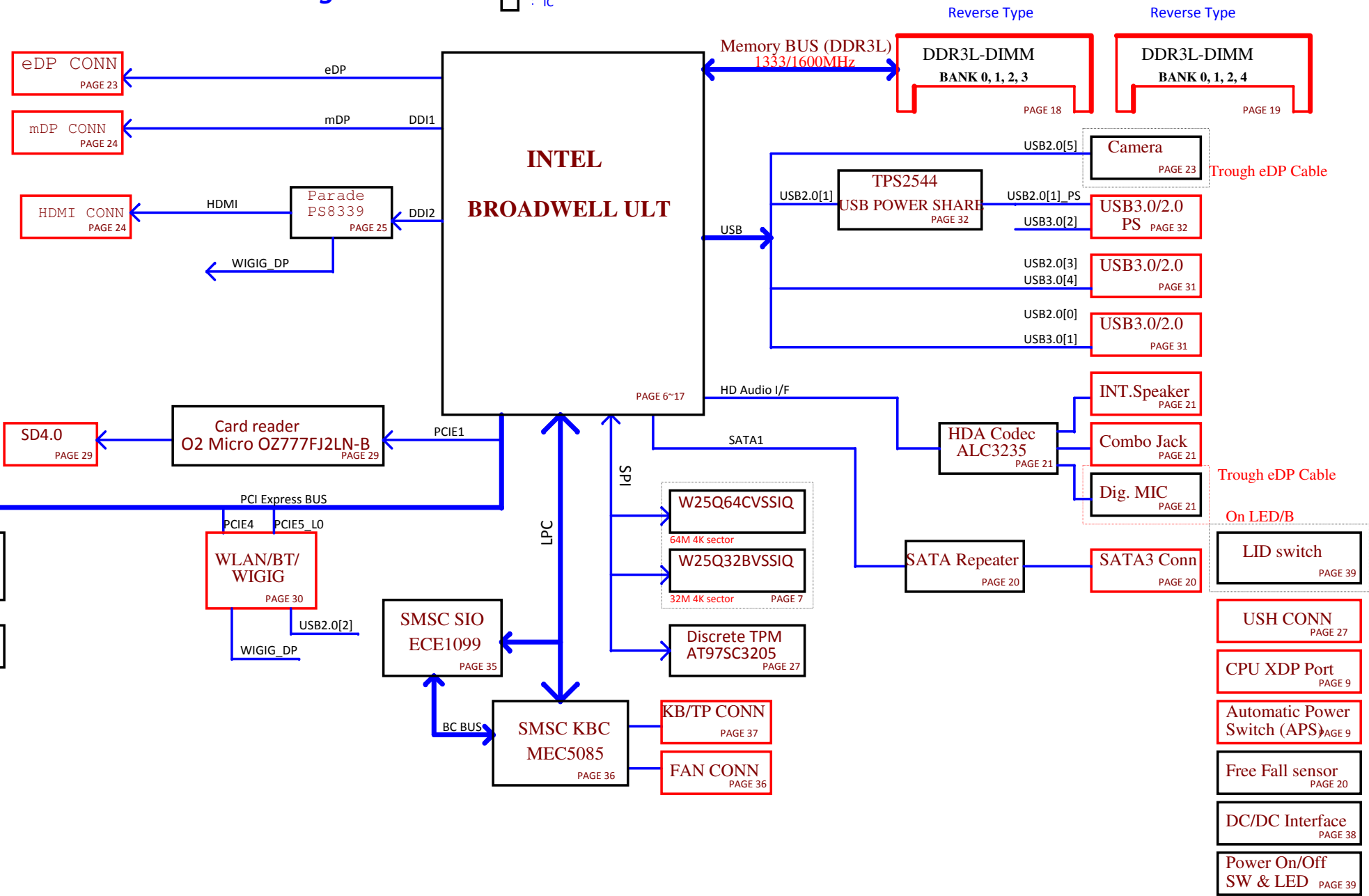
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Houston 12 - non Dock Block Diagram

□ : CONNECTOR

□ : IC



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Block diagram			
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE +1.5V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6	L3	SATA 0	
	L2	SATA 1	JSATA1 (HDD)
	L1		
	L0		

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	

USH	0	BIO
	1	NA

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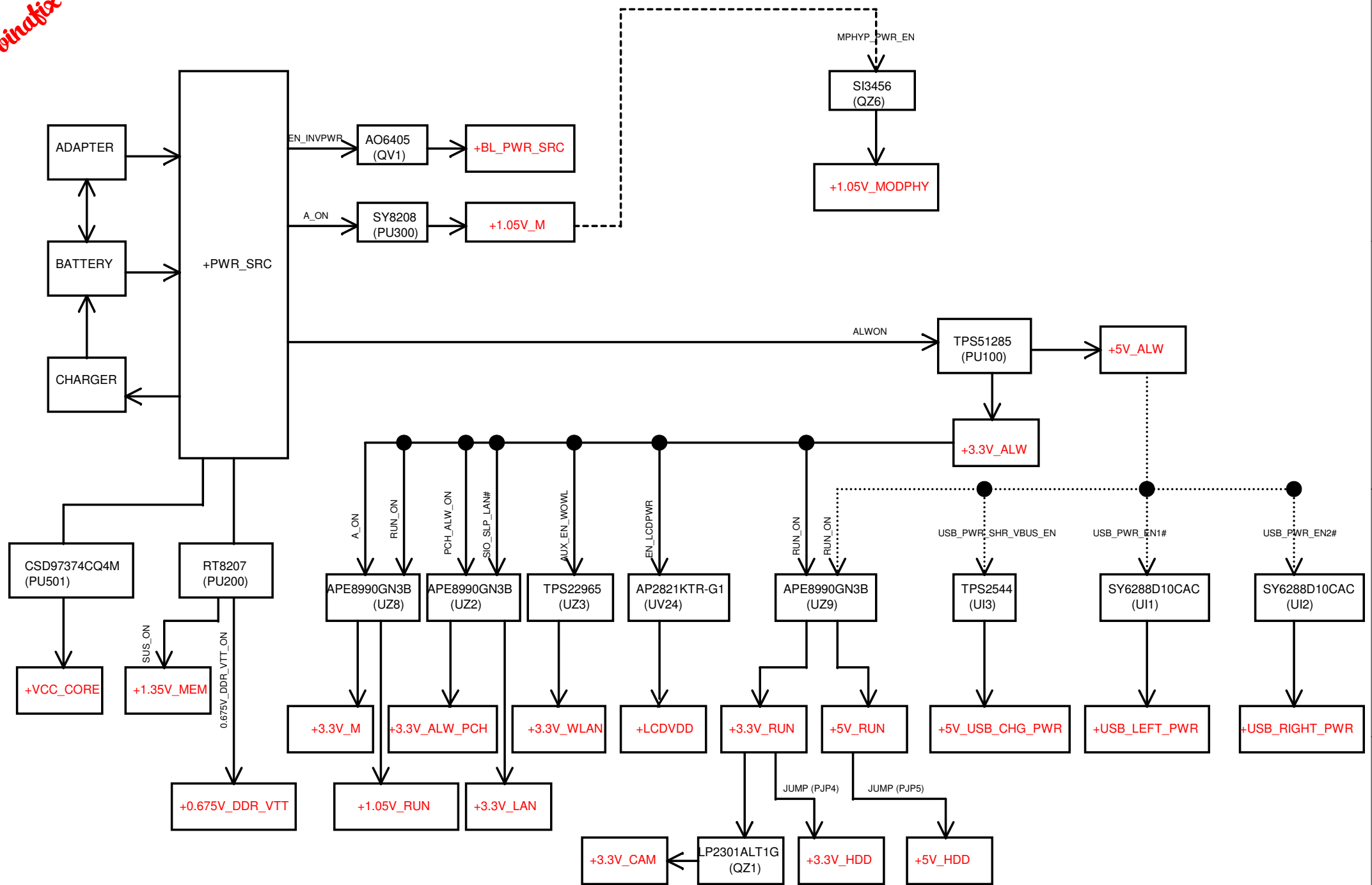
Port assignment

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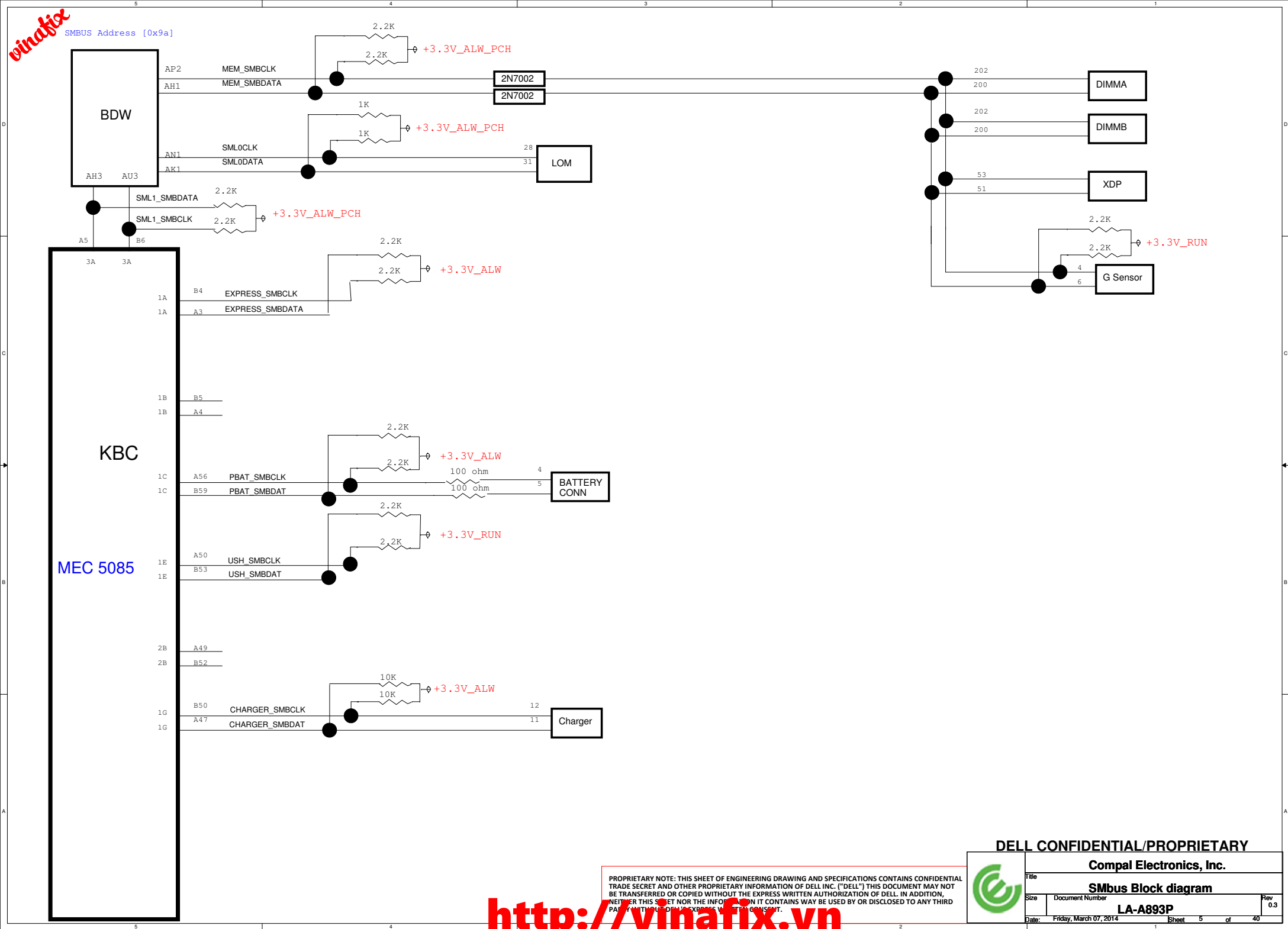
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Power rails

LA-A893P

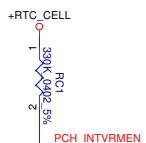
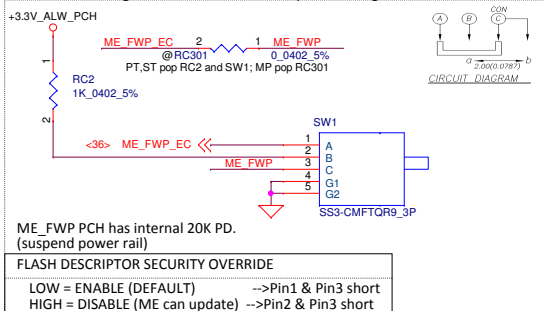
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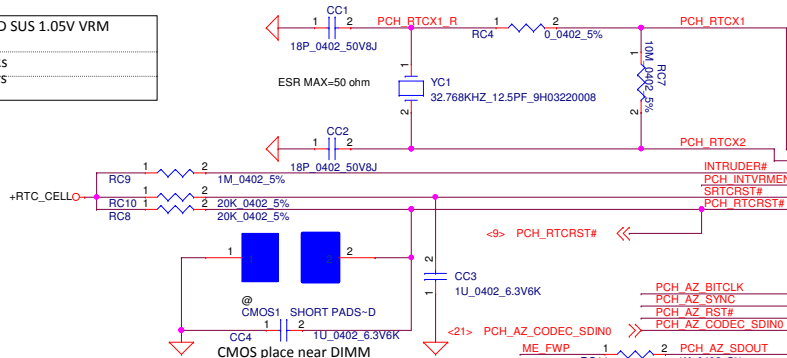
UMA SATA port



Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

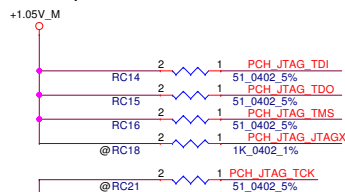


INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

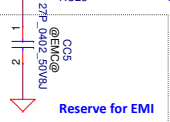
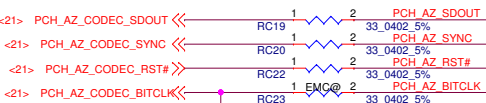


ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



HDA for Codec



SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H12 Entry	NA	NA
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H14D_En	NA	NA
NA	HDD	H14U_En	NA	NA
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H15D_En	NA	M2 3030 WIGIG
NA	HDD	H15U_En	NA	Express card

contact to WWAN

SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

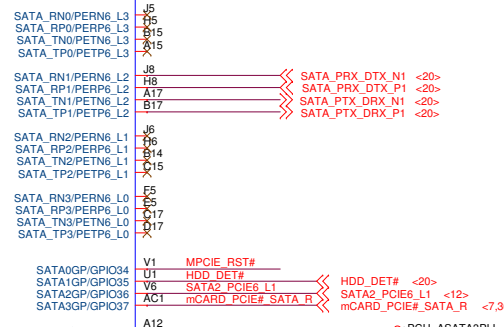
SATA2/PCIE6_L1 contact to WWAN
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

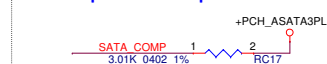
contact to WLAN

contact to Express card

SATA HDD



SATA Impedance Compensation



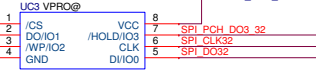
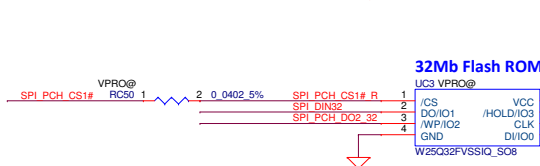
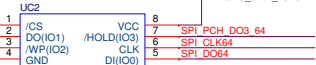
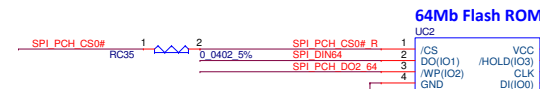
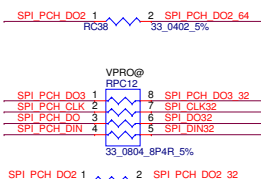
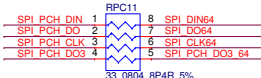
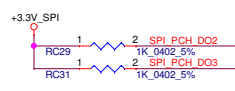
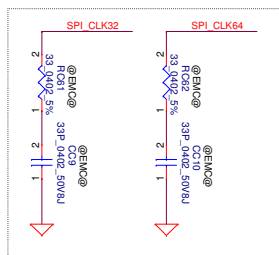
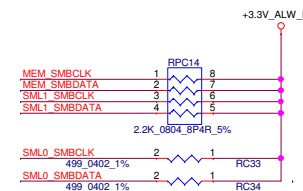
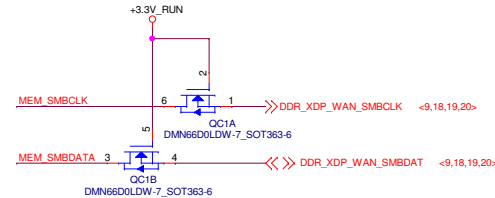
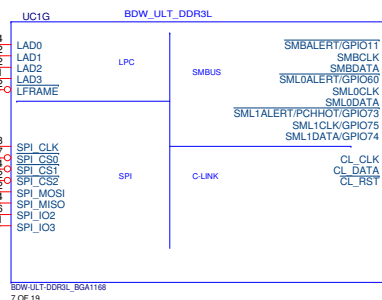
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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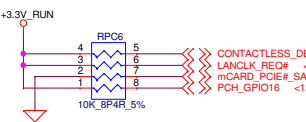
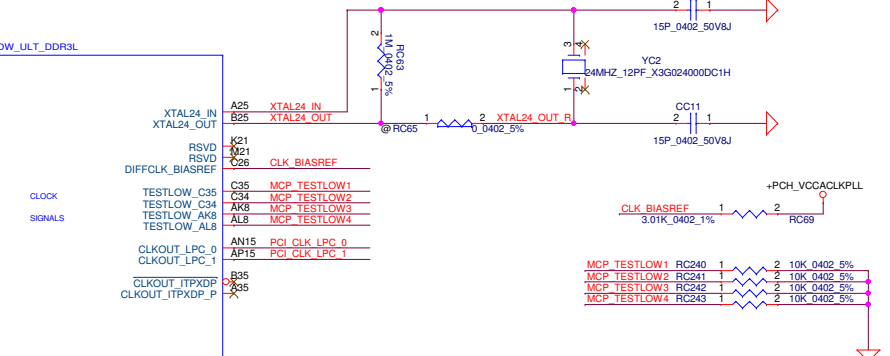
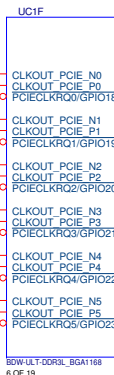
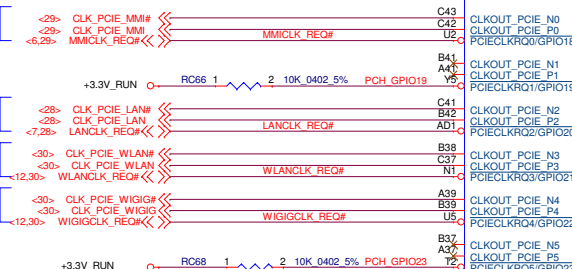
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CPU (1/12)			
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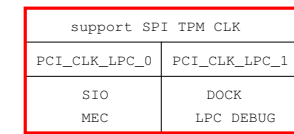
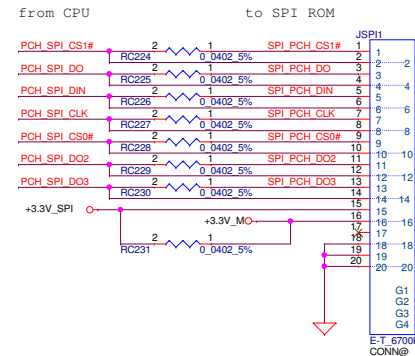
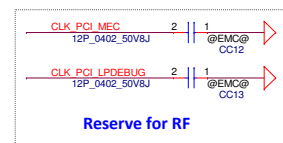
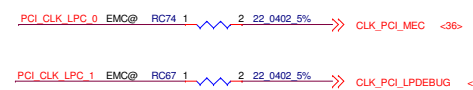
UC1G				BDW_ULT_DDR3L			
<36>	LPC_LAD0	<<>	LPC_LAD0	AU14	LAD0		SMBALERT/GPI0T1
<36>	LPC_LAD1	<<>	LPC_LAD1	AW12	LAD1	LPC	SMBCLK
<36>	LPC_LAD2	<<>	LPC_LAD2	AY12	LAD2		SMBDATA
<36>	LPC_LAD3	<<>	LPC_LAD3	AW11	LAD3	SMBUS	SMBDUALERT/GPI0R0
<36>	LPC_LFRAME#	<<>	LPC_LFRAME#	AV12	LFRAME		SMBCLK
							SMBDATA
							SMLTALERT/PCHPHOT/GPI073
<27>	PCH_SPI_CLK	<<>	PCH_SPI_CLK	AA3	SPI_CLK		CL_CLK
			PCH_SPI_CS0#	Y7	SPI_CS0		CL_DATA
			PCH_SPI_CS1#	Y4	SPI_CS1		CL_RST
			PCH_SPI_CS2#	AC20	SPI_CS2	SPI	
<27>	PCH_SPI_CS2#	<<>	PCH_SPI_DO	AA2	SPI_CS2#		
<27>	PCH_SPI_DO	<<>	PCH_SPI_DIN	AA1	SPI_MOSI	C-LINK	
<27>	PCH_SPI_DIN	<<>	PCH_SPI_DQ0	Y6	SPI_MISO		
			PCH_SPI_DQ3	AX1	SPI_IO2		



PCIECLK for UMA



PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA



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CPU (2/12)

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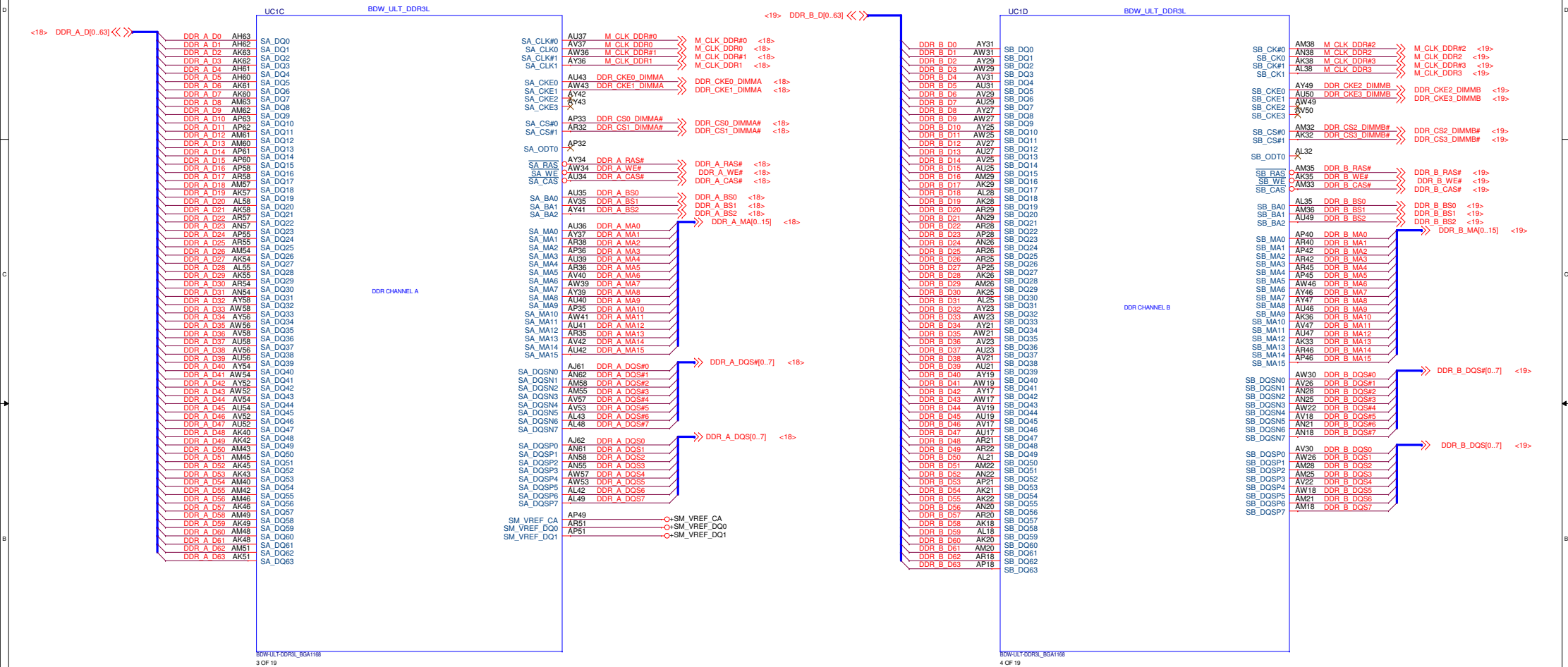
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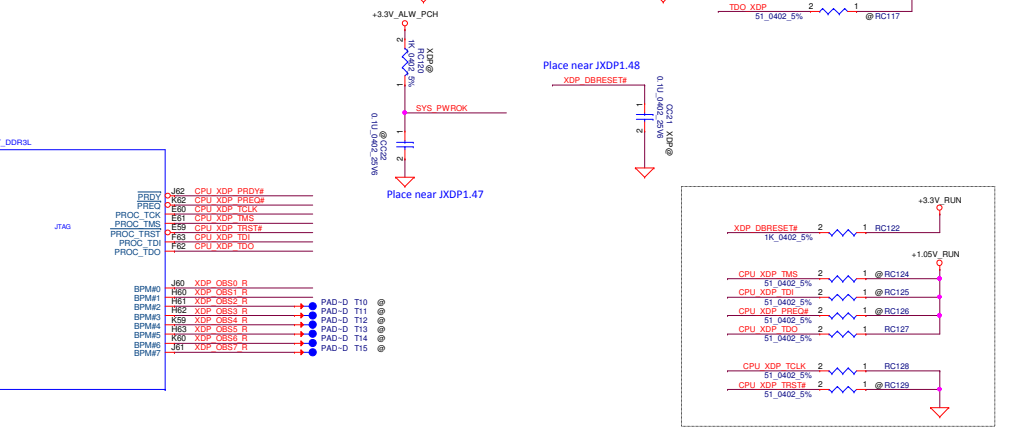
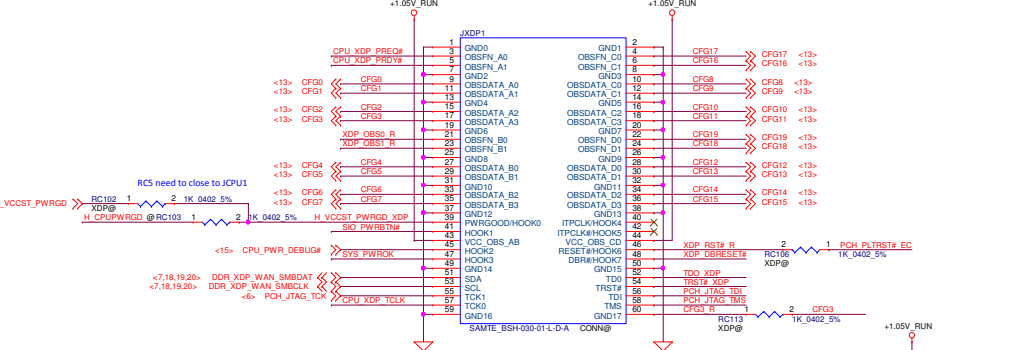
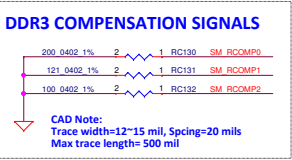
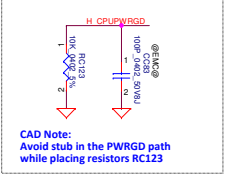
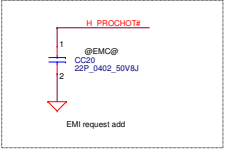
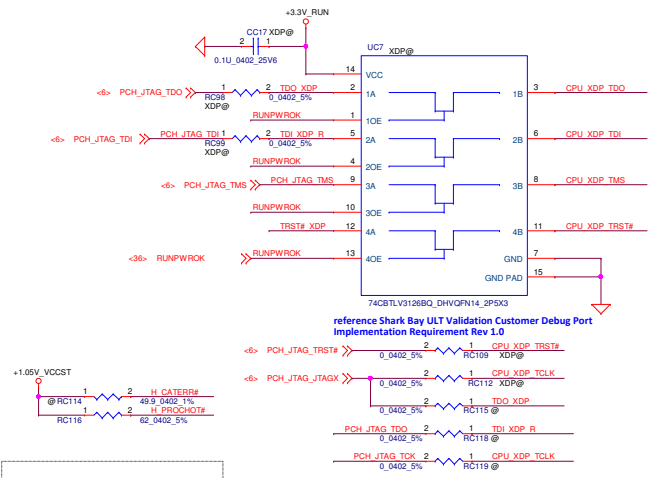
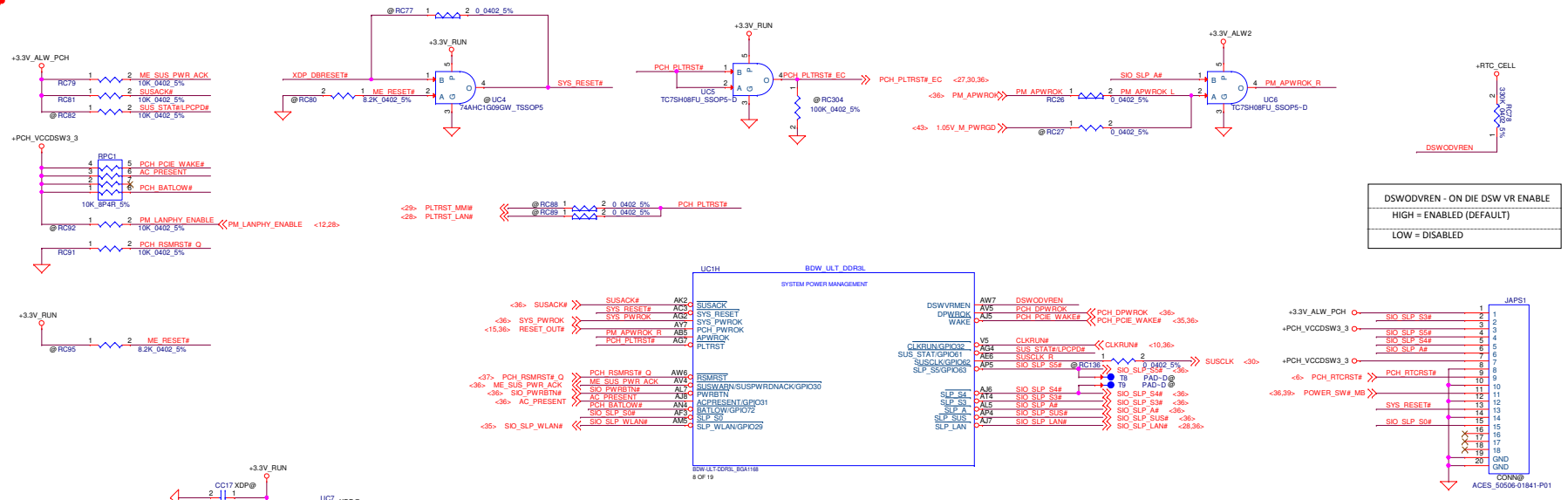
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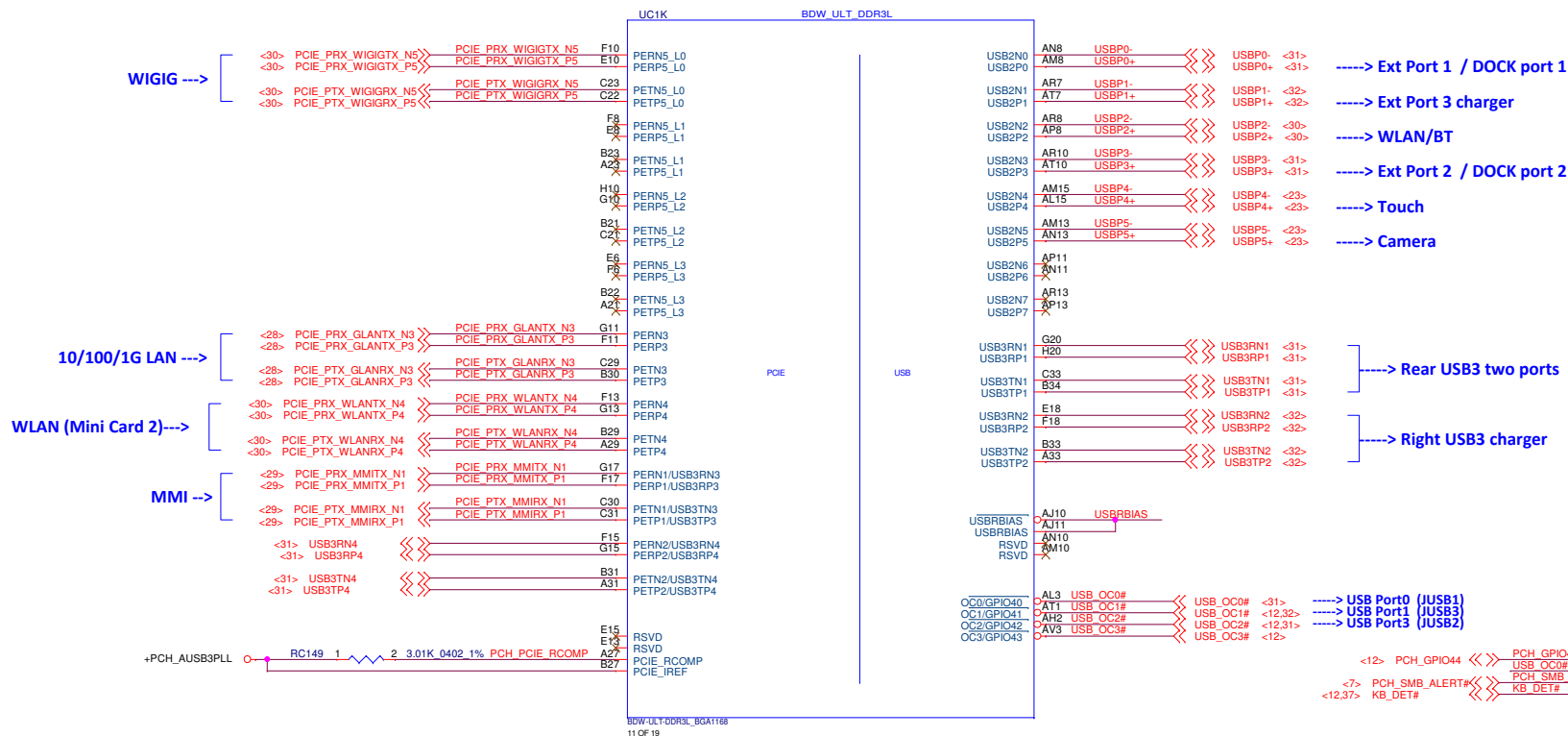
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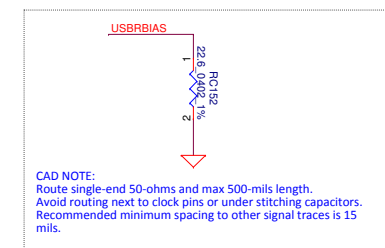


PCIE for UMA



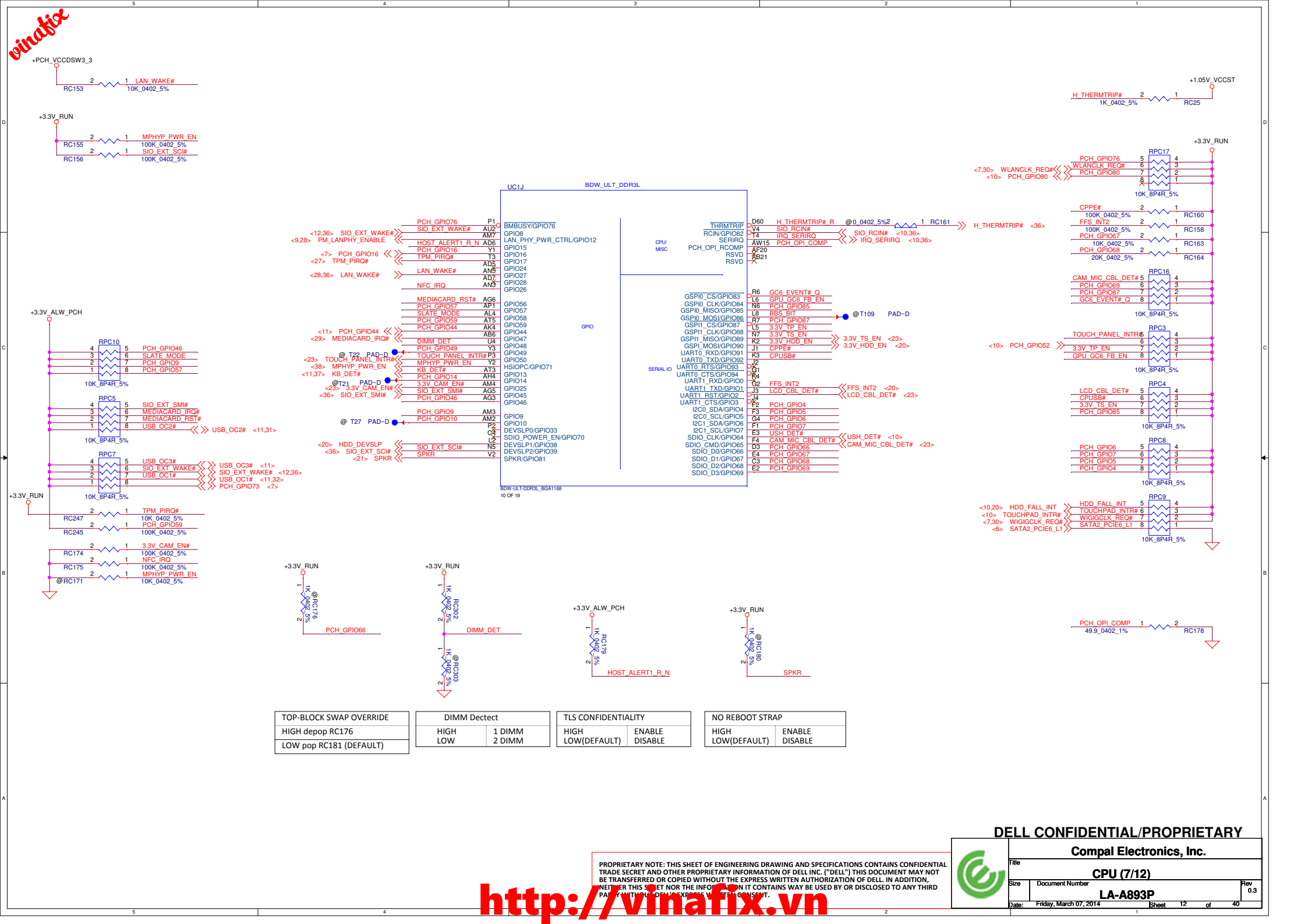
PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	Express

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card



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TOP-BLOCK SWAP OVERRIDE	
HIGH depop RC176	
LOW pop RC181 (DEFAULT)	

DIMM Detectect	
HIGH	1 DIMM
LOW	2 DIMM

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

NO REBOOT STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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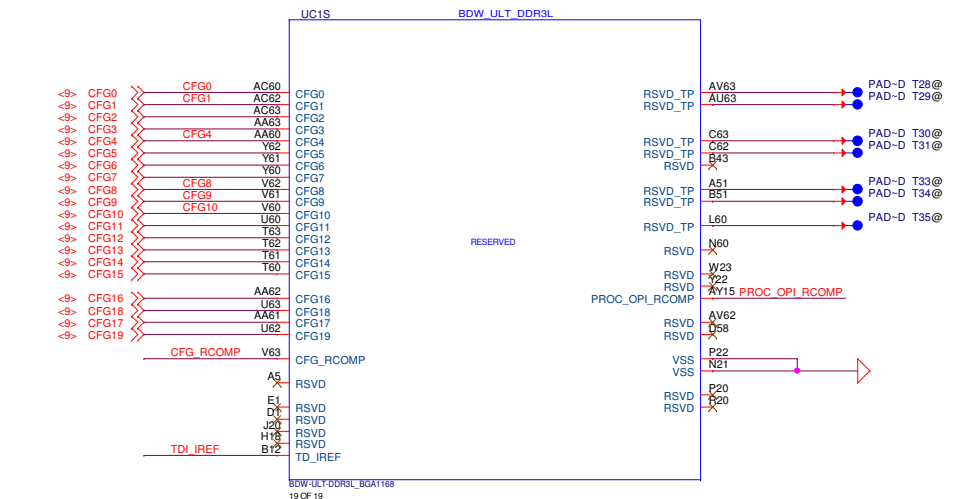
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CPU (7/12)

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CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

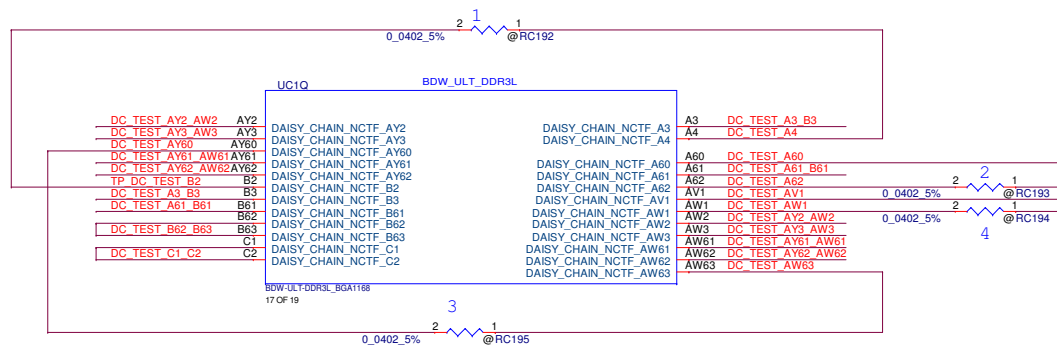
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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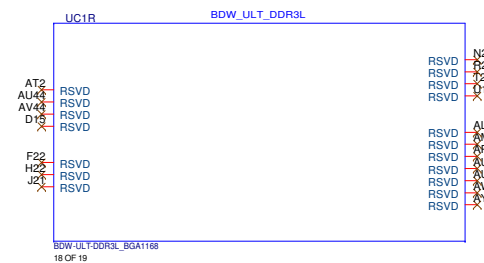
Compal Electronics, Inc.		
Title		
CPU (8/12)		
Size	Document Number	Rev
	LA-A893P	0.3
Date:	Friday, March 07, 2014	Sheet 13 of 40

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Package Daisy Chain:

- 1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
- 2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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Title: **CPU (9/12)**

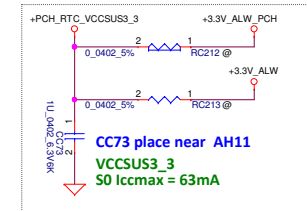
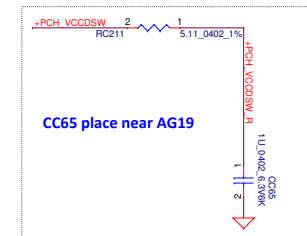
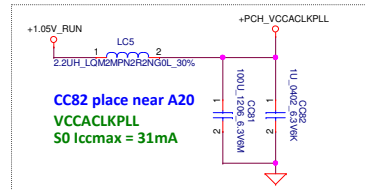
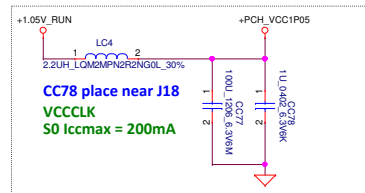
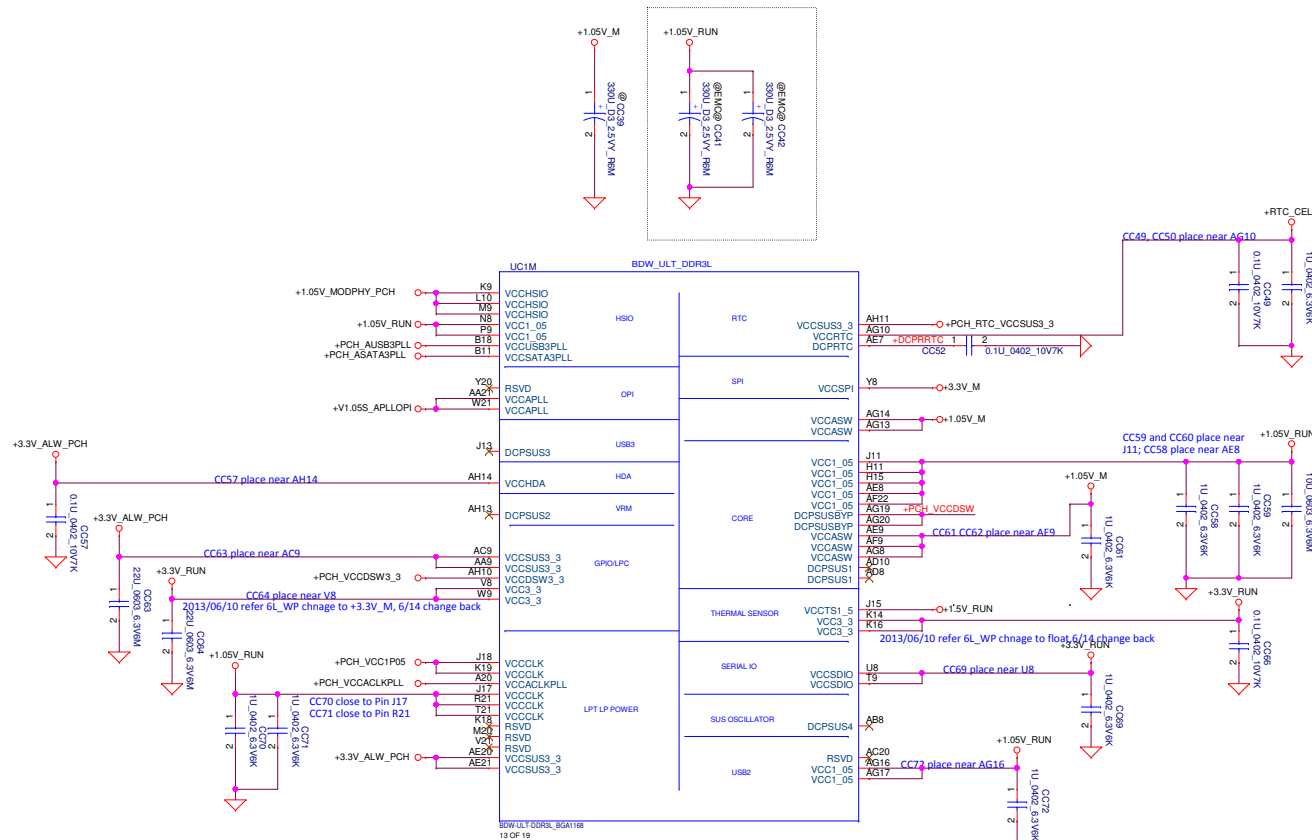
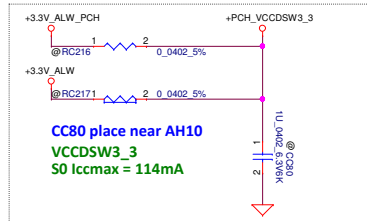
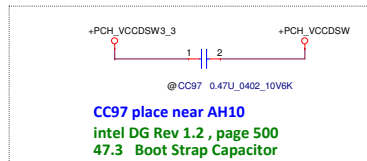
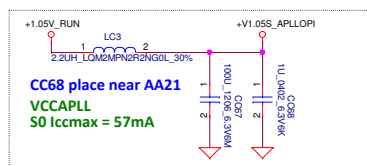
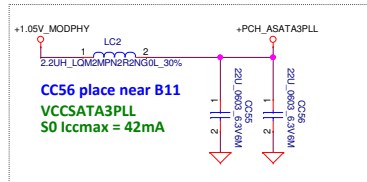
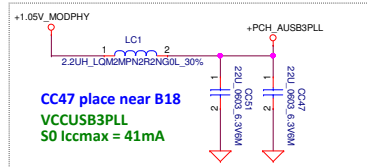
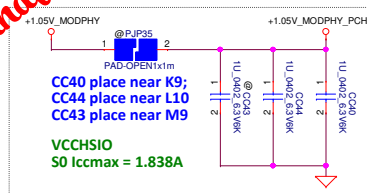
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Date: Friday, March 07, 2014

Document Number: **LA-A893P**

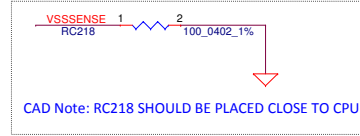
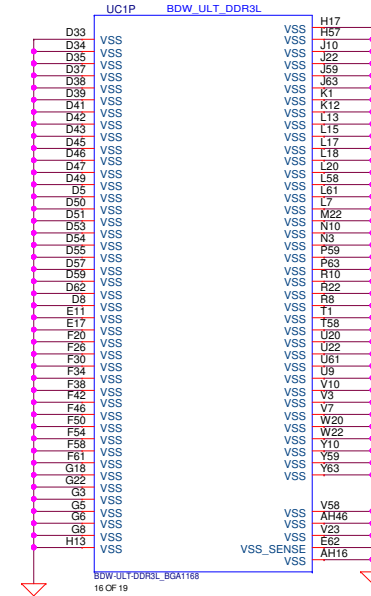
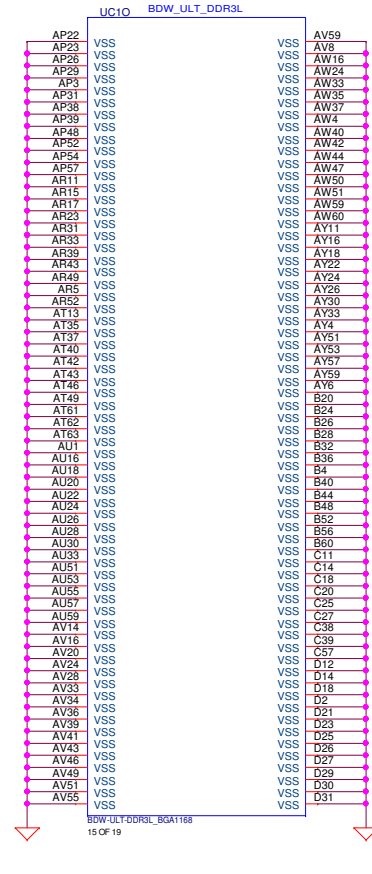
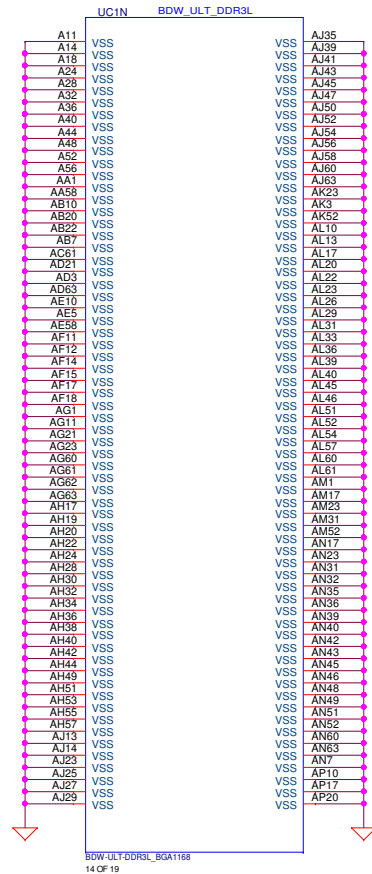
Rev: **0.3**

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Voltage Rail	Voltage (V)	S0 Iccmax Current (A) ³	Sx Iccmax Current (A) ³	Deep Sx Iccmax (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSU3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSU3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μ A See Note 1, 2

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CPU (12/12)

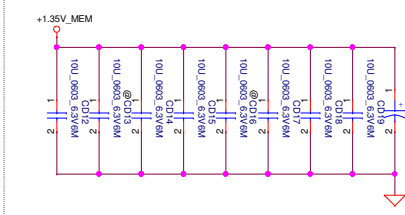
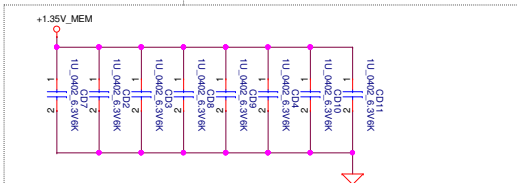
LA-A893P

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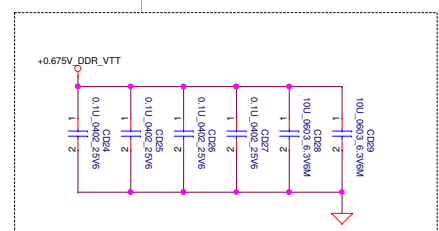
Rev 0.3

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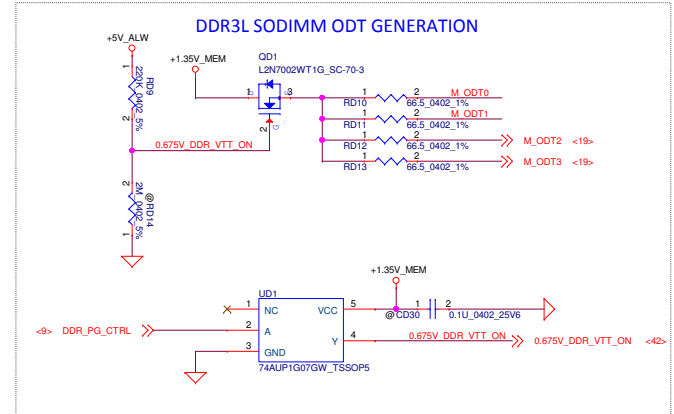
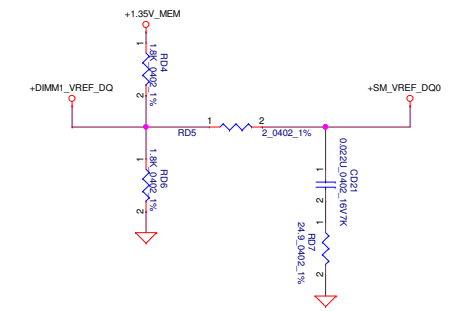
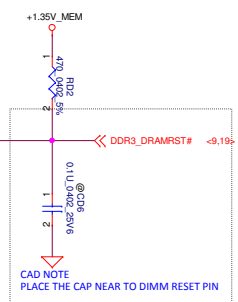
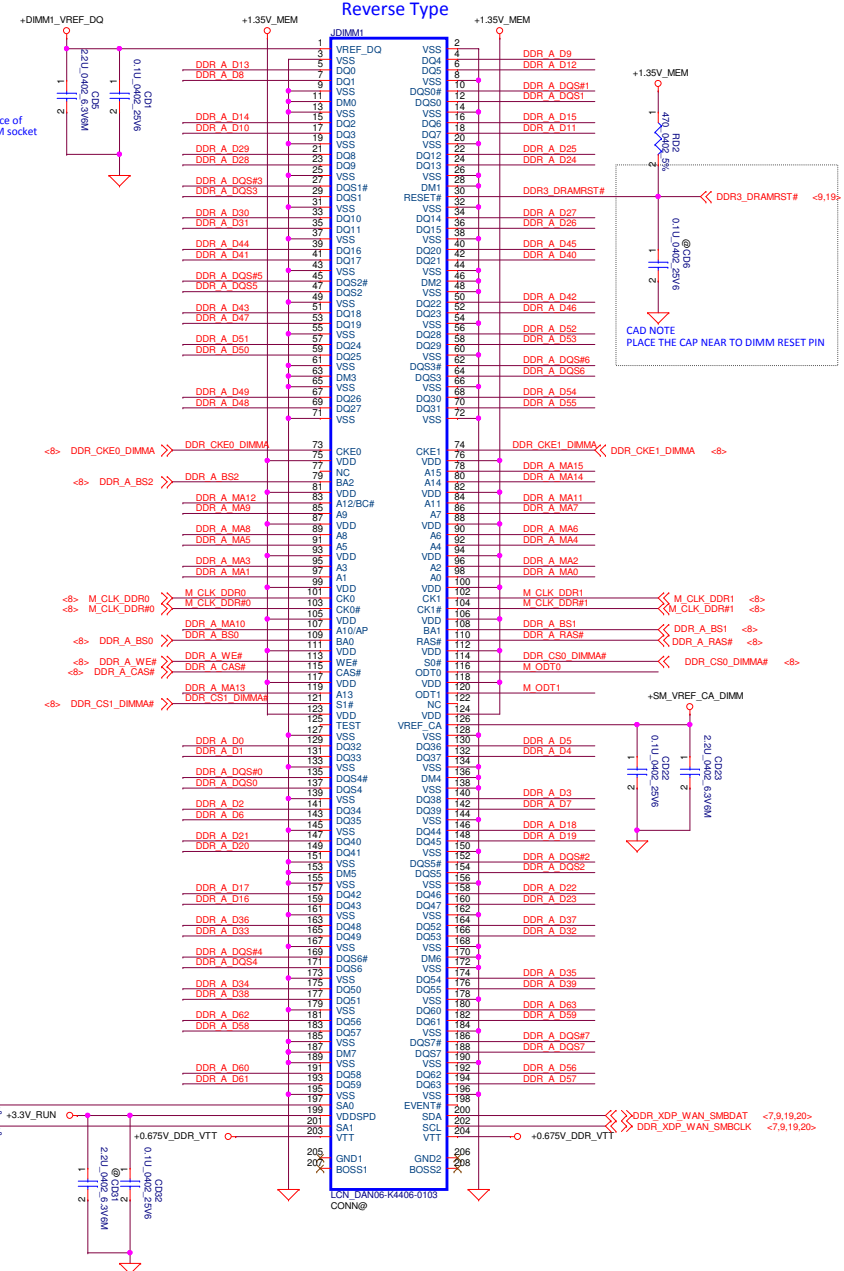
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



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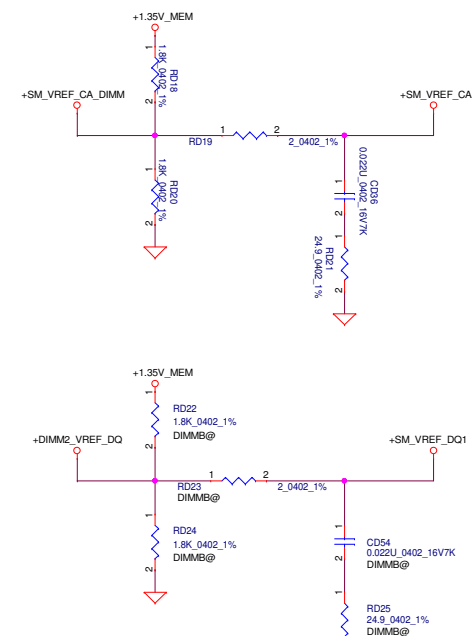
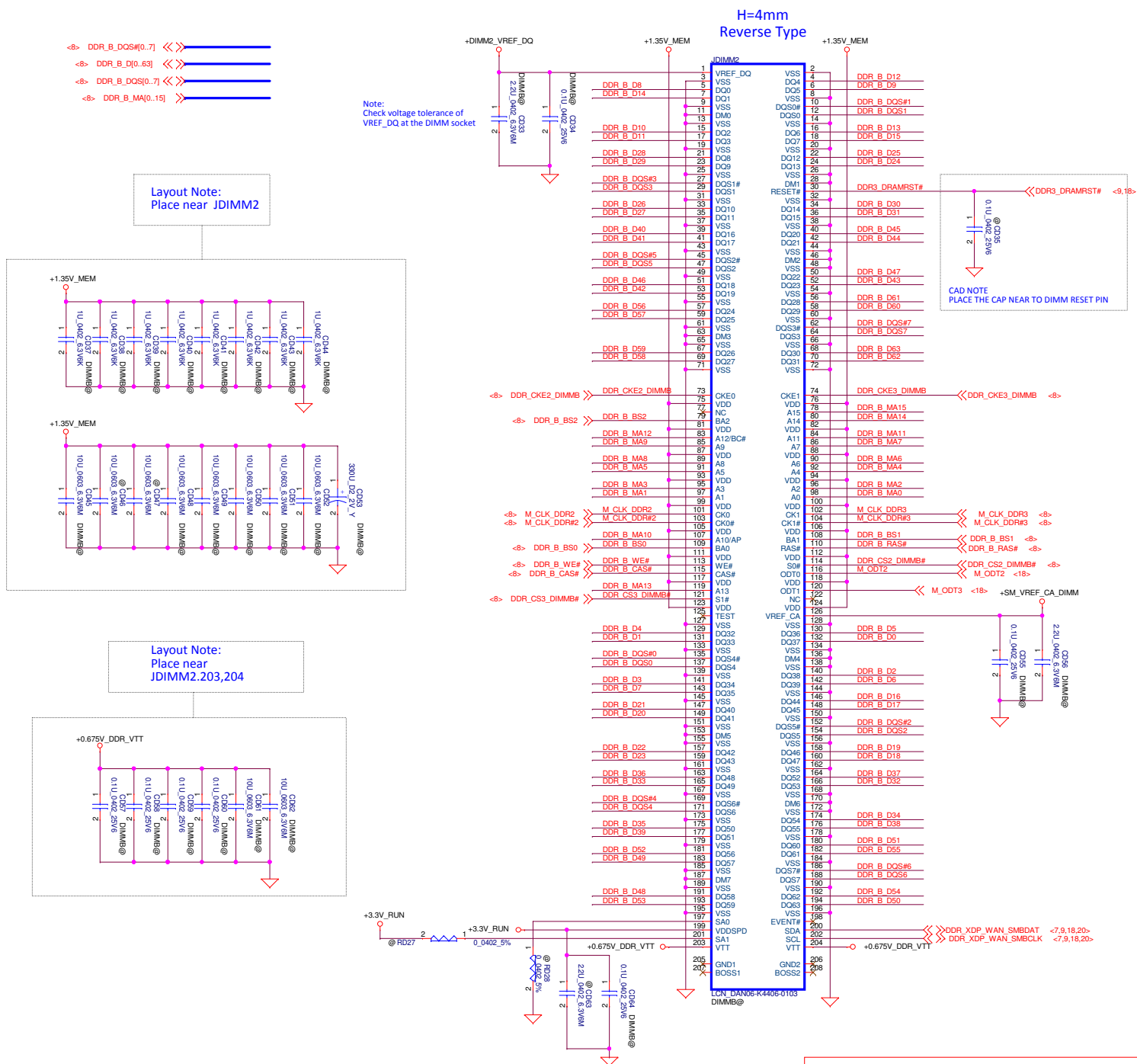
DDR3L

LA-A893P

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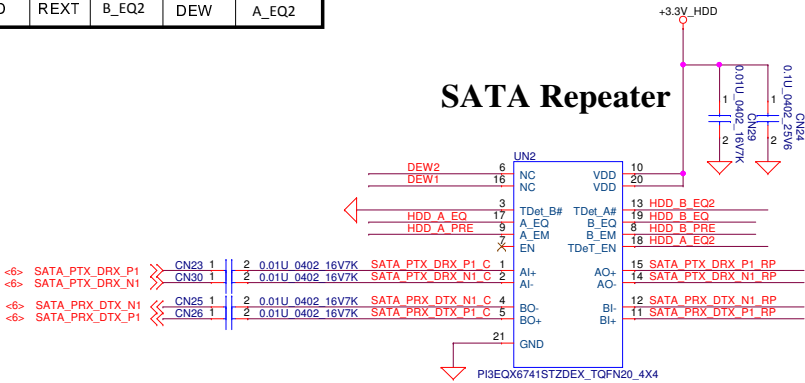
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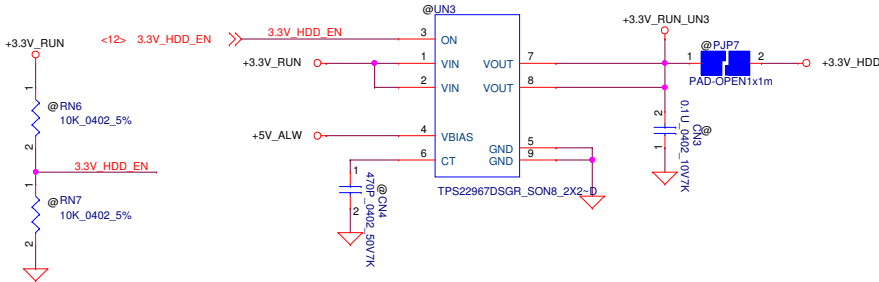
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDet_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater



			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -6dB -3dB	0dB -6dB -3dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB	0 M 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB			
		M M	12.2dB	12.2dB			
		M 0	9.4dB	9.4dB			
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
1 1	5dB	5dB					



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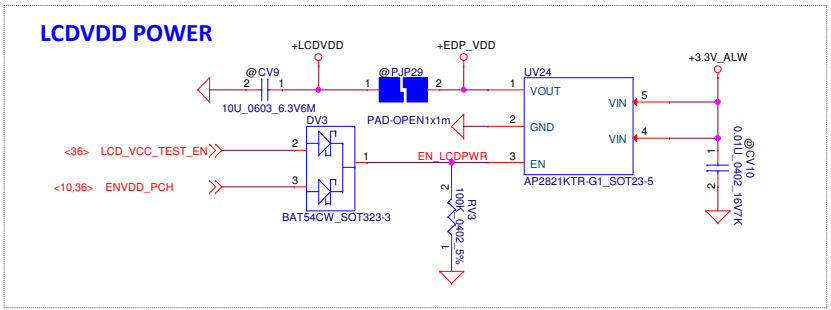
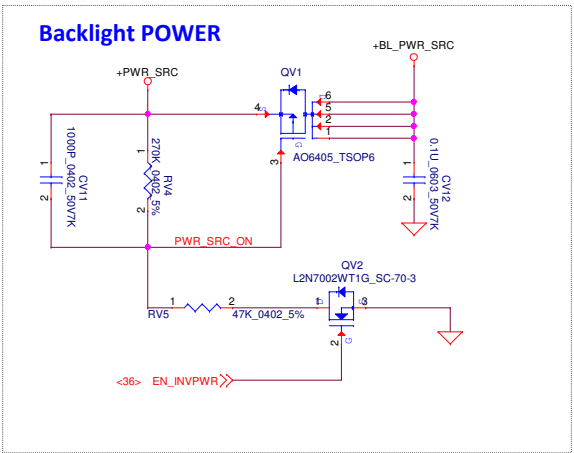
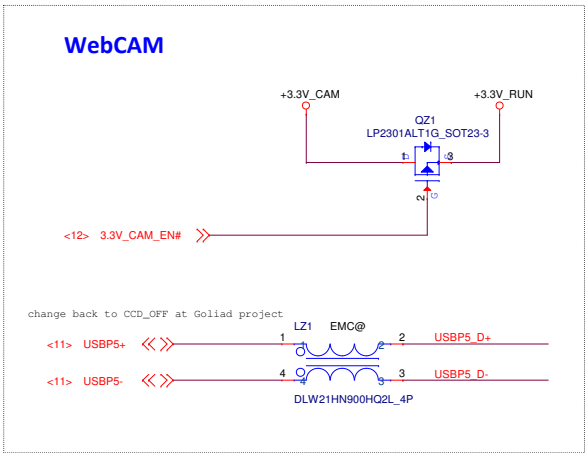
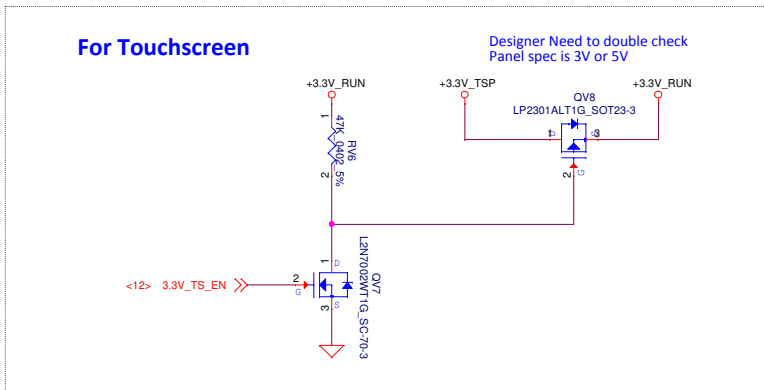
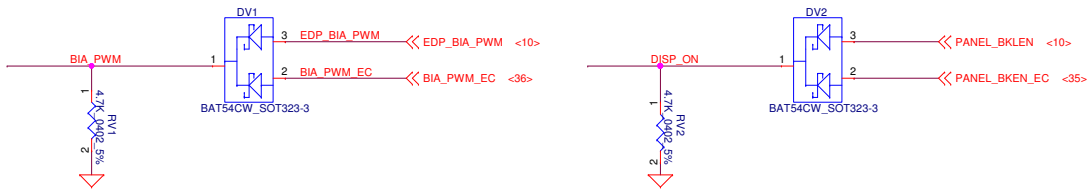
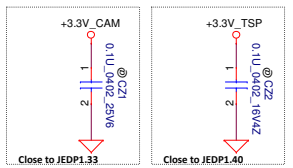
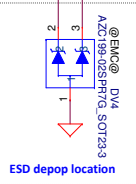
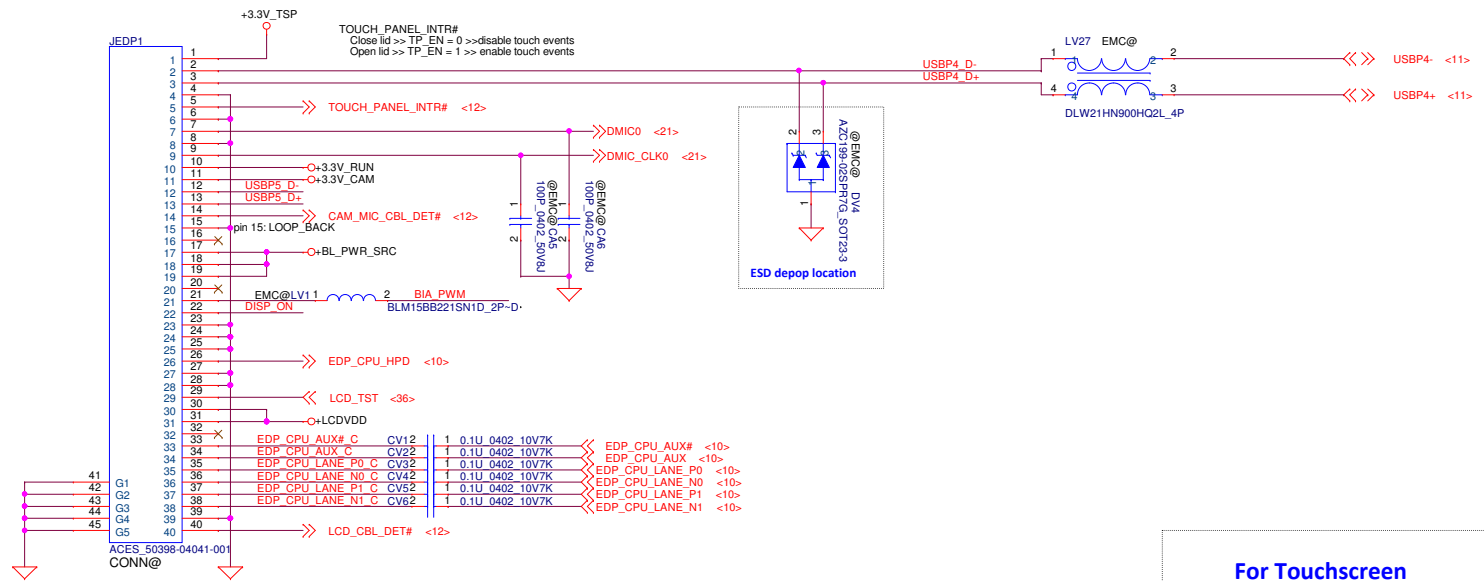


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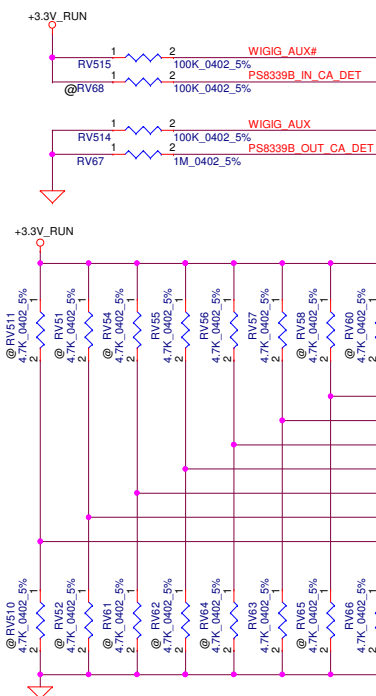


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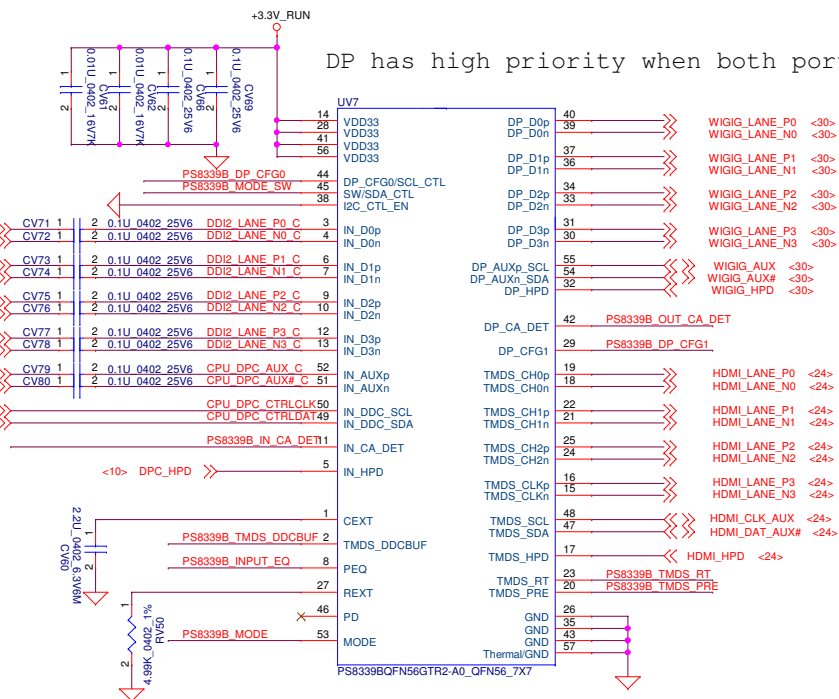
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eDP CONN & Touch screen			
LA-A893P			
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PCB	DP SWITCH
H12 UMA	PS8338+PS8339
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338



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 <10> DD12_LANE_N0
 <10> DD12_LANE_P1
 <10> DD12_LANE_N1
 <10> DD12_LANE_P2
 <10> DD12_LANE_N2
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 <10> CPU_DPC_CTRLCLK#
 PS8339B_TMDS_DDCBUF
 PS8339B_INPUT_EQ
 PS8339B_MODE
 PS8339B_TMDS_PRE
 PS8339B_TMDS_RT
 PS8339B_DP_CFG1
 PS8339B_DP_CFG0
 PS8339B_MODE_SW



DP has high priority when both ports plugged

Dock has higher priority

MODE = L: Control Switching Mode, HDMI ID disable
 = H: Automatic Switching Mode, HDMI ID disable
 = M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
 = H: 1.5dB pre-emphasis
 = M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
 = H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
 = H: DDC active buffer
 = M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 = H: HEQ, compensate channel loss up to 15dB @ HBR2
 = M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
 = H: auto test enable & input offset cancellation enable
 = M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
 = H: automatic EQ disable & AUX interception enable
 = M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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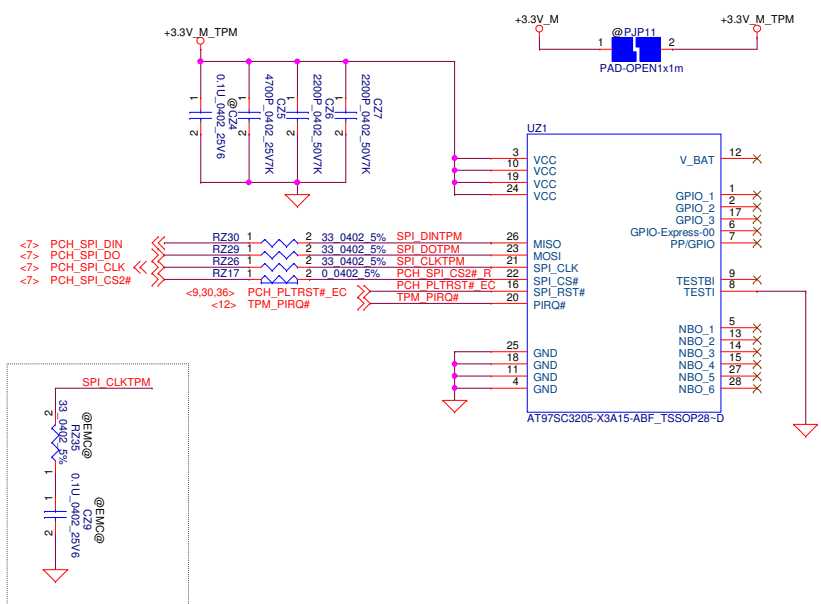
Compal Electronics, Inc.		
Title DP SW		
Size	Document Number LA-A893P	Rev 0.3
Date	Friday, March 07, 2014	
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Houston 12 Entry Configure needn't PS8338

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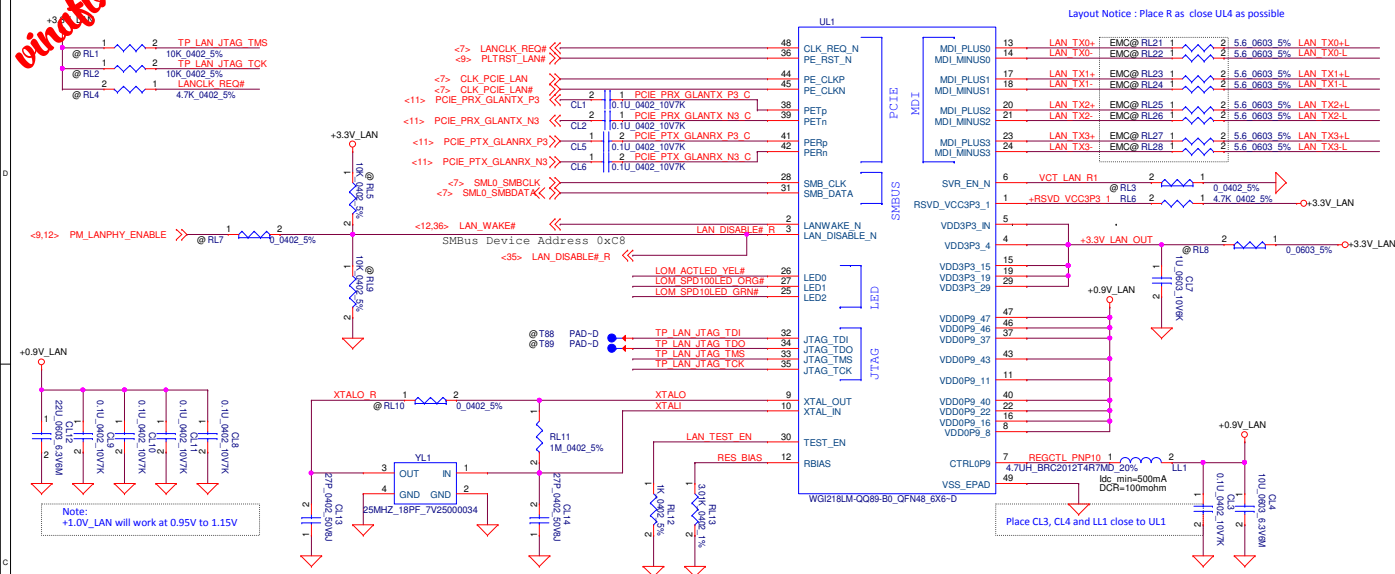
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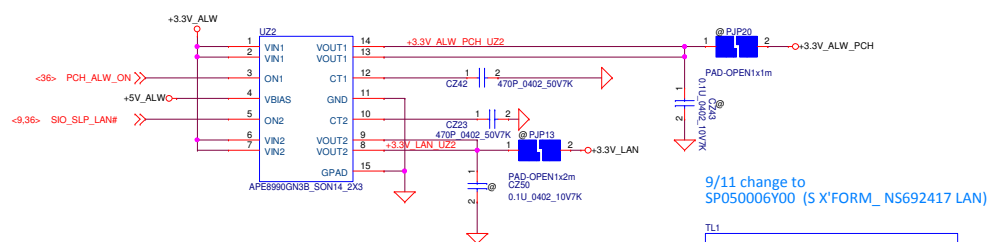


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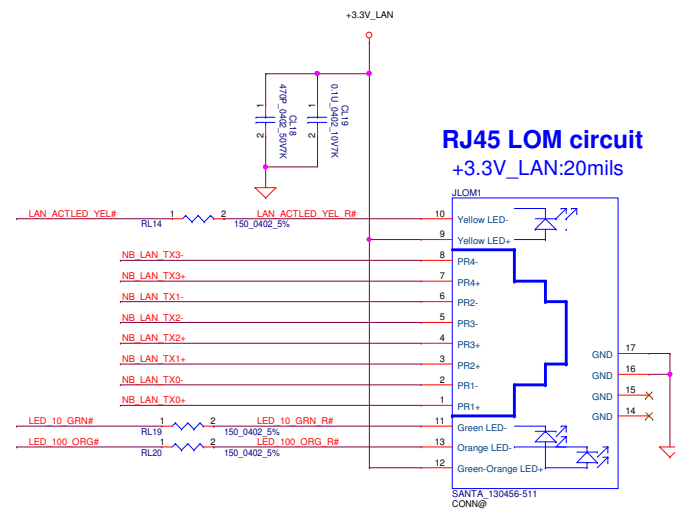
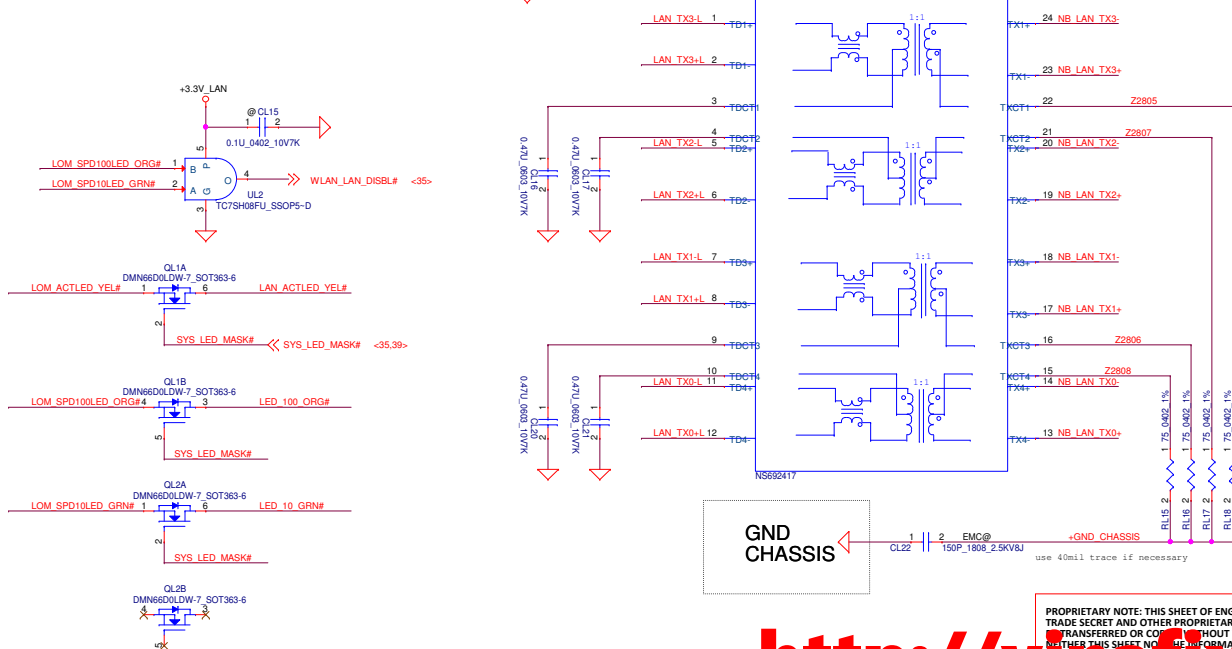
vinatix



+3.3V_ALW_PCH/+3.3V_LAN



9/11 change to
SP050006Y00 (S X'FORM NS692417 LAN)



RJ45 LOM circuit
+3.3V LAN:20mils

SANTA_130456-511
CONN@

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LAN

LA-A992B

Rev
0.3

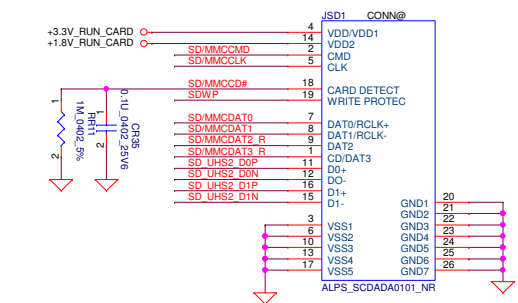
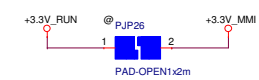
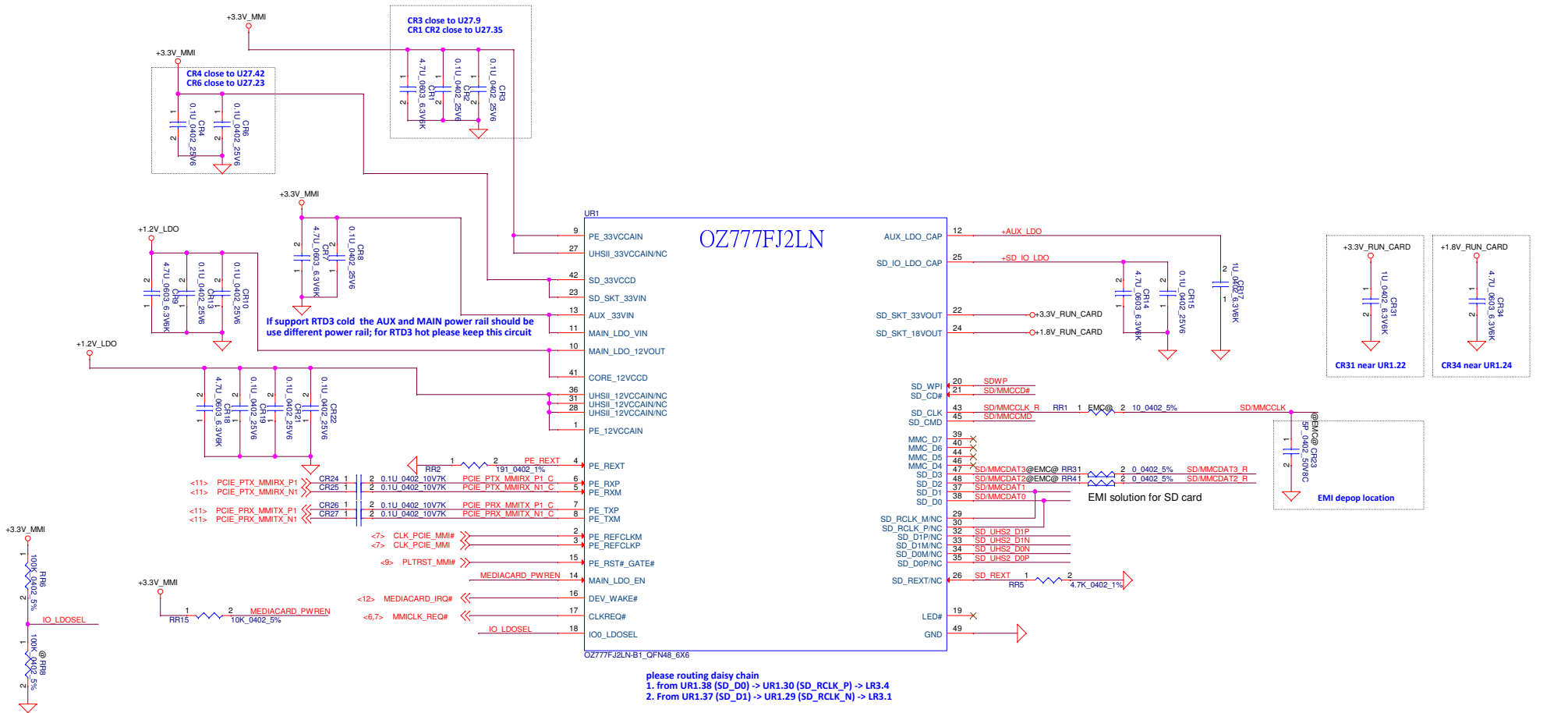
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Compal Electronics, Inc.

Card Reader

LA-A893P

Date: Friday, March 07, 2014

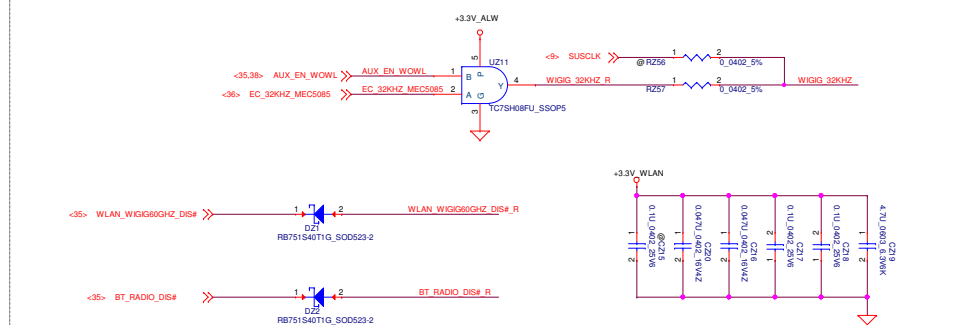
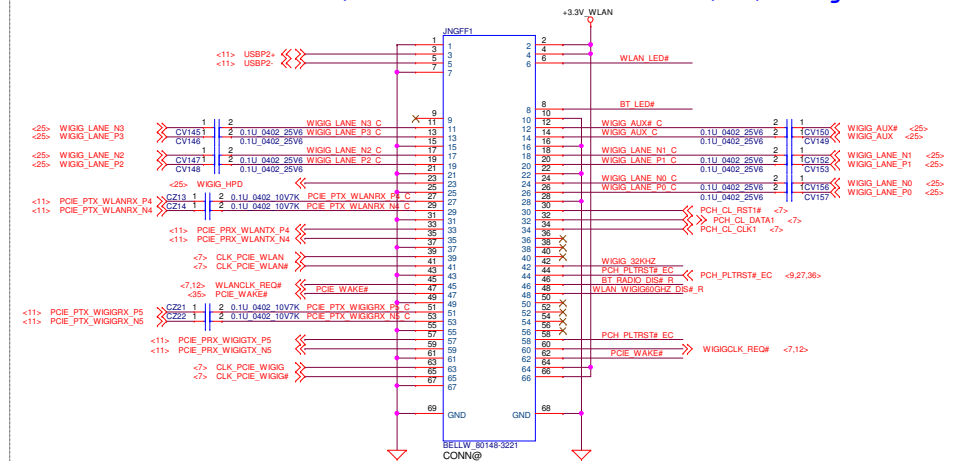
Sheet 29 of 40

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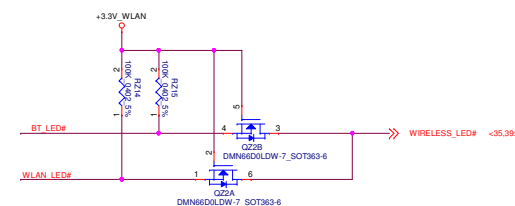
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M.2 (Card. Type 3030, Mechanical Key A) -WLAN/BT Combo or TriBand WLAN/BT/WiGig



LED control circuit



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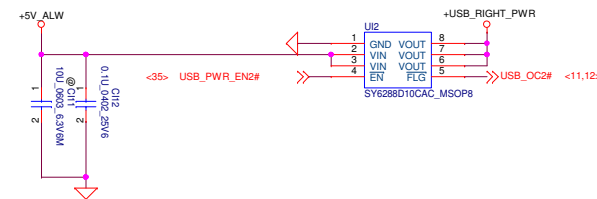
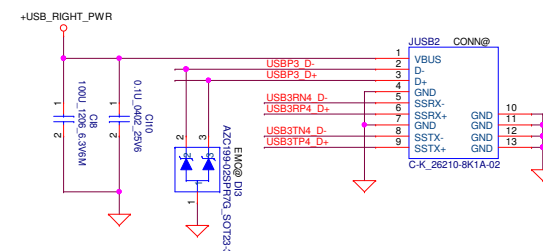
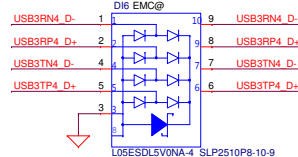
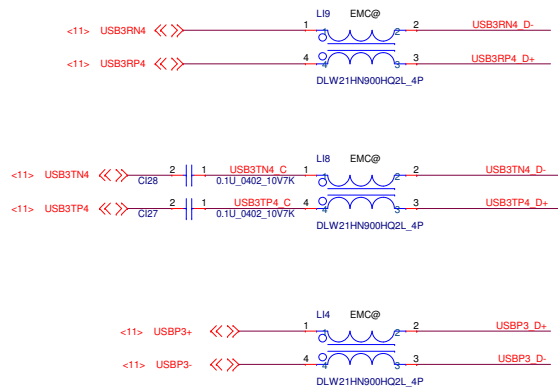
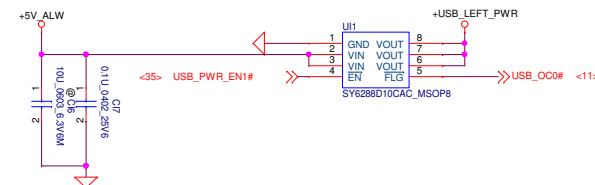
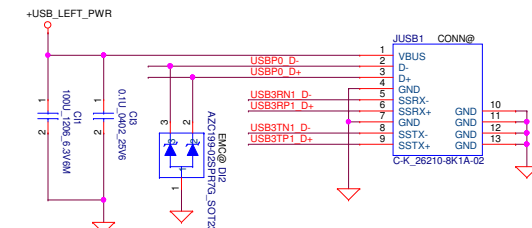
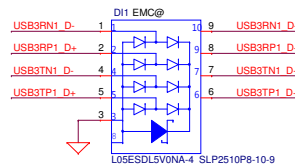
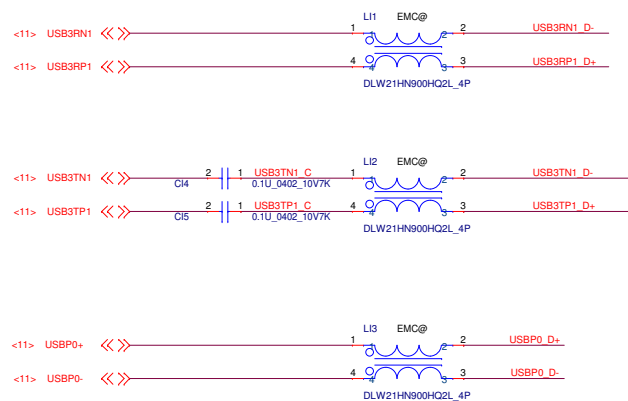


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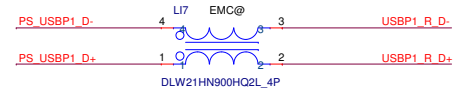
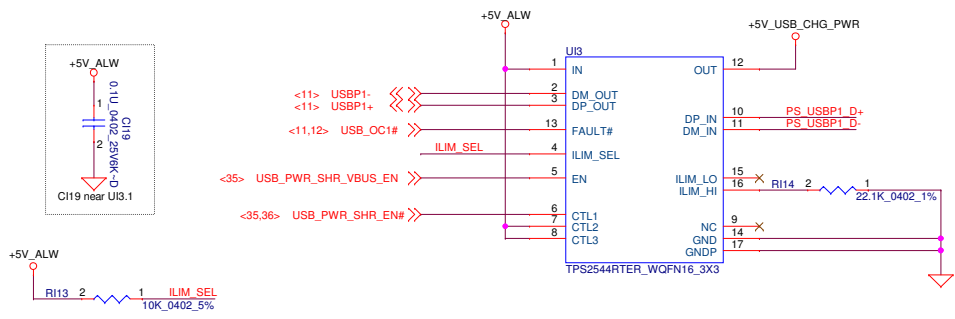
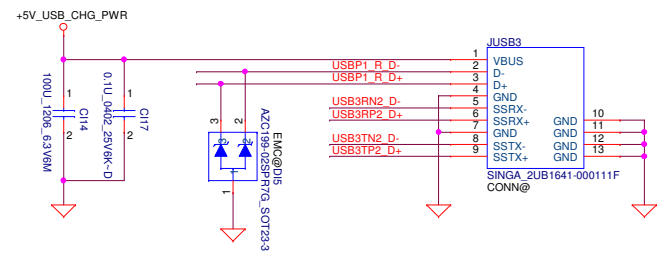
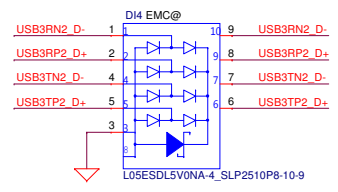
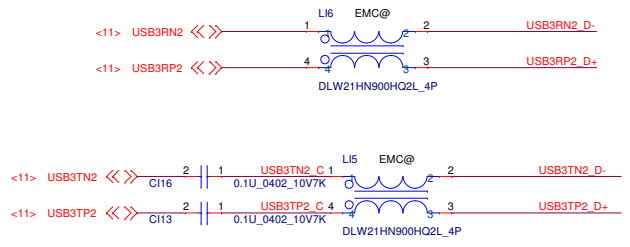
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File	USB3.0		
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USB SW			
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Houston 12 doesn't support NFC

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Title			
NFC			
Size	Document Number		Rev
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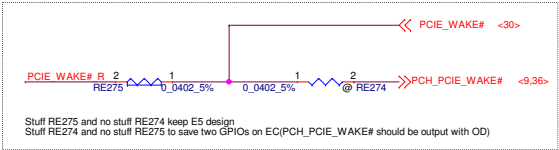
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Houston 12 Entry Configure doesn't support Dock

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E-Dock		
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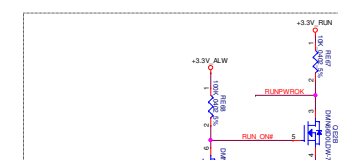
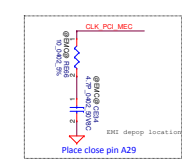
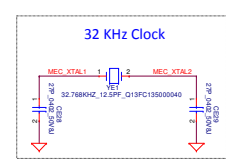
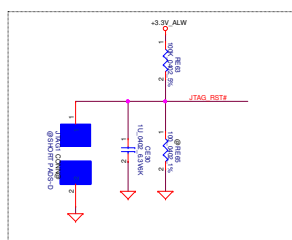
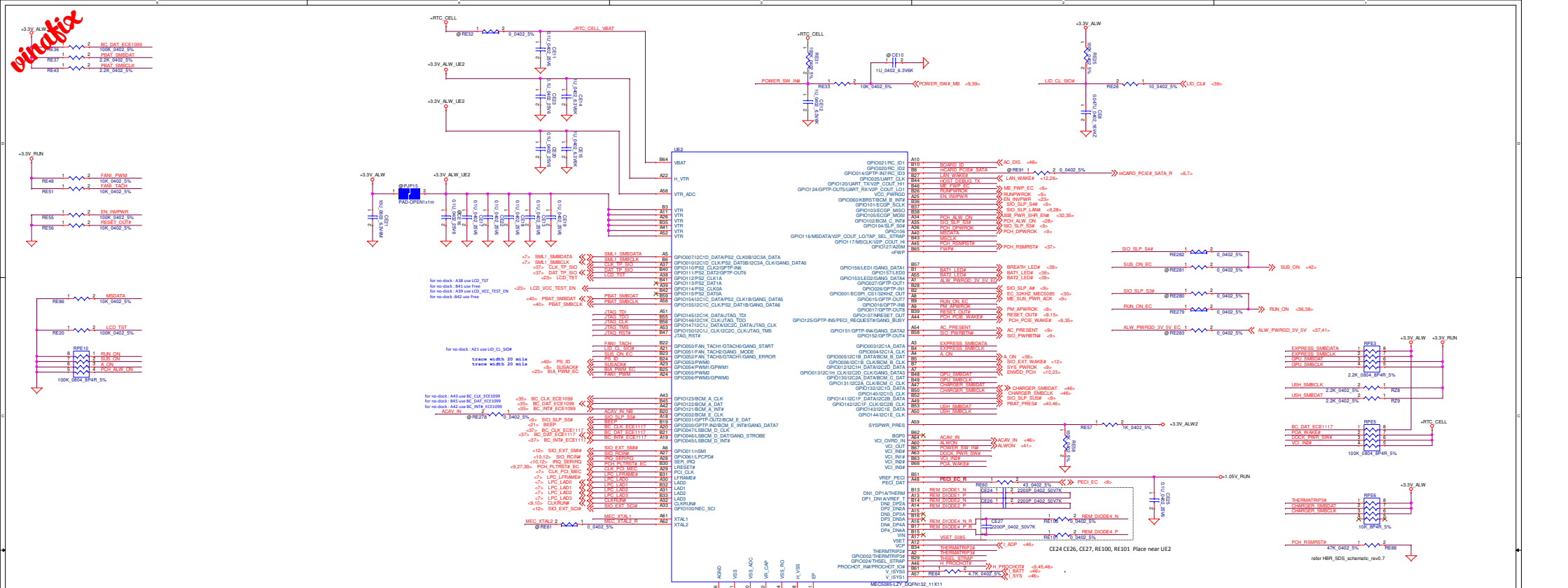


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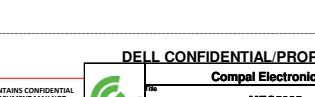
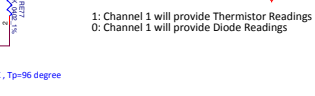
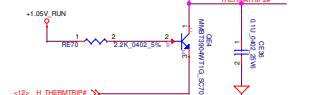
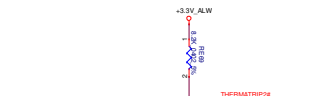
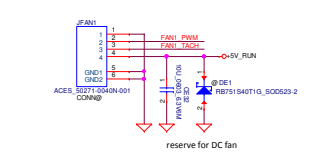
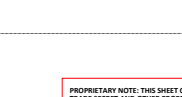
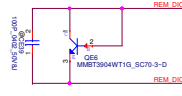
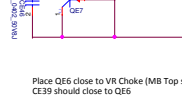
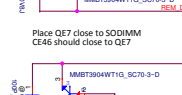
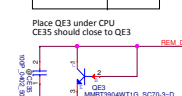
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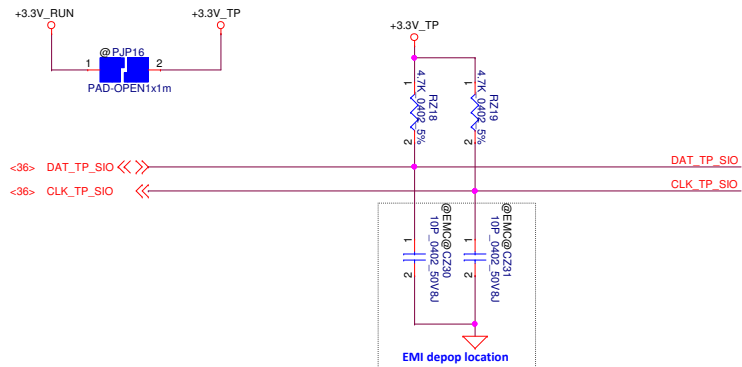
Setting for Thermal Design

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DP2/DN2a	WLAN
DP4/DN4	V.R

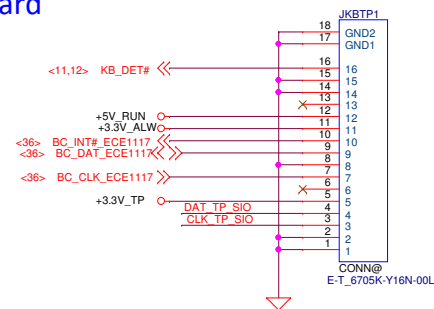


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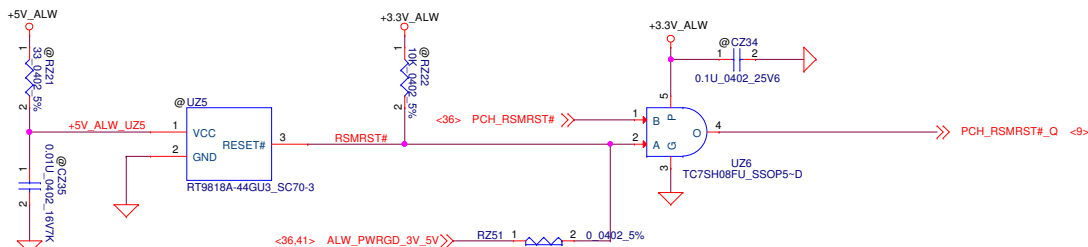
Touch Pad



Keyboard



RSMRST circuit



@IO FFC

Part Number	Description
DA30000GZ00	FFC 0VN LF-9591P REV0 M/B-IO/B

@eDP TS Cable

Part Number	Description
DC02C004S00	H-CONN SET 0VN MB-LCD-LED-CAM-TS

@eDP Cable

Part Number	Description
DC02C004T00	H-CONN SET 0VN MB-LCD-LED-CAM

@SATA Cable

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@MEDIA Board FFC

Part Number	Description
NBX0001CW00	FFC 8P G P0.5 PAD0.3 50MM MB-MEDIA/B 0VN

@KBTP FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@NFC Board FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@USH Board FFC

Part Number	Description
NBX0001CY00	FFC 20P G P0.5 PAD=0.3 75MM MB-USH/B 0VN

@FP FFC

Part Number	Description
NBX0001D100	FFC 6P G P0.5 PAD=0.3 75MM USH/B-FP 0VN

@Speak

Part Number	Description
FK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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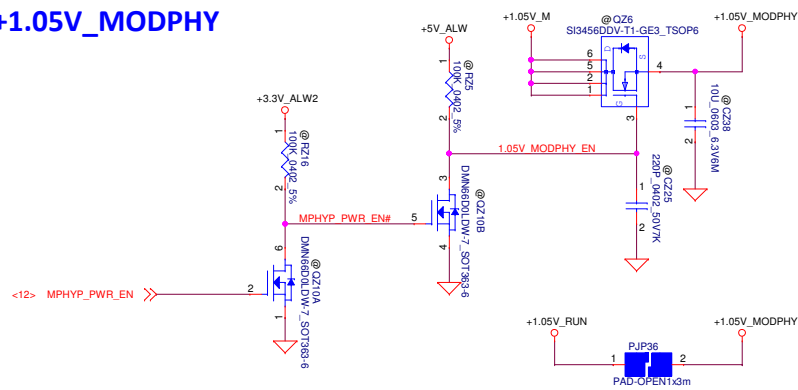
Keyboard

LA-A893P

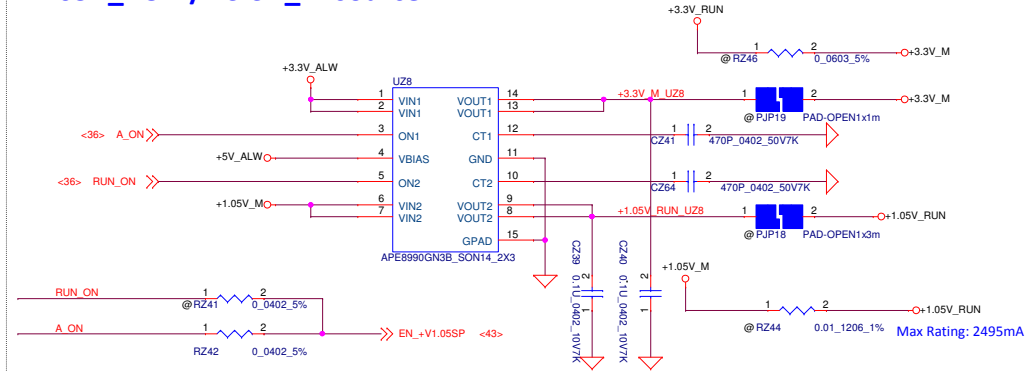
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Size	Document Number
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+1.05V_MODPHY

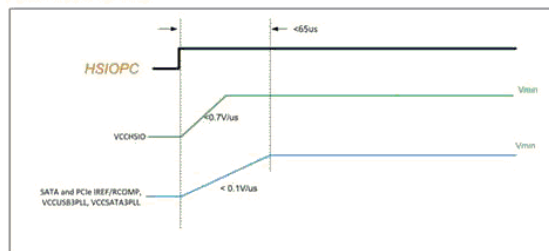


+1.05V_RUN / +3.3V_M source

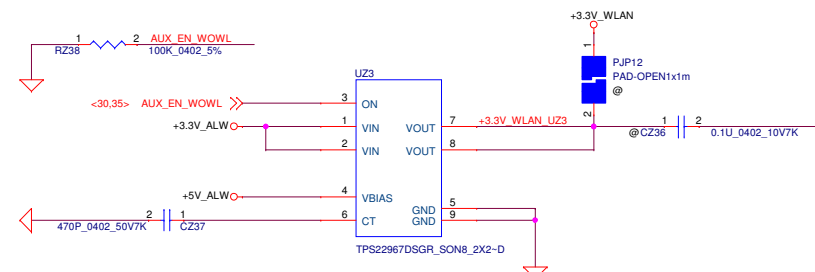


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

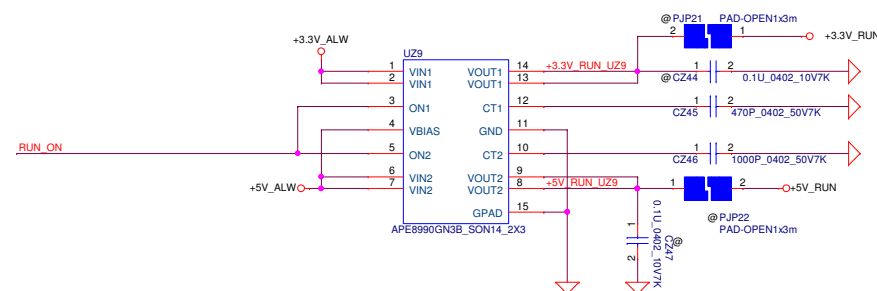
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



+3.3V_WLAN source



+3.3V_RUN/+5V_RUN source



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Power control

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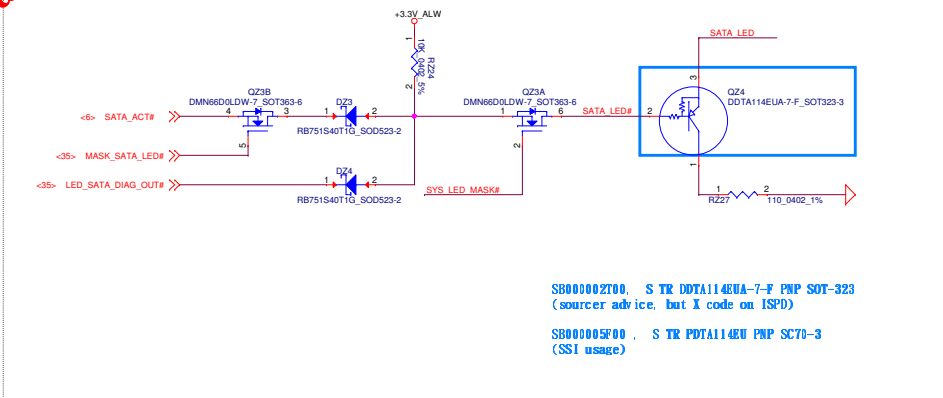
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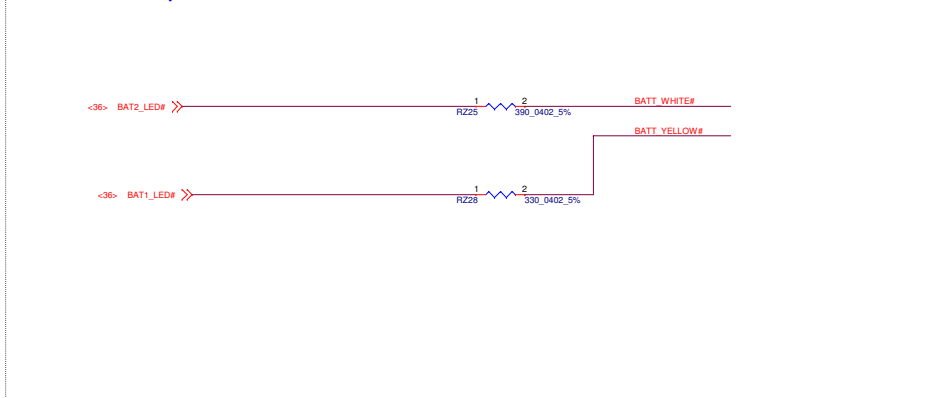
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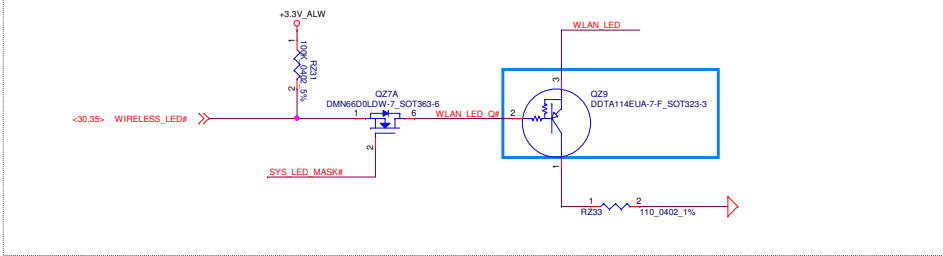
LED solution for White LED



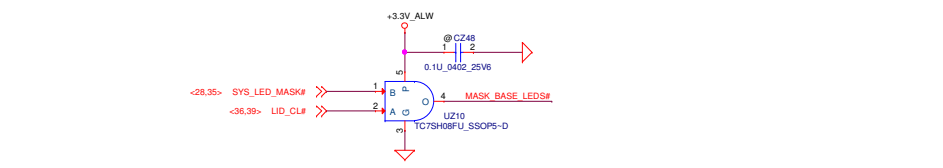
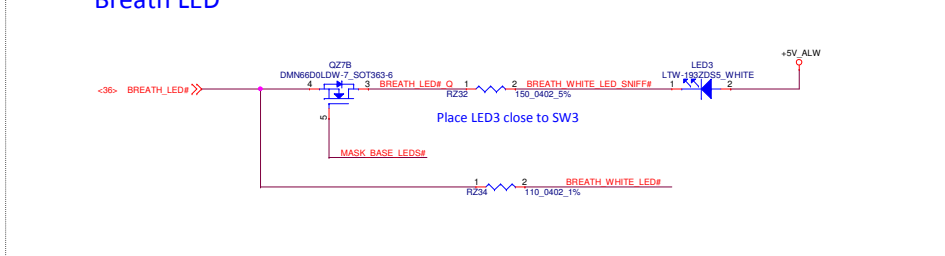
Battery LED



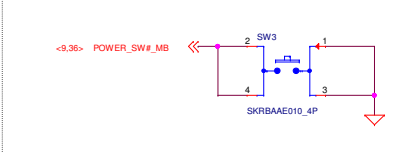
WLAN LED solution for White LED



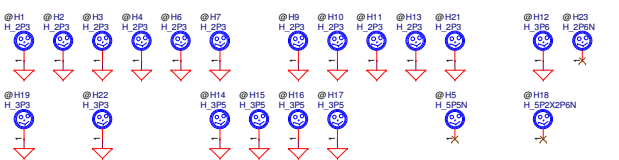
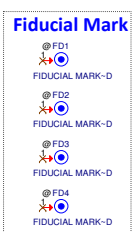
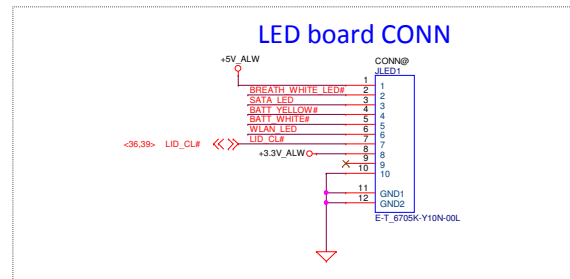
Breath LED



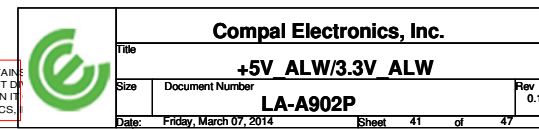
POWER & INSTANT ON SWITCH



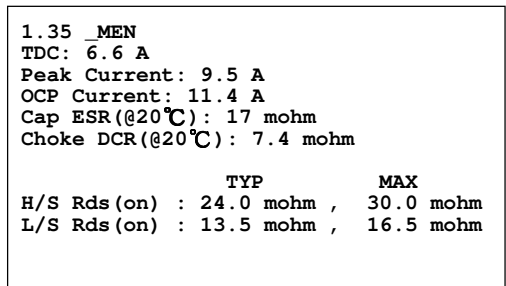
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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```
0.675 Volt
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A
```



Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

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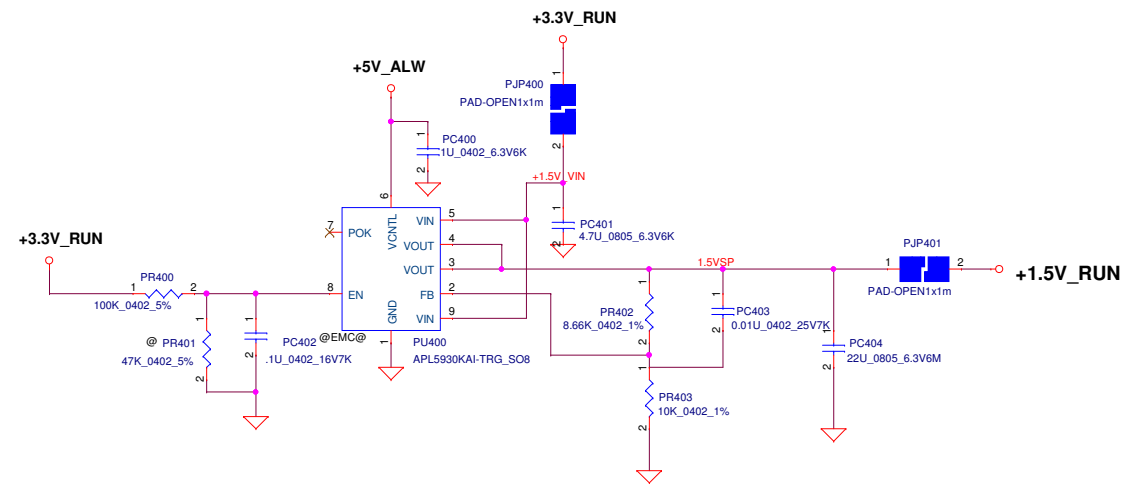
+1.35V_MEN/+0.675V_DDR_VTT

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+1.5V_RUN
TDC: 0.47 A
Peak Current: 0.67 A



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Title			
+1.5VSP			
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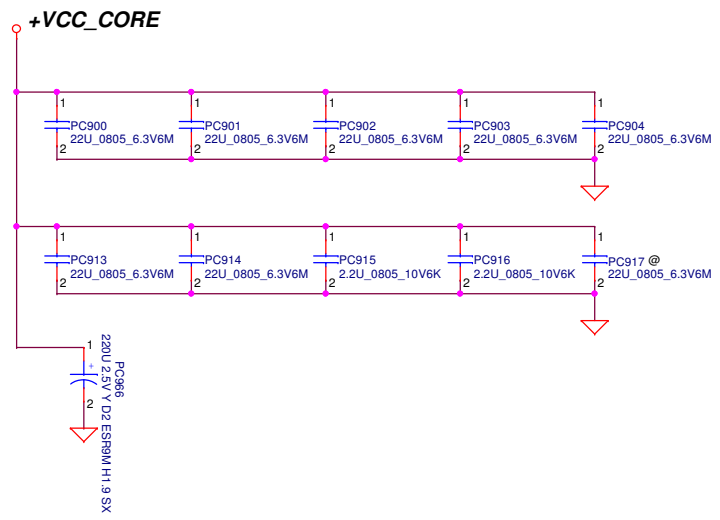
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828) PR71



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	PROCESSOR DECOUPLING				
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version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
2	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
3	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR715, PR729 to 154k	X01
4	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
5	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
6	ALL	ALL	10/31	Compal	RF request	Pop PR522, PC508, PR726, PC721, PC713, PL501, PC520	X01
7	46	Charger	12/05	Compal	Has the same behavior with dock circuit	Add PQ711	X01
8	46	Charger	12/05	Compal	To add 2nd source	Remove PQ702 Add PQ709, PQ710	X01
9	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
10	46	Charger	3/03	Compal	To set OVP level	Remove PR729	X02
11	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
12	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
13	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. add QV20,CZ69,RV210,RV212,QV21 external FET switch circuit 7. UV8 pin B5, B6 change to +3.3V_RUN_VMM 8. LP_CTL add RV516, 2.2K resistor PU to +3.3V_RUN_VMM 9. Depop RV73 10. add LP_EN on UV8.A5 (10/18) 11. depop QV20,CZ69,RV210,RV212, QV21 external FET switch circuit (10/24) 12.RPV2 pin1 & pin2 NC (11/4)	0.2 (X01)
5	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2 (X01)
6	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, , reserved RC27.	0.2 (X01)
7	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
8	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
9	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
10	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
11	7,38	HW	2013/10/17	COMPAL	for UMA DOCK configure, it support has non-VPRO configure.	add PJP33, PJP34 UC3, CC7, RC50, RC55, RPC12, UZ7, CZ64 change to VPRO@	0.2 (X01)
12	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
13	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	remove QZ5, QZ7.2 & QZ3.2 change to SYS_LED_MASK#	0.2 (X01)
14	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	add UN3, CN3, CN4, PJP7 and reserved it.	0.2 (X01)
15	30,36	HW	2013/10/17	COMPAL	follow Dell requirement.	add back SUS_ON, change +3.3V_SUS control pin to SIO_SLP_S4# 1. UL3.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282 (Pop), RE281 (depop) 4. add RE279, RE280 (dock only) 5. UE2.B9 → RUN_ON_EC	0.2 (X01)
16	23	HW	2013/10/18	COMPAL	follow ESD recommend.	LZ1 change from SM070001N00 to SM070003Y00	0.2 (X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4 to replace PCH_GPIO48, remove	0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	30	HW	2013/10/29	COMPAL	New SIM connector has no this pin.	remove UIM_DET on JNGFF2 pin58	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for Goliad, Houston doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ43, 100k pull up for WWAN_PWR_EN	0.2 (X01)
23	38	HW	2013/10/29	COMPAL	for support VPRO & NVPRO BOM option.	remove PJP33, PJP34, PJP19 add RZ44, RZ46, RZ47	0.2 (X01)
24	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
25	37	HW	2013/10/29	COMPAL	Dell request.	add RZ48, RZ49, QZ12 depop UZ5, UZ6, RZ21, RZ22, CZ35, RC91 (11/4) add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88 (11/4)	0.2 (X01)
26	25	HW	2013/10/29	COMPAL	DDC need pull high.	pop RV514 & RV515	0.2 (X01)
27	21	HW	2013/10/29	COMPAL	Follow RF team request	pop RA17, CA33, CA30, CA54 and Change CA33 from 10pF to 15pF	0.2 (X01)

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version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
28	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
29	28	HW	2013/11/04	COMPAL	SSI design will cause LED behavior error.	Change QL1, QL2 contorl pin from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)
30	21	HW	2013/11/04	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
31	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
32	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
33	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2 (X01)
34	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN9,RN11,RN13,RN16 pop 0ohm	0.2 (X01)
35	28	HW	2013/11/06	COMPAL	For EMI request	RL21~ RL28 change to 5.6 ohm	0.2 (X01)
36	29	HW	2013/12/17	COMPAL	Remove USH schematic on Entry config	1. remove +3.3V_SUS power rail,UZ3 change from TPS22966 to TPS22965 2. remove CL23, CL24, PJP 3. USH SMBUS change to PU +3.3V_RUN 4. Delete JUSH1,CZ10,CZ11,CZ12 5. remove RC87 (11/29 add) 6 make USBP6+ / USBP6- (11/29add) 7. remove BCM5882_ALERT# (11/29 add)"	0.3 (X01)
37	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3 (X01)
38	36 , 37	HW	2013/12/17	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2. remove QZ12,RZ48,RZ49,RZ50	0.3 (X01)
39	15	HW	2013/12/17	COMPAL	follow EMI request	pop CC23, CC79, CC84, CC85 add CC94, CC95, CC96	0.3 (X01)
40	28 , 39	HW	2013/12/17	COMPAL	Because TPS22965 is X1 code	For Dock, UN3,UZ7 change fron TPS22965 to SA000070S002. For Entry, UN3,UZ3 change from TPS22965 to SA000070S00	0.3 (X01)
41	36	HW	2013/12/17	COMPAL	add for thermal sensor debug	reserve RE100 & RE101	0.3 (X01)
42	19	HW	2013/12/17	COMPAL	add DIMMB@	add DIMMB@ for below loaction,CD33 ,CD34 ,CD37 ,CD38 ,CD39 ,CD40 , CD41 ,CD42 ,CD43 ,CD44 ,CD45 ,CD48 ,CD49 ,CD50 ,CD51 ,CD52 ,CD53 , CD54 ,CD55 ,CD56 ,CD57 ,CD58 ,CD59 ,CD60 ,CD61 ,CD62 ,CD64 , JDIMM2, RD22, RD23, RD24, RD25	0.3 (X01)
43	38	HW	2014/02/07	COMPAL	For no support MODPHY	1.PJP36 pin1 from +1.05V_M to +1.05V_RUN 2.depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.4 (X01)
44	36	HW	2014/02/07	COMPAL	EC request,for Delray common code reserved	Add RE283	0.4 (X01)
45	9, 16	HW	2014/02/07	COMPAL	Follow intel DG 1.2	Reserved 0.47uF between +PCH_VCCDSW3_3 and +PCH_VCCDSW Reserved RC92 to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE.	0.4 (X01)

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