Compal Confidential

MB Schematic Document

FH51M

LA-J871P

Rev:1.0

2020.02.11

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Compal Electronics, Inc.		
Title: Cover Sheet		
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mDP - JDP1
- VGA Port E
P.39

HDMI - JHDMI1
- VGA Port C
P.40

N18P-G61/G62
- MAX-Q
- GDDR6 4G
P.27-37

VBIOS ROM
- SOP8
- Size : 1M
P.29

eDP - JEDP1
- CPU eDP
P.38

DDI

PEG x16
8GT/s

CoffeeLake H Processor
BGA1440 (42X28)
(CFL-H & CML-H _ 8+2)
P.6-13

Memory BUS

Interleaved (DDR4 2400/2666)
- DDR4 So-DIMM 260 pin
- Channel A
- BANK 0,1,2,3
- Address : 0XA0/1 P.23
- DDR4 So-DIMM 260 pin
- Channel B
- BANK 4,5,6,7
- Address : 0XA3/4 P.24

X4 DMI

IO_B
P.73

LAN(GbE) JRJ45
- PCIE 2.0 5GT/s
- Port 14
- E2600

USB3.1 - JUSB 3
- GEN2
- USB3.1 Port 2
- USB2.0 Port 2

USB3.1 - JUSB 2
- GEN2
- USB3.1 Port 5
- USB2.0 Port 3

USB3 Re-driver
- PS8713

USB3 Re-driver
- PS8713

USB3.1 - JUSB 1
- GEN2
- On M/B
- Port 1
- W/USB Charger
(SLGC55544)
P.71

Type C - JTYPEC1
- USB3.1 GEN2
- USB3.1 Port3&4
- RTS5441E
P.42-43

Cannonlake PCH - H
FCBGA874 (25X24)

CFL-H : HM370
CML-H : HM470
P.14-21

SPI

SPI ROM 16M
- SOP8
- Size : 16M
P.16

LPC/eSPI BUS

TPM
- NPCT750
P.66

HDD - JHDD1
- SATA 3.0
- Port 13
(SATA 0B)
P.67

SSD - JSSD3 (PCIE/SATA)
- PCIE 2.0 5GT/s
- PCIE Port 17-20
- SATA @ Port 17
P.69

SSD - JSSD2 (PCIE/SATA)
- PCIE 2.0 5GT/s
- PCIE Port 9-12
- SATA @ Port 12
P.68

SSD - JSSD1 (PCIE)
- PCIE 2.0 5GT/s
- PCIE Port 21-24
P.68

HD Audio

I2C

EMR - JEMR1
- PCH I2C0
P.64

Touch Pad
- EC PS2
- PCH I2C1 P.63

EC KB9022
P.58

I2C/PS2

Fan Control*2
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WIFI - JNGFF1
- PCIE1.0 2.5GT/s
- PCIE Port 15
- USB2 Port 4
P.52

DDC Camera
- Port 5
P.38

Finger print
- USB2 Port 8
P.66

Tuch Screen
- USB2 Port 6
- PCH I2C2
P.38

HDA Codec
- ALC295
P.56

Extend IC
- I2C
- KC3810 P.59

Int.KBD
- KSI/KSO
- W/BL or 4 Zone RGB
P.63

Int. Speaker
- ON IO/B > L
- ON M/B > R

Int. DMIC
- On CCD Module

Audio Jack
- On IO/B

Sub Board	
IO/B (JIO1/JIO2)	P.73
HS/B (JHS1)	P.66
TURBO/B (JTURBO1)	P.77
RTC CKT. (JRTC1)	P.20
Power On/Off CKT.	P.63
HW Circuit DC/DC	P.78
Power Circuit DC/DC	P.82-111

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Title: Block Diagrams

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Vcc	3.3V +/- 5%
Ra	100K +/- 1%

EC Board ID Table for AD channel

Board ID	Rb	Vmin	Vtyp	Vmax	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

	Board ID
SD034120280	0
SD034150280	1
SD034200280	2
SD034270280	3
SD034330280	4
SD034430280	5
SD034560280	6
SD034750280	7
SD034100380	8
SD034130380	9
SD034160380	10
SD034200380	11
SD034750380	12
SD000001B80	13
SD00000G280	14
SD034330380	15
SD00000WM80	16
SD034560380	17
SD00000AL80	18
	19

*PCB Version
*Key board type

Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev0.3
3	50 Rev1.0
4	50 Rev0.2+RGB
5	50 Rev0.3+RGB
6	50 Rev1.0+RGB
7	60 Rev0.1
8	60 Rev0.2
9	60 Rev0.3
10	60 Rev1.0
11	60 Rev0.2+RGB
12	60 Rev0.3+RGB
13	60 Rev1.0+RGB
14	
15	
16	
17	
18	
19	

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	XXXXXX (EMR)			
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK (+3VALW) EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	Thermal Sensor (G781)	1001_101xb	1001_1011b	1001_1010b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		
	KC3810	0xC0		

Item (X43 / X76)	BOM Structure		Item (X43 / X76)	BOM Structure	
Unpop	@		eDP-TS USB	TS_USB@	
Connector	CONN@		eDP-TS USB	NONTS_I2C@	V
PCB	PCB@	V	eDP-TS I2C	TS_I2C@	
UMA Only(Reserved)	UMA@		mDP	DP@	V
H62 CPU(Reserved)	H62@		For Acer IOAC	IOAC@	V
H82 CPU(POP)	H82@	V	No Acer IOAC	NIOAC@	
CFL i5QS CPU	CFLi5QS@		Intel CNVi	CNVI@	V
CFL i5 CPU	CFLi5@		FOR UART BT module	UART_BT@	
CFL QS PCH	CFLPCHQS@		FOR UART debug	UART@	
			Extend GPIO	KC3810@	
CML i5QS CPU	CMLi5QS@				
CML i7QS CPU	CMLi7QS@		Finger Print	FP@	V
CML i9QS CPU	CMLi9QS@		FinerPrint(with PBA)	PBA@	V
CML QS PCH				Remove KBLED@	
CML i5 CPU	CMLi5@		KB LED driver	LED14P@	
CML i7 CPU	CMLi7@		EMR 1.8V	WC18V@	
CML i9 CPU			EMR 3.3V	WC33V@	
CML PCH	CMLPCH@		Thermal sensor	TMS@	V
			TPM pop	TPM@	
			TPM non-pop	NTPM@	V
dGPU circuit	VGA@	V	SSD3 pop	SSD3@	
N17P GPU	N17P@				
N18P GPU	N18P@	V			
N18P-G61	VGAG61@		PVT	PVT@	
N18P-G62 MP2	VGAG62@		PVT W/RGB	PVTRGB@	

43 Level	Descript i on	BOM Structure
431AMBBOL02	FH51M PG61QS 4G	PCB@/H82@/SATANRD@/CMLi5@/CMLPCH@/VGA@/N18P@/VGAG61@/TS_USB@/NONTS_I2C@/DP@/IOAC@/CNVI@/FP@/PBA@/KBLED@/LED14P@/WC18V@/TMS/@TPM@

Item (X4E)	BOM Structure	
EMI requirement	EMI@	V
EMI require reserve	XEMI@	
ESD requirement	ESD@	V
ESD require reserve	XESD@	
FP ESD requirement	FPESD@	V
X4EAMBBOL01	PG6162 FOR EE	
X4EP4MBOL01	PG6162 IO FOR EE	

Item (X76)	BOM Structure
OVRM-uPI	uPI_X76@
OVRM-ON	ON_X76@
VRAM-SAMSUNG	X76SAM@
VRAM-MICRON	X76MIC@

X76869BOL01 - MICRON
X76869BOL02 - SAMSUNG
X76869BOL03 - ON OVRM
X76869BOL04 - UPI OVRM

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Title: Notes List

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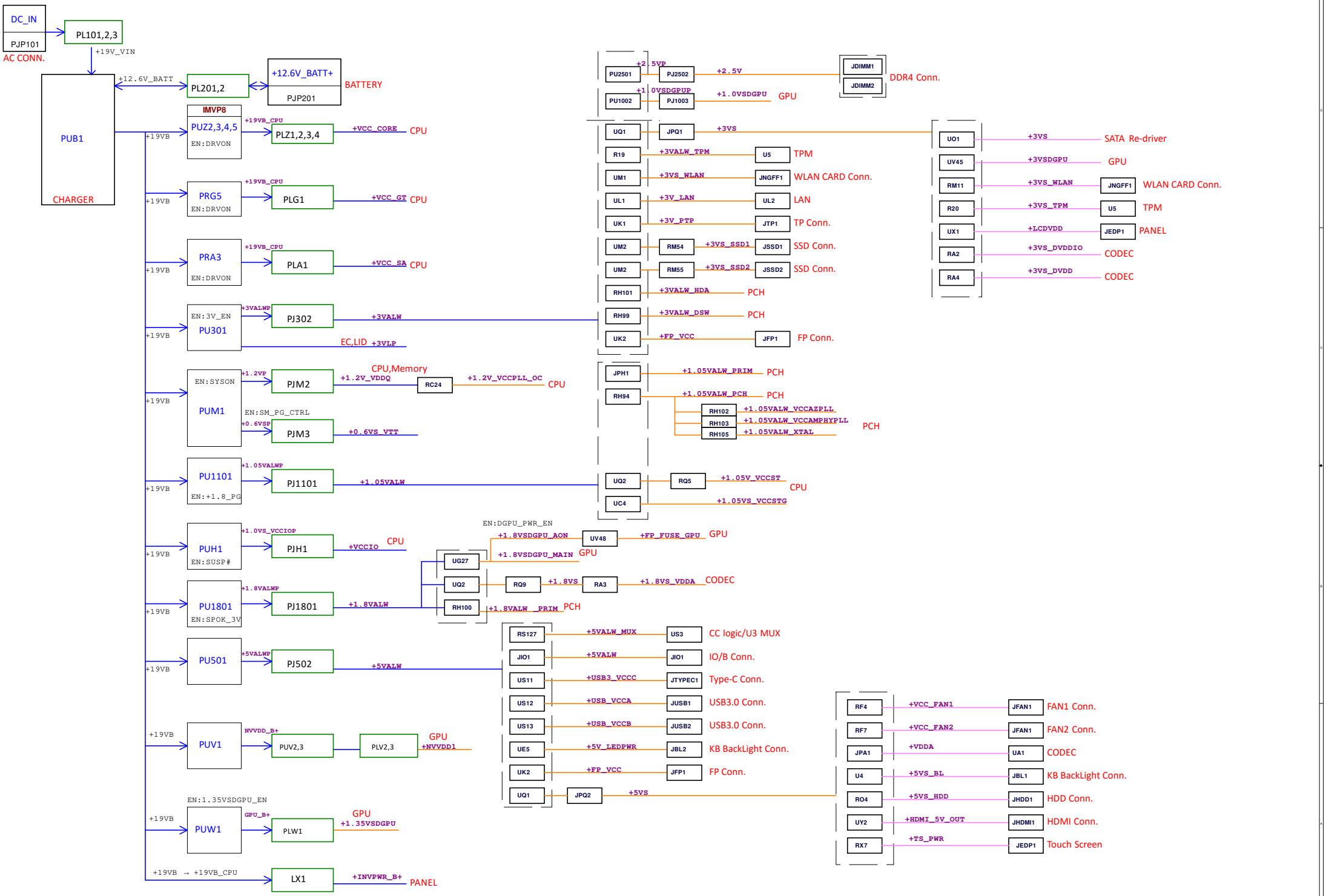

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Power Map

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DH5VF_EVT Power Sequence AC mode

BIOS ver: V0.02W1
EC: ver: V002AT04

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Compal Electronics, Inc.

Title: Power Sequence

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Coffee Lake-H
- Re-fresh R0 stepping

UC1
CFLi5QS@
S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00

UC5
CFLi5@
S IC CL8068404121905 SRF6X U0 2.4G
SA0000COG40

UH1
CFLPCHQS@
S IC FHHM370 QNYF B0 BGA 874P PCH-
SA0000BPF10

Comet Lake-H

UC1
CMLi5QS@
S IC CL8070104398806 QTJ1 R0 2.1G 1440 S
SA0000D3I10

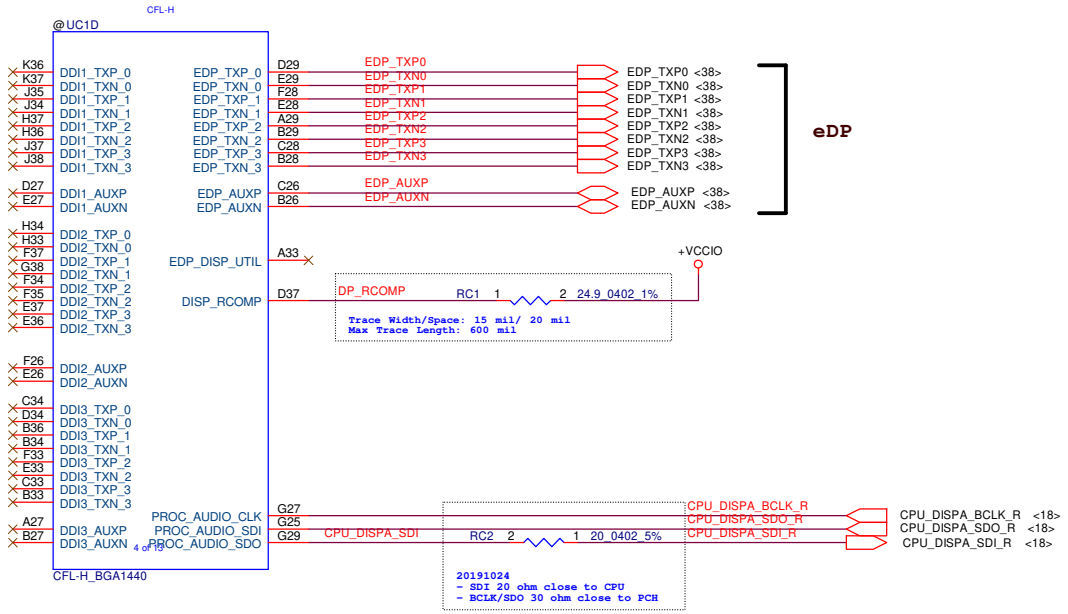
UC6
CMLi5@
S IC CL8070104399510 SRH84 R1 2.5G
SA0000DCP40

UC1
CMLi7QS@
S IC CL8070104398908 QTJ2 R0 2.4G 1440 S
SA0000D3N10

UC8
CMLi7@
S IC CL8070104399510 SRH84 R1 2.5G
SA0000DCP40

UC1
CMLi9QS@
S IC CL8070104399007 QTJ0 R0 2.8G S
SA0000D3G10

UH1
CMLPCH@
S IC FH82HM470 SRJAU A0 FCBGA PCH-H
SA0000DDP80



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Compal Electronics, Inc.

Title: CFL-H(1/8)DDI/eDP

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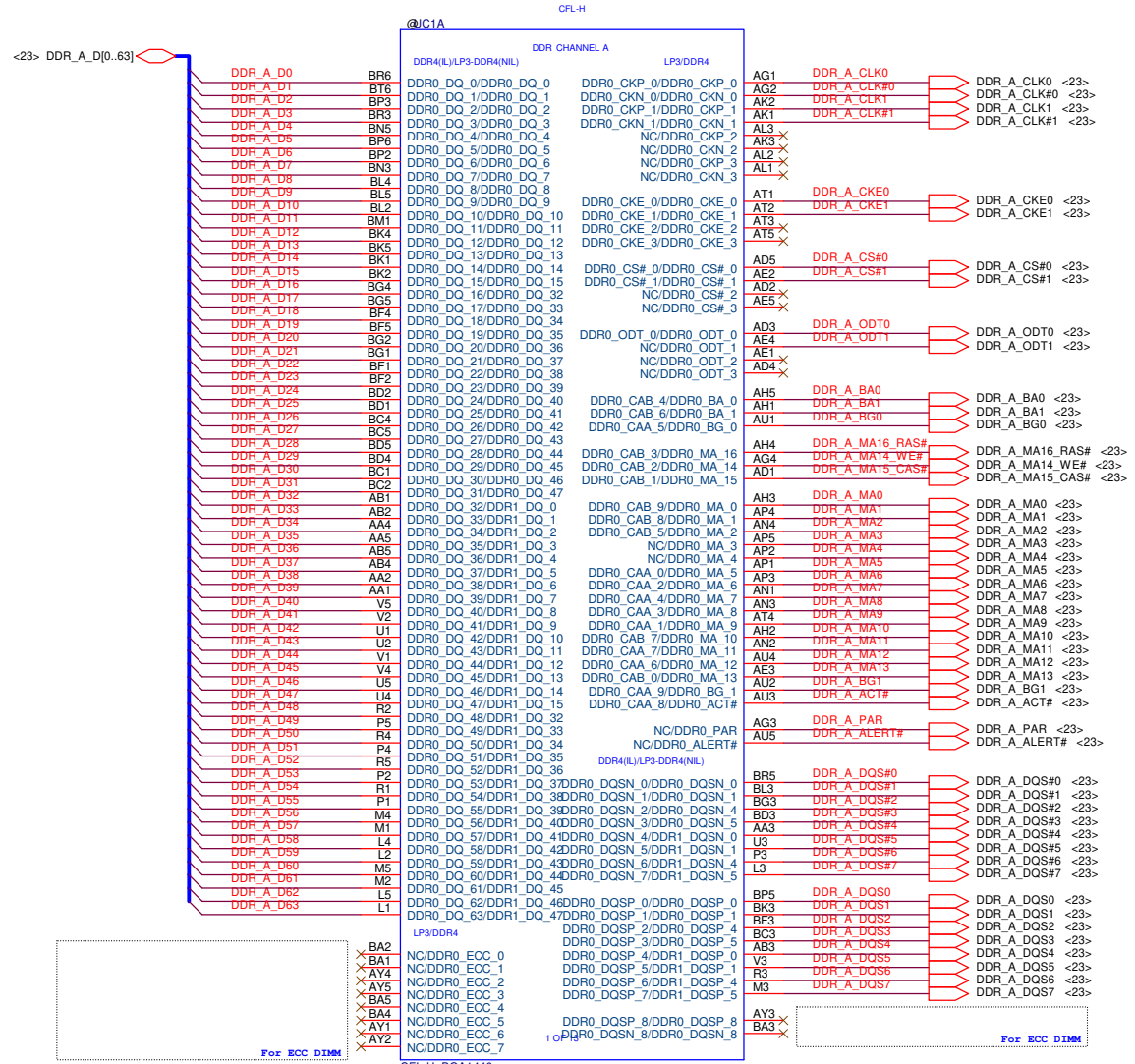
CHANNEL-A Interleaved Memory



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CFL-H(2/8)DIMMA

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

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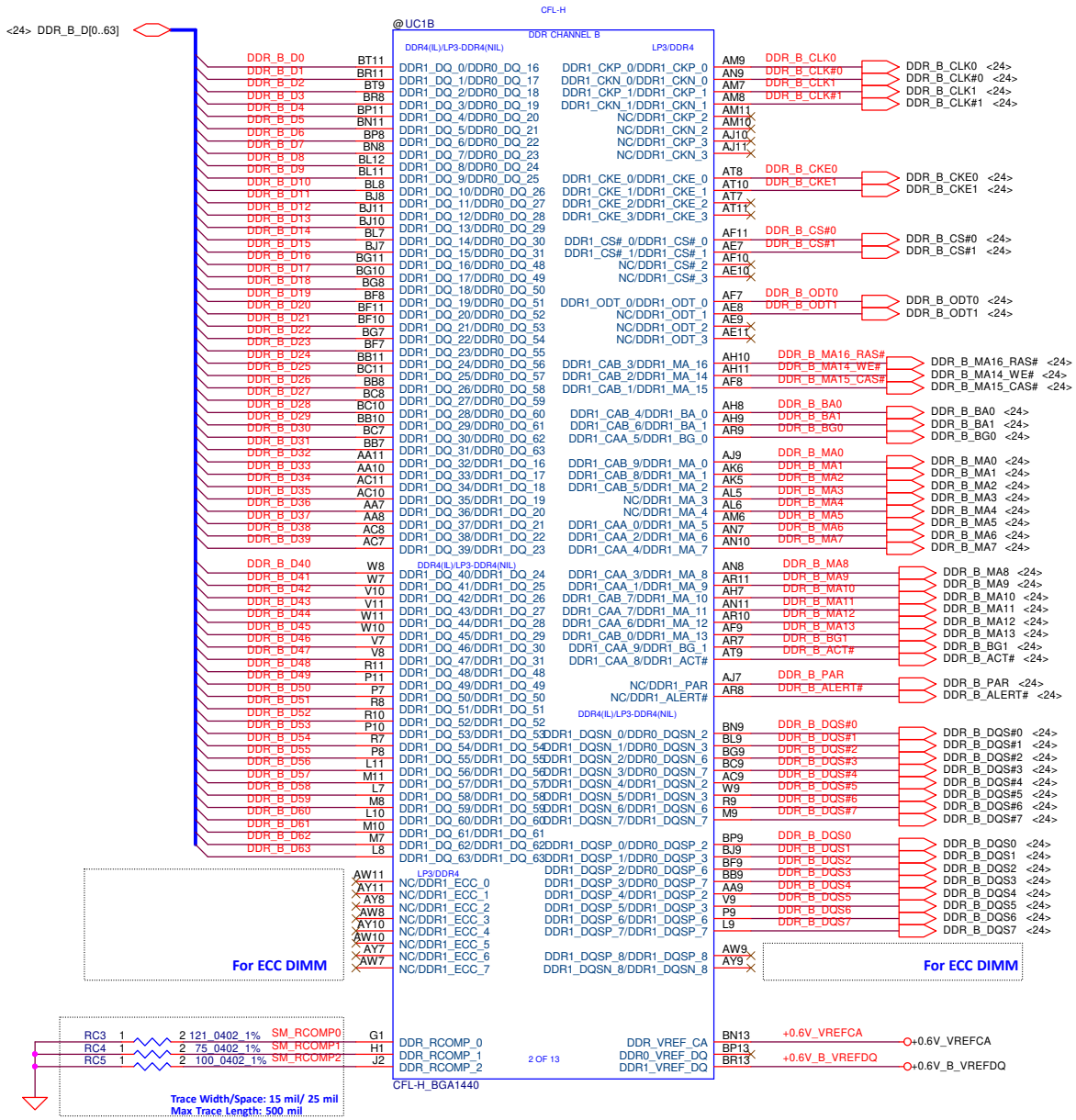
CHANNEL-B Interleaved Memory



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Compal Electronics, Inc.			
Title	CFL-H(3/8)DIMMB		
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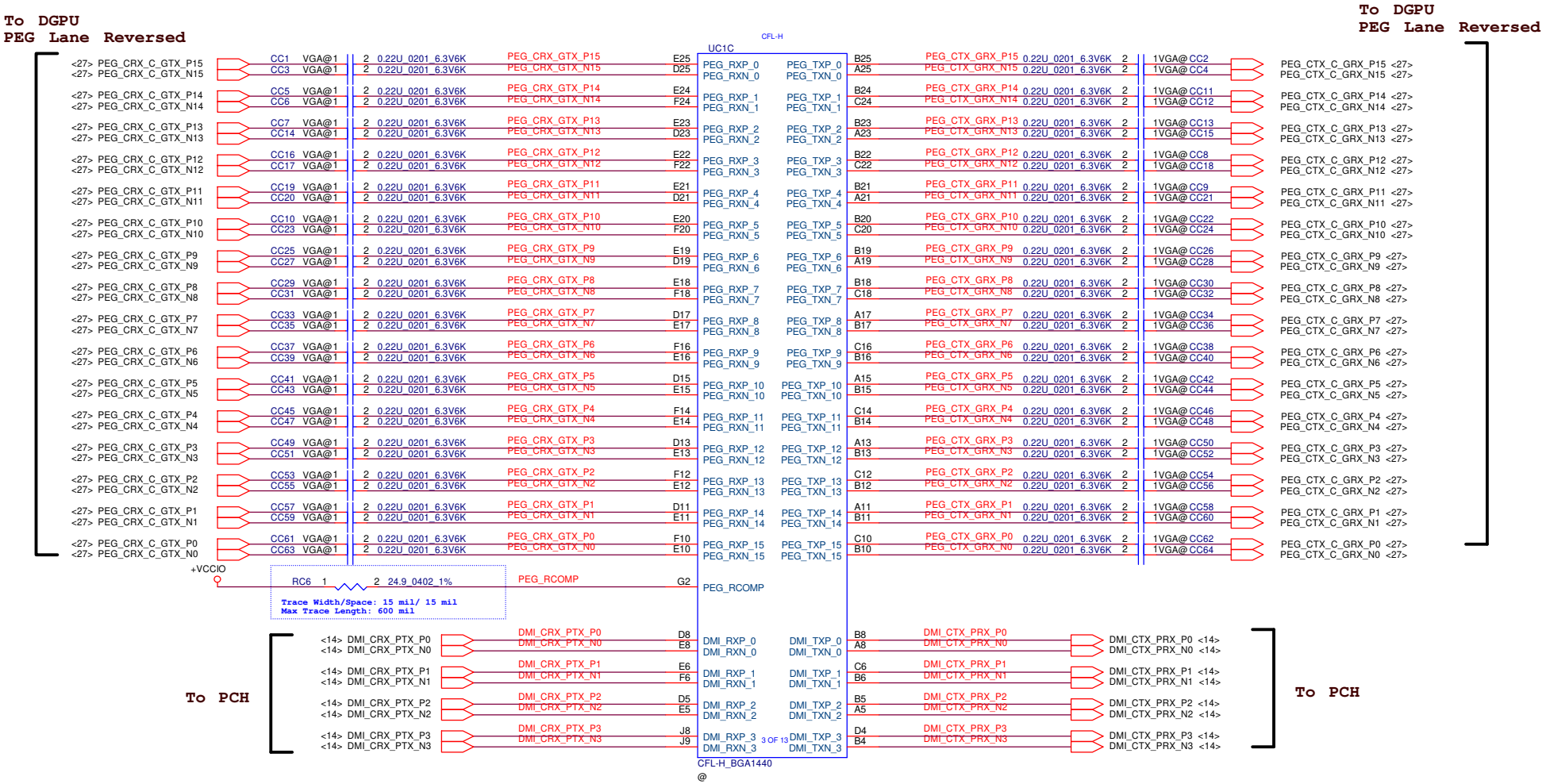
PEG&DMI



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Compal Electronics, Inc.

Title: PEG/DMI

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571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

UC1E
CFL-H
CFL-H_BGA1440
5 OF 13

<15> PCH_CPU_BCLK_P
<15> PCH_CPU_BCLK_N
PCH_CPU_BCLK_P
PCH_CPU_BCLK_N
B31
A32
BCLKP
BCLKN

<15> PCH_CPU_PCIBCLK_P
<15> PCH_CPU_PCIBCLK_N
PCH_CPU_PCIBCLK_P
PCH_CPU_PCIBCLK_N
D35
C36
PCI_BCLKP
PCI_BCLKN

<15> PCH_CPU_24M_CLK_P
<15> PCH_CPU_24M_CLK_N
PCH_CPU_24M_CLK_P
PCH_CPU_24M_CLK_N
E31
D31
CLK24P
CLK24N

Sensitive
<91> CPU_SVID_CLK_R
CPU_SVID_ALERT#
CPU_SVID_CLK_R
CPU_SVID_DAT_R
H_PROCHOT#_R
BH31
BH32
BH29
BR30
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#

DDR_PG_CTRL
BT13
DDR_VTT_CNTL

Sensitive
EC_VCCST_PG
H13
VCCST_PWRGD

<18> H_CPUPWRGD
<17> H_PLTRST_CPU#
<17> H_PM_SYNC_R
H_CPUPWRGD
H_PLTRST_CPU#
H_PM_SYNC_R
H_PM_DOWN
H_PECI
H_THERMTRIP#
BT31
BP35
BM34
BP31
BT34
J31
PROCPWRGD
RESET#
PM_SYNC
PM_DOWN
PECI
THERMTRIP#

<17,58> H_PECI
<17> PCH_THERMTRIP#_R
RC17 1 @ 2 0_0402_5%

@ TC5
SKTOCC#
BR33
BN1
SKTOCC#
PROC_SELECT#

@ TC6
CATERR#
BM30
CATERR#

AT13
AW13
ZVM#
MSM#
AU13
AY13
RSVD1
RSVD2

CFG_0 BN25 CFG0
CFG_1 BN27
CFG_2 BN26 CFG2
CFG_3 BN28
CFG_4 BR20 CFG4
CFG_5 BM20 CFG5
CFG_6 BT20 CFG6
CFG_7 BP20 CFG7
CFG_8 BR23
CFG_9 BR22
CFG_10 BT23
CFG_11 BT22
CFG_12 BM19
CFG_13 BR19
CFG_14 BP19
CFG_15 BT19
CFG_17 BN23
CFG_16 BP23
CFG_19 BP22
CFG_18 BN22

BPM#_0 BR27 XDP_BPM#0 TC1 @
BPM#_1 BT27 XDP_BPM#1 TC2 @
BPM#_2 BM31 XDP_BPM#2 TC3 @
BPM#_3 BT30 XDP_BPM#3 TC4 @

PROC_TDO BT28 CPU_XDP_TDO
PROC_TDI BL32 CPU_XDP_TDI
PROC_TMS BP28 CPU_XDP_TMS
PROC_TCK BR28 CPU_XDP_TCK0
PROC_TRST# BP30 CPU_XDP_TRST#
PROC_PREQ# BL30 XDP_PREQ#
PROC_PRDY# BP27 XDP_PRDY#

CPU_XDP_TDO <18>
CPU_XDP_TDI <18>
CPU_XDP_TMS <18>
CPU_XDP_TCK0 <18>
CPU_XDP_TRST# <21>
TC19 @
TC20 @
To be confirm

CFG_RCOMP BT25
CFG_RCOMP 1 RC18 2 49.9_0402_1%
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

XDP_PREQ# <21>
XDP_PRDY# <21>

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

CFG0 RC7 1 @ 2 1K_0402_5%
CFG2 RC8 1 @ 2 1K_0402_5%
CFG4 RC9 1 @ 2 1K_0402_5%
CFG5 RC10 1 @ 2 1K_0402_5%
CFG6 RC11 1 @ 2 1K_0402_5%
CFG7 RC12 1 @ 2 1K_0402_5%

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
* 0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

20191024
PROC_SELECT#
> should be unconnected on CFL/CML processor

XESD@ 0.1U_0201_10V6K 1 2 CC65 H_CPUPWRGD
ESD@ 1000P_0402_50V7K 1 2 CC66 H_PROCHOT#_R
XESD@ 0.1U_0201_10V6K 1 2 CC67 H_THERMTRIP#
ESD@ 1000P_0402_50V7K 1 2 CC68 EC_VCCST_PG

Near CPU side

8/21 follow 1050 Request

+1.05V_VCCST
RH1 1 2 1K_0402_5% H_THERMTRIP#

+1.2V_VDDQ
CC69 0.1U_0201_10V6K
UC3
74AUP1G07SE-7_SOT353-5
DDR_PG_CTRL
+3VS
RC23 330K_0402_5%
SM_PG_CTRL <88>

8/21 PU 330K follow CRB

*20191024
– CML RCP/PDG/Check list , PROC_TDO PU 100 ohm to VCCXT
*20191104
– CMC@ change to always pop (RC76/77/78/79)

+1.05VS_VCCSTG
RC76 2 1 51_0402_5% CPU_XDP_TMS
RC77 2 1 51_0402_5% CPU_XDP_TDI
RC78 2 1 51_0402_5% CPU_XDP_TDO
Place to CPU side

RC79 2 1 51_0402_5% CPU_XDP_TCK0
RC80 2 @ 1 51_0402_5% PCH_JTAG_TCK1
RC81 2 @ 1 51_0402_5% CPU_XDP_TRST#
PCH_JTAG_TCK1 <18>
Place to CPU side

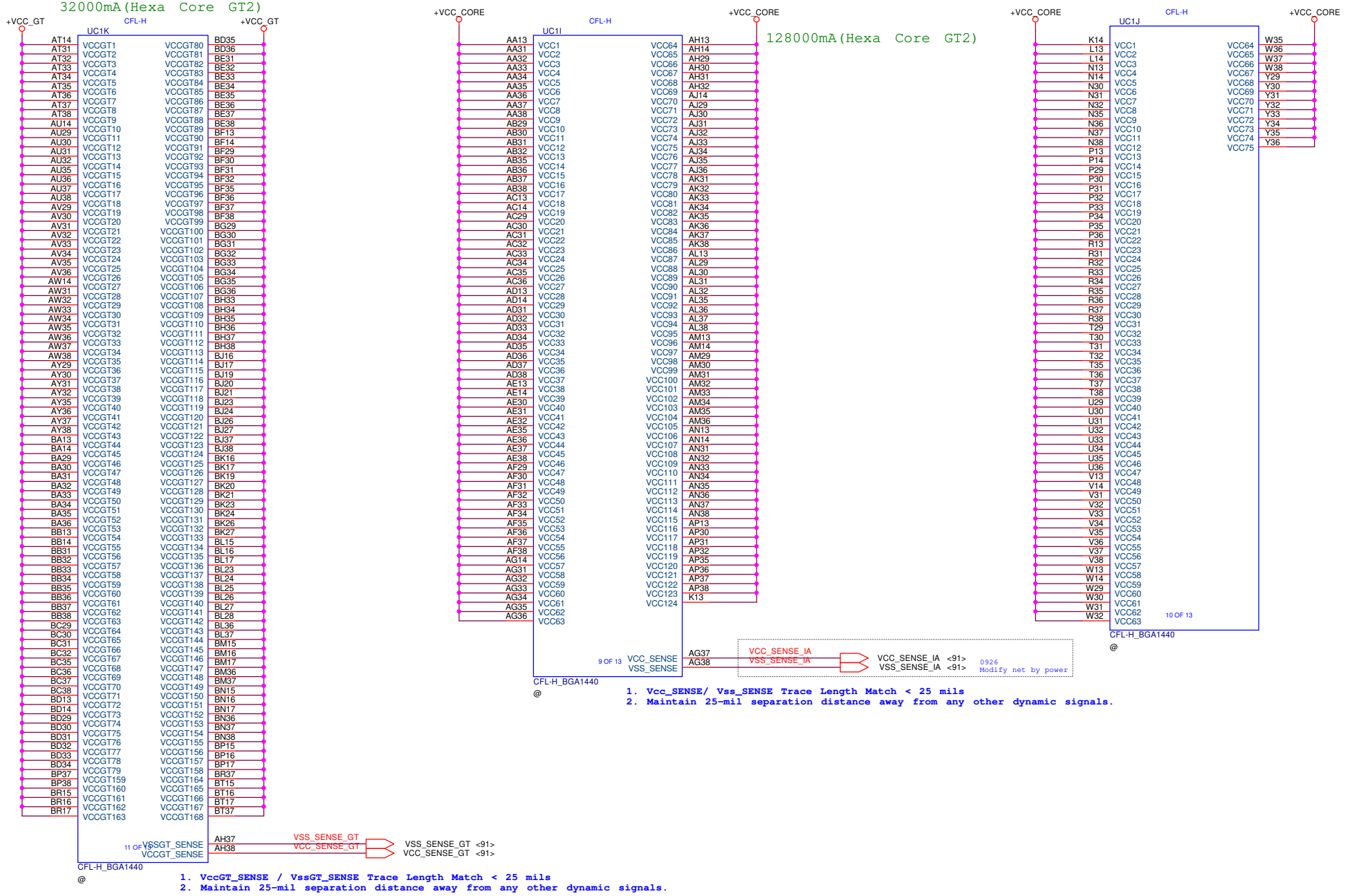
+1.05VS_VCCSTG
RC21 1K_0402_5%
<58,85> H_PROCHOT#
RC14 1 2 499_0402_1% H_PROCHOT#_R
+1.05V_VCCST
RC22 1K_0402_5%
<58,78> EC_VCCST_PG_R
RC151 2 60.4_0402_1% EC_VCCST_PG
<17> H_PM_DOWN_R
RC16 1 2 20_0402_5% H_PM_DOWN
RH2 @ 13_0402_5%

SVID

+1.05V_VCCST
RC19 56_0402_1%
RC20 100_0402_1%
<91> CPU_SVID_ALERT#_R
RC13 1 2 220_0402_5% CPU_SVID_ALERT#
<91> CPU_SVID_DAT_R
CPU_SVID_DAT_R

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom
Document Number: FH51M M/B LA-J871P
Rev: 1.0
Date: Tuesday, February 11, 2020
Sheet 10 of 112



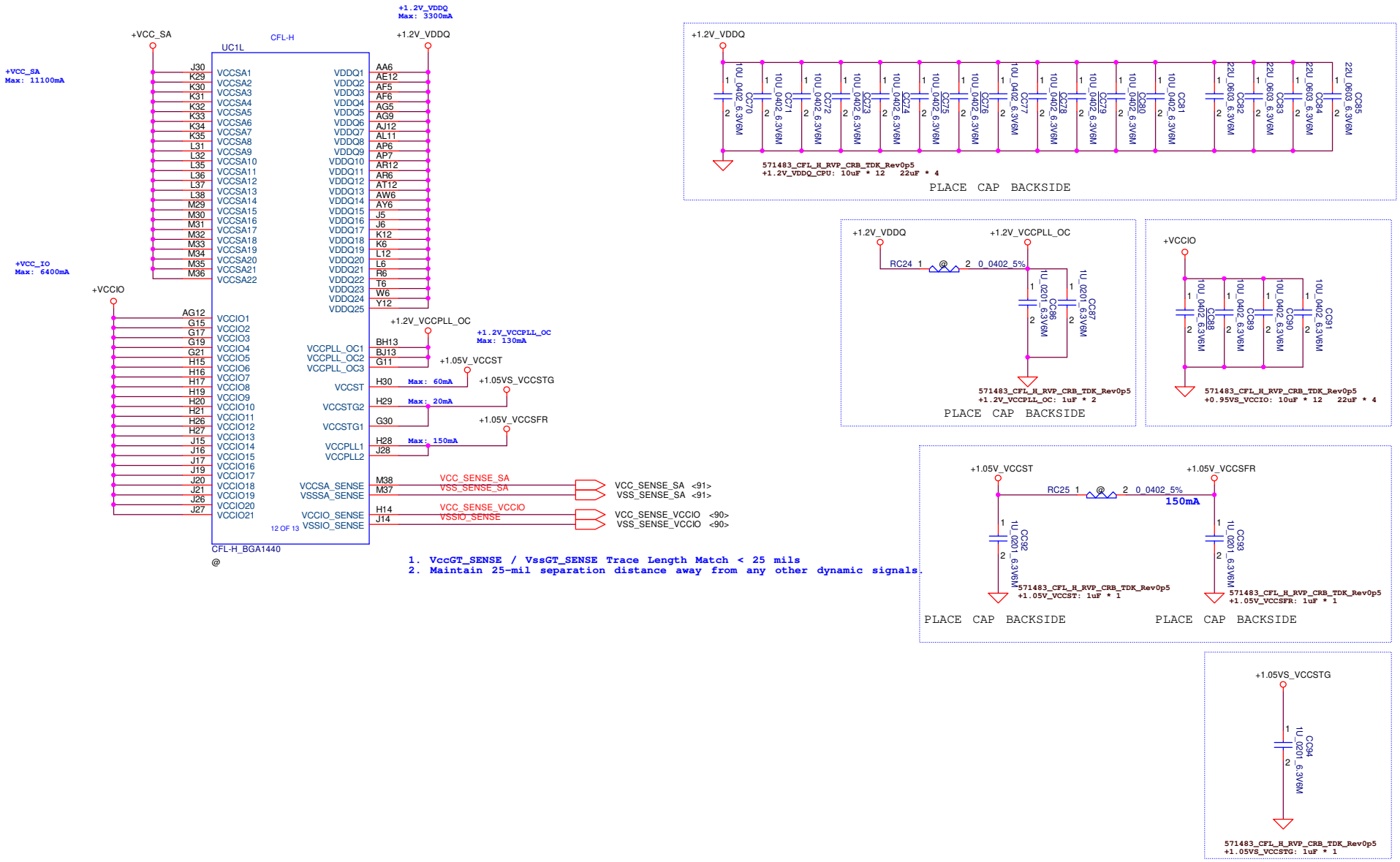
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 11 of 112



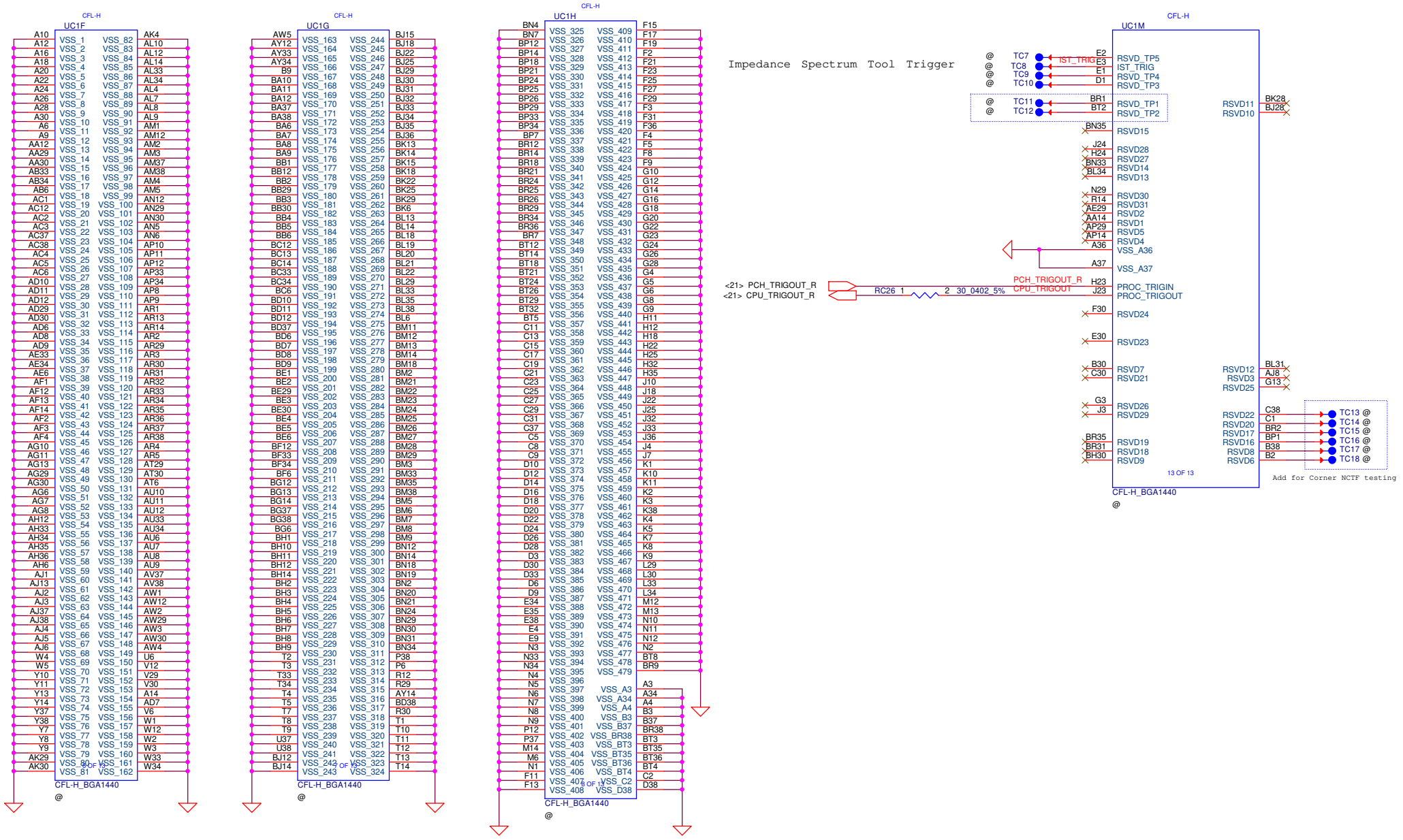
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	FH51M M/B LA-J871P	1.0

Date: Tuesday, February 11, 2020 Sheet 12 of 112



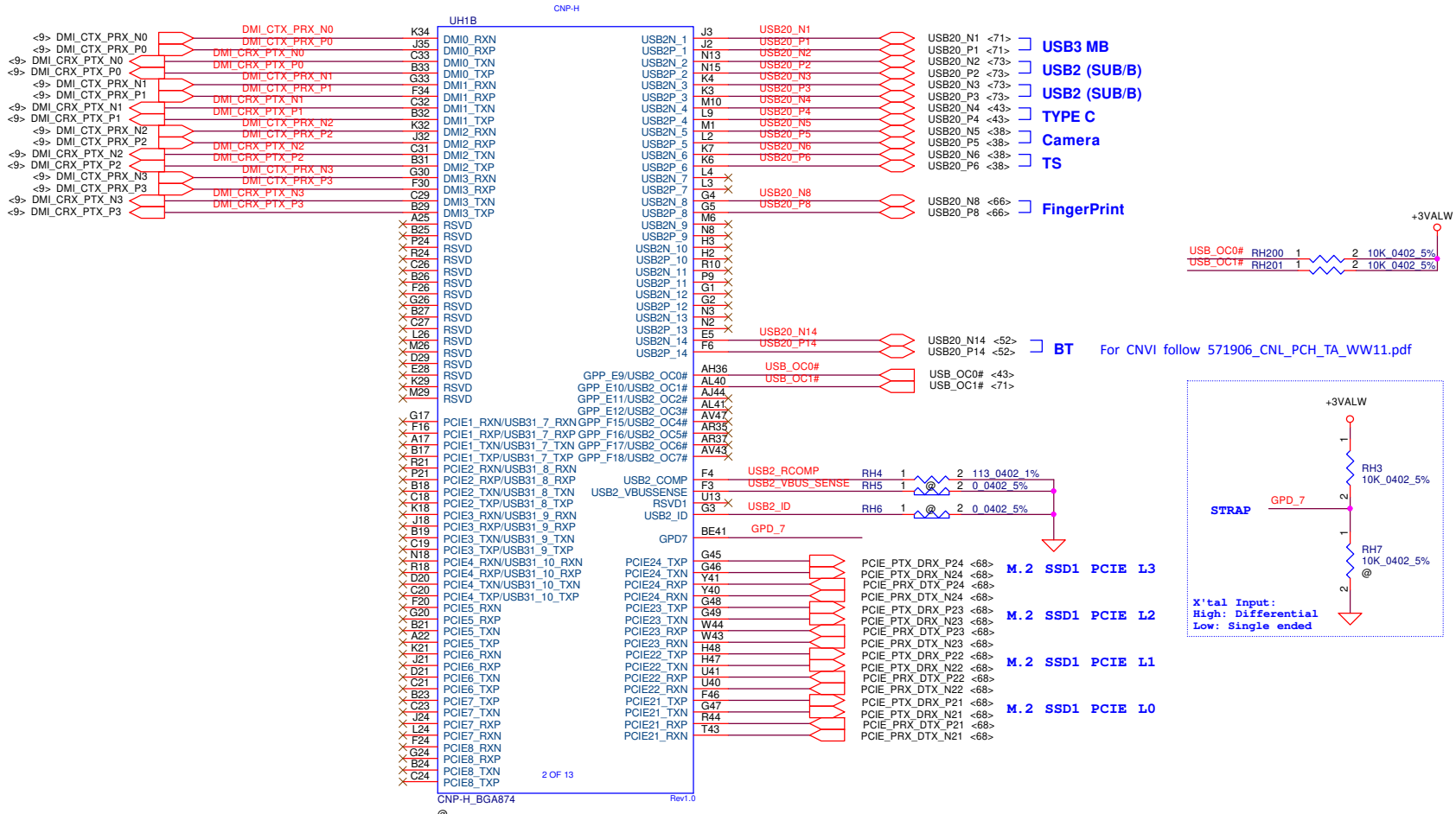
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: CFL-H(8/8)GND/RSVD

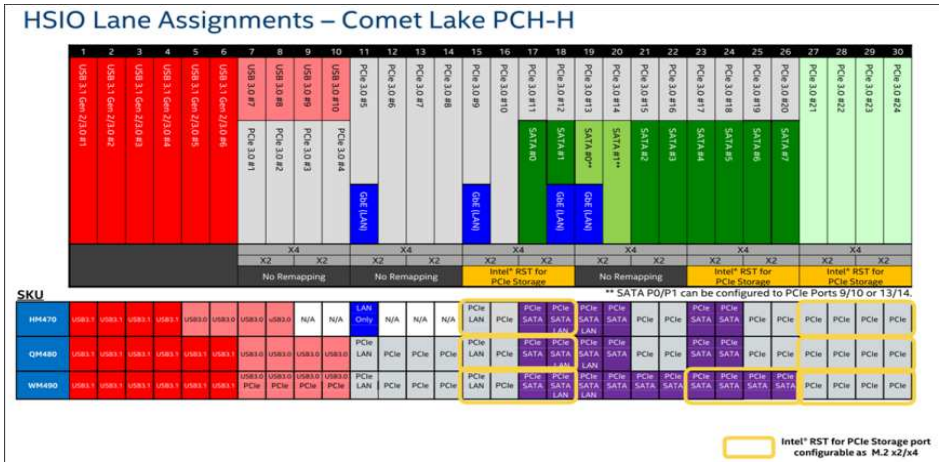
Size	Document Number	Rev
Custom	FH51M M/B LA-J871P	1.0

Date: Tuesday, February 11, 2020 Sheet 13 of 112



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configuration, and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size	Document Number	Rev
Custom	FH51M M/B LA-J871P	1.0
Date: Tuesday, February 11, 2020	Sheet 14 of 112	

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT — RH11 EMI@ 33_0402_1% — XTAL_24M_PCH_OUT_R

XTAL_24M_PCH_IN — RH8 1M_0402_5% — RH9 EMI@ 33_0402_1% — XTAL_24M_PCH_IN_R

YH1 24MHZ_18PF_7R24000001 (NC NC)

CH5 33P_0402_50V8J — CH6 18P_0402_50V8J

PCH_RTCX1 — RH12 10M_0402_5% — PCH_RTCX2

YH2 32.768KHZ_9PF_X1A000141000200

CH7 10P_0201_50V8J — CH8 10P_0201_50V8J

Trace Space: 15 mil
Max Trace Length: 1000 mil

use same part w C5MMH

20200114
– CH7/CH8 Change to SE173100J80

remove TP as C5PRH

UH1G — CNP-H

<10> PCH_CPU_24M_CLK_P / PCH_CPU_24M_CLK_N — BE33 D7 C6 — GPP_A16/CLKOUT_48 — CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC# — CLKOUT_ITPXDP# CLKOUT_ITPXDP_P — Y3 Y4 — TH2 TH3

<10> PCH_CPU_BCLK_P / PCH_CPU_BCLK_N — B8 C8 — CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK# — CLKOUT_CPUPCIBCLK# CLKOUT_CPUPCIBCLK_P — B6 A6 — PCH_CPU_PCIBCLK_N <10> / PCH_CPU_PCIBCLK_P <10>

XTAL_24M_PCH_OUT_R / XTAL_24M_PCH_IN_R — U9 U10 — XTAL_OUT XTAL_IN

RH10 2_60.4_0402_1% — XCLK_BIASREF — T3 — XCLK_BIASREF

XCLK_BIASREF (PDG)
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil
8/24

PCH_RTCX1 — BA49 — RTCX1
PCH_RTCX2 — BA48 — RTCX2

VGA_CLKREQ# — BF31 — GPP_B5/SRCCLKREQ0#

<73> LAN_CLKREQ# — BE31 — GPP_B6/SRCCLKREQ1#
<52> WLAN_CLKREQ# — AR32 — GPP_B7/SRCCLKREQ2#
<68> SSD2_CLKREQ# — BB30 — GPP_B8/SRCCLKREQ3#
<68> SSD1_CLKREQ# — BA30 — GPP_B9/SRCCLKREQ4#
<69> SSD3_CLKREQ# — AN29 — GPP_B10/SRCCLKREQ5#

20190918 SSD2&3 Change

20191209
> SSD1 – GPP_B9/CLKREQ4# (PCIE only) (2018 @SSD2)
> SSD2 – GPP_B8/CLKREQ3# (PCIE/SATA) (2018 @SSD1)
> SSD3 – GPP_B10/CLKREQ5# (PCIE/SATA) (2019 NEW)

remove no use srcclkreq

GPP_B0/SRCCLKREQ6# — AE47
GPP_H1/SRCCLKREQ7# — AC48
GPP_H2/SRCCLKREQ8# — AE41
GPP_H3/SRCCLKREQ9# — AF48
GPP_H4/SRCCLKREQ10# — AC41
GPP_H5/SRCCLKREQ11# — AC39
GPP_H6/SRCCLKREQ12# — AE39
GPP_H7/SRCCLKREQ13# — AB48
GPP_H8/SRCCLKREQ14# — AC44
GPP_H9/SRCCLKREQ15# — AC43

CLKOUT_PCIE_N15 / CLKOUT_PCIE_P15 — V2 V3
CLKOUT_PCIE_N14 / CLKOUT_PCIE_P14 — T2 T1
CLKOUT_PCIE_N13 / CLKOUT_PCIE_P13 — AA1 Y2
CLKOUT_PCIE_N12 / CLKOUT_PCIE_P12 — AC7 AC6

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CLKOUT_PCIE_N0 / CLKOUT_PCIE_P0 — AJ6 AJ7 — CLK_PEG_VGA# <27> / CLK_PEG_VGA <27> — DGPU
CLKOUT_PCIE_N1 / CLKOUT_PCIE_P1 — AH9 AH10 — CLK_PCIE_LAN# <73> / CLK_PCIE_LAN <73> — GLAN
CLKOUT_PCIE_N2 / CLKOUT_PCIE_P2 — AE14 AE15 — CLK_PCIE_WLAN# <52> / CLK_PCIE_WLAN <52> — NGFF WL+BT(KEY E)
CLKOUT_PCIE_N3 / CLKOUT_PCIE_P3 — AE6 AE7 — CLK_PCIE_NGFF1# <68> / CLK_PCIE_NGFF1 <68> — M2 SSD1
CLKOUT_PCIE_N4 / CLKOUT_PCIE_P4 — AC2 AC3 — CLK_PCIE_NGFF3# <68> / CLK_PCIE_NGFF3 <68> — M2 SSD3
CLKOUT_PCIE_N5 / CLKOUT_PCIE_P5 — AB2 AB3 — CLK_PCIE_NGFF2# <69> / CLK_PCIE_NGFF2 <69> — M2 SSD2
CLKOUT_PCIE_N6 / CLKOUT_PCIE_P6 — W4 W3
CLKOUT_PCIE_N7 / CLKOUT_PCIE_P7 — W7 W6
CLKOUT_PCIE_N8 / CLKOUT_PCIE_P8 — AC14 AC15
CLKOUT_PCIE_N9 / CLKOUT_PCIE_P9 — U2 U3
CLKOUT_PCIE_N10 / CLKOUT_PCIE_P10 — AC9 AC11
CLKOUT_PCIE_N11 / CLKOUT_PCIE_P11 — AE9 AE11

CLKIN_XTAL — R6 — REFCLK_CNV <52>

RH14 10K_0402_5%

CNP-H_BGA874 — Rev1.0

+3VS

RH204 10K_0402_5% LAN_CLKREQ#
RH205 10K_0402_5%
RH206 10K_0402_5% WLAN_CLKREQ#
RH207 10K_0402_5% SSD2_CLKREQ#
RH220 10K_0402_5% SSD3_CLKREQ#
RH300 10K_0402_5% SSD1_CLKREQ#

→ VGA_CLKREQ# <27>

For DDX03 R02

XTAL Frequency Select

+1.8VALW_PRIM — RH15 4.7K_0402_5% — CNV_BRI_PTX_DRX — STRAP

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

VCCPSPI Select

+1.8VALW_PRIM — RH21 @ 4.7K_0402_5% — GPP_J9 — STRAP

The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

20191210C
– RH22 change to 20K for CNVI review

M.2 CNV Mode Select

+1.8VALW_PRIM — RH22 20K_0402_1% — CNV_RGI_PTX_DRX
RH23 @ 10K_0402_5% — STRAP

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

Pulled down by CRF CNVi RGI_DT pin

remove SD signal from PCH

remove CPU_C10_GATE#

UH1M — CNP-H

GPP_G0/SD_CMD — AW13
GPP_G1/SD_DATA0 — BE9
GPP_G2/SD_DATA1 — BF8
GPP_G3/SD_DATA2 — BF9
GPP_G4/SD_DATA3 — BG8
GPP_G5/SD_CD# — BE8
GPP_G6/SD_CLK — BD8
GPP_G7/SD_WP — AV13

GPP_I11/M2_SKT2_CFG0 — AP3
GPP_I12/M2_SKT2_CFG1 — AP2
GPP_I13/M2_SKT2_CFG2 — AN4
GPP_I14/M2_SKT2_CFG3 — AM7

3.3V

20190927 <38> I2C_TS_INT# — I2C_TS_INT# — AV6
<38> I2C_TS_RST# — I2C_TS_RST# — AY3

GPP_J0/CNV_PA_BLANKING — AR13
GPP_J1/CPU_C10_GATE# — AV7
GPP_J11/A4WP_PRESENT — AW3
GPP_J10 — AT10
GPP_J_2 — AV4
GPP_J_3 — AY2

1.8V

<52> CNV_BRI_PTX_DRX — CNV_BRI_PTX_DRX
<52> CNV_BRI_PRX_DTX — CNV_BRI_PRX_DTX
<52> CNV_RGI_PTX_DRX — CNV_RGI_PTX_DRX
<52> CNV_RGI_PRX_DTX — CNV_RGI_PRX_DTX

GPP_J4/CNV_BRI_DT/UART0B_RTS# — BA4
GPP_J5/CNV_BRI_RSP/UART0B_RXD — AV3
GPP_J6/CNV_RGI_DT/UART0B_TXD — AW2
GPP_J7/CNV_RGI_RSP/UART0B_CTS# — AU9
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD

GPP_J9

CNV_WR_CLKN / CNV_WR_CLKP — BD4 BE3 — CLK_CNV_PRX_DTX_N <52> / CLK_CNV_PRX_DTX_P <52>
CNV_WR_D0N / CNV_WR_D0P — BB3 BB4 — CNV_PRX_DTX_N0 <52> / CNV_PRX_DTX_P0 <52>
CNV_WR_D1N / CNV_WR_D1P — BA3 BA2 — CNV_PRX_DTX_N1 <52> / CNV_PRX_DTX_P1 <52>
CNV_WT_CLKN / CNV_WT_CLKP — BC5 BB6 — CLK_CNV_PTX_DRX_N <52> / CLK_CNV_PTX_DRX_P <52>
CNV_WT_D0N / CNV_WT_D0P — BE6 BD7 — CNV_PTX_DRX_N0 <52> / CNV_PTX_DRX_P0 <52>
CNV_WT_D1N / CNV_WT_D1P — BG6 BF6 — CNV_PTX_DRX_N1 <52> / CNV_PTX_DRX_P1 <52>
CNV_WT_RCOMP — BA1 — RH16 150_0402_1%

PCIE_RCOMPN — B12 — RH17 100_0402_1%
PCIE_RCOMPP — A13
SD_1P8_RCOMP — BE5 — RH18 200_0402_1%
SD_3P3_RCOMP — BE4 — RH19 200_0402_1%
GPPJ_RCOMP_1P81 — BD1
GPPJ_RCOMP_1P82 — BE1 — GPPJ_RCOMP_1P8 — RH20 200_0402_1%
GPPJ_RCOMP_1P83 — BE2

20191024
– CML Check list OK

RSVD2 — Y35
RSVD3 — Y36
RSVD1 — BC1
TP — AL35 — TH4

#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

13 OF 13

CNP-H_BGA874 — Rev1.0

+1.8VALW_PRIM

RH1811 CNVI@ 20K_0402_1% — CNV_BRI_PRX_DTX
RH1821 CNVI@ 20K_0402_1% — CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

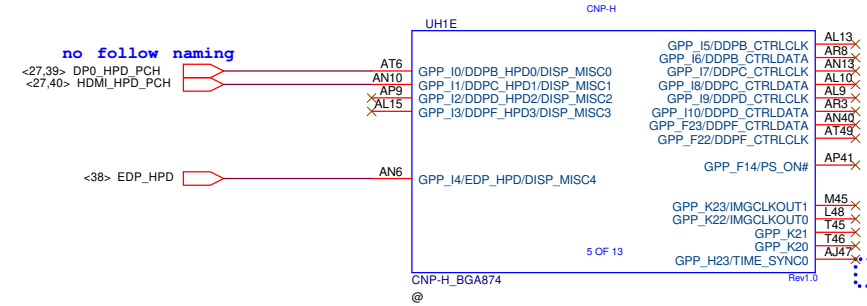
Date: Tuesday, February 11, 2020 | Sheet 15 of 112

no follow naming

can remove if no use DP
08/18

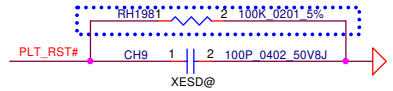
remove PCH DP SCLK/SDATA

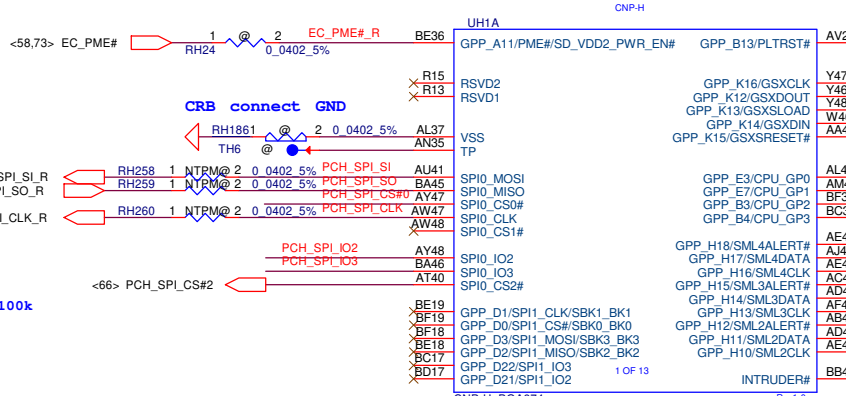
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.



remove CIO_PLUG_EVENT#

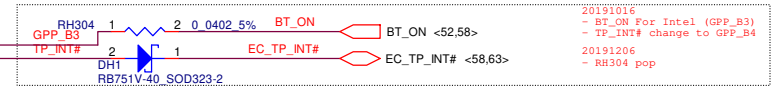
intel critical net recommend

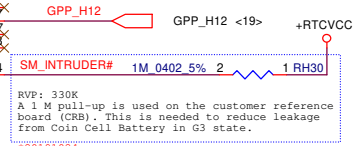




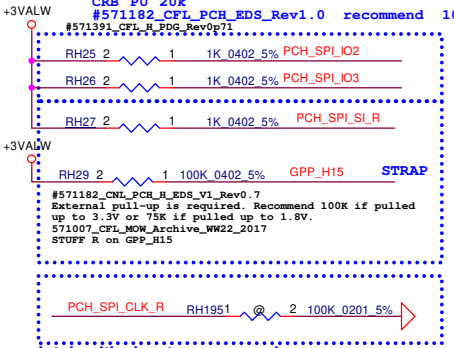
CRB connect GND

GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH.

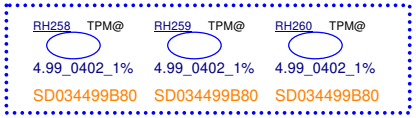


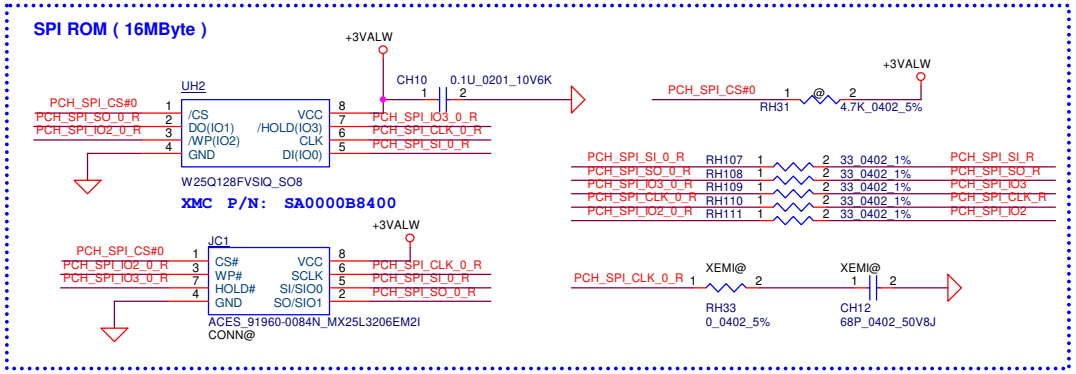


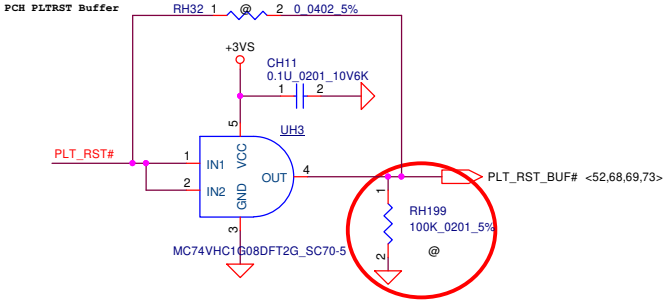
* wait confirm CG7
PDG P348 quad mode support PH1K
CRB PU 20k
#571182_CFL_PCH_EDS_Rev1.0 recommend 100k
#571391_CFL_H_PDG_Rev0p71



intel critical net recommend







Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PCH(3/8)DDC/SPI

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 16 of 112

#571391_CFL_H_PDG_Rev0p5
• eSPI clock and eSPI data mismatched: <500 mils.
• eSPI clock and eSPI chip select mismatched: <500 mils.
• eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

CNP-H
@UH1F

USB3 MB
<71> USB3_PTX_DRX_N1
<71> USB3_PTX_DRX_P1
<71> USB3_PRX_DTX_N1
<71> USB3_PRX_DTX_P1
F9 USB31_1_TXN
F7 USB31_1_TXP
D11 USB31_1_RXN
C11 USB31_1_RXP

USB3 IO/B
<73> USB3_PTX_DRX_N2
<73> USB3_PTX_DRX_P2
<73> USB3_PRX_DTX_N2
<73> USB3_PRX_DTX_P2
C3 USB31_2_TXN
D4 USB31_2_TXP
B9 USB31_2_RXN
C9 USB31_2_RXP

20191016
USB3 IO/B
<73> USB3_PTX_DRX_N5
<73> USB3_PTX_DRX_P5
<73> USB3_PRX_DTX_N5
<73> USB3_PRX_DTX_P5
USB3_PTX_DRX_N5
USB3_PTX_DRX_P5
USB3_PRX_DTX_N5
USB3_PRX_DTX_P5
C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP

20191016
USB3 Type C
<43> USB3_PTX_DRX_P3
<43> USB3_PTX_DRX_N3
<43> USB3_PRX_DTX_P3
<43> USB3_PRX_DTX_N3
G12 USB31_3_TXP
F11 USB31_3_TXN
C10 USB31_3_RXP
B10 USB31_3_RXN

20190924
USB3 Type C
<43> USB3_PTX_DRX_P4
<43> USB3_PTX_DRX_N4
<43> USB3_PRX_DTX_P4
<43> USB3_PRX_DTX_N4
USB3_PTX_DRX_P4
USB3_PTX_DRX_N4
USB3_PRX_DTX_P4
USB3_PRX_DTX_N4
C14 USB31_4_TXP
B14 USB31_4_TXN
J15 USB31_4_RXP
K16 USB31_4_RXN

1.8V (eSPI)
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
6 OF 13
CNP-H_BGA874
Rev1.0

BB39 LPC_AD0
AW37 LPC_AD1
AV37 LPC_AD2
BA38 LPC_AD3
LPC_AD0 <58>
LPC_AD1 <58>
LPC_AD2 <58>
LPC_AD3 <58>
LPC Bus check straps
LPC : +3.3V

BE38 LPC_FRAME#
AW35 TPM_SERIRQ
BA36 LPC_PIRQA#
BE39 RCIN#
BF38 ESPI_RST#
LPC_FRAME# <58>
TPM_SERIRQ <58,66>
RH261 1 @ 2 0_0402_5%
OVRM_EN <36,58>
BB36 CLK_LPC
BB34
RH35 2 1 22_0402_5%
CLK_LPC_R <58>
T48
T47
AH40
AH35 SSD_DEVSLP1
AL48
AP47
AN37
AN46
AR47 SSD_DEVSLP4
AP48
SSD_DEVSLP1 <68>
SSD_DEVSLP4 <69>
20191025
- SATA Port 4

+3VS
RCIN# 2 1 RH219 10K_0402_5%
+3VS
TPM_SERIRQ 2 1 RH37 10K_0402_5%
LPC_PIRQA# 1 2 RH38 10K_0402_5%

CNP-H
@UH1C

For Intel CLINK
TH10 @
TH11 @
TH12 @
CL_CLK AR2 CL_CLK
CL_DATA AT5 CL_DATA
CL_RST# AU4 CL_RST#
P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11
L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3
N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7

M.2 SSD2 PCIE L1
<68> PCIE_PTX_DRX_P11
<68> PCIE_PTX_DRX_N11
<68> PCIE_PRX_DTX_P11
<68> PCIE_PRX_DTX_N11
C36 PCIE11_TXP/SATA0A_TXP
B36 PCIE11_TXN/SATA0A_TXN
F39 PCIE11_RXP/SATA0A_RXP
G38 PCIE11_RXN/SATA0A_RXN

20190918 Port4 change to Port3
DGPU_PRSNT#
AR42 GPP_F10/SATA_SCLOCK
AR48 GPP_F11/SATA_SLOAD
AU47 GPP_F13/SATA_SDATAOUT0
AU46 GPP_F12/SATA_SDATAOUT1

GLAN
<73> PCIE_PTX_DRX_N14
<73> PCIE_PTX_DRX_P14
<73> PCIE_PRX_DTX_N14
<73> PCIE_PRX_DTX_P14
PCIE_PTX_DRX_N14
PCIE_PTX_DRX_P14
PCIE_PRX_DTX_N14
PCIE_PRX_DTX_P14
C39 PCIE14_TXN/SATA1B_TXN
D39 PCIE14_TXP/SATA1B_TXP
D46 PCIE14_RXN/SATA1B_RXN
C47 PCIE14_RXP/SATA1B_RXP

HDD
<67> SATA_PTX_DRX_N0B
<67> SATA_PTX_DRX_P0B
<67> SATA_PRX_DTX_N0B
<67> SATA_PRX_DTX_P0B
SATA_PTX_DRX_N0B
SATA_PTX_DRX_P0B
SATA_PRX_DTX_N0B
SATA_PRX_DTX_P0B
B38 PCIE13_TXN/SATA0B_TXN
C38 PCIE13_TXP/SATA0B_TXP
C45 PCIE13_RXN/SATA0B_RXN
C46 PCIE13_RXP/SATA0B_RXP
20191016
- HDD change to Port 0B

M.2 SSD2 PCIE L0
<68> PCIE_PTX_DRX_P12
<68> PCIE_PTX_DRX_N12
<68> PCIE_PRX_DTX_P12
<68> PCIE_PRX_DTX_N12
E37 PCIE12_TXP/SATA1A_TXP
D38 PCIE12_TXN/SATA1A_TXN
J41 PCIE12_RXP/SATA_1A_RXP
H42 PCIE12_RXN/SATA1A_RXN

M.2 SSD3 PCIE L3
M.2 SSD3 PCIE L2
20190918
<69> PCIE_PTX_DRX_P20
<69> PCIE_PTX_DRX_N20
<69> PCIE_PRX_DTX_P20
<69> PCIE_PRX_DTX_N20
<69> PCIE_PTX_DRX_P19
<69> PCIE_PTX_DRX_N19
<69> PCIE_PRX_DTX_P19
<69> PCIE_PRX_DTX_N19
PCIE_PTX_DRX_P20
PCIE_PTX_DRX_N20
PCIE_PRX_DTX_P20
PCIE_PRX_DTX_N20
PCIE_PTX_DRX_P19
PCIE_PTX_DRX_N19
PCIE_PRX_DTX_P19
PCIE_PRX_DTX_N19
B44 PCIE20_TXP/SATA7_TXP
A44 PCIE20_TXN/SATA7_TXN
R37 PCIE20_RXP/SATA7_RXP
R35 PCIE20_RXN/SATA7_RXN
D43 PCIE19_TXP/SATA6_TXP
C44 PCIE19_TXN/SATA6_TXN
N42 PCIE19_RXP/SATA6_RXP
M44 PCIE19_RXN/SATA6_RXN
3 OF 13
CNP-H_BGA874
Rev1.0

PCIE9_RXN G36
PCIE9_RXP F36
PCIE9_TXN C34
PCIE9_TXP D34
PCIE_PRX_DTX_N9
PCIE_PRX_DTX_P9
PCIE_PTX_DRX_N9
PCIE_PTX_DRX_P9
PCIE_PRX_DTX_N9 <68>
PCIE_PRX_DTX_P9 <68>
PCIE_PTX_DRX_N9 <68>
PCIE_PTX_DRX_P9 <68>
M.2 SSD2 PCIE L3

PCIE10_RXN K37
PCIE10_RXP J37
PCIE10_TXN C35
PCIE10_TXP B35
PCIE_PRX_DTX_N10
PCIE_PRX_DTX_P10
PCIE_PTX_DRX_N10
PCIE_PTX_DRX_P10
PCIE_PRX_DTX_N10 <68>
PCIE_PRX_DTX_P10 <68>
PCIE_PTX_DRX_N10 <68>
PCIE_PTX_DRX_P10 <68>
M.2 SSD2 PCIE L2

PCIE15_RXN/SATA2_RXN F44
PCIE15_RXP/SATA2_RXP E45
PCIE_15_SATA_2_TXN B40
PCIE15_TXP/SATA2_TXP C40
PCIE_PRX_DTX_N15
PCIE_PRX_DTX_P15
PCIE_PTX_DRX_N15
PCIE_PTX_DRX_P15
.1U_0402_16V7K 1 2 CH1
.1U_0402_16V7K 1 2 CH2
PCIE_PRX_DTX_N15 <52>
PCIE_PRX_DTX_P15 <52>
PCIE_PTX_C_DRX_N15 <52>
PCIE_PTX_C_DRX_P15 <52>
NGFF
WL+BT(KEY E)

PCIE16_RXN/SATA3_RXN L41
PCIE16_RXP/SATA3_RXP M40
PCIE16_TXN/SATA3_TXN B41
PCIE16_TXP/SATA3_TXP C41

PCIE17_RXN/SATA4_RXN K43
PCIE17_RXP/SATA4_RXP K44
PCIE17_TXN/SATA4_TXN A42
PCIE17_TXP/SATA4_TXP B42
PCIE_PRX_DTX_N17
PCIE_PRX_DTX_P17
PCIE_PTX_DRX_N17
PCIE_PTX_DRX_P17
PCIE_PRX_DTX_N17 <69>
PCIE_PRX_DTX_P17 <69>
PCIE_PTX_DRX_N17 <69>
PCIE_PTX_DRX_P17 <69>
M.2 SSD3 PCIE L0

PCIE18_RXN/SATA5_RXN P41
PCIE18_RXP/SATA5_RXP R40
PCIE18_TXN/SATA5_TXN C42
PCIE18_TXP/SATA5_TXP D42
PCIE_PRX_DTX_N18
PCIE_PRX_DTX_P18
PCIE_PTX_DRX_N18
PCIE_PTX_DRX_P18
PCIE_PRX_DTX_N18 <69>
PCIE_PRX_DTX_P18 <69>
PCIE_PTX_DRX_N18 <69>
PCIE_PTX_DRX_P18 <69>
M.2 SSD3 PCIE L1
20190918

GPP_E8/SATA_LED# AK48
GPP_E0/SATAXPCIE0/SATAGP0 AH41
GPP_E1/SATAXPCIE1/SATAGP1 AJ43
GPP_E2/SATAXPCIE2/SATAGP2 AK47
GPP_F0/SATAXPCIE3/SATAGP_3 AN47
GPP_F1/SATAXPCIE4/SATAGP4 AM46
GPP_F2/SATAXPCIE5/SATAGP5 AM43
GPP_F3/SATAXPCIE6/SATAGP6 AM47
GPP_F4/SATAXPCIE7/SATAGP7 AM48
SATA_GP1
SATA_GP2
SATA_GP4
SATA_GP5
RH187 1 PBA@ 2 10K_0402_5%
TH50
TH13
SATA_GP1 <68>
SATA_GP4 <69>
20191206
- JSSD3 detect pin change to SATA_GP4

GPP_F21/EDP_BKLTCTL AU48
GPP_F20/EDP_BKLTEN AV46
GPP_F19/EDP_VDDEN AV44
PCH_BKL_PWM
ENBKL
PCH_ENVDD
PCH_BKL_PWM <38>
ENBKL <58>
PCH_ENVDD <38>

THRMTRIP# AD3
PECI AF2
PM_SYNC AF3
PLTRST_CPU# AG5
PM_DOWN AE2
PCH_THERMTRIP#
PCH_PECI
H_PM_SYNC
H_PLTRST_CPU#
H_PM_DOWN_R
RH40 1 2 620_0402_5%
RH41 1 @ 2 13_0402_5%
RH42 1 2 30_0402_5%
#571391_CFL_H_PDG_Rev0p5.pdf
H_PECI
H_PM_SYNC_R
PCH_THERMTRIP#_R <10>
H_PECI <10,58>
H_PM_SYNC_R <10>
H_PLTRST_CPU# <10>
H_PM_DOWN_R <10>

+3VS
SATA_GP4 RH3032 1 10K_0402_5%
SATA_GP1 RH39 2 1 10K_0402_5%
M.2 SSD PCIE/SATA select pin

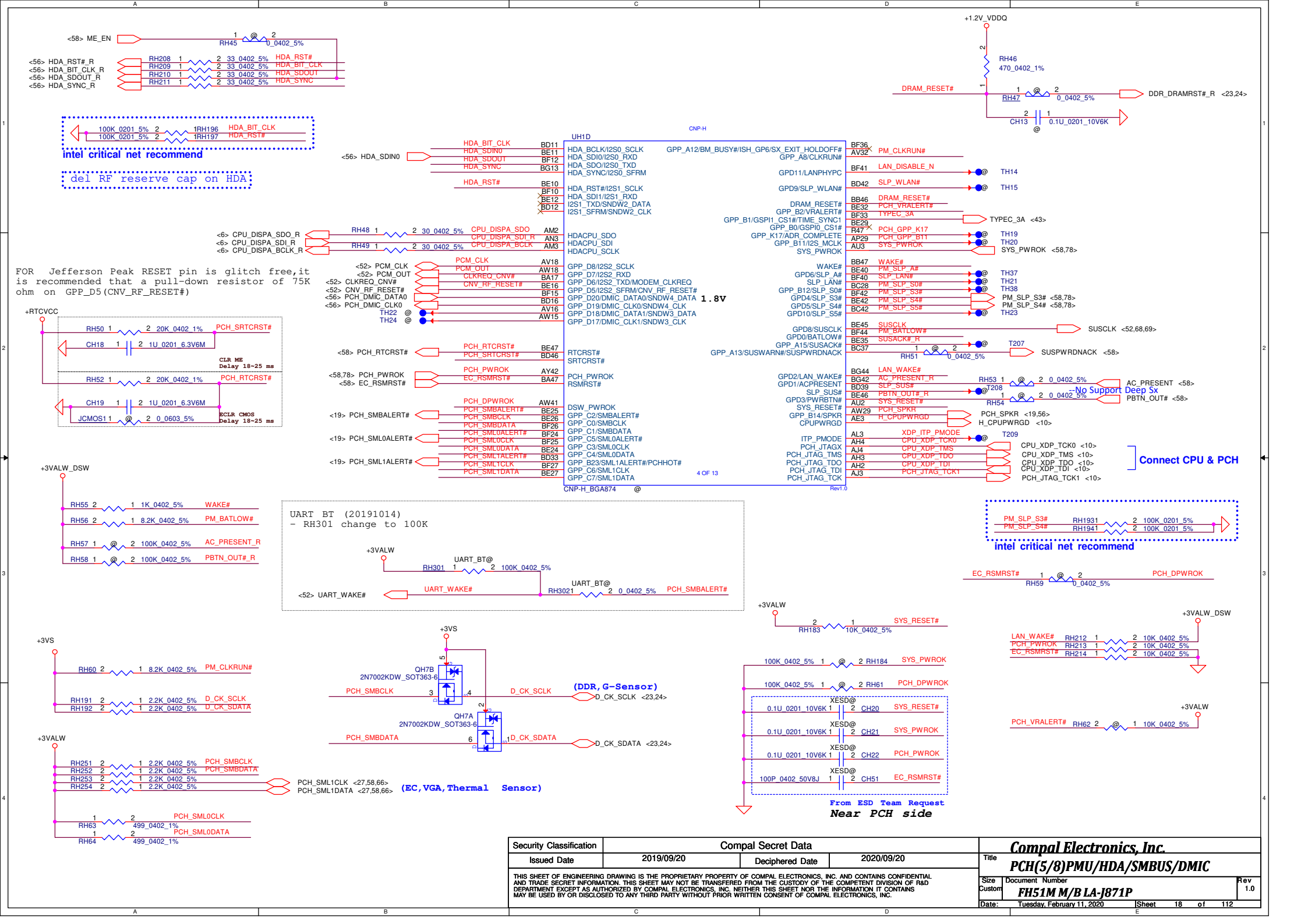
H_PECI 0.1U_0201_10V6K 1 XESD@ 2 CH50

+3VALW
RH43 10K_0402_5% UMA@
DGPU_PRSNT#
RH44 10K_0402_5% VGA@

	GPP_F13 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.
Title: PCIE/SATA/USB3/eSPI
Size: Custom
Document Number: FH51M M/B LA-J871P
Rev: 1.0
Date: Tuesday, February 11, 2020
Sheet 17 of 112



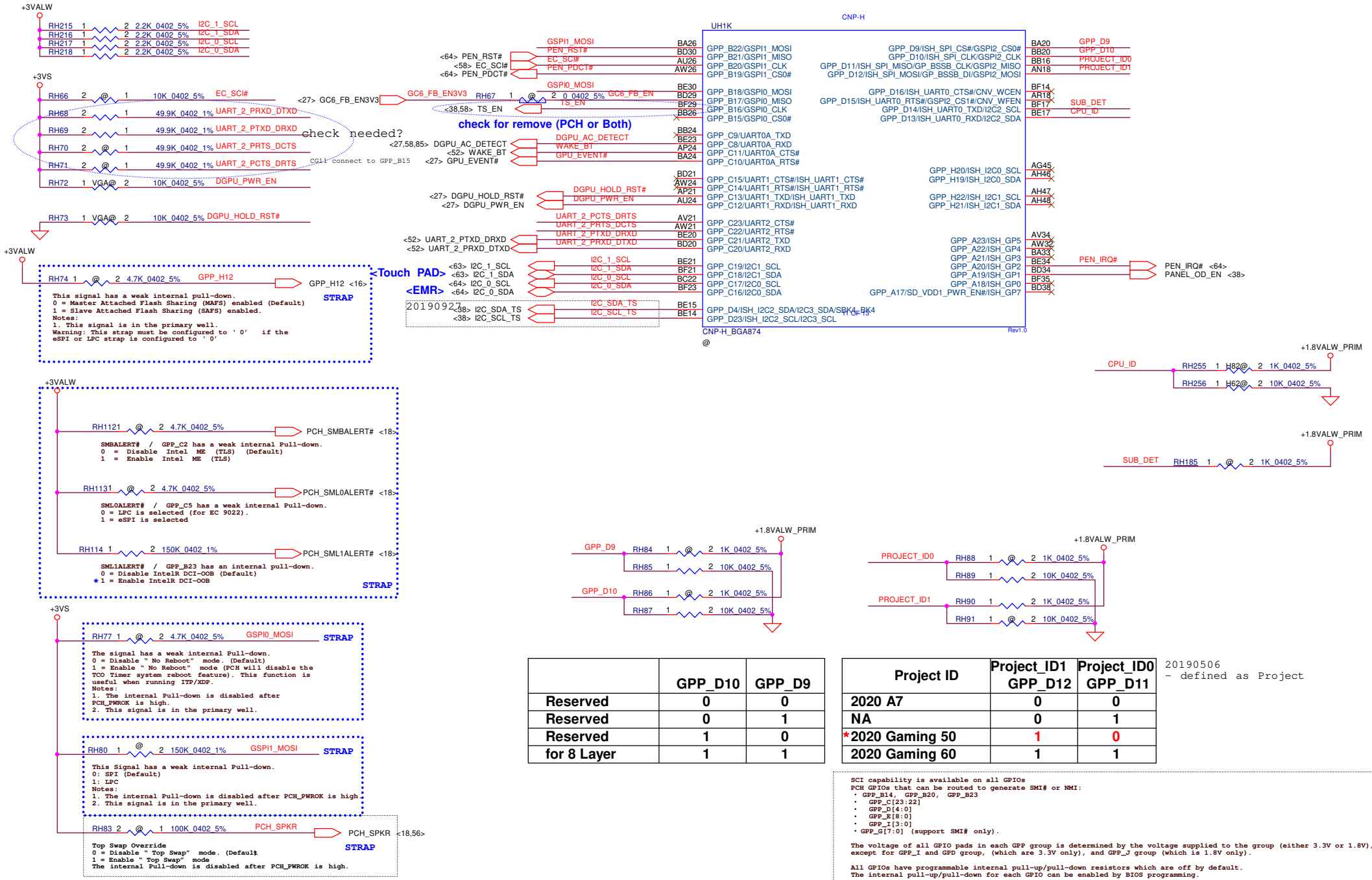
Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS/DMIC

Size	Document Number	Rev
Custom	FH51M M/B LA-J871P	1.0

Date: Tuesday, February 11, 2020 Sheet 18 of 112



	GPP_D10	GPP_D9
Reserved	0	0
Reserved	0	1
Reserved	1	0
for 8 Layer	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
2020 A7	0	0
NA	0	1
*2020 Gaming 50	1	0
2020 Gaming 60	1	1

20190506
- defined as Project

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	FH51M M/B LA-J871P	1.0

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GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

Place Near UH1 VCCPRIM_1_0523~29 3-5MM FROM PACKAGE EDGE

place near VCCDUSB FOR W22/W23

1-3MM FROM PACKAGE VCCPRIM_MPHY W31

1-3MM FROM PACKAGE EDGE

1-5MM FROM PACKAGE EDGE FOR VCCAPLL C1/C2

1-3MM FROM PACKAGE EDGE FOR VCCA_BCLK V19

1-5MM FROM PACKAGE EDGE FOR VCCAPLL B1/B2/B3

1-3MM FROM PACKAGE EDGE

LC filter close to pin
1uF 1-3MM FROM PACKAGE EDGE

reserve filter follow CRB 8/21

1-3MM FROM PACKAGE FOR PGPPEF AE35/AE37

1-3MM FROM PACKAGE FOR PGPPHK AC35/AC36

1-3MM FROM PACKAGE FOR VCCPRIM AY8/BB7

reserved for cnvi

near AG19/AG20

change to 10k

20200114
- RH100 Change to R-short

Short pins AJ22,AJ23,AK22,AK23 together at surface layer from PDG Rev0.71

RH174 for 571391_CFL_H_PDG_Rev0p71.pdf

SP02000RO00

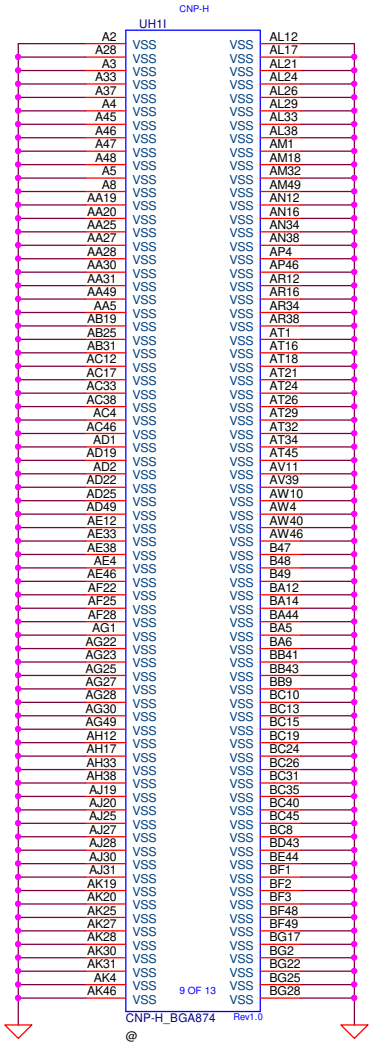
Security Classification	Compal Secret Data	
Issued Date	2019/09/20	Deciphered Date 2020/09/20

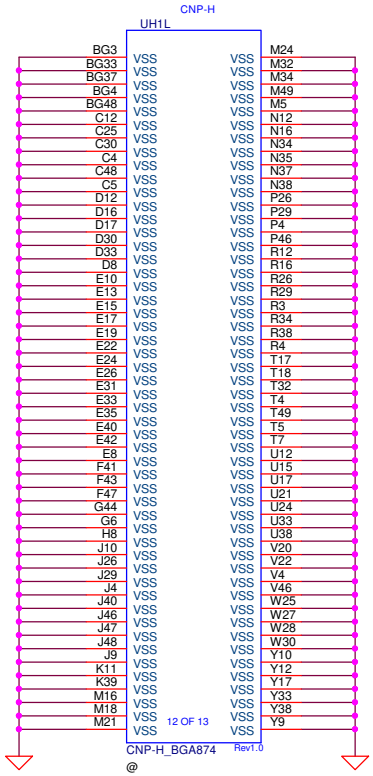
Compal Electronics, Inc.

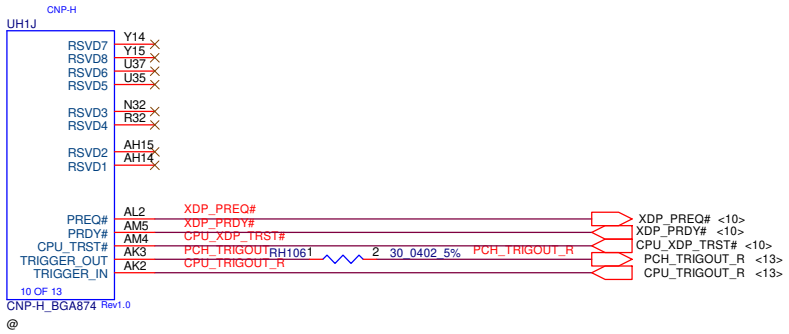
Title: PCH(7/8)Power

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 20 of 112







Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size: Custom | Document Number: FH51M M/B LA-J871P | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 21 of 112

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

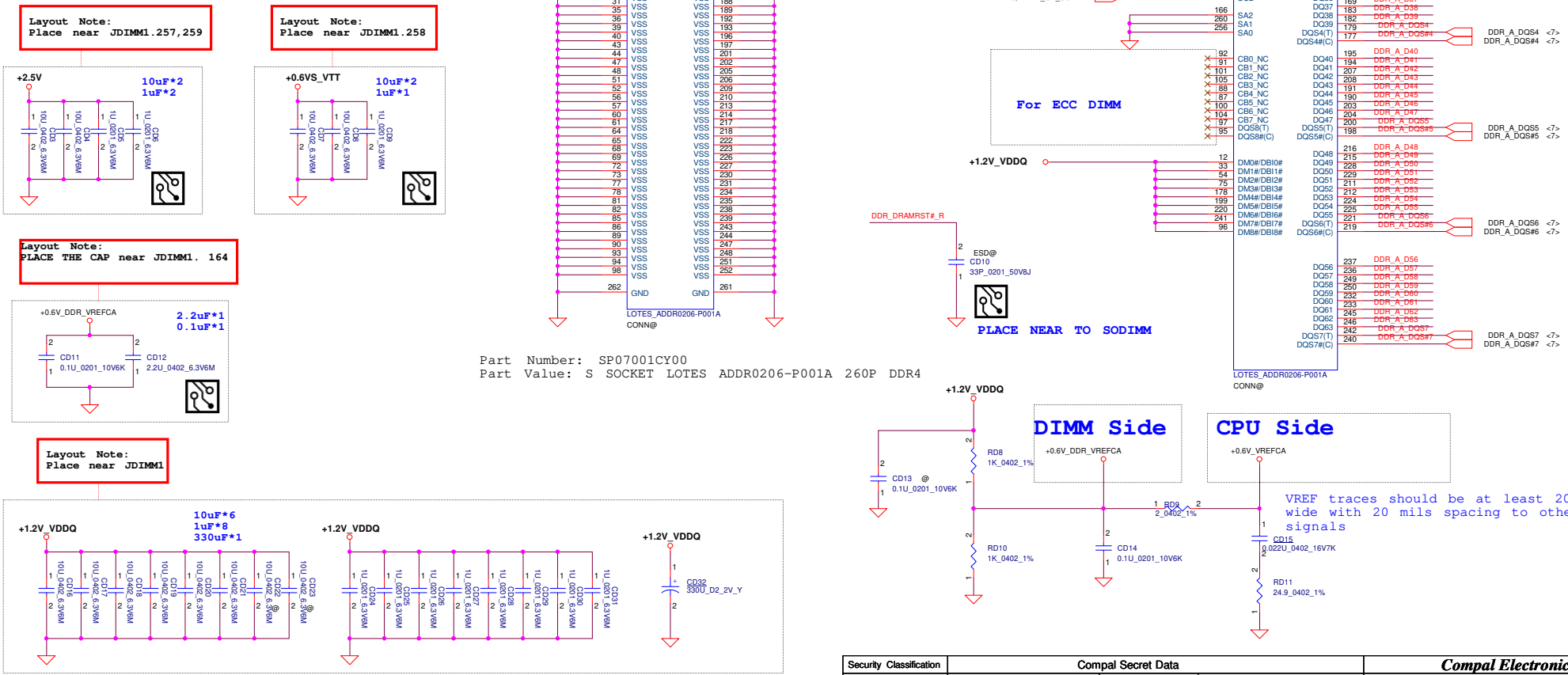
Title: *Reserve*

Size | Document Number: *FH51M M/B LA-J871P* | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 22 of 112

CHANNEL-A (Interleaved Memory)
> BOT : Reverse type (4mm)
> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



Part Number: SP07001CY00
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

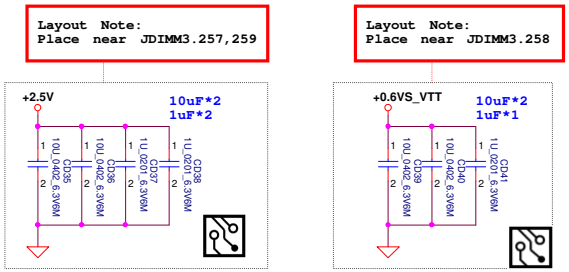
Title: **DDRIV_CHA: DIMM0**

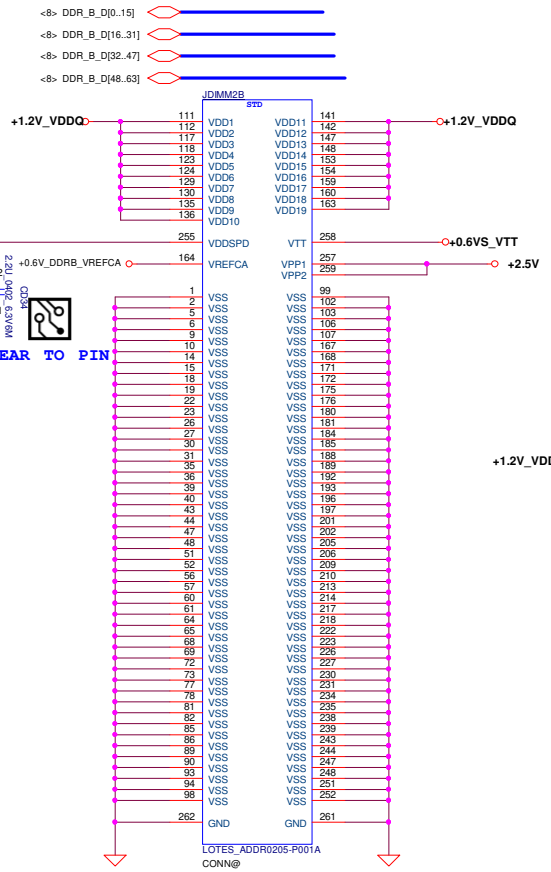
Size	Document Number	Rev
	FH51M M/B LA-J871P	1.0

Date: Tuesday, February 11, 2020 | Sheet 23 of 112

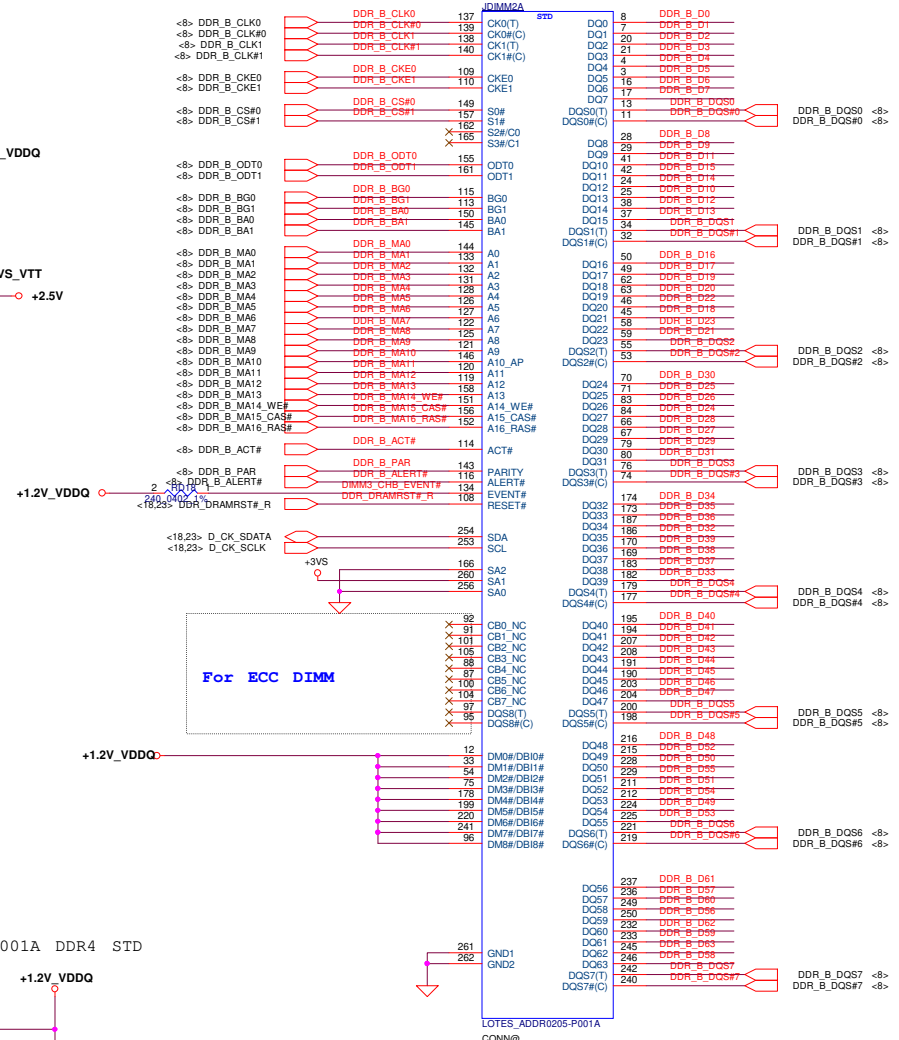
CHANNEL-B (Interleaved Memory)
> BOT : STD type (4mm)
> Non-ECC SO-DIMM

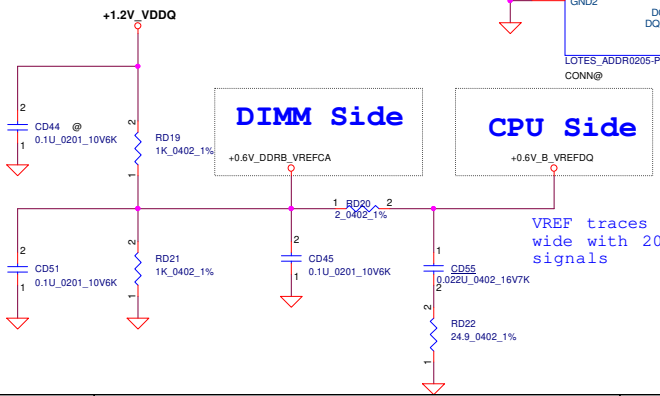
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S





Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD





Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size	Document Number	Rev
	FH51M M/B LA-J871P	1.0

Date: Tuesday, February 11, 2020 | Sheet 24 of 112

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.		
Title: *Reserve*		
Size	Document Number: *FH51M M/B LA-J871P*	Rev: 1.0
Date: Tuesday, February 11, 2020	Sheet 25 of 112	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: *Reserve*

Size | Document Number: *FH51M M/B LA-J871P* | Rev: 1.0

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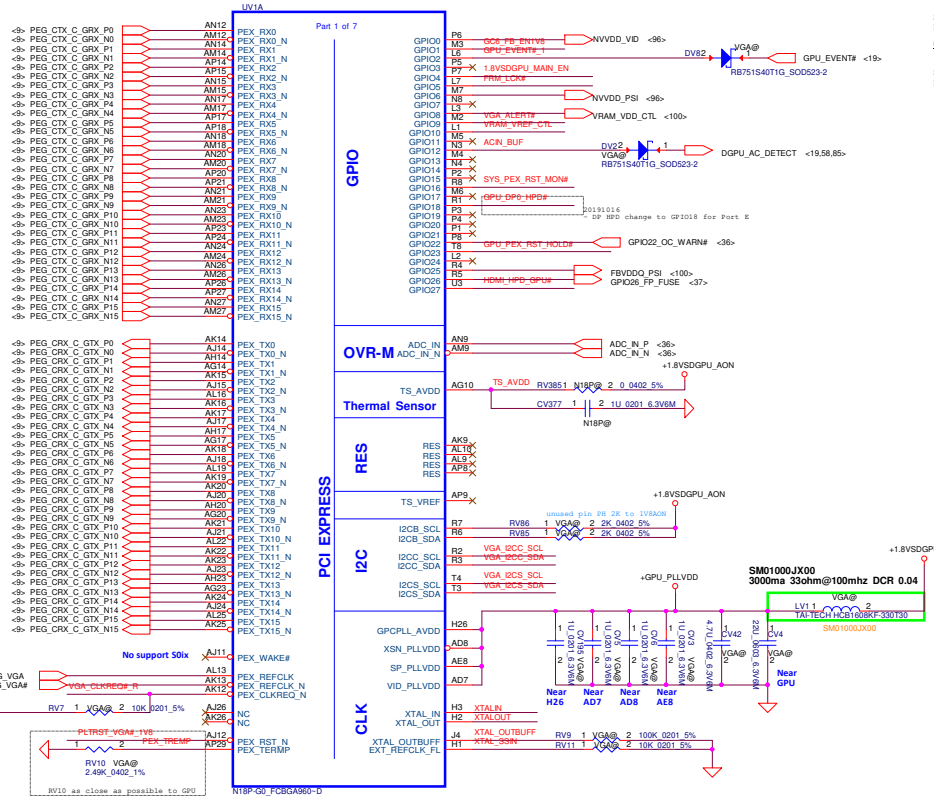
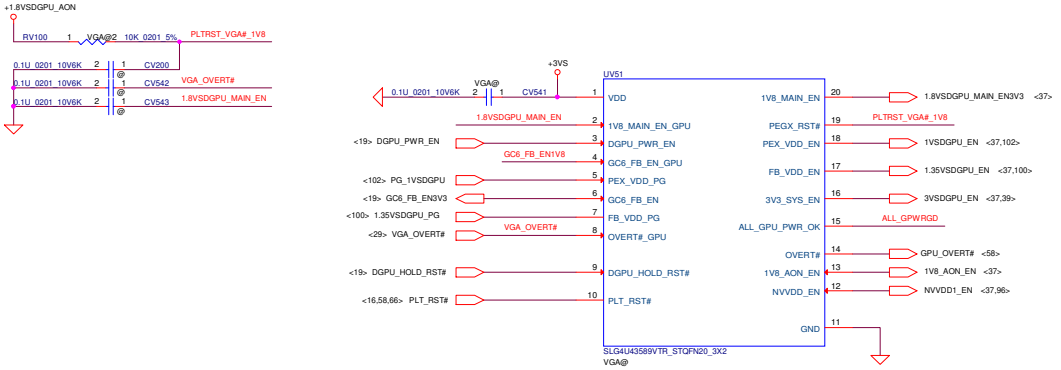
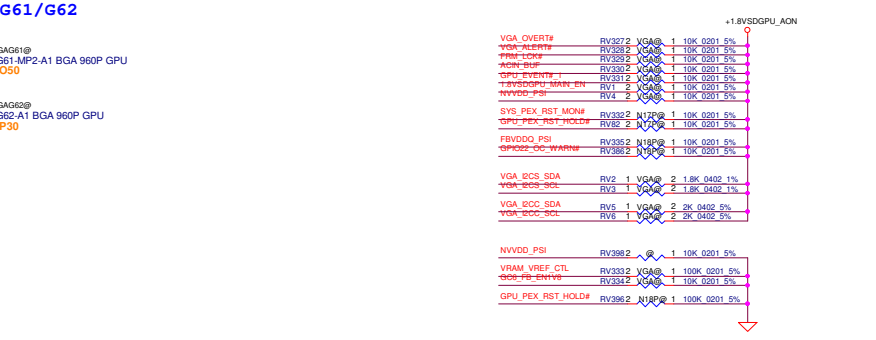
N18P-G61/G62

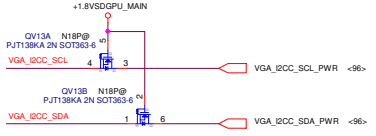
UV1 VGA61@ S IC N18P-G61-MP2-A1 BGA 960P GPU SA0000CZ050

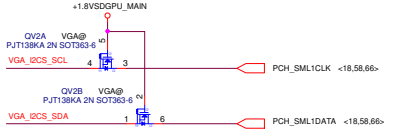
UV1 VGA62@ S IC N18P-G62-A1 BGA 960P GPU SA0000CZP30

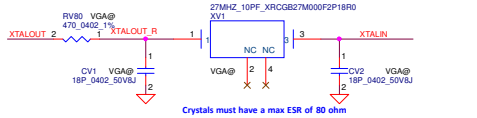


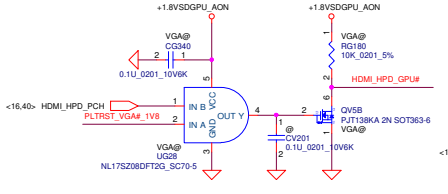


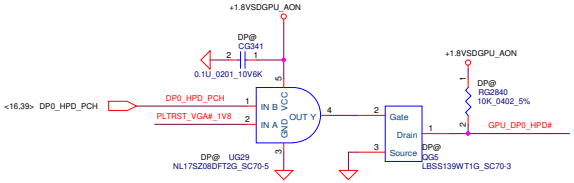


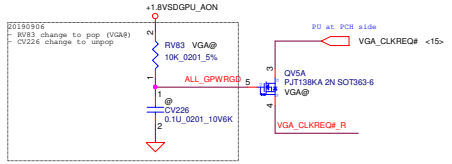












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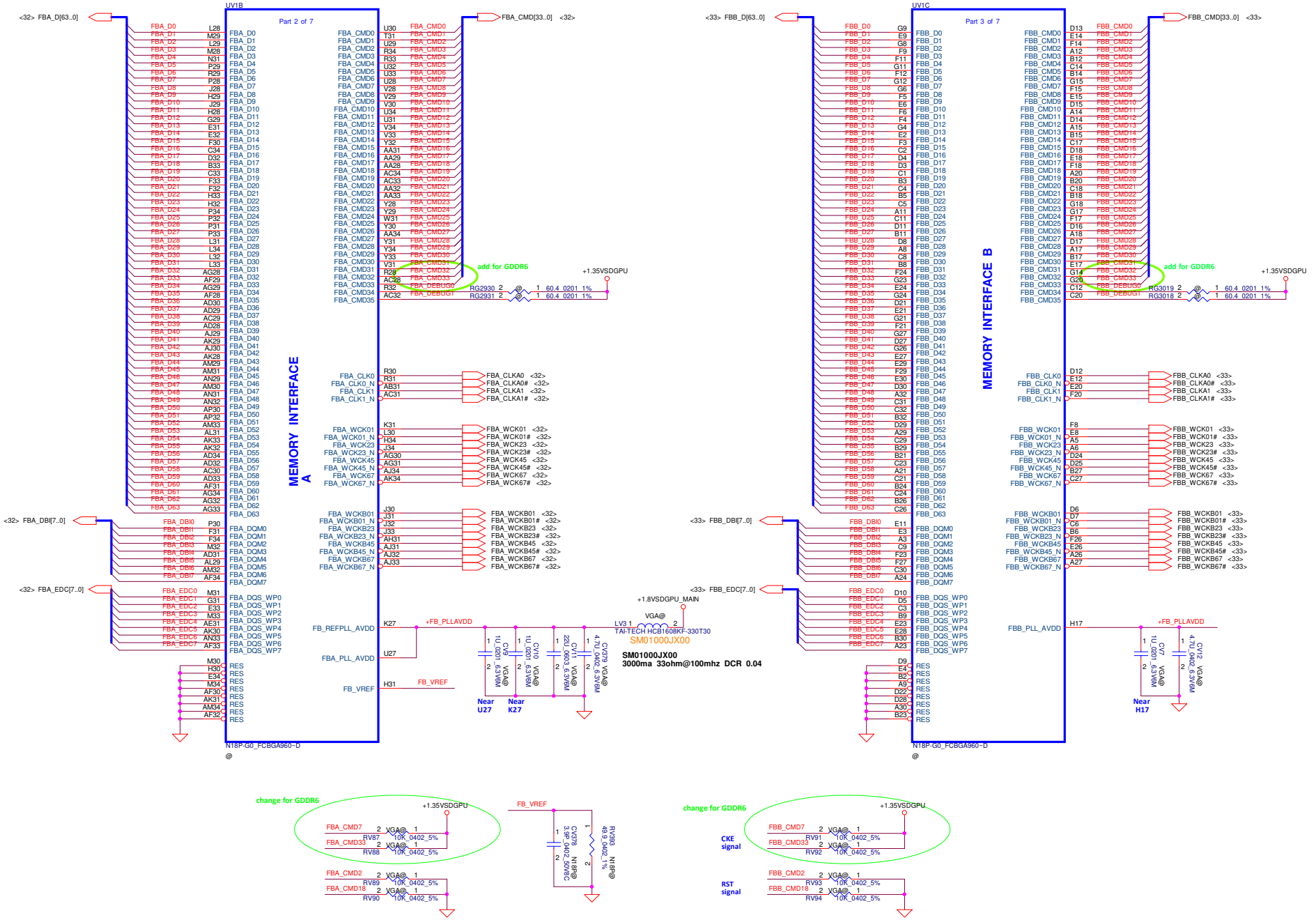

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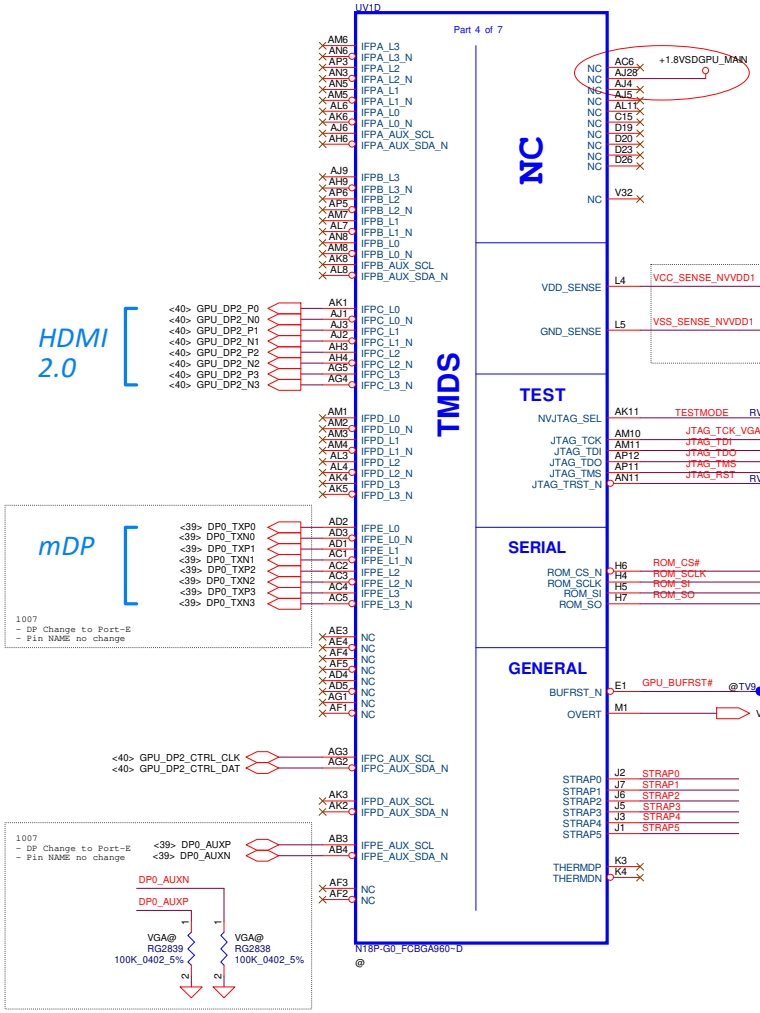
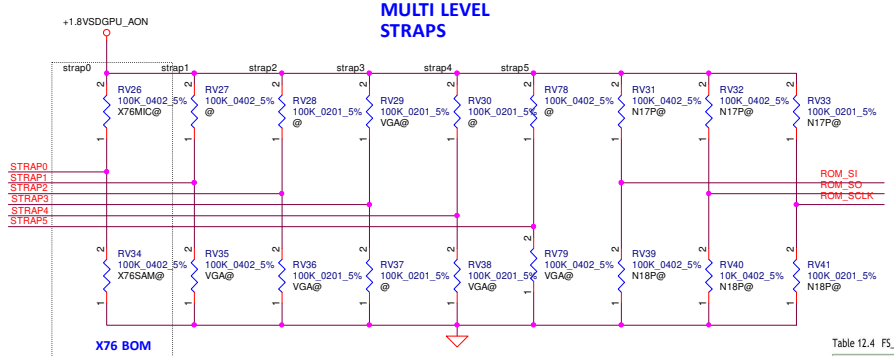




X76 BOM

UV4	X76SAM@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000C6280	X76MIC@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000BND80
UV5	X76SAM@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000C6280	X76MIC@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000BND80
UV6	X76SAM@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000C6280	X76MIC@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000BND80
UV7	X76SAM@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000C6280	X76MIC@ S IC D6 256M32 K4Z80325BC-HC14 FBGA 1.2V SA0000BND80

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Table 8. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[4]	Full	Production candidate

Notes:
1. For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
2. DVS is required to run WCLK > 5500 MHz.
3. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
4. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

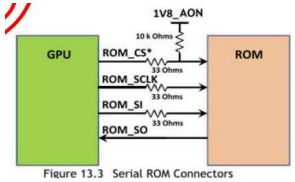
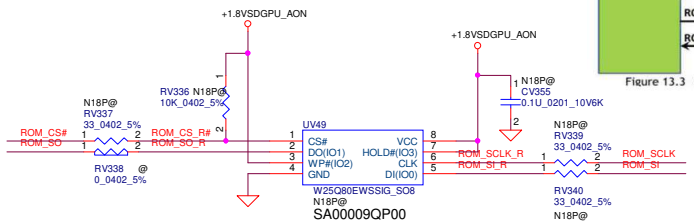


Figure 13.3 Serial ROM Connectors



DGPU VBIOS ROM 8Mb

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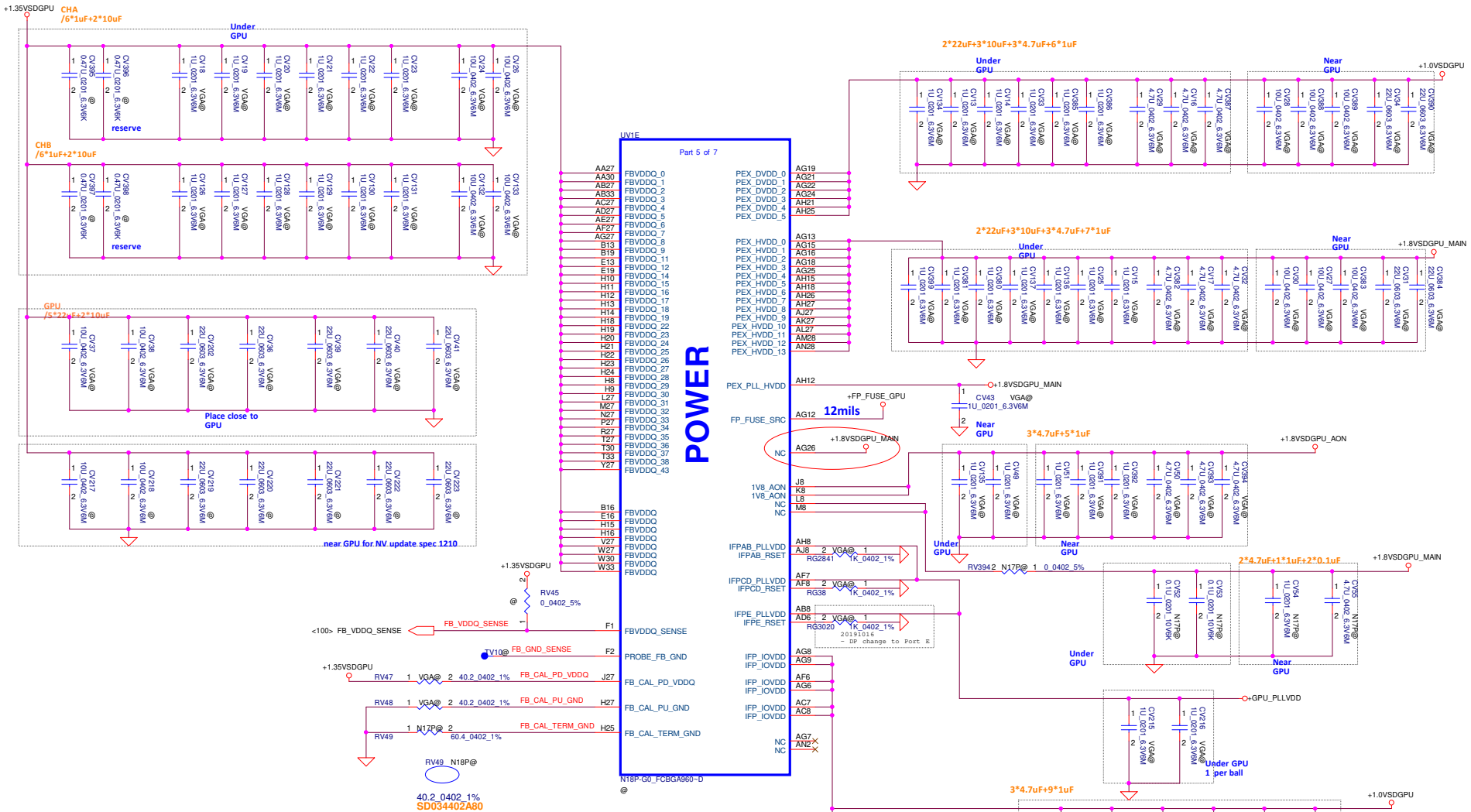

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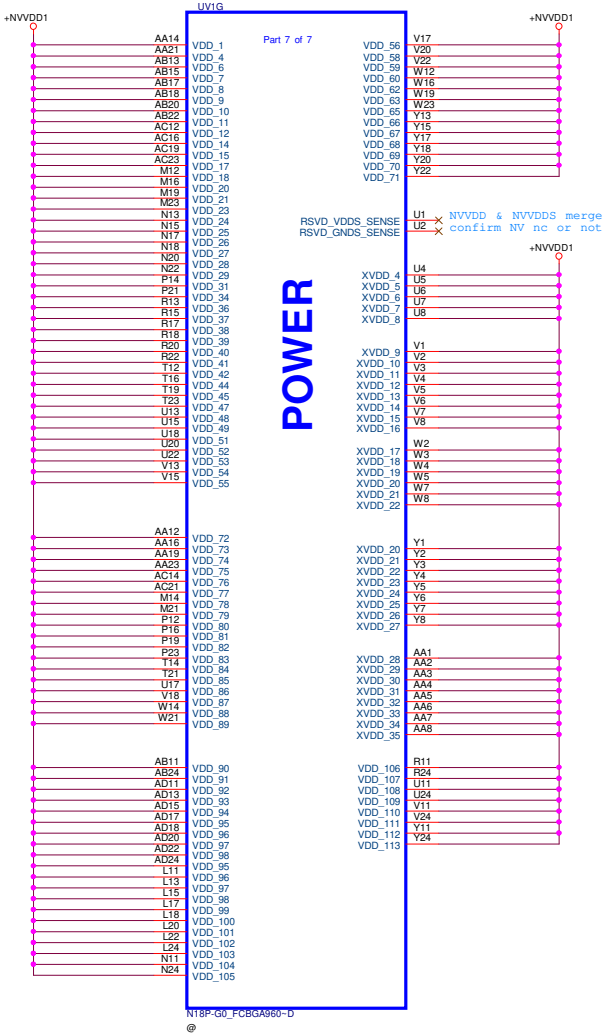
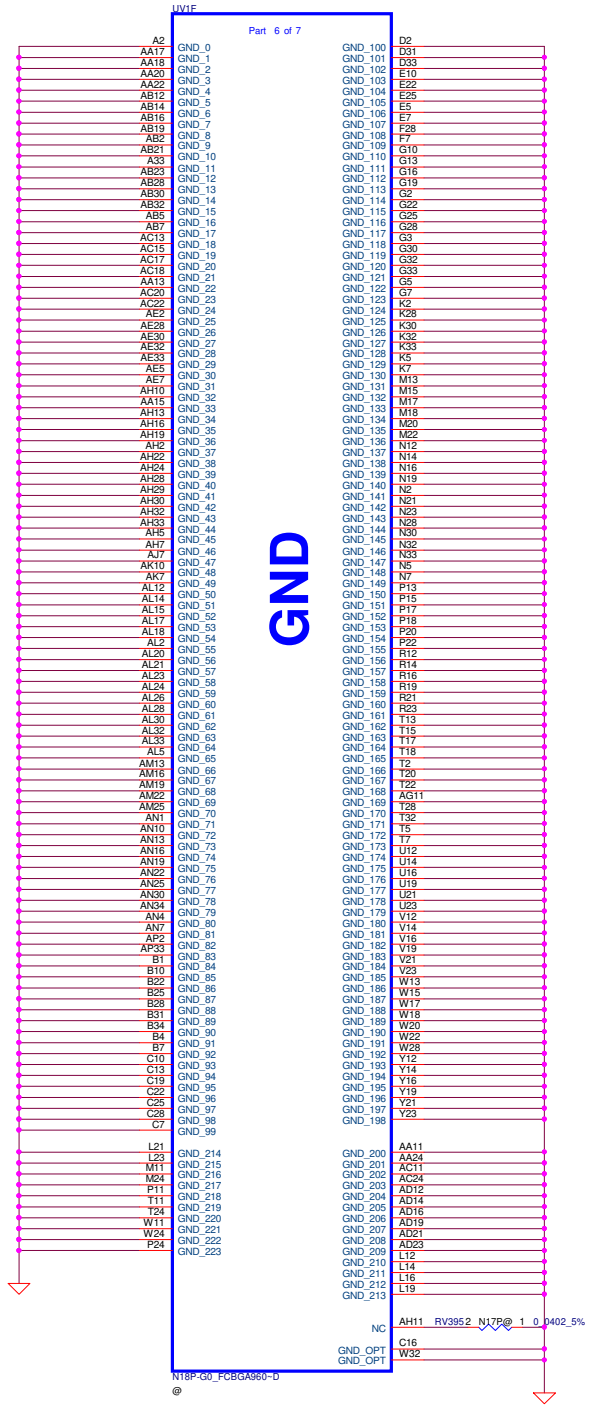
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2





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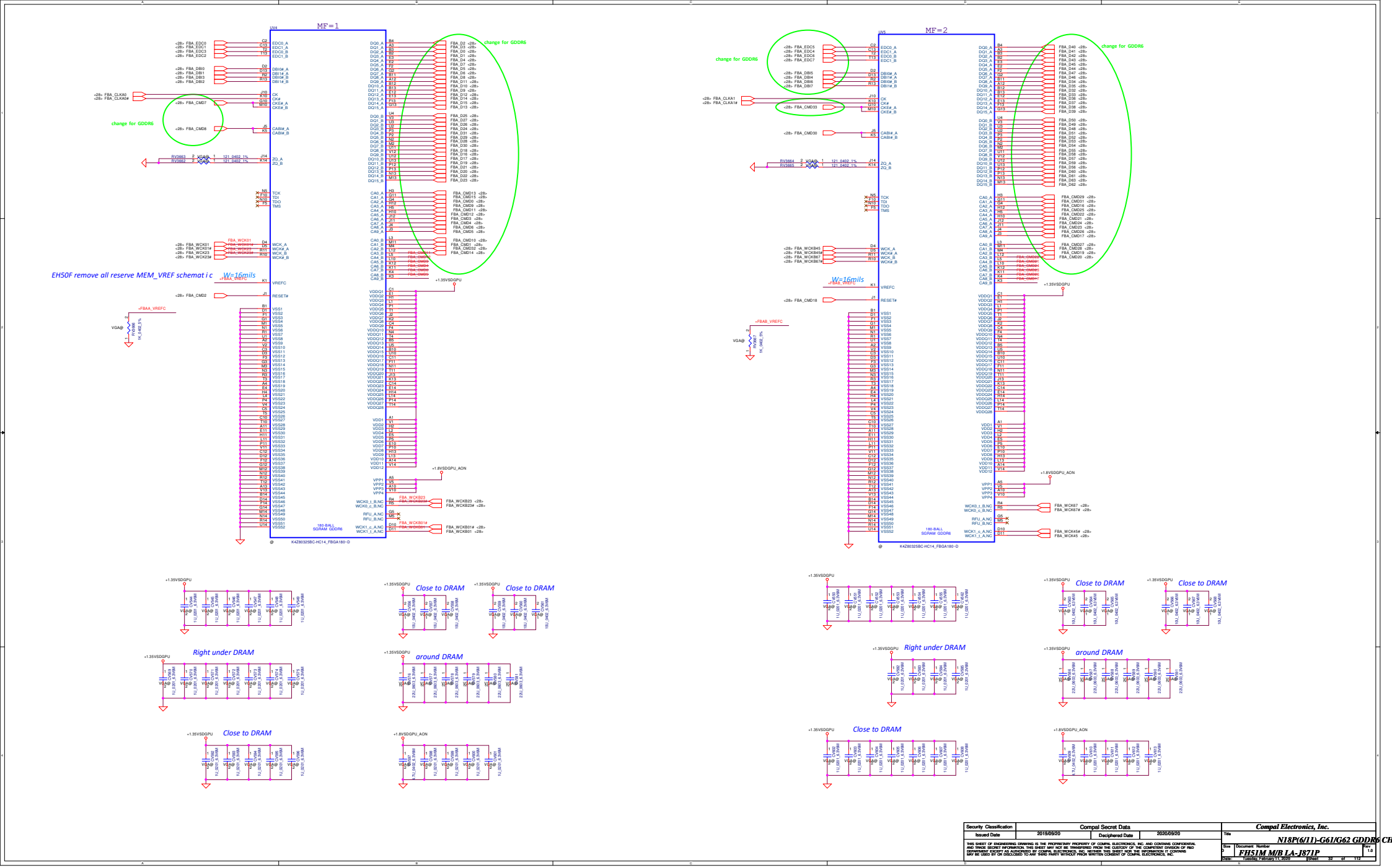

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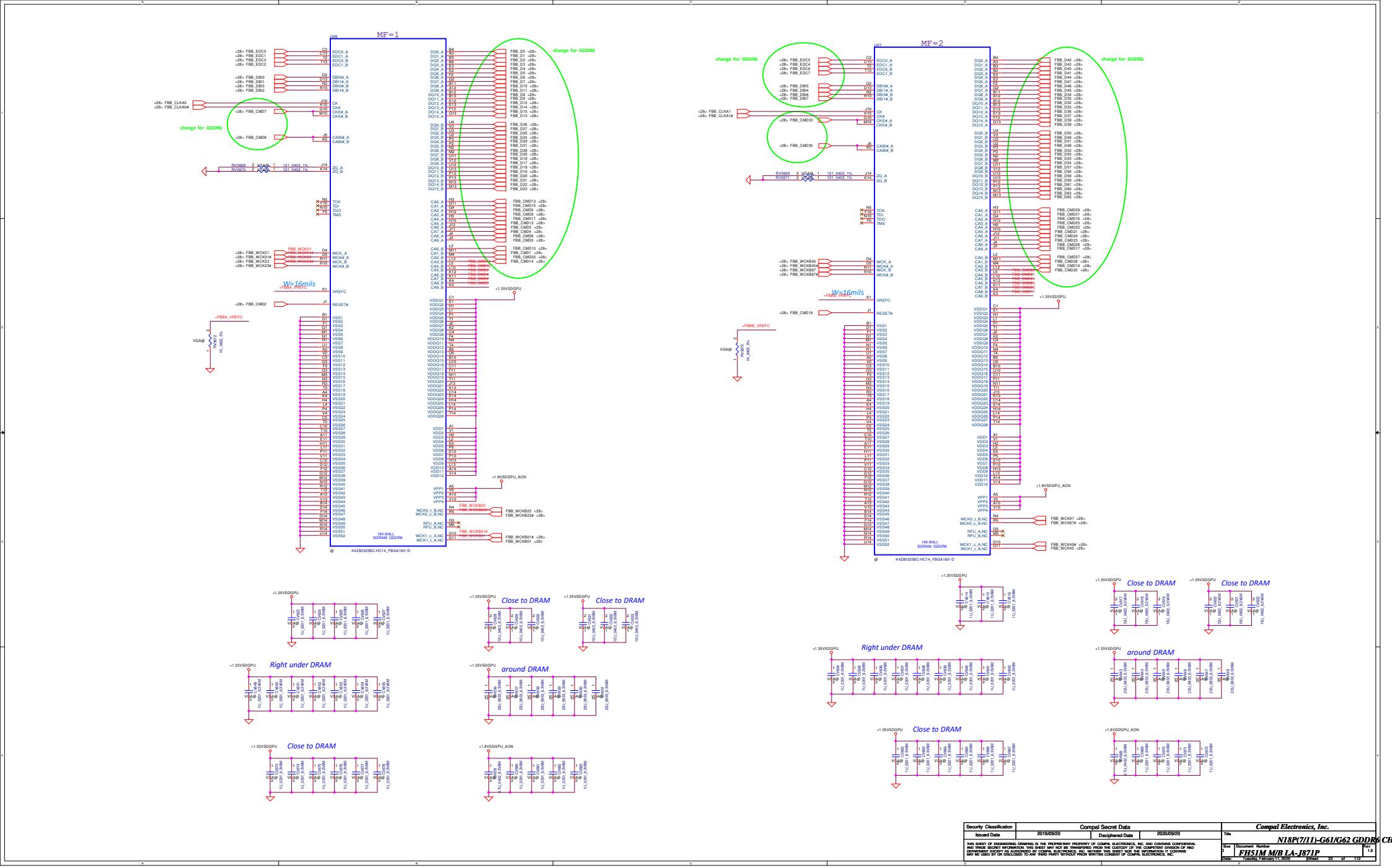

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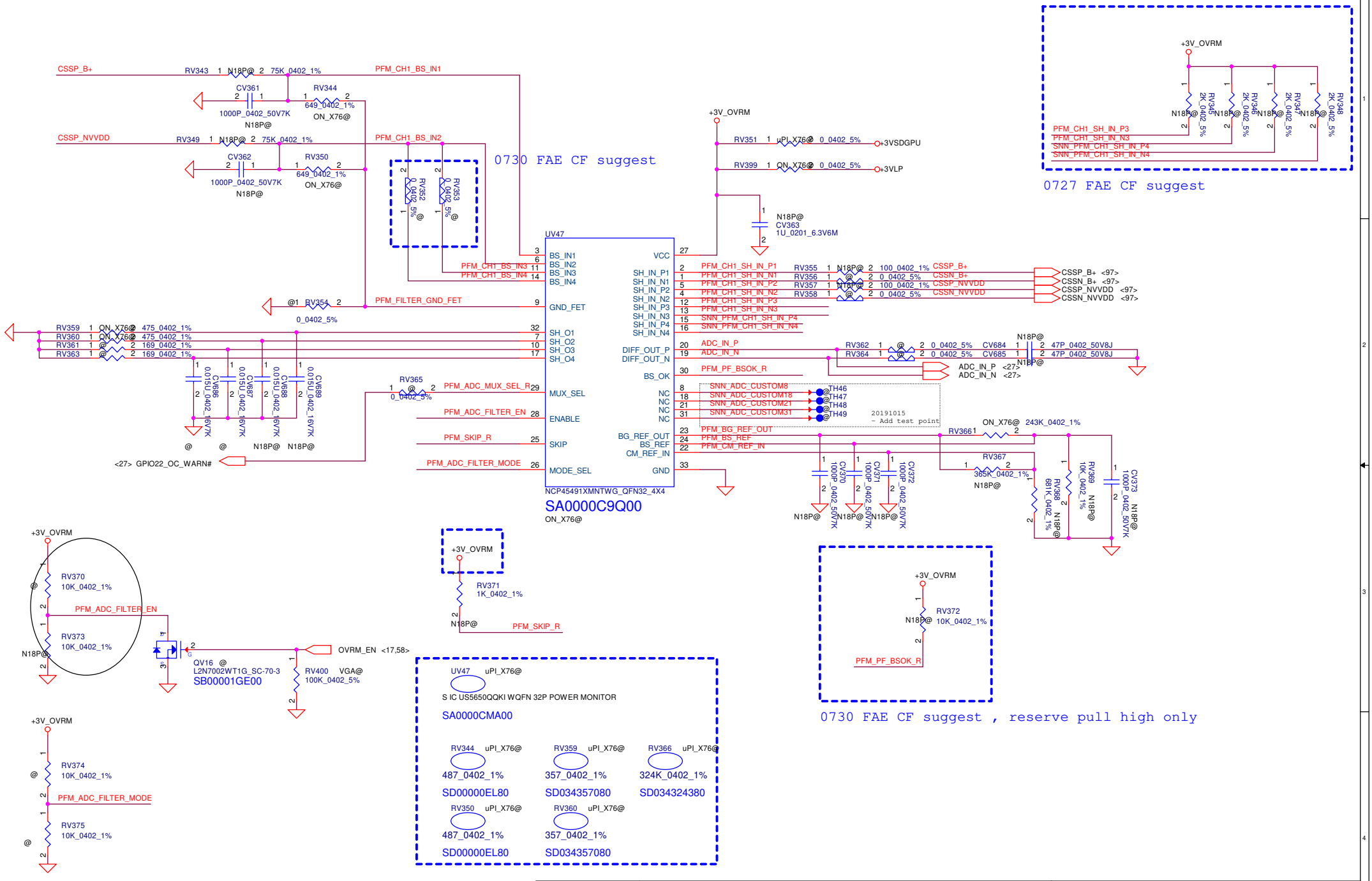
0730 FAE CF suggest
0727 FAE CF suggest
0730 FAE CF suggest , reserve pull high only
UV47
NCP45491XMNTWG_QFN32_4X4
SA0000C9Q00
ON_X76@
+3V_OVRM
+3VSDGPU
+3VLP
CSSP_B+
CSSP_NVVDD
PFM_CH1_BS_IN1
PFM_CH1_BS_IN2
PFM_CH1_BS_IN3
PFM_CH1_BS_IN4
PFM_FILTER_GND_FET
PFM_ADC_MUX_SEL_R
PFM_ADC_FILTER_EN
PFM_SKIP_R
PFM_ADC_FILTER_MODE
PFM_PF_BSOK_R
GPIO22_OC_WARN#
OVRM_EN
ADC_IN_P
ADC_IN_N
QV16 @
L2N7002WT1G_SC-70-3
SB00001GE00
S IC US5650QQKI WQFN 32P POWER MONITOR
SA0000CMA00
SD00000EL80
SD034357080
SD034324380
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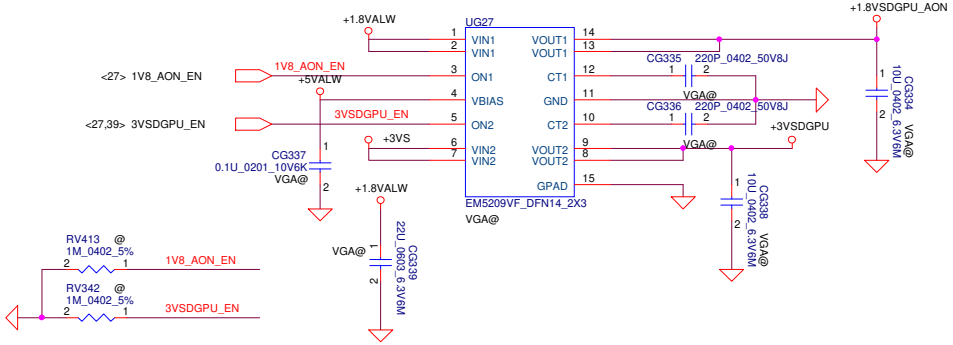
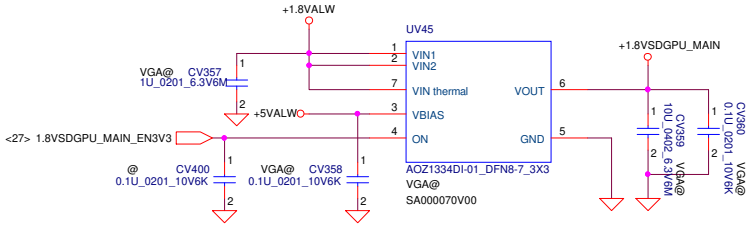
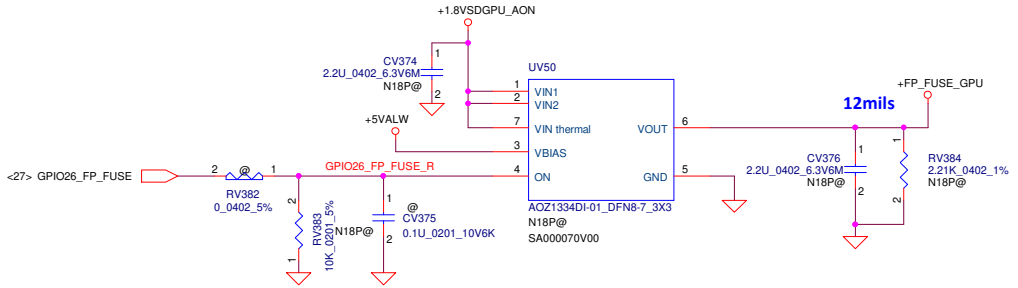
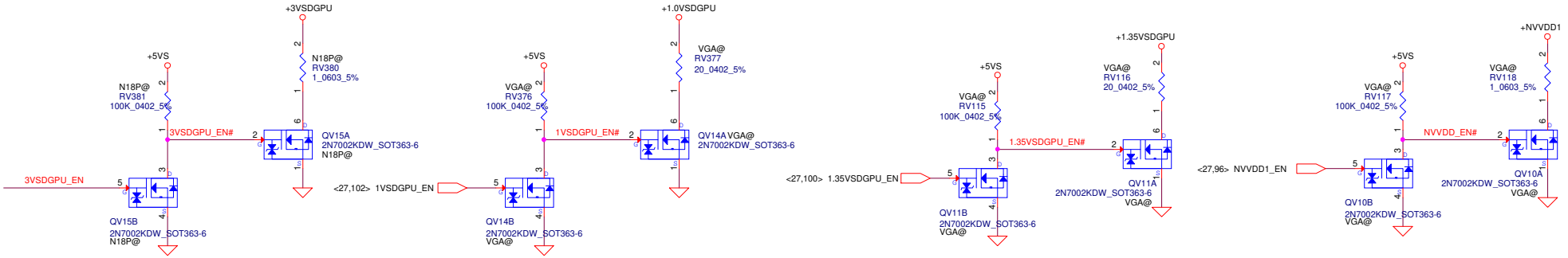
+1.8V_AON/+3VSDGPU



+1.8V_MAIN







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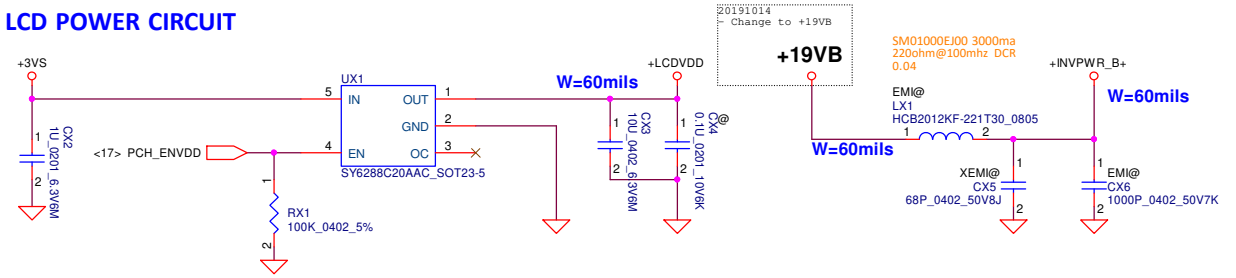
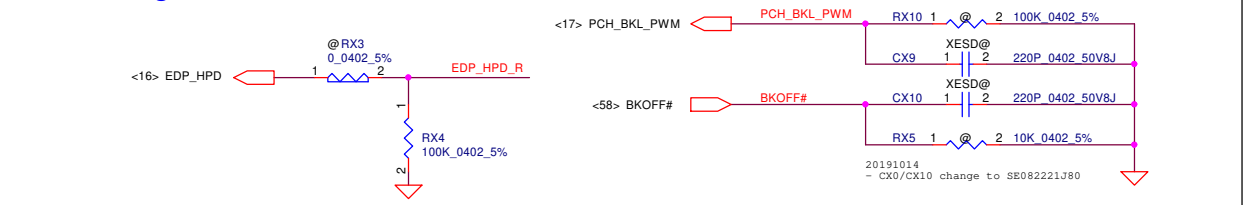
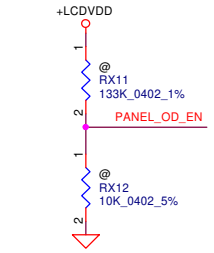
LCD POWER CIRCUIT



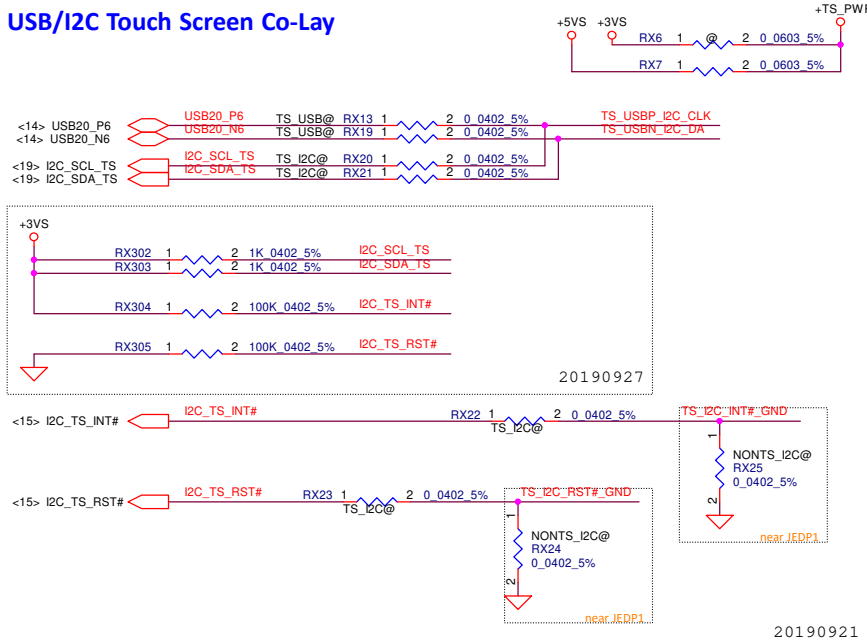
LCD enable signal



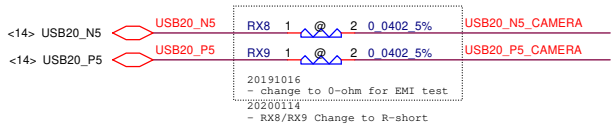
Panel OD



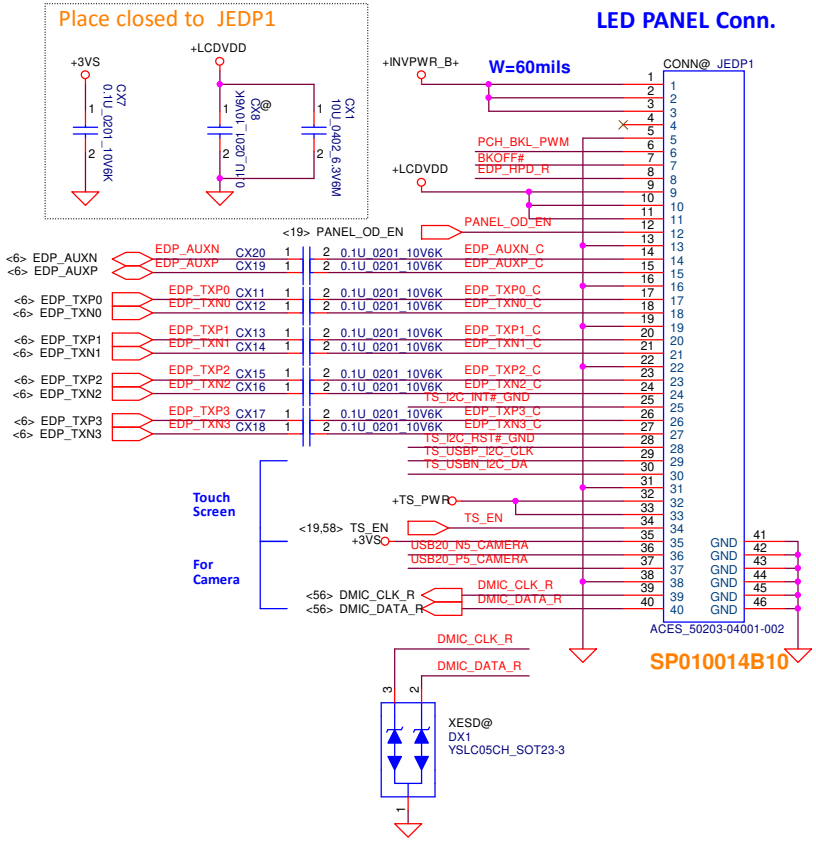
USB/I2C Touch Screen Co-Lay



CAMERA



LED PANEL Conn.



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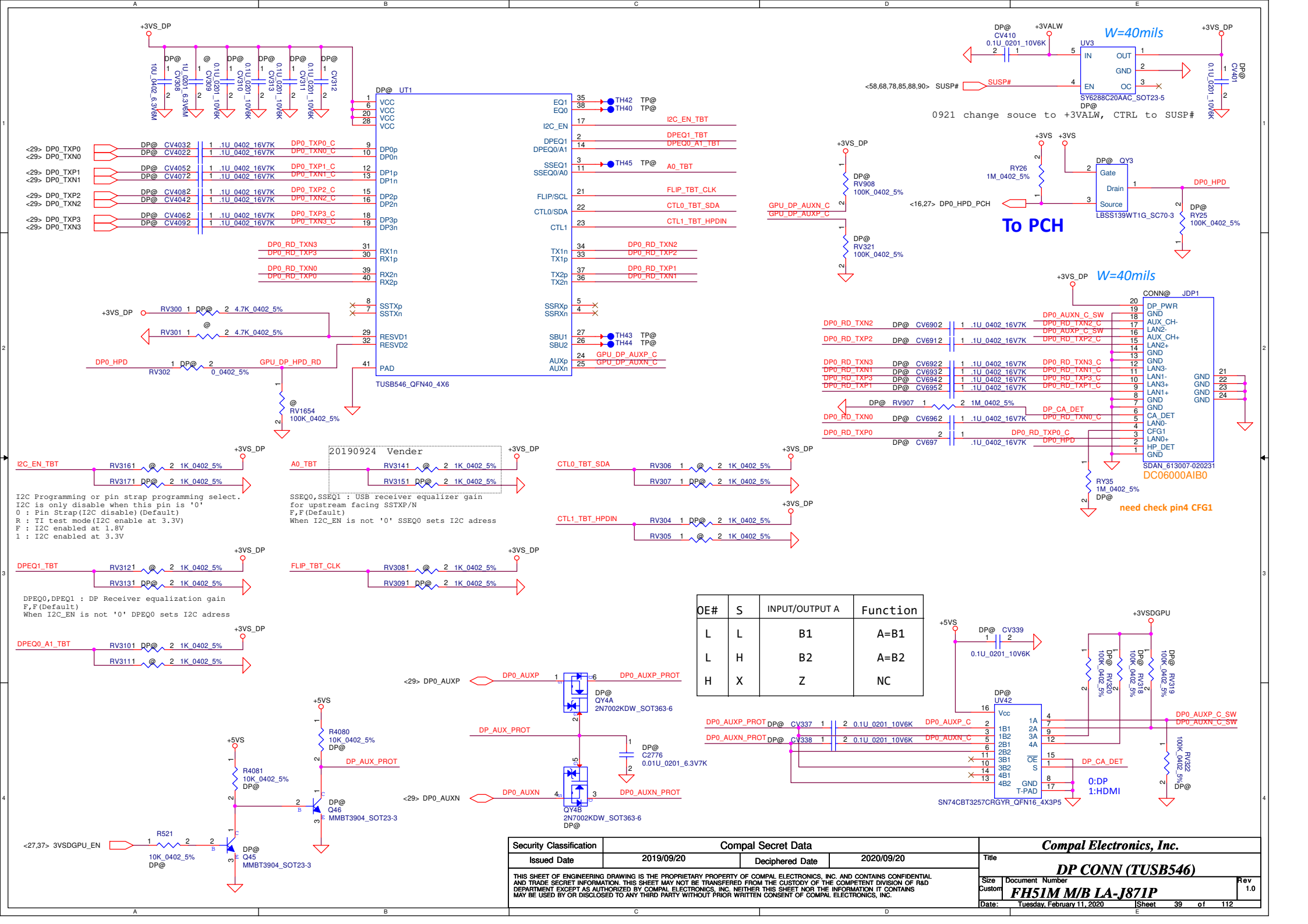

OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

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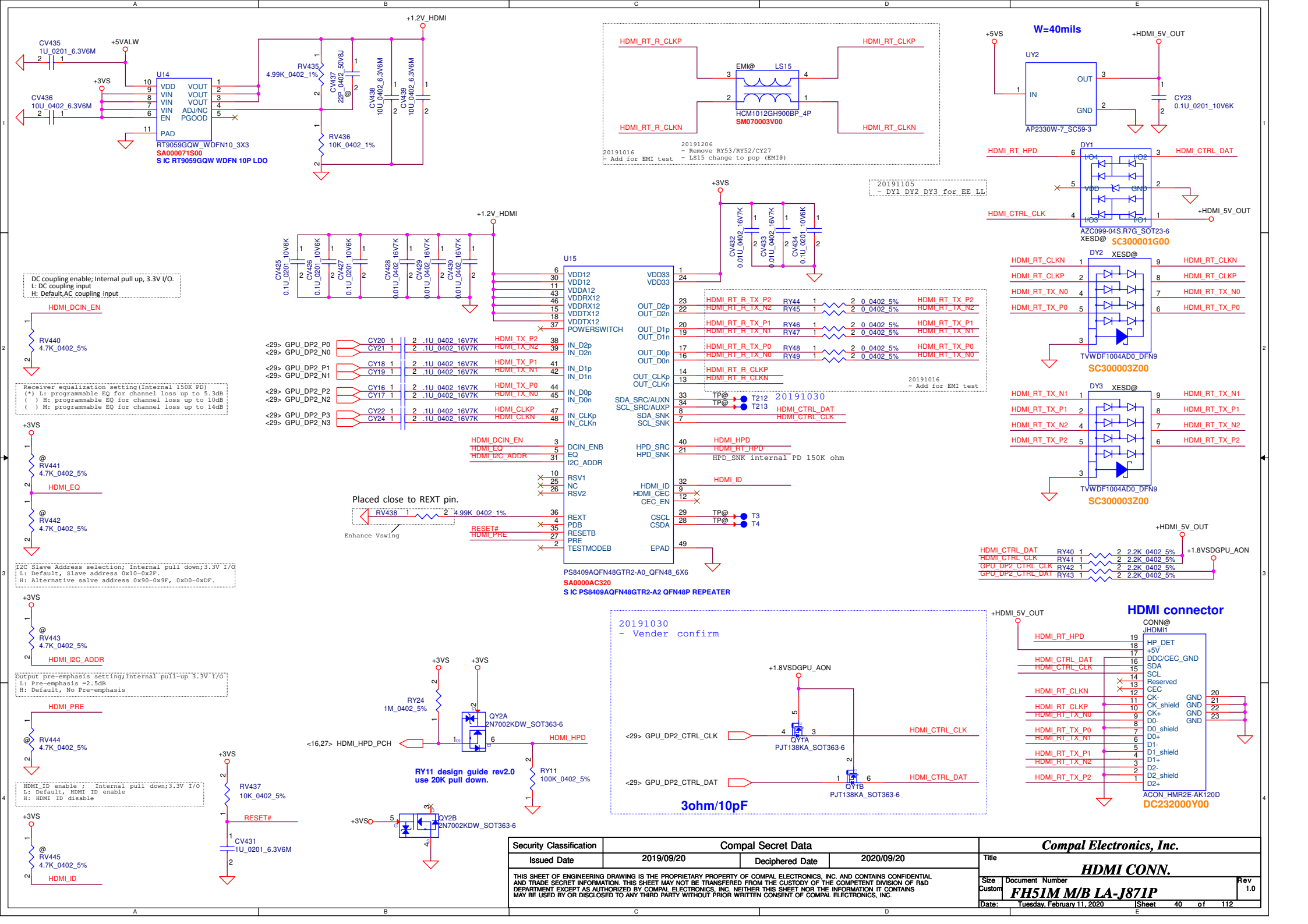

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Title: *N18E-GDDR6_D*

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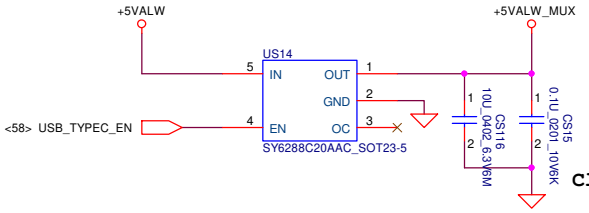
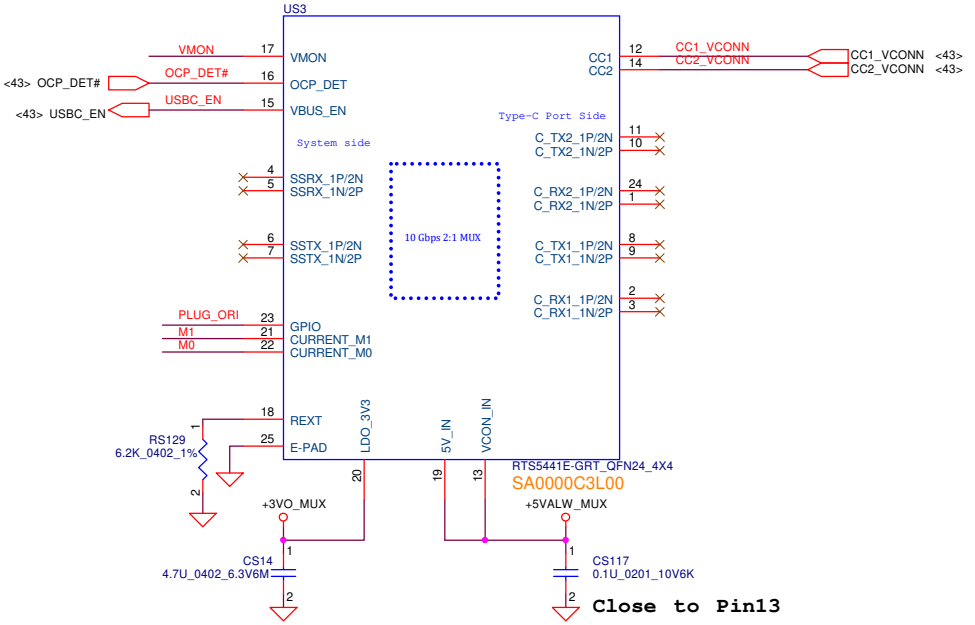
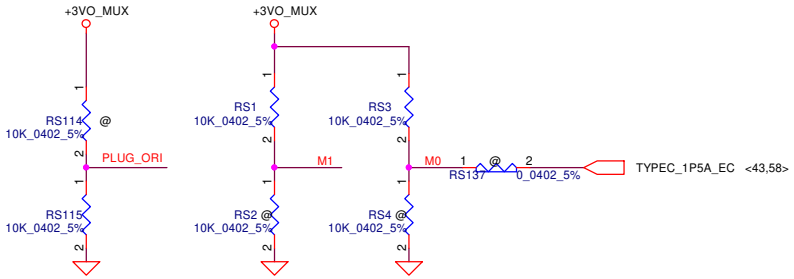
20191014
- Change to "with no Dual Role support"
- 5441E only uses the function of CC & Power SW

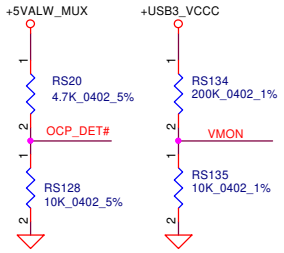


Close to Pin19



Close to Pin13





5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

confirm realtek hand-shake

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

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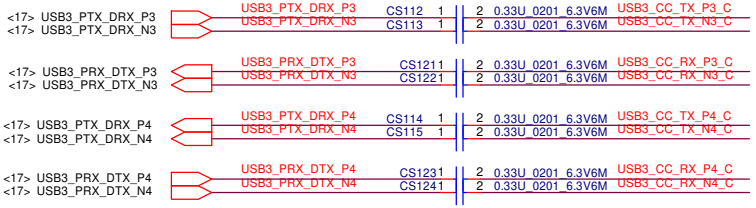
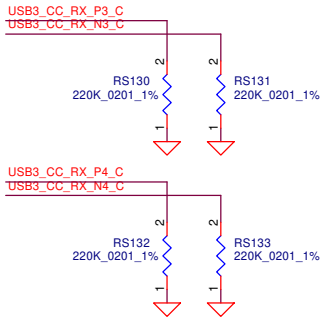
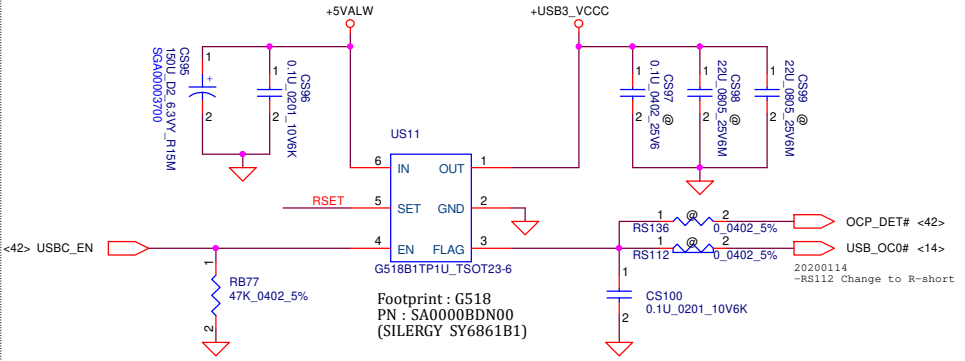


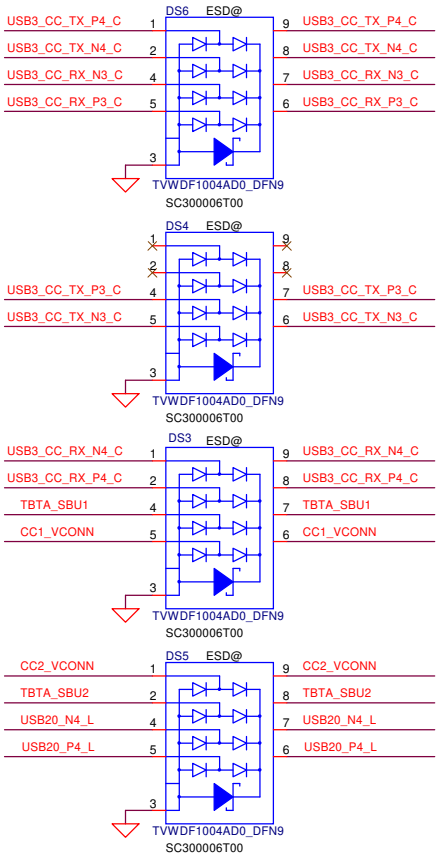


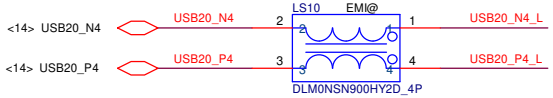
20191014
- Change to "with no Dual Role support"
- CS112/113/114/115 change to 0.33U

20191016
- USB3 Port5 change to Port3

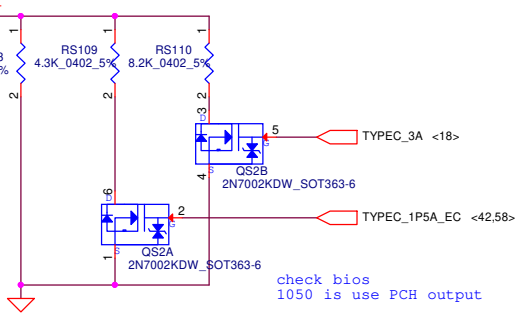


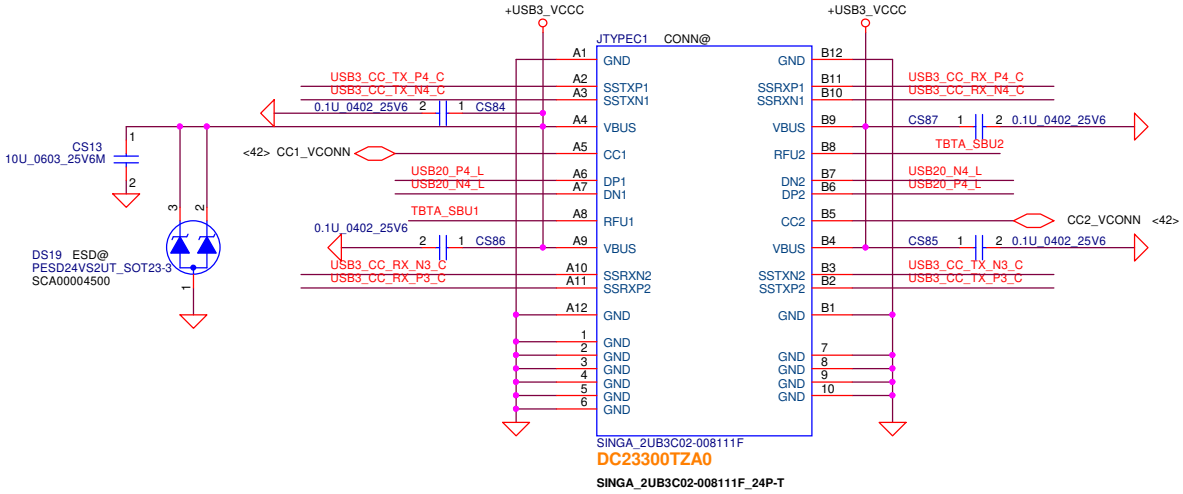
20191015 - Pin SWAP for layout
20191016 For ESD request - Gen2 Solution SC300006T00





G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A





CC1_VCONN & CC2_VCONN need 20miil trace width.

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: CC+USB TYPE C

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *FH51M M/B LA-J871P* | Rev: 1.0

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

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20190918
LAN more to IO/B

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Compal Electronics, Inc.		
Title: LAN Killer-E2600		
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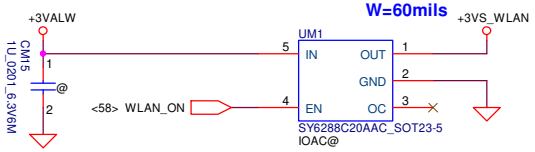
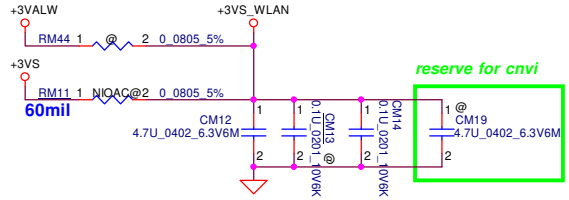
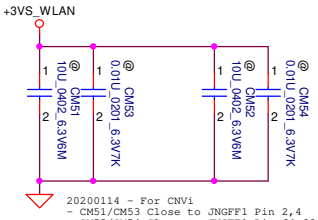
Wireless LAN



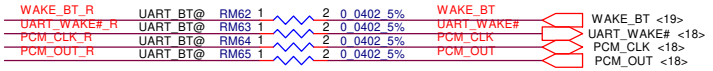




20191210C [FH51M CNVi review]
> RM69 change to 71.5k & CNVI@
> RM70 set CNVI@
> RH22 change to 20K
> RM36/RM37/RM67/RM68 change to 22 ohm
> RM16 recommend to 4.7K (no action)
> RM199 recommend to pop (no action)
> RM45 recommend to10K (no action)
> WL_OFF# recommend to PU 10K (no action)

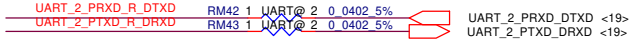
20191205 [FH5VF CNVi review]
Pin10 - RM41 Close to PCH
Pin14 - CLKREQ_CNV# PD RM69(71.5K) (Reserve)
Pin20 - UART_WAKE PU RM70(4.7K) (Reserve)
Pin22 - RM36@M.2 / RH181@PCH
Pin32 - RM37@PCH / RH22@M.2
Pin34 - RM67@M.2 / RH182@PCH
Pin36 - RM68@PCH / RH15@M.2

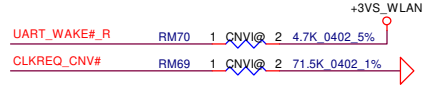
UART BT



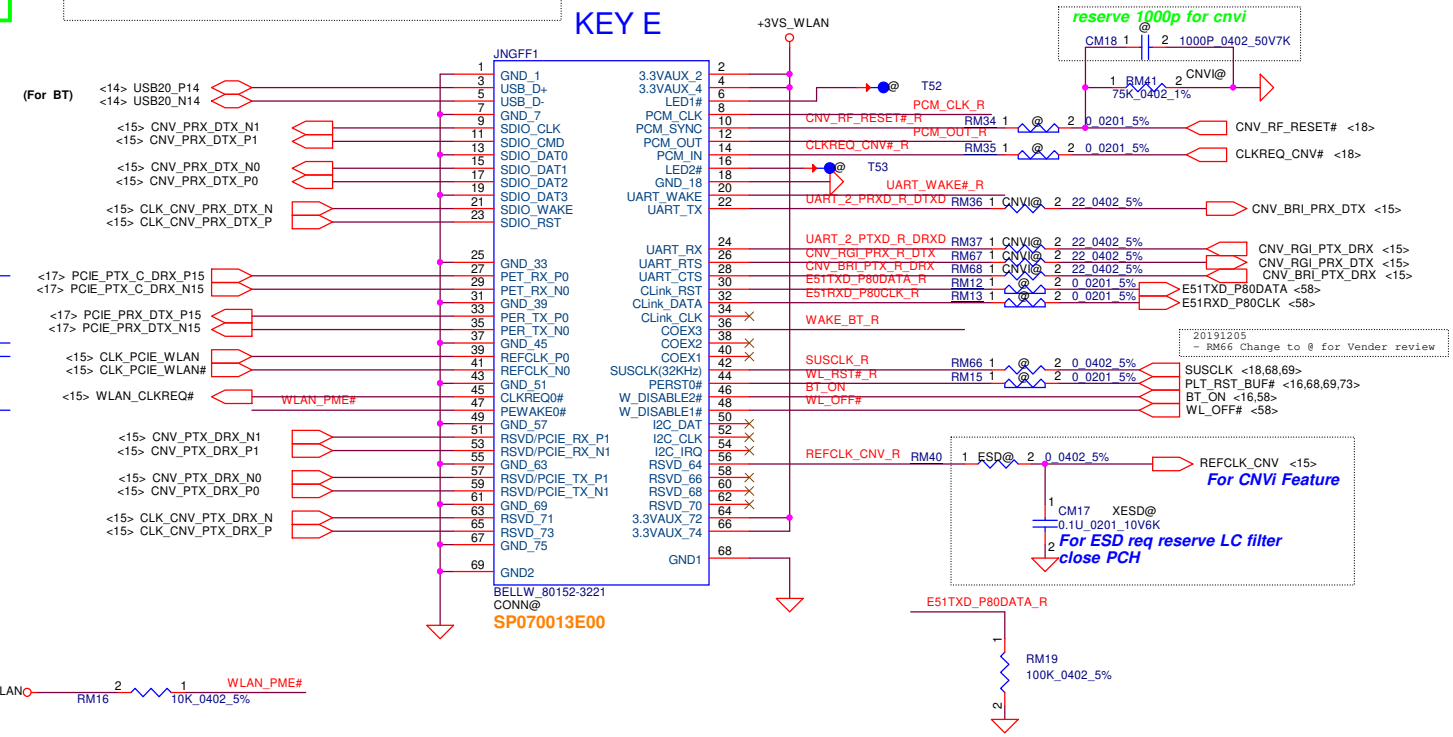
20191007
- Add RM62/63/64/65

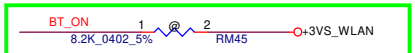
Co-layout with CNVi for SW debug





KEY E





NGFF WL+BT (KEY E)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *M.2 Key E (WLAN)*

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Compal Electronics, Inc.

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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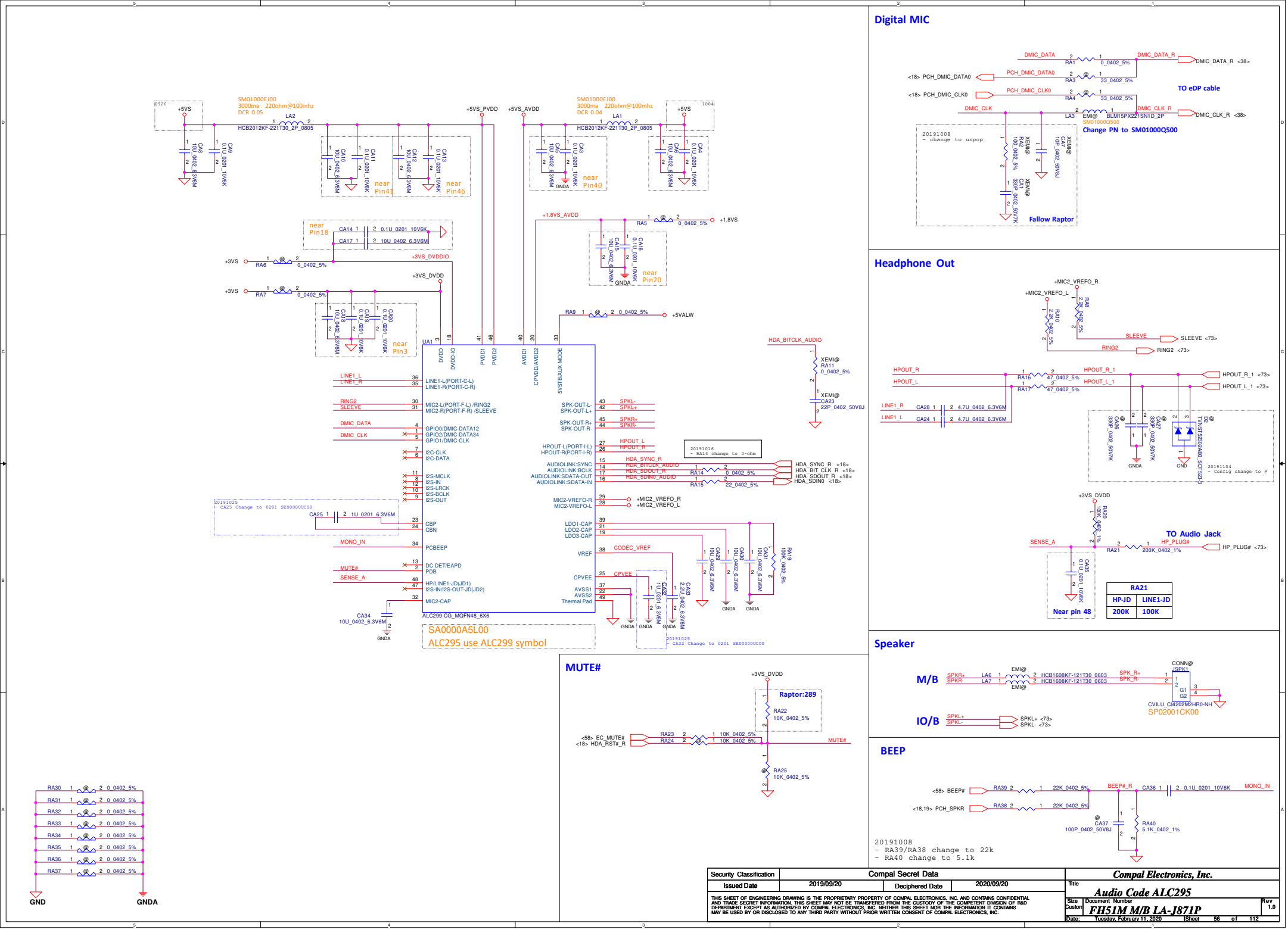

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.	
Title	Audio Code ALC295
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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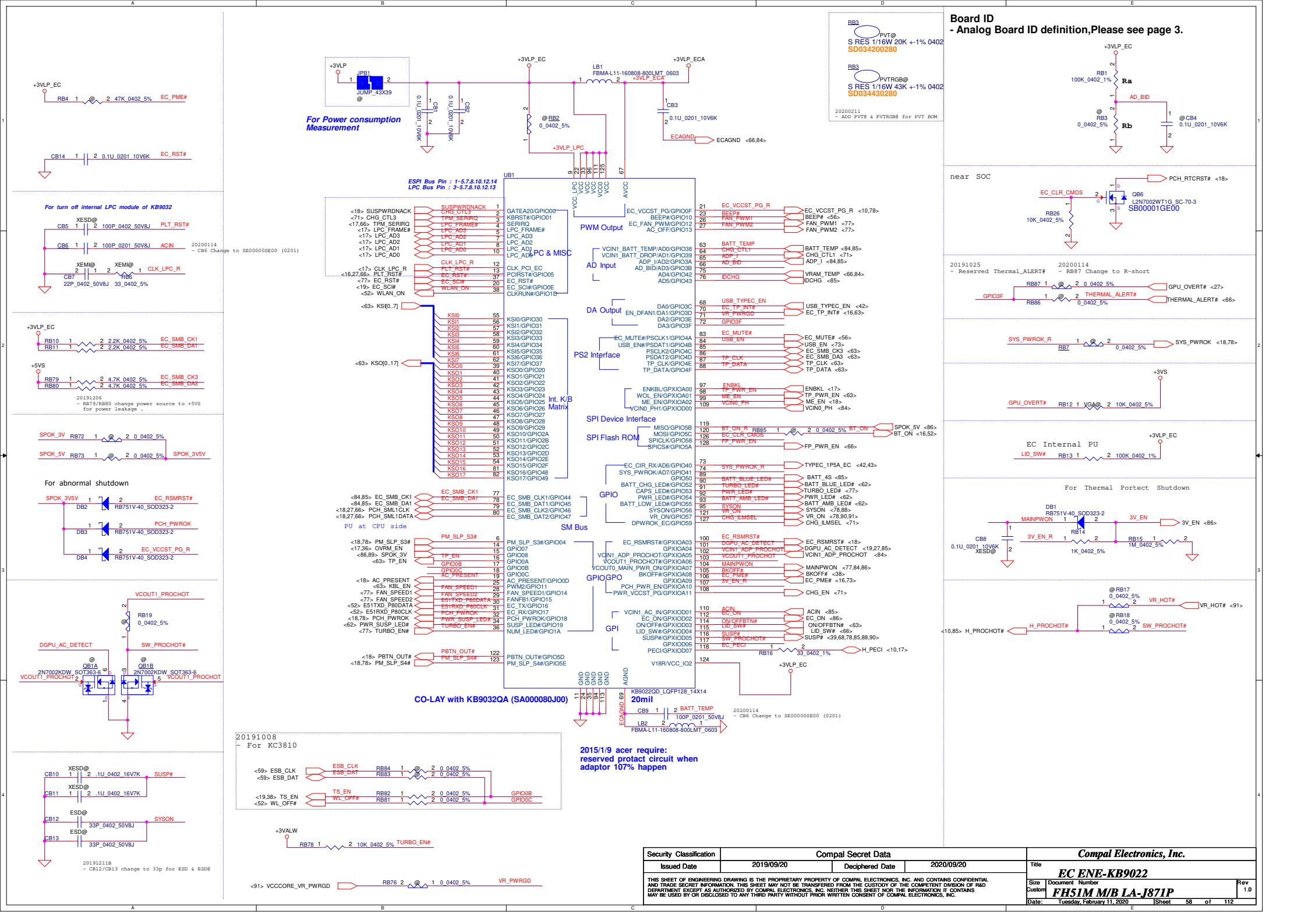
Board ID
- Analog Board ID definition,Please see page 3.
For Power consumption Measurement
ESPI Bus Pin : 1-5.7.8.10.12.14
LPC Bus Pin : 3-5.7.8.10.12.13
For turn off internal LPC module of KB9032
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPIO
GPO
GPI
near SOC
EC Internal PU
For Thermal Portect Shutdown
For abnormal shutdown
PU at CPU side
CO-LAY with KB9032QA (SA000080J00)
20mil
2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen
For KC3810
Security Classification
Compal Secret Data
Issued Date
2019/09/20
Deciphered Date
2020/09/20
Compal Electronics, Inc.
EC ENE-KB9022
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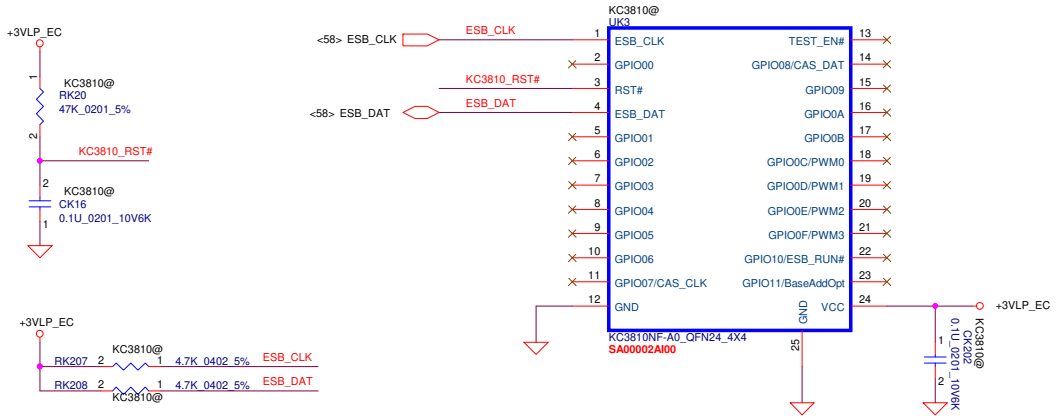
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.

OMEN New ESB CLK&DAT for Extend I/O



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: N18E-GDDR6_D

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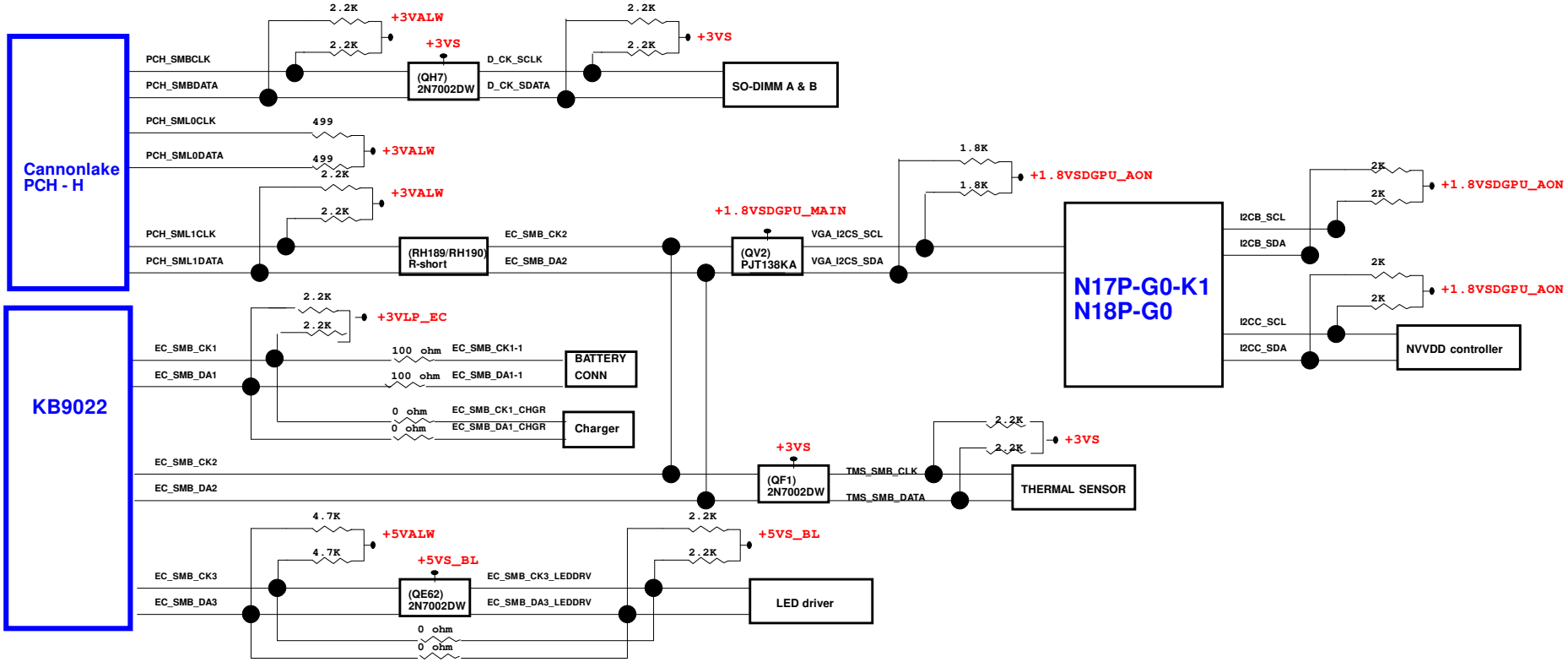

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Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: N17E-GDDR5_D

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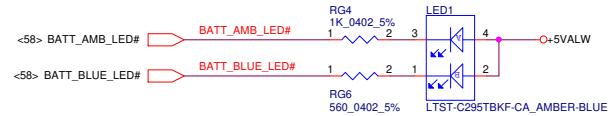
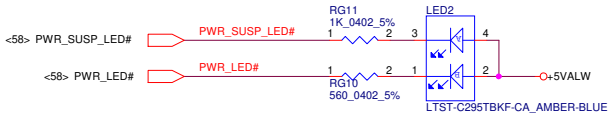
Battery LED



Power LED




```
20200211
- RG4/RG11 change to 1k
```

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Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: **LED**

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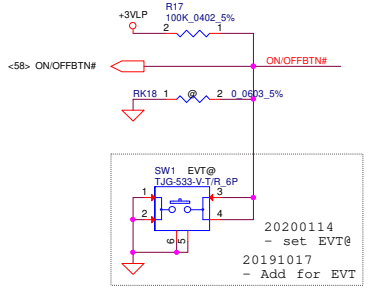
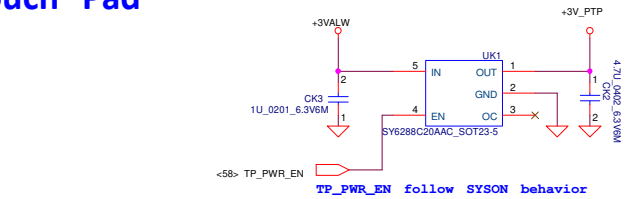
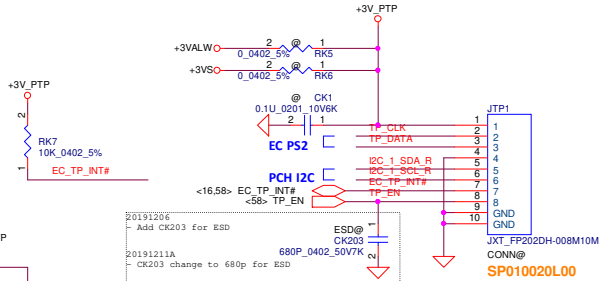
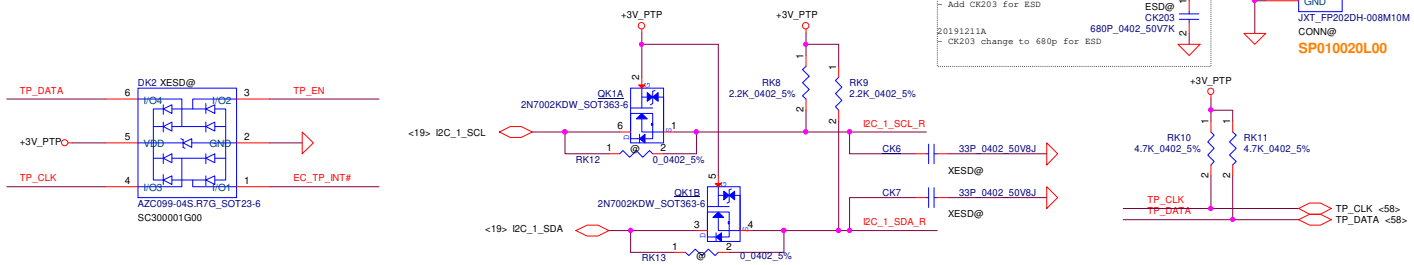
ON/OFF BTN
- For TEST



Touch Pad





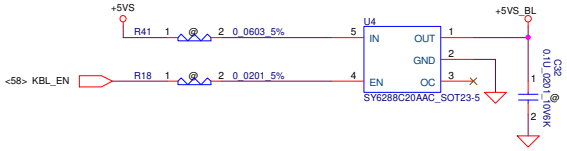


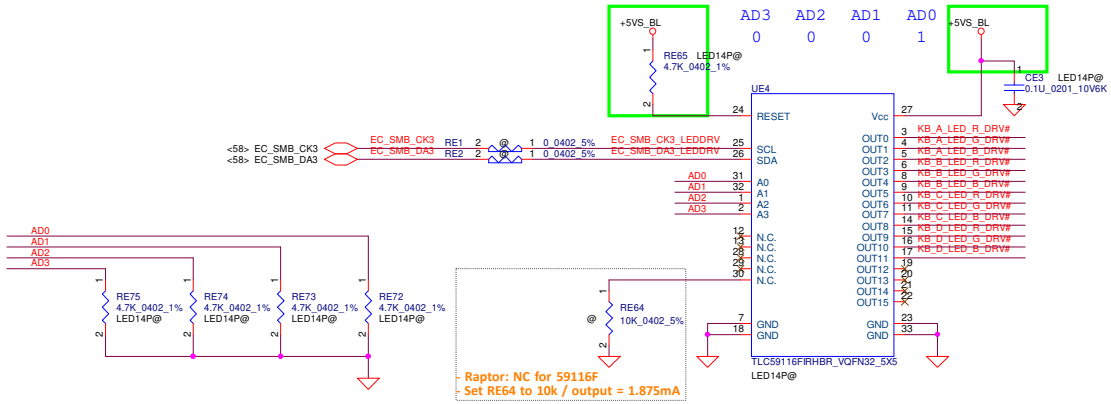
LED driver

20191016
- Remove QE62/RE70/RE69
- PU +5VALW @ EC

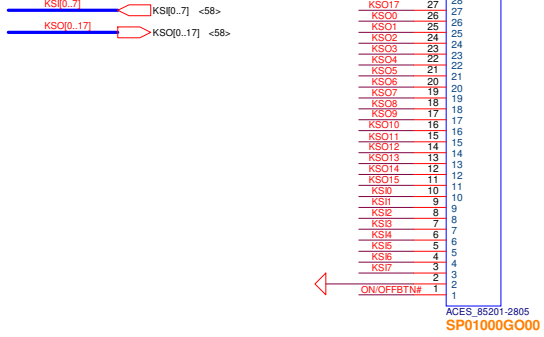
20191001
- Change to +5VS only
- KBL_EN only (Check EC Code)
- pop (Normal & RGB)

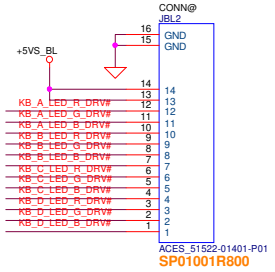
20200115
- R41/R18 change to R-short

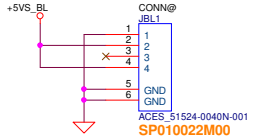




KB Conn. / Backlight







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Issued Date	2019/09/20	Deciphered Date 2020/09/20

Compal Electronics, Inc.

Title: KB & TP & TPM Connector

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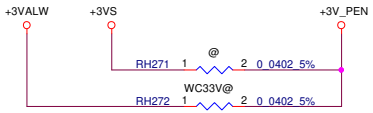
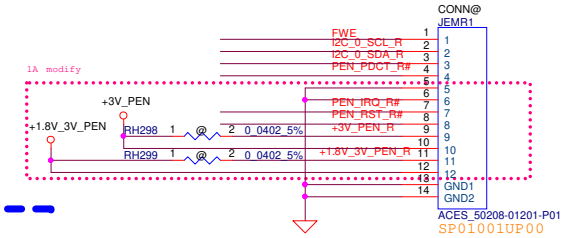
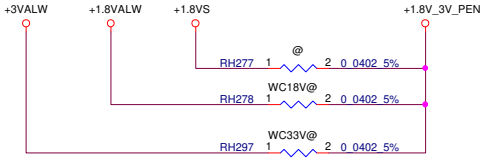
3V_PEN



EMR

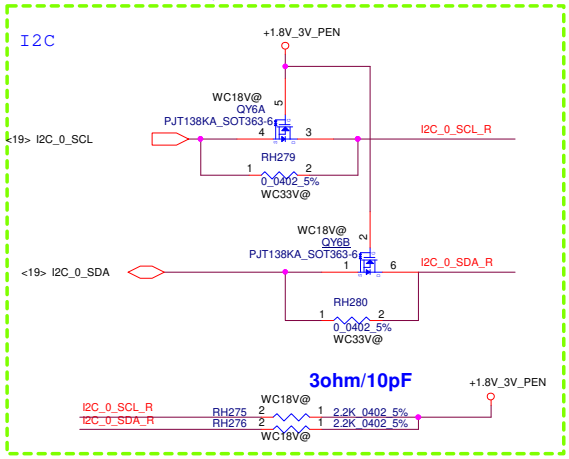


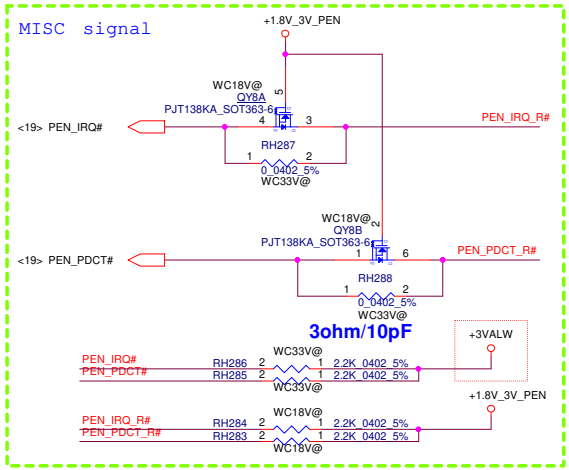
1.8V_PEN

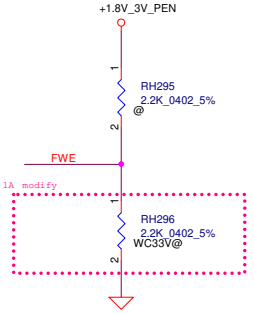


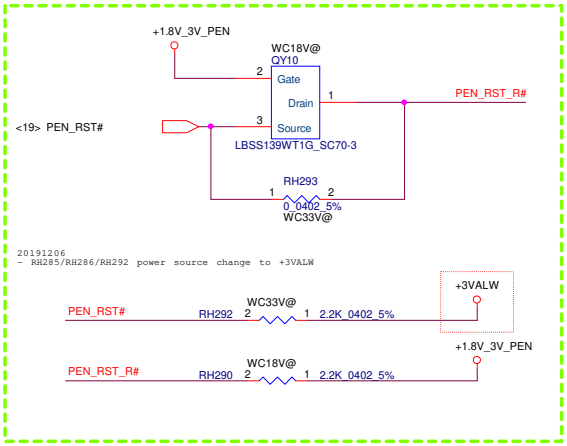
20191008
- QY6/QY8 change to SB000016K00

Default use 0ohm(WC33V@)









Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: N18E-GDDR6_D

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Compal Electronics, Inc.

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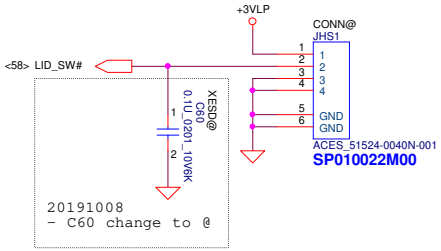
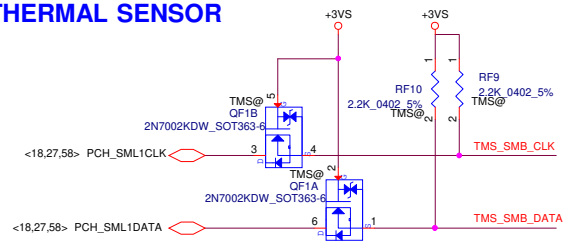
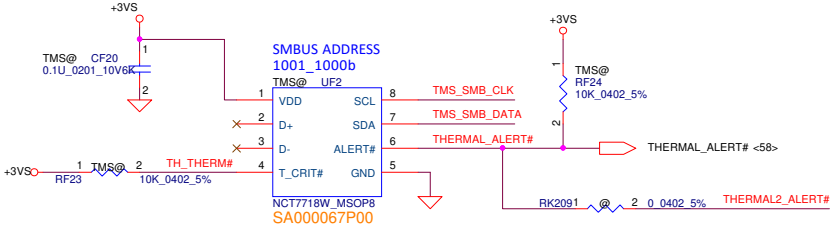
To Hall sensor/B



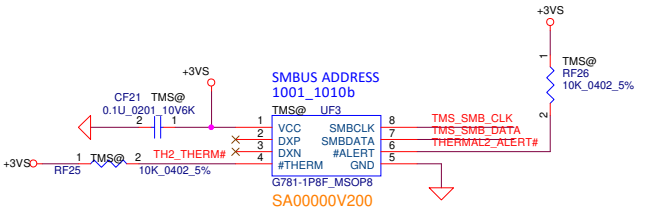
THERMAL SENSOR



Close to SO-DIMM

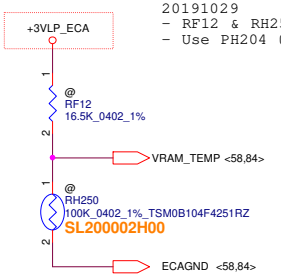


Close to Thermal SKIN

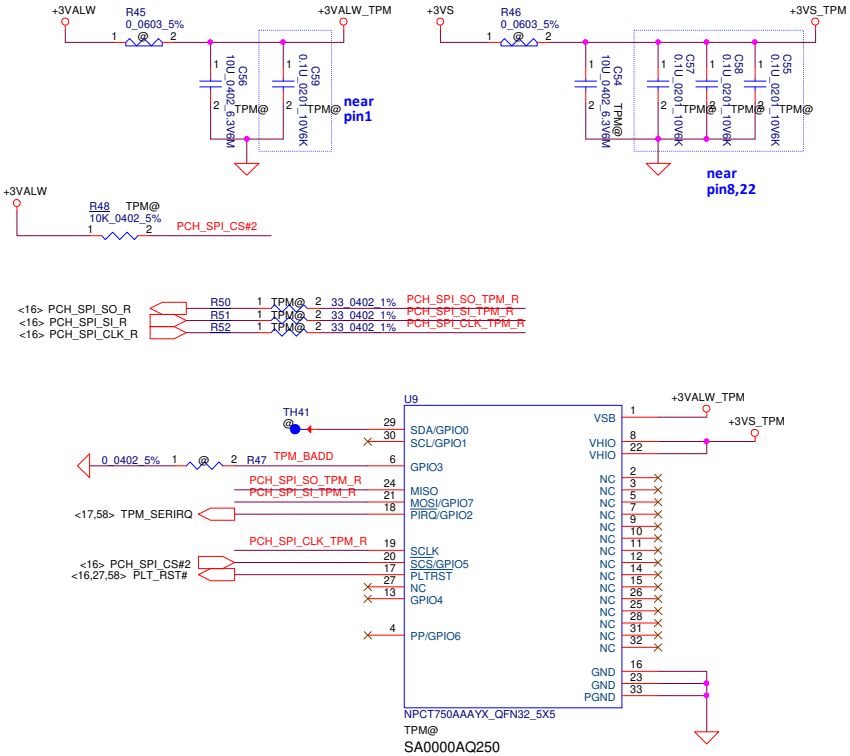


Close to VRAM choke

20191029
- RF12 & RH250 change to unpop
- Use PH204 @ Power

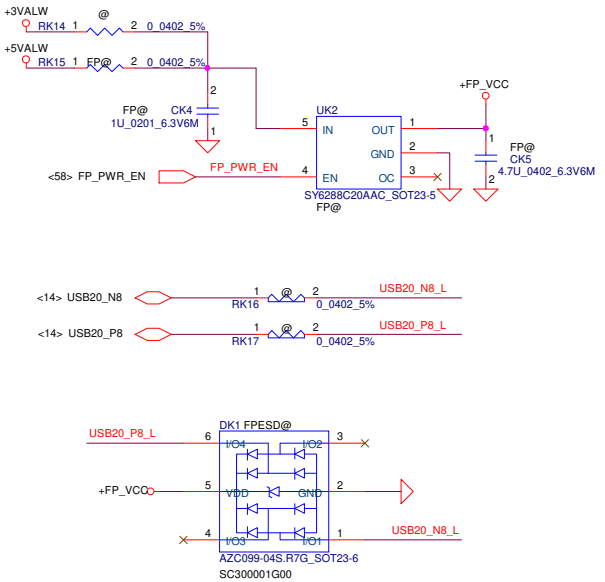


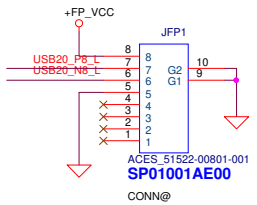
TPM



SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

Finger Print





PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: Sensors/FP/TPM

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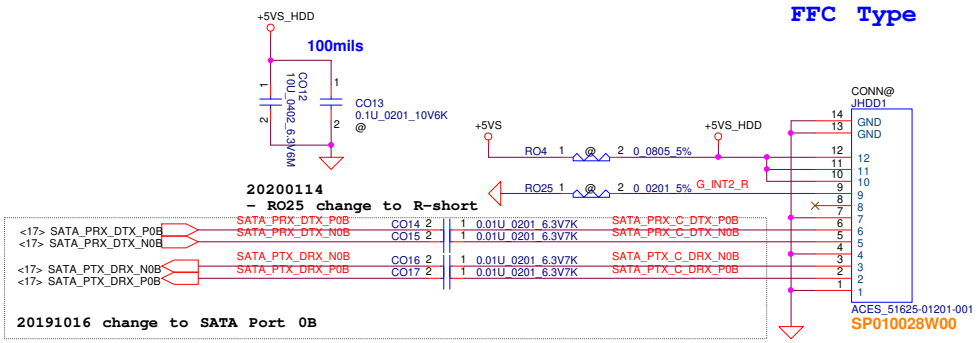

20190918
Remove HDD Re-driver

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.		
Title: HDD/ Re-Driver/ G-sensor		
Size: Custom	Document Number: FH51M M/B LA-J871P	Rev: 1.0
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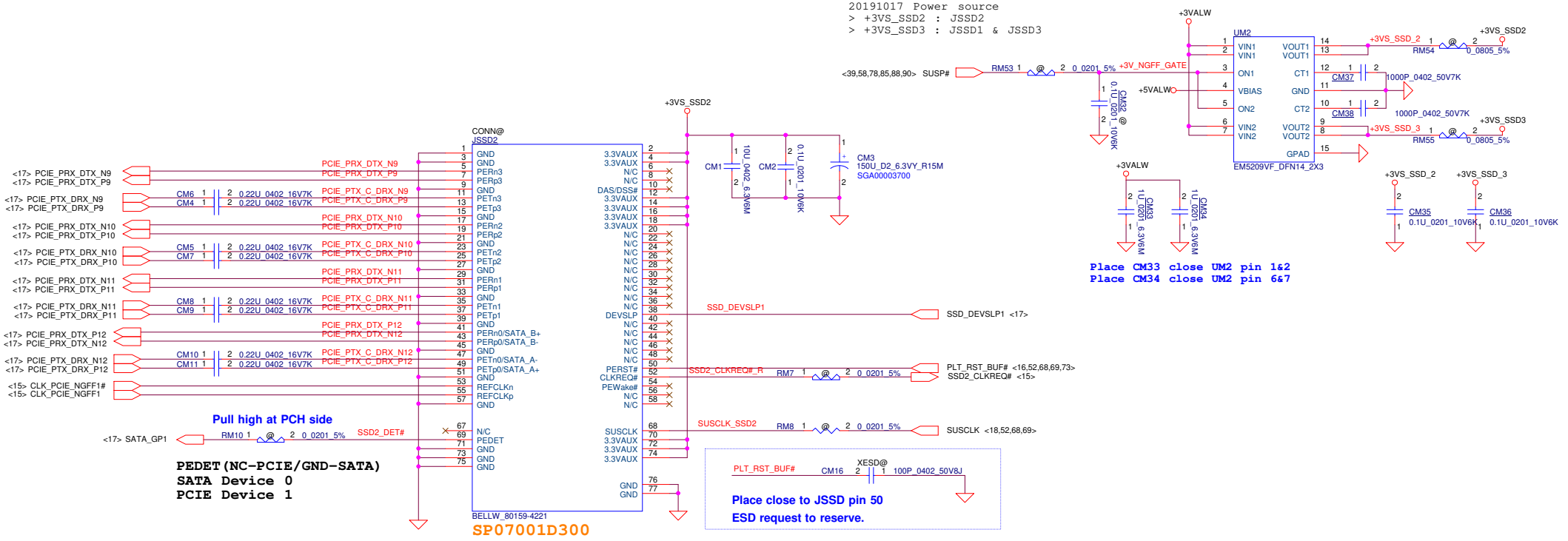
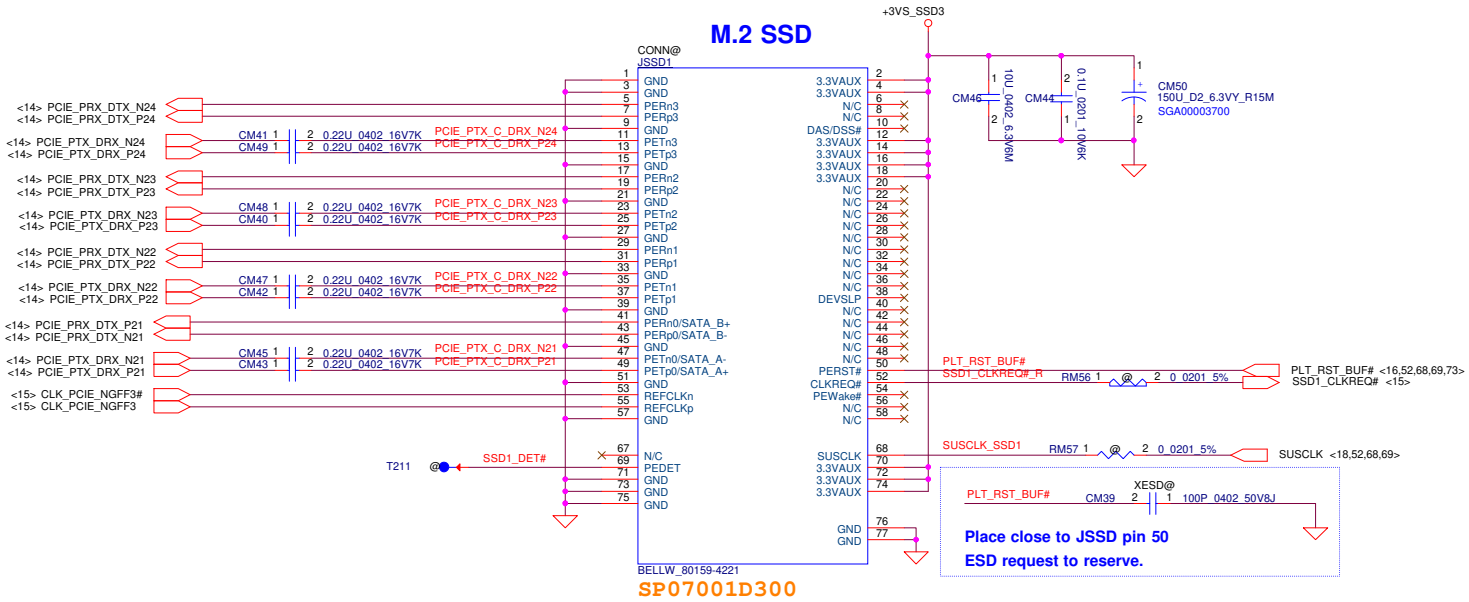
20191017 Power source
> +3VS_SSD2 : JSSD2
> +3VS_SSD3 : JSSD1 & JSSD3



M.2 SSD



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: SATA/PCIE-SSD

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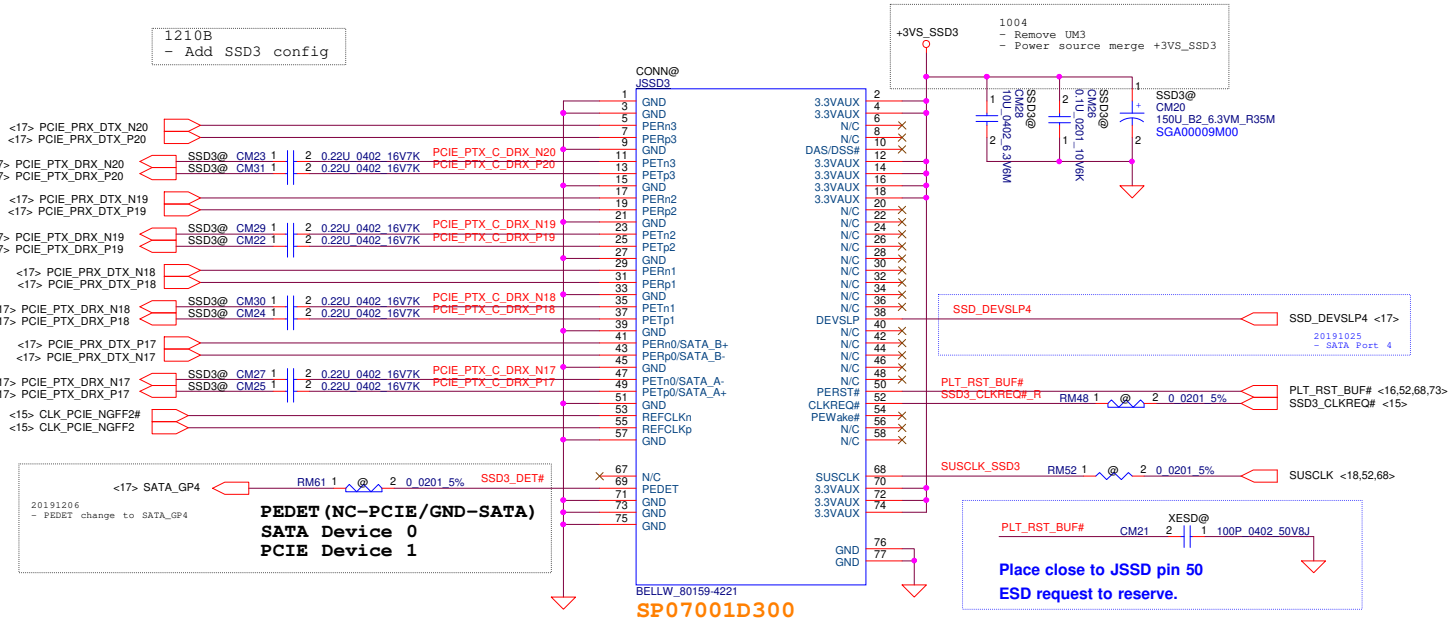

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.		
Title	N18E-GDDR6_D	
Size	Document Number: FH51M M/B LA-J871P	Rev 1.0
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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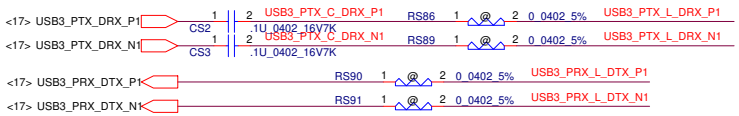
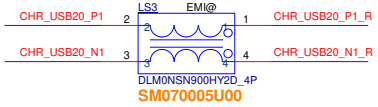
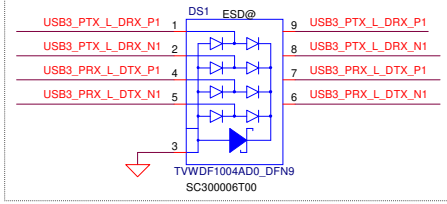
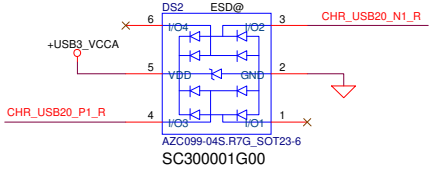
USB3.0

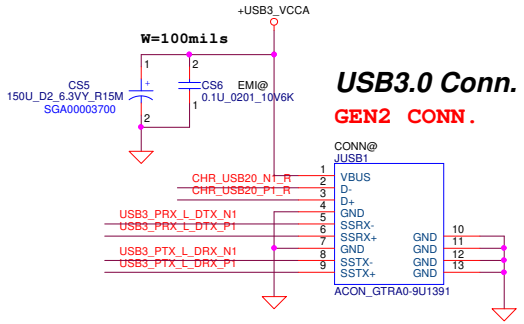




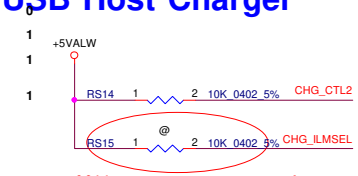
20191016 For ESD request
- Gen2 Solution SC300006T00



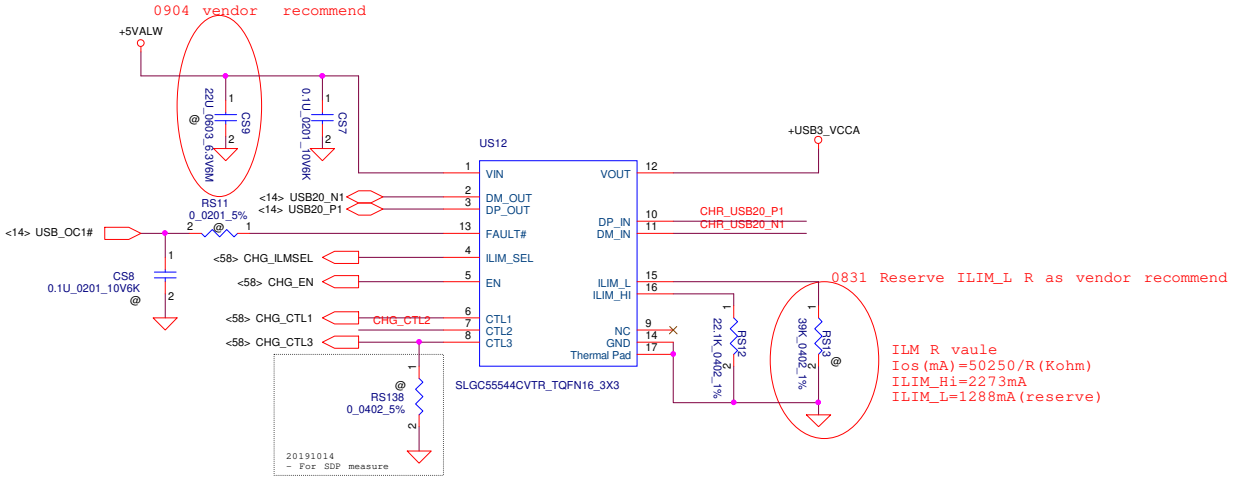




USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: USB3.0 Conn/USB Charger

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20190918
USB3 Port3 move to IO/B

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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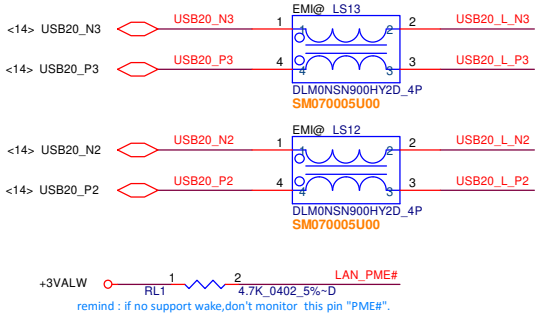
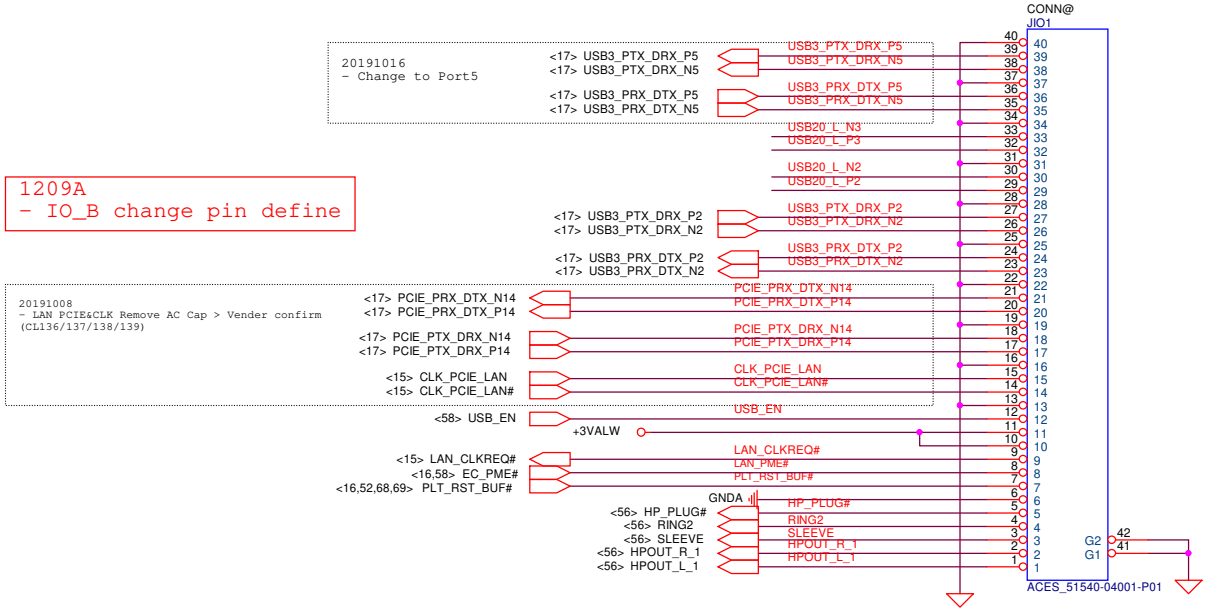
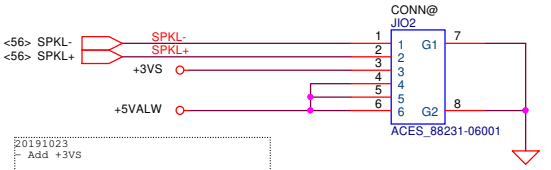
IO/B CONN



1209A
- IO_B change pin define





Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: IO/B_LAN E2600

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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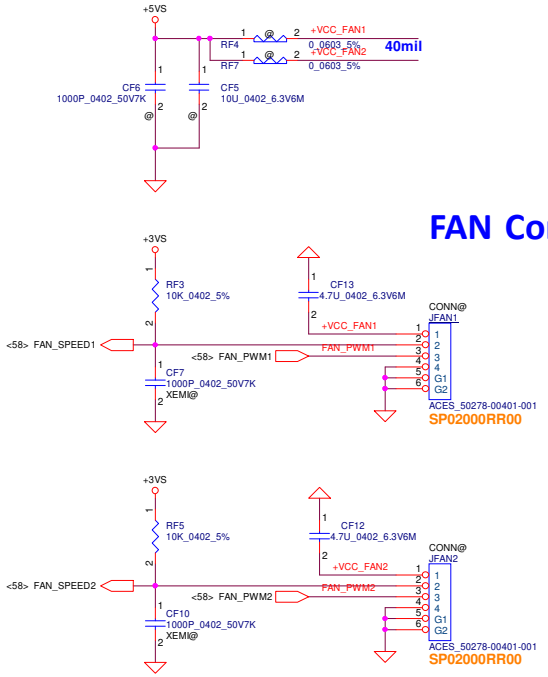
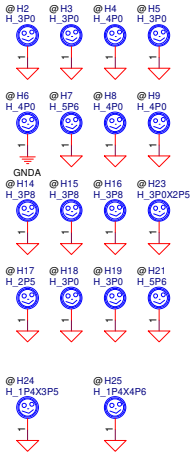
FAN Conn

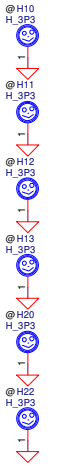


Screw Hole

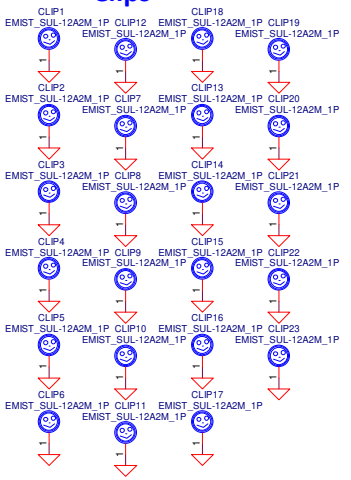
20191210B
- H6 change to GNDA for Layout

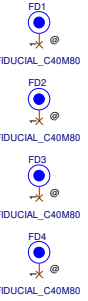


Stand OFF

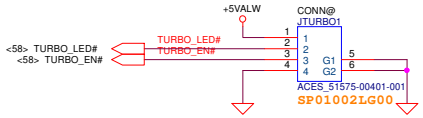


Clips



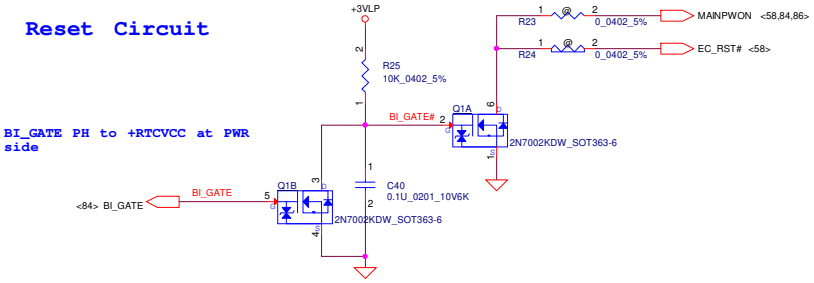


Turbo Key

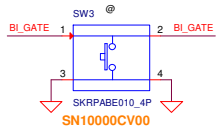


Reset Circuit

BI_GATE PH to +RTCVCC at PWR side



Reset Button



SN10000CV00

change PN to SN10000CV00

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: FAN & Screw Hole

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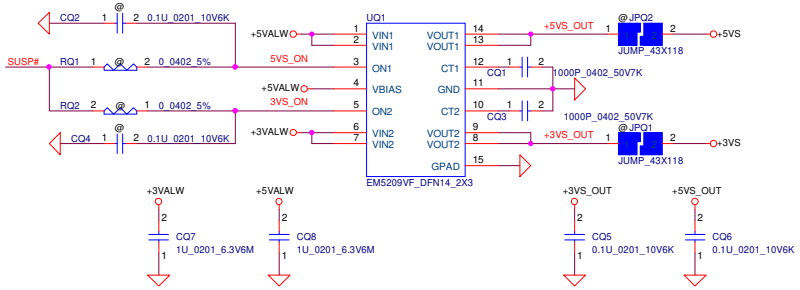
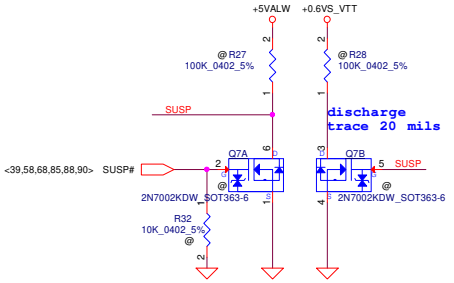
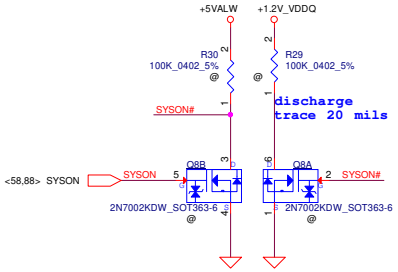
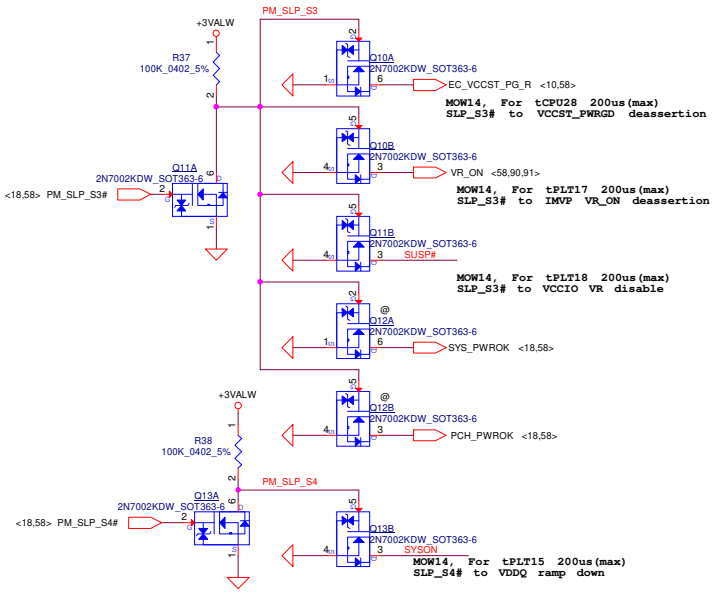
System DC inferface





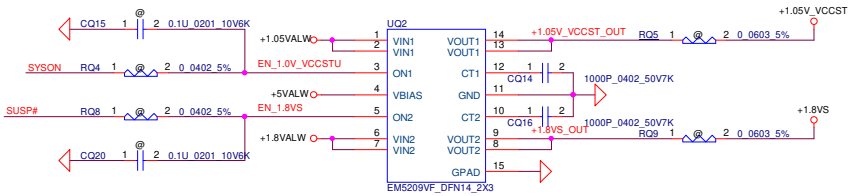


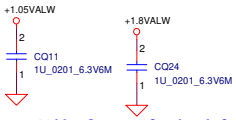
For Power ON/Off Sequence

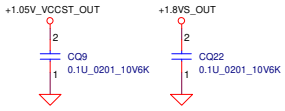


P/N: SB00000EO00 footprint use SB00000ZU00

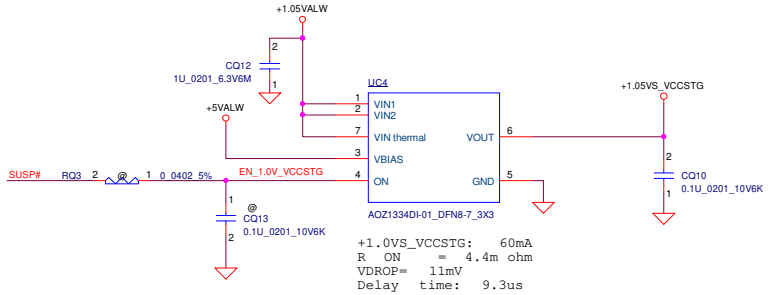
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS







+1.05VALW TO +1.05VS_VCCSTG



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: FH51M M/B LA-J871P		Rev: 1.0
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Compal Electronics, Inc.		
Title: *Reserve*		
Size	Document Number: *FXXXX M/B LA-J871P*	Rev: 1.0
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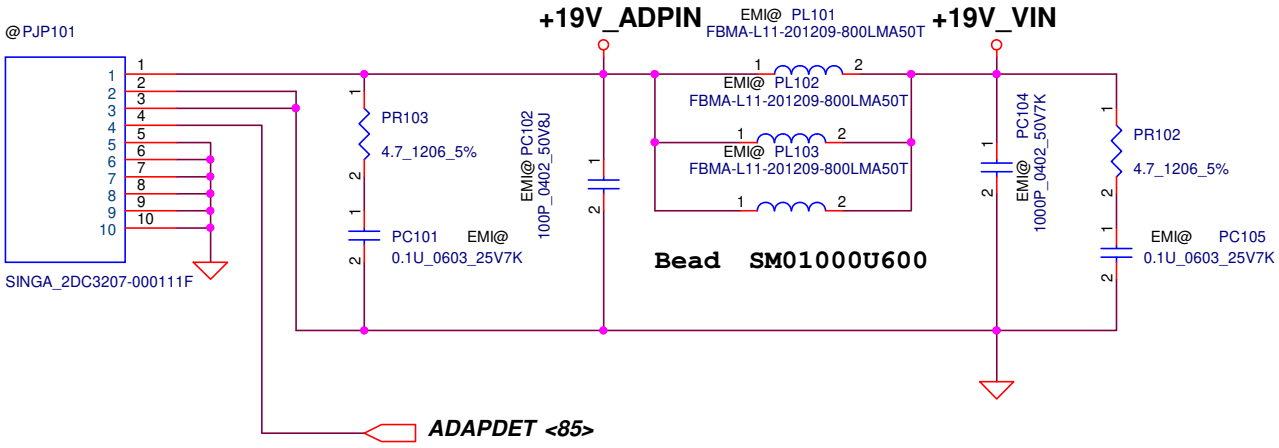

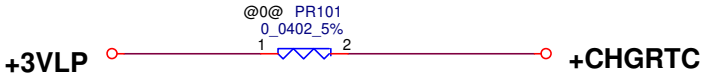

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: DCIN

Size: Custom | Document Number: FXXXX M/B LA-J871P | Rev: 1.0

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Compal Electronics, Inc.

Title: **Reserve**

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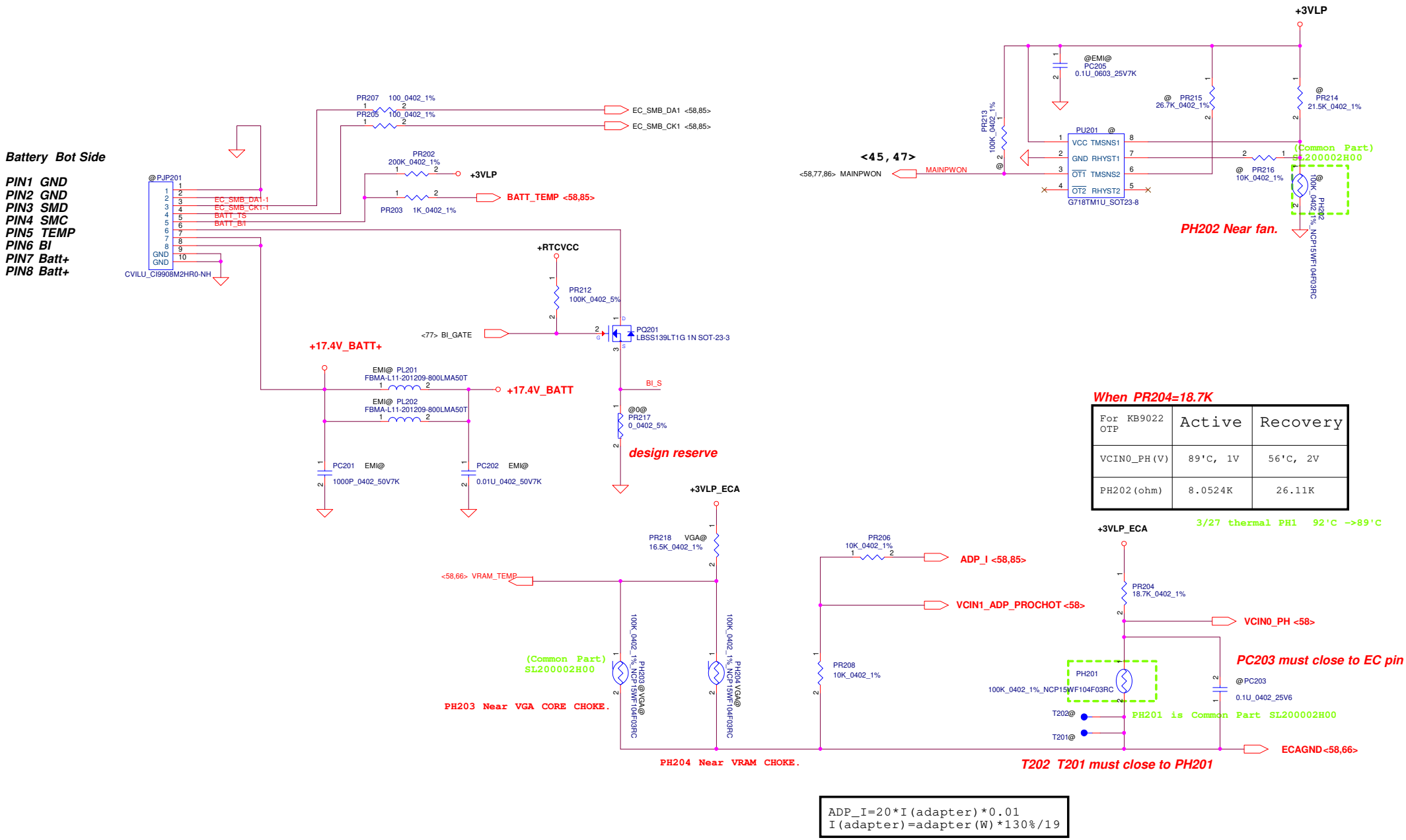

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: FXXXX M/B LA-J871P | Rev: 1.0

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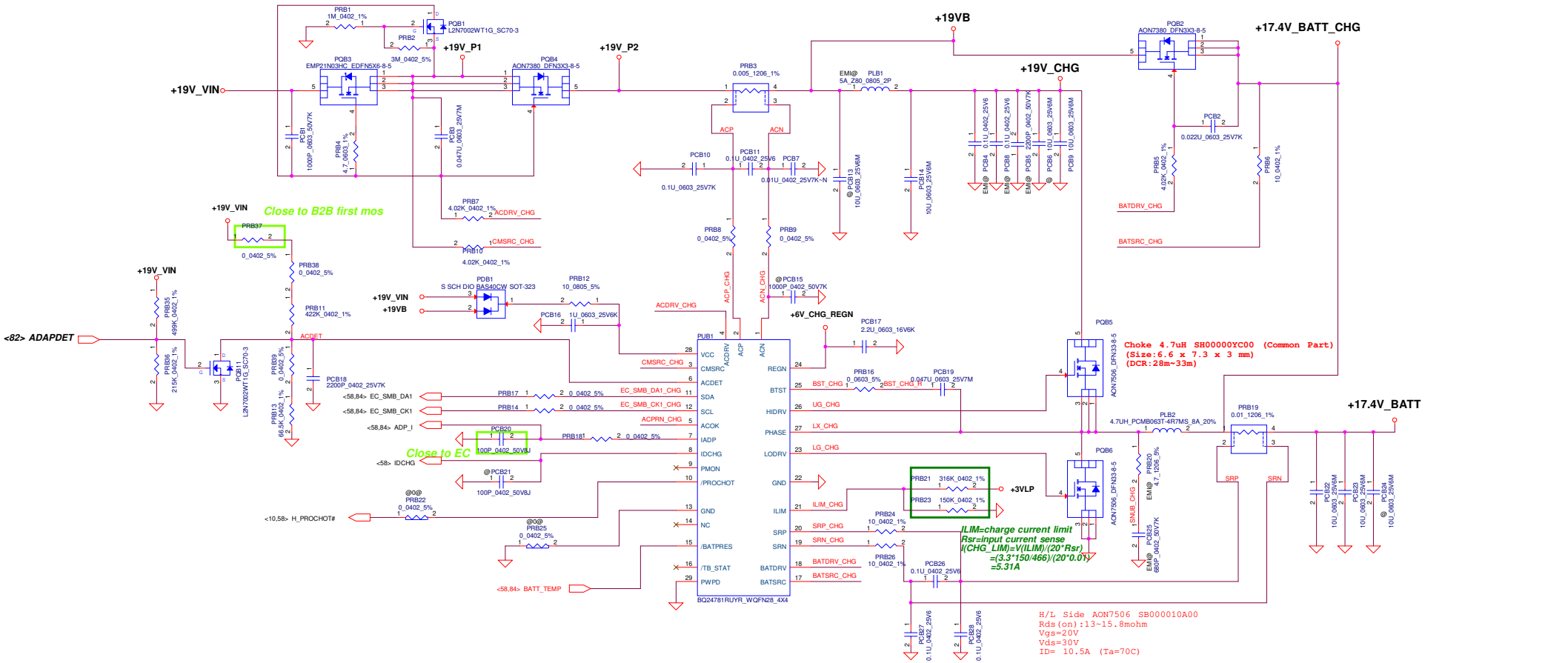

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.	
Title	PWR_CHARGER
Size	Document Number: FXXXX M/B LA-J871P
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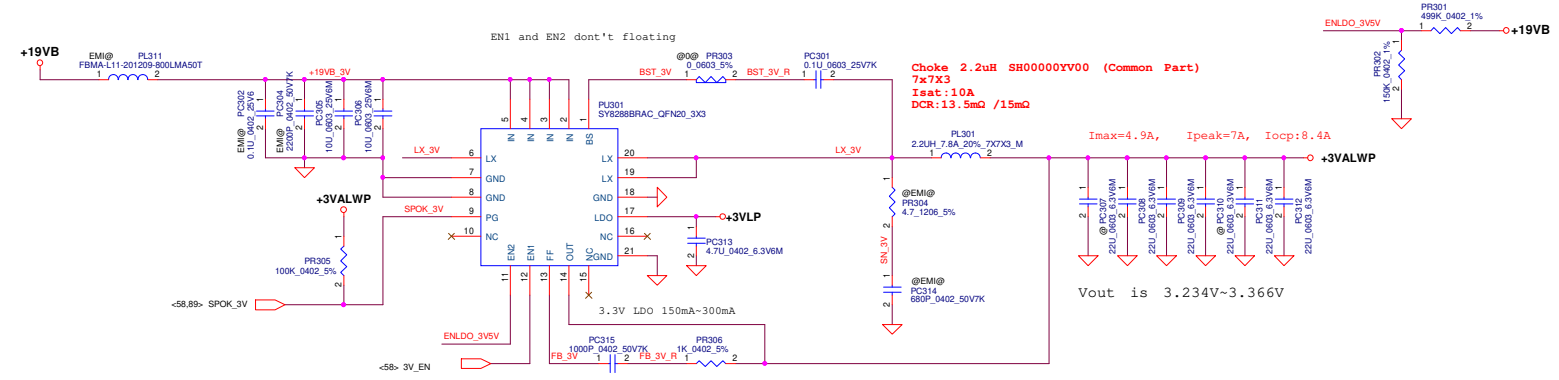

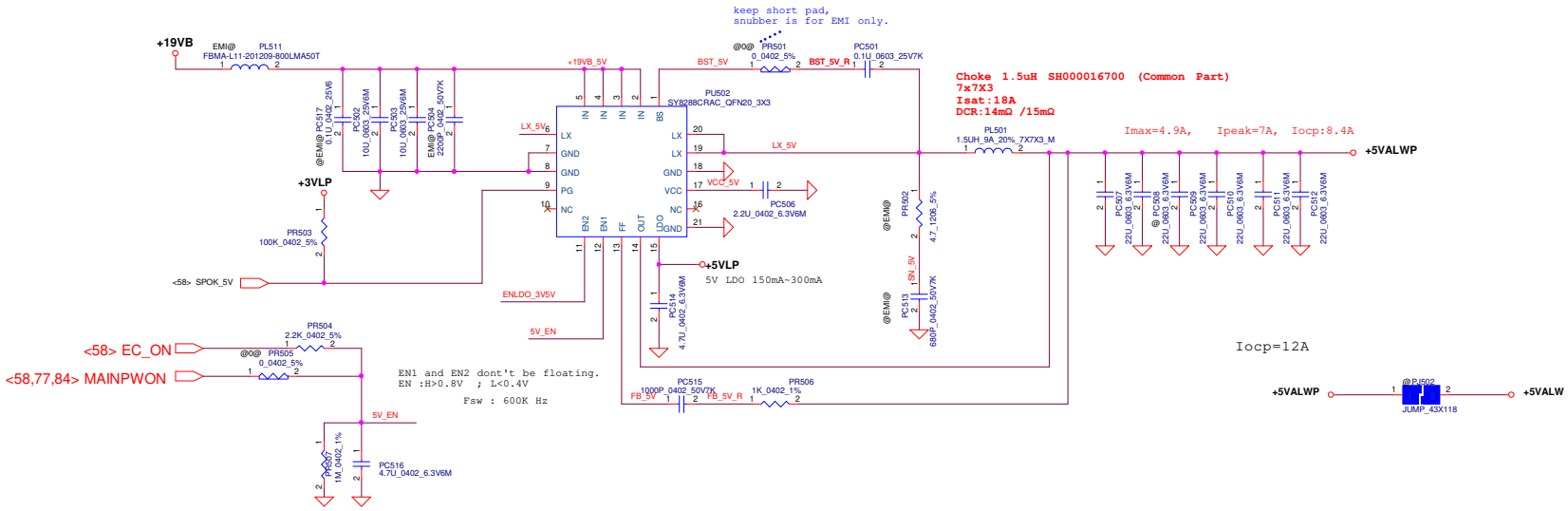

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Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: +3VALW/+5VALW

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Compal Electronics, Inc.

Title: **Reserve**

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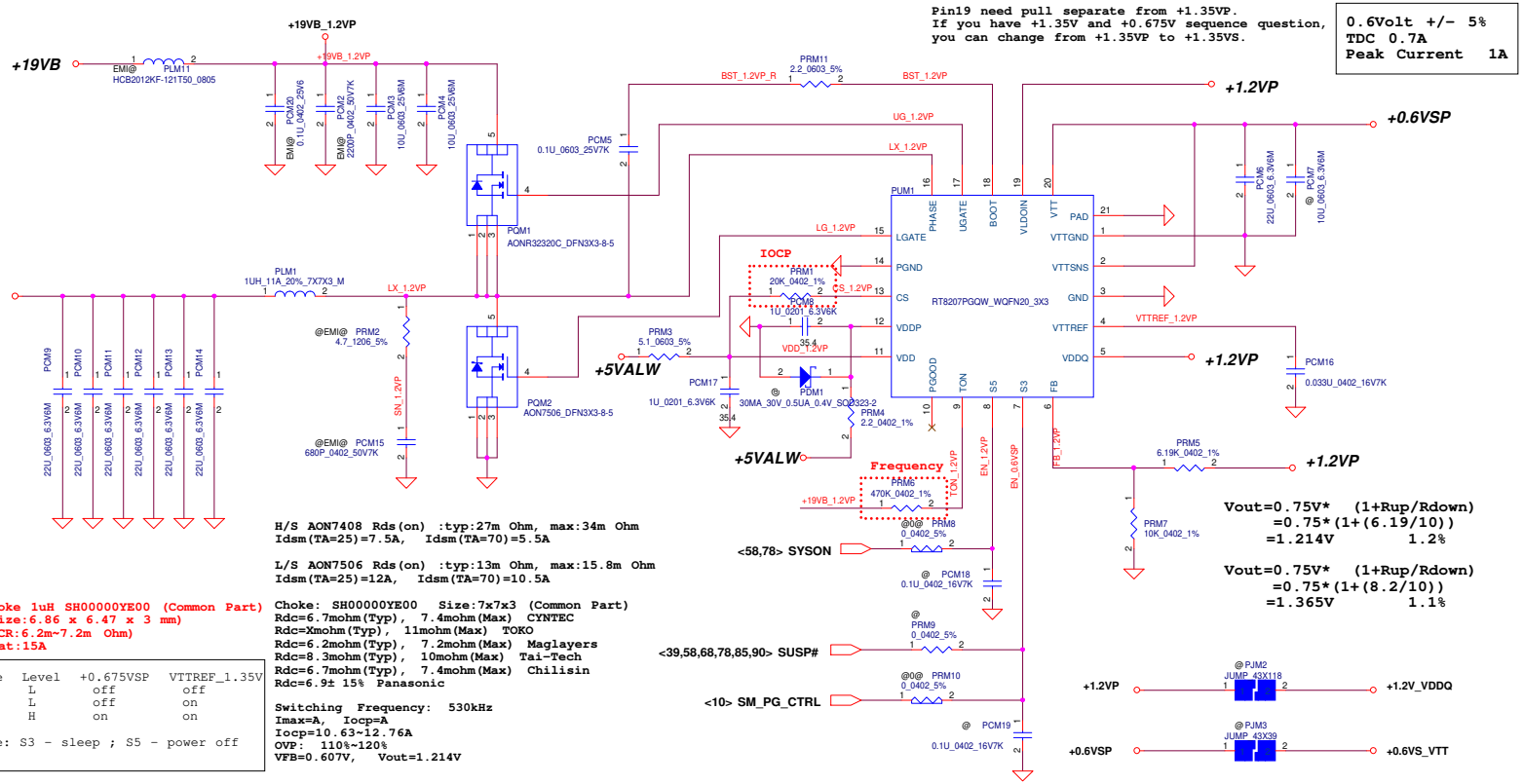
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A



Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(6.19/10))
=1.214V 1.2%

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(8.2/10))
=1.365V 1.1%

H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13m Ohm, max:15.8m Ohm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

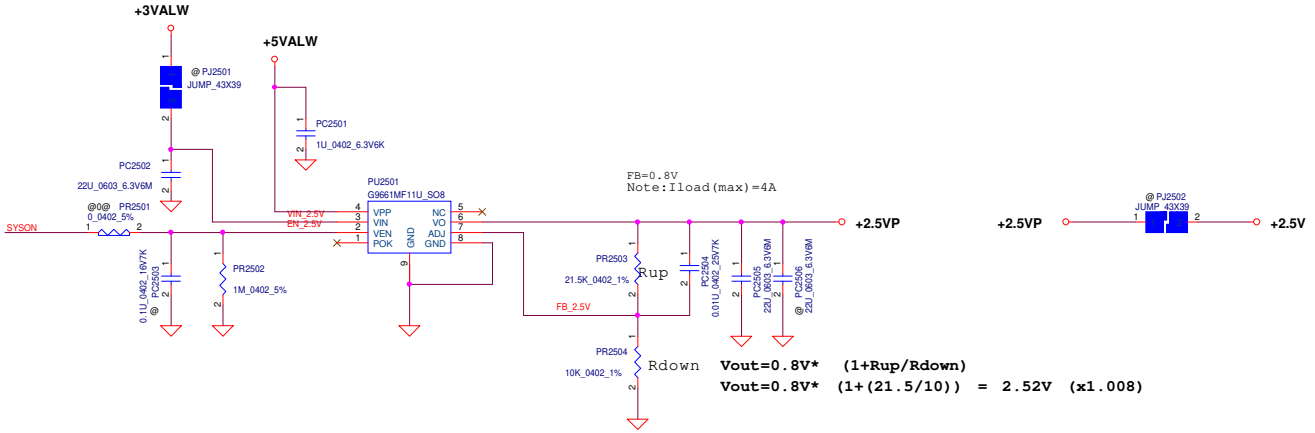
Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)
Isat:15A

Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic

Switching Frequency: 530kHz
Imax=A, Iocp=A
Iocp=10.63~12.76A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



Vout=0.8V* (1+Rup/Rdown)
Vout=0.8V* (1+(21.5/10)) = 2.52V (x1.008)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDR4

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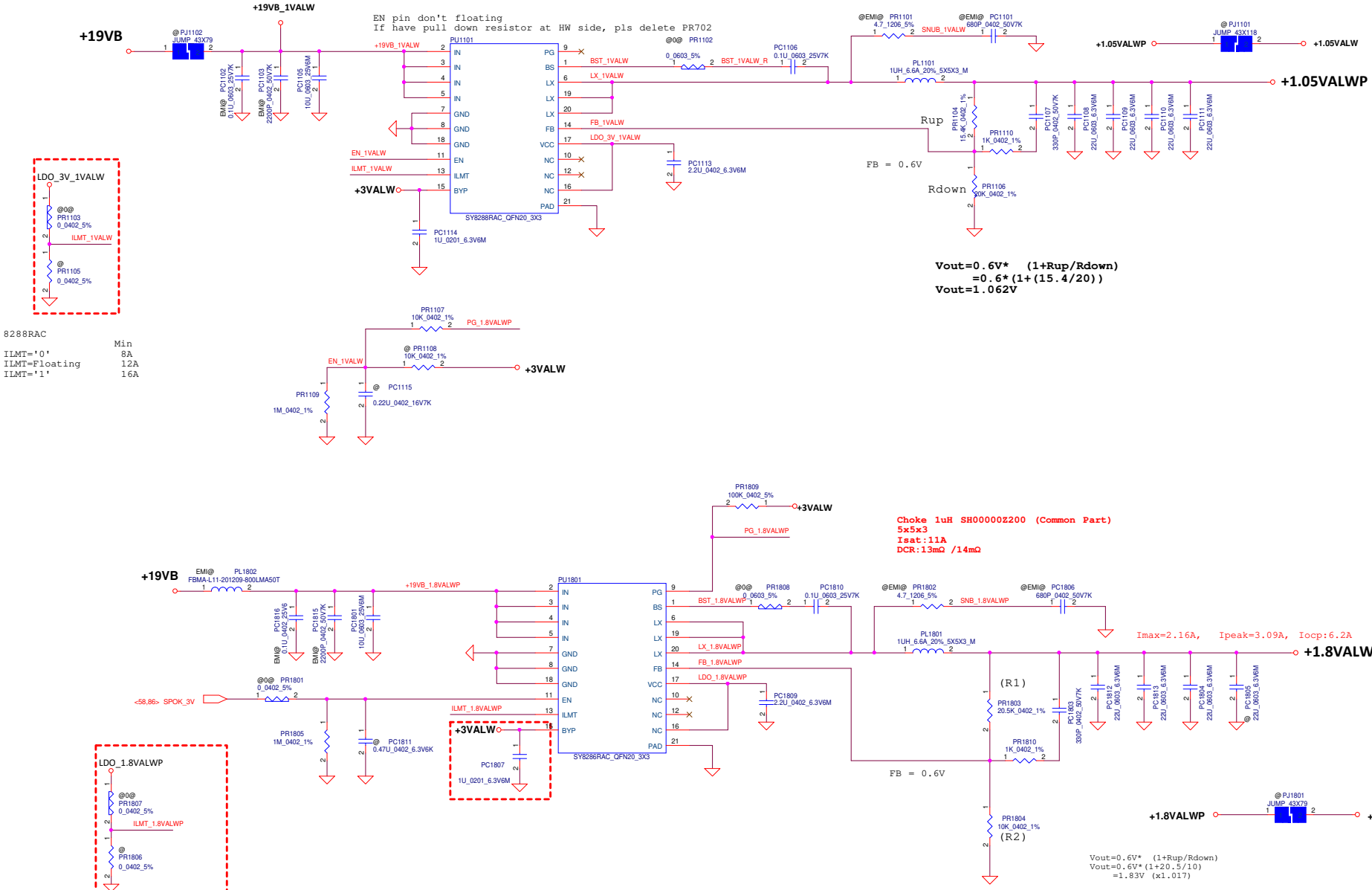
Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)
Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic



Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: 1V

Size	Document Number	Rev
C	FXXXX M/B LA-J871P	1.0

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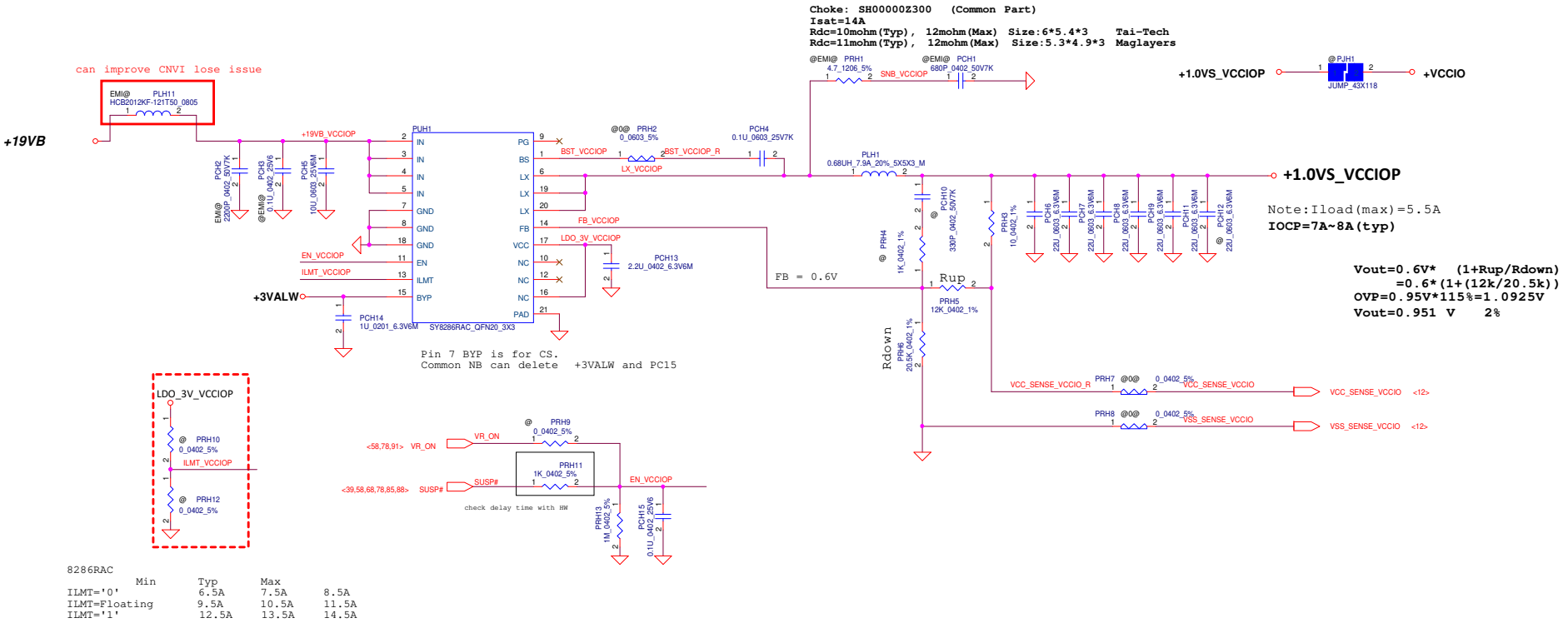

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: 1.0VS_VCCIO

Size	Document Number	Rev
C	FXXXX M/B LA-J871P	1.0

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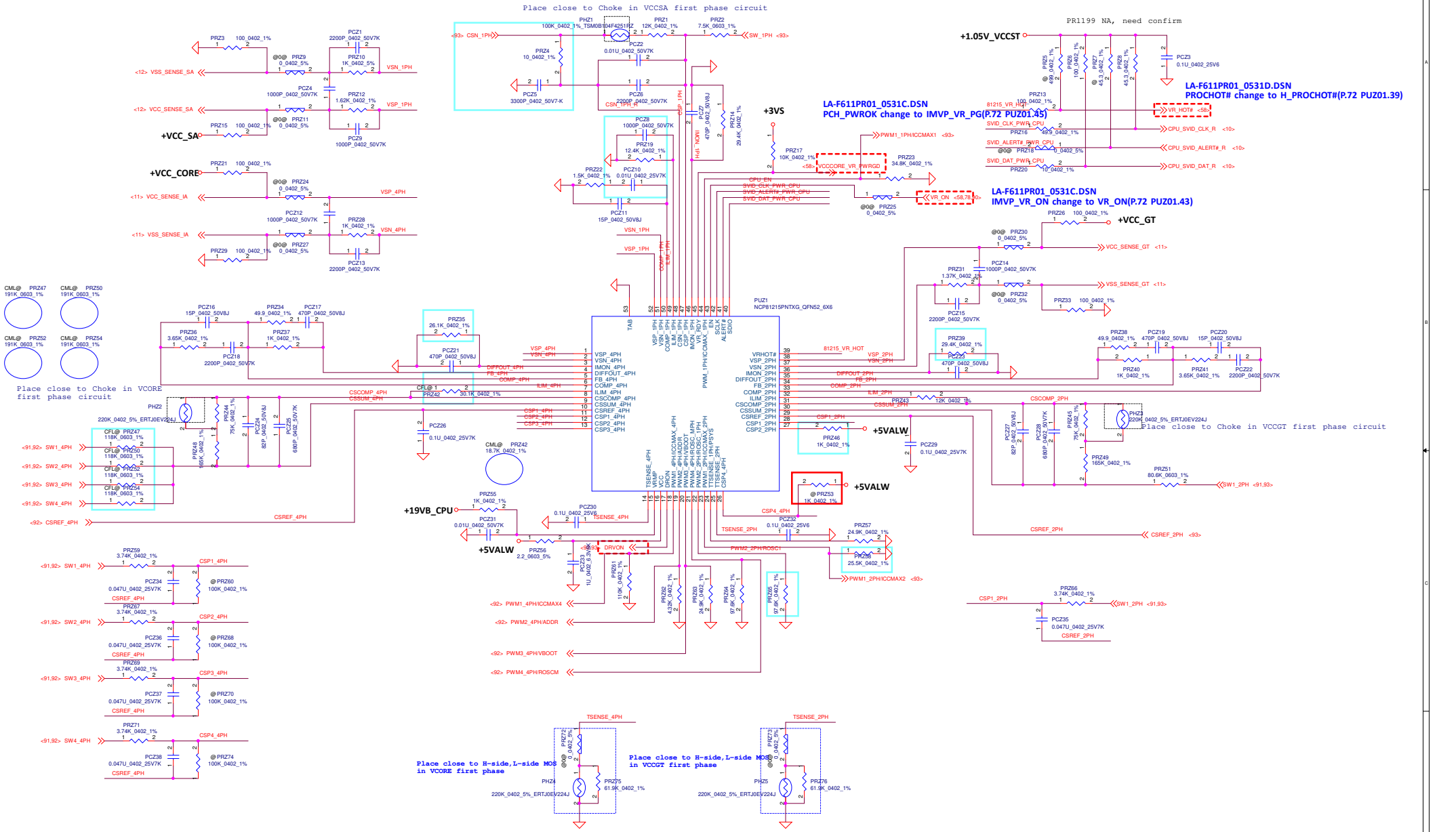

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Compal Electronics, Inc.

Title			
Size: Custom	Document Number: CPU IC CFL_H 42		Rev: 1.0
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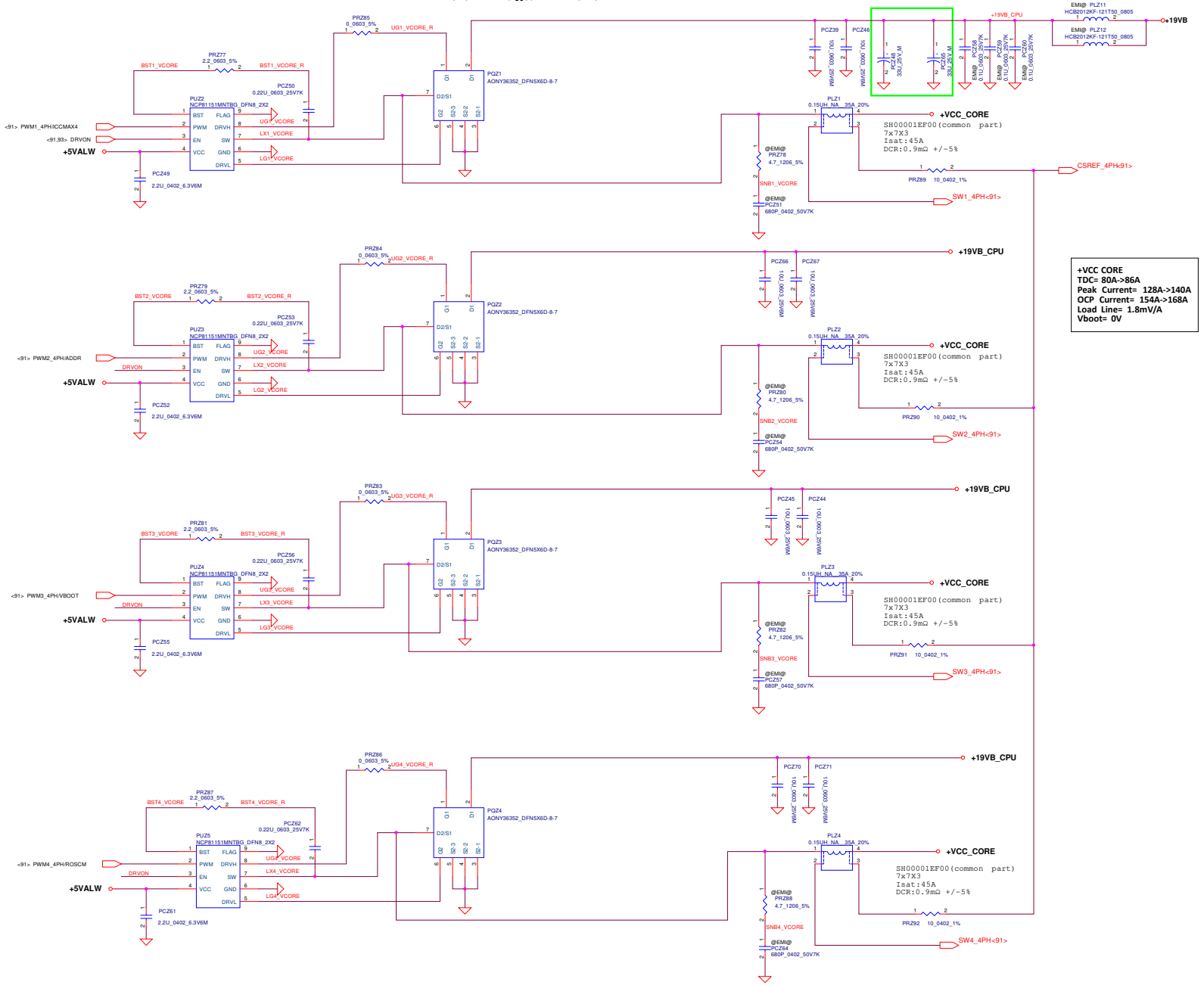
Main Func = CORE

MOSFET: DFN 5X6E
H/S Rds(on): 7.1mohm(Typ), 9.1mohm(Max)
L/S Rds(on): 2mohm(Typ), 2.5mohm(Max)



+VCC CORE
TDC= 80A->86A
Peak Current= 128A->140A
OCP Current= 154A->168A
Load Line= 1.8mV/A
Vboot= 0V

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Title: CPU_CORE
Size: Custom | Document Number | Rev: 1.0
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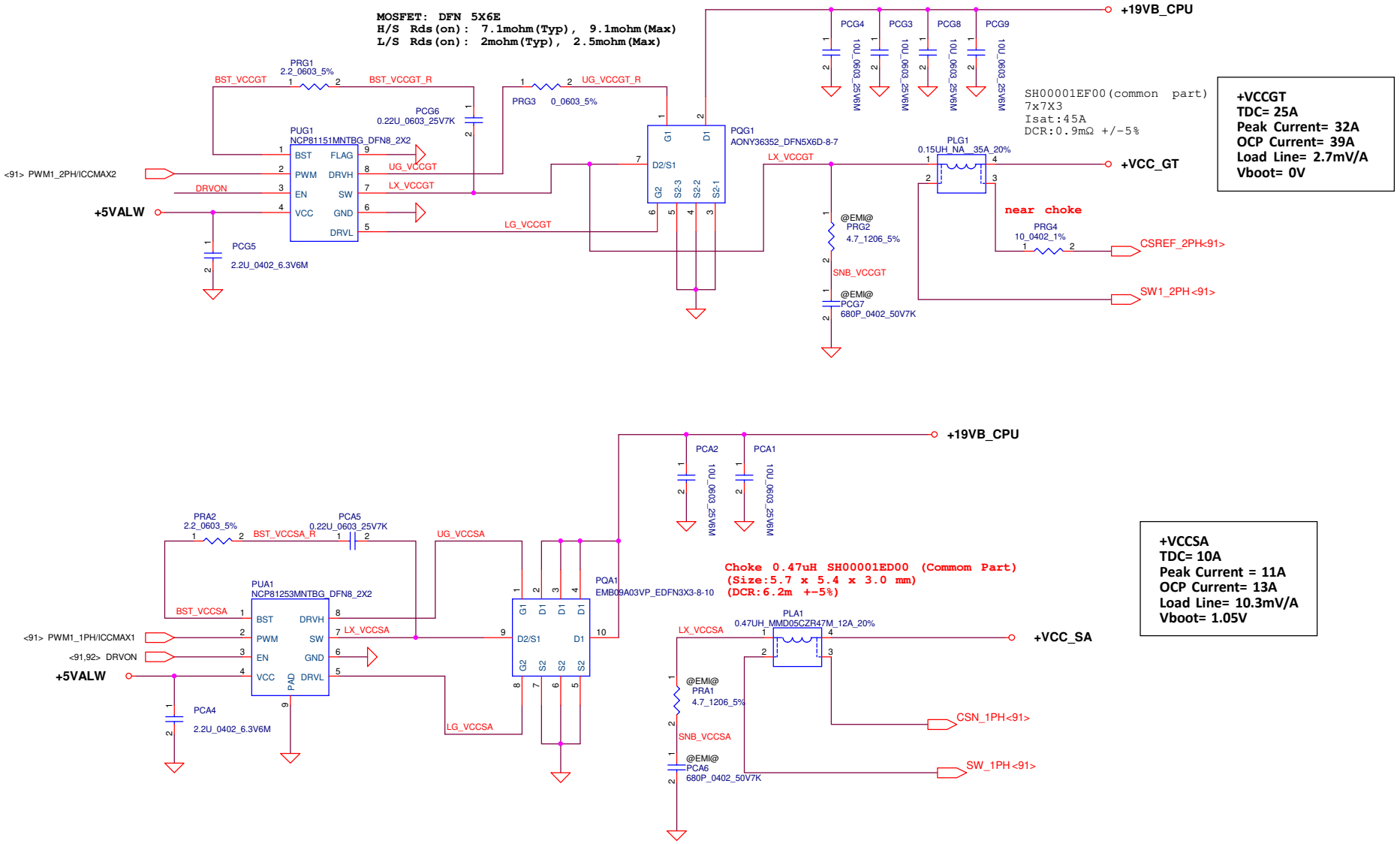
Main Func = VCCGT/+VCCSA



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Compal Electronics, Inc.			
Title	+VCC_GT/+VCC_SA		
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Title: *Reserve*		
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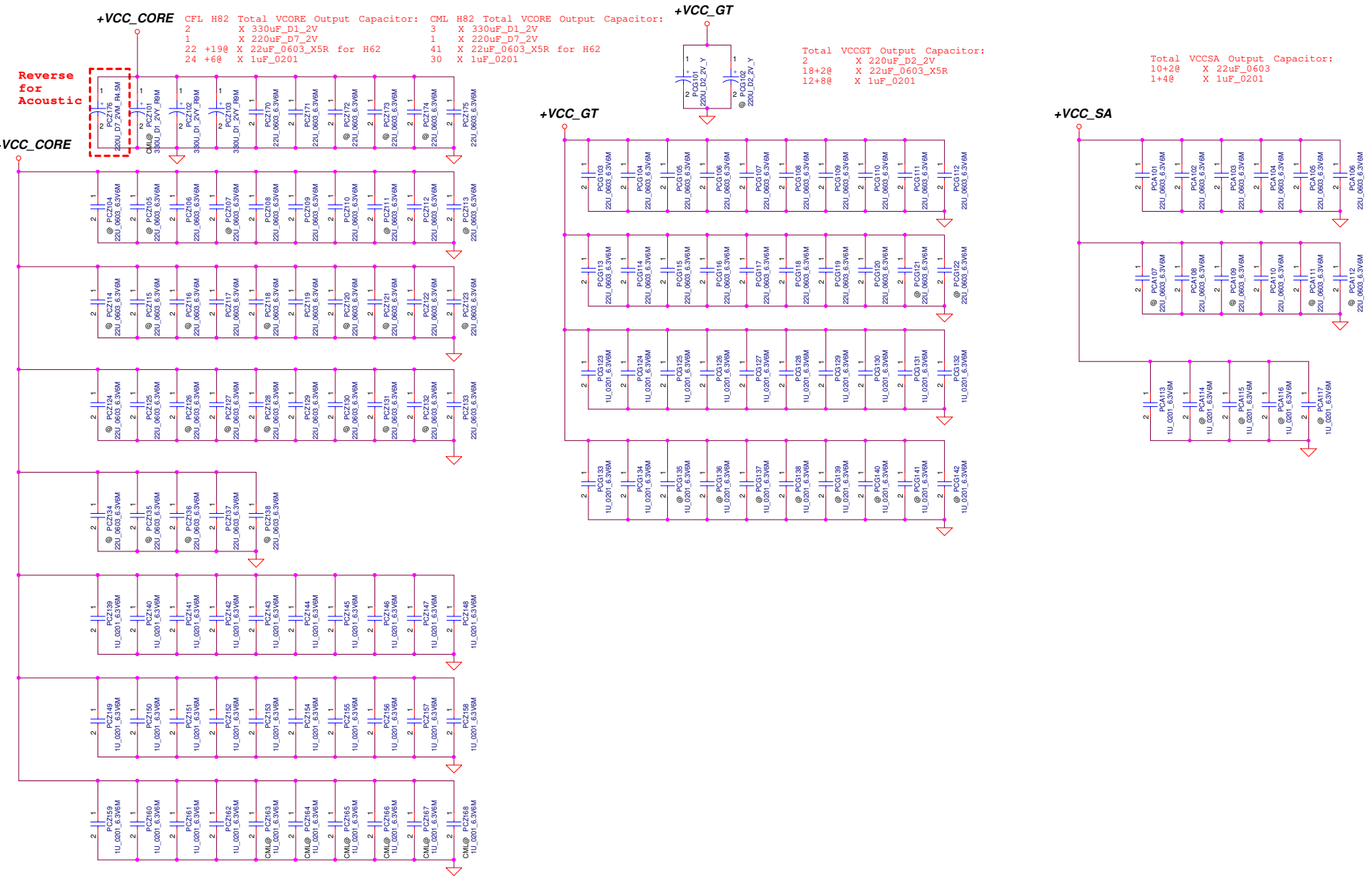

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Issued Date	2019/09/20	Deciphered Date	2020/09/20

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Title: FXXXX M/B LA-J871P

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Custom		1.0

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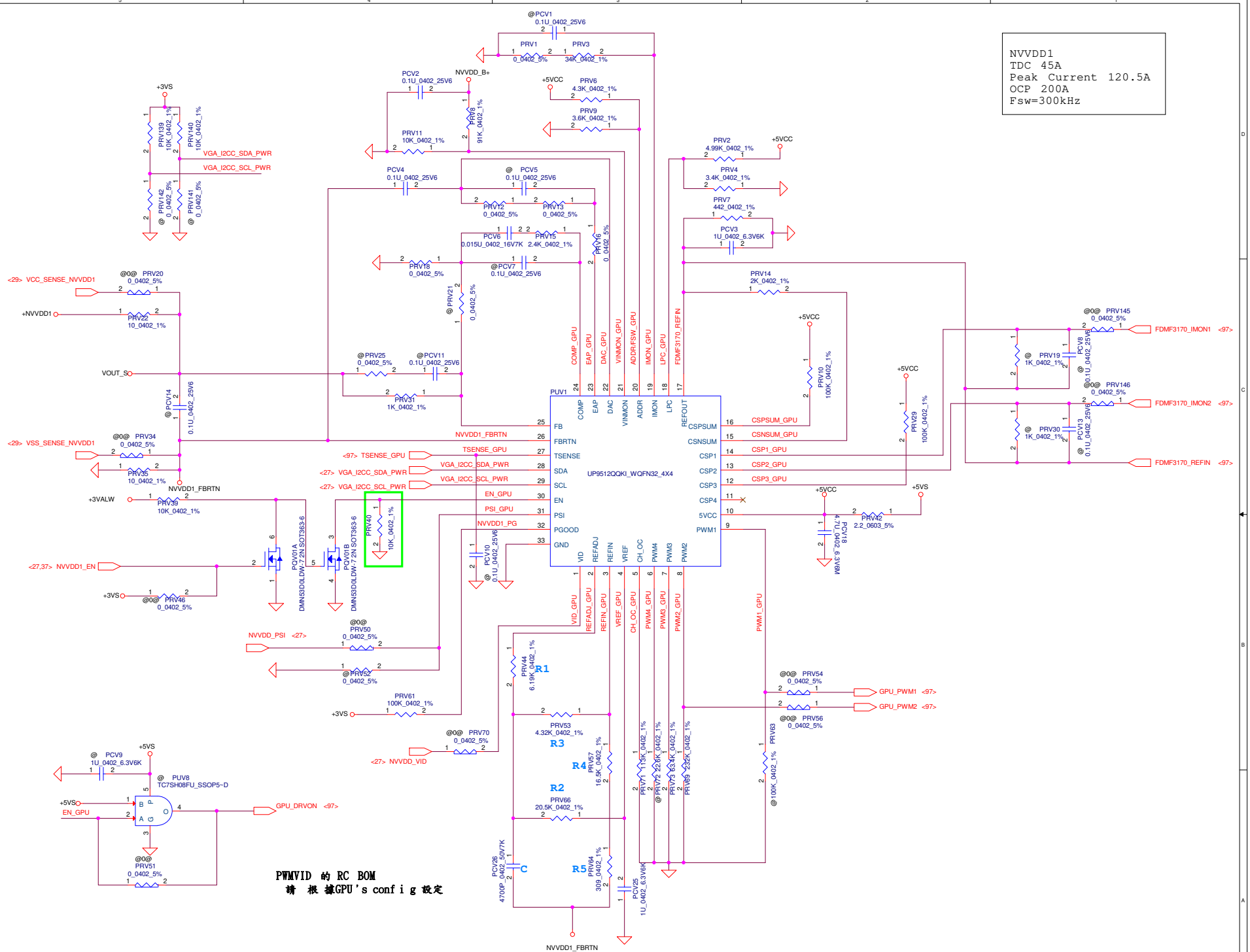

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.			
Title: PWR_VGA_UP9512P			
Size	Document Number: FXXXX M/B LA-J871P		Rev: 1.0
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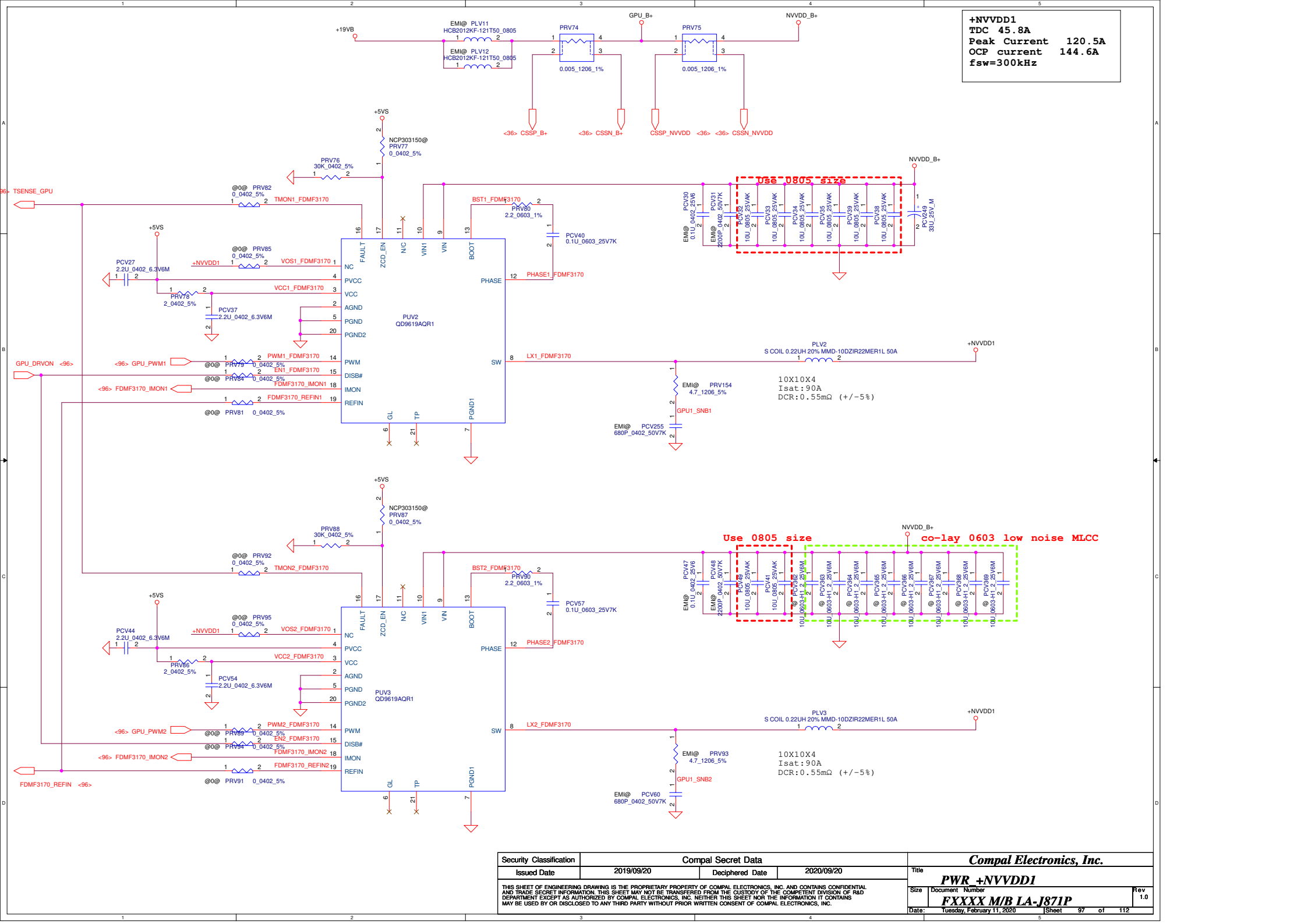

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

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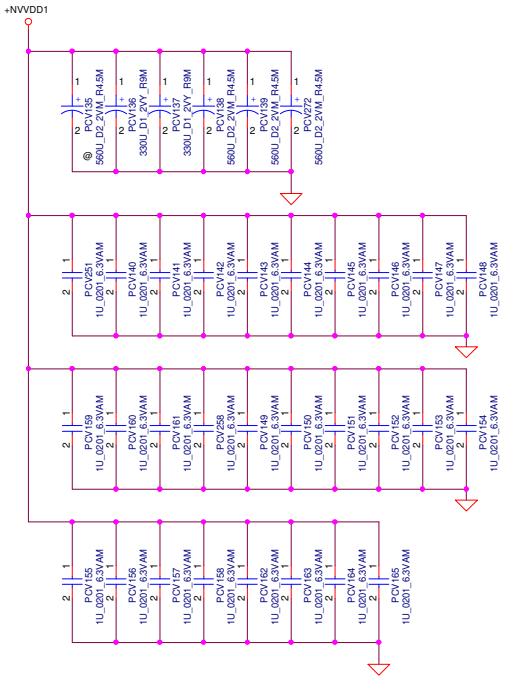
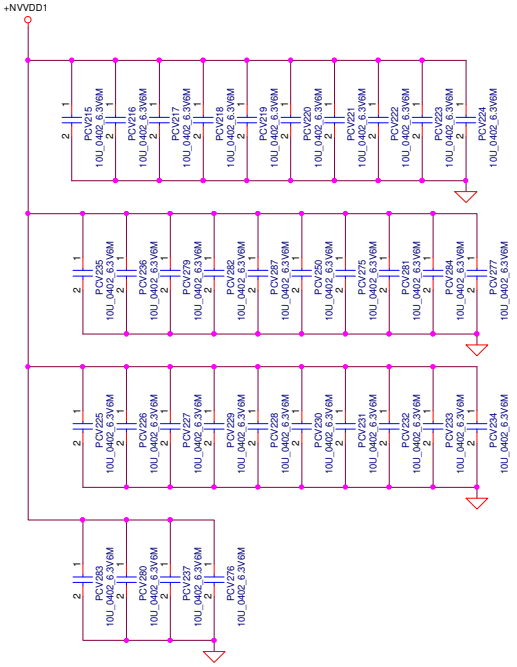
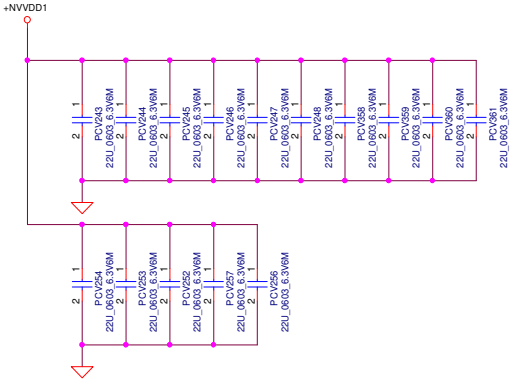
N18P-G62
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)







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Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: **PWR_VGA DECOUPLING**

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co-lay 0603 low noise MLCC

Samesung & Micron VRAM
When,VRAM_VDD_CTL=High
Vboot=1.25V
When,VRAM_VDD_CTL=Low
Vboot=1.2V

MOSFET: DFN 5X6E
H/S Rds(on): 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on): 0.8mohm(Typ), 1.05mohm(Max)

13X8X4
Isat:55A
DCR:1.3mΩ (+/-5%)

+1.35VSDGPU
N18P-G62
TDC 17.2A
Peak Current 18.4A
OCP current 30A
fsw=400kHz

+1.35VSDGPU

REF1
REF2
RBOOT
REFADJ

Rocset for 75.6A

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Title: PWR_+1.5VRAM

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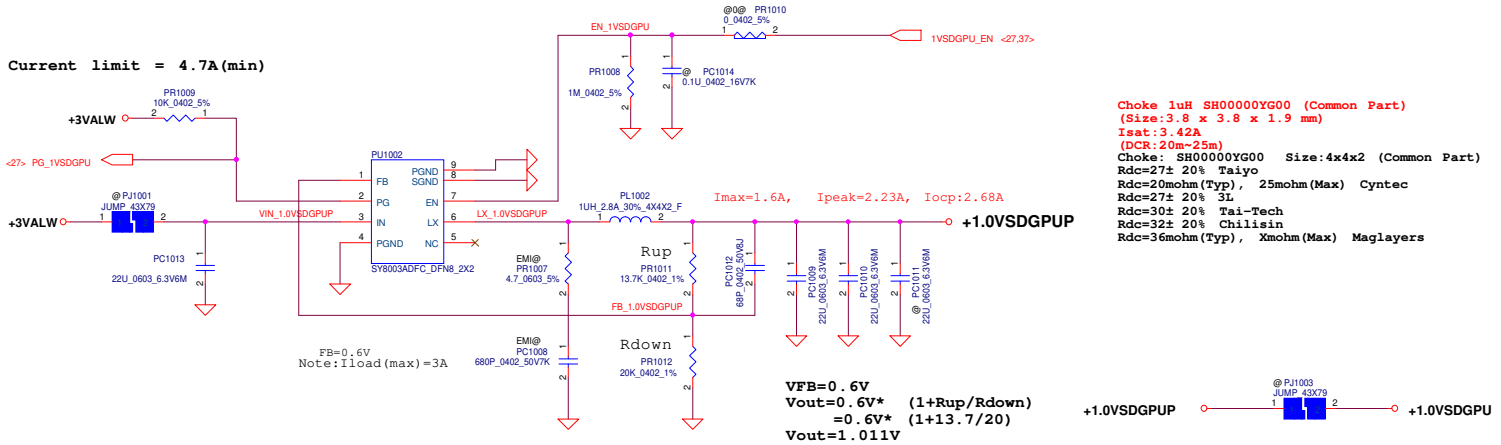

Security Classification	Compal Secret Data		
Issued Date	2019/09/20	Deciphered Date	2020/09/20

Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
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Compal Electronics, Inc.

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	NA	for cost down		PUZ1 change from ncp81215m_SA0000AQE00 to ncp81215p_SA0000CTW00 PCZ24, PCZ27 change from 82P_0402_SE000014700 to 82p_0402_SE071820J80 PCB17 change from 2.2u_0603_25V_SE00000WP00 to 2.2u_0603_16V_SE000006S80 PCB20 & PCB21 change from 100p_0603_SE024101J80 to 100p_0402_SE071101J80 PCM6 change from 10u_0603_SE000005T80 to 22u_0603_SE00000M000 PCM7 10u_0603_SE000005T80 change to unpop PRB12 change form 10_1206_SD011100A80 to 10_0805_SD002100A80	1202	DVT
02	NA	avoid incomplete replacement	P85	PQB1 & PQB11 change from 2n7002_SB000009Q80 to 2n7002_SB00001GE00	1202	DVT
03	NA	sourcer request	P84	PQ201 change from BSS139_SB00001GD00 to BSS138_SB00000PF00	1202	DVT
04	NA	NA	P85	Add PRB37 & PRB38 & PRB39 0_0402_SD028000080. avoid chager B2B damage	1209	DVT
05	NA	for acoustic noise	P97	Co-lay PCV362~PCV369 10u_0603_SE00000X210 for acoustic noise.	1209	DVT
06	NA	for acoustic noise	P100	Co-lay PCW24~PCW26 10u_0603_SE00000X210 for acoustic noise.	1209	DVT
07	NA	CPU transient	P91	PRZ49 change from 274k_0402_SD034274380 to 165k_0402_SD034165380 PRZ14 change from 28k_0402_SD034280280 to 29.4k_0402_SD034294280	1212	DVT
08	NA	CPU transient	P95	PCZ101 330u_D2_SGA00009S00 change to unpop for CFL PCZ102 & PCZ103 330u_D2_SGA00009S00 change to SMT for CFL PCZ108, PCZ109, PCZ110, PCZ112, PCZ119, PCZ125, PCZ133, PCZ137 change to SMT for CFL PCZ163, PCZ164, PCZ165, PCZ166, PCZ167, PCZ168 1u_0201_SE00000UC00 change to SMT for CFL PCZ107, PCZ113, PCZ114, PCZ115, PCZ116, PCZ121, PCZ123, PCZ127, PCZ128, PCZ130, PCZ131, PCZ132, PCZ172, PCZ173, PCZ174 change to unpop for CFL PCZ104, PCZ105, PCZ107, PCZ111, PCZ113, PCZ114, PCZ115, PCZ116, PCZ118, PCZ120, PCZ121, PCZ123, PCZ124, PCZ126, PCZ127, PCZ128, PCZ130, PCZ131, PCZ132, PCZ134, PCZ135, PCZ136, PCZ138, PCZ172, PCZ173, PCZ174 22u_0603_SE00000M000 change to unpop for CML	1212	DVT
09	NA	for efficiency	P100	PRW13 change from 383k_SD034383380 to 453k_SD034453380	1212	DVT
10	NA	for DFB issue	P85	PRB3 footprint change from R_1206_4P to R_1206_4P-D	0114	PVT
11	NA	NA	P100	reserve PCW28 & PCW29 330_D1_SGA00009S00	0114	PVT
12	NA	NA	P84	PH204 SL200002H00 change to SMT PH203 SL200002H00 change to unpop	0114	PVT
13	NA	NA		PR217,PRB22,PRB25,PRV50,PRV51,PRW9 change from 0_0402 to R-short	0114	PVT
14	NA	for DFB issue	P85	PRB19 footprint change from R_1206_4P to R_1206_4P-D	0116	PVT

Compal Electronics, Inc.

Title: PIR

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PRG5 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Chnage the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 鐵鐵 鋁 皮 鐵鐵 ESD 能量透過HS小板及HS cable coupling到板造成 刮	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE00000G880) for EMI request	1/15	B
11	Design Update	Design change	90, 87	delete boost circuit and PCZ47	5/7	FH58F EVT
12	Design Update	Design change	90, 87	delete PC1112	5/7	FH58F EVT
13	Design Update	Design change	88, 93	change PCB15 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to 1U 16V K X5R 0402(SE00000OU00) change PCB16 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to S CER CAP 2.2U 16V K X5R 0402(SE000013780) Add PLV2, PLV3 second source S COIL .22UH TMPC1004H-R22MG-R5505-D 50A(SH00001XH00)	6/25	INV2
14	Design Update	change CH_OC to 75A	95	change PRV71 from S RES 1/16W 133K +-1% 0402(SD034133380) to S RES 1/16W 113K +-1% 0402(SD034113380)	6/25	FH58F PVT

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Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	52	CNVi	1205B	CNVi-Intel review (FH5VF)	Add RM67 / RM68 0-ohm Add PU RM70 / PD RM69 (Reserve)		
2	52	UART_BT	1205B	UART_BT review	RM66 Change to @ for Vender review		
3	81-111	PWR SCH	1206A	POWER update	Combined Power SCH (1204)		
4	40	HDMI	1206B	HDMI EMI solution	Remove RY52/RY53/CY27 , LS15 change to pop (EMI@) .		
5	17/69	JSSD3	1206B	JSSD3 SATA/PCIE detect	SATAGP change to GP4 & RH303 PU		
6	64	EMR	1206B	EMR Power source	RH285/RH286/RH292 power source change to +3VALW		
7	63	Touch Pad	1206B	ESD	Add CK203(100p) for ESD		
8	27	VGA	1206C	CLKREQ	RV83 change to pop(VGA@) / CV226 change to unpop (@)		
9	19	PROJECT ID	1206C	PROJECT ID	defined as Project - 50 (ID1:H / ID0:L)		
10	38	Panel OD	1206C	Panel OD function	RX11 change to unpop & BIOS needs to detect panel to select H or L .		
11	16/58	BT_ON	1206C	BT_ON change to PCH	RH304 pop (PCH) & RB85 unpop (EC)		
12	73	IO_B conn.	1209A	IO_B conn.	IO_B change pin define		
13	15/68/69	M.2 SSD	1209B	Fixed naming	› SSD1 - GPP_B9/CLKREQ4# (PCIE only) (2018 @SSD2) › SSD2 - GPP_B8/CLKREQ3# (PCIE/SATA) (2018 @SSD1) › SSD3 - GPP_B10/CLKREQ5# (PCIE/SATA) (2019 NEW)		
14	52	CNVi	1209B	CNVi-Intel review (FH5VF)	RM70 change power source to +3VS_WLAN		
15	81-111	PWR SCH	1209C	POWER update	Combined Power SCH (1209)		
16	81-111	PWR SCH	1210A	POWER update	Combined Power SCH (1209B)		
17	77	H6	1210B	For Layout	H6 change to GNDA for Layout .		
18	69	SSD3	1210B	BOM Config	ADD "SSD3@" for BOM		
19	58	Board ID	1210B	Board ID config	ADD DVT@ & DVTRGB@ for DVT BOM		
20	52	CNVi	1210C	CNVi-Intel review (FH51M)	› RM69 change to 71.5k & CNVI@ › RM70 set CNVI@ › RH22 change to 20K › RM36/RM37/RM67/RM68 change to 22 ohm		
21	63	ESD	1211B		› Pop CK203 680p & ESD@ › CB12/CB13 change to 33p for ESD & ESD@		
				PVT Rev 1.0			
22	63	SW	0114A	BTN	SW1 set EVT@		
23	58		0114A	Action plan	CB6/CB9 100P 0402 Change to SE00000SE00 (0201)		
24	15		0114A	Action plan	CH7/CH8 10P 0402 Change to SE173100J80 (0201)		
25			0114A	Action plan	RO25 Change to 0201 R-short		
26			0114A	Action plan	RH100 Change to 0603 R-short		
27			0114A	Action plan	RS112/RS137/RA9/RB87/RX8/RX9 Change to 0402 R-short		
28	52	CNVi	0114A	CNVi-Intel review (FH5VF)	Add CM51/CM52 10U Add CM53/CM54 0.01U		
29	81-111	PWR SCH	0114B	POWER update	Combined Power SCH (0114B)		
30	63		0115B	Action plan	R41 Change to 0603 R-short R18 Change to 0201 R-short *remove KBLED@		
31	81-111	PWR SCH	0116A	POWER update	Combined Power SCH (0116)		
32	6	CPU/PCH	0211A		Update CPU/PCH PN & config		
33	62	LED	0211A		RG4/RG11 change to 1k		
34	58	Board ID	0211A	Board ID config	ADD PVT@ & PVTRGB@ for PVT BOM		

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