UltraBook 15" Schematics Document

Ivy Bridge
Panther Point

2012-08-14
REV : A00

DY : None Installed
UMA: UMA only installed
SG: Optimus solution installed.

<Core Design>

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Title: *Cover Page*		
Size: A3	Document Number: *BMW Z5 DIS*	Rev: *A00*
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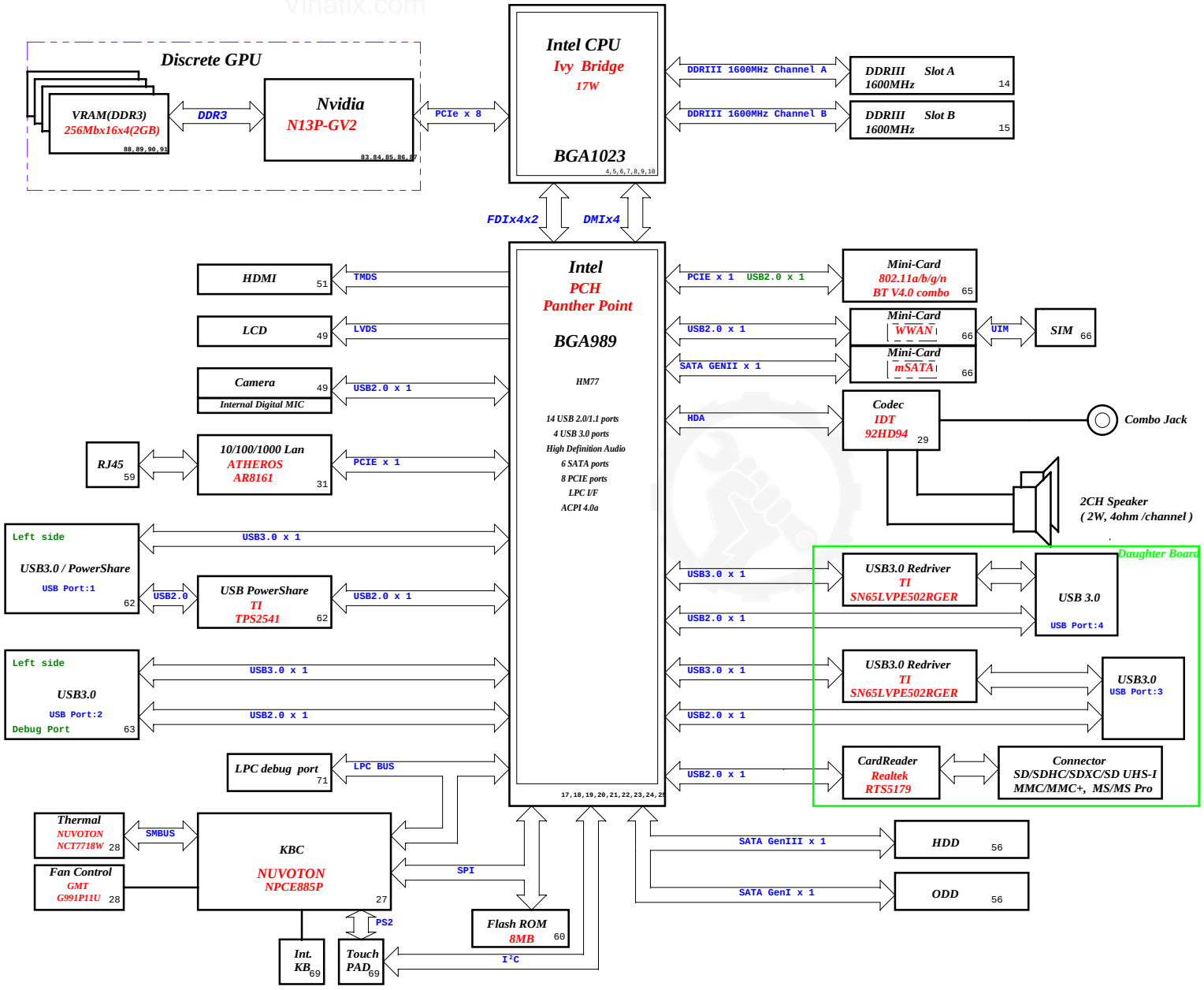
Block Diagram (Discrete / UMA)

Project code : 91.4VQ01.001
PCB P/N : 1319F
Revision : 11307-1



CHARGER BQ24727 40	
INPUTS	OUTPUTS
AD+	BT+

SYSTEM DC/DC TPS51125RGER 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

CPU DC/DC VT1318+VT1326 42,43	
INPUTS	OUTPUTS
5V_S5	VCC_CORE

GFX DC/DC VT1318+VT1323 44	
INPUTS	OUTPUTS
5V_S5	VCC_GFXCORE

SYSTEM DC/DC VT385	
INPUTS	OUTPUTS
5V_S5	1D05V_PCH VCCP_CPU 45

SYSTEM DC/DC TPS51216 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC APL5916 48	
INPUTS	OUTPUTS
5V_S5	0D85_S0

VGA DC/DC ADP3211 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5 3D3V_S5 3D3V_S5 1D8V_S0 1D5V_S3 VCCP_CPU	1D5V_S0 5V_S0 3D3V_S0 3D3V_WLAN_AOAC 3D3V_VGA_S0 1D8V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0

UMA/Discrete PCB LAYER	
L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
INTVRMEN	Integrated 1 V VRMs is enabled when high, External when low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
DF_TVS	DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor.
HAD_DOCK_EN# /GPIO[33]	This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Sandy & Ivy Bridge Compatibility

Pin Name	Configuration	Schematic Notes
DDR3 VREF	Sandy Bridge + Ivy Bridge	DDR3 VREF, M1 and M3 function are required.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	Sandy Bridge + Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO_SEL	Sandy Bridge + Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both.
	Ivy Bridge	No change.
VCCSA_VID[0:1]	Sandy Bridge + Ivy Bridge	VCCSA[0:1] are the select pin of VCCSA's power control.
	Ivy Bridge	No change.

Power Plane

Power Plane	Voltage	Actice Status	Description
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1V_S0 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1V 0.85V 0.75V 0.3V to 1.3V 0 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Processor Strapping

Chief River Schematic Checklist Rev.0_72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value	POP Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1	0
CFG[4]		1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	1	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express	11	10

USB Table

Pair	Device
0	USB3.0 port1, With Power Share
1	USB3.0 port2 , Debug Port
2	USB3.0 port3
3	USB3.0 port4
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

PCIE Table

PCIE	
Lane	Device
1	NC
2	NC
3	NC
4	WLAN
5	NC
6	Onboard LAN
7	NC
8	WWAN

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	NC
3	NC
4	ODD
5	NC

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Title: Table of Content

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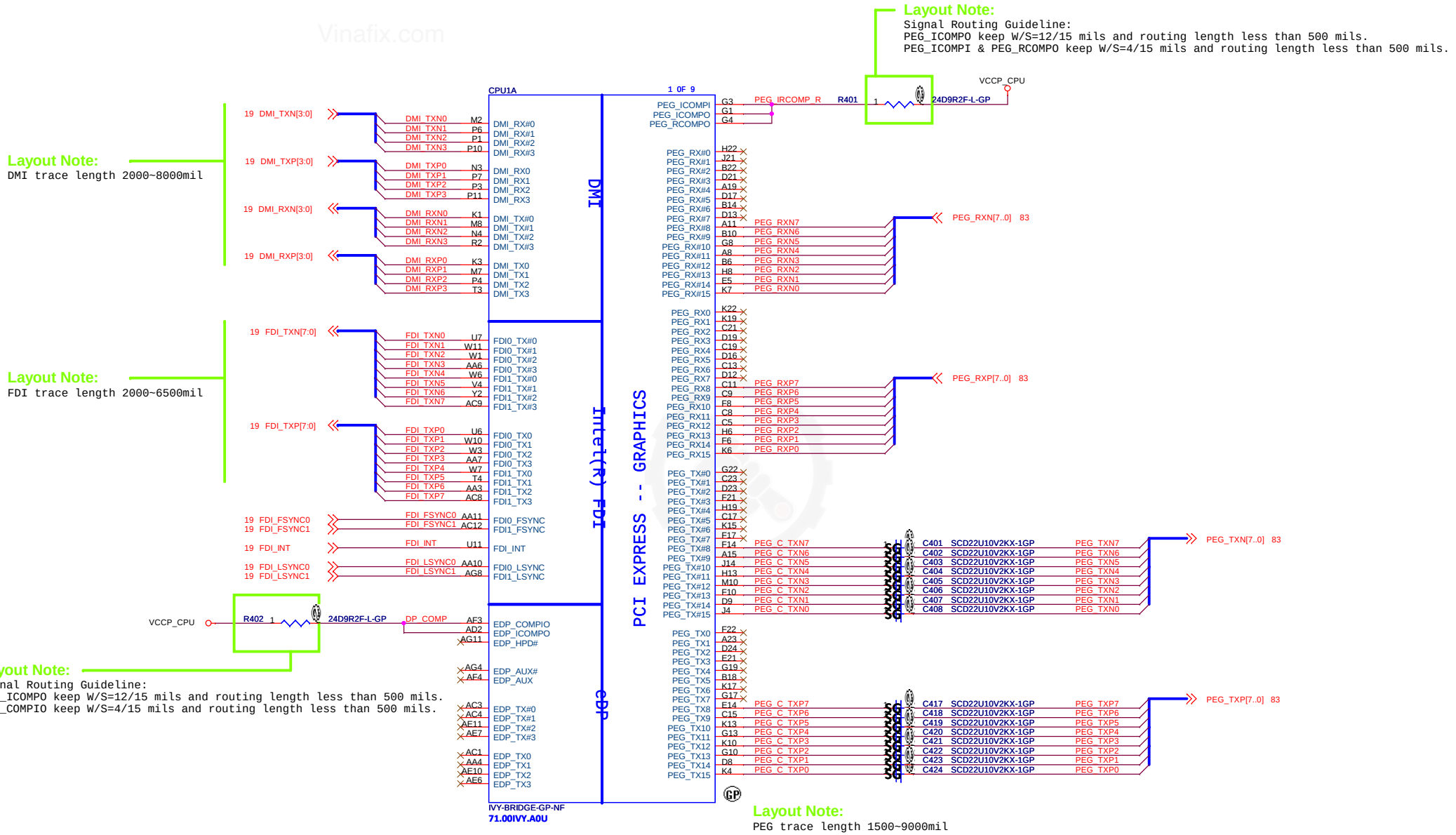
SSID = CPU



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Title: CPU(PCIE/DMI/FDI)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

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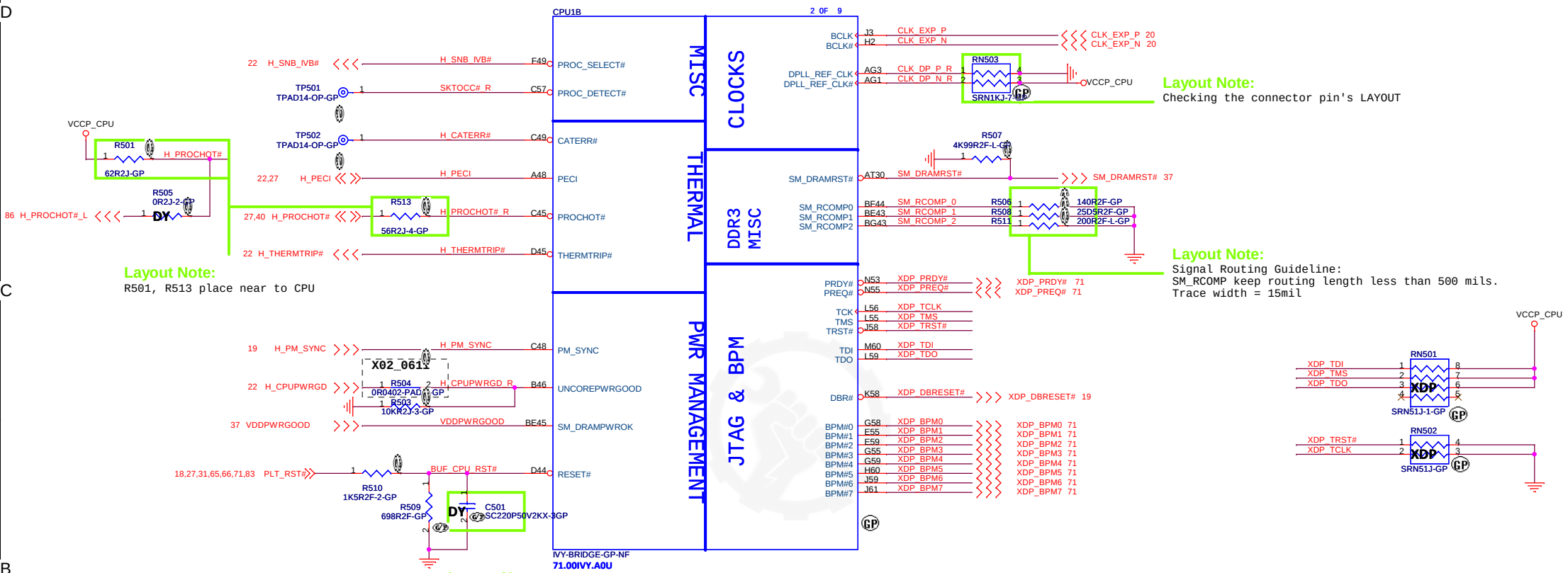
SSID = CPU



Layout Note:
R501, R513 place near to CPU

Layout Note:
C501 place near to CPU

Layout Note:
Checking the connector pin's LAYOUT

Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil

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Title: CPU(THERMAL/CLOCK/PM)

Size	Document Number	Rev
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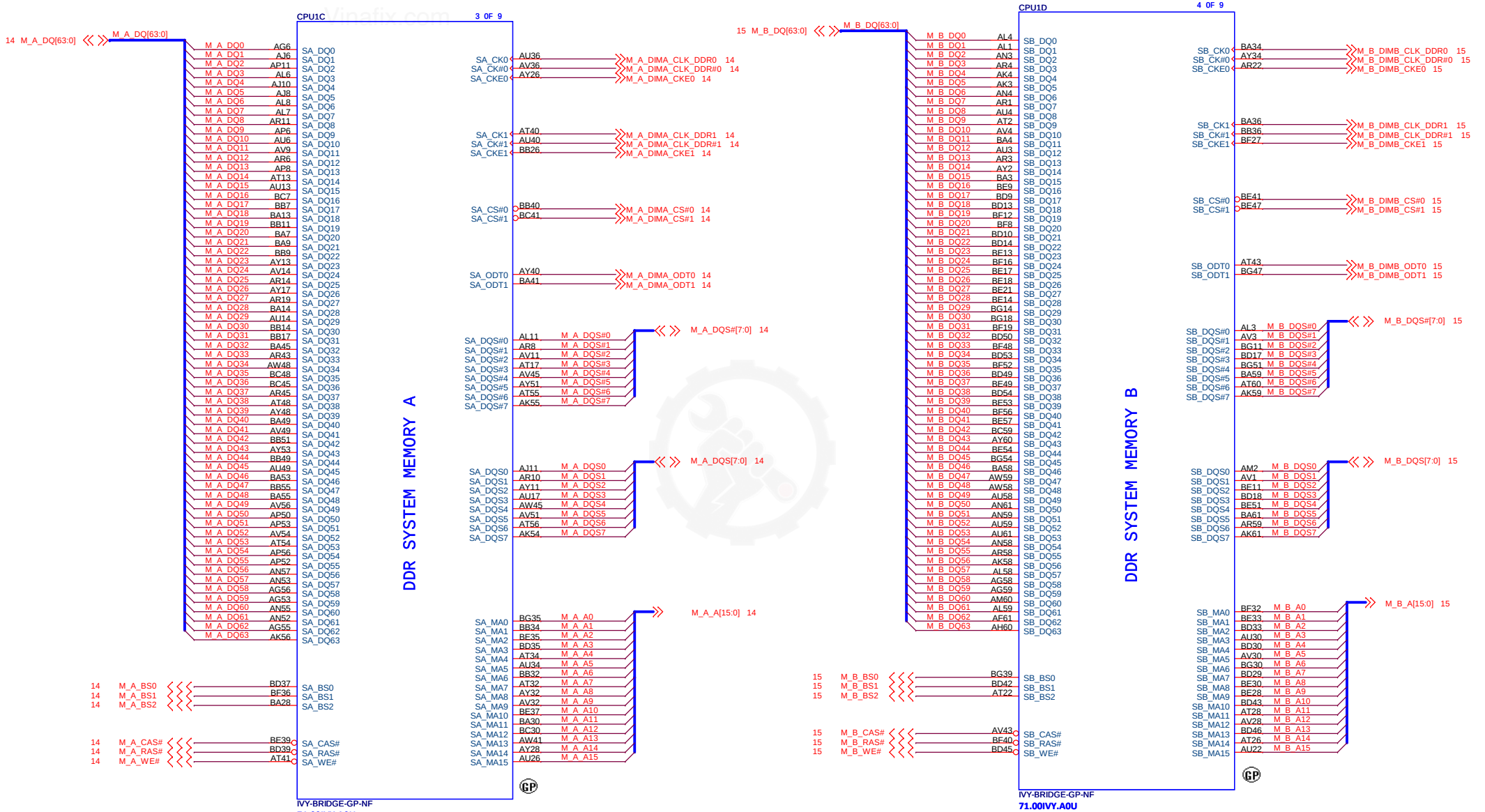
SSID = CPU



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Title: CPU (DDR)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

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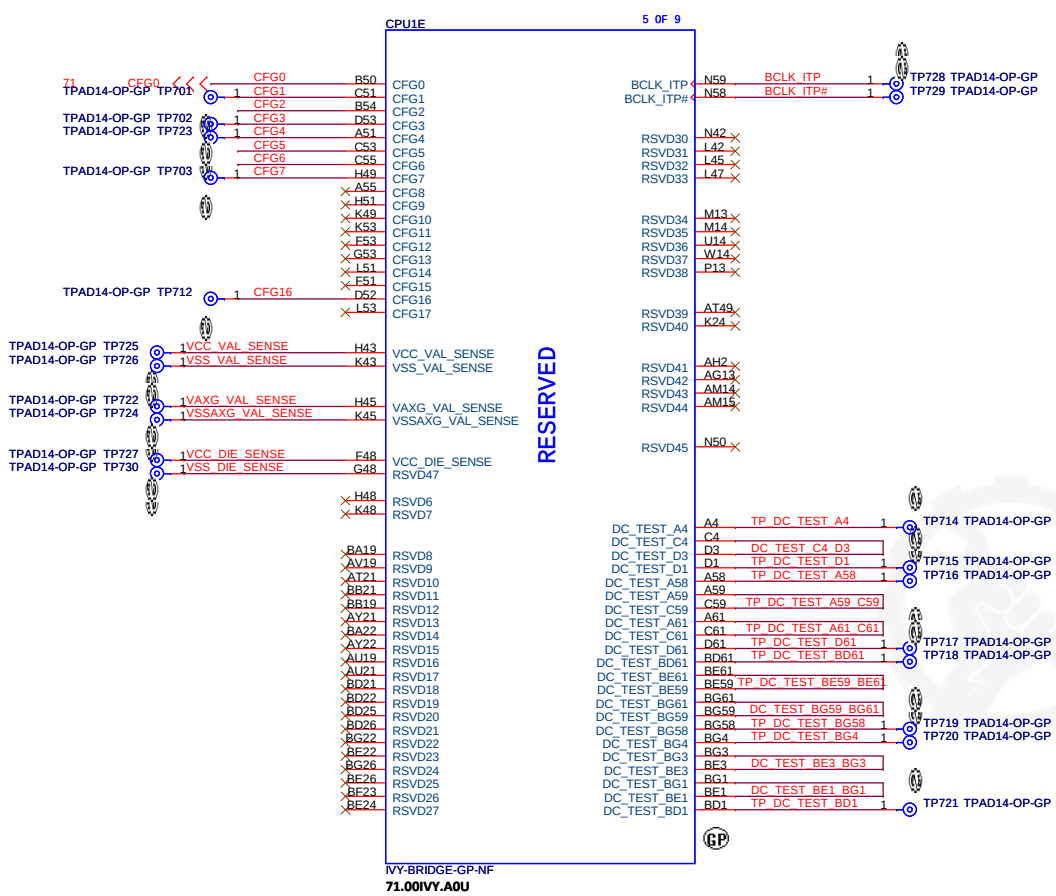
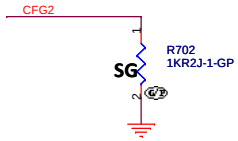
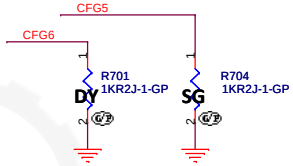
SSID = CPU





PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express
	10: 2 x8 - PCI Express
	01: Reserved
	00: 1x8, 2x4 PCI Express

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Title: CPU (RESERVED)

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

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SSID = CPU

POWER

6 OF 9

CPU1F

1u Cap x13
22u Cap x3
10u Cap x 9

8.5A

VCC_CORE

33A

X01_0412

22u Cap x20

Layout Note: 10u x 12 Cap place during CPU & IMVP

Layout Note: 2.2u x 10 Cap place under CPU

VCC Output Decoupling Recommendation:
1.9m ohm loadline design:(for SV)
470u x 4(Remove)
22u x 20(0805)
2.2u x 35(0402)

2.9m ohm loadline design:(for ULV/LV)
330u x 3(Remove)
22u x 12(0805)
2.2u x 16(0402)

VCCIO Output Decoupling Recommendation:
330u x 2(Remove)
10u x 10(0603)
1u x 26(0402)

VCCPQ Output Decoupling Recommendation:
1u x 1(0402)

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	29
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	4
VCCPLL	1.8	1.2

Added, cause the 1.05V far away CPU

X01_0424

CRB is DY

X02_0611

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Need place Pull Hi at IMVP page

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing
3. VCC_SENSE 25ohm~34ohm

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing
3. VCCIO_SENSE_VCCIO 55 ohm

IVY-BRIDGE-GP-NF
71.00IVY.A0U

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Title: CPU (VCC_CORE)
Size: A2
Document Number: BMW Z5 DIS
Rev: A00
Date: Tuesday, August 14, 2012
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SSID = CPU

POWER

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	29
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	4
VCCPLL	1.8	1.2

Layout Note:
+V_SM_VREF_CNT should have 10 mil trace width

22u Cap x 20
10u Cap x 6
1u Cap x 7

VCC_GFXCORE
29A
X01_0424
X02_0613

CPU1G
7 OF 9

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54 VAXG55 VAXG56

GRAPHICS

SM_VREF AY43
SA_DIMM_VREFDQ BE7 DDR_WR_VREFA
SB_DIMM_VREFDQ BG7 DDR_WR_VREFB
+V_SM_VREF_CNT
RN902 SRN1KJ-7-GP

VREF

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18 VDDQ19 VDDQ20 VDDQ21 VDDQ22 VDDQ23 VDDQ24 VDDQ25 VDDQ26
1D5V_S0
5A

VDDQ Output Decoupling Recommendation:
330u x 1(Remove)
10u x 8(0603)
1u x 10(0402)

VCCDQ Output Decoupling Recommendation:
1u x 1(0402)

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

VCC_GFXCORE
R903 100R2F-L1-GP-U
R904 100R2F-L1-GP-U
42 VCC_AXG_SENSE
42 VSS_AXG_SENSE
VCC_AXG_SENSE F45
VSS_AXG_SENSE G45
VAXG_SENSE
VSSAXG_SENSE

SENSE LINES

VCCDQ1 AM28
VCCDQ2 AN26
+V1.5S_VCCD_Q
1D5V_S0
R909 0R0402-PAD-2-GP

QUIET RAILS

VCCPLL1 BB3
VCCPLL2 BC1
VCCPLL3 BC4
1D8V_S0
1.2A

1.8V RAIL

VCCPLL Output Decoupling Recommendation:
330u x 1(Remove)
1u x 2(0402)

VCCAXG Output Decoupling Recommendation:
3.9m ohm loadline design:(for GT2)
470u x 2(remove)
22u x 6(0805)
10u x 6(0603)
1u x 11(0402)

4.6m ohm loadline design:(for GT1)
330u x 2(remove)
22u x 5(0805)
10u x 6(0603)
1u x 6(0402)

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8 VCCSA9 VCCSA10 VCCSA11 VCCSA12 VCCSA13 VCCSA14 VCCSA15 VCCSA16
L17 L21 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20
0D85V_S0
4A

SA RAIL

VDDQ_SENSE BC43 TP_VDDQ_SENSE
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS
TP901 TPAD14-OP-GP
TP902 TPAD14-OP-GP

SENSE LINES

VCCSA_SENSE U10
VCCSA_SENSE 48

VCCSA_VID0 D48 VCCSA_SEL0
VCCSA_VID1 D49 VCCSA_SEL1
VCCSA_SEL0 48
VCCSA_SEL1 48

VCCSA VID lines

VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
LV & ULV 0.85	0	1
Others 0.8		
0.775	1	0
0.75	1	1

VCCSA Output Decoupling Recommendation:
330u x 1(Remove)
10u x 5(0603)
1u x 5(0402)

IVY-BRIDGE-GP-NF
71.00IVY.A0U

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Title: CPU (VCC_GFXCORE)
Size: A3
Document Number: BMW Z5 DIS
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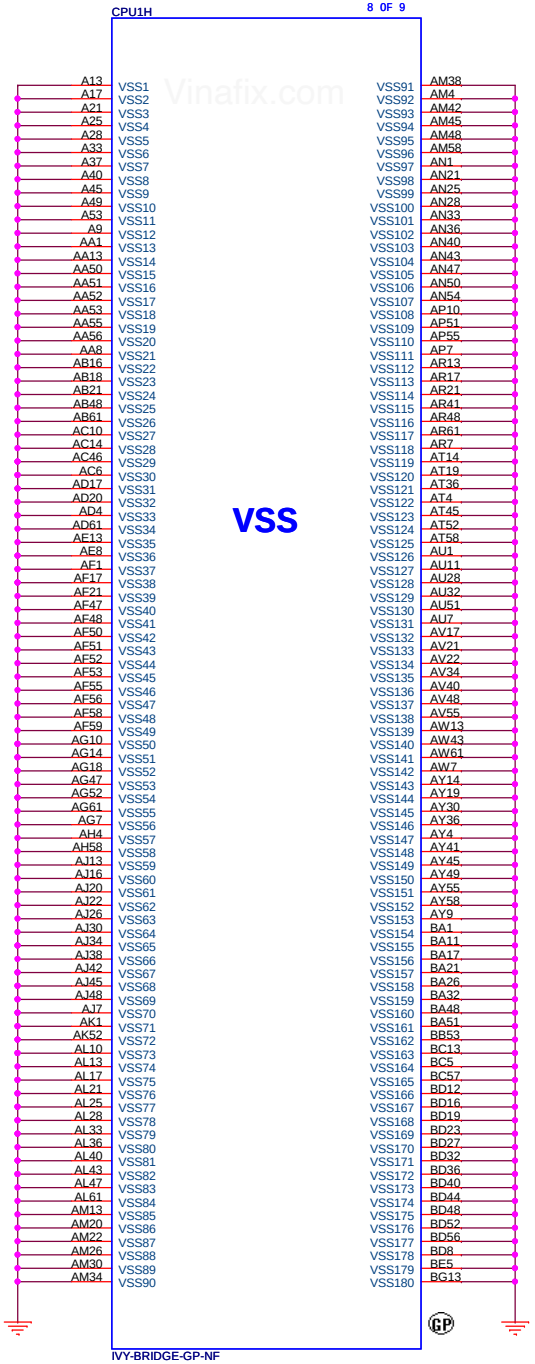
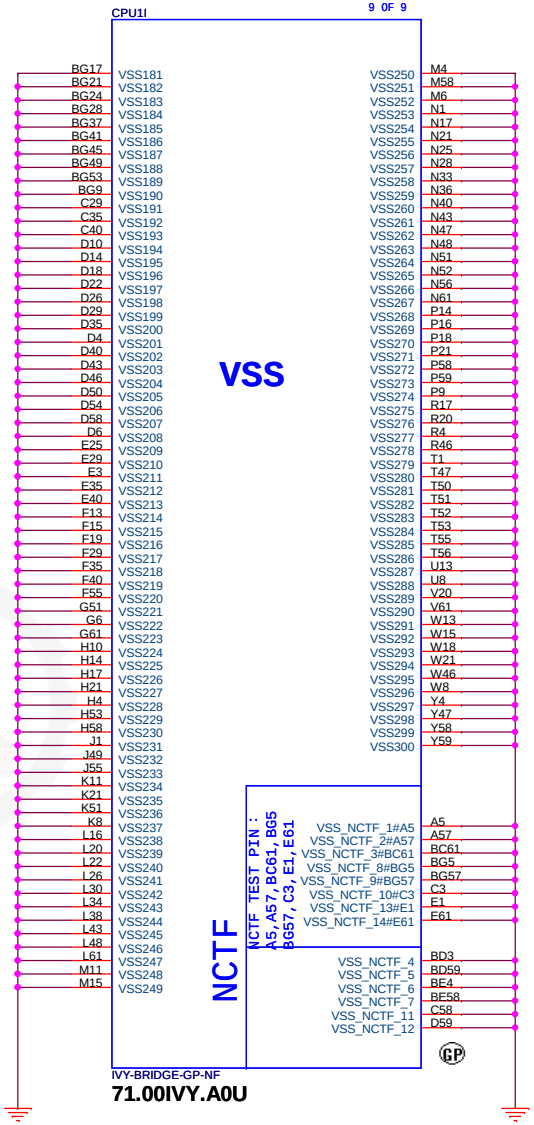
SSID = CPU





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Title: CPU (VSS)

Size	Document Number	Rev
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Title: XDP

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

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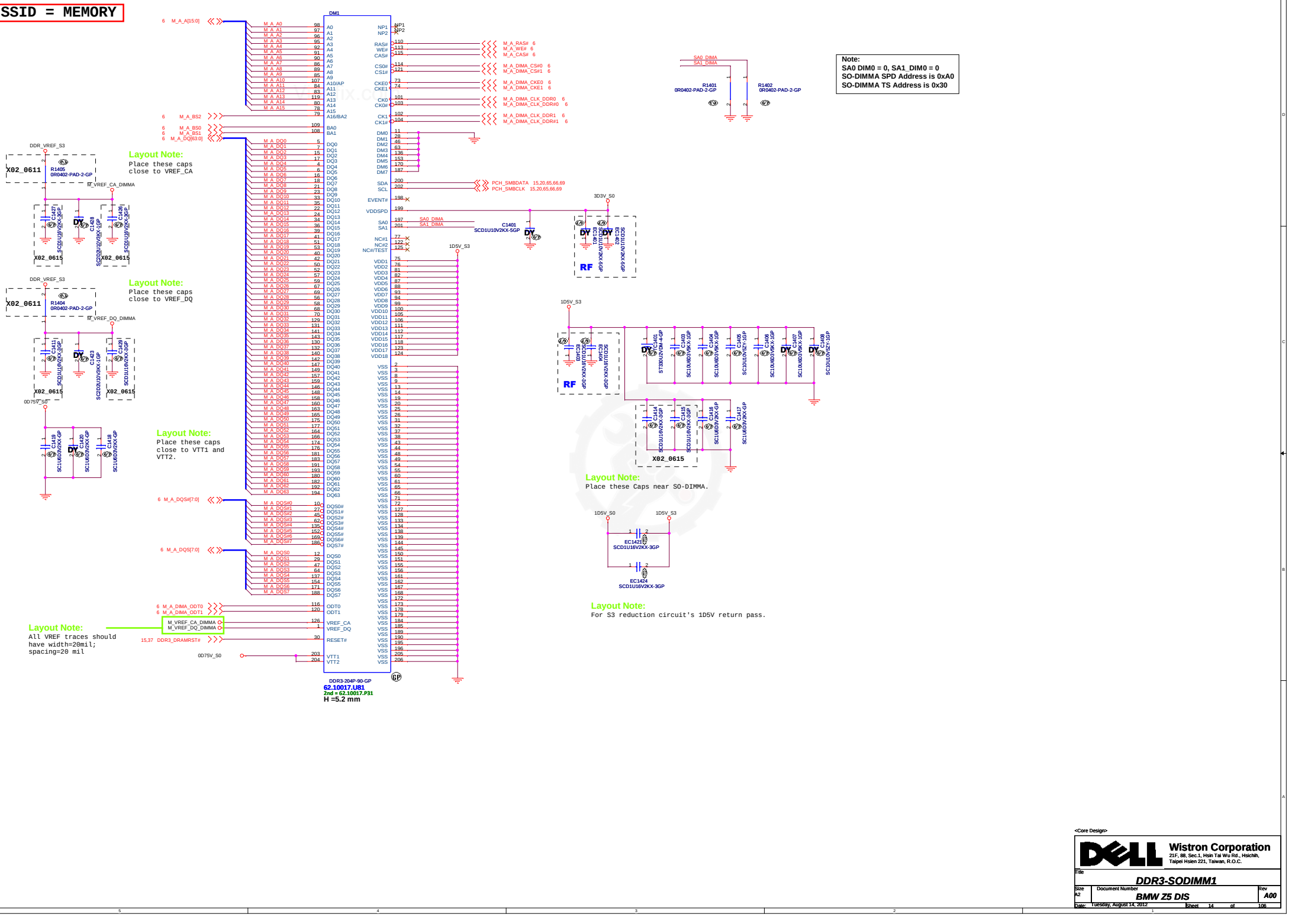
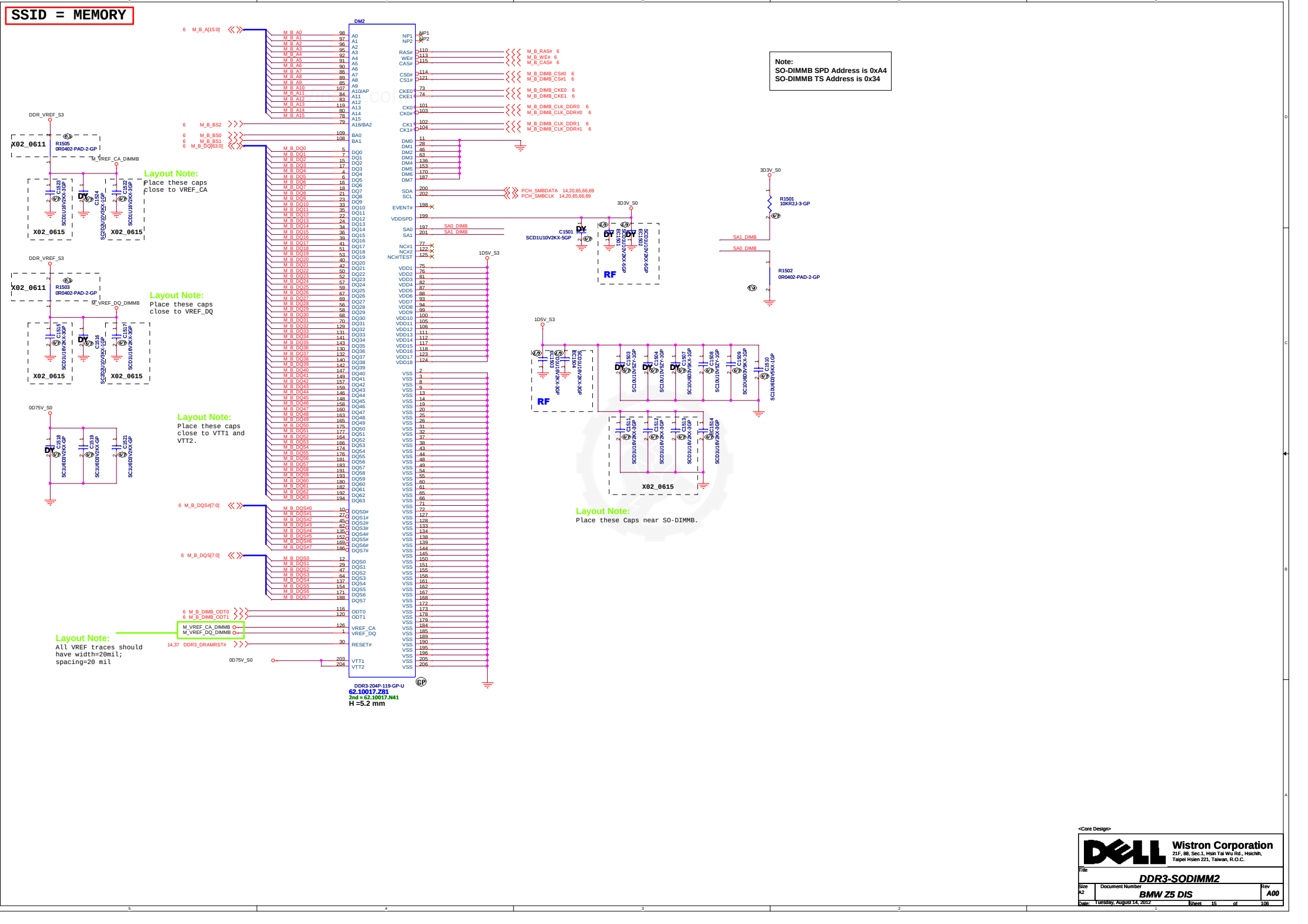
SSID = MEMORY

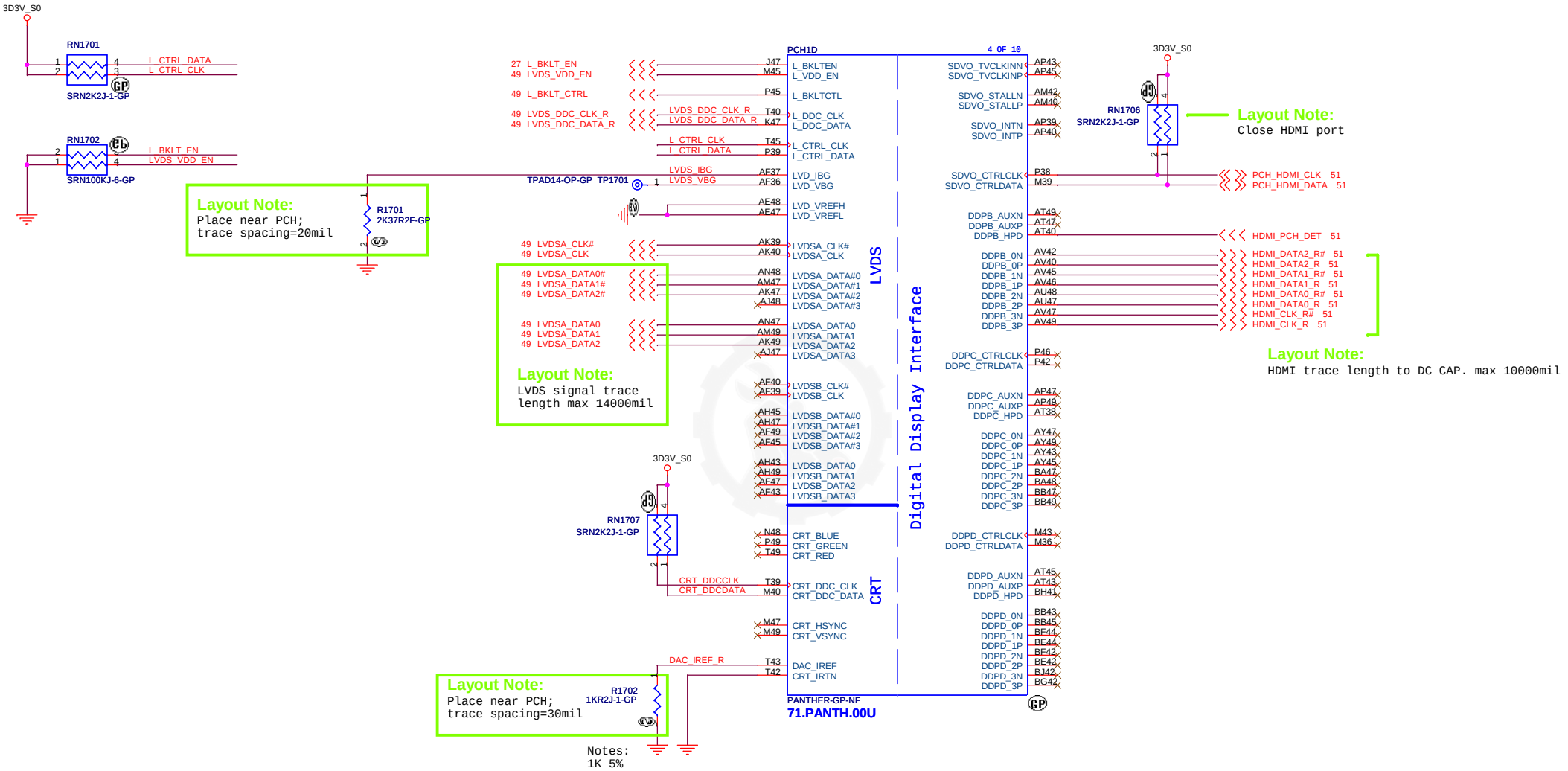


SSID = MEMORY



(Blanking)

SSID = PCH



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Title	PCH (LVDS/CRT/DDI)	
Size A3	Document Number BMW Z5 DIS	Rev A00
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SSID = PCH

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB Table

Pair	Device
0	USB3.0 port1, With Power Share
1	USB3.0 port2, Debug Port
2	USB3.0 port3 — DB
3	USB3.0 port4 — DB
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

Layout Note:
Trace Length :
PCH ~~9000mil~~Cap~~1000mil~~CONN

USB2.0 Signal Group

Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCH1E — PANTHER-GP-NF — 5 OF 10

RSVD | PCI | USB

R1801 4K7R2J-2-GP (DY)
R1805 / R1806 22R2J-2-GP
EC1802 / EC1804 SC4D7P50V2CN-1GP (DY)
R1823 0R0402-PAD-2-GP
R1816 100KR2J-1-GP (DY)
C1801 SCD1U16V2ZY-2GP (DY)
X02_0401 / X01_0417
RN1803 SRN10KJ-6-GP
RN1802 SRN8K2J-2-GP-U
RN1801 SRN8K2J-2-GP-U
R1811 22D6R2F-L1-GP

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Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: BMW Z5 DIS | Rev: A00
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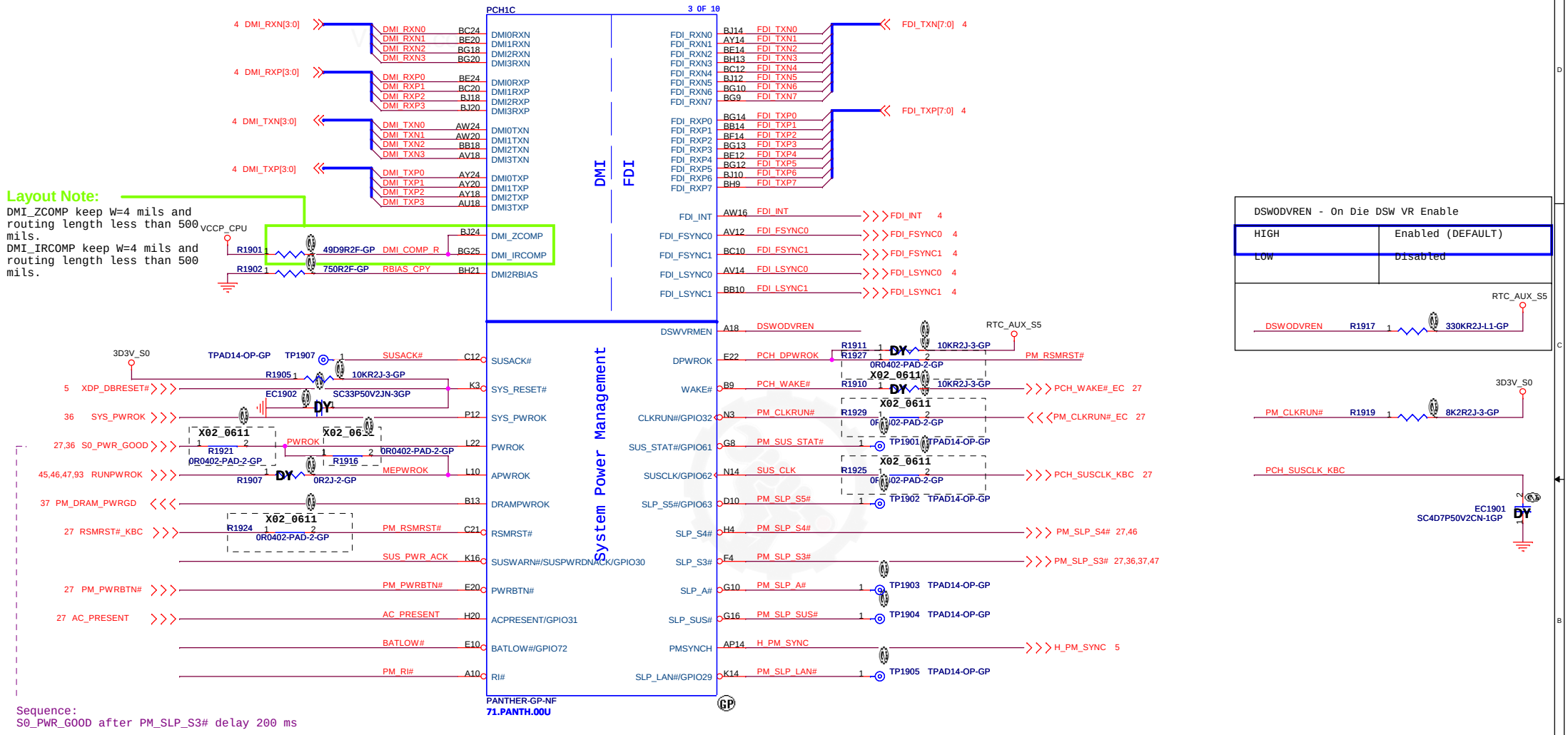
SSID = PCH



<Core Design>

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Title: PCH (DM I/FDI/PM)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

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SSID = PCH

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#

PCIE_CLK_RQ3#
PCIE_CLK_RQ0#
PCIE_CLK_RQ4#
PCIE_CLK_RQ5#
PCIE_CLK_RQ7#
PCIE_CLK_RQ2#
PCIE_CLK_RQ1#
PCIE_CLK_RQ6#

PCH1B
2 OF 10
PANTHER-GP-NF
71.PANTH.00U

PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS

WLAN CLK
LAN CLK

Layout Note:
Layout trace < 14000mil

Layout Note:
CLKOUT termination
place close to PCH <500mil

Layout Note:
CLKOUT termination
place close to PCH <500mil

Layout Note:
Layout trace < 14000mil

Layout Note:
Can Place Far away PCH

CRB : 1K
CEKLT: 10K

X02_0615
X02_0613
X02_0611

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

BIOS UMA/DIS Strap pin

	BOARD_ID1	BOARD_ID2
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
UMA	1	0
Optimus(NV)	1	1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A3
Document Number: BMW Z5 DIS
Rev: A00
Date: Tuesday, August 14, 2012
Sheet 20 of 106

SSID = PCH

Layout Note:
Place it at the open door location.

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

Layout Note:
Place near PCH

Layout Note:
Place close together.
For RNxxxx later.

Layout Note:
HDA_SDO and HDA_BCLK must be
length matched to within 500 mils

Layout Note:
Place at the separated point

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default * High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V High = 1.5V *

Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil

Layout Note:
Place close PCH(<500mil)

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A — 1 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

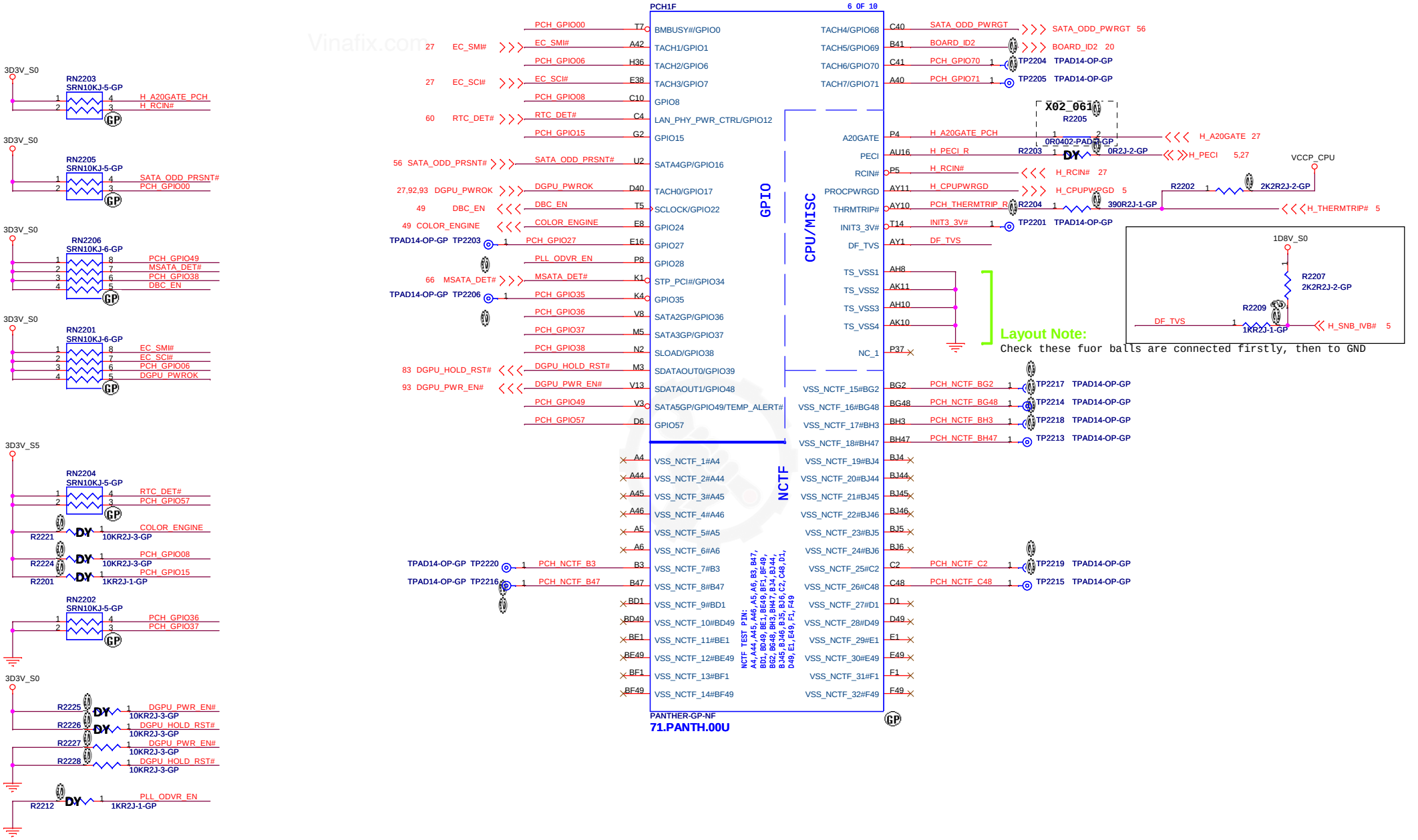
HDD1
mSATA
ODD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: BMW Z5 DIS | Rev: A00
Date: Tuesday, August 14, 2012 | Sheet 21 of 106

SSID = PCH



PLL ON DIE VR ENABLE	
GPIO28 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

<Core Design>

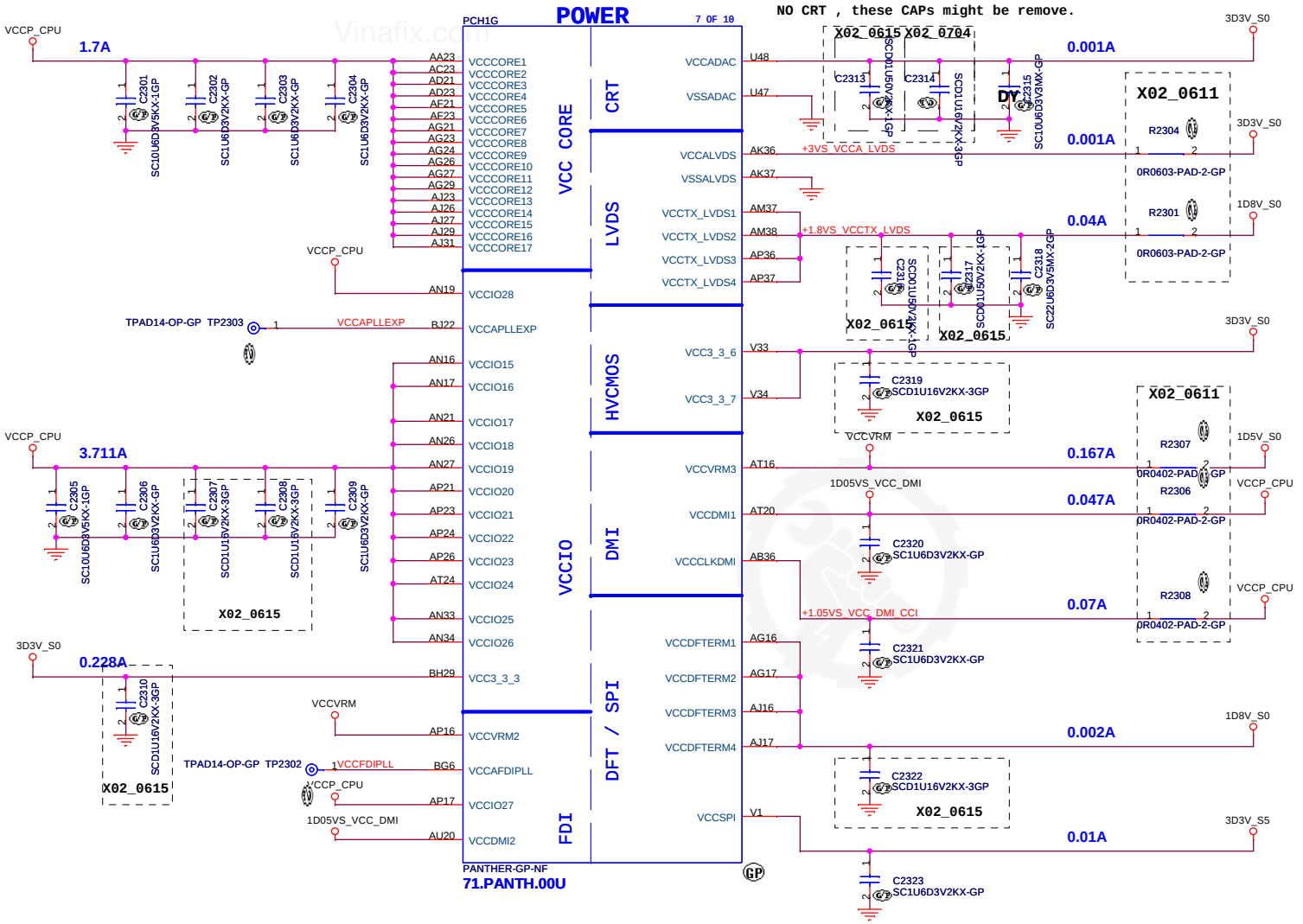
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 22 of 106

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.0.7

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 23 of 106

SSID = PCH

DG: none
CRB: 10uH

PCH1J

POWER

10 OF 10

Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

VCCSUSHDA need to be at either 3.3V or 1.5V.
All the CODEC I/O Voltages need to be at the same level either 3.3 V or 1.5 V.

<Core Design>

Refer to chipset EDS V.0.7

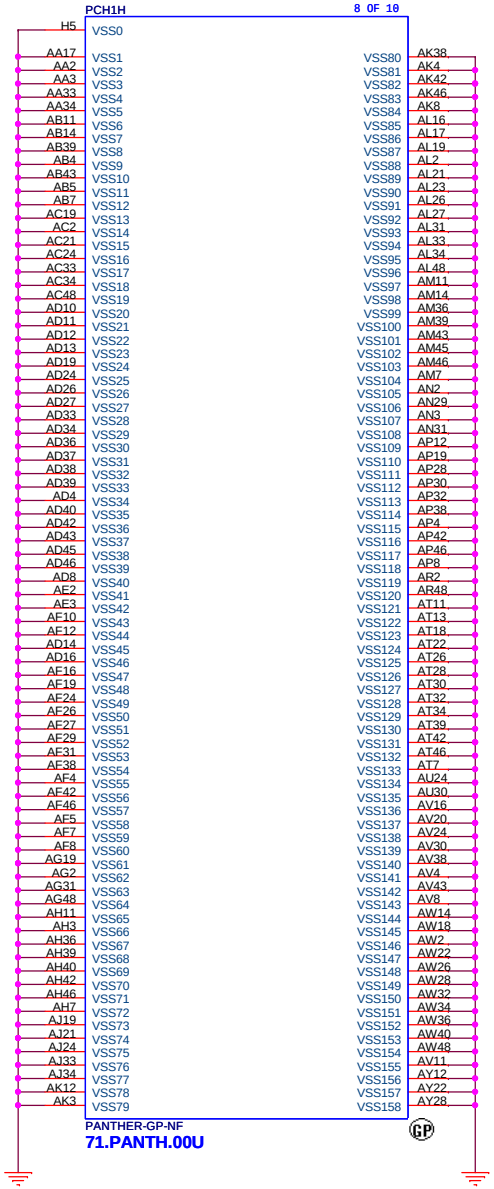
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

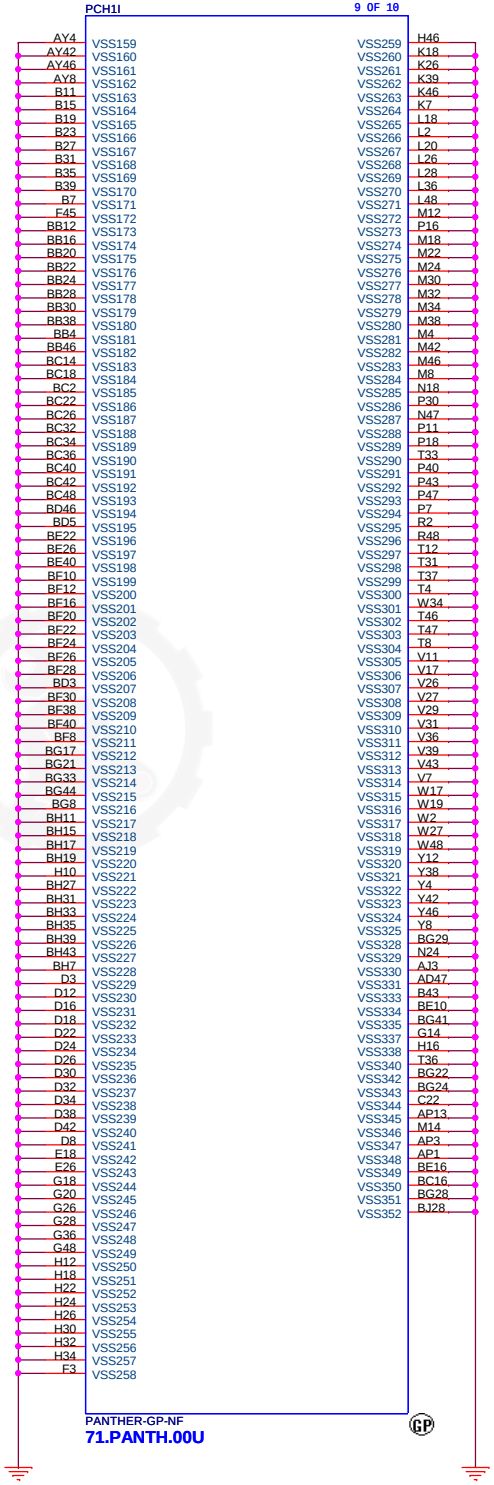
Title: PCH (POWER2)

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 24 of 106

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size: A3 | Document Number: **BMW Z5 DIS** | Rev: **A00**

Date: Tuesday, August 14, 2012 | Sheet 25 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z5 DIS* | Rev: *A00*

Date: Tuesday, August 14, 2012 | Sheet 26 of 106

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DMB50	100.0K	10.0K (64.10025.6DL)	3.0V
TBD	100.0K	13.7K (64.13725.6DL)	2.902V
TBD	100.0K	17.8K (64.17825.6DL)	2.801V
TBD	100.0K	22.1K (64.22125.6DL)	2.702V
TBD	100.0K	27.0K (64.27025.6DL)	2.598V
TBD	100.0K	32.4K (64.32425.6DL)	2.492V
TBD	100.0K	37.4K (64.37425.6DL)	2.402V
TBD	100.0K	43.2K (64.43225.6DL)	2.304V
TBD	100.0K	49.9K (64.49925.6DL)	2.201V
TBD	100.0K	57.6K (64.57625.6DL)	2.093V
TBD	100.0K	64.9K (64.64925.6DL)	2.001V
TBD	100.0K	73.2K (64.73225.6DL)	1.905V
TBD	100.0K	82.5K (64.82525.6DL)	1.808V
TBD	100.0K	93.1K (64.93125.6DL)	1.709V
TBD	100.0K	107K (64.10735.6DL)	1.594V
TBD	100.0K	120K (64.12035.6DL)	1.499V
TBD	100.0K	137K (64.13735.6DL)	1.392V
TBD	100.0K	154K (64.15435.6DL)	1.299V
TBD	100.0K	200K (64.20035.6DL)	1.099V
TBD	100.0K	232K (64.23236.6DL)	0.994V

TP

Charger

PCH

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

AOAC Ambient temperature detect

Power Switch Logic(PSL)

EC_GPIO47 High Active

For System Reset.

R2799 Stuff if LID_CLOES# is open drain.

<Core Design>

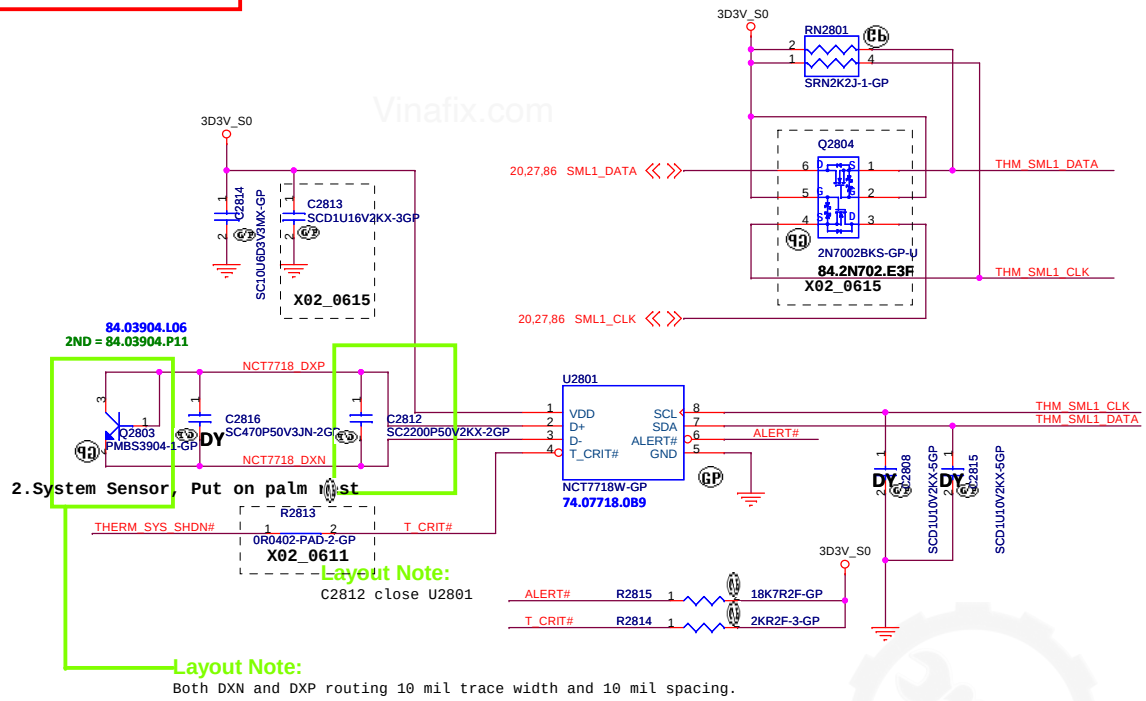
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

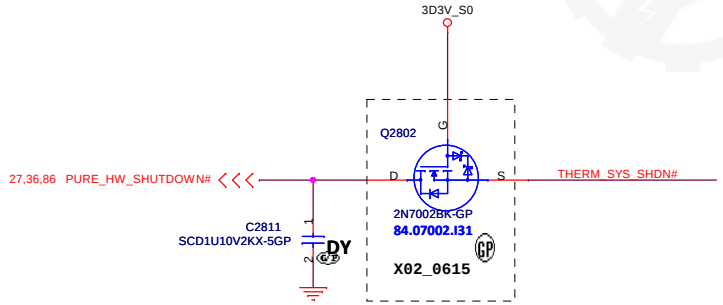
Title: KBC Nuvoton NPCE885

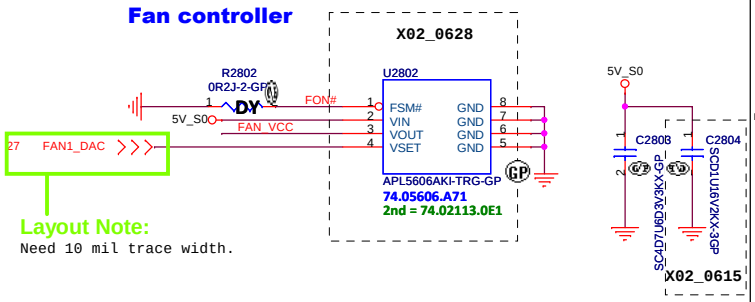
Size: A2 | Document Number: BMW Z5 DIS | Rev: A00

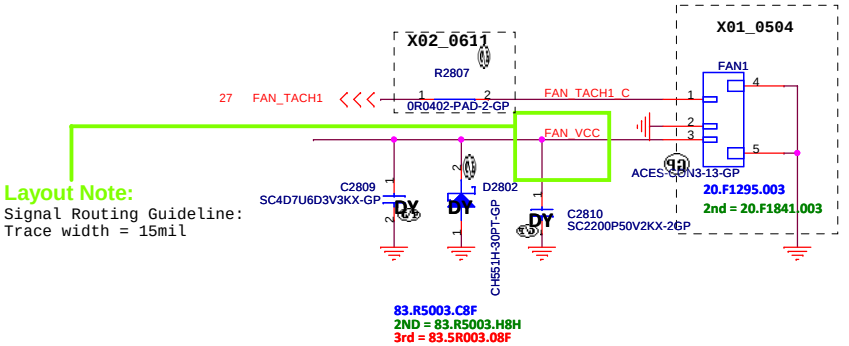
Date: Tuesday, August 14, 2012 | Sheet 27 of 106

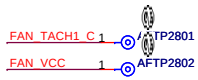
SSID = Thermal

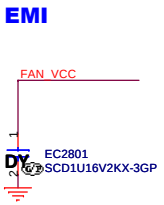












<Core Design>

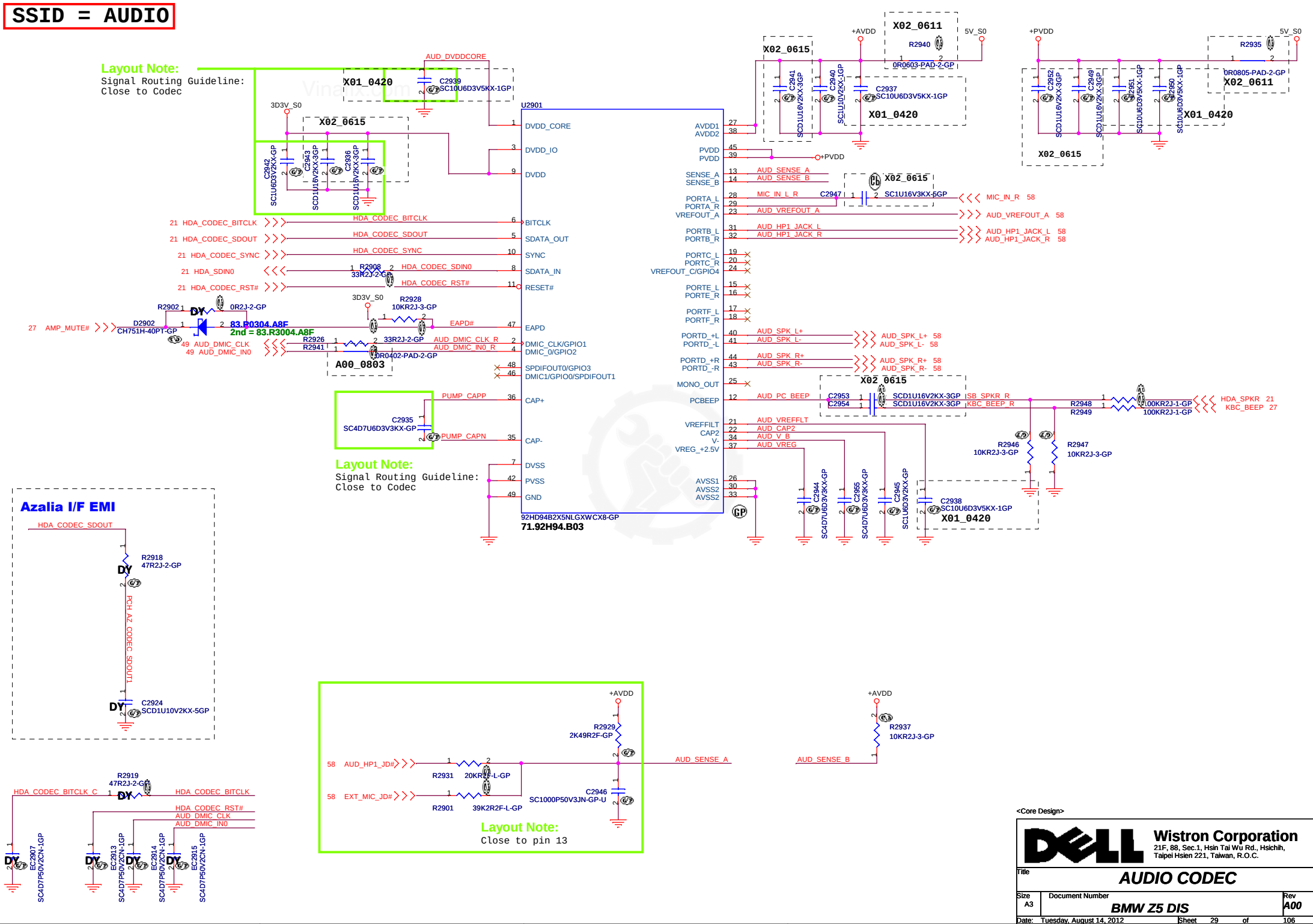
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan Controllor P2793

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 28 of 106

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 29 of 106

(Blanking)

<Core Design>

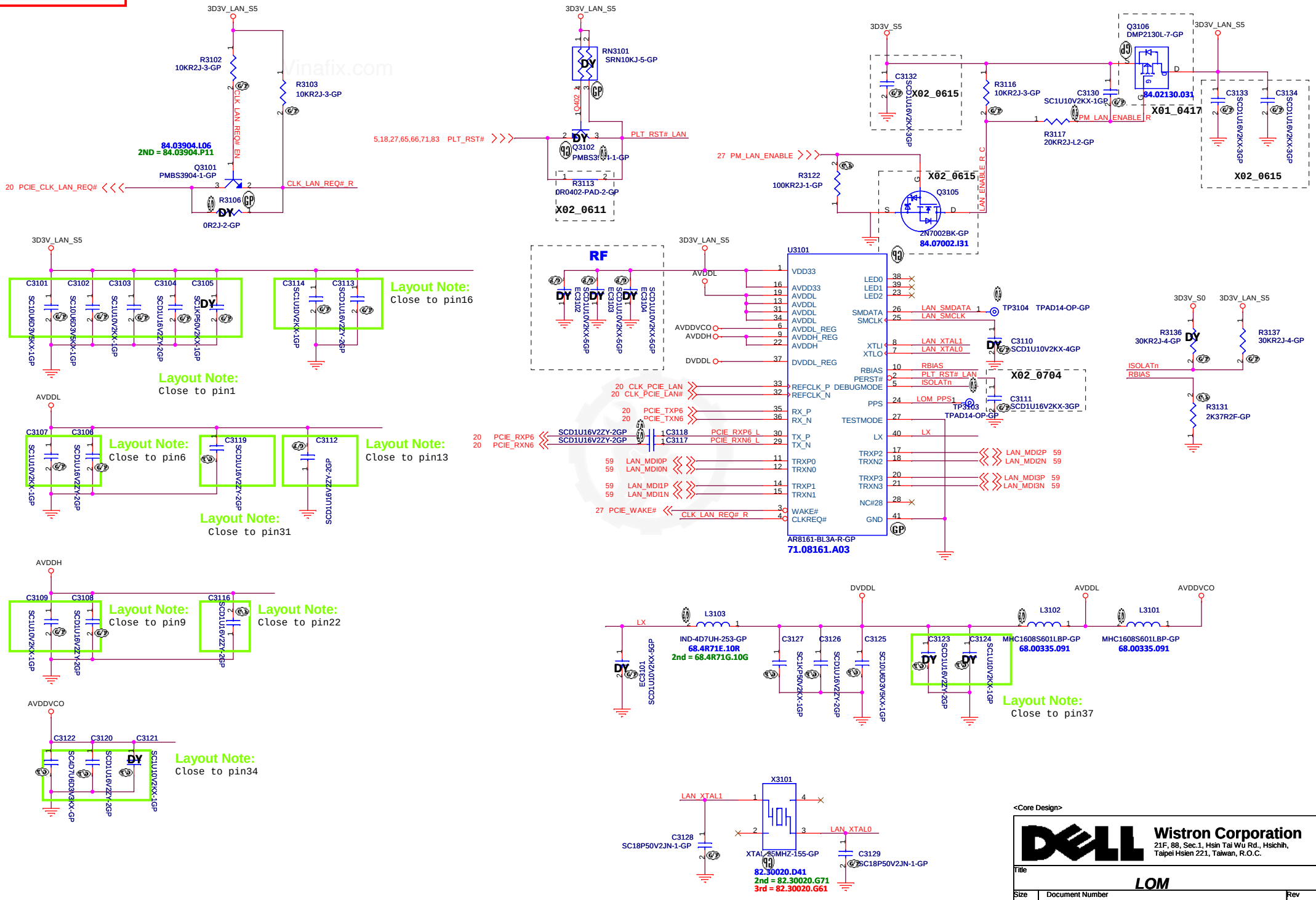
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *BMW Z5 DIS* | Rev: *A00*

Date: Tuesday, August 14, 2012 | Sheet 30 of 106

SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM		
Size: A3	Document Number: BMW Z5 DIS	Rev: A00
Date: Tuesday, August 14, 2012	Sheet 31 of 106	

(Blanking)

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

Date: Tuesday, August 14, 2012 Sheet 33 of 106

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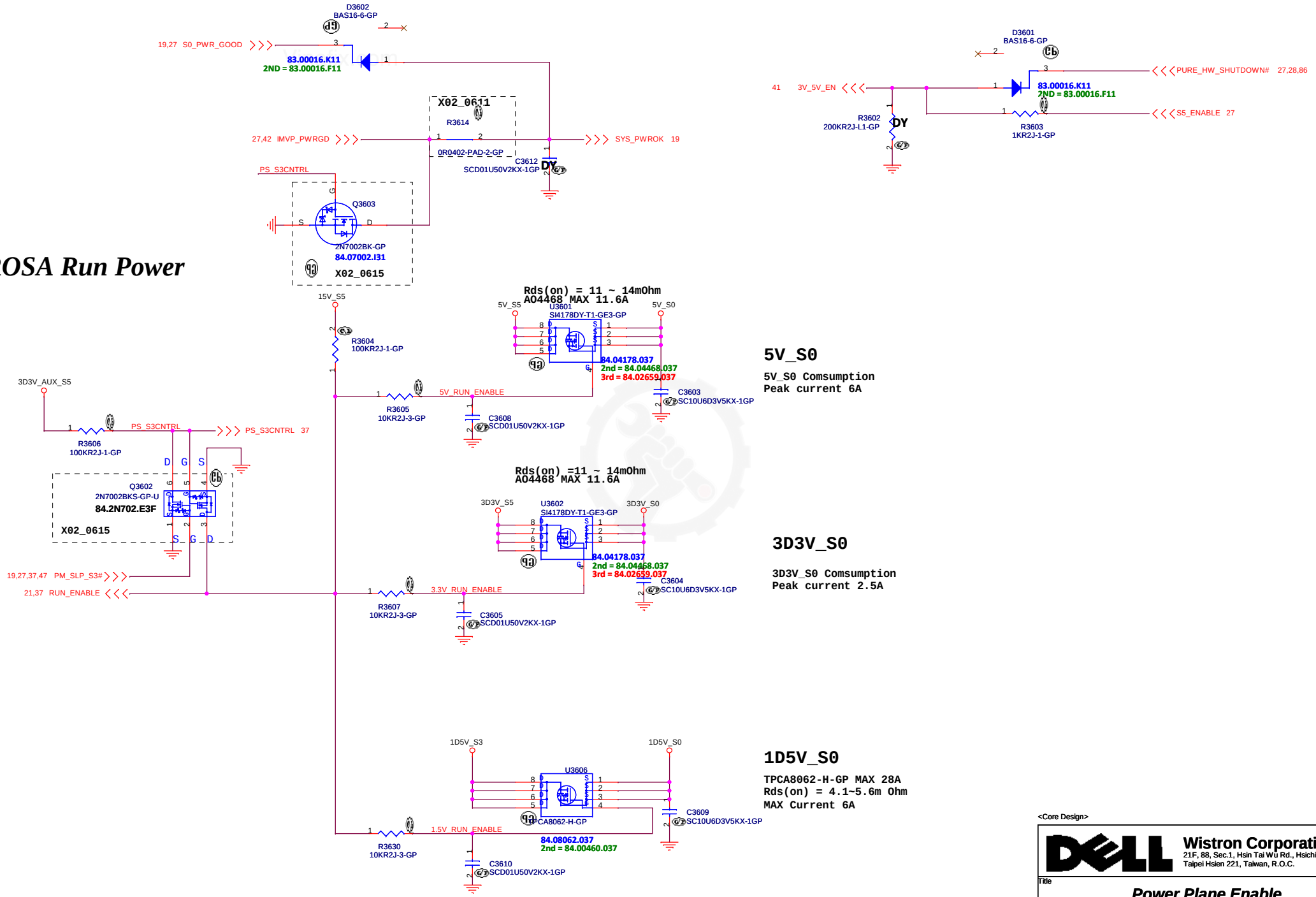
(Blanking)

SSID = Reset.Suspend

ROSA Run Power



5V_S0

5V_S0 Comsumption
Peak current 6A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

1D5V_S0

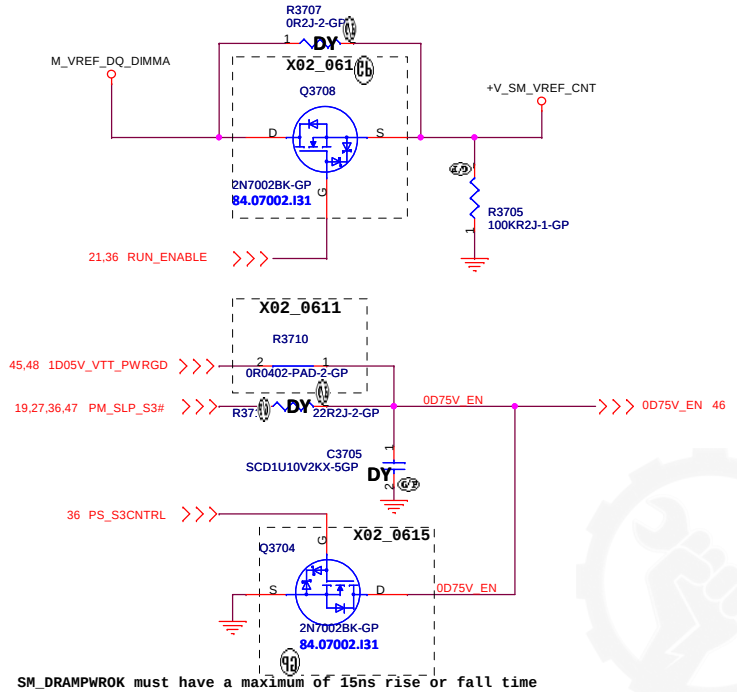
TPCA8062-H-GP MAX 28A
Rds(on) = 4.1~5.6m Ohm
MAX Current 6A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

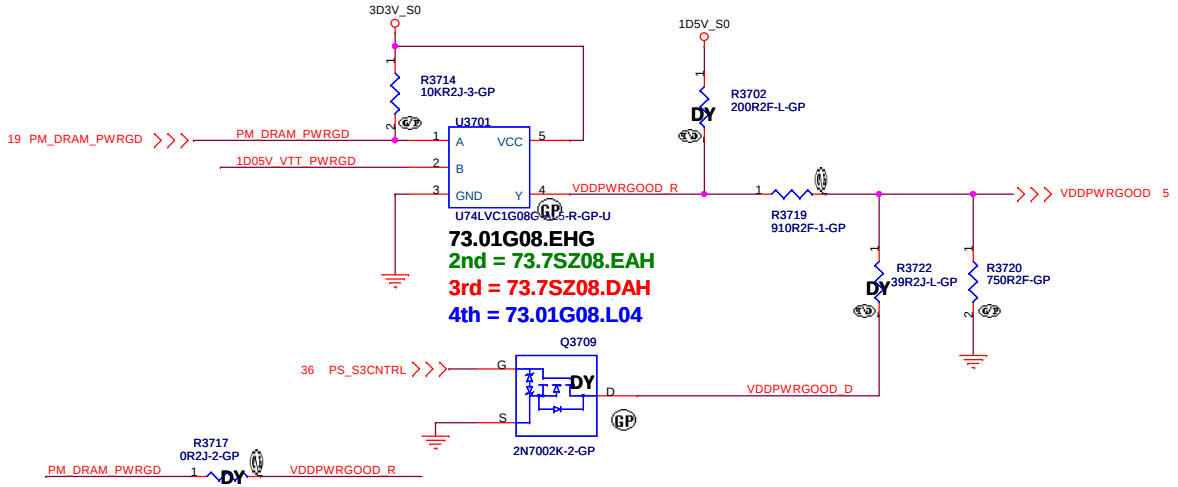
Title	Power Plane Enable	
Size A3	Document Number BMW Z5 DIS	Rev A00
Date: Tuesday, August 14, 2012	Sheet 36 of 106	

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

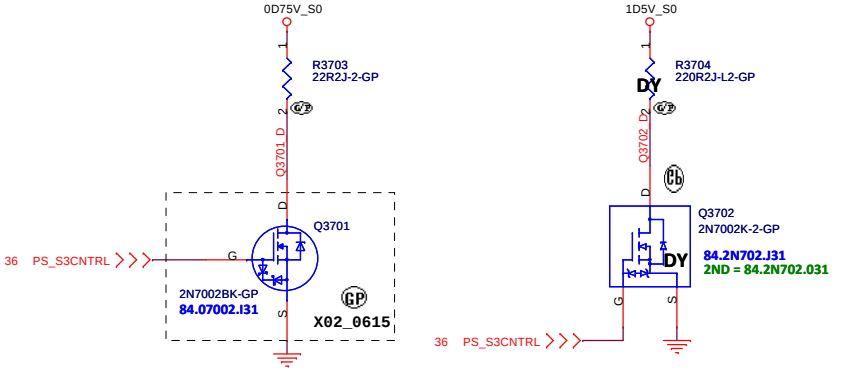


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

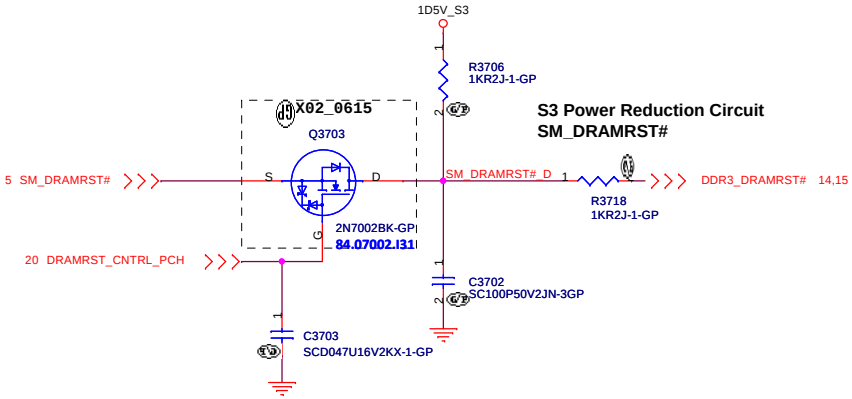
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMRST#



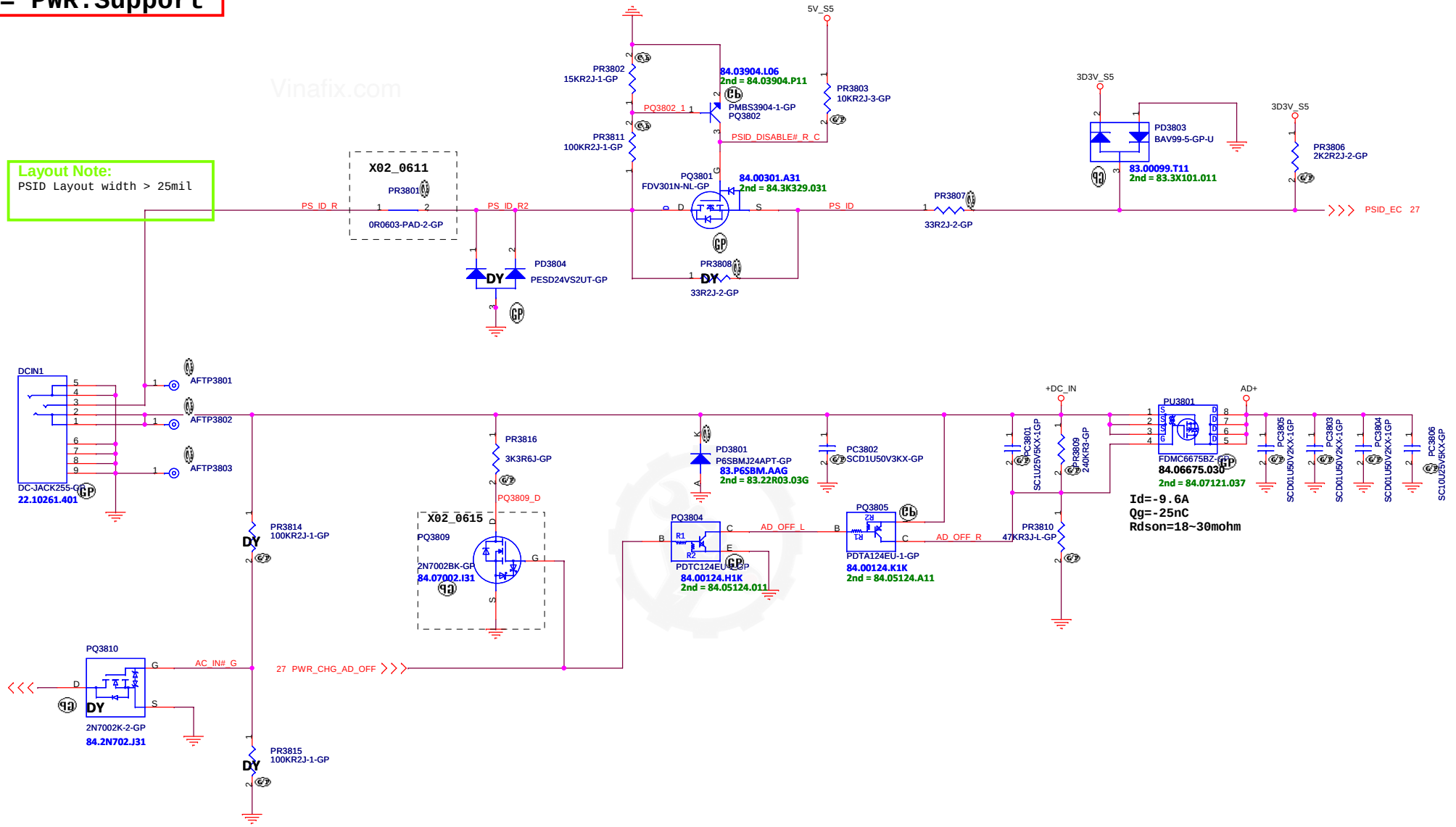
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S3 Power Reduction***		
Size: A3	Document Number: ***BMW Z5 DIS***	Rev: ***A00***
Date: Tuesday, August 14, 2012	Sheet 37 of 106	

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size A3	Document Number BMW Z5 DIS	Rev A00
Date: Tuesday, August 14, 2012	Sheet 38 of 106	

SSID = PWR.Support

A00_0806

EG3915 GAP-CLOSE-PWR-GP
EG3914 GAP-CLOSE-PWR-GP
EG3910 GAP-CLOSE-PWR-GP
EG3911 GAP-CLOSE-PWR-GP
EG3912 GAP-CLOSE-PWR-GP
EG3913 GAP-CLOSE-PWR-GP

BT+ BT+_G BT+_G

C3901 SC2200P50V2KX-2GP

PD3903 1SMA18AT3G-GP

Batt CONN

BATT1 SYN-CON9-24-GP

20.81755.009
2nd = 20.81771.009

27,40 BAT_SCL
27,40 BAT_SDA
27 BAT_IN#

R3902 100R2J-2-GP
R3903 100R2J-2-GP
R3904 100R2J-2-GP

PBAT_SMBCLK1
PBAT_SMBDAT1
PBAT_PRES1#
SYS_PRES1#

EC3901 SC10P50V2JN-4GP
EC3902 SC10P50V2JN-4GP

X01_0330

Avoiding MB crack on assembling

R3901 0R2J-2-GP

SYS_PRES1#
SYS_PRES1#

BATSW1 SW-SLIDE77-GP

62.40068.021
2nd = 62.40018.641

AFTP3902 PBAT_PRES1#
AFTP3903 PBAT_SMBDAT1
AFTP3904 PBAT_SMBCLK1
AFTP3905 BT+_G

BAT_IN#
BAT_SDA
BAT_SCL

D3902 BAV99-5-GP-U
D3903 BAV99-5-GP-U
D3901 BAV99-5-GP-U

83.00099.T11
2nd = 83.00099.K11
3rd = 83.BAV99.D11

3D3V_AUX_KBC

Layout Note:
Place near Battery CONN

<Core Design>

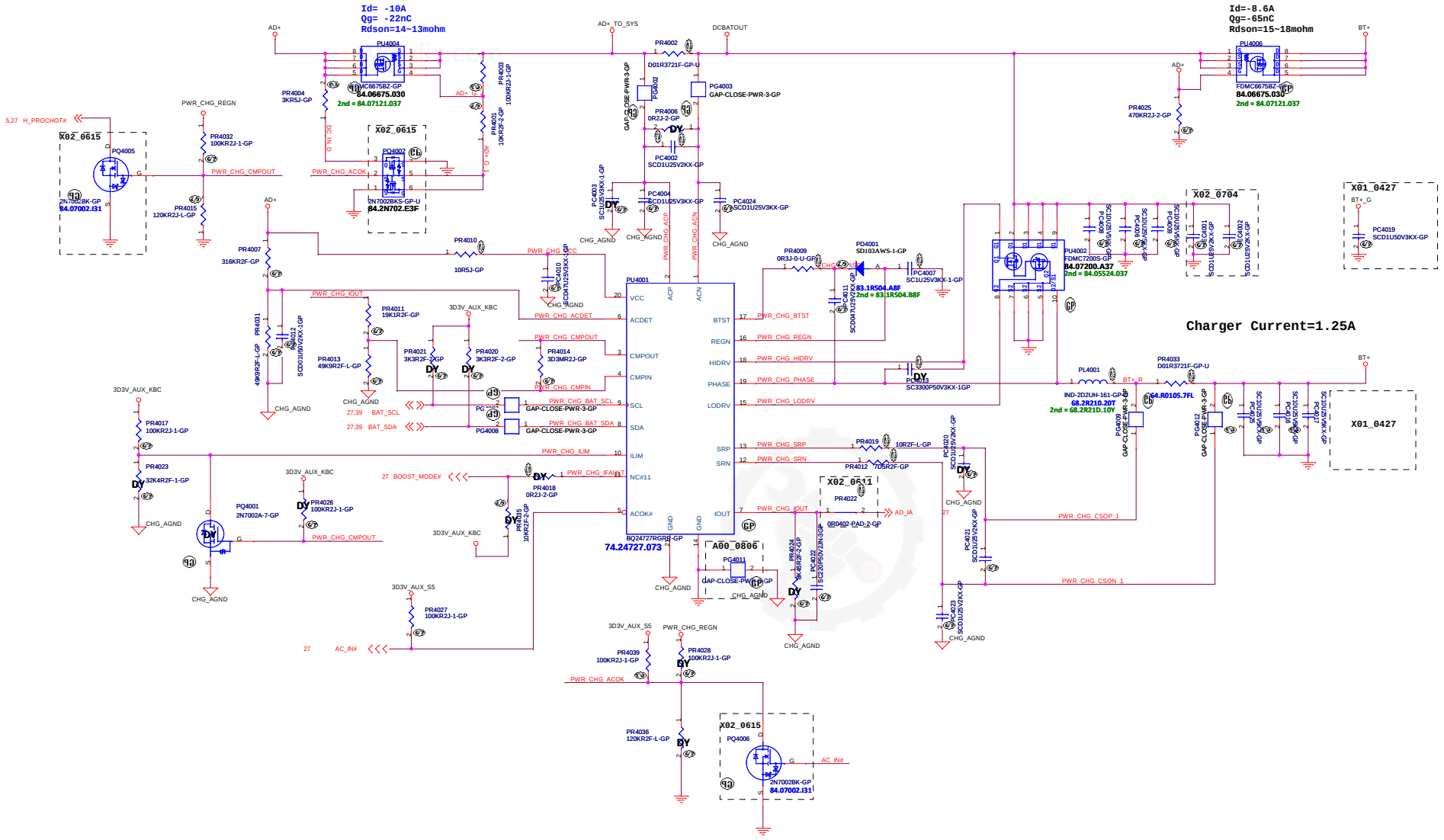
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 39 of 106

SSID = Charger



EC Code only BQ24707A

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

<Core Design>

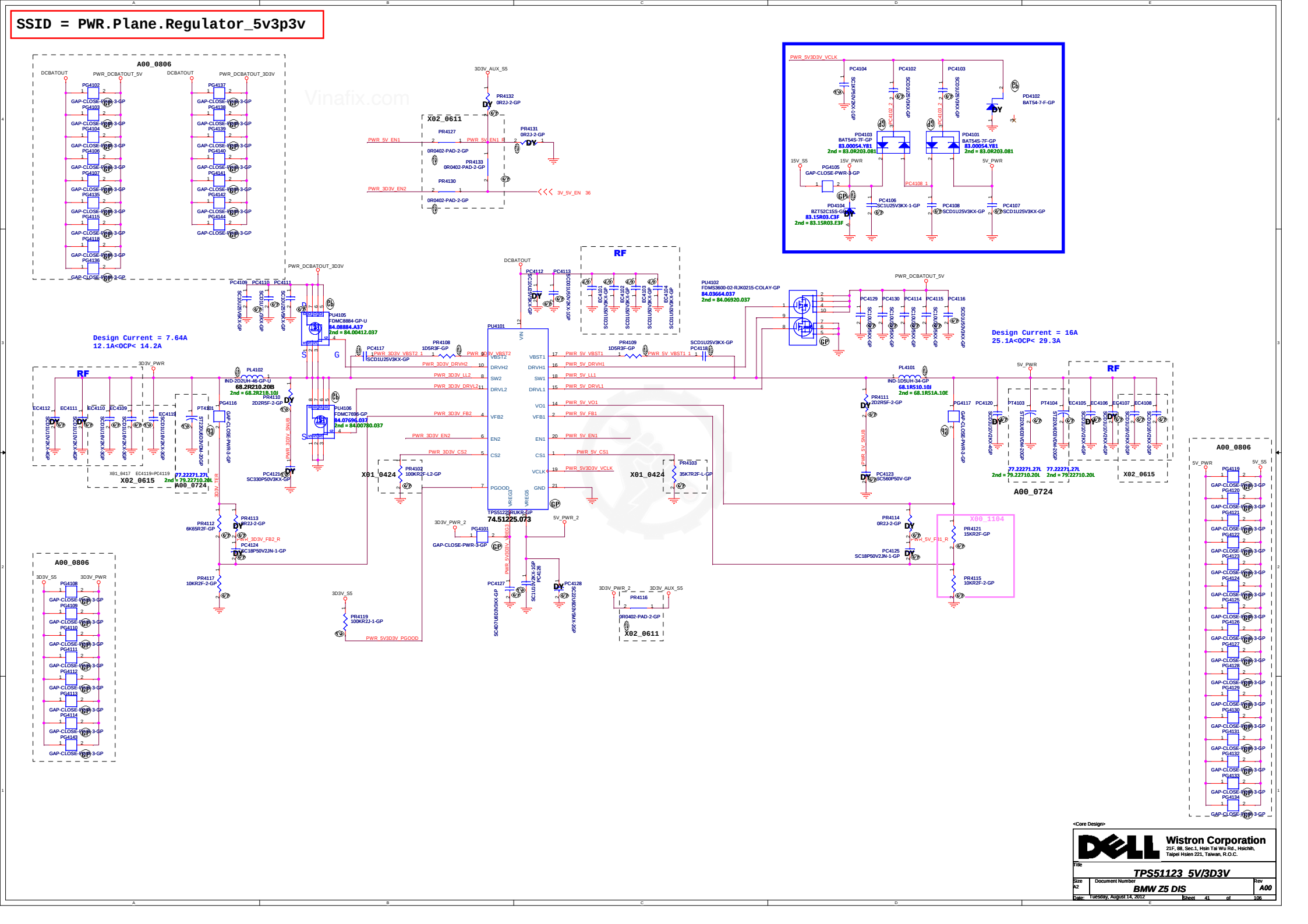
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size: A2 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 40 of 106

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123 5V/3D3V

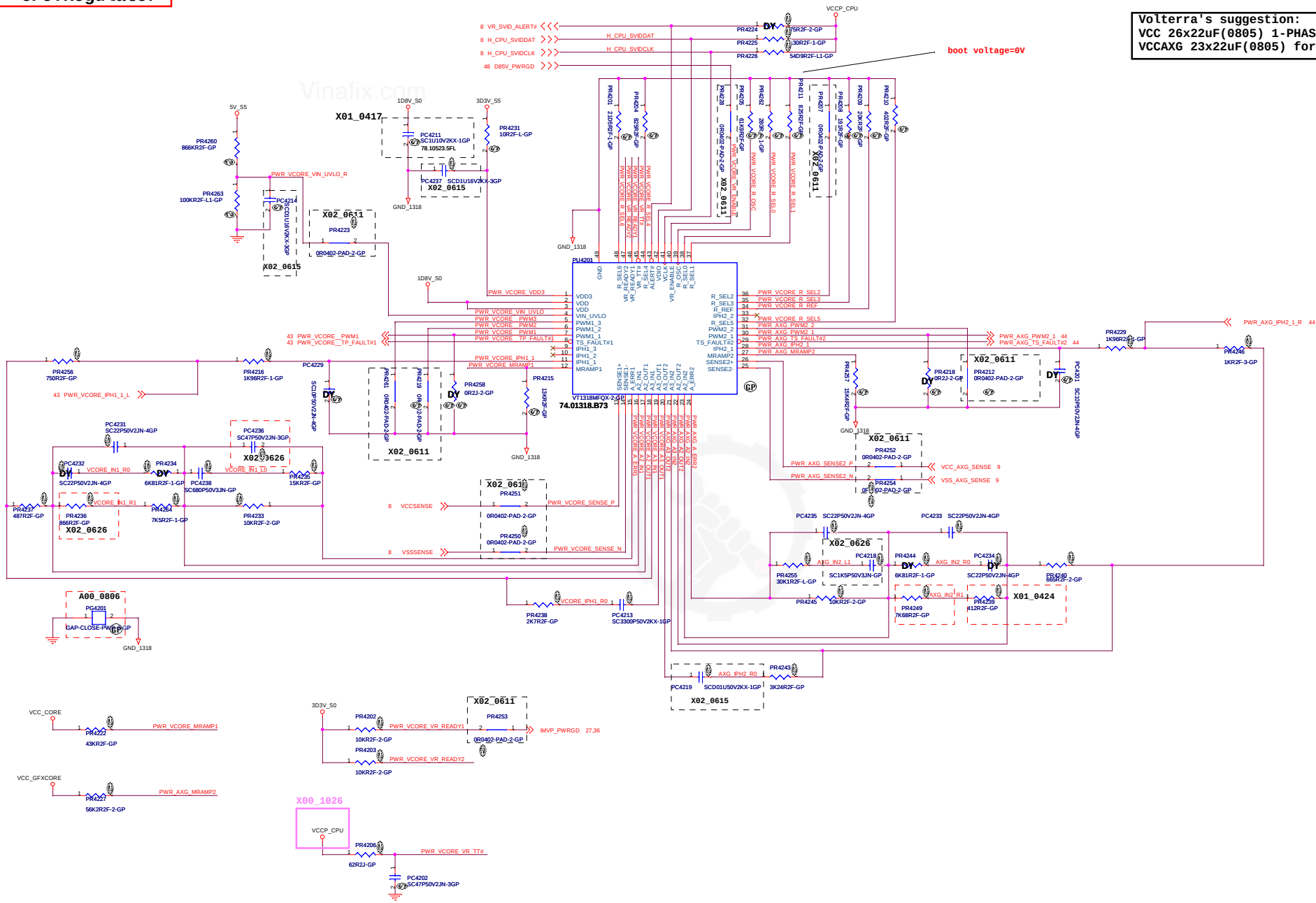
Size: A2 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 41 of 106

SSID = CPU.Regulator

Volterra's suggestion:
VCC 26x22uF(0805) 1-PHASE VCC
VCCAXG 23x22uF(0805) for 1-PHASE VCCAXG

boot voltage=0V



<Core Design>

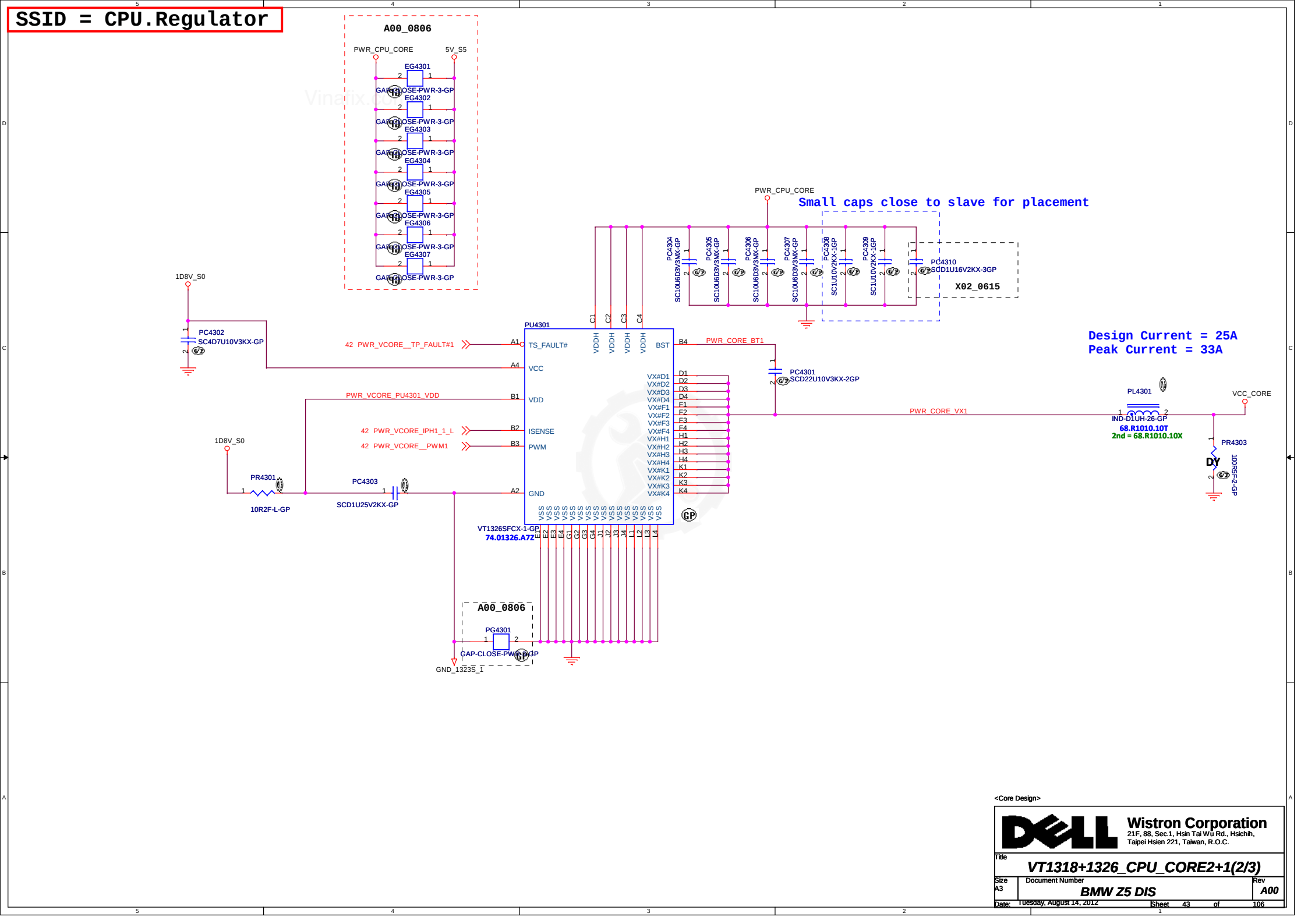
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VT1318+1323_CPU_CORE1+1(1/3)*

Size: A2 | Document Number: *BMW Z5 DIS* | Rev: *A00*

Date: Tuesday, August 14, 2012 | Sheet 42 of 106

SSID = CPU.Regulator

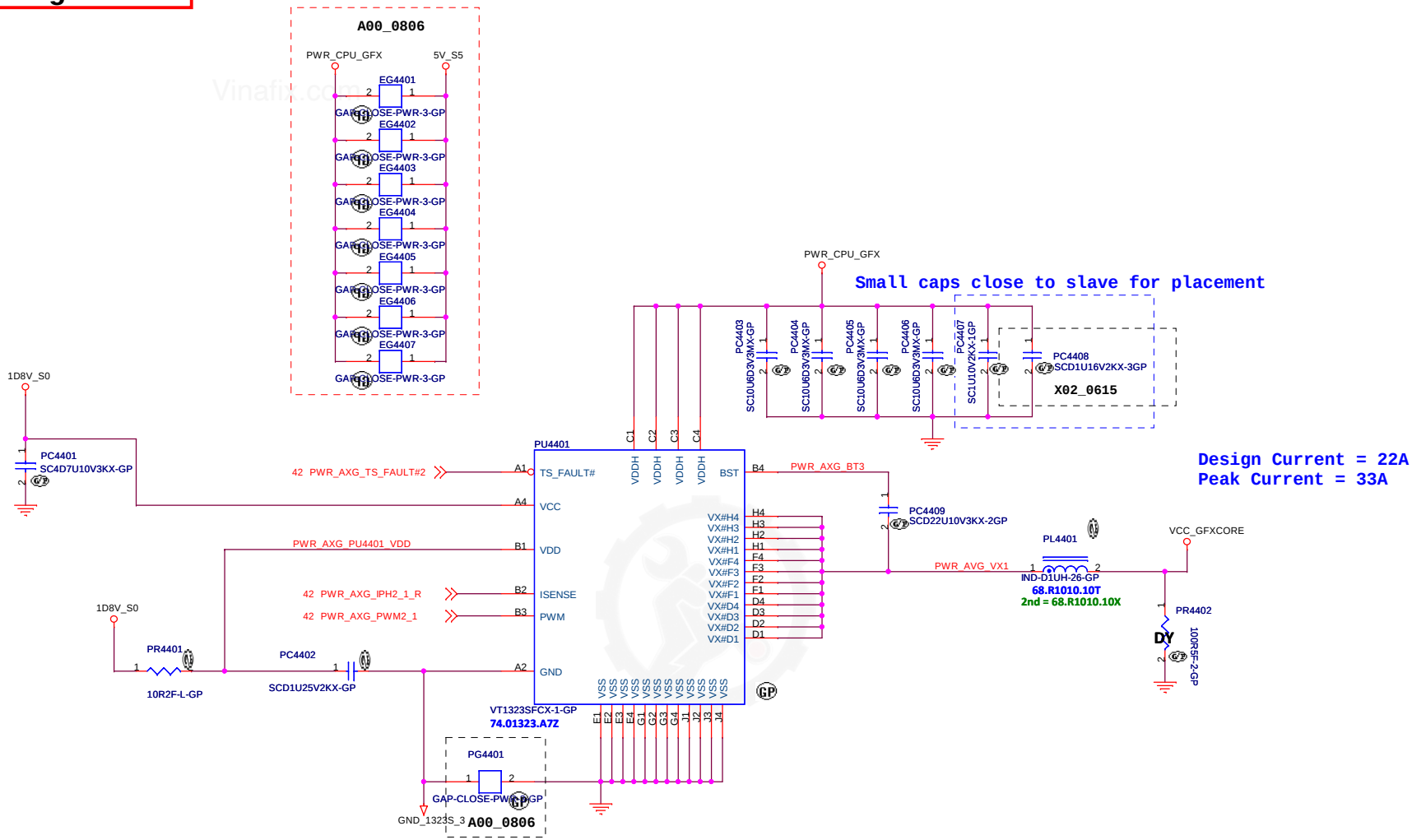


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VT1318+1326_CPU_CORE2+1(2/3)	
Size A3	Document Number BMW Z5 DIS	Rev A00
Date: Tuesday, August 14, 2012	Sheet 43 of 106	

SSID = CPU.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VT1318+1323_CPU_CORE1+1(3/3)	
Size A3	Document Number BMW Z5 DIS	Rev A00
Date: Tuesday, August 14, 2012	Sheet 44 of 106	

SSID = PWR.Plane.Regulator_1p05v

140mils or Copper Shape

A00_0806

5V_S5 +PWR_SRC_1D05V

EG4527 EG4528 EG4525 EG4522

GAP-CLOSE-PWR-GP

3D3V_S0

PR4518 10KR2J-3-GP

PWR_1D05V_STAT

X02_0611 PR4523 0R0402-PAD-2-GP

1D05V_VTT_PWRGD 37,48

DY PC4531 SC2200P50V2KX-2GP

A00_0806 1D05VTT_PWR VCCP_CPU

PG4506 PG4507 PG4510 PG4512 PG4516 PG4519

A00_0806 1D05VTT_PWR VCCP_CPU

PG4513 PG4508 PG4509 PG4514 PG4515 PG4511 PG4517 PG4518 PG4520

Design Current = 10.67A

16.77A<OCP< 19.82A

+PWR_SRC_1D05V

PC4508 SC22U6D3V5MX-2GP DY

PC4507 SC22U6D3V5MX-2GP

PC4514 SC4D7U6V3KX-GP

PC4515 SCD1U16V2KX-3GP

X02_0615

X01_0418

PU4501

VDD VDD SENSE+ SENSE- STAT OE GND GND AGND

VX#B2 VX#B3 VX#B4 VX#C2 VX#C3 VX#C4

VT386FCX-ADJ-GP

74.00386.03Z

Diff pair

PWR_1D05V_VSENSE+

PWR_1D05V_VSENSE-

PWR_1D05V_STAT

PU4501_OE

19,46,47,93 RUNPWROK

PR4506 2K74R2F-GP

PR4507 6K81R2F-1-GP

X02_0611 PR4522 0R0402-PAD-2-GP

PC4539 SCD1U10V2KX-4GP DY

PR4515 150R2F-1-GP DY

PC4502 SC3300P50V2KX-1GP

PC4501 SC4700P50V2KX-1GP

VCCIO_SENSE_1

A00_0806 PG4505 GAP-CLOSE-PWR-GP

AGND_1D05V_385

PL4501 COIL-D2UH-2-GP

68.R2010.20B

2nd = 68.R2010.10Q

PR4501 25K5R2F-GP

400mils or Copper Shape

1D05VTT_PWR

PC4518 PC4519 PC4521 PC4528 PC4530 PC4529 PC4522 SC22U6D3V5MX-2GP

SCD1U10V2KX-5GP

SCD1U10V2KX-5GP RF

X02_0615

VCCP_CPU

X02_0615 PC4506 SCD1U16V2KX-3GP

PC4523 PC4509 PC4510 PC4511 PC4512 PC4513 PC4516 PC4517 PC4525 PC4520 PC4526 PC4527 SC22U6D3V5MX-2GP

22u Cap x 18

0.1 u Cap x 2

close output MLCC

VCCIO_SENSE_C

PR4510 0R0402-PAD-2-GP VCCIO_SENSE 8

PR4511 0R0402-PAD-2-GP VSSIO_SENSE 8

X02_0611

close output MLCC

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

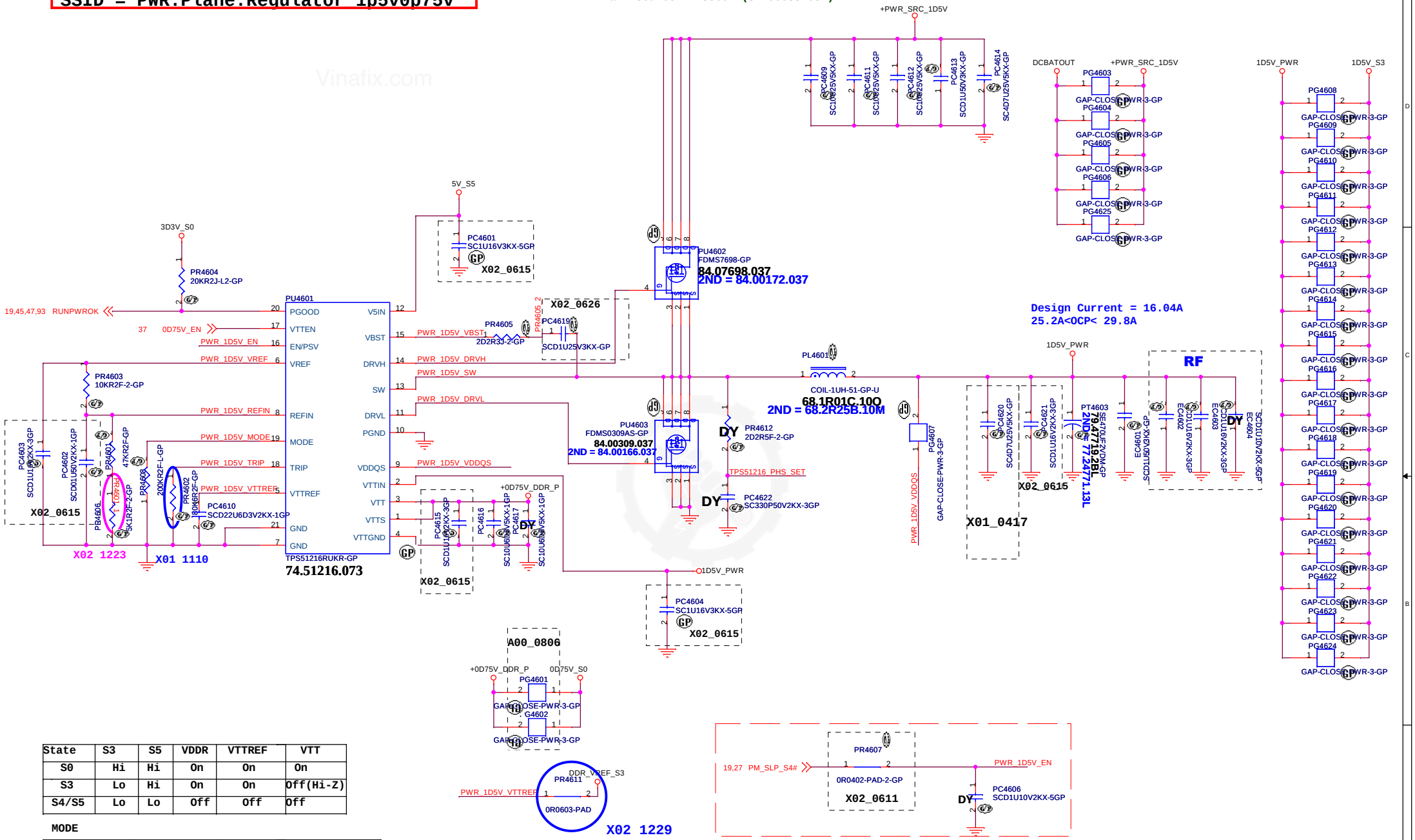
Title: 1D05V_PCH & VCCP_CPU

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 45 of 106

SSID = PWR.Plane.Regulator_1p5v0p75v

PU4602
Main source FDMS3604 (84.00033.037)



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M Cyntec 3mohm/3.3mohm Isat =28Arms68.1R01C.10Q
O/P cap: CHIP CAP 470UF 2V EEFSX0D471X 6mOhm 3.5Arm/Panasonic/79.47719.2BL
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

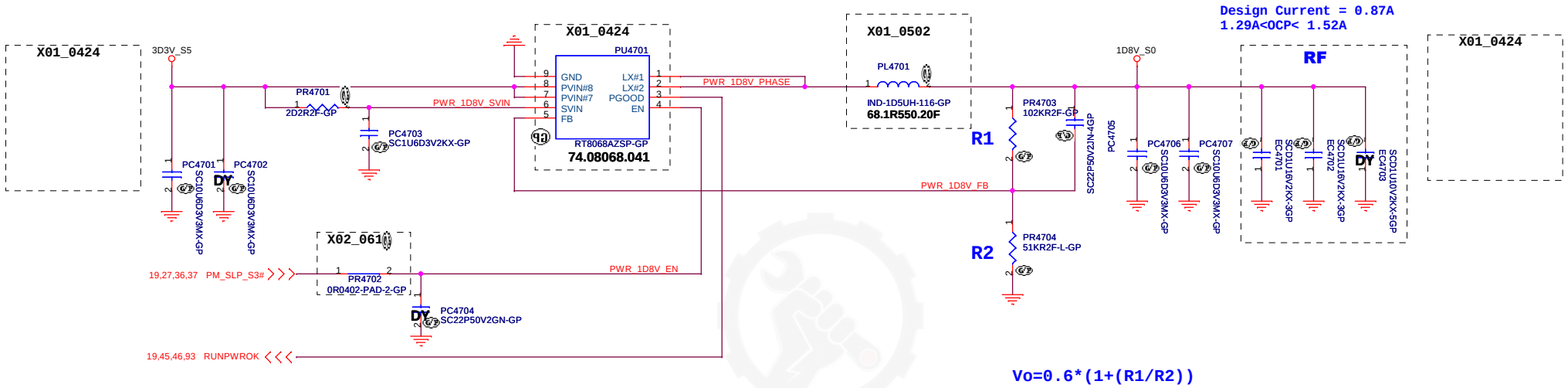
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.5V_SUS
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: A00
Date: Tuesday, August 14, 2012
Sheet 46 of 106

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

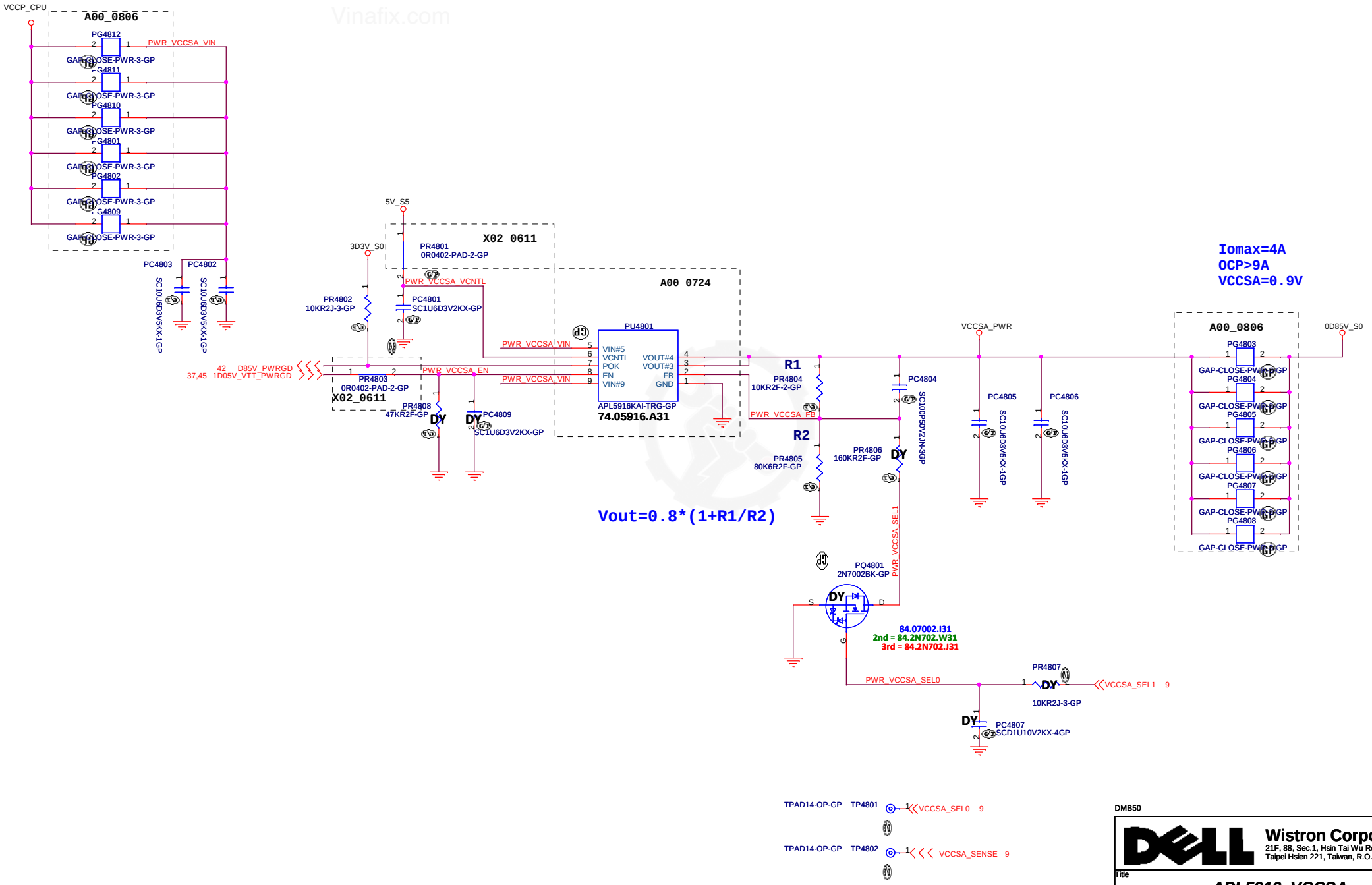


DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT8068A_1D8V_S0*	
Size A3	Document Number BMW Z5 DIS	Rev *A00*
Date: Tuesday, August 14, 2012	Sheet 47 of 106	

SSID = PWR.Plane.Regulator_vccsa



DMB50

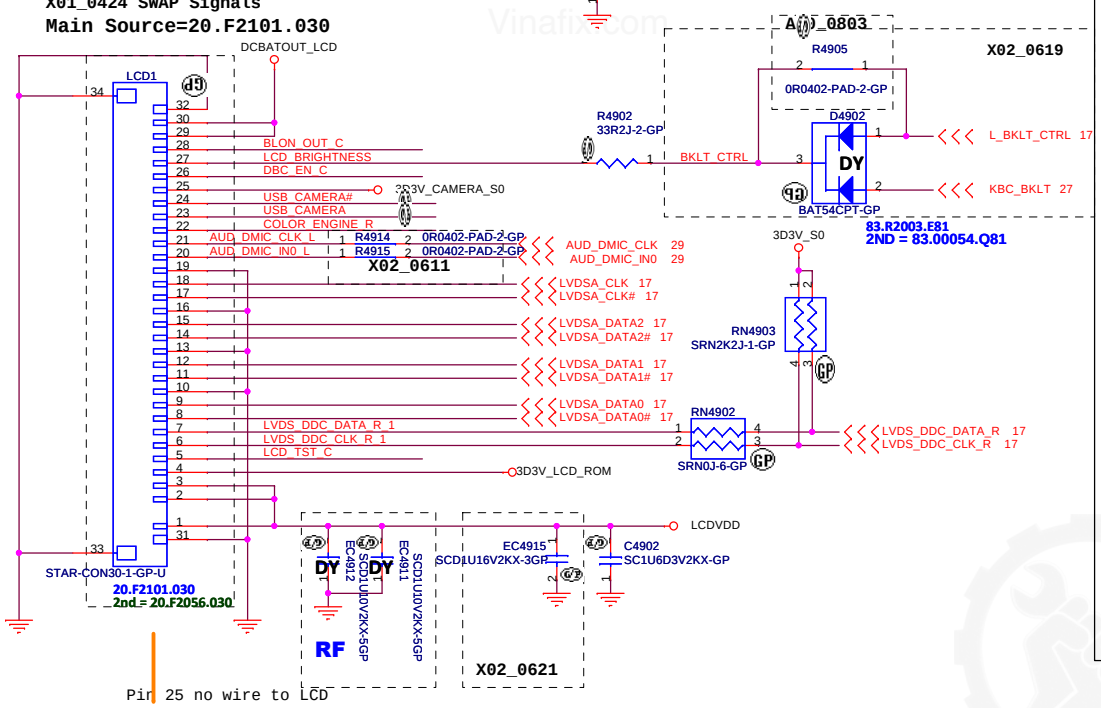
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*APL5916_VCCSA*	
Size A3	Document Number *BMW Z5 DIS*	Rev *A00*
Date: Tuesday, August 14, 2012	Sheet 48 of 106	

SSID = VIDEO

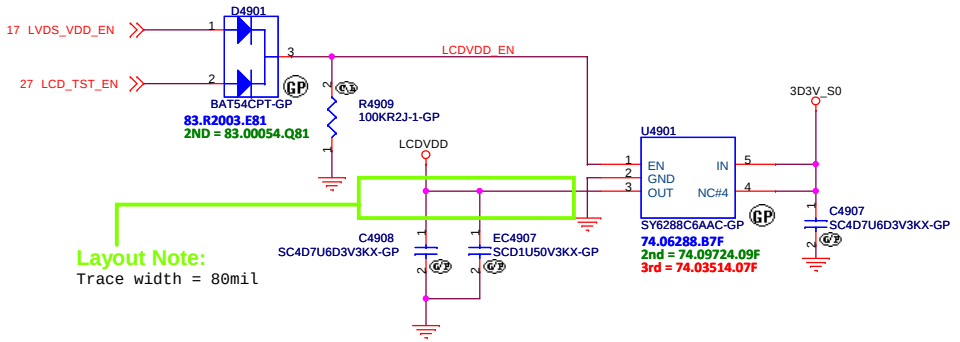
LVDS CONN

X01_0417
X01_0424 SWAP Signals
Main Source=20.F2101.030

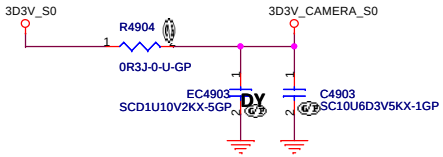


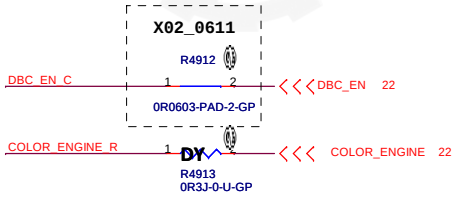
SSID = VIDEO

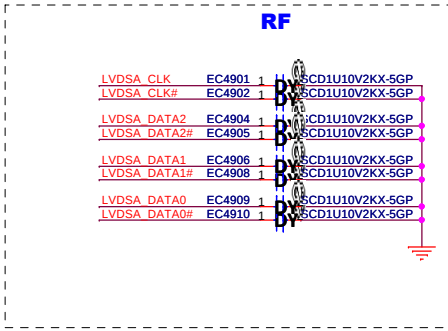
LCD Power for ROSA

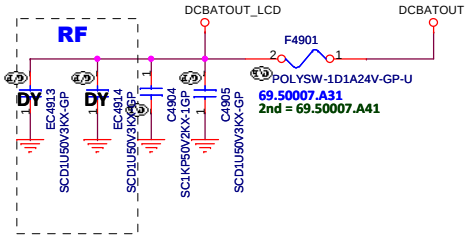


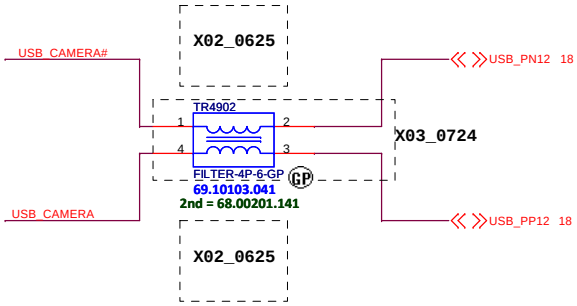
Camera Power











DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector	
Size A3	Document Number BMW Z5 DIS	Rev A00
Date: Tuesday, August 14, 2012	Sheet 49 of 106	

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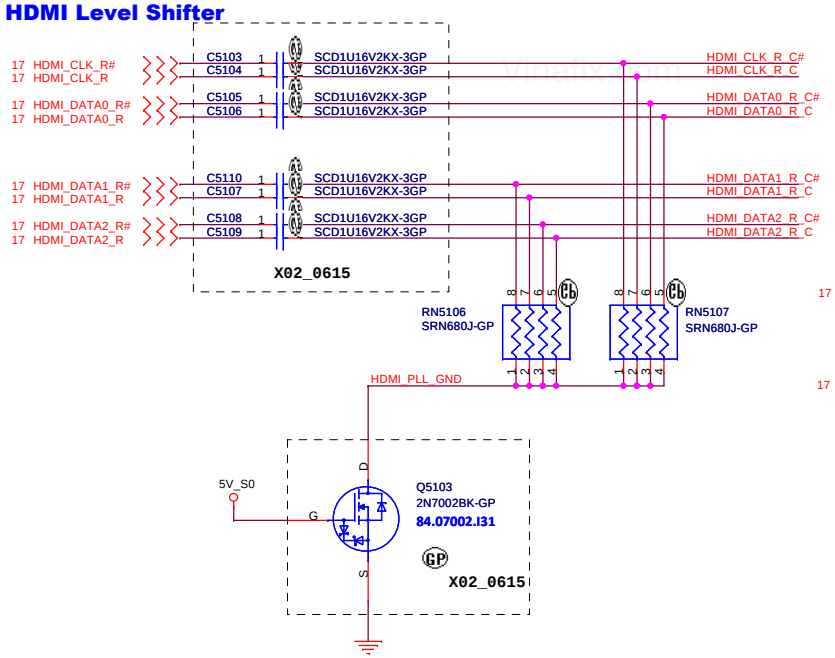
DMB50

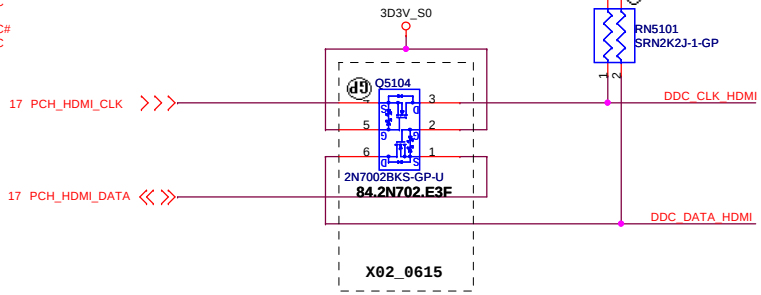
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

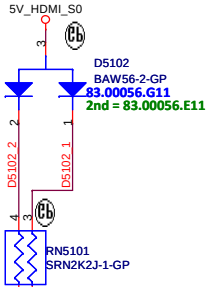
Title: CRT Connector		
Size: A3	Document Number: BMW Z5 DIS	Rev: A00
Date: Tuesday, August 14, 2012	Sheet 50 of 106	

SSID = VIDEO

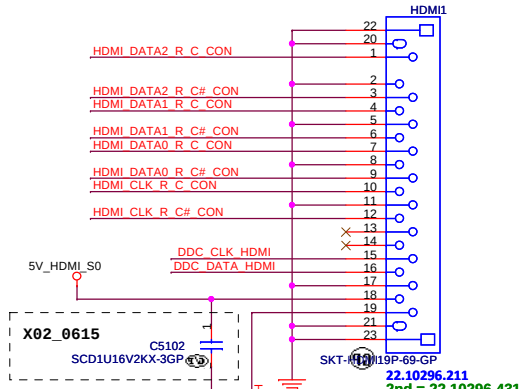
HDMI Level Shifter

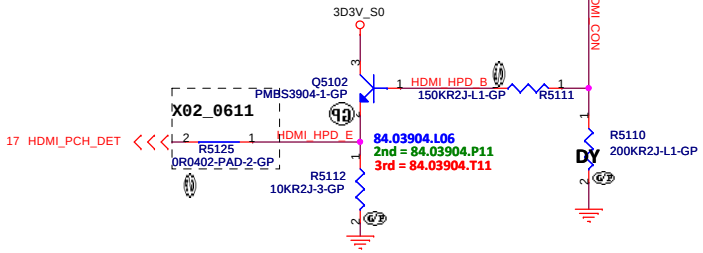


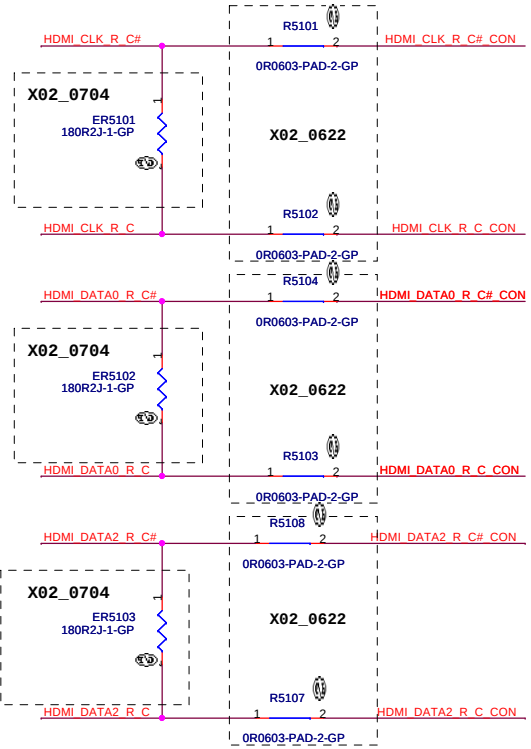


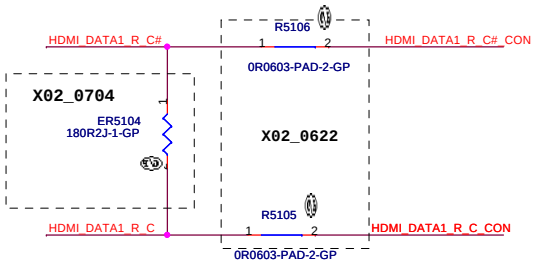


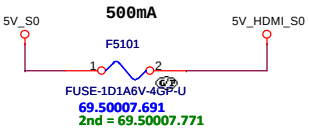
HDMI CONN











DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z5 DIS* | Rev: *A00*

Date: Tuesday, August 14, 2012 | Sheet 52 of 106

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

Date: Tuesday, August 14, 2012 Sheet 53 of 106

(Blanking)

DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

Date: Tuesday, August 14, 2012 Sheet 54 of 106

(Blanking)

DMB50

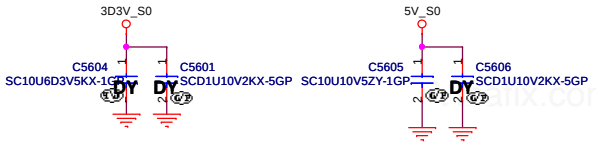
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

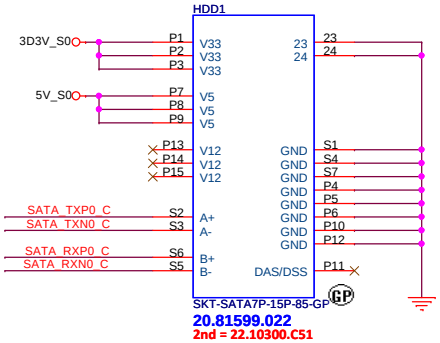
Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 55 of 106

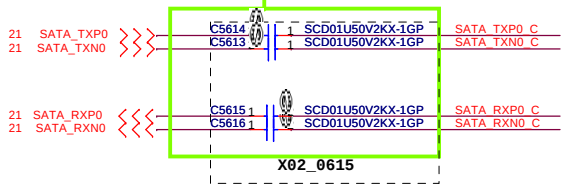
SSID = SATA



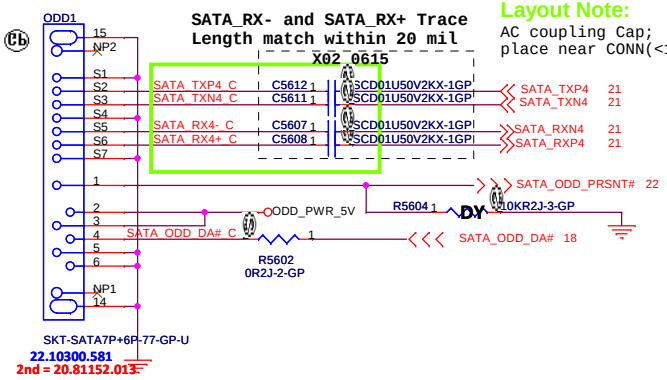
HDD CONN



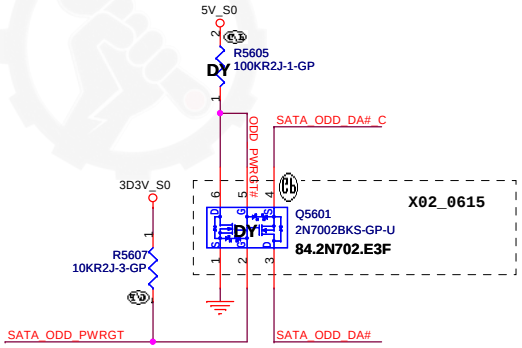
Layout Note:
AC coupling Cap;
place near CONN(<100mils)



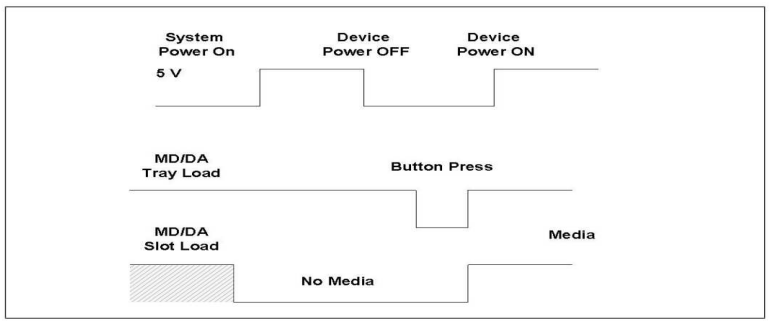
ODD CONN

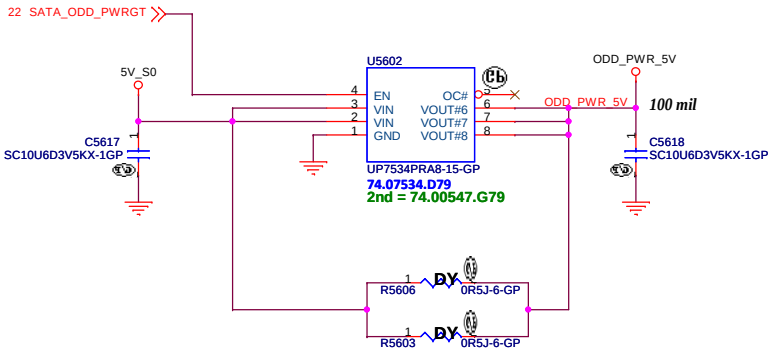


Layout Note:
AC coupling Cap;
place near CONN(<100mils)



Zero Power ODD Power Sequence





DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

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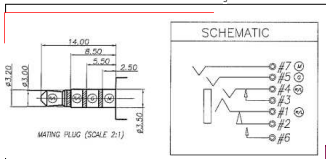
DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

Date: Tuesday, August 14, 2012 Sheet 57 of 106



Speaker

X01_0417

SPK1

ACES-CON4-29-GP

20.F1639.004

2ND = 20.F1804.004

AUD_SPK_L- C

AUD_SPK_L+ C

AUD_SPK_R- C

AUD_SPK_R+ C

SC1KP50V2KX-1GP EC5809

SC1KP50V2KX-1GP EC5808

SC1KP50V2KX-1GP EC5807

SC1KP50V2KX-1GP EC5810

DY

X02_0622

R5801 0R0603-PAD-2-GP

R5802 0R0603-PAD-2-GP

R5803 0R0603-PAD-2-GP

R5804 0R0603-PAD-2-GP

AUD_SPK_L- 29

AUD_SPK_L+ 29

AUD_SPK_R- 29

AUD_SPK_R+ 29

Layout Note:
trace width=30mil

AFTP5801 AUD_SPK_L- C

AFTP5802 AUD_SPK_L+ C

AFTP5803 AUD_SPK_R- C

AFTP5804 AUD_SPK_R+ C

Combo Jack

HPMIC1

PHONE-JK509-GP

22.10270.171

2ND = 22.10270.P11

RING2

AUD_HP1_JACK_L1

AUD_HP1_JD# 29

AUD_HP1_JACK_R1

SLEEVE

BLM18BD601SN1D-GP L5801

BLM18BD601SN1D-GP L5802

AUD_HP1_JACK_L

AUD_HP1_JACK_L 29

AUD_HP1_JACK_R

AUD_HP1_JACK_R 29

EC5801

83.00402.0A0

2ND = 83.05125.0A0

TVL-0402-01-AB1-GP

X01_0417

AFTP5810

EC5802 SC1KP50V2KX-1GP

EC5804 SC1KP50V2KX-1GP

X02_0615

EC5803 SC1KP25V2KX-GP

EC5805 SC1KP25V2KX-GP

AFTP5805 SLEEVE

AFTP5806 RING2

AFTP5807 AUD_HP1_JACK_L1

AFTP5808 AUD_HP1_JACK_R1

AFTP5809 AUD_HP1_JD#

29 AUD_VREFOUT_A

AUD_VREFOUT_A

R5807 2K2R2J-2-GP

C5806 SC1U10V2KX-1GP

29 MIC_IN_R

MIC_IN_R

R5808 0R0402-PAD-2-GP

A00_0803

MIC_IN_R_C

Layout Note:
L5803 close to Jack

L5803 BLM18BD601SN1D-GP

MICP

C5809 SC100P50V2JN-3GP

C5811 SC220P50V2KX-3GP

3D3V_S0

RTC_AUX_S5

R5810 100KR2J-1-GP

R5809 10KR2J-3-GP

X02_0615 Q5803

2N7002BK-GP

84.07002.I31

SLEEVE

X02_0615 Q5802

2N7002BK-GP

84.07002.I31

3D3V_S0

C5801 SC1U6D3VM3X-GP

C5802 SC470U6D3VBX-GP

C5803 SCD1U25V2KX-3GP

C5804 SCD1U50V2KX-1GP

X02_0615

U5801

TS3A225ERTER-GP

73.03225.003

VDD

VDD

SCL

SDA

SLEEVE_SENSE

SLEEVE

TIP_SENSE

RING2_SENSE

RING2

MIC_PRESENT

DET_TRIGGER

ADDR_SEL

MICP

MICN

GND

GND

GND

MIC_SCL

MIC_SDA

SLEEVE

RING2

AUD_HP1_JACK_L1

R5805 10KR2J-3-GP

AUD_HP1_JD

EXT_MIC_JD# 29

MICP

C5805 SC33P50V2JN-3GP

EC5806 SCD1U10V6KX-3GP

29 AUD_HP1_JD#

AUD_HP1_JD#

Q5801 2N7002BK-GP

84.07002.I31

X02_0615

R5806 100KR2J-1-GP

AUD_HP1_JD

C5807 SCD1U10V2KX-4GP

3D3V_S0

RN5801 SRN2K2J-1-GP

MIC_SCL

MIC_SDA

DMB50

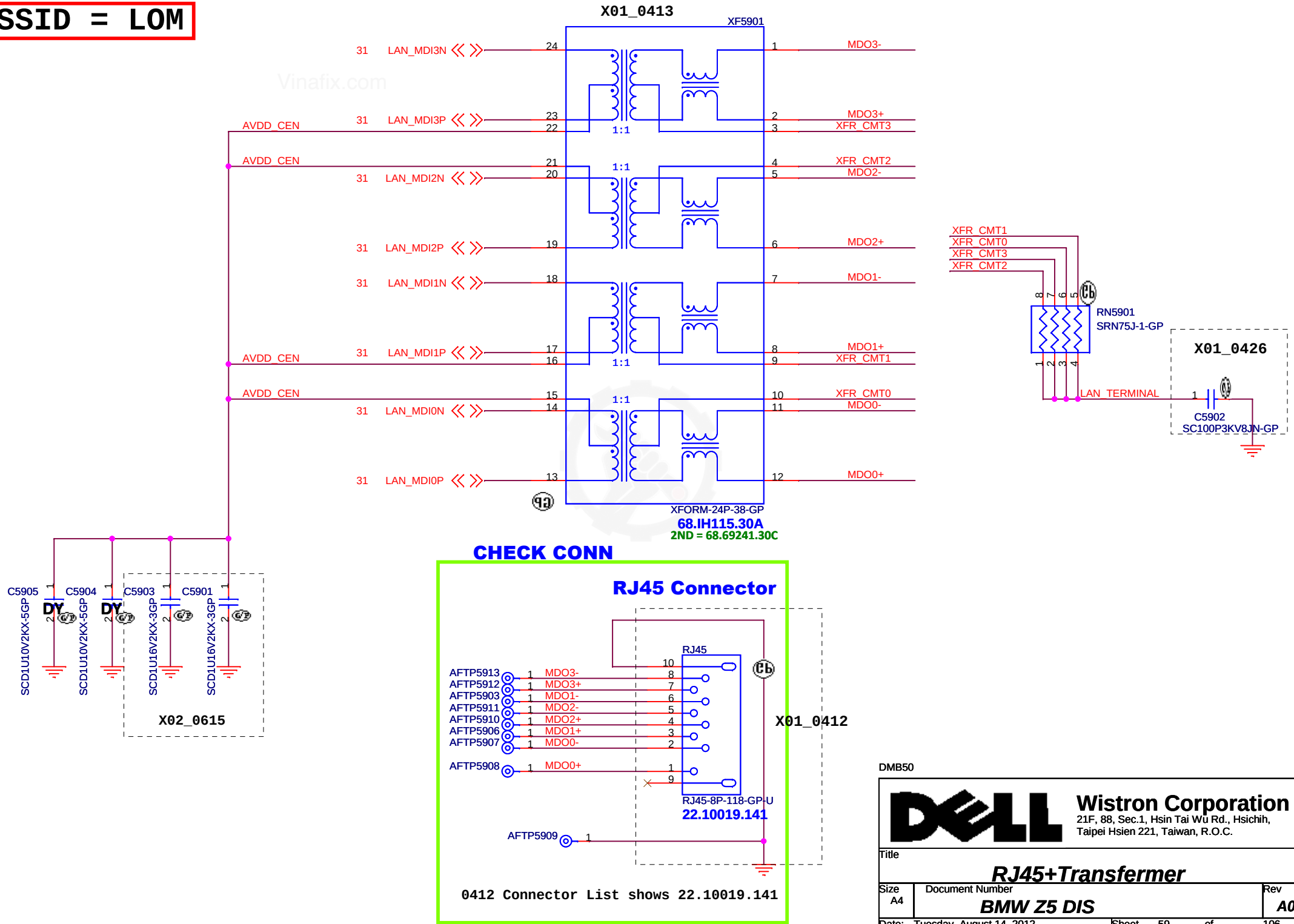
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size: A2 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 58 of 106

SSID = LOM



DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

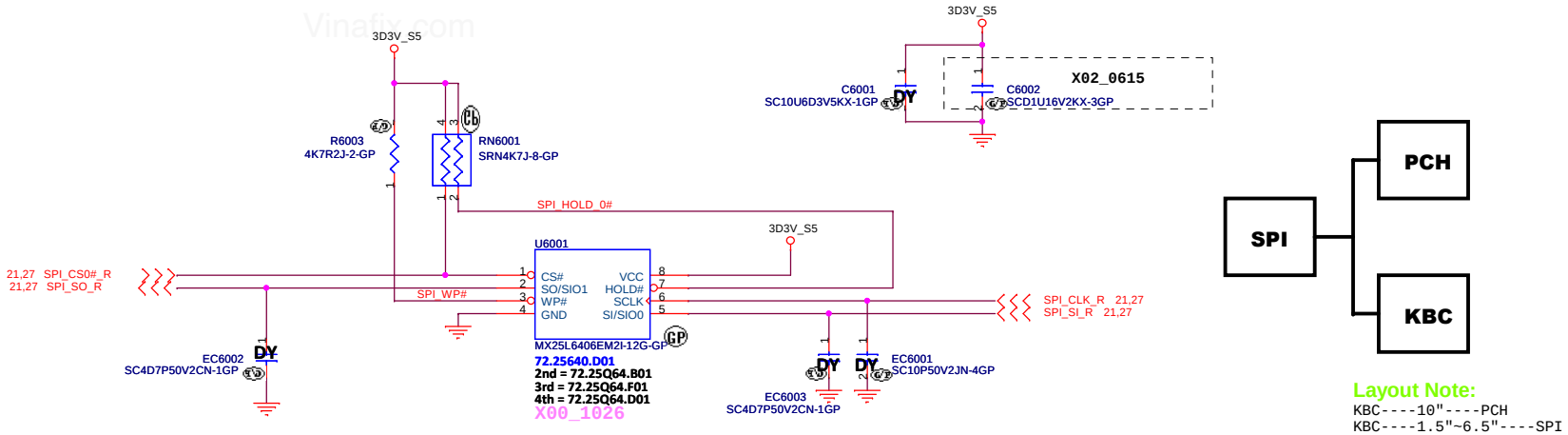
Title: ***RJ45+Transfermer***

Size	Document Number	Rev
A4	***BMW Z5 DIS***	***A00***

Date: Tuesday, August 14, 2012 Sheet 59 of 106

SSID = Flash.ROM

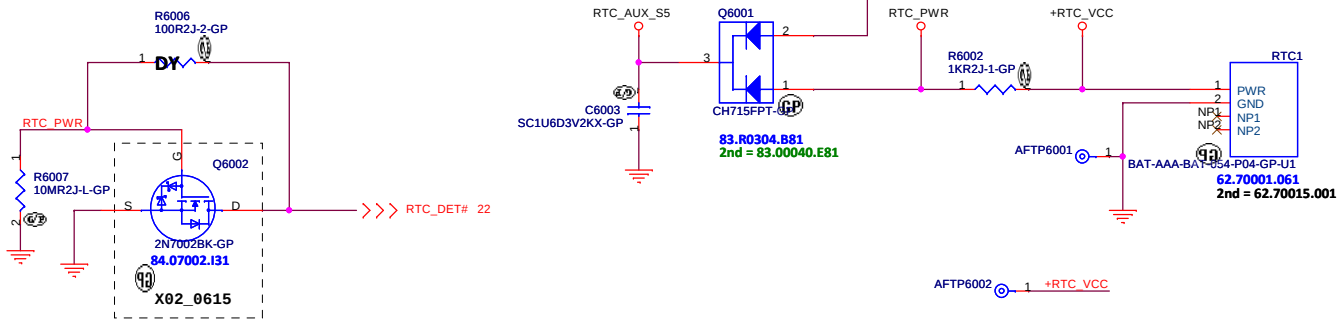
SPI Flash ROM(8M) for PCH



Layout Note:

KBC----10"----PCH
KBC----1.5"~6.5"----SPI
PCH----0.5"~6.5"----SPI

SSID = RBATT



DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Flash/RTC*		
Size: A3	Document Number: *BMW Z5 DIS*	Rev: *A00*
Date: Tuesday, August 14, 2012	Sheet 60 of 106	

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

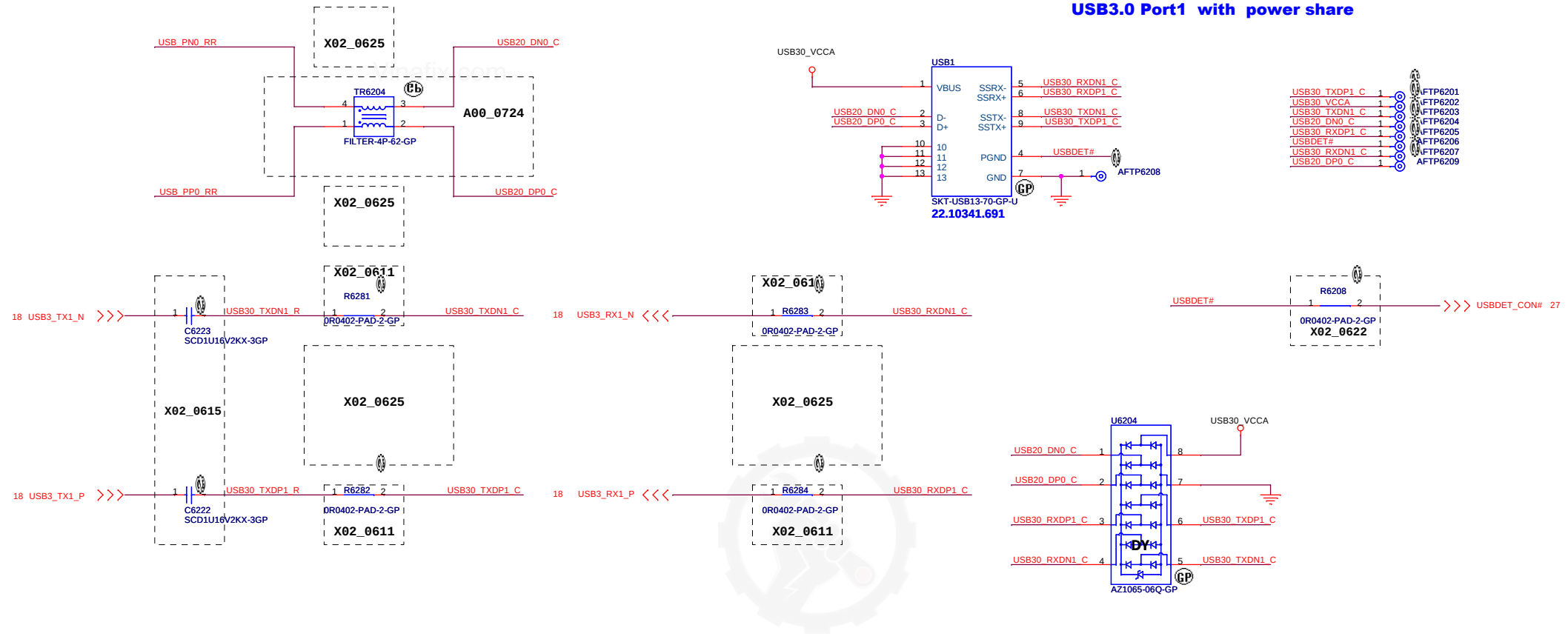
Title: ***Reserved***

Size	Document Number	Rev
	BMW Z5 DIS	***A00***

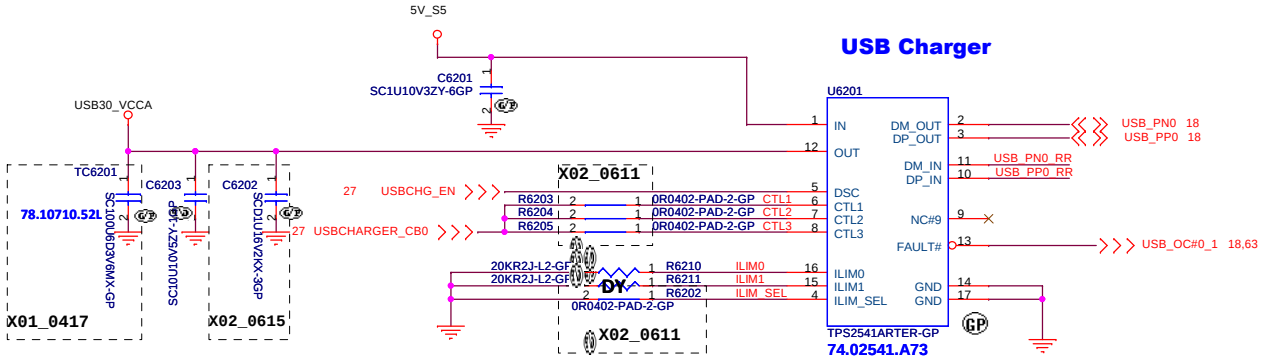
Date: Tuesday, August 14, 2012 Sheet 61 of 106

SSID = USB

USB3.0 Port1 with power share



USB Charger



TPS2541 charging type setting			
	CTL1	CTL2	CTL3
CDP	1	1	1
DCP	0	0	X

DMB50

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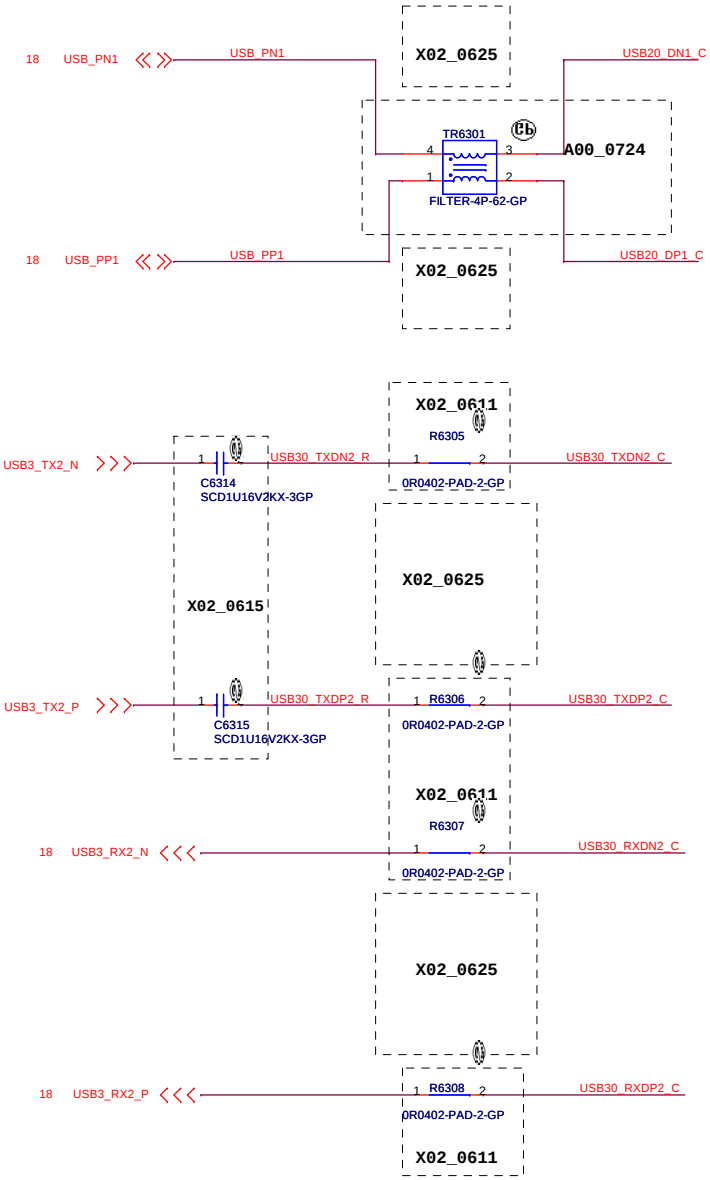
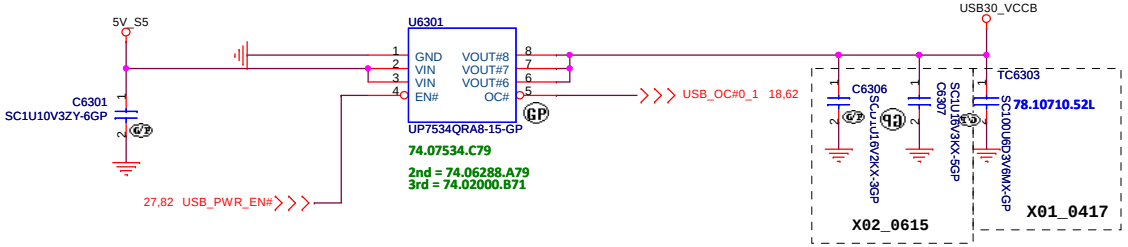
Title: USB 3.0

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

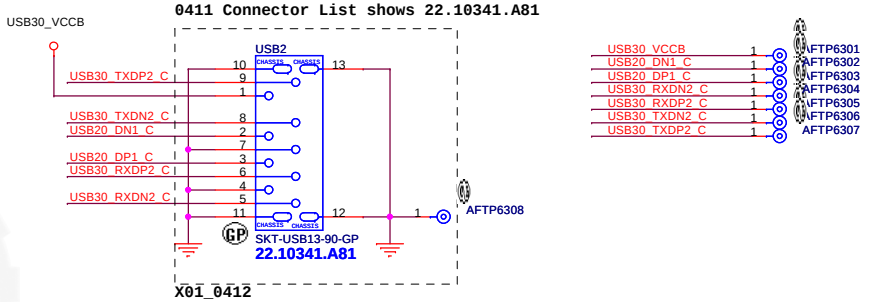
Date: Tuesday, August 14, 2012 Sheet 62 of 106

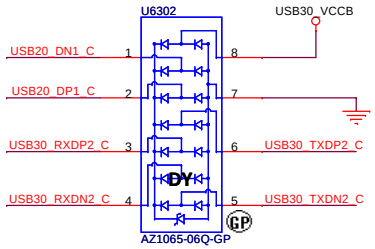
SSID = USB





USB3.0 Port2





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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB3.0 PORT***

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

Date: Tuesday, August 14, 2012 Sheet 63 of 106

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Printer***

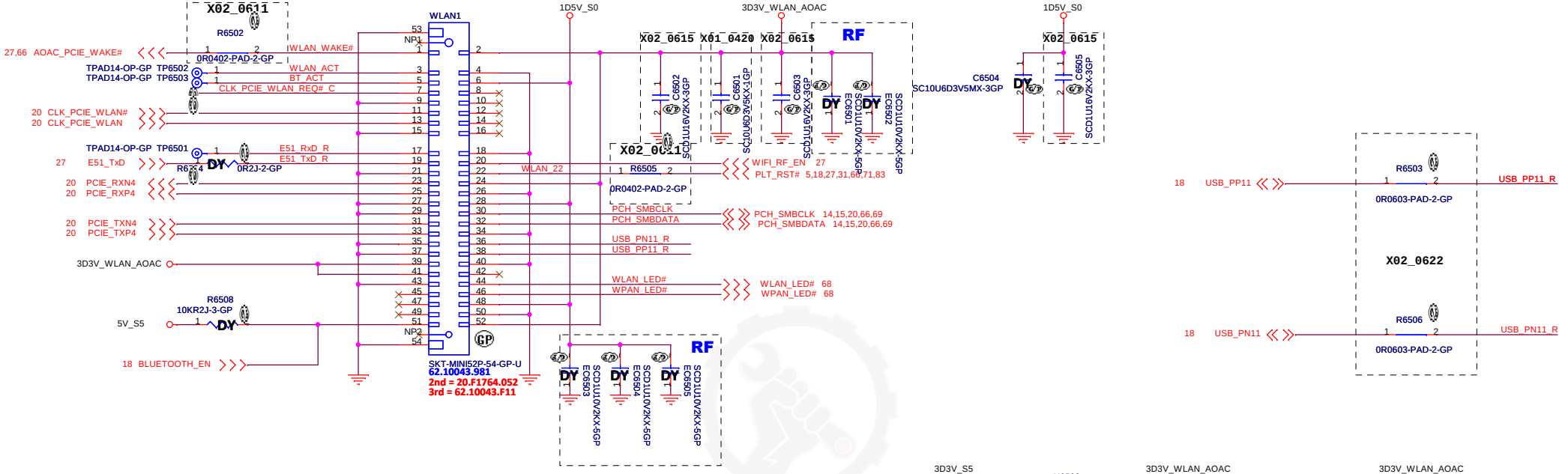
Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

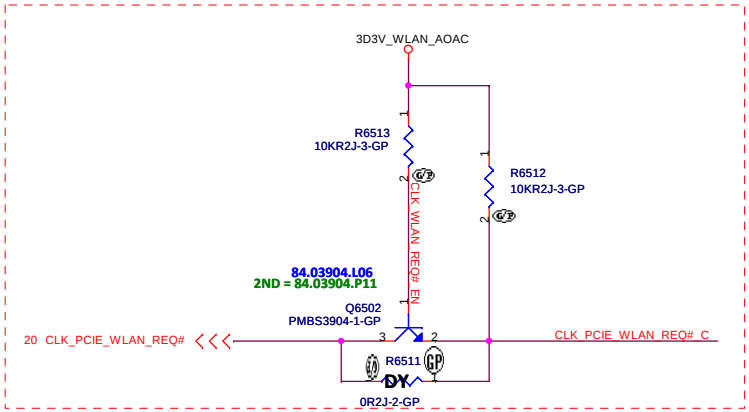
Date: Tuesday, August 14, 2012 Sheet 64 of 106

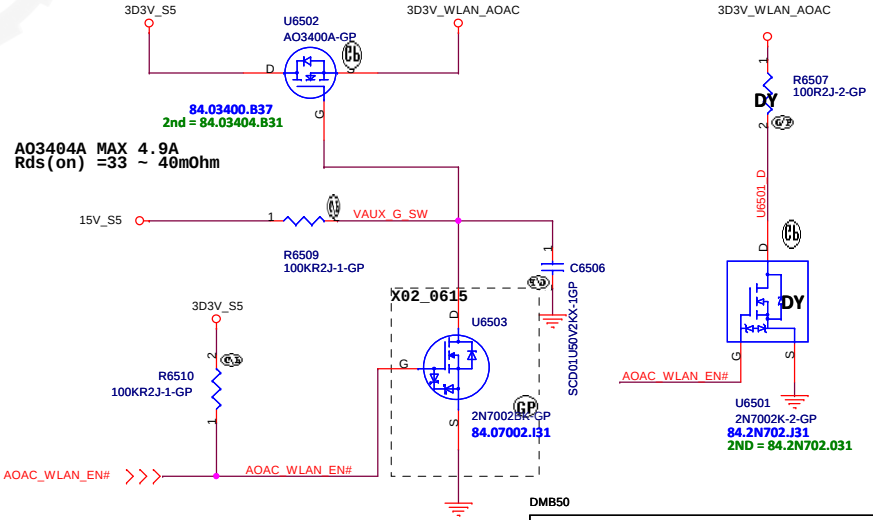
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

WLAN CONN







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Taipei Hsien 221, Taiwan, R.O.C.

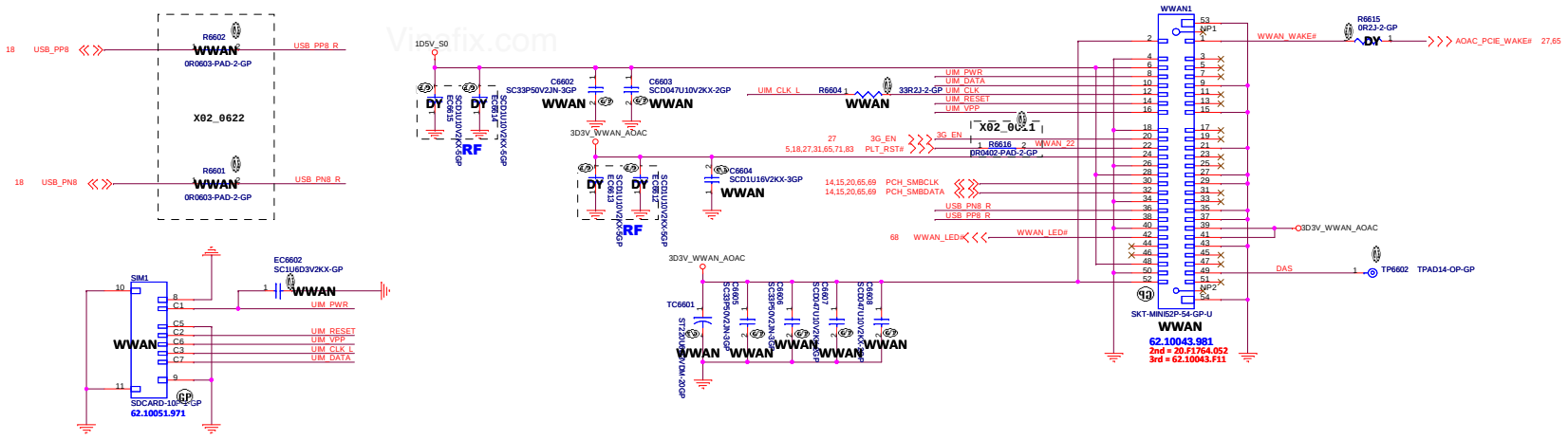
Title: **WLAN/BT**

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

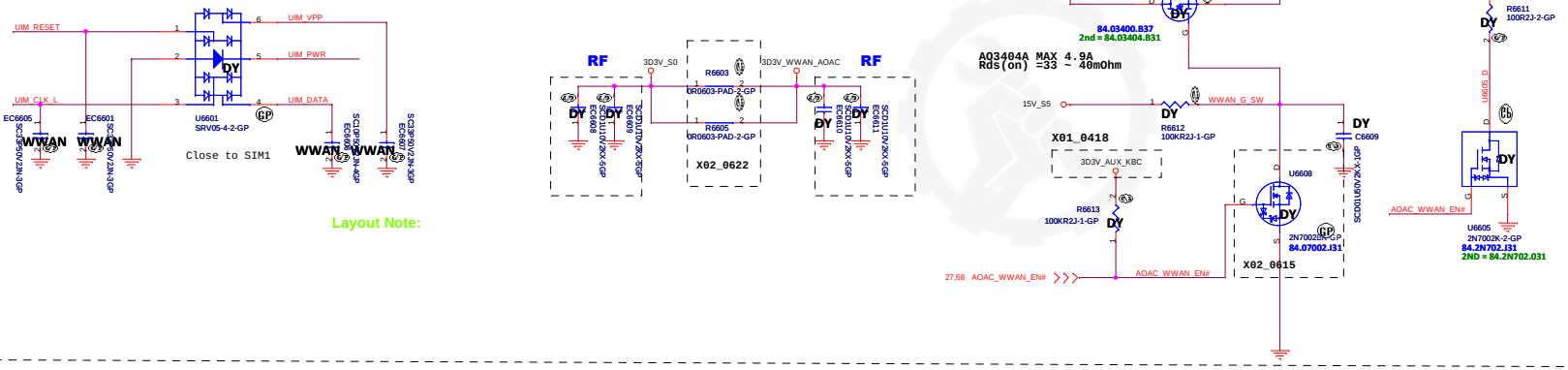
Date: Tuesday, August 14, 2012 Sheet 65 of 106

SSID = Wireless

WWAN CONN



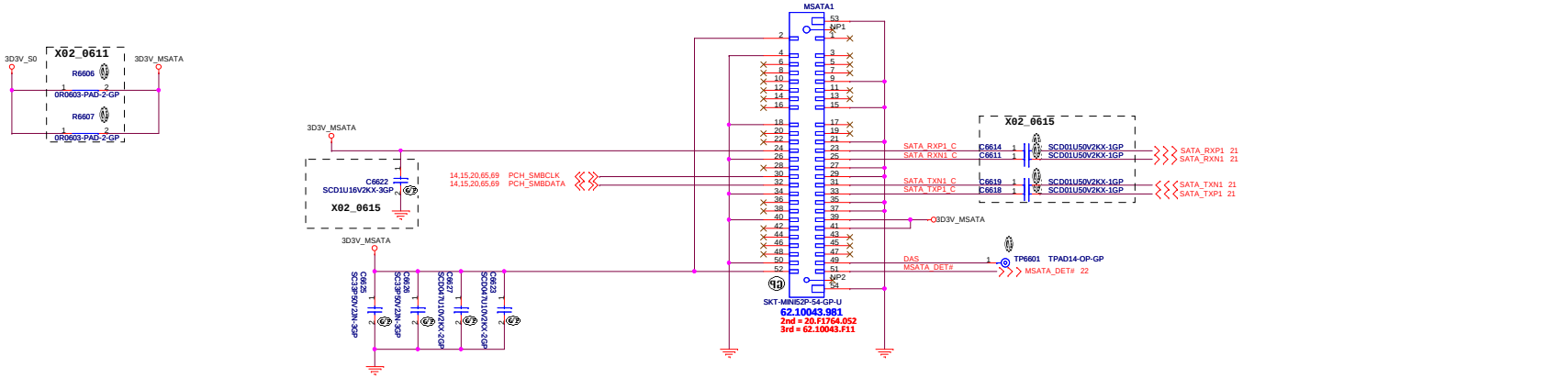
Layout Note:
DATA & CLK keep about 20mil



Layout Note:

SSID = MSATA

mSATA CONN



DMB50			
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: WWAN/MSATA			
Size: A2	Document Number: BMW Z5 DIS		Rev: A00
Date: Tuesday, August 14, 2012	Sheet 66 of 106		

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

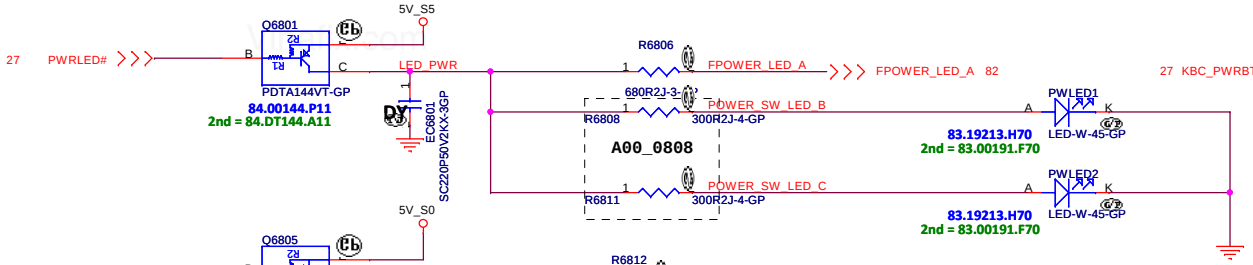
Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

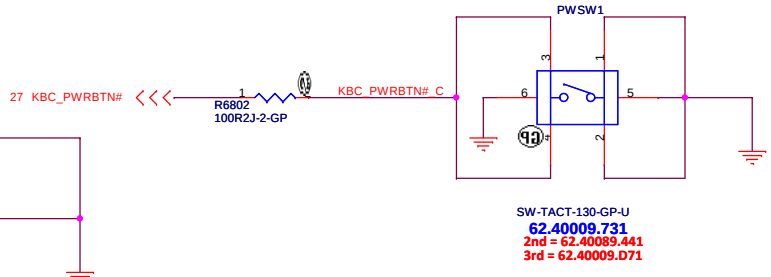
Date: Tuesday, August 14, 2012 Sheet 67 of 106

SSID = User.Interface

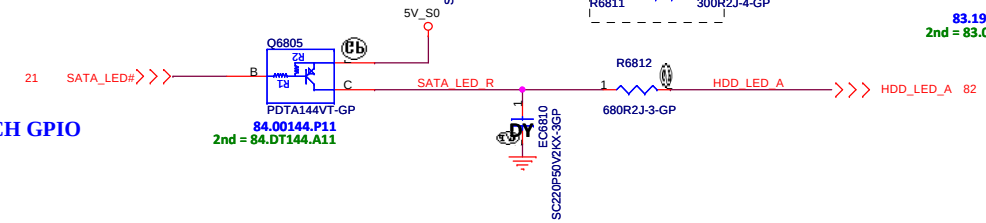
Front Power LED
LOW actived from KBC GPIO



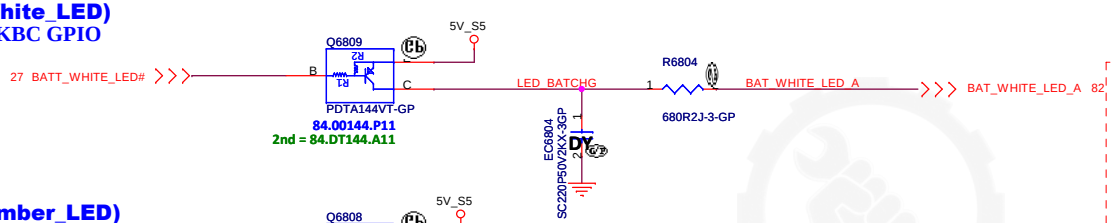
PWRBTN



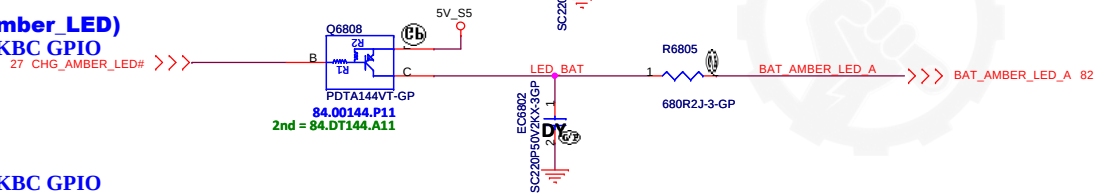
SATA HDD LED
LOW actived from PCH GPIO



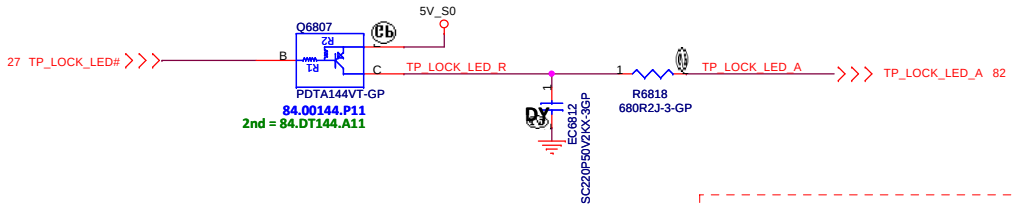
Battery LED2(White_LED)
LOW actived from KBC GPIO



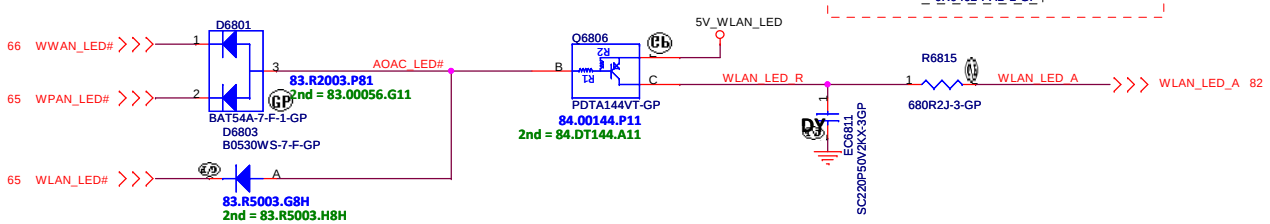
Battery LED1(Amber_LED)
LOW actived from KBC GPIO

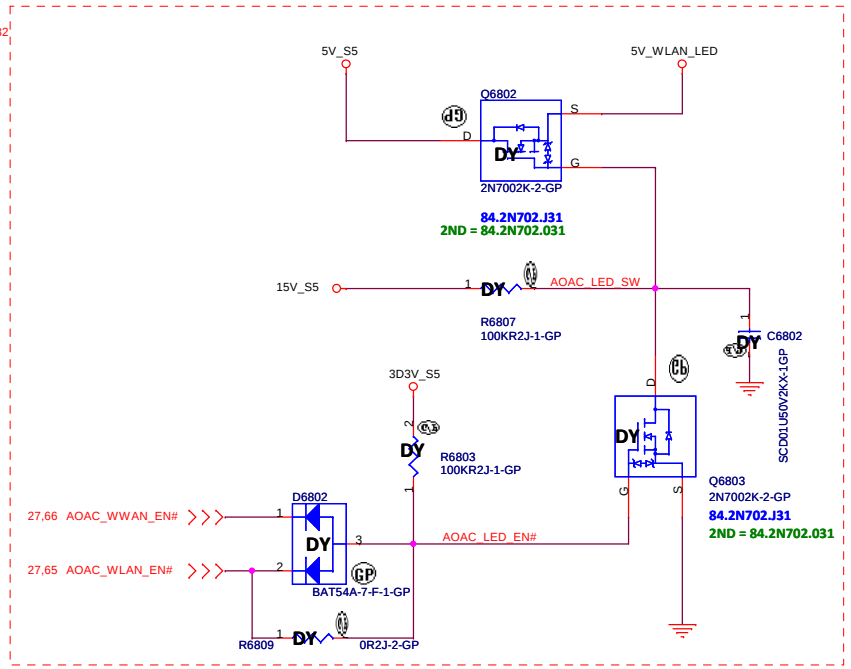


TPLOCK LED
LOW actived from KBC GPIO



WLAN LED
LOW actived from KBC GPIO





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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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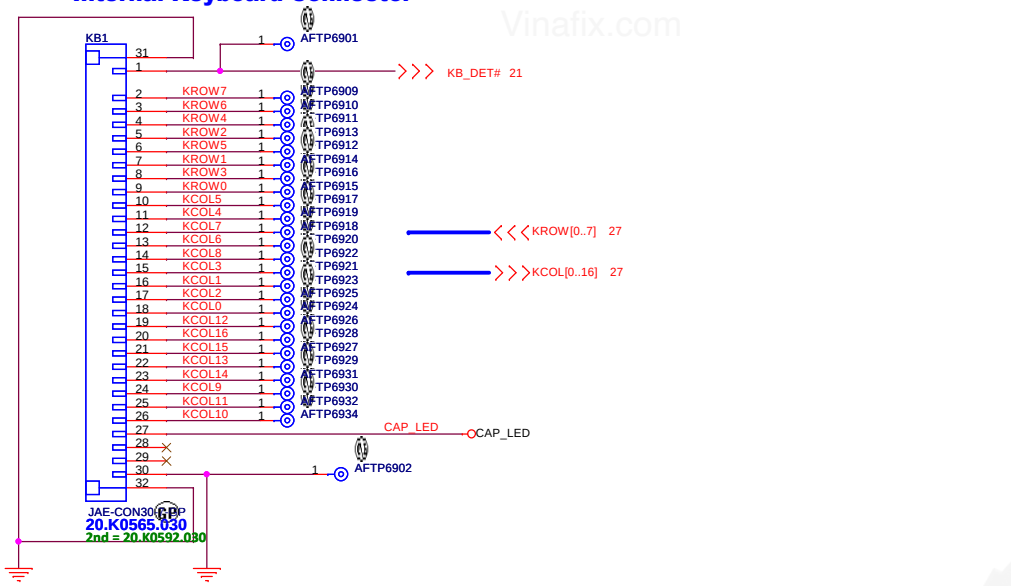
Title: LED Bard/Power Button

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 68 of 106

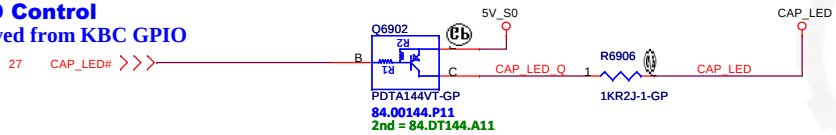
SSID = KBC

Internal Keyboard Connector



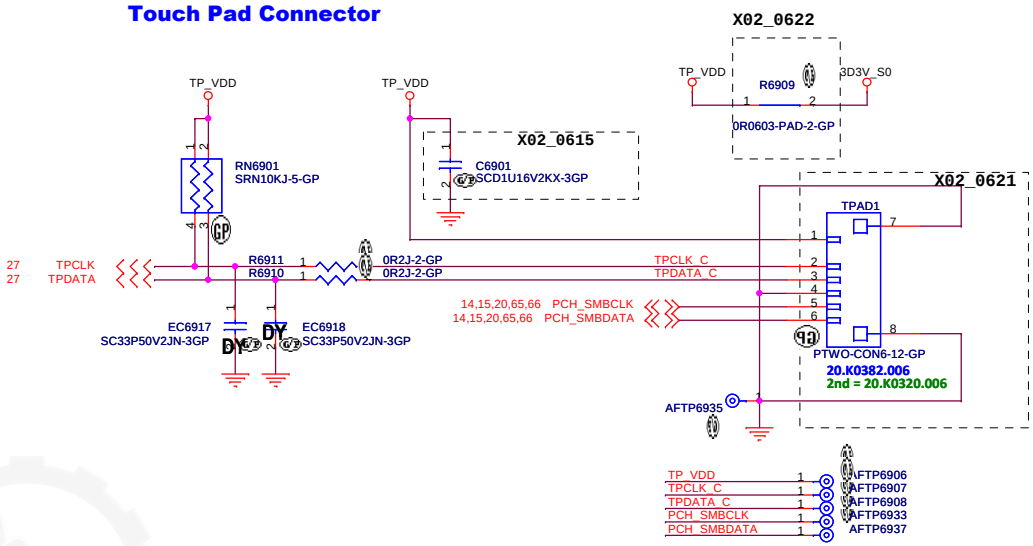
CAP LED Control

LOW actived from KBC GPIO

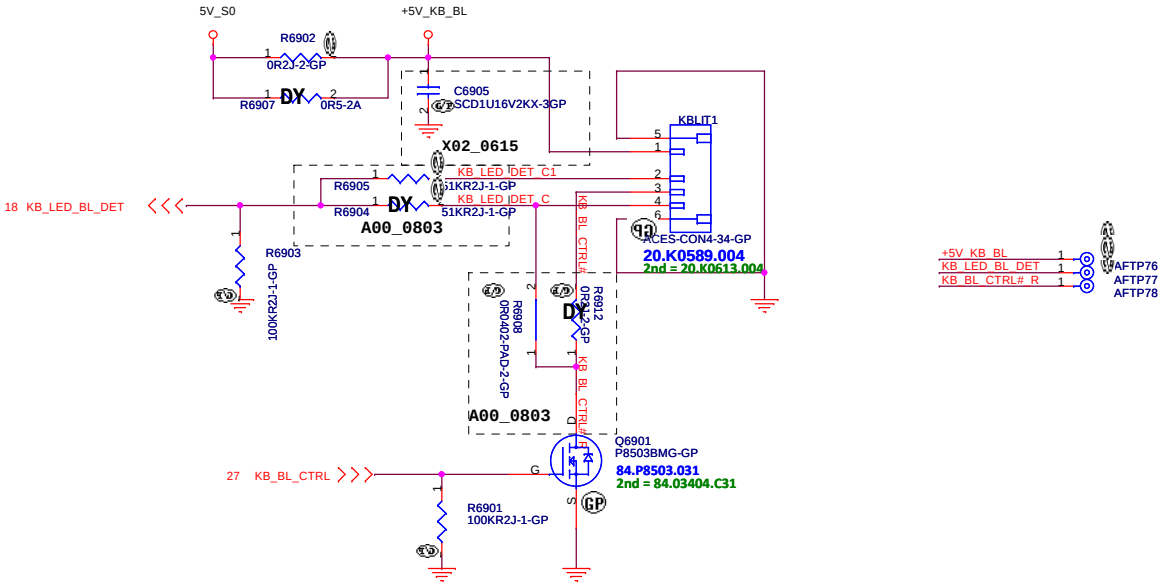


SSID = Touch.Pad

Touch Pad Connector



KB Backlight Connector



DMB50

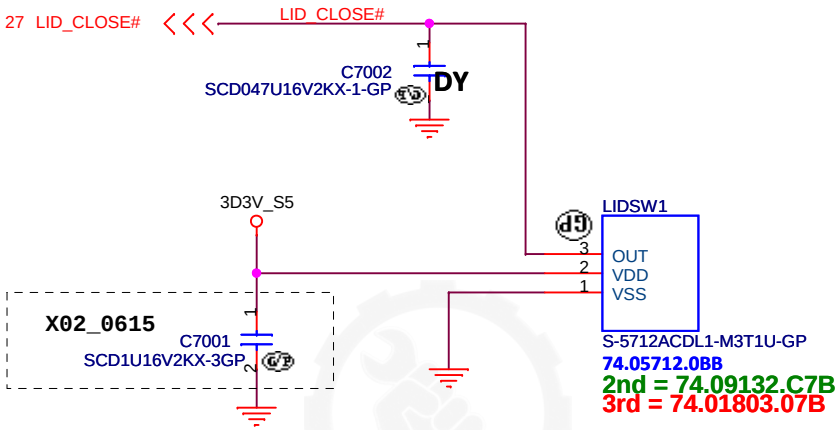
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 69 of 106

SSID = User.Interface



DMB50

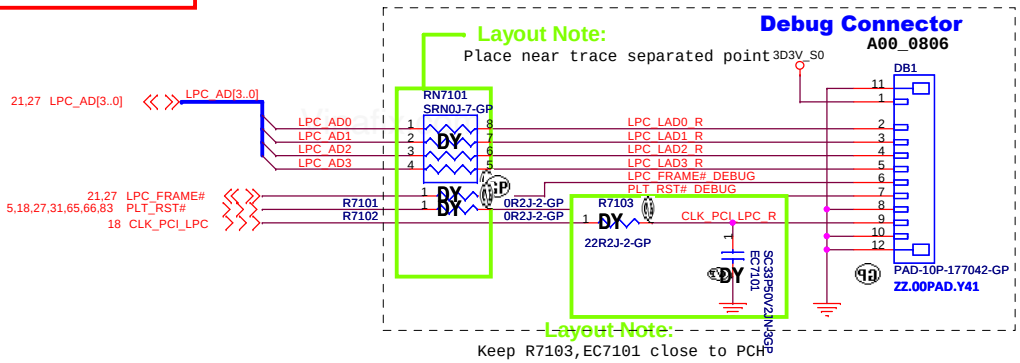
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

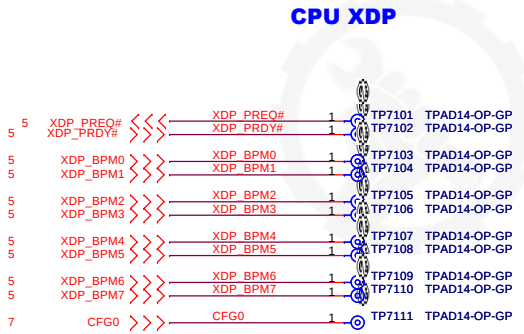
Size	Document Number	Rev
A4	***BMW Z5 DIS***	***A00***

Date: Tuesday, August 14, 2012 Sheet 70 of 106

SSID = DEBUG PORT



SSID = CPU



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

Date: Tuesday, August 14, 2012 Sheet 72 of 106

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

Date: Tuesday, August 14, 2012 Sheet 78 of 106

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

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DMB50

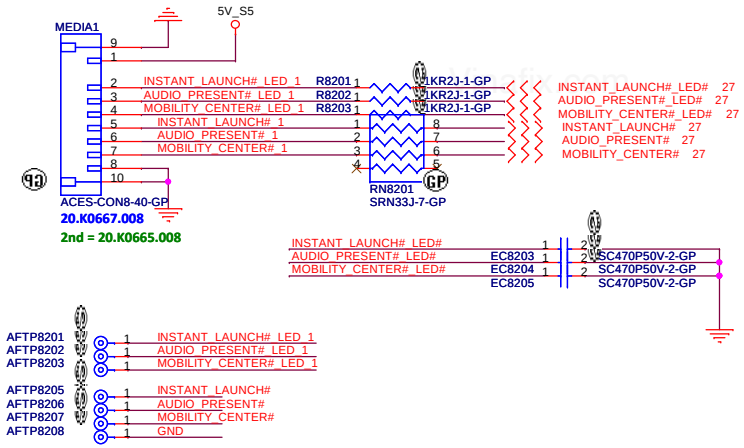
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

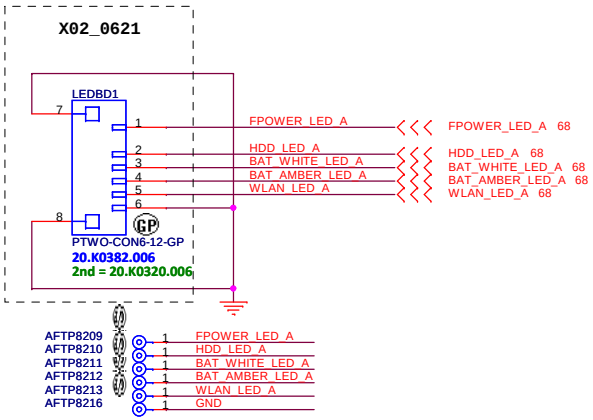
Title: *Reserved*

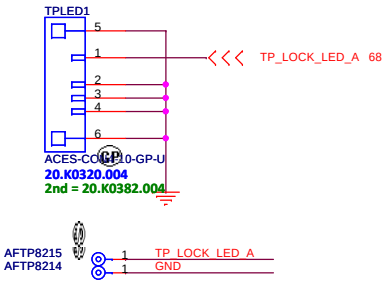
Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

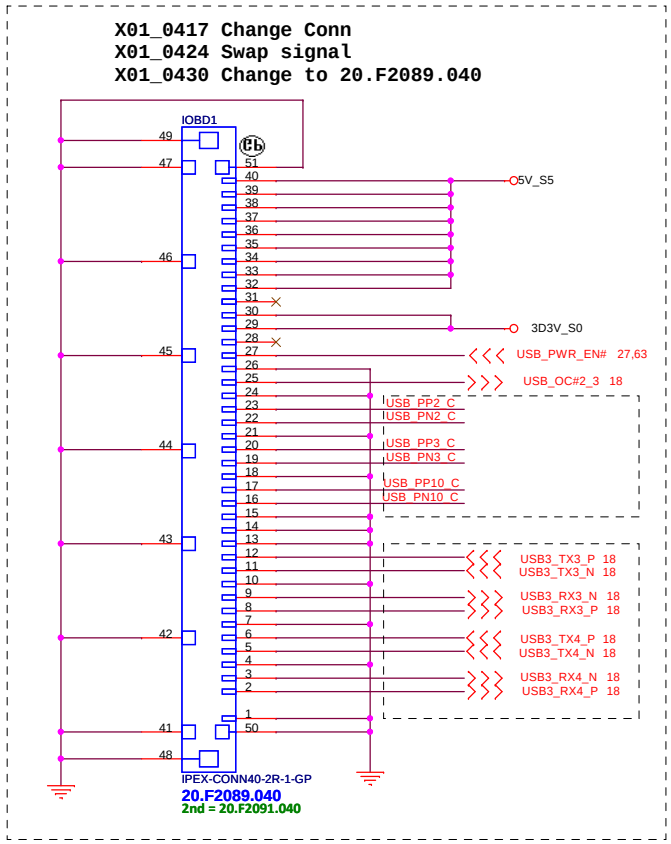
Date: Tuesday, August 14, 2012 Sheet 81 of 106

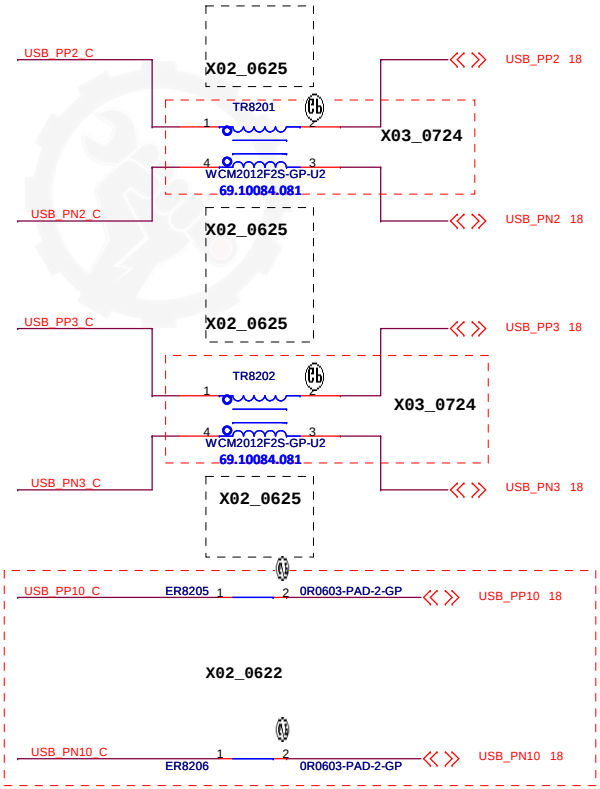
SSID = User.Interface

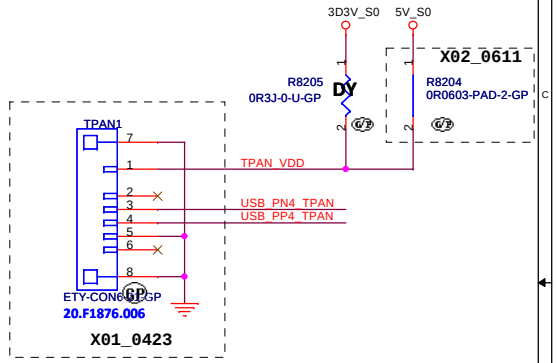


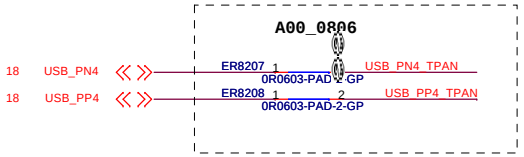


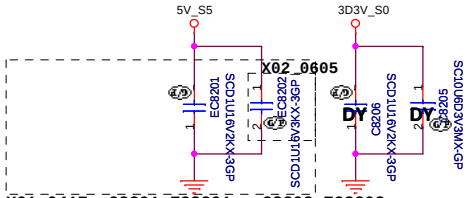












X01_0417 C8201=EC8201 , C8202=EC8202

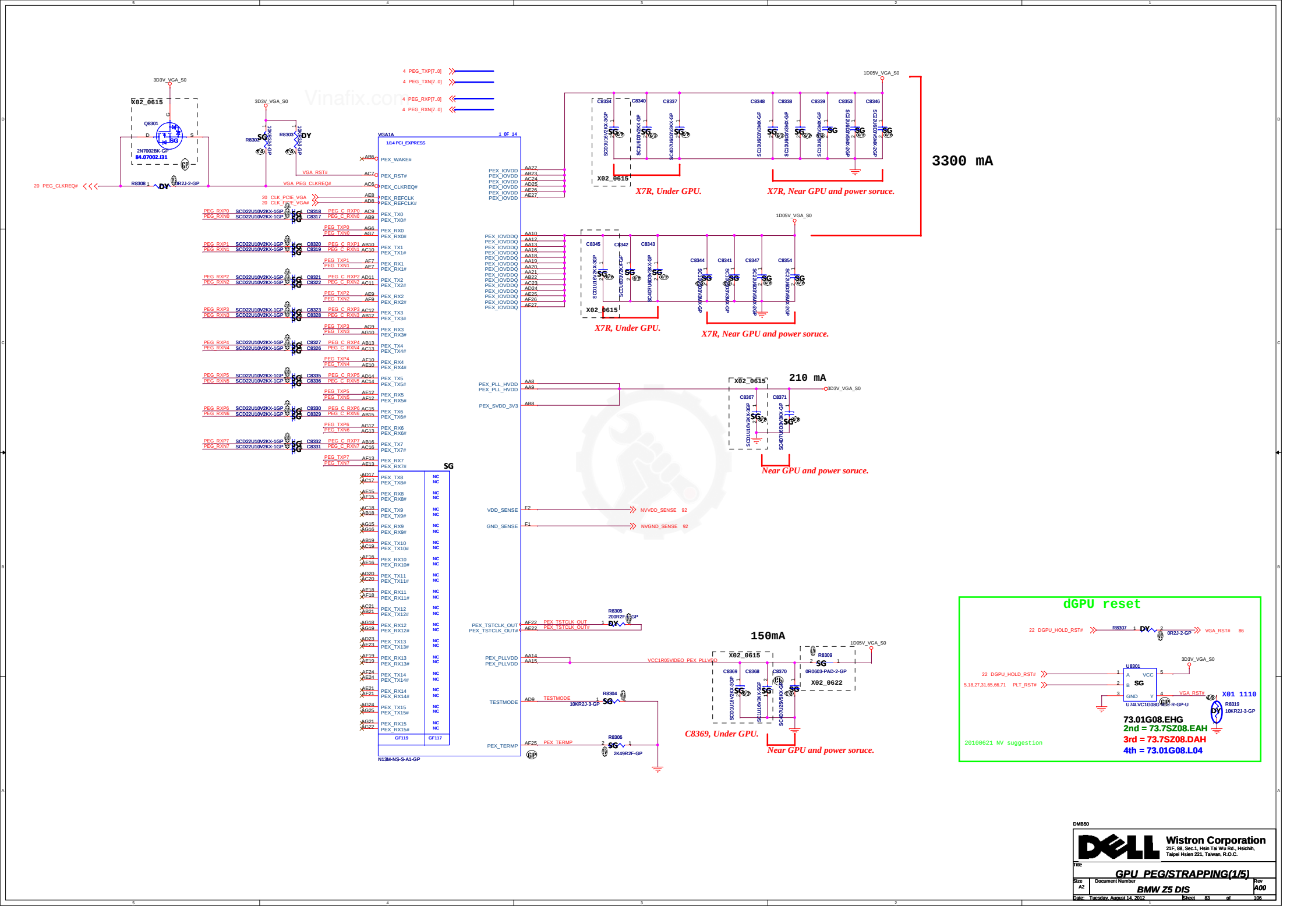
DMB50

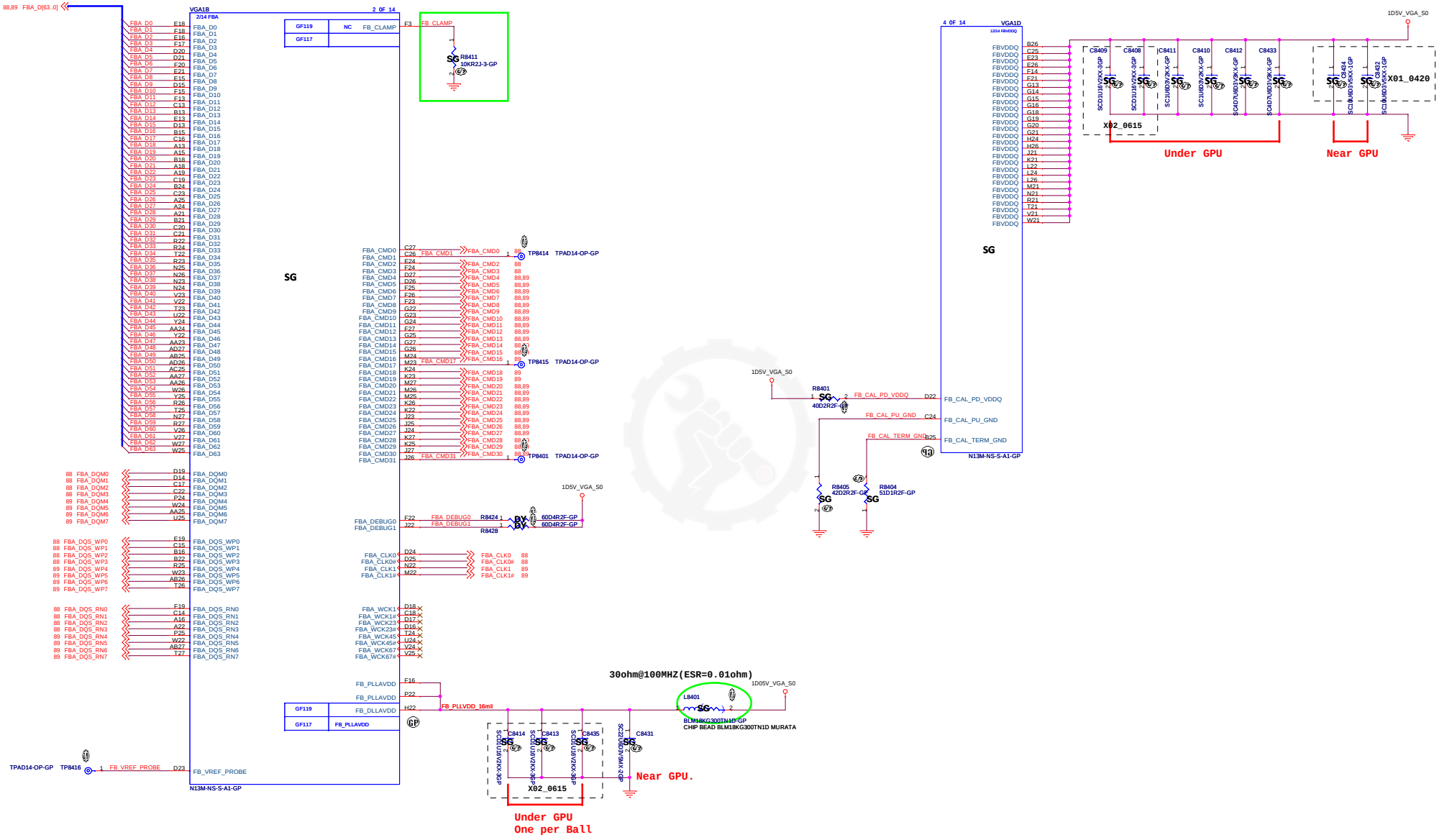
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 82 of 106


3300 mA
X7R, Under GPU.
X7R, Near GPU and power soruce.
210 mA
Near GPU and power soruce.
150mA
C8369, Under GPU.
dGPU reset
73.01G08.EHG
2nd = 73.7SZ08.EAH
3rd = 73.7SZ08.DAH
4th = 73.01G08.L04
20100621 NV suggestion
Wistron Corporation
GPU_PEG/STRAPPING(1/5)
BMW Z5 DIS
A00



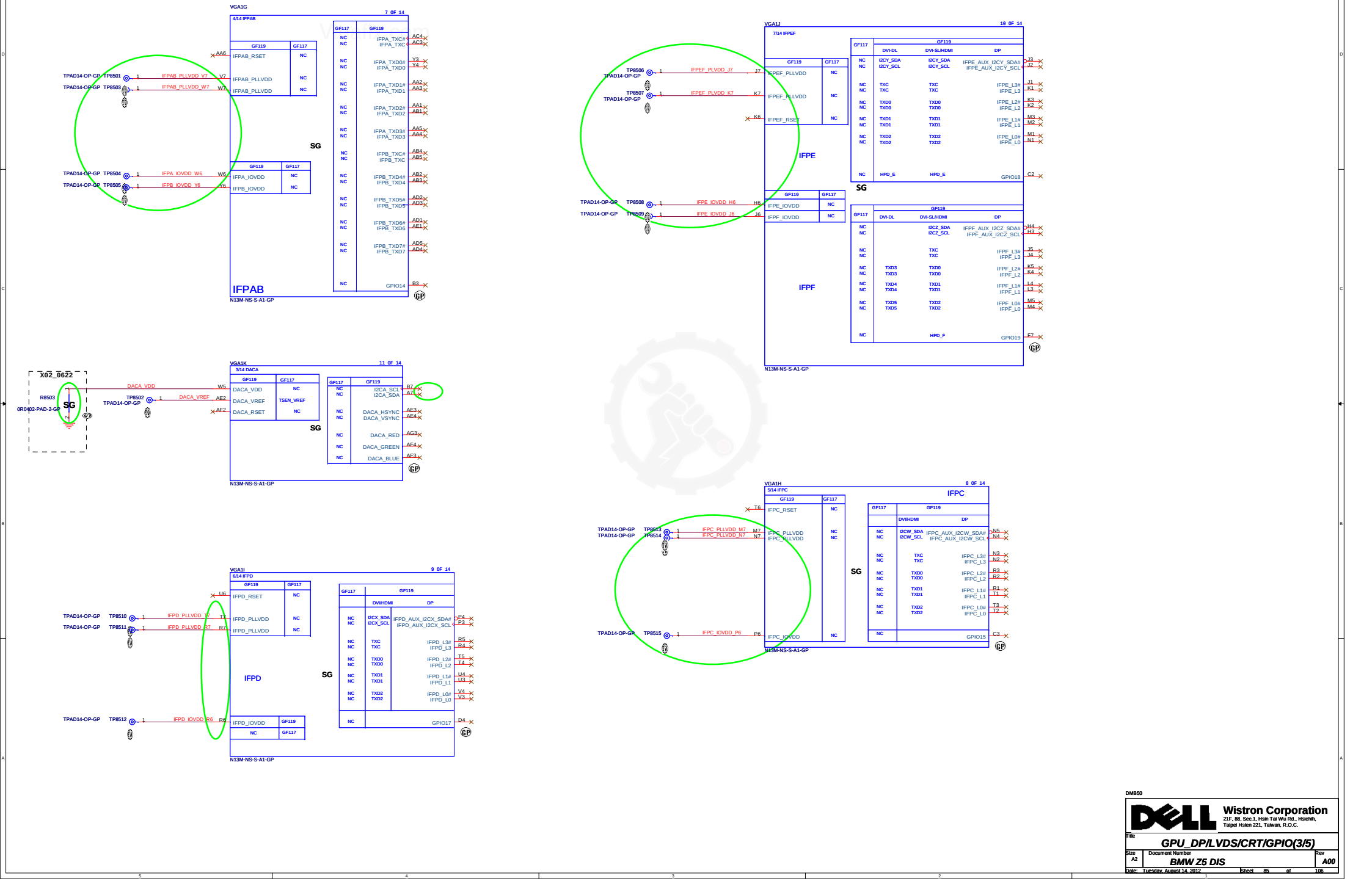
DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU Memory(2/5)**

Size	Document Number	Rev
A2	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 84 of 106


VGA1G
7 OF 14
4/4 IFPAB
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXC#
IFPA_TXC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXC#
IFPB_TXC
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
GPIO14
IFPAB
SG
N13M-NS-S-A1-GP
TPAD14-OP-GP TP8501
TPAD14-OP-GP TP8503
TPAD14-OP-GP TP8504
TPAD14-OP-GP TP8505
IFPA_PLLVDD_V7
IFPA_PLLVDD_W7
IFPA_IOVDD_W6
IFPB_IOVDD_Y6
VGA1J
10 OF 14
7/14 IFPEF
IFPEF_PLLVDD
IFPEF_PLLVDD
IFPEF_RSET
IFPE_IOVDD
IFPF_IOVDD
DVI-DL
DVI-SL/HDMI
DP
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
HPD_E
GPIO18
IFPE
SG
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
HPD_F
GPIO19
IFPF
N13M-NS-S-A1-GP
TPAD14-OP-GP TP8506
TPAD14-OP-GP TP8507
TPAD14-OP-GP TP8508
TPAD14-OP-GP TP8509
IFPEF_PLVDD_J7
IFPEF_PLVDD_K7
IFPE_IOVDD_H6
IFPE_IOVDD_J6
X02_0622
R8503
0R0402-PAD-2-GP
TP8502
TPAD14-OP-GP
DACA_VDD
DACA_VREF
VGA1K
11 OF 14
3/14 DACA
DACA_VDD
DACA_VREF
DACA_RSET
TSEN_VREF
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
SG
N13M-NS-S-A1-GP
VGA1H
8 OF 14
5/14 IFPC
IFPC_RSET
IFPC_PLLVDD
IFPC_PLLVDD
IFPC_IOVDD
DVI/HDMI
DP
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
GPIO15
IFPC
SG
N13M-NS-S-A1-GP
TPAD14-OP-GP TP8513
TPAD14-OP-GP TP8514
TPAD14-OP-GP TP8515
IFPC_PLLVDD_M7
IFPC_PLLVDD_N7
IFPC_IOVDD_P6
VGA1I
9 OF 14
6/14 IFPD
IFPD_RSET
IFPD_PLLVDD
IFPD_PLLVDD
IFPD_IOVDD
DVI/HDMI
DP
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GPIO17
IFPD
SG
N13M-NS-S-A1-GP
TPAD14-OP-GP TP8510
TPAD14-OP-GP TP8511
TPAD14-OP-GP TP8512
IFPD_PLLVDD_T7
IFPD_PLLVDD_R7
IFPD_IOVDD_R6
DMB50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DP/LVDS/CRT/GPIO(3/5)
Size
A2
Document Number
BMW Z5 DIS
Rev
A00
Date: Tuesday, August 14, 2012
Sheet 85 of 106

1.05V +/- 3%
150mA
(180 ohm ESR=0.2)

1D05V_VGA_S0 PLLVDD_PWR

L8601 0R0603-PAD-2-GP

X02_0622 X02_0615

C8608 C8609 C8604 C8605

NEAR GPU

X7R, Under GPU.

TP8606 TPAD14-OP-GP

VGA1M 9/14 XTAL_PLL 13 OF 14

CORE_PLLVDD SP_PLLVDD VID_PLLVDD N6

VID_PLLVDD GF119 NC GF117

VIDEO_CLK_XTAL_SS A10 XTAL_SSIN

C11 XTAL_IN

XTAL_OUTBUFF C10 N12P_XTAL_OUTBUFF

XTAL_OUT B10

N13M-NS-S-A1-GP

R8604 10KR2J-3-GP

R8605 10KR2J-3-GP

27MHZ_IN 27MHZ_OUT

C8611 SC12P50V2JN-3GP

82.30034.641
2nd = 82.30034.651
3rd = 82.30034.681

X8601 XTAL-27MHZ-85-GP

1MR2F-GP R8606

R8607 0R0402-PAD-2-GP

X02_0622

C8610 SC12P50V2JN-3GP

27MHZ_OUT_R

VGA1N 8/14 MISC1 14 OF 14

TPAD14-OP-GP TP8607 THERMDN E12

TPAD14-OP-GP TP8608 THERMDP F12

TPAD14-OP-GP TP8609 TPAD14-OP-GP TP8603 TPAD14-OP-GP TP8604 TPAD14-OP-GP TP8605

JTAG_TCK_VGA AE5 NV_TMS AD6 NV_TDI AE6 NV_TDO AF6 JTAG_TRST# AG4

JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST#

RN8602 SRN10KJ-5-GP

I2CS_SCL I2CS_SDA I2CC_SCL I2CC_SDA

SMBC_Therm_NV SMBD_Therm_NV GPU_LVDS_CLK1 GPU_LVDS_DATA1

GF117 GF119 NC I2CB_SCL I2CB_SDA

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13

NV_VID4 NV_VID3 NV_VID1 NV_VID2 NV_THERM_OVERT NV_THERM_ALERT NV_VID0 PWR_LEVEL NV_VID5

GPIO16 GPIO20 GPIO21

N13M-NS-S-A1-GP

3D3V_VGA_S0 RN8606 SRN2K2J-1-GP

GPIO12
1 - > normal mode
0 -> P8 mode

R8606 100KR2J-1-GP AC_PRESENT_R

X02_0615 Q8603 2N7002BKS-GP-U 84.2N702.E3F

R8609 10KR2J-3-GP PWR_LEVEL

27 OVER_CURRENT_P8#

R8610 100KR2J-1-GP H_PROCHOT#_LL

Q8604 ME2N7002DKW-G-GP 84.2N702.F3F
2nd = 84.2N702.A3F
3rd = 84.DMN66.03F

5 H_PROCHOT#_L

Samsung (72.41646.00U)
Micron (72.41K26.00U)

	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
Micron(0x5)	1	0	1	0	0
	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
Samsung(0x1)	1	0	0	0	0

RN8603 SRN10KJ-5-GP

NV_THERM_OVERT NV_THERM_ALERT

VGA_RST# R8641 0R2J-2-GP VGA_RST#_R

Q8602 2N7002BK-GP 84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

PURE_HW_SHUTDOWN# 27,28,36

RN8605 SRN4K7J-8-GP

X02_0615 Q8601 2N7002BKS-GP-U 84.2N702.E3F

SMBC_Therm_NV SMBD_Therm_NV

SML1_CLK 20,27,28 SML1_DATA 20,27,28

VGA1L 1014 MISC2 12 OF 14

VMON_IN0 VMON_IN1

RAM_CFG[0] RAM_CFG[1] RAM_CFG[2] RAM_CFG[3] PCIE_MAX_SPEED

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4

GF119 GF117 STRAP5 NC

MULTI_STRAP_REF0_GND

MULTI_STRAP_REF1_GND NC

MULTI_STRAP_REF2_GND NC

N13M-NS-S-A1-GP

Follow PUN-05935-001_V03

R8636 10KR2J-3-GP

ROM_CS# ROM_SI ROM_SO ROM_SCLK

SUB_VENDOR VGA_DEVICE SMB_ALT_ADDR

R8624 2KR2F-GP R8625 10KR2F-GP R8626 15KR2F-GP

R8627 10KR2F-2-GP R8617 10KR2F-2-GP R8618 10KR2F-2-GP

BUFRST# PGOOD CEC

VGA_PGOOD

R8639 10KR2F-2-GP

N13x GPUs do not support CEC.Leave the CEC pin as NC

R8631 10KR2F-2-GP R8633 10KR2F-2-GP Micron R8635 10KR2F-2-GP

R8630 10KR2F-2-GP R8632 10KR2F-2-GP SAMSUNG R8634 10KR2F-2-GP

R8640 10KR2F-2-GP R8638 4K99R2F-L-GP

R8637 10KR2F-2-GP R8623 10KR2F-2-GP

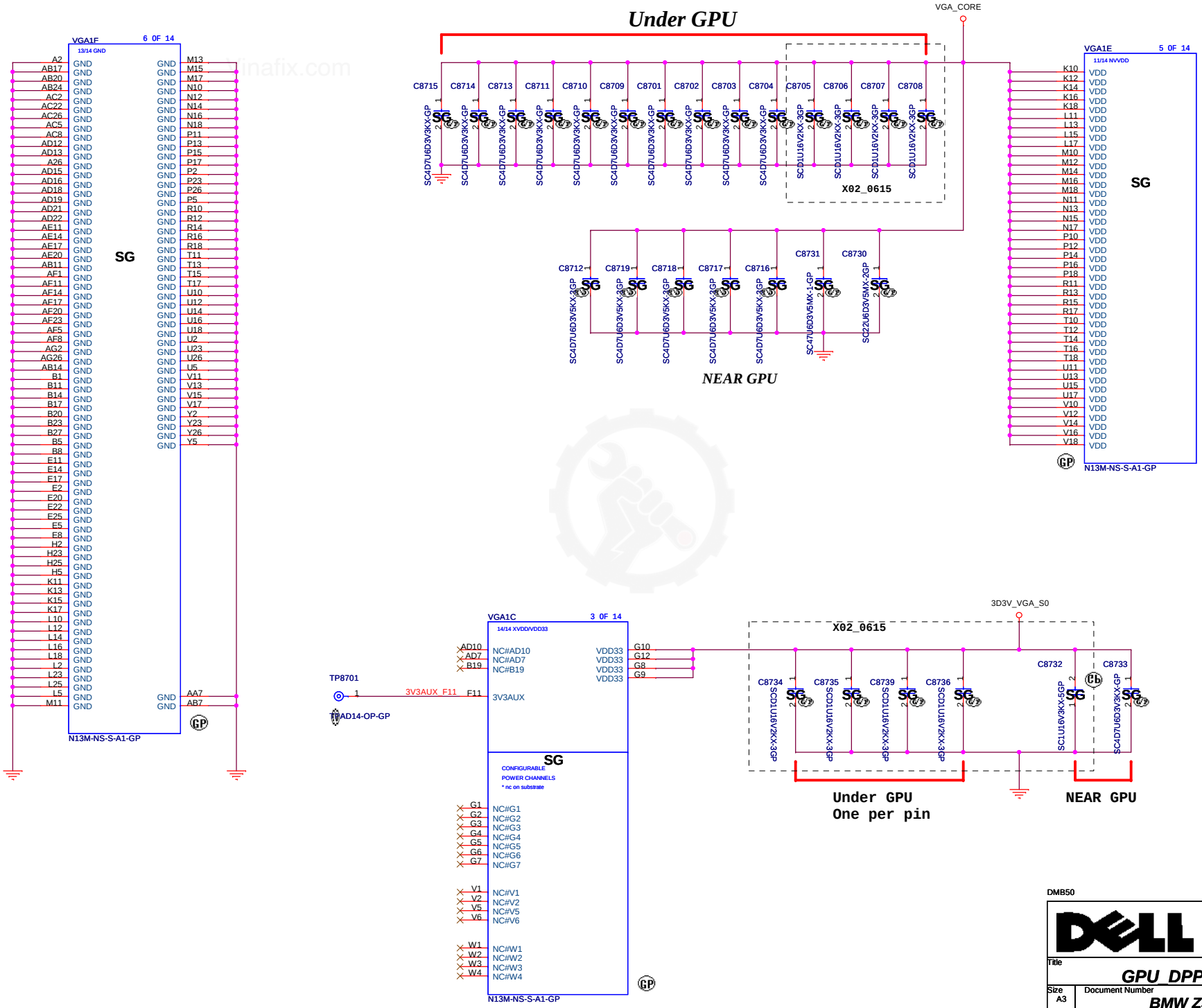
DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 Document Number: BMW Z5 DIS Rev: A00

Date: Tuesday, August 14, 2012 Sheet 86 of 106



DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

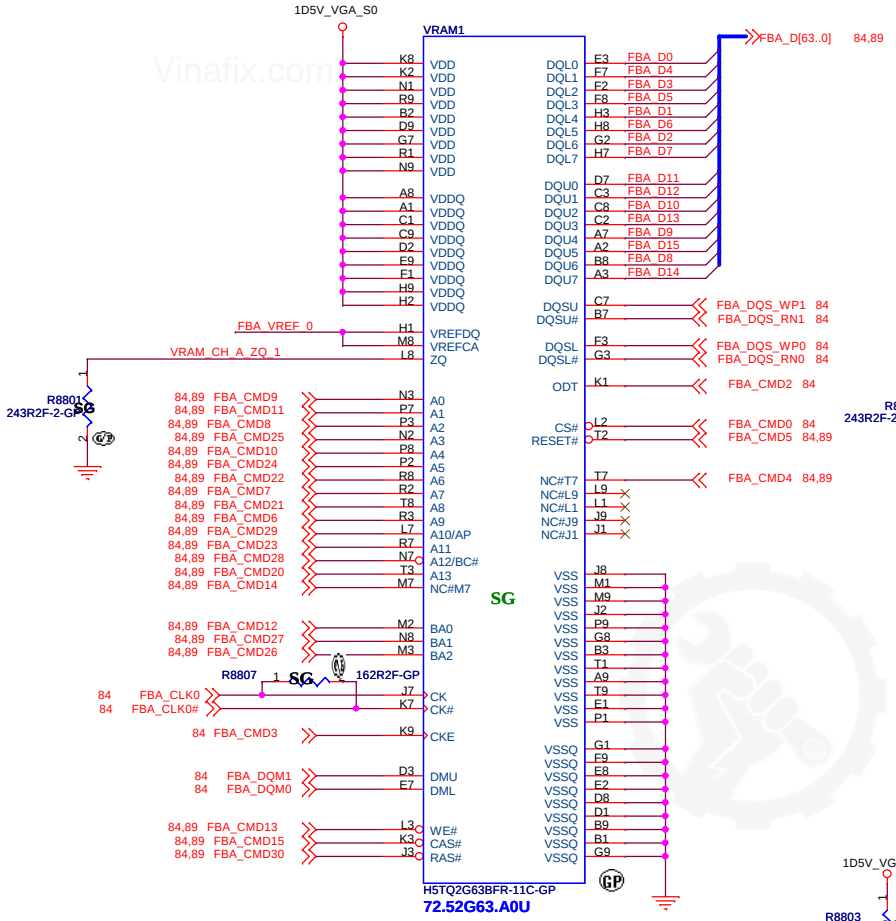
Date: Tuesday, August 14, 2012 Sheet 87 of 106

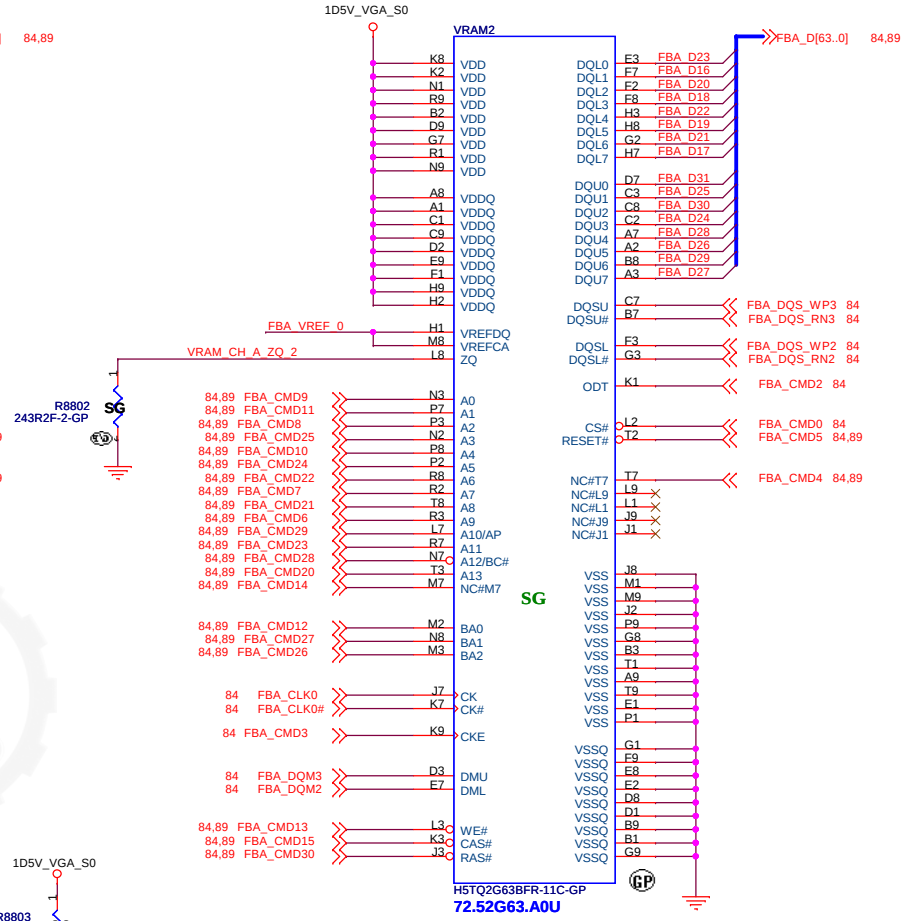
MODE D

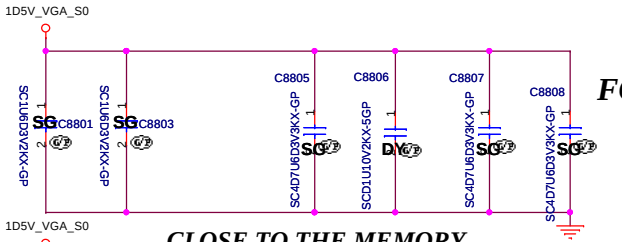
GF1XX SDDR3 CMD MAPPING

	0-31	32-63
CMD0	CS0*	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0*
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		

* A15 is not required for any x16 device, even up to 4Gb density
* A15 is only needed if we support x8 configurations, and only at 4Gb

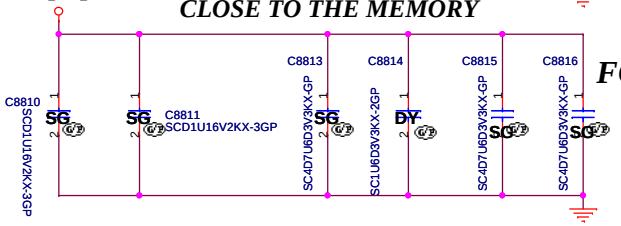




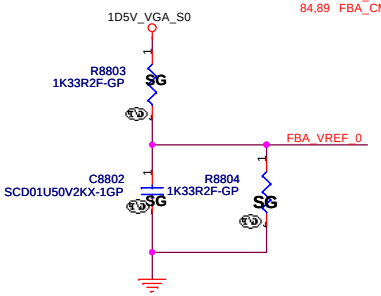


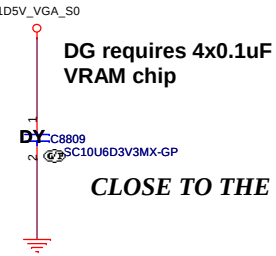
FOR VRAM1

CLOSE TO THE MEMORY



FOR VRAM2

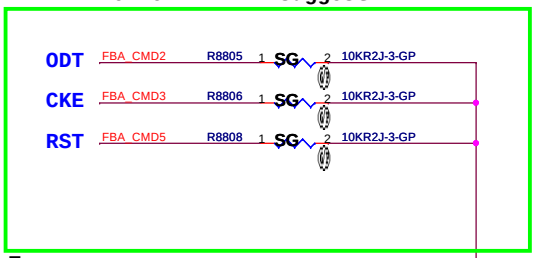




CLOSE TO THE MEMORY

DG requires 4x0.1uF and 8x1.0uF per VRAM chip

follow NV FAE suggest



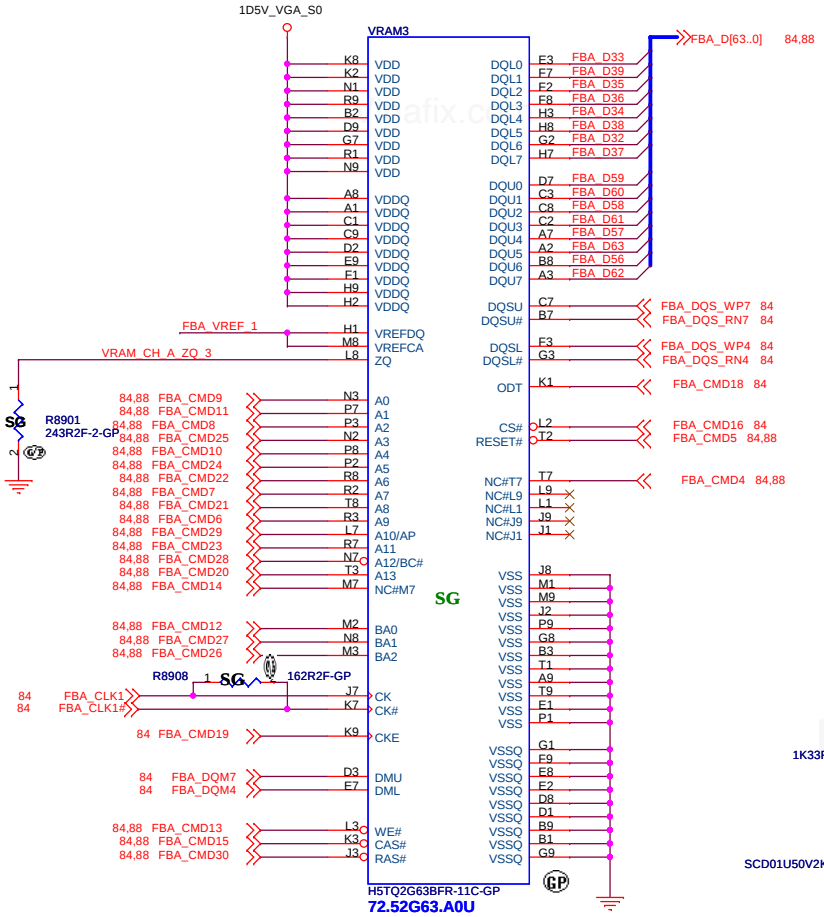
DMB50

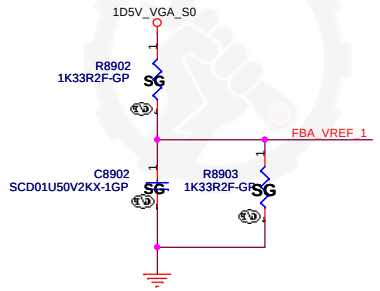
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

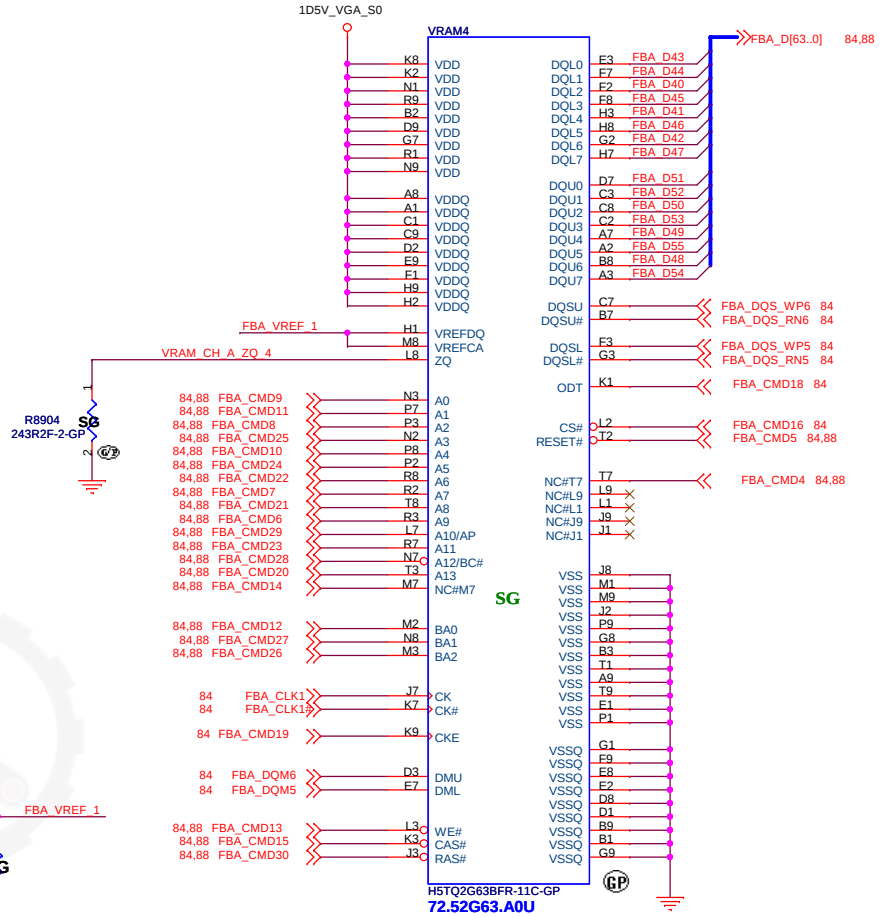
Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

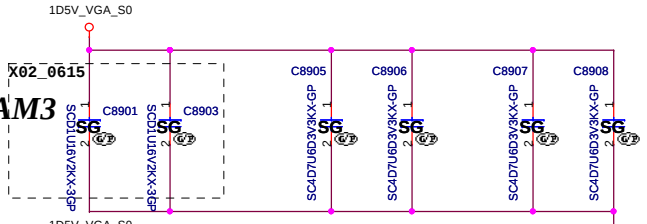
Date: Tuesday, August 14, 2012 | Sheet 88 of 106





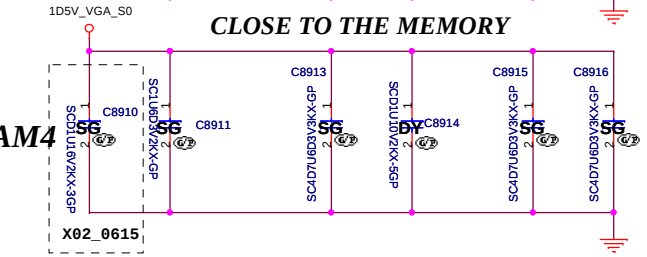


FOR VRAM3

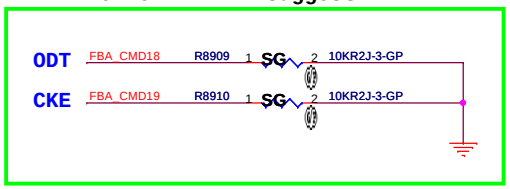


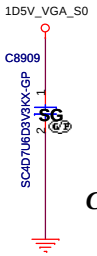
CLOSE TO THE MEMORY

FOR VRAM4



follow NV FAE suggest





CLOSE TO THE MEMORY

DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 89 of 106

(Blanking)

DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: BMW Z5 DIS | Rev: A00

Date: Tuesday, August 14, 2012 | Sheet 90 of 106

(Blanking)

DMB50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (3/4)		
Size: A3	Document Number: BMW Z5 DIS	Rev: A00
Date: Tuesday, August 14, 2012	Sheet 91 of 106	

SSID = PWR.Plane.Regulator_vga_core

V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0

Please confirm with H/W for resistor pull high and pull GND

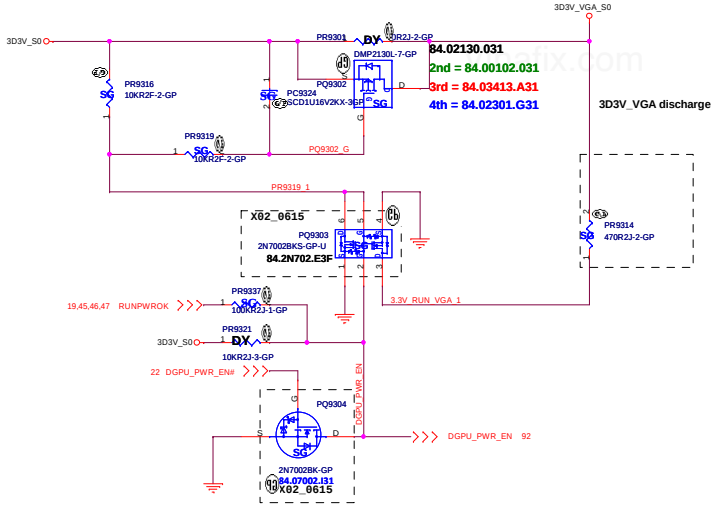
Please confirm on H/W side whether have resistor pull high and pull GND by 100 ohm

Design Current = 25A
OCP>31A

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File:	ADP3211+VGA_CORE
Size: A1	Document Number: SMW Z5 DIS
Date: Tuesday, August 14, 2012	Sheet 92 of 106

SSID = PWR.Plane.Regulator_3p3v_vga, 1p8v_vga, 1p5v_vga, 1v_vga

3D3V_S0 to 3D3V_VGA_S0 Transfer



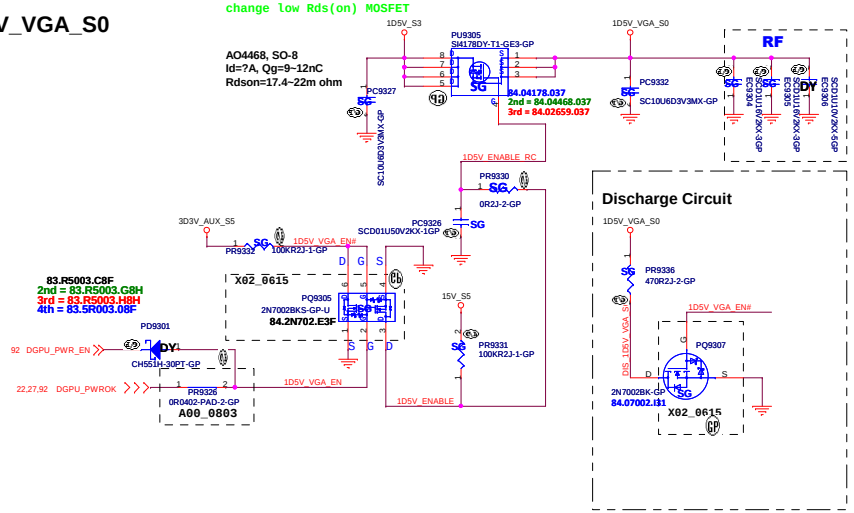
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

NV do not need 1.8V

1D5V_VGA_S0

change low Rds(on) MOSFET

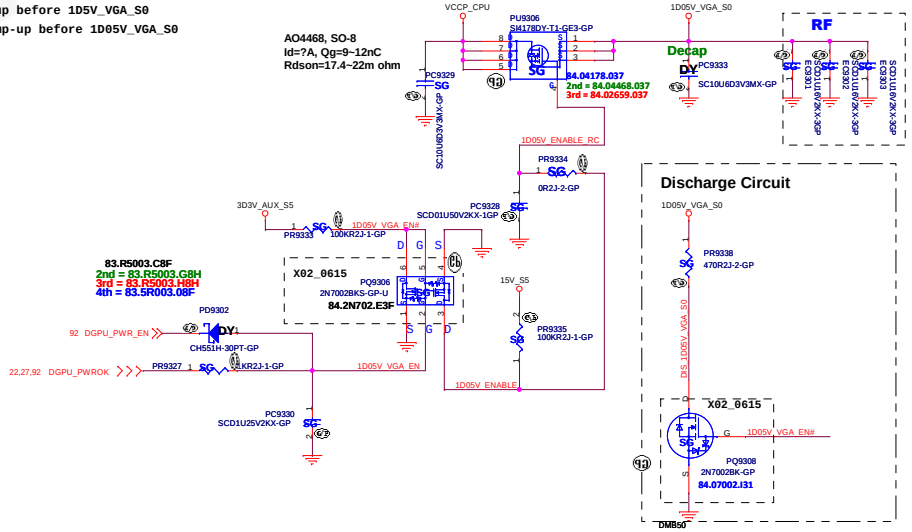
AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm



1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0

AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm



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Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	BMW Z5 DIS	A00

Date: Tuesday, August 14, 2012 Sheet 93 of 106

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z5 DIS*	*A00*

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Title: *Reserved*

Size: A3 | Document Number: *BMW Z5 DIS* | Rev: *A00*

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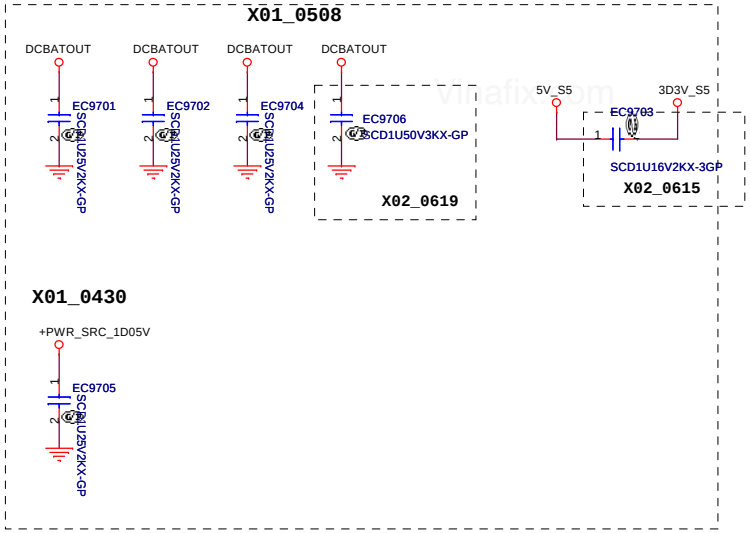
SSID = User.Interface



On the TOP side

HS1 STF237R148H67-GP

HS2 STF237R148H67-GP

HS3 STF237R117H83-1-GP

HS4 STF237R117H83-1-GP

H1 HOLE256R115-GP

H2 HOLE256R115-GP

H3 HOLE237R95-GP

H4 HOLE256R115-GP

H5 HOLE335R115-GP

H6 HOLE335R115-GP

H7 HT85BE95R29-U-5-GP

H8 HOLE197R166-1-GP

H9 HOLE197R166-1-GP

H10 HOLE197R166-1-GP

H11 HOLET335B131R115-GP

H12 HOLE237R95-GP

H13 HOLE237R95-GP

H14 HOLE237R95-GP

SPR1 SPRING-13-GP-U

X01_0412

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Title: *UNUSED PARTS/EMI Capacitors*

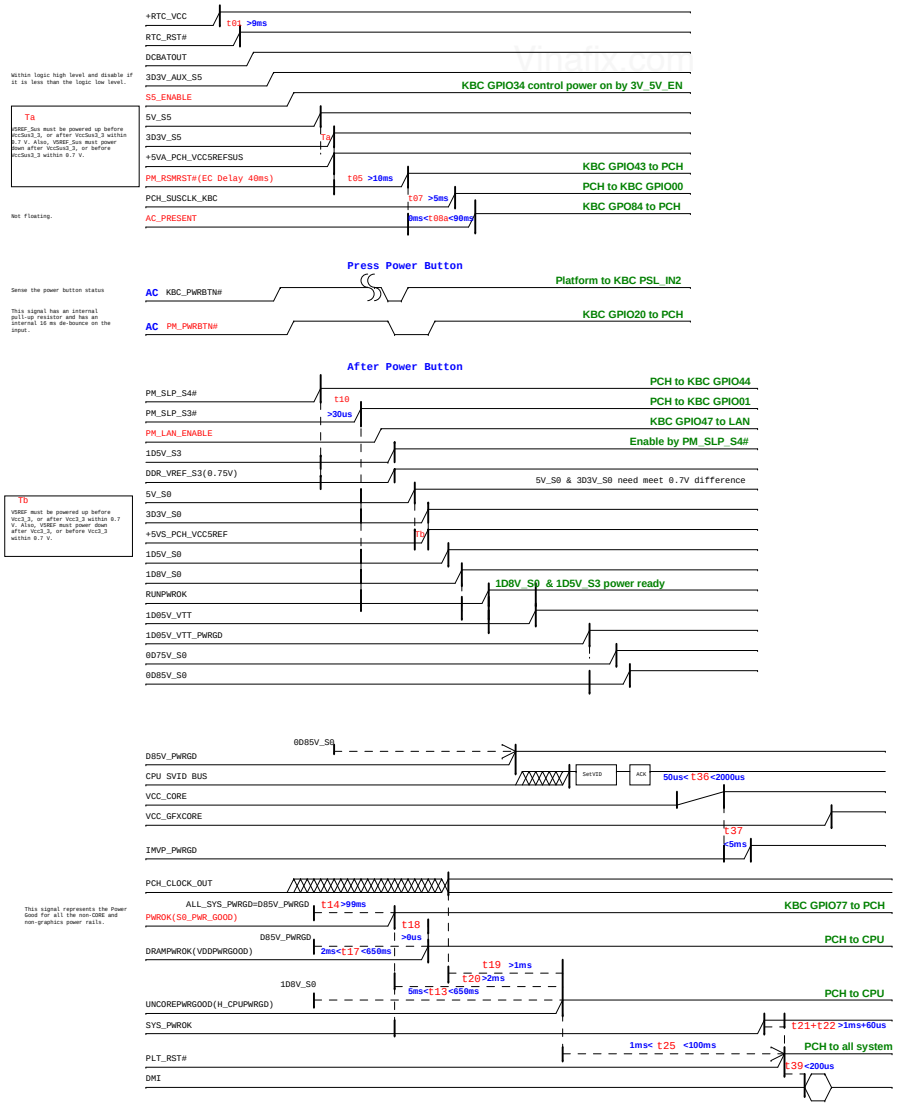
Size: A3 | Document Number: *BMW Z5 DIS* | Rev: *A00*

Date: Tuesday, August 14, 2012 | Sheet 97 of 106

Chief River Platform Power Sequence

(AC mode)

Red Words: Controlled by EC GPIO



Within logic high level and disable if it is less than the logic low level.

Ta: VSREF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, VSREF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.

Not floating.

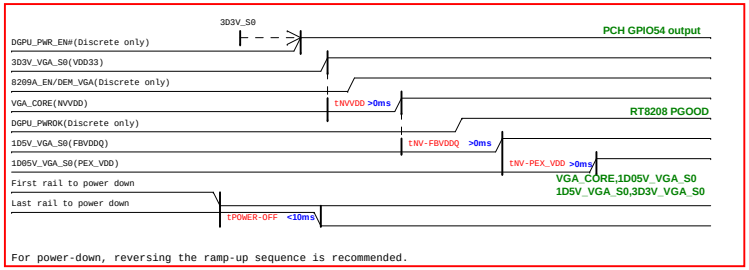
Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.

Tb: VSREF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, VSREF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

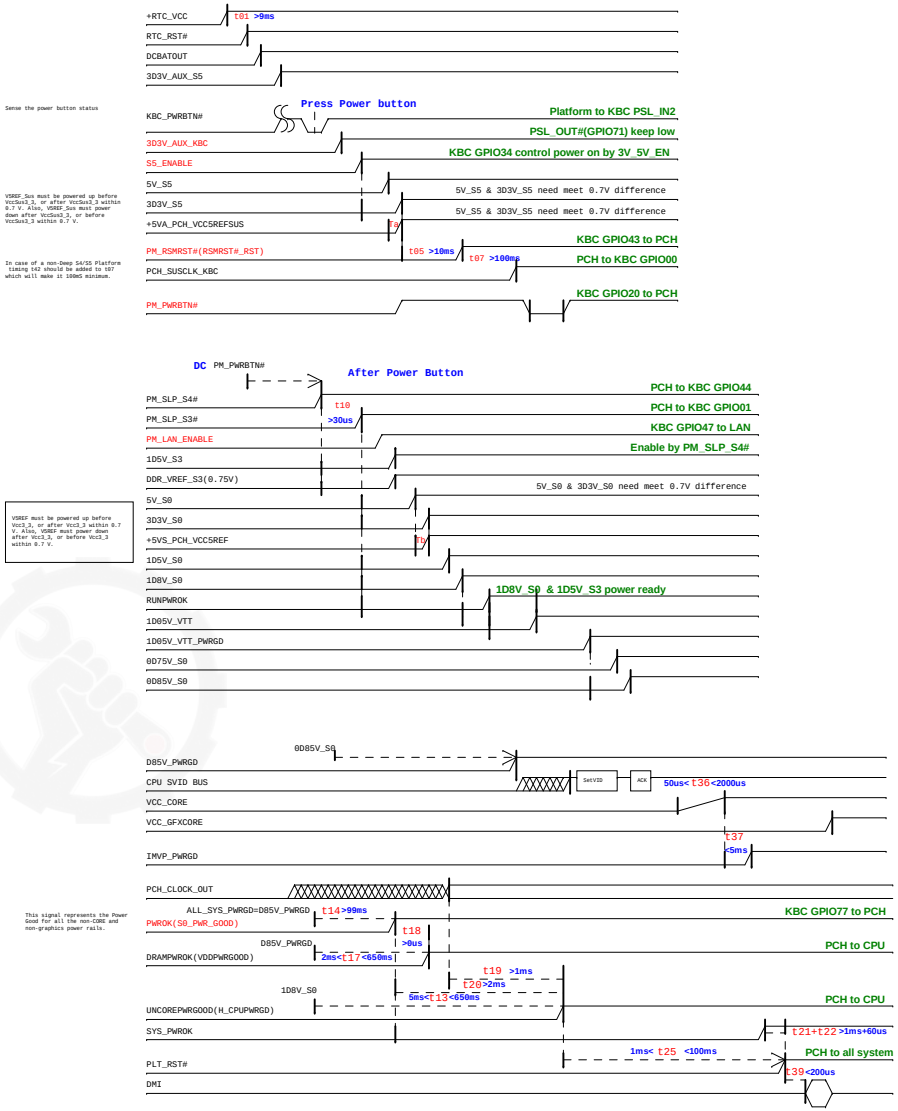
N13M-GS Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

Red Words: Controlled by EC GPIO



Sense the power button status

VSREF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, VSREF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.

In case of a non-Deep S4/S5 Platform timing t42 should be added to t07 which will make it 100mS minimum.

VSREF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, VSREF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

CN0D50

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Title: Power Sequence

Size	Document Number	Rev
A1	BMW Z5 DIS	A00

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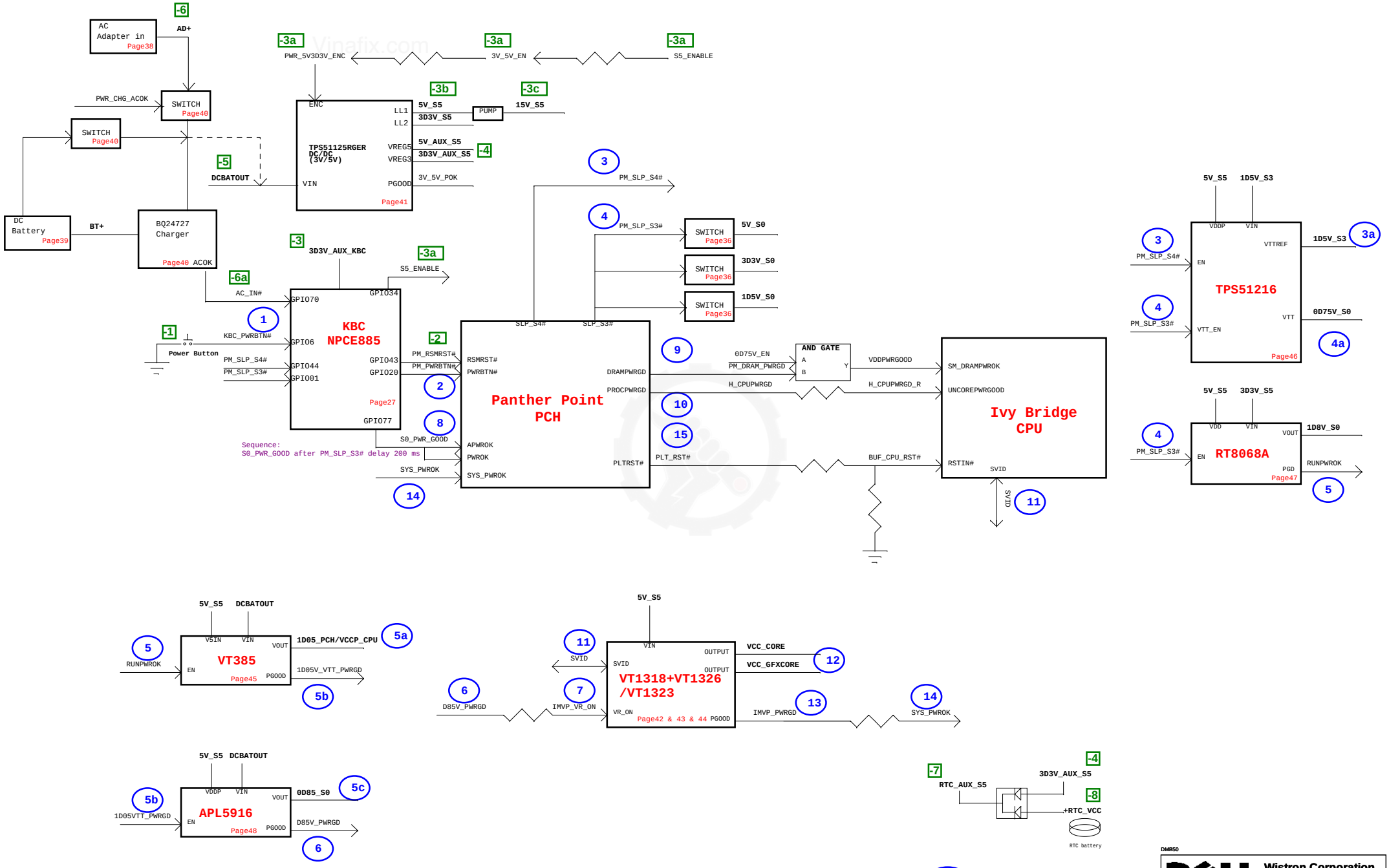
Wistron CHIEF RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15

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Title: *Power Sequence Diagram*

Size	Document Number	Rev
A2	*BMW Z5 DIS*	*A00*

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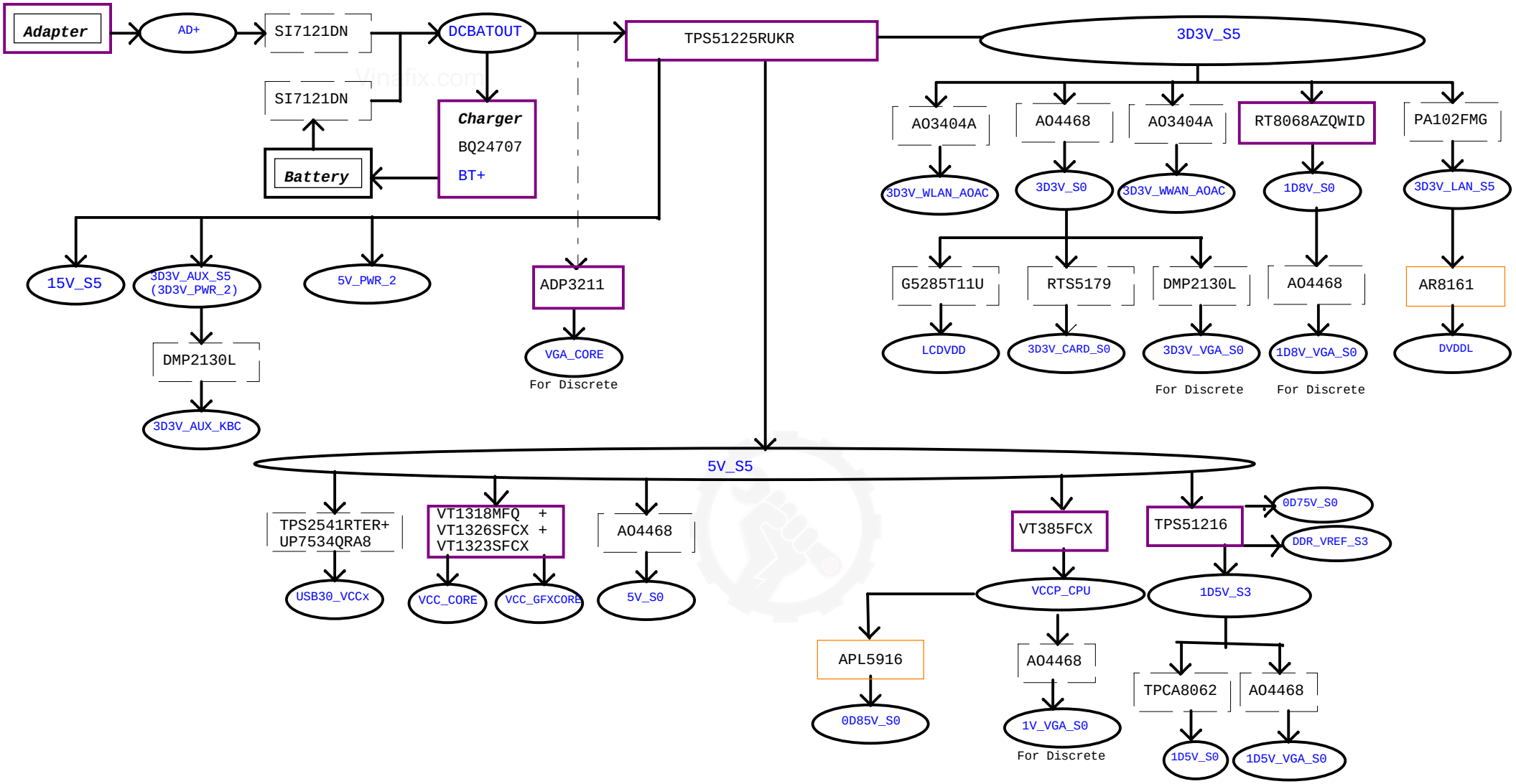

Power Shape

Regulator	LDO	Switch

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Title: **Power Block Diagram**

Size	Document Number	Rev
A3	BMW Z5 DIS	A00

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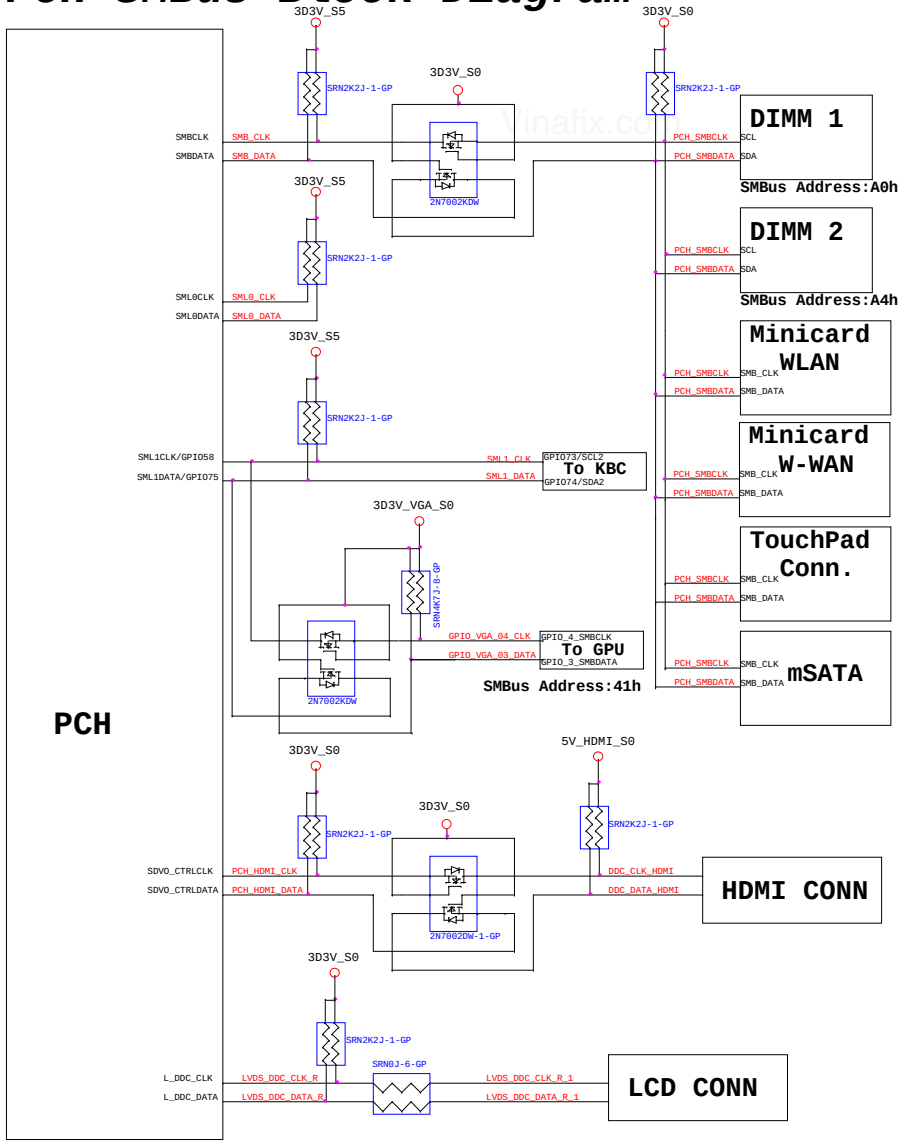
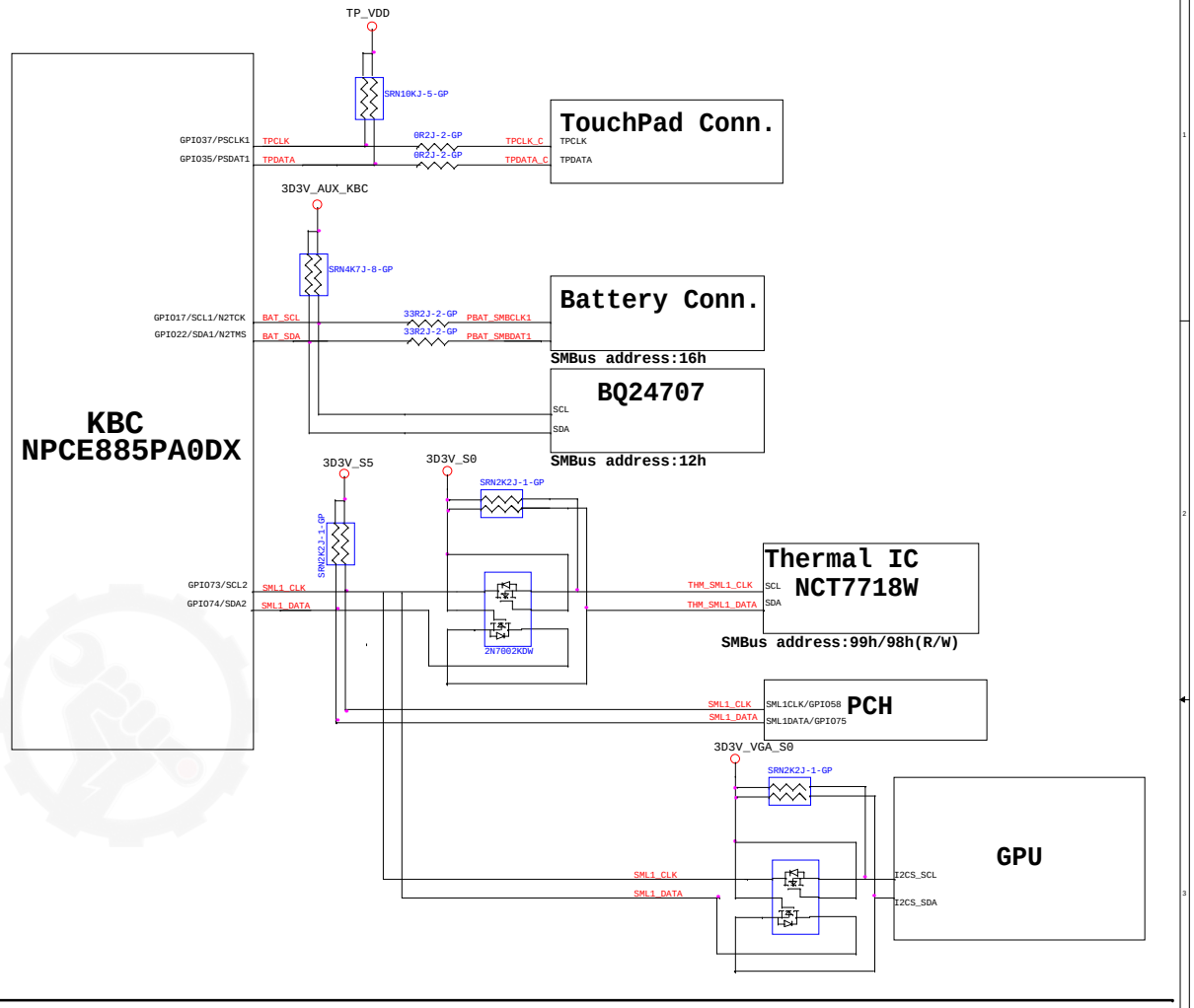
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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A2	BMW Z5 DIS	A00

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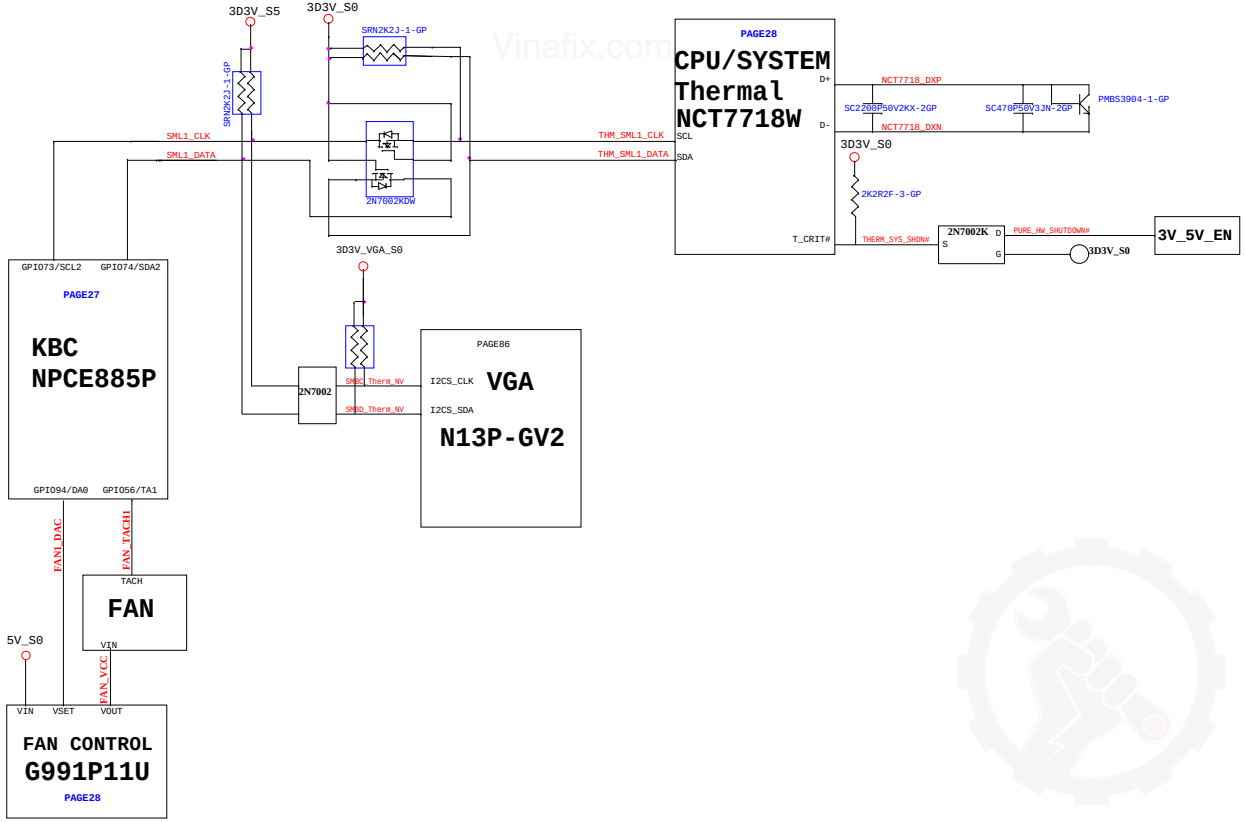
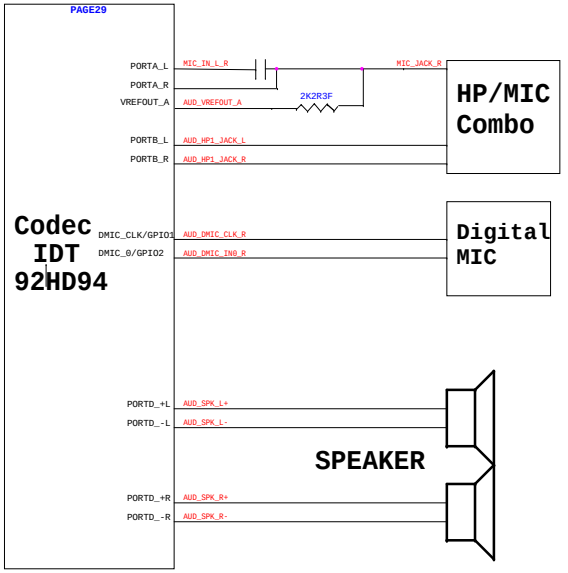
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
A2	BMW Z5 DIS	A00

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DATA	PAGE	Change Iteam	Owner
3/30	39	DY R3901, Stuff BATSW1 For PT Build	EE
	27	Change R2724 to 20KΩ For PT Build	EE
	71	DY RN7101,R7101,R7102,R7103,DB1 For PT Build	EE
	69	Change R6909 Type to 0603 Prevent not enough power	EE
4/9	49	Change U4901 to 74.06288.B7F Sourcer provide	EE
4/12	49	LCD1 chanage to 20.F2101.030 By ME	ME
	59	RJ45 change to 68.IH601.301 By ME	ME
	66	USB2 change to 22.10341.A81 By ME	ME
	97	H3 change to ZZ.00PAD.921 By ME	ME
	97	Add H12 , H13 to ZZ.00PAD.921 By ME	ME
	97	Add SPR1 to 34.43E24.001 By ME	ME
	8	Del C845, C849, C843, C821, C846, C848, C831 Avoid Through Gole	EE
4/13	27	R2713 change to 64.10025.6DL from 64.1002D.6DL For 0.1% ==> 1%	ME
4/17	31	Change Q3106 from 84.00102.031 to 84.02130.031 Merge source.	EE
	62	Change TC6201,TC6303 to 78.10710.52L By EMC	EMC
	18	Change C1801 to 78.10491.4FL Merge source	EE
	82	C8201=EC8201 , C8202=EC8202 By EMC	EMC
	97	Add EC9701,EC9702,EC9703,EC9704 By EMC	EMC
	56	Add TP5601,TP5602,TP5603 By EMC	EMC
	41	Change PT4101,PT4103 to 77.52271.09L By EMC	EMC
	41	EC4119=PC4119 By EMC	EMC
	58	Change EC5801 to 83.00402.0A0 By EMC	EMC
	42	Change PC4211 to 78.10523.5FL For Merge Source	EE
	46	Change PC4620 to 79.47719.2BL For Merge Source	EE
	58	Change to SPK1 to 20.F1639.004 By ME	ME
4/18	41	Change PT4101,PT4103 to 77.22271.27L By EMC	EMC
	45	Change U4501 to 74.00386.03Z By Power team	Power
	65	Change R6510 PH to 3D3V_S5 , Change R6613 PH to 3D3V_AUX_KBC Prevent Leackage	EE
4/20	51	Add ER5101,ER5102,ER5103,ER5104 By EMC	EMC
	29	C2937 C2938 C2939 C2950 C2951 C6501 C8432 C8434 Change to 78.10620.51L For Merge Source	EE
4/23	82	Change TPAN1 to 20.F1876.006 By ME	ME
4/24	45	1.05v :ADD GAP EG4527, EG4529, EG4528, EG4525, EG4522 By EMC	EMC
	43	CPU::ADD GAP EG4301, EG4302, EG4303,,EG4304, EG4305, EG4306, EG4307 By EMC	EMC
	44	GFX: ADD GAP EG4401, EG4402, EG4403, EG4404, EG4405, EG4406, EG4407 By EMC	EMC

DATA	PAGE	Change Iteam	
	40	CHARGER :ADD GAP EG4010, EG4011, EG4012, EG4013 By EMC	EMC
	41	PR4103 33KR2F-GP change to 35K7R2F-L-GP (64.35725.L0L)By Power team	Power
	41	PR4102 120k change to 100KR2F-L2-GP(64.10035.L1L) By Power team	Power
	92	PR9238=196k ohm , PR9225=2.26k ohm By Power team	Power
	92	PU9204, PU9205=SIR166DP-T1-GE3-GP(84.00166.037) By Power team	Power
	47	Del EG4701,EG4702,EG4703,EG4704,EG4705,EG4706,EG4707 By EMC	EMC
	49	Swap LVDS1 signals for change LVDS1 CONN For correct Net	EE
4/25	59	Add XF5901 2nd source 68.69241.30C By EMC	EMC
	42	1) change PR4236=953-->1.3kohm for VCC LL 2) change PR4239=300-->412ohm for VCCAXG LL By Power team	Power
4/26	92	PR9225 change to 64.24915.6DL By Power team	Power
	59	Change C5902 to 78.1013N.14L By Power team	Power
	39.40	Change EG4010,EG4011,EG4012,EG4013 Location to EG3910,EG3911,EG3912,EG3913 By EMC	EMC
	39	Add EG3914,EG3915 By EMC	EMC
4/27	45	Del EG4529 By EMC	EMC
	40	Change PC4019 to BT+_G By EMC	EMC
	39	Change AFTP3905 to BT+_G By EMC	EMC
	92	Change PR9238 to 0603 size By Power team	Power
4/30	60	RTC1 change to 62.70001.061 By ME	ME
	49	LCD1 change to 20.F2101.030 By ME	ME
	70	LIDSW1 change to 74.05712.0BB By ME	ME
	97	Add EC9705 to 78.10422.5FL By EMC	EMC
5/3	49	Delete EC4915 By EMC	EMC
5/4	28	Change FAN1 to 20.F1295.003 By ME	ME
	47	Change PL4701 to 68.1R550.20F By Power team	Power
	56	Add TP5601,TP5602,TP5603 For Layout	EE
5/8	62,63,82	Change and Stuff TR6301,TR6204,TR8201,TR8202 1st 68.00201.241 , 2nd 69.10084.081 By EMC	EMC
	82	Change EC8202 to 78.10423.2FL By EMC	EMC
	97	Stuff EC9701,EC9702,EC9703,EC9704,EC9705 By EMC	EMC
	49	Change and Stuff TR4902 1st 69.10084.071 , 2rd 69.10080.021 By EMC	EMC

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Title: Change History

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DATA	PAGE	Change Iteam	Version
5/19	82	Change EC8202 P/N to 78.10421.2BL for correction Footprint	EE
6/05	27	Change R2724 P/N to 64.33025.6DL for correction PCB VERSION	EE
6/11		Change PR3801,R2301,R2304,R2412,R2702,R2940,R4912,R6606,R6607, R8204 to 0603 short pad	EE
6/11		Change PR4022,PR4116,PR4127,PR4130,PR4133,PR4207,PR4212,PR4219, PR4223,PR4228,PR4250,PR4251,PR4252,PR4253,PR4254,PR4261,PR4510, PR4511,PR4522,PR4523,PR4607,PR4702,PR4801,PR4803,R1404,R1405, R1503,R1505,R1823,R1916,R1921,R1924,R1925,R1927,R1929,R2136,R2205, R2306,R2307,R2308,R2402,R2403,R2404,R2720,R2723,R2727,R2728,R2733, R2764,R2765,R2767,R2768,R2778,R2792,R2794,R2807,R2813,R3113,R3614, R3710,R4914,R4915,R504,R5125,R6202,R6203,R6204,R6205,R6281,R6282, R6283,R6284,R6305,R6306,R6307,R6308,R6502,R6505,R6616,R6810,R812, R909 to 0402 short pad	EE
6/11	29	Change R2935 to 0805 short pad	EE
6/11	20	Change RN2012 to 0402 short pad R2001,R2002. Change RN2014 to 0402 short pad R2012,R2014. Change RN2017 to 0402 short pad R2016,R2017.	EE
6/13	49	Change TR4902 to 69.10103.041 For Layout, Keep NO swap components so change orignal one	EE
	62,63	Change TR6204,TR6301 to 69.10080.021 For Layout, Keep NO swap components so change orignal one	EE
	20	Change R2001,R2002 to RN2012, 4P2R short pad	EE
	20	Change R2012,R2014 to RN2014, 4P2R short pad	EE
6/15	49	Change TR4902 to 1st 69.10080.021 , 2nd 69.10103.041	EE
	31	Add C3111 , Prevent PLT_RST#_LAN rise time fail.	EE
	69	Change Net Rule KB_BL_CTRL# to 20 mils	EE
		Common Part change 78.10321.2FL --> 78.10324.2FL 78.10423.2FL --> 78.10421.2FL 78.10523.5BL --> 78.10521.2BL 84.2N702.031 --> 84.07002.I31 84.DM601.03F --> 84.2N702.E3F	EE
6/19	27	Add R2793 for new NETNAME KBC_BKLT connect to D4902.2	EE
	49	Move L_BKLT_CTRL to D4902.1	EE
	49	Add D4902 and R4905. Add a new NETNAME BKLT_CTRL to replace L_BKLT_CTRL	EE
	97	Add EC9706	EMC
6/20	14,15	C1514 -->EC1514 C1424 -->EC1424 C1421 -->EC1421 Follow EMC request	EMC
6/21	49	Change U4901 to 74.05285.07F.Prevent LG Falling time Fail.	EE
		Change C4901 to EC4915.	EMC

DATA	PAGE	Change Iteam	
	92	PL9201 change to 68.R2210.10N For 3mm H	Power
		TPAD1 and LEDBD1 Change to 20.K0320.006 Follow Connector List	ME
6/22	48	Change PU4801 to 74.05916.A31 for Reversion changed.	Power
		Delete TR8203,TR5101,TR5102,TR5104,TR5103,TR6501, TR6601.Follow PSE recommand.	EMC
6/25	62,63	Delete TR6205,TR6206,TR6302,TR6303.Follow PSE recommand.	EMC
	62,63	Delete R6279,R6280,R6303,R6304,R4903,R4906,TR8204,ER8201, ER8202,ER8203,ER8204.Follow PSE recommand.	EMC
	29	Add R2902,D2902 may replace by R2902	EE
	69	Delete C6906 For new NET NAME	EE
	69	KB_LED_DET_C change to 20mil.	EE
	69	AFTP78 conect to Q6901.D	EE
	56	Delete TP5601/5602/5603 , because no need.	EE
6/26		Change PR9238 to 174KΩ Change PC9210 to 680pF Change PR4236 to 866Ω Change PC4236 to 47pF Change PC4218 to 1500pF Follow Power Team change	Power
6/28	28	Change U2802 from 74.00991.031 to 74.05606.A71. For 74.00991.031 life cycle status is obsoleted	EE
7/30	69 21 29 49 58 92 93	DY R6912 , R6908 change to short pad. DY R6904, Pop R6905. RN2101 change to short pad 0R8P4R-PAD-1-G R2941 change to short pad R4905 change to short pad R5808 change to short pad PR9226, PR9227, PR9239 change to short pad PR9326 change to short pad	EE
8/3	27	Change R2724 to 47kΩ for A00.	EE
	20	Change R2003 to short pad	EE
8/6	71	Change DB1 to ZZ.00PAD.Y41	EE
		Page40,41,42,43,44,45,46,48,39 Change Pad type, change to green cover type.	EE
		Change ER8207,ER8208 to short pad.	EE
8/8	71	Change R6808,R6811 form 680Ω to 300Ω	EE

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Title: Change History

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DATA	PAGE	Change Iteam	Version

DATA	PAGE	Change Iteam	

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Title
Change History

Size	Document Number	Rev
A3	***BMW Z5 DIS***	***A00***

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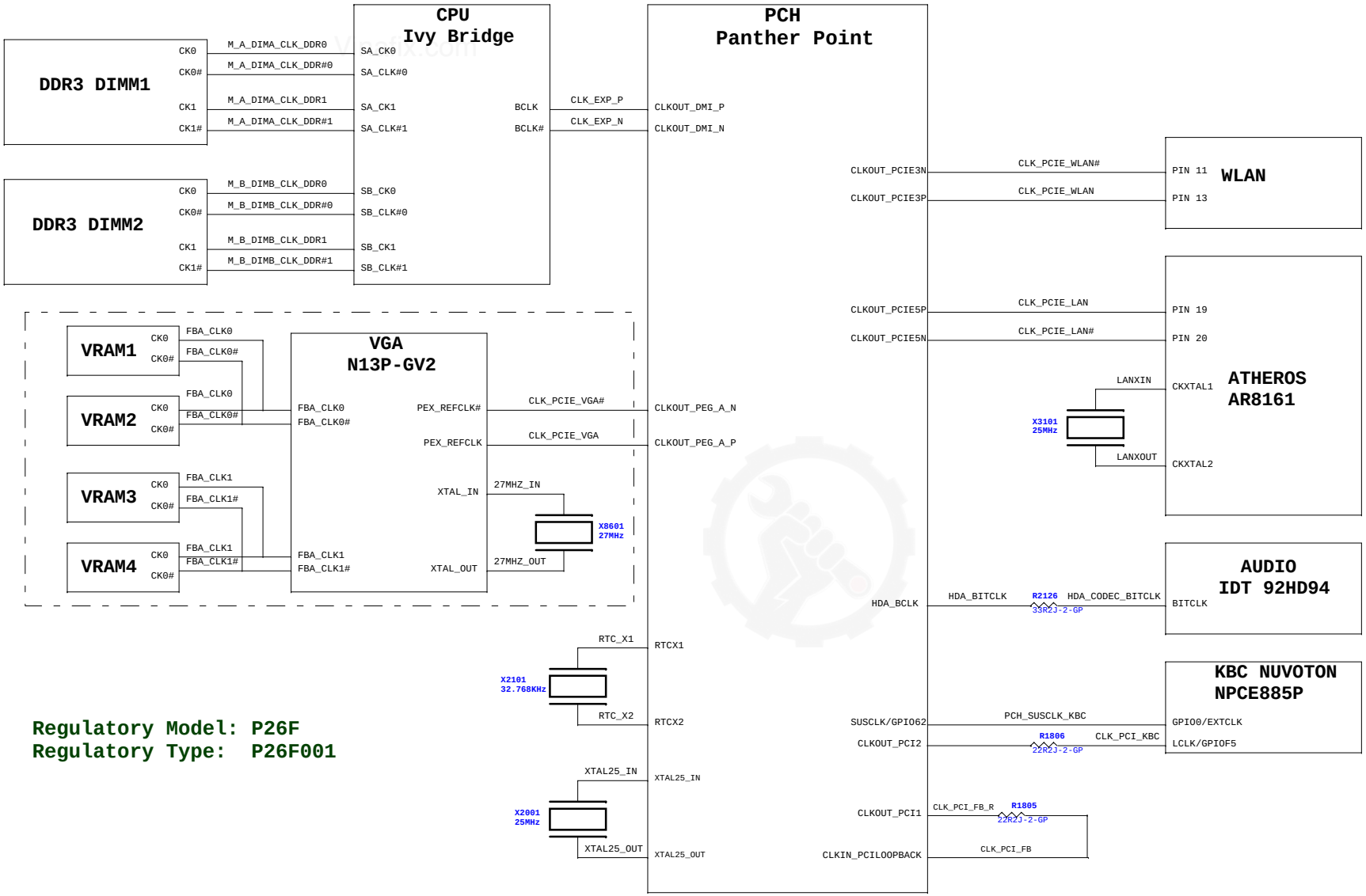
BMW Z5 DIS CLK Block Diagram



Regulatory Model: P26F
Regulatory Type: P26F001

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Title: CLK DIAG

Size	Document Number	Rev
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