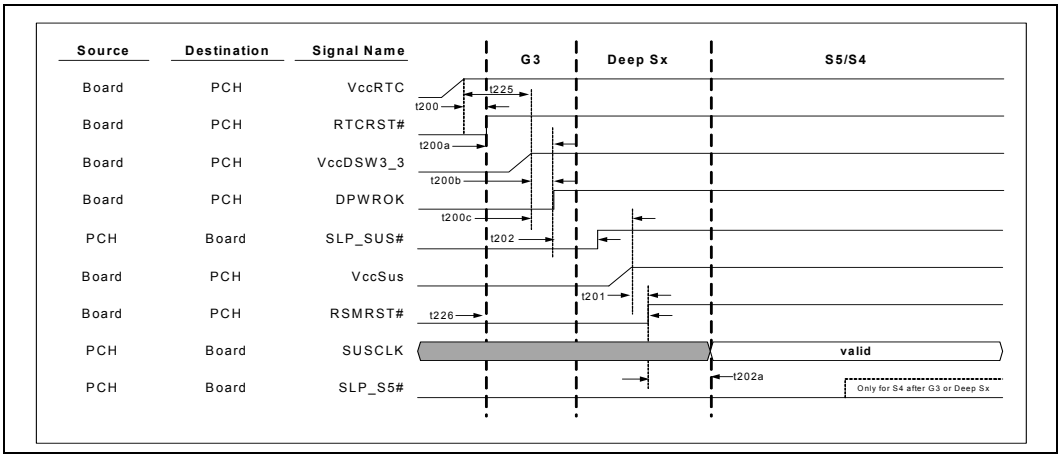
8.8 Power Management Timing Diagrams

Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



Note: VccSus rail ramps up later in comparison to VccDSW3_3 due to assumption that SLP_SUS# is used to control power to VccSus.

Figure 8-2. G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram

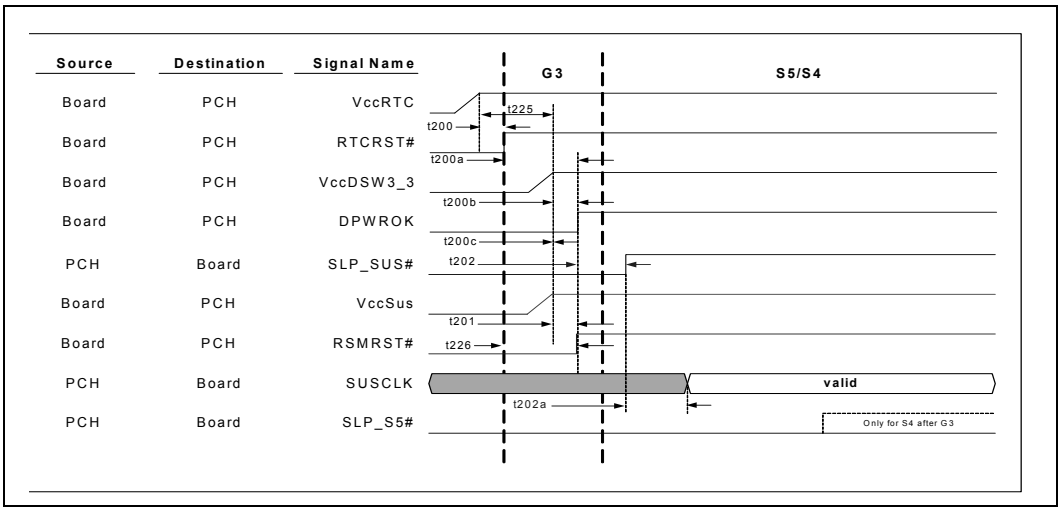
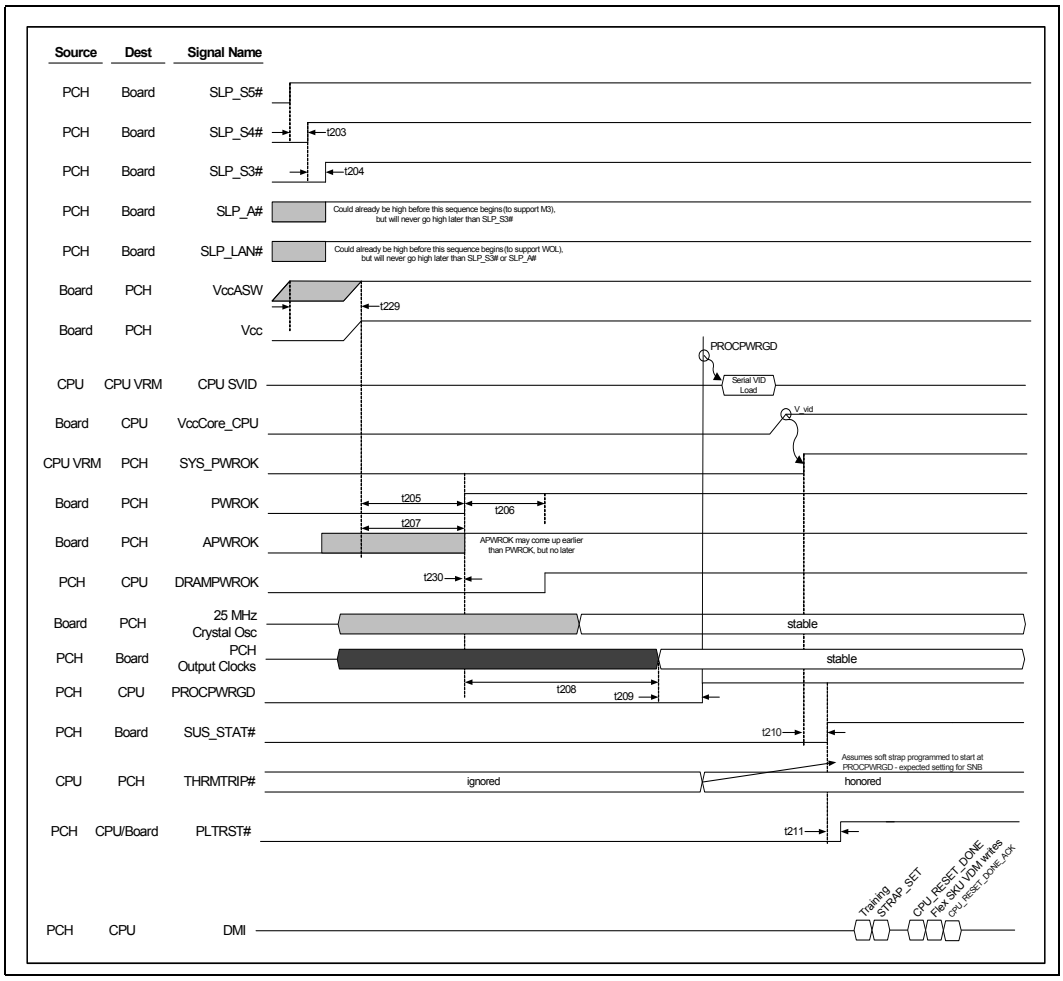


Figure 8-3. S5 to S0 Timing Diagram



INTEL HM7X 时序图

Figure 8-4. S3/M3 to S0 Timing Diagram

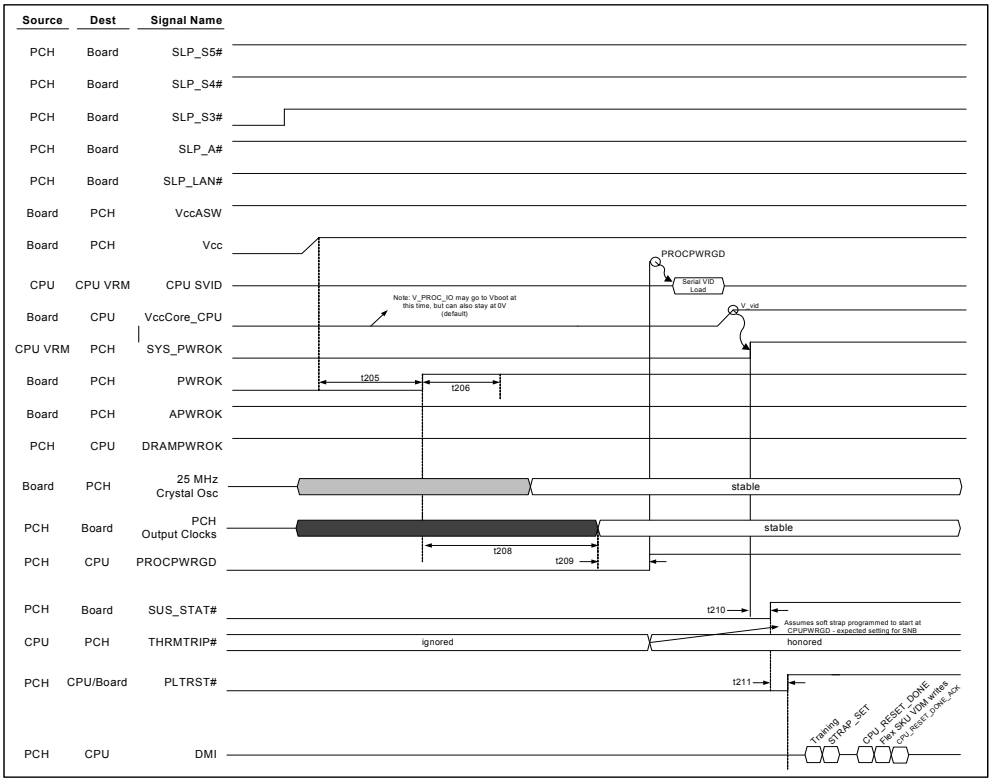


Figure 8-5. S5/Moff - S5/M3 Timing Diagram

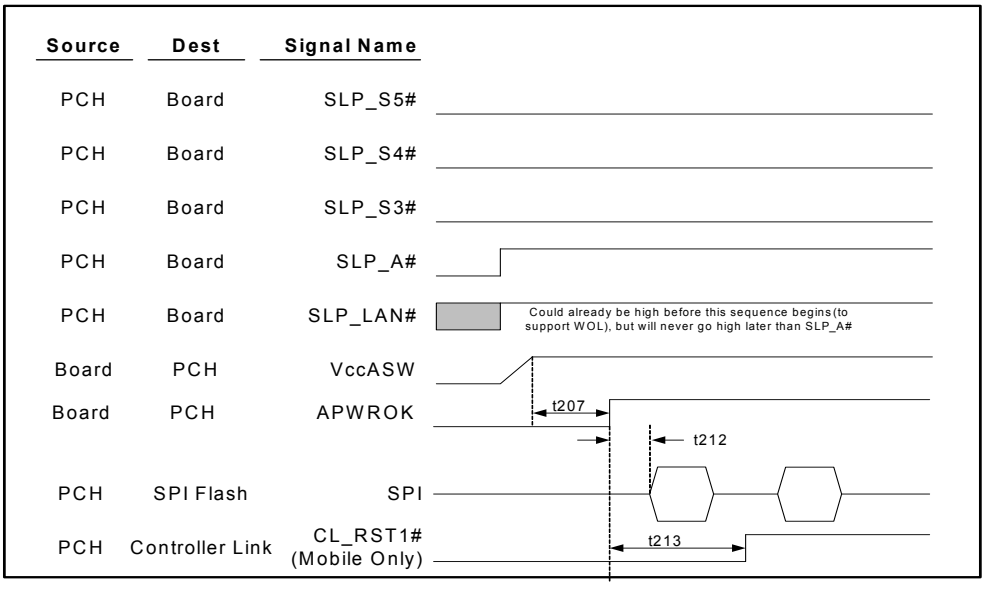


Figure 8-6. S0 to S5 Timing Diagram

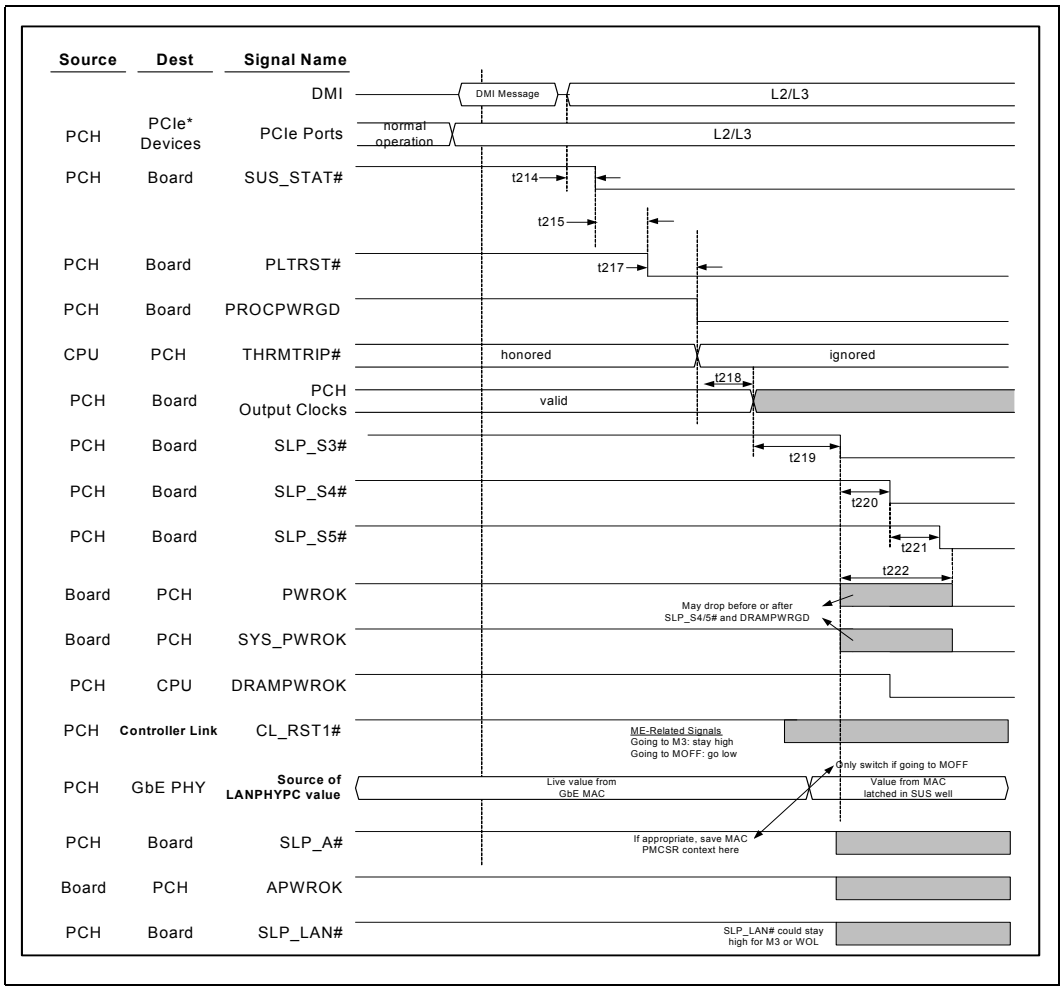


Figure 8-7. S3/S4/S5 to Deep Sx to G3 w/ RTC Loss Timing Diagram

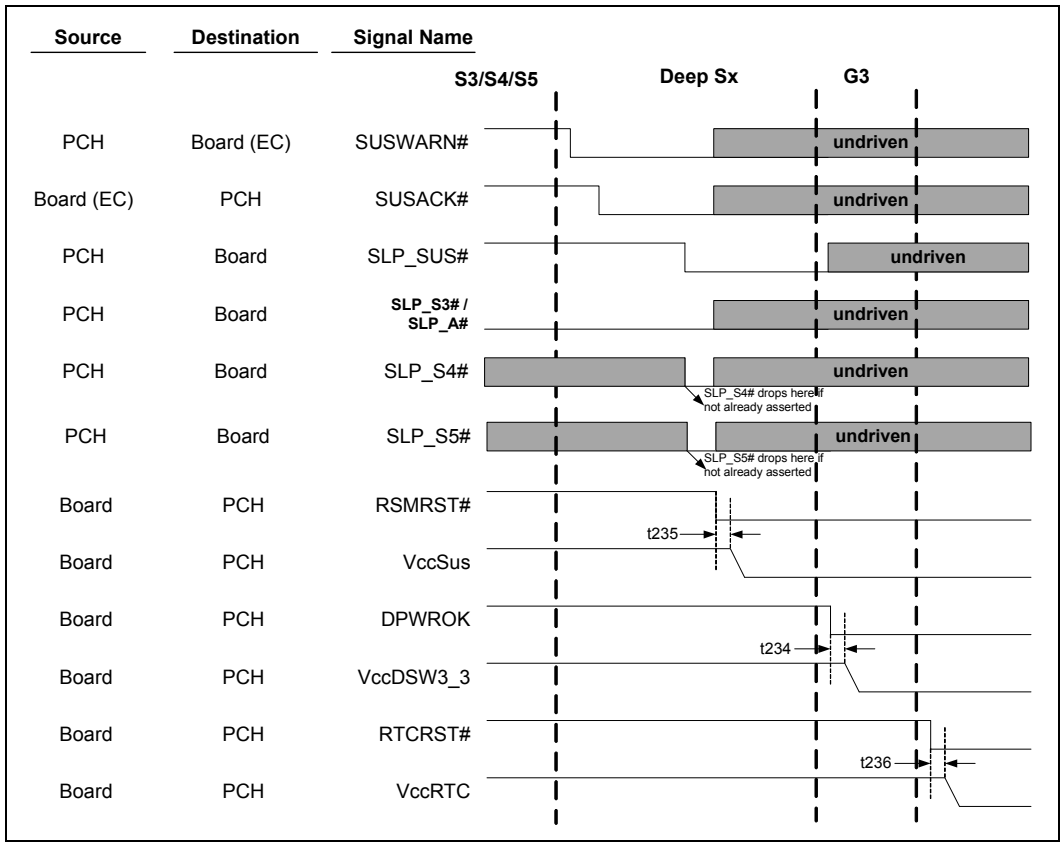


Figure 8-8. DRAMPWROK Timing Diagram