INTEL HM5X 时序图



8.8 Power Management Timing Diagrams

Figure 8-1. G3 w/RTC Loss to S4/S5 Timing Diagram

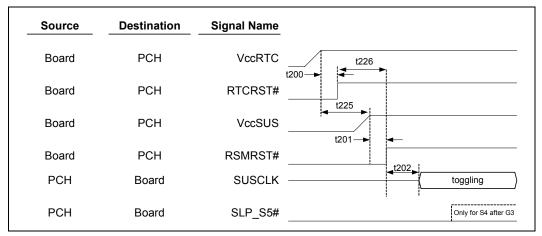
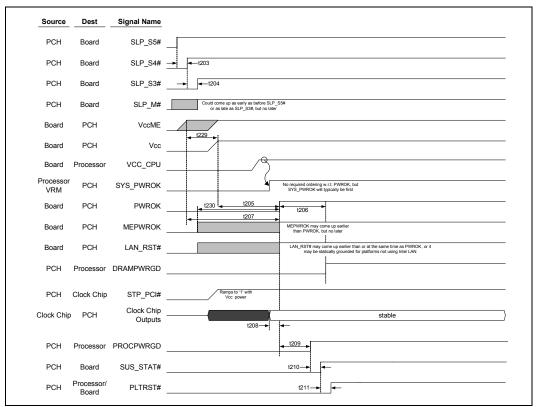


Figure 8-2. S5 to S0 Timing Diagram



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INTEL HM5X 时序图

Figure 8-3. S3/M3 to S0 Timing Diagram

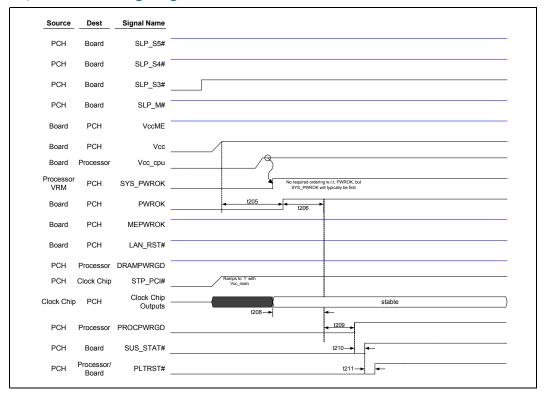
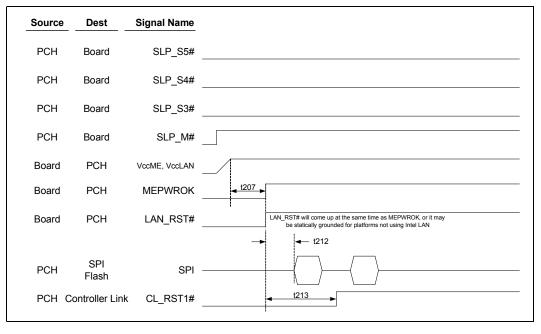


Figure 8-4. S5/Moff - S5/M3 Timing Diagram



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Figure 8-5. S0 to S5 Timing Diagram

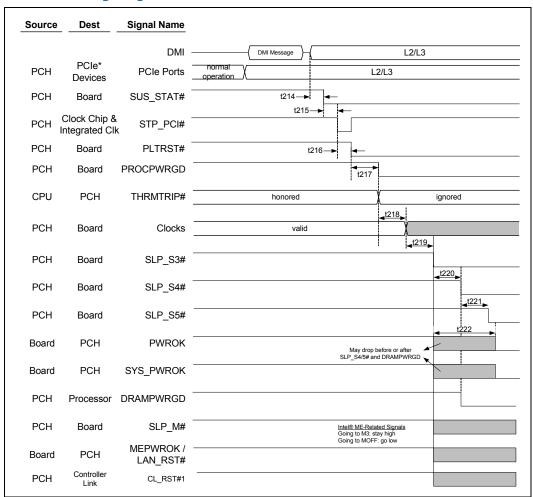
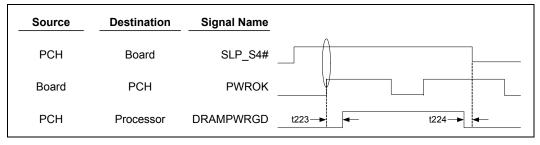


Figure 8-6. DRAMPWRGD Timing Diagram



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