NAP00 Power On Sequence XDP_DBRESET# ON/OFFBTN# (From EC to TCH) SYSON (From EC to control +1.5V) +V_DDR3_DIMM_REF **DGPU Power Sequence** SUSP# (From EC to control VS Power) +3VS_DELAY +VGA CORE +1.8VSDGPU +1.5VS_DGPU DGPU PWR EN (From ICH to control DGPU Power) ONLY FOR DGPU _ +1.8VSDGPU +1.5VS_DGPU +1.05VSDGPU PEG_RST# +1.8V +VCCP VGATE (From IMVP to ICH & EC) PM_PWROK (From EC to ICH) PLT_RST#_BUFF (From ICH to CPU) H_RESET# (Output from CPU) Security Classification Compal Secret Data Compal Electronics, Inc. Issued Date Deciphered Date **Power Sequence** THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMMA. ELECTRONICS, NO. AND CONTAINS COMPIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET HAN TO BE TRANSFERSED FIND HE HAD EXPORTED TO SHE ON ONE PROPRIETATION DISCOVERY OF THE COMPINENT DISCOVERY OF THE CONTAINS HE SHEET NOT THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PROP WRITTEN CONSENSITY OF COMPILE LECTRONICS, INC. LA-5811P