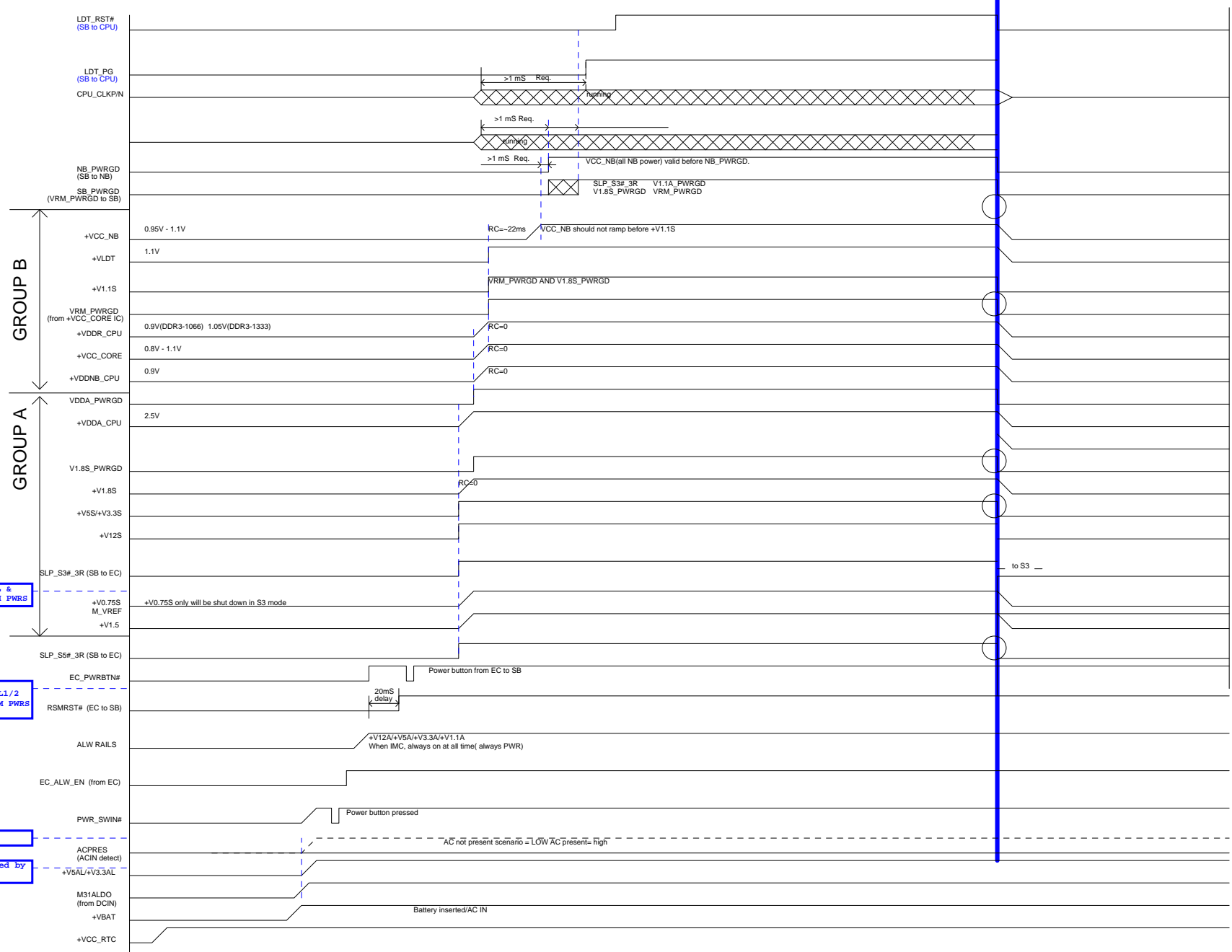




GROUP B

GROUP A



CPU MEM CTL & DDR3 SODIMM PWRS

CPU\_THM/SB/SB\_SCL1/2  
SB\_KB/SPI/LPC ROM PWRS

KBC is ready

KBC is powered by +V3.3AL

**Power on Sequence required:**

**SB820:**

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

**RS880M:**

- 1, 0 <(+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC\_NB