

COMPAL CONFIDENTIAL

MODEL NAME : LOKI N3V3 KBL UMA

PCB NO : DA60022P010

BOM P/N : 431AET31L01~L10&L51~L57

KBL-U & R + MEC1416 board 2018-11-06

REV : 1.0 (A00)

PCB R1

ZZZ
DA60022P010
PCBR1@
PCB 2E1 LA-G714P REV1 M/B 5

DAZ R1

ZZZ
DAZ2E100200
DAZR1@
PCB EDI72 LA-G714P LS-F112P/F114P/F117P

DAZ R3

ZZZ
DAZ2E100201
DAZR3@
PCB EDI72 LA-G714P LS-F112P GOLD A31

X4E#

ZZZ
X4EAET31L51
100@X4E@
SMT EMC N3 KBL UMA EE AG714 EDI73

X4E#

ZZZ
X4EAET31L01
1000@X4E@
SMT EMC N3V3 KBL UMA EE AG714 EDI72

KBL R3

UC1
SA0000A377L
i5KBLU_R3@
S IC FJ8067702739739 SR342 H0 2.5G A311

UC1
SA0000BLD1L
i3KBLU42_SMB0_R3@
S IC FJ8067703282620 SR3LD Y0 2.3G A311

UC1
SA0000BYB1L
i3KBLU23_SMB0_R3@
S IC FH8067703037315 SR3N6 J1 2.3G A311

UC1
SA0000A346L
i7KBLU_R3@
S IC FJ8067702739740 SR341 H0 2.7G A311

UC1
SA0000ADL3L
KBLU_Celeron_R3@
S IC FJ8067702739933 SR349 H0 1.8G A311

UC1
SA0000ADV3L
KBLU_Pentium_R3@
S IC FJ8067702739932 SR348 H0 2.3G A311

UC1
SA0000BKN3L
i3KBLR_R3@
S IC FJ8067703282221 SR3W0 Y0 2.2G A311

UC1
SA0000AWB3L
i5KBLR_R3@
S IC FJ8067703282221 SR3LE Y0 1.8G A311

UC1
SA0000AWC2L
i7KBLR_R3@
S IC FJ806770281816 SR3LC Y0 1.8G A311

UC1
SA0000BLH1L
i3KBLU22_SMB0_R3@
S IC FJ8067702739769 SR3TK H0 2.3G A311

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
EC@ : EC
JP@/PIP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
MODS@ : Modern Standby

Layout Dell logo



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REV: X00
PWB: 9HTP8

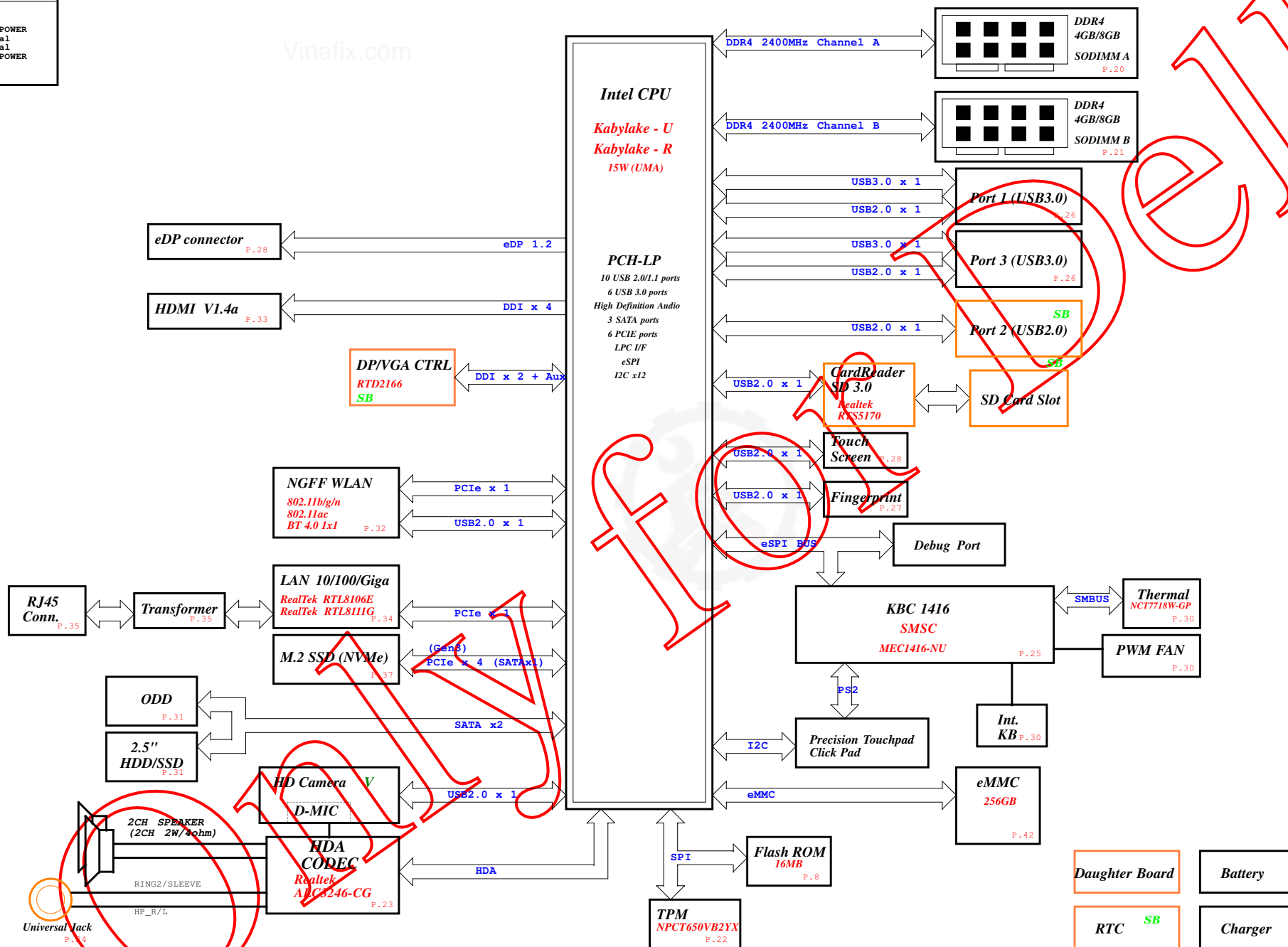
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PCB Stack

1.0mm/6L

L1:TOP
L2:GND/POWER
L3:Signal
L4:Signal
L5:GND/POWER
L6:BOT

Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB2.0 Port1
2	USB2.0 Port2 , IO/B
3	USB2.0 Port3
4	NC
5	CCD
6	Card Reader IO/B
7	BT
8	Touch Screen
9	Finger Printer
10	NC

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 Port1
USB3.0-2			NC
USB3.0-3			USB3.0 Port3
USB3.0-4			NC
USB3.0-5	PCIE-1		NC
USB3.0-6	PCIE-2		NC
	PCIE-3		NC
	PCIE-4		NC
	PCIE-5		10/100M LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

PM TABLE

<div>power plane</div> <div>State</div>	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

Board ID table

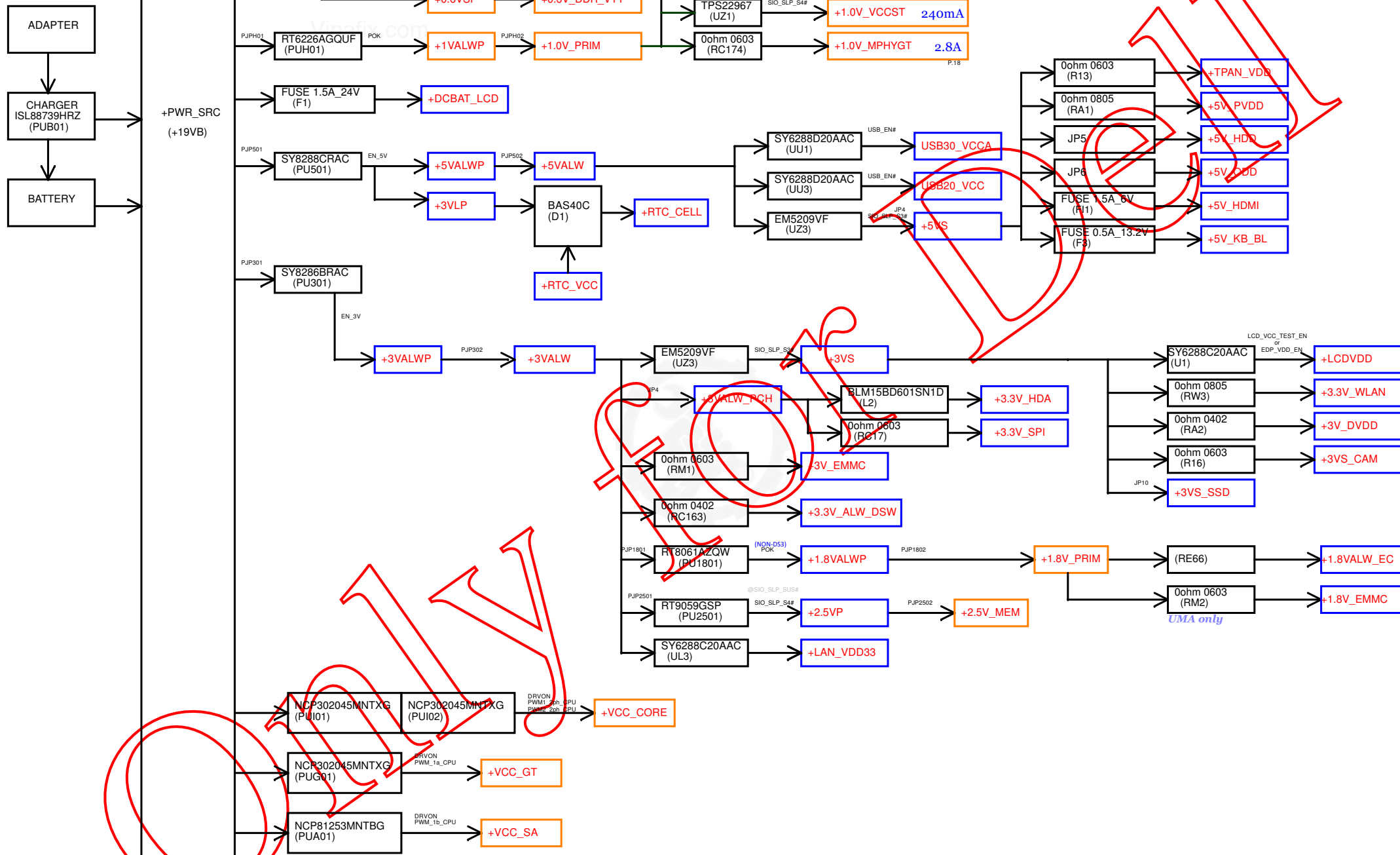
Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	EVT
2	100	17.8K	2.801	DVT1
3	100	27K	2.598	DVT2
4	100	37.4K	2.402	
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	
11	100	TBD	0.9	
12	100	TBD	0.7	
13	100	TBD	0.5	
14	100	TBD	0.3	

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

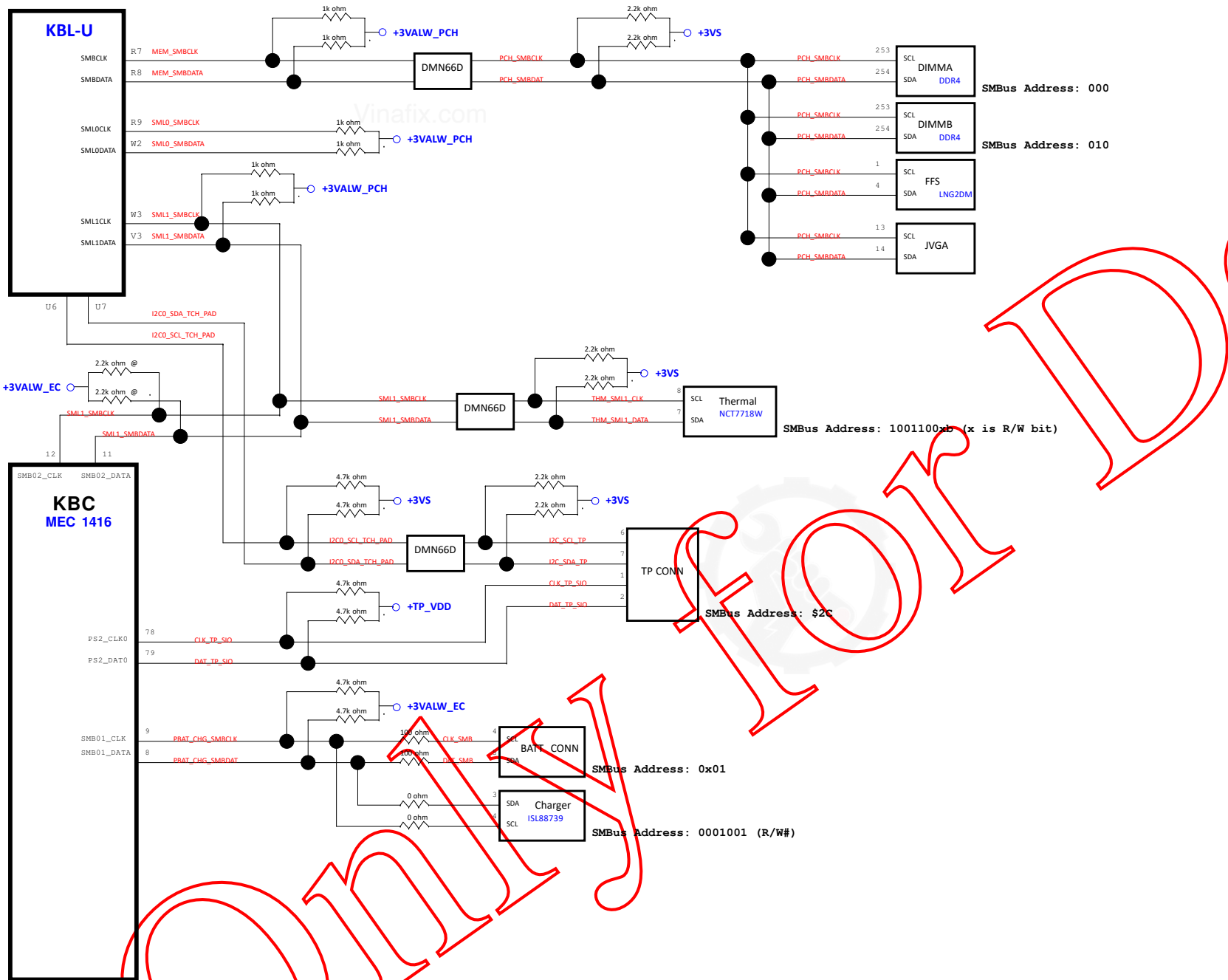
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CPU PWR
Peripheral Device PWR



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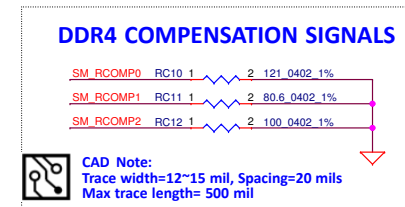


1

Main Func = CPU

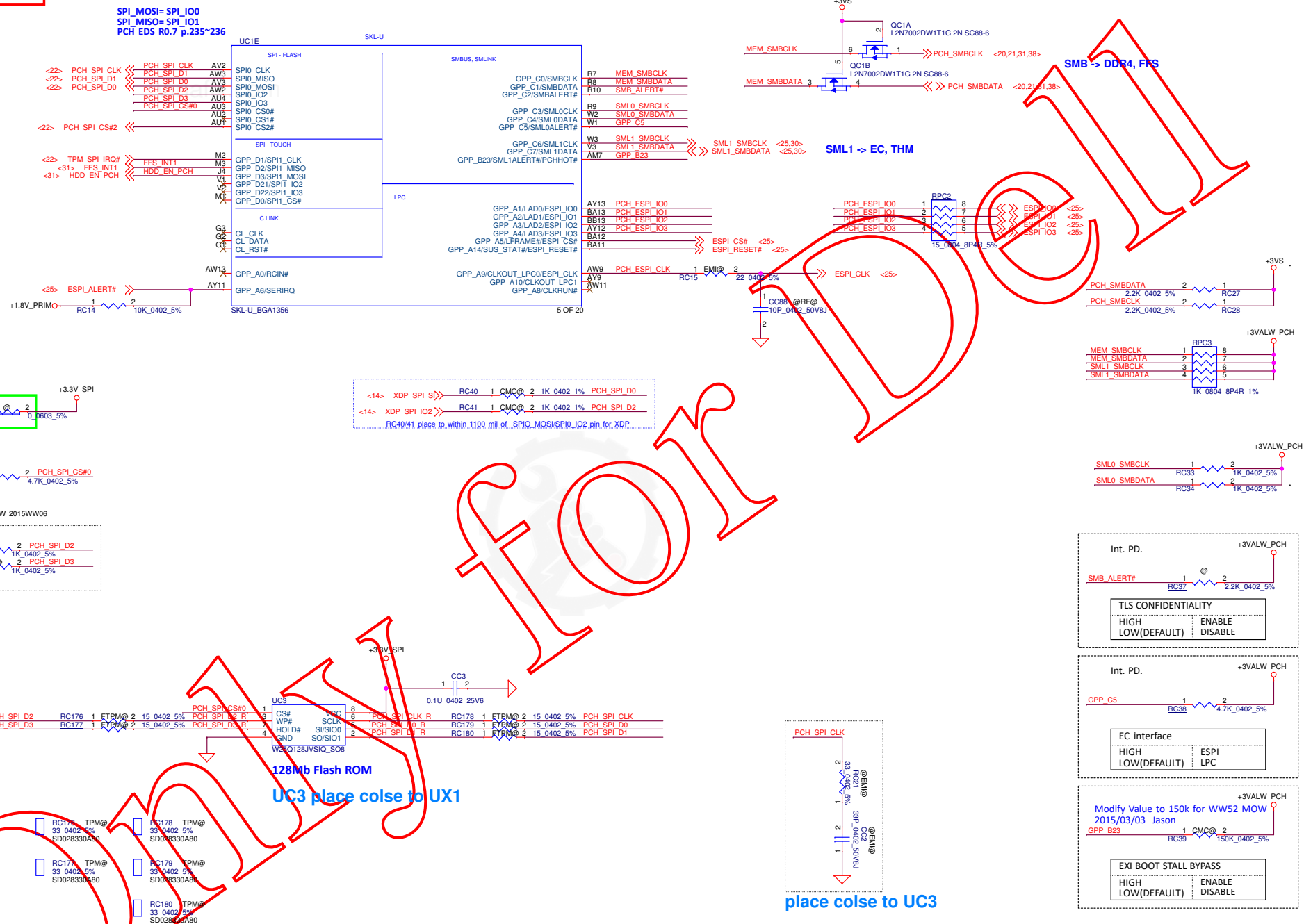


DDR4 Interleaved Memory



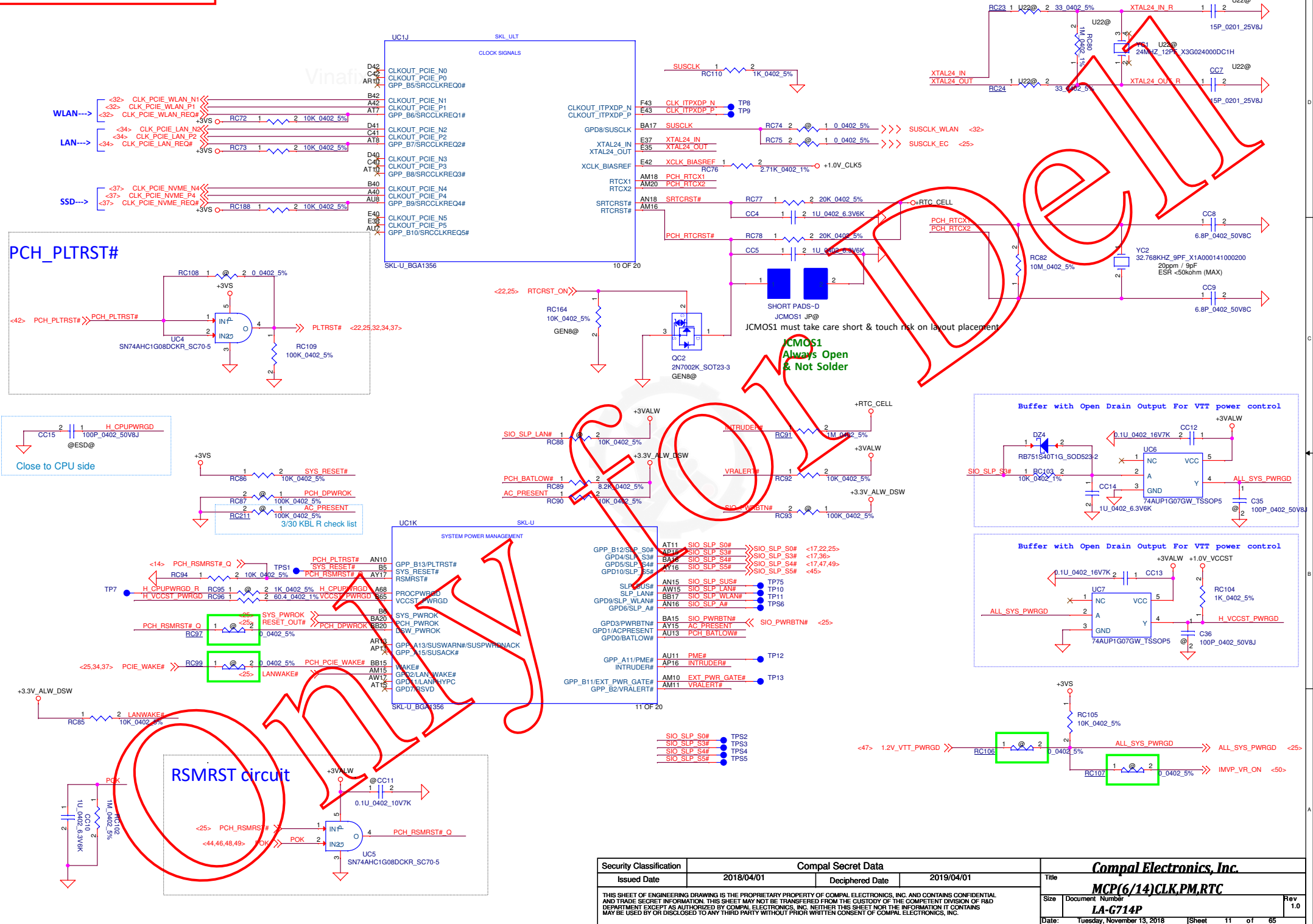
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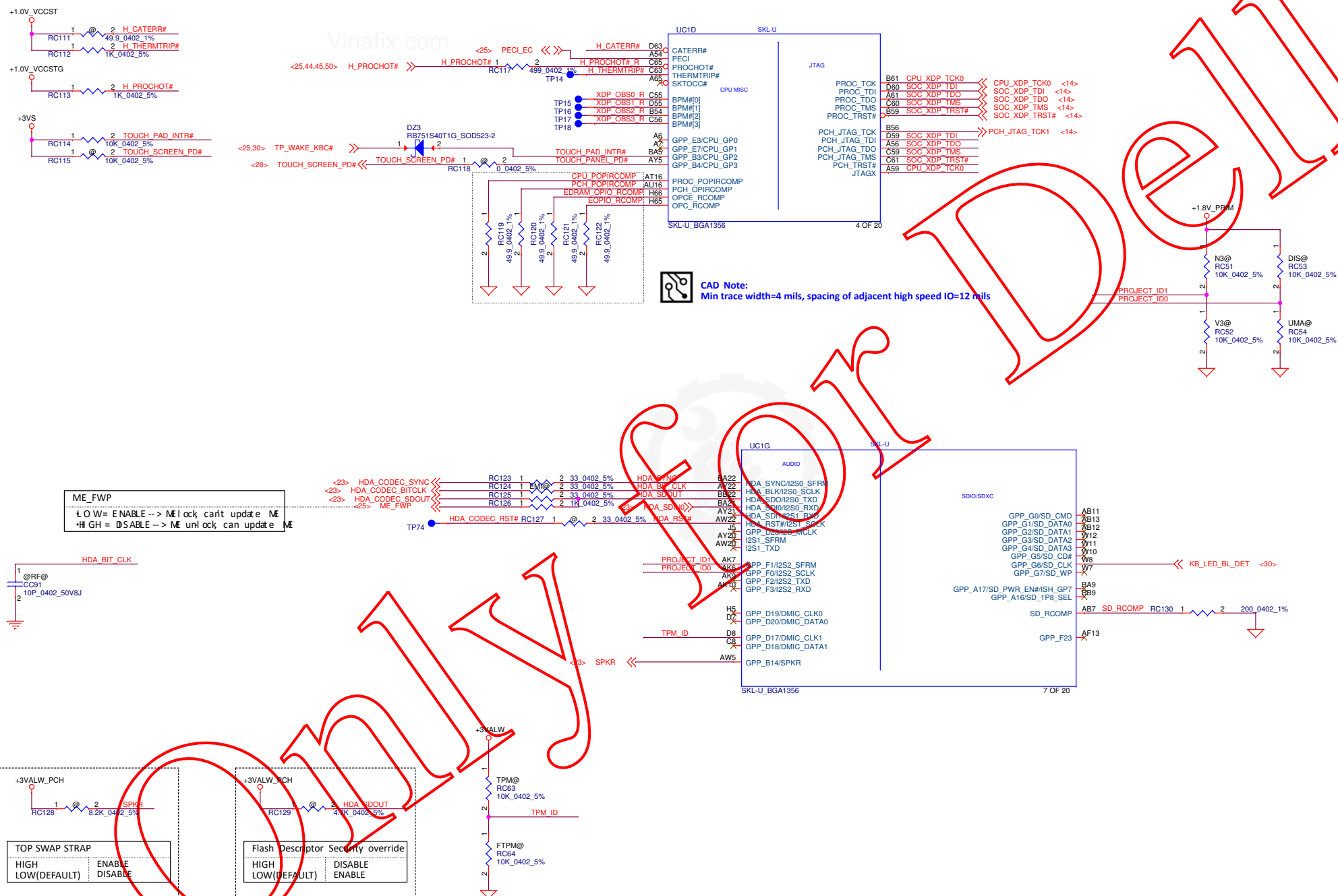


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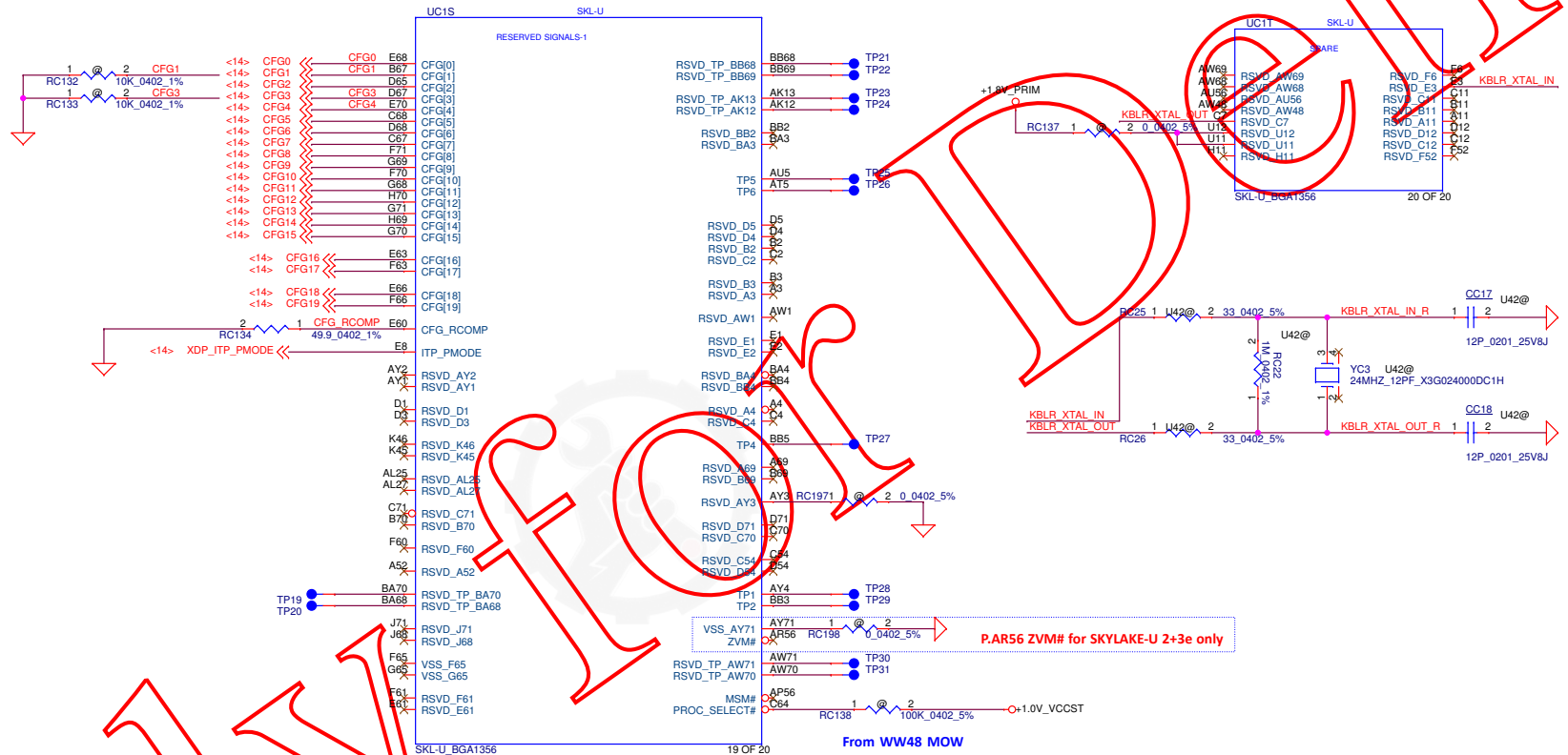
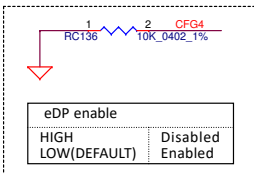
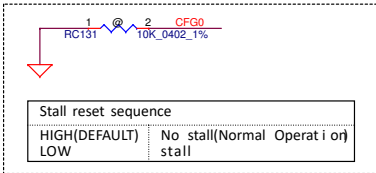
Main Func = CPU



Main Func = CPU



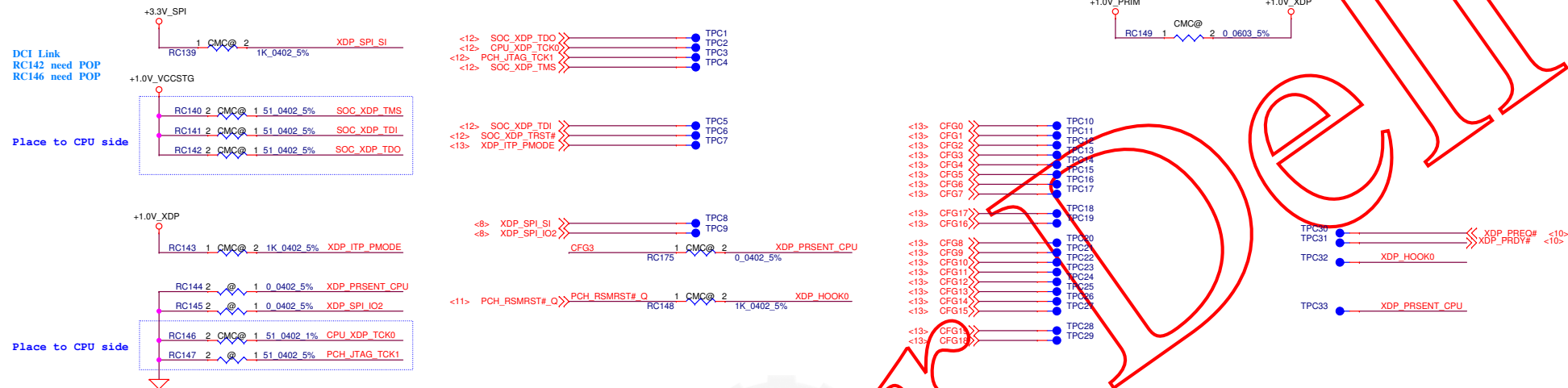
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Connector Less Routing Topology

Vinafix.com

PRIMARY CMC CONN



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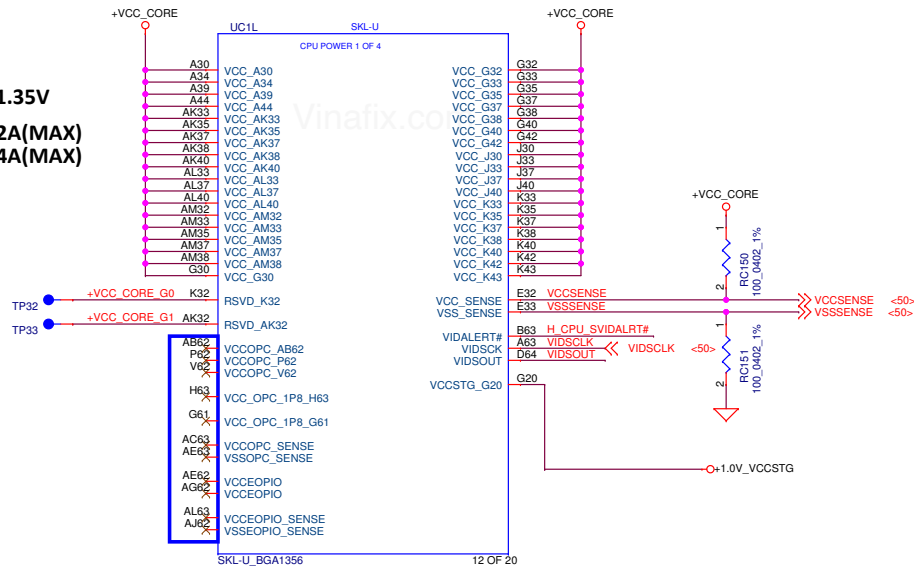
Main Func = CPU

+VCC_CORE: 0.3~1.35V

+VCC_CORE(U22): 32A(MAX)

+VCC_CORE(U42): 64A(MAX)

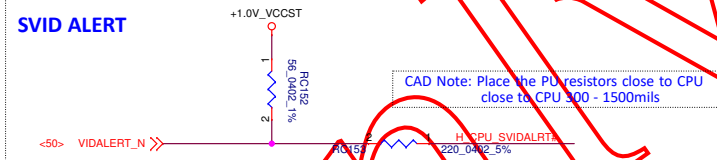
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



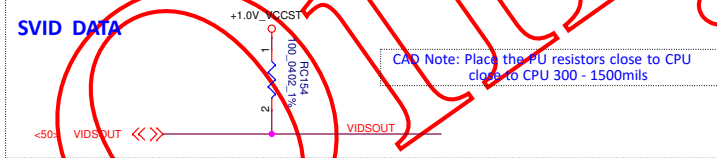
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

SVID ALERT



SVID DATA

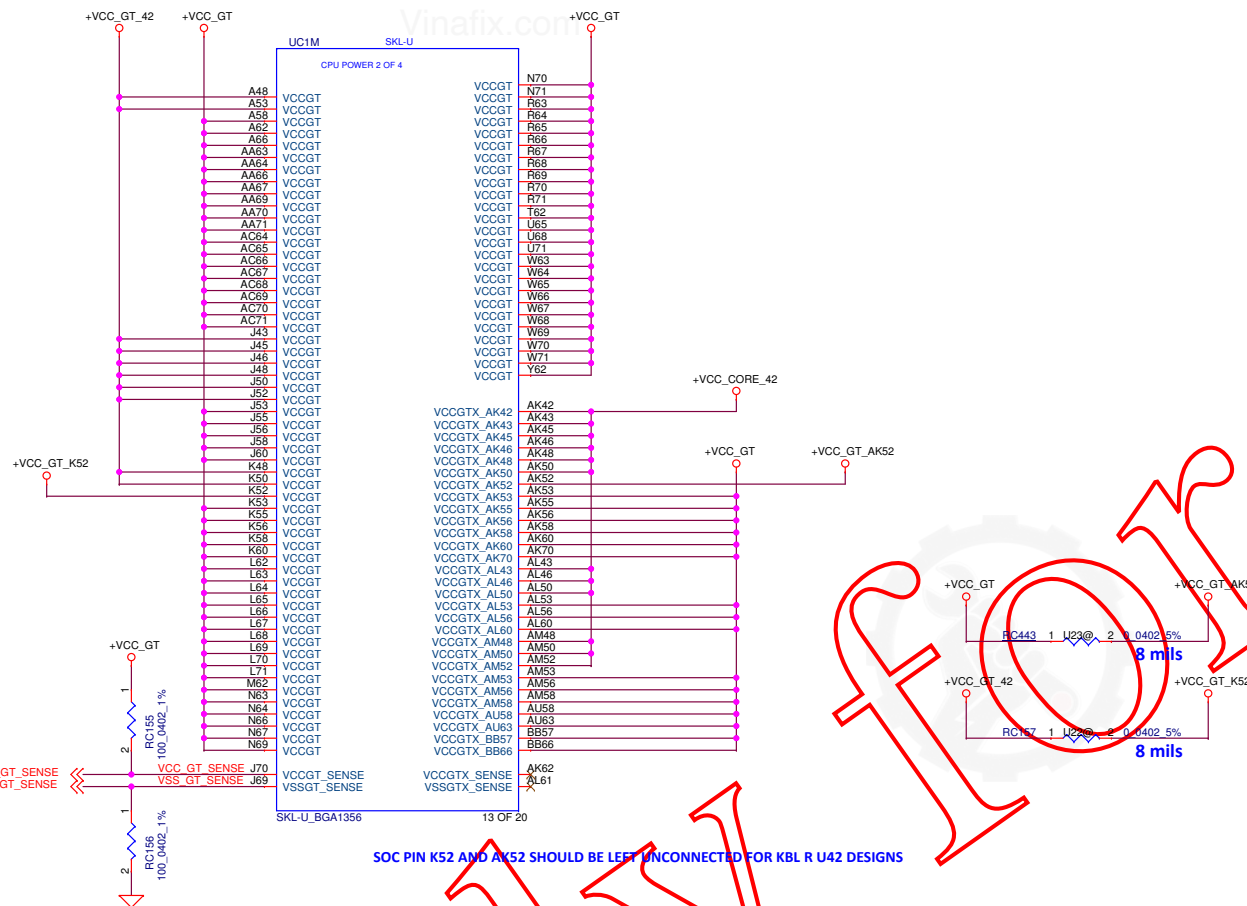


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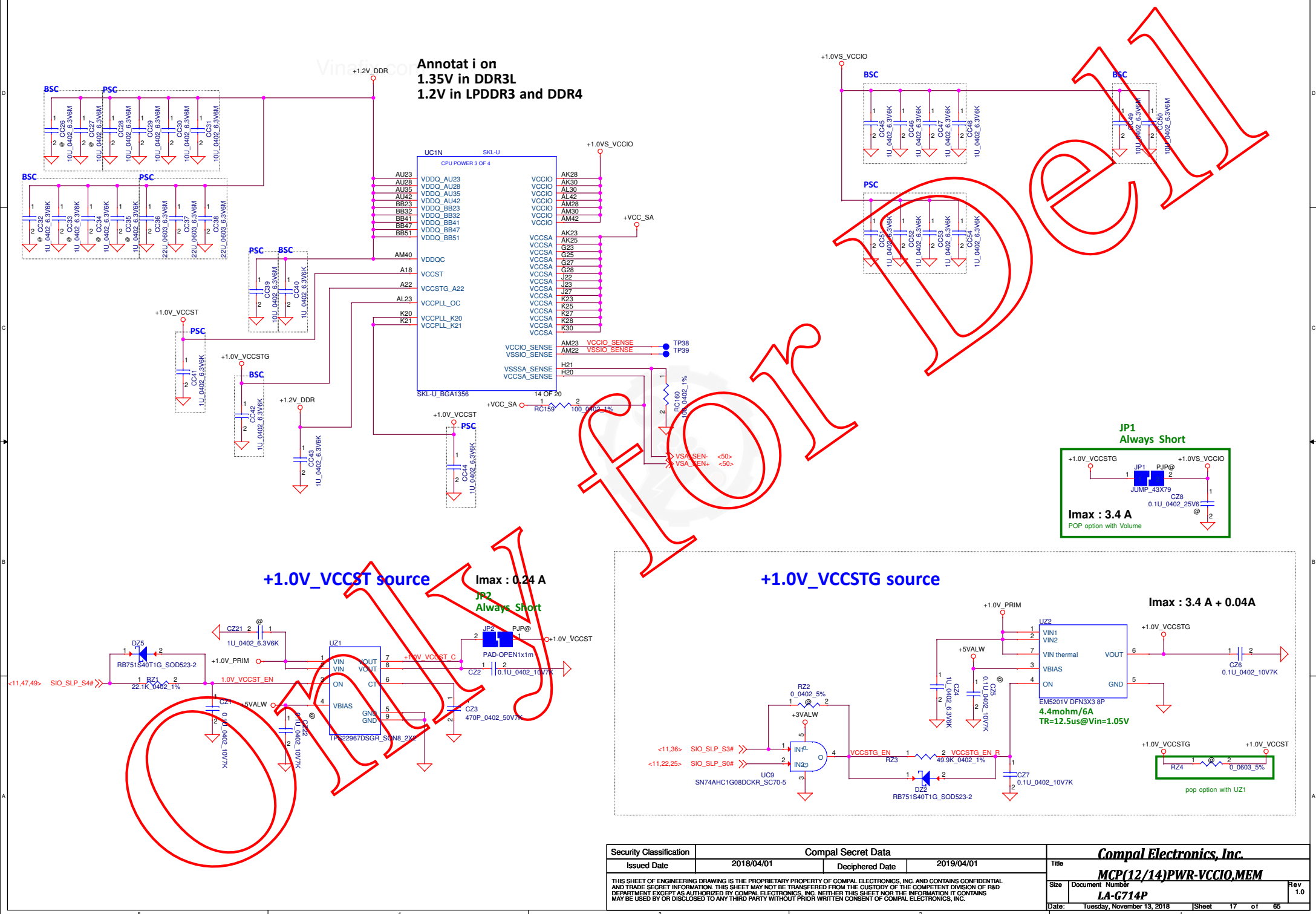
Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGT_X : 0.3~1.35V

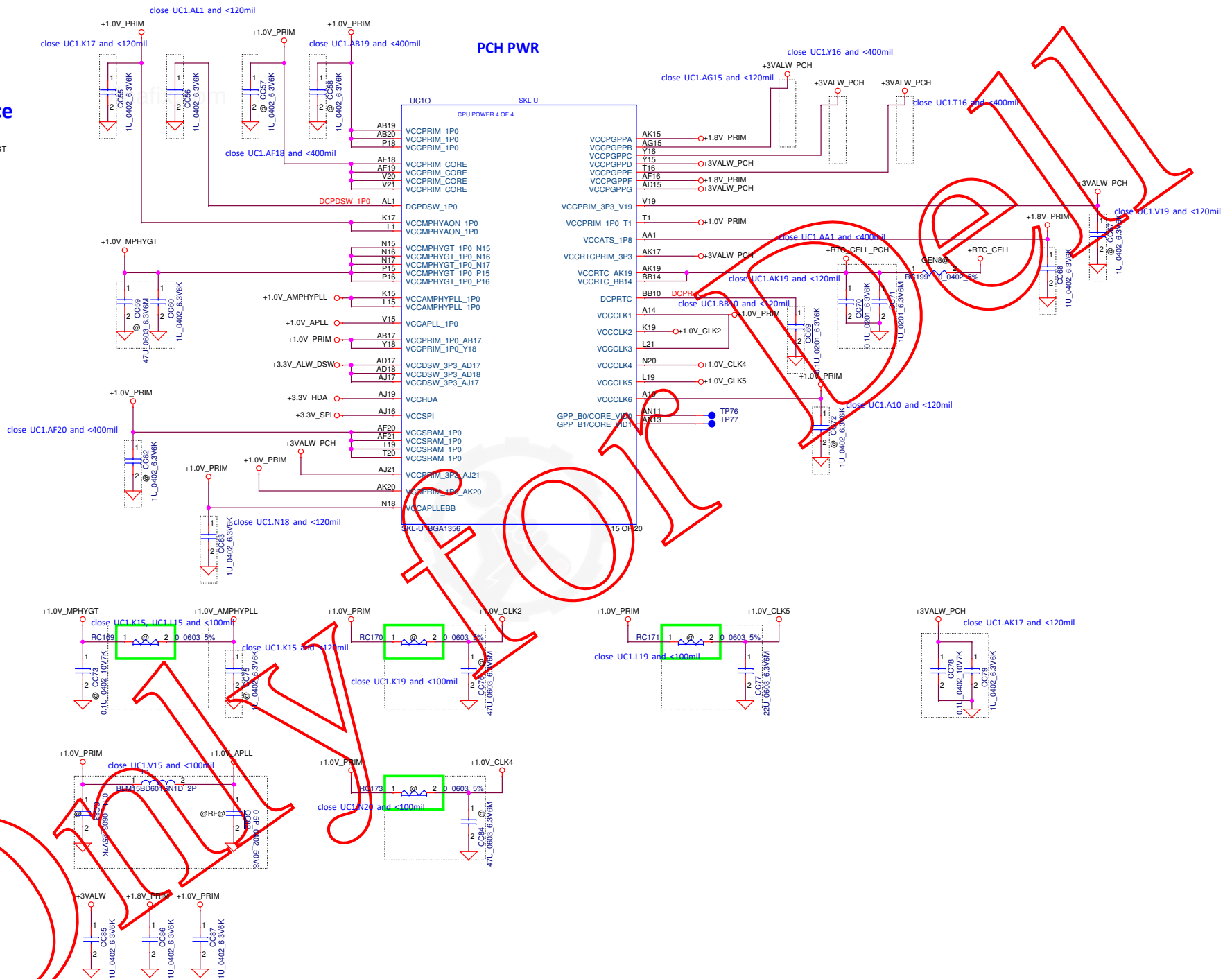
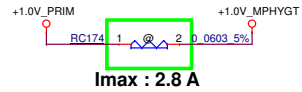
+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



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+1.0V_MPHYGT source



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Main Func = CPU

UC1P SKL-U

GND 1 OF 3

UC1Q SKL-U

GND 2 OF 3

UC1R SKL-U

GND 3 OF 3

A5	VSS	AL65	VSS	AT63	VSS	BA49	VSS	F8	VSS	L18	VSS
A67	VSS	AL66	VSS	AT68	VSS	BA53	VSS	G10	VSS	L2	VSS
A70	VSS	AM13	VSS	AT71	VSS	BA57	VSS	G22	VSS	L20	VSS
AA2	VSS	AM21	VSS	AU10	VSS	BA6	VSS	G43	VSS	L4	VSS
AA4	VSS	AM25	VSS	AU15	VSS	BA62	VSS	G45	VSS	L8	VSS
AA65	VSS	AM27	VSS	AU20	VSS	BA66	VSS	G48	VSS	N10	VSS
AA68	VSS	AM43	VSS	AU32	VSS	BA71	VSS	G5	VSS	N13	VSS
AB15	VSS	AM45	VSS	AL38	VSS	BB18	VSS	G52	VSS	N19	VSS
AB16	VSS	AM46	VSS	AV1	VSS	BB26	VSS	G55	VSS	N21	VSS
AB18	VSS	AM55	VSS	AV68	VSS	BB30	VSS	G58	VSS	N6	VSS
AB21	VSS	AM60	VSS	AV69	VSS	BB34	VSS	G6	VSS	N65	VSS
AB8	VSS	AM61	VSS	AV70	VSS	BB38	VSS	G63	VSS	N68	VSS
AD13	VSS	AM68	VSS	AV71	VSS	BB43	VSS	G66	VSS	P17	VSS
AD16	VSS	AM71	VSS	AW10	VSS	BB55	VSS	H15	VSS	P19	VSS
AD19	VSS	AM8	VSS	AW12	VSS	BB6	VSS	H18	VSS	P20	VSS
AD20	VSS	AN20	VSS	AW14	VSS	BB60	VSS	H71	VSS	P21	VSS
AD21	VSS	AN23	VSS	AW16	VSS	BB64	VSS	J11	VSS	R13	VSS
AD62	VSS	AN28	VSS	AW18	VSS	BB67	VSS	J13	VSS	R6	VSS
AD8	VSS	AN30	VSS	AW21	VSS	BB70	VSS	J25	VSS	T15	VSS
AE64	VSS	AN32	VSS	AW23	VSS	C1	VSS	J28	VSS	T17	VSS
AE65	VSS	AN33	VSS	AW26	VSS	C25	VSS	J32	VSS	T18	VSS
AE66	VSS	AN35	VSS	AW28	VSS	C5	VSS	J35	VSS	T2	VSS
AE67	VSS	AN37	VSS	AW30	VSS	D10	VSS	J38	VSS	T21	VSS
AE68	VSS	AN38	VSS	AW32	VSS	D11	VSS	J42	VSS	T4	VSS
AE69	VSS	AN40	VSS	AW34	VSS	D14	VSS	J8	VSS	T10	VSS
AF1	VSS	AN42	VSS	AW36	VSS	D18	VSS	K16	VSS	U63	VSS
AF10	VSS	AN58	VSS	AW38	VSS	D22	VSS	K18	VSS	U64	VSS
AF15	VSS	AN63	VSS	AW41	VSS	D25	VSS	K22	VSS	U66	VSS
AF17	VSS	AP10	VSS	AW43	VSS	D26	VSS	K61	VSS	U67	VSS
AF2	VSS	AP18	VSS	AW45	VSS	D30	VSS	K63	VSS	U69	VSS
AF4	VSS	AP20	VSS	AW47	VSS	D34	VSS	K64	VSS	U70	VSS
AF63	VSS	AP23	VSS	AW49	VSS	D39	VSS	K65	VSS	V16	VSS
AG16	VSS	AP28	VSS	AW51	VSS	D44	VSS	K66	VSS	V17	VSS
AG17	VSS	AP32	VSS	AW53	VSS	D45	VSS	K67	VSS	V18	VSS
AG18	VSS	AP35	VSS	AW55	VSS	D47	VSS	K68	VSS	W13	VSS
AG19	VSS	AP38	VSS	AW57	VSS	D48	VSS	K70	VSS	W6	VSS
AG20	VSS	AP42	VSS	AW6	VSS	D53	VSS	K71	VSS	Y17	VSS
AG21	VSS	AP58	VSS	AW60	VSS	D58	VSS	L11	VSS	Y19	VSS
AG71	VSS	AP63	VSS	AW62	VSS	D6	VSS	L16	VSS	Y20	VSS
AH13	VSS	AP68	VSS	AW64	VSS	D62	VSS	L17	VSS	Y21	VSS
AH6	VSS	AP70	VSS	AW66	VSS	D66	VSS				
AH63	VSS	AR11	VSS	AW8	VSS	D69	VSS				
AH64	VSS	AR15	VSS	AY66	VSS	E11	VSS				
AH67	VSS	AR16	VSS	B10	VSS	E15	VSS				
AJ15	VSS	AR20	VSS	B14	VSS	E18	VSS				
AJ18	VSS	AR23	VSS	B18	VSS	E21	VSS				
AJ20	VSS	AR28	VSS	B22	VSS	E46	VSS				
AJ4	VSS	AR35	VSS	B30	VSS	E50	VSS				
AK11	VSS	AR42	VSS	B34	VSS	E53	VSS				
AK16	VSS	AR43	VSS	B39	VSS	E56	VSS				
AK18	VSS	AR45	VSS	B44	VSS	E6	VSS				
AK21	VSS	AR46	VSS	B48	VSS	E65	VSS				
AK22	VSS	AR48	VSS	B53	VSS	E71	VSS				
AK27	VSS	AR5	VSS	B58	VSS	F1	VSS				
AK63	VSS	AR50	VSS	B62	VSS	F13	VSS				
AK68	VSS	AR52	VSS	B66	VSS	F2	VSS				
AK69	VSS	AR53	VSS	B71	VSS	F22	VSS				
AK8	VSS	AR55	VSS	BA1	VSS	F23	VSS				
AL2	VSS	AR58	VSS	BA10	VSS	F27	VSS				
AL28	VSS	AR63	VSS	BA14	VSS	F28	VSS				
AL32	VSS	AR8	VSS	BA18	VSS	F32	VSS				
AL35	VSS	AT2	VSS	BA2	VSS	F33	VSS				
AL38	VSS	AT20	VSS	BA23	VSS	F35	VSS				
AL4	VSS	AT23	VSS	BA28	VSS	F37	VSS				
AL45	VSS	AT28	VSS	BA32	VSS	F38	VSS				
AL48	VSS	AT35	VSS	BA36	VSS	F4	VSS				
AL52	VSS	AT4	VSS	F68	VSS	F40	VSS				
AL55	VSS	AT42	VSS	BA45	VSS	F42	VSS				
AL58	VSS	AT56	VSS								
AL64	VSS	AT58	VSS								

SKL-U_BGA1356 16 OF 20

SKL-U_BGA1356 17 OF 20

SKL-U_BGA1356 18 OF 20

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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				Date:	Tuesday, November 13, 2018	Sheet 19 of 65

Main Func = DDR

<7> DDR_A_D0_63J
<7> DDR_A_MA(0..13)
<7> DDR_A_DQS#(0..7)
<7> DDR_A_DQS(0..7)

Layout Note:
Place near JDIMM1.257,259

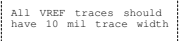
Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

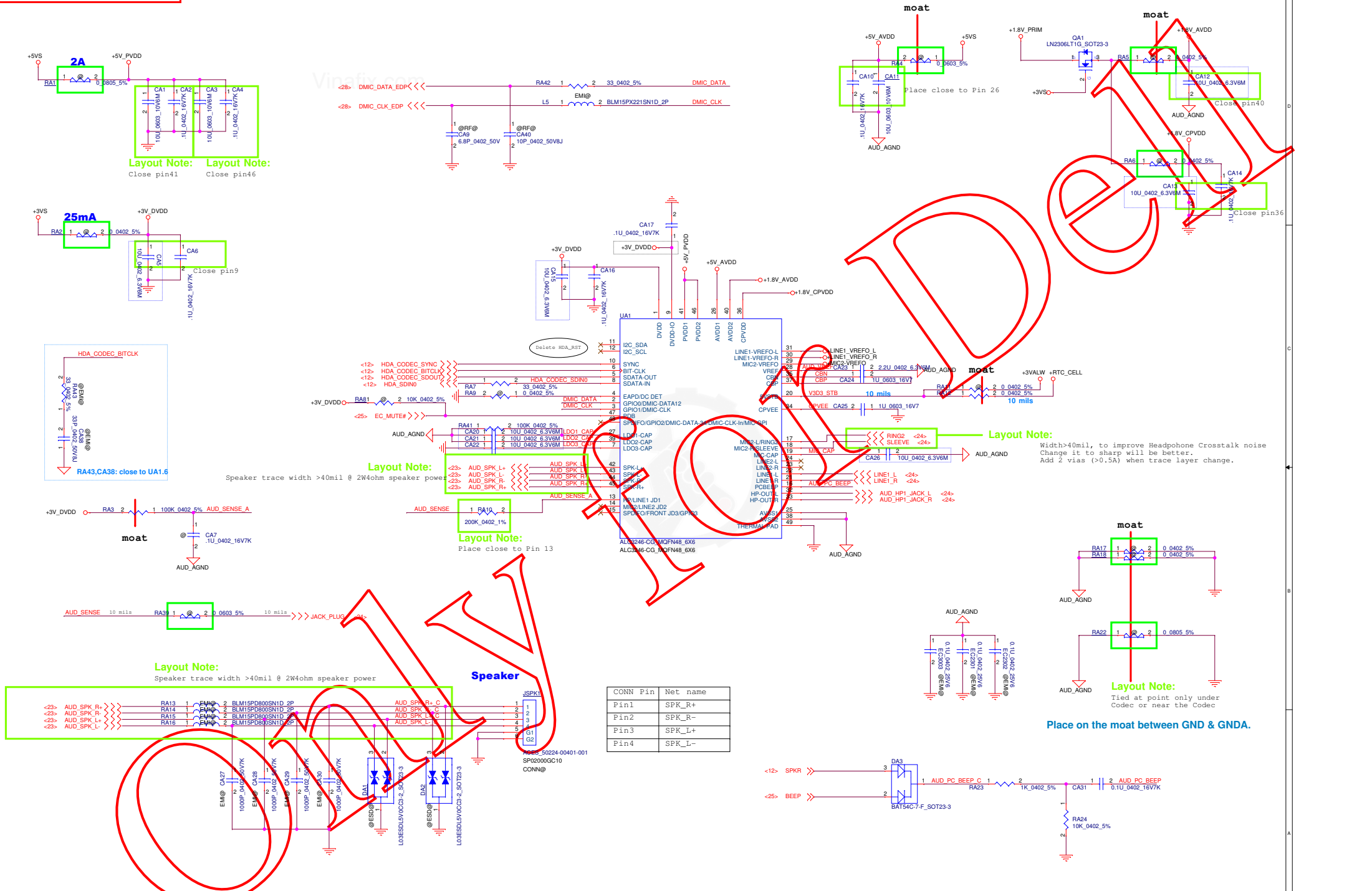
All VREF traces should
have 10 mil trace width

Layout Note:
Place near JDIMM2.255

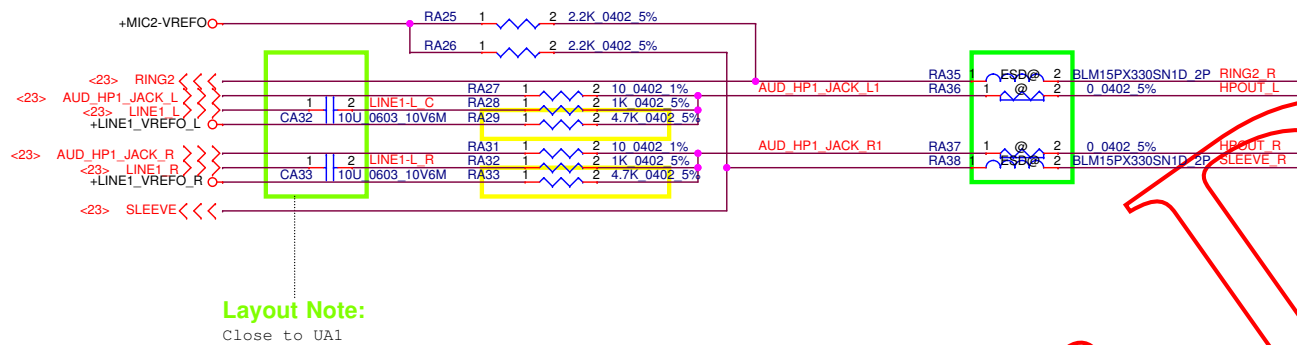


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			Document Number	
			Rev 1.0	
			LA-G714P	
			Date:	Tuesday, November 13, 2018 [Sheet 21 of 65]

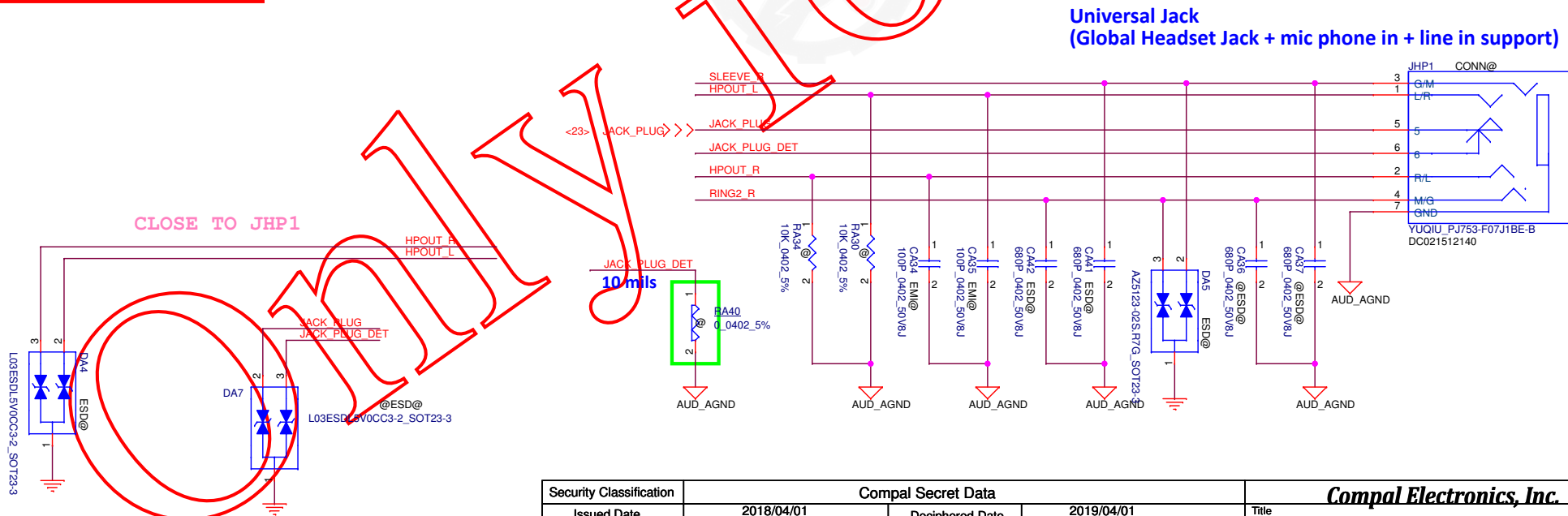
Main Func = Audio



Main Func = Audio Jack

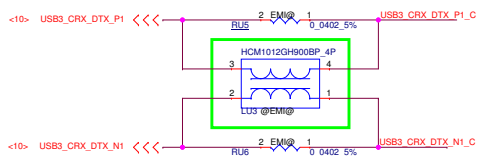
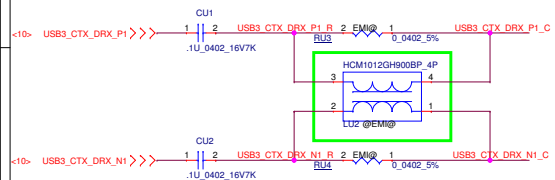
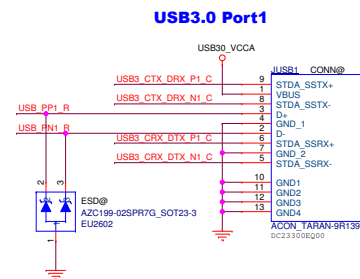
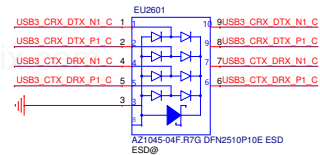
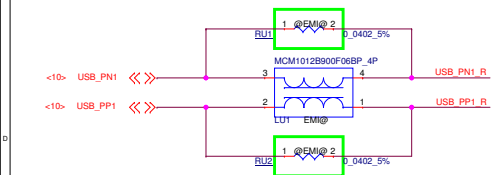


Main Func = Audio Jack

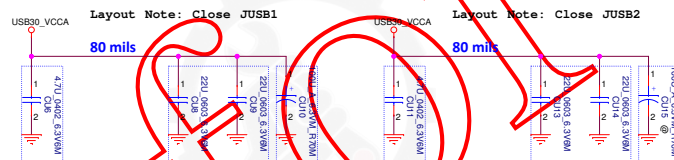
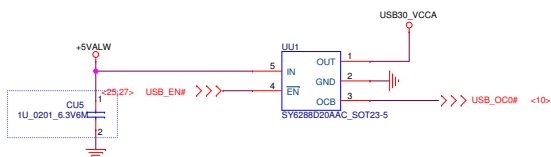


Security Classification		Compal Secret Data		Title	
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Audio JACK	
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				LA-G714P	Rev 1.0
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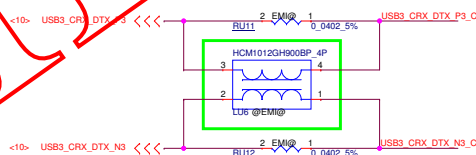
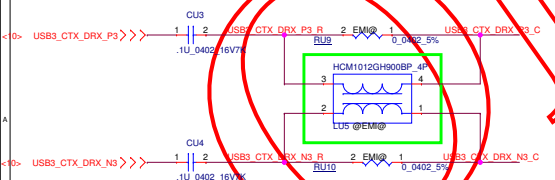
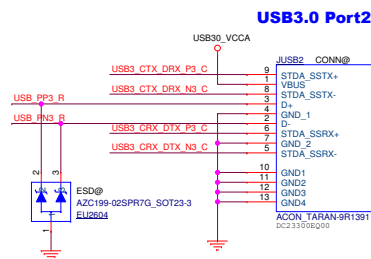
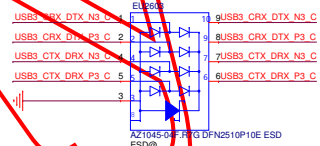
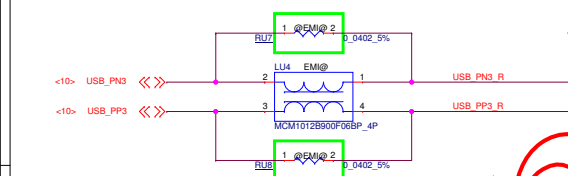
Main Func = USB3.0 Port1



Maximum Output Current 2A

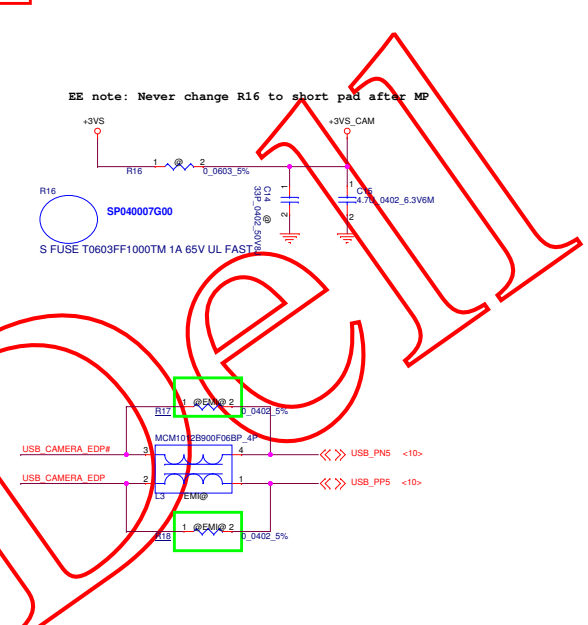


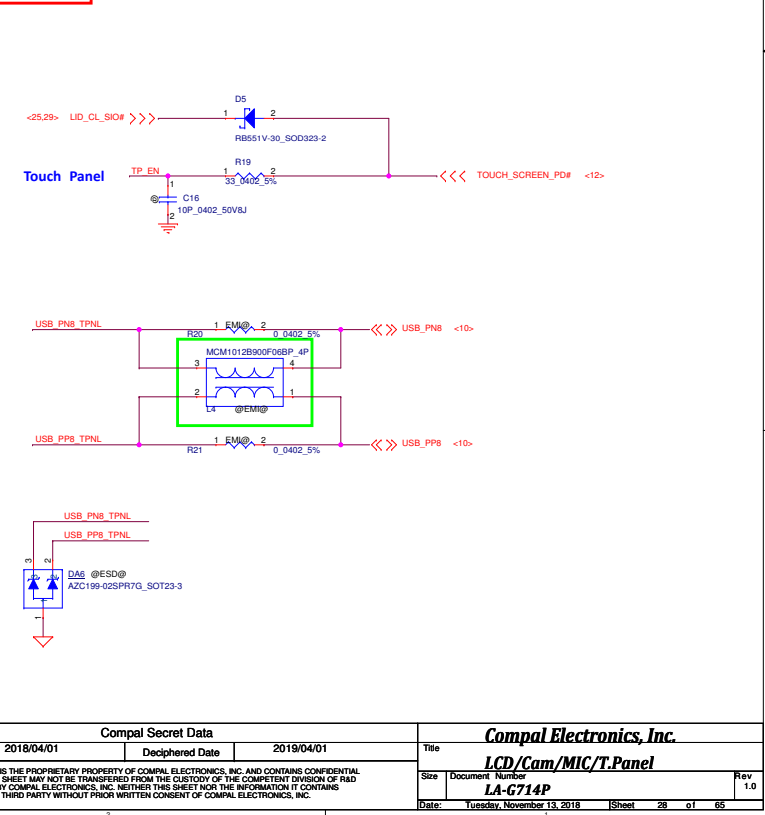
Main Func = USB3.0 Port2



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Size	Document Number	Date	Yuesday, November 13, 2018	Sheet 26 of 65

Main Func = CAM



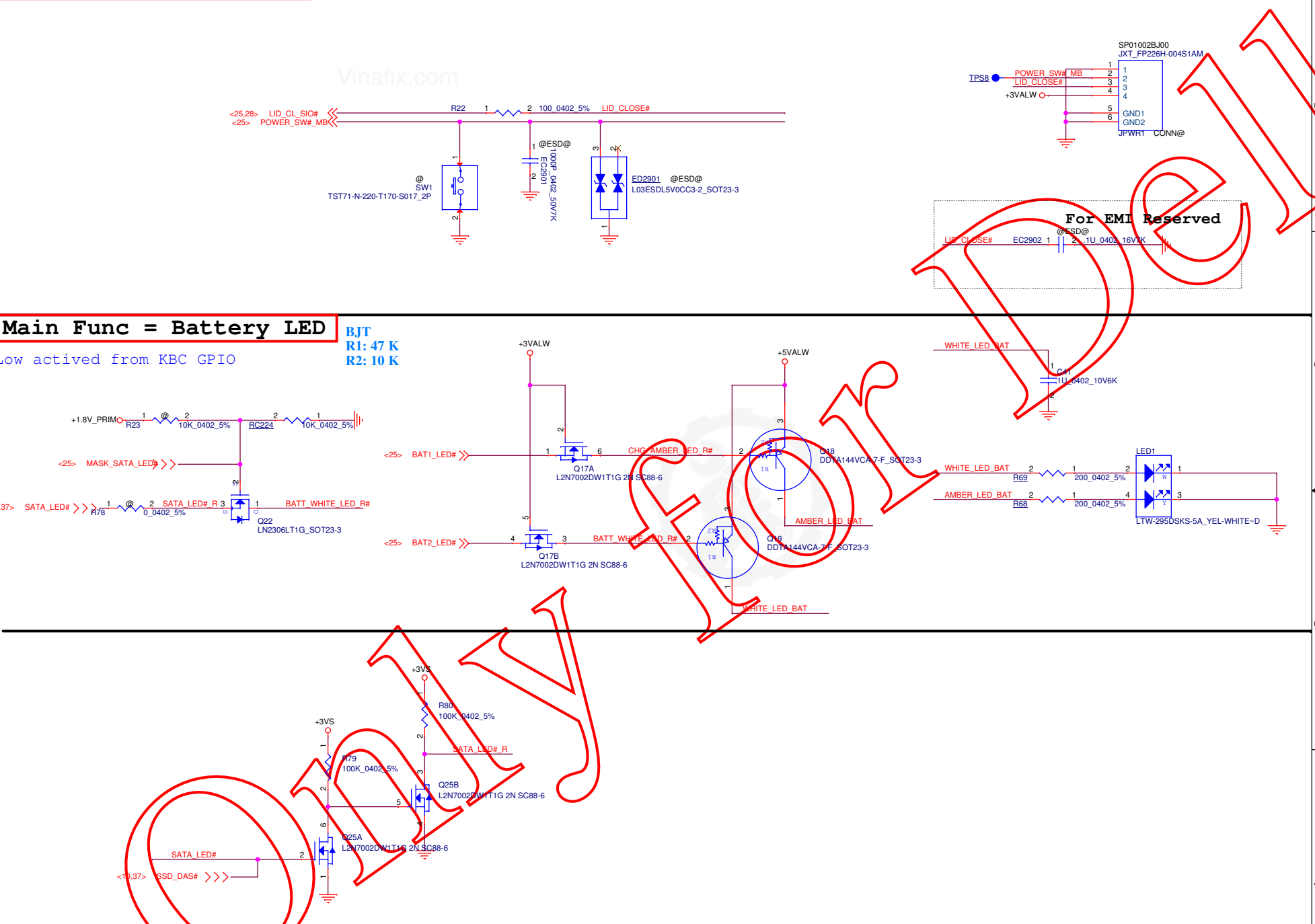


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Date:	Tuesday, November 13, 2018	Sheet 28 of 65

Main Func = Power BTN

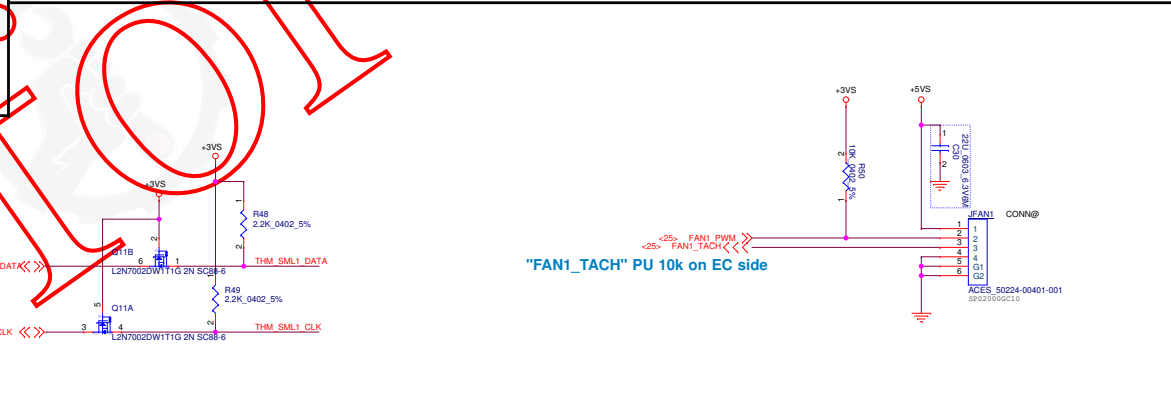
Main Func = Battery LED

Low actived from KBC GPIO

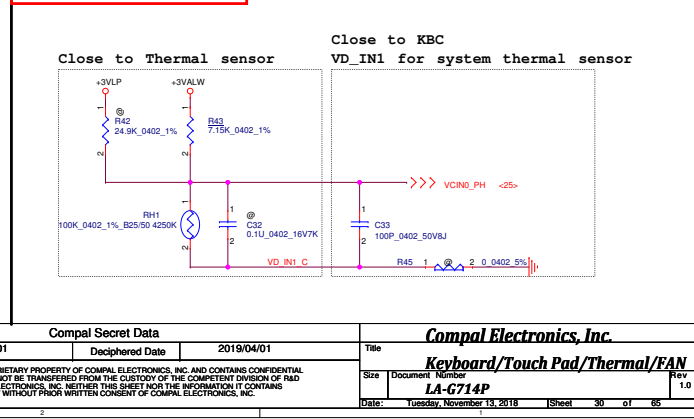


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				Size	Document Number
				LA-G714P	
				Date:	Tuesday, November 13, 2018
				Sheet	29 of 65
				Rev	1.0

Main Func = OTP

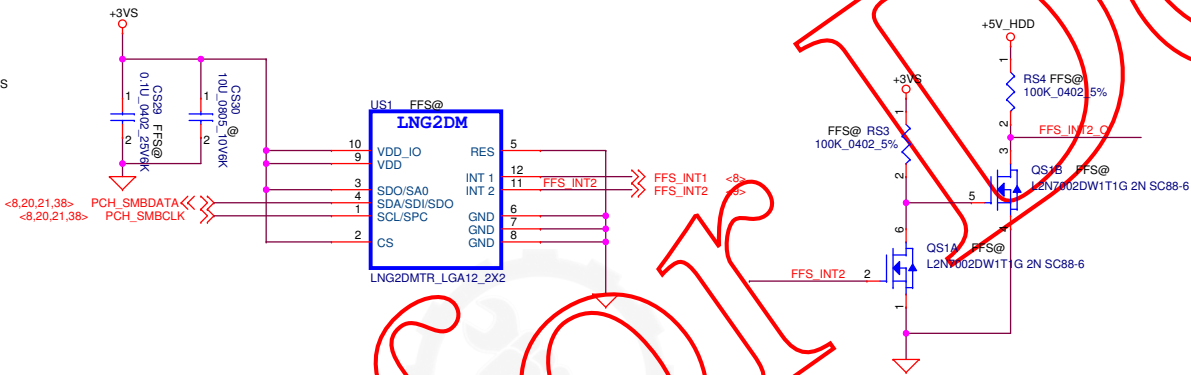
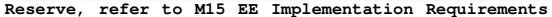
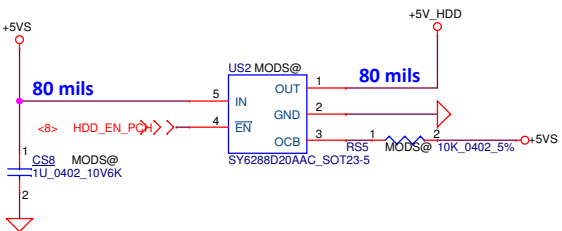


Main Func = OTP



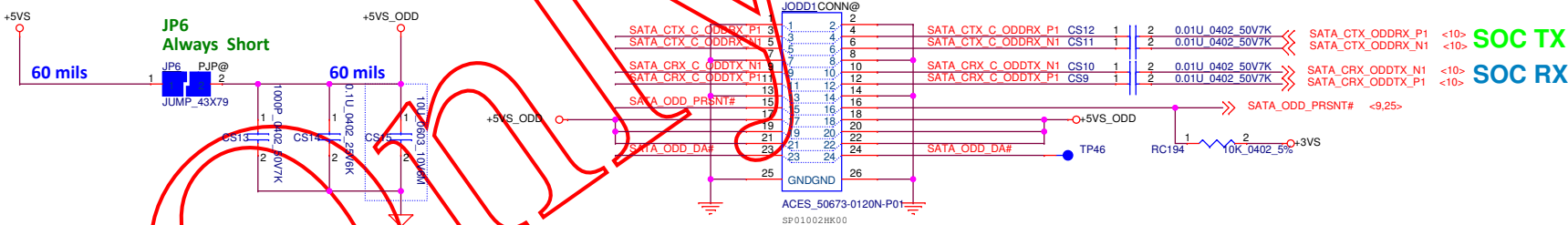
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

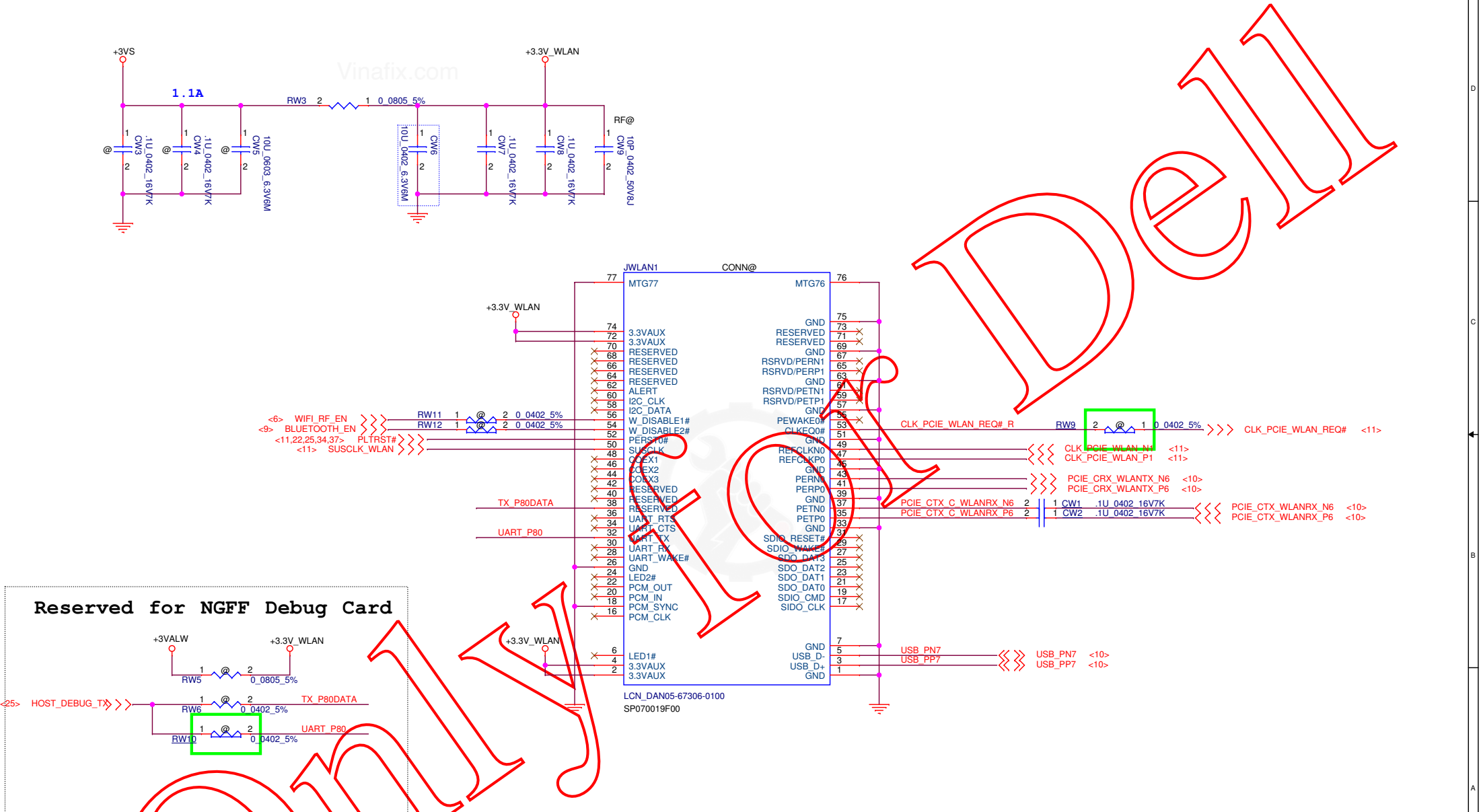
Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9 10 11
5V	P3	
Attenti o	P4	12
GND	P5	
GND	P6	

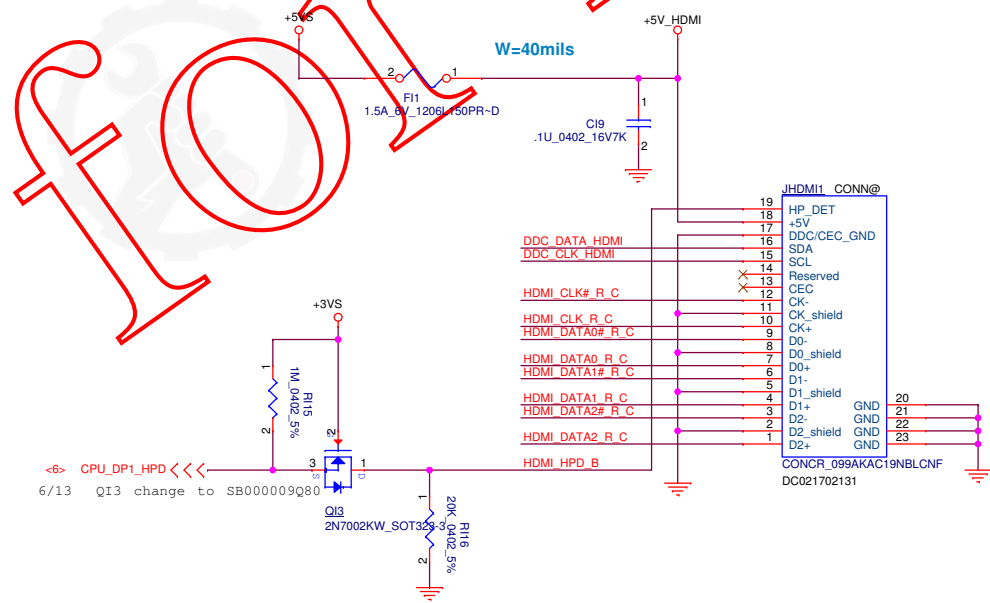
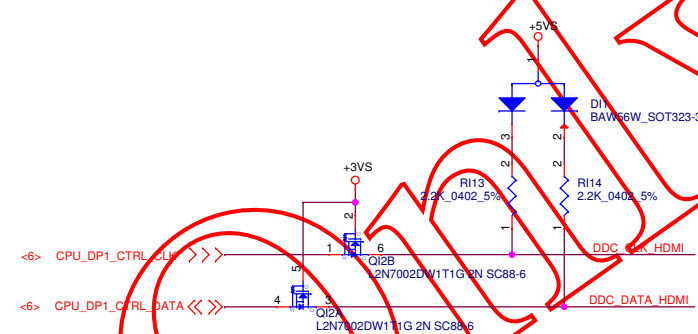
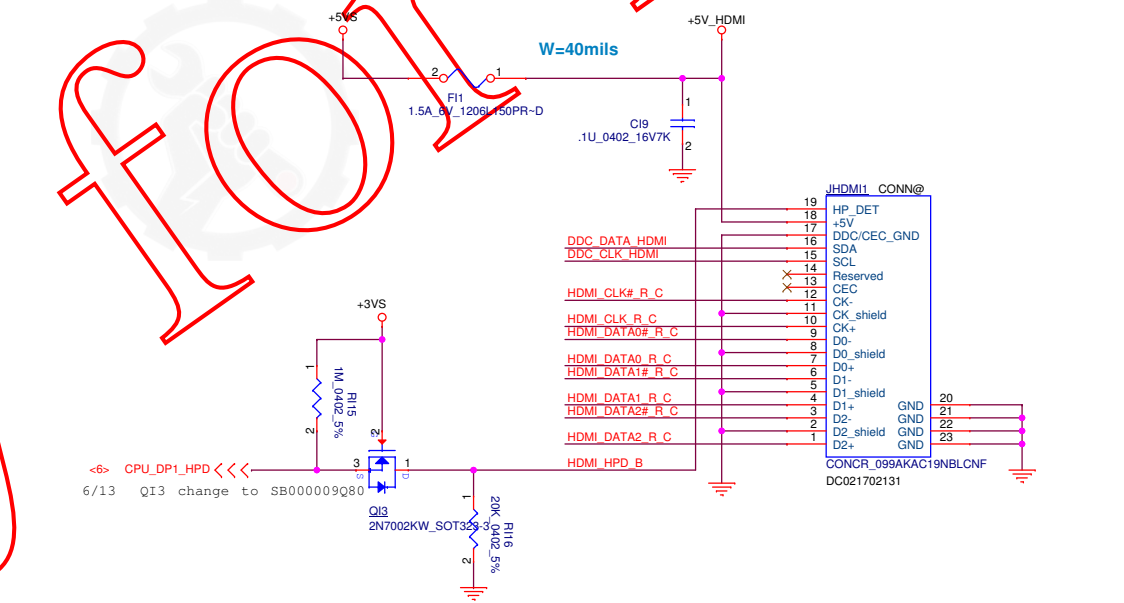
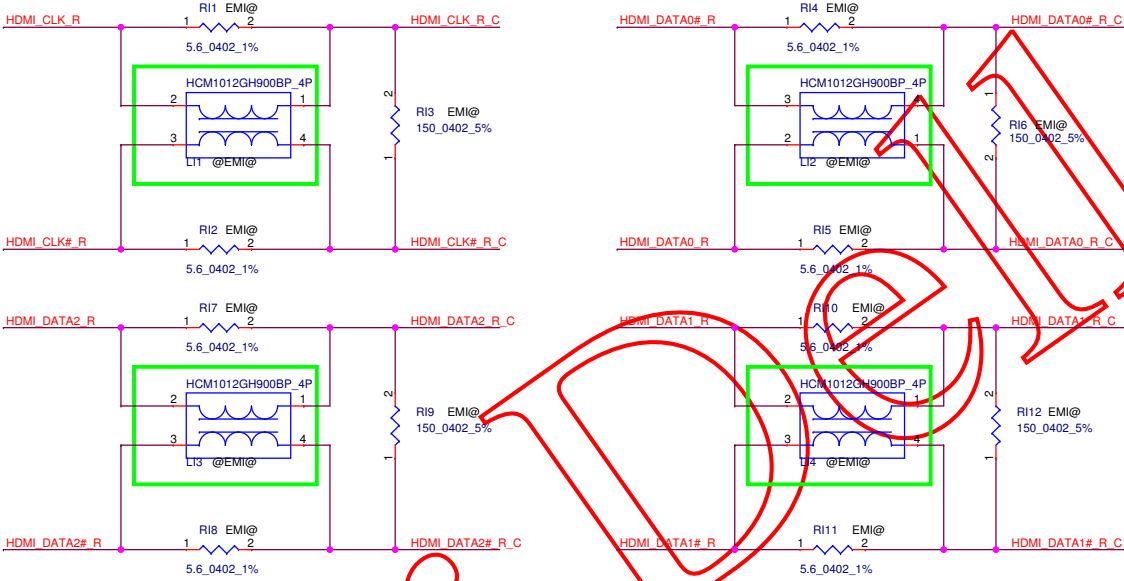
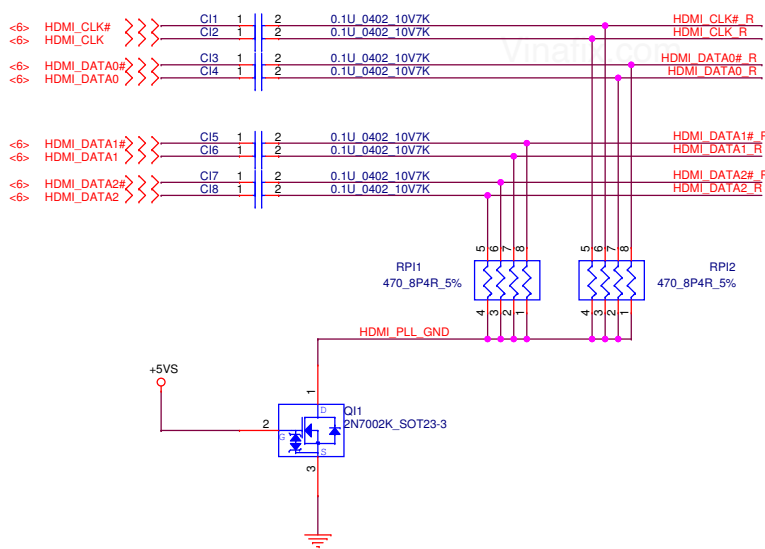
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title HDD/FFS/ODD		
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Main Func = WLAN A Key CONN

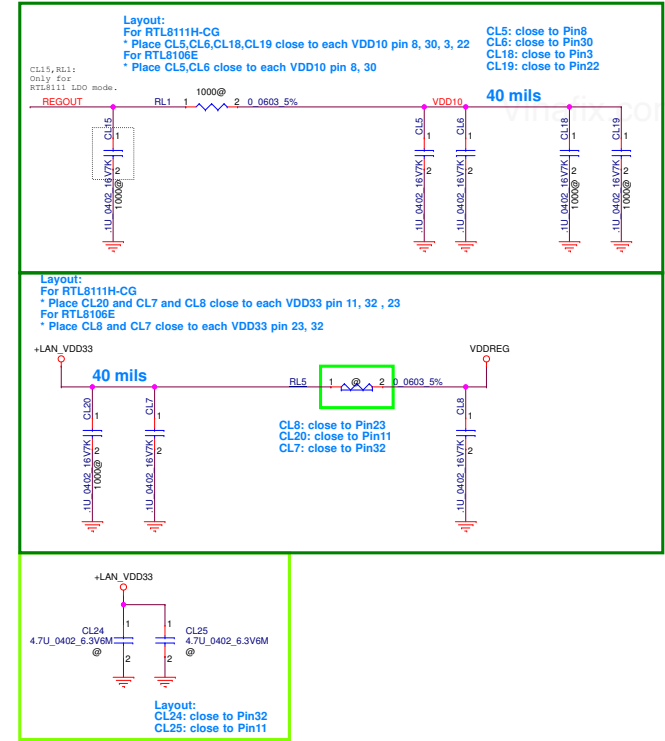


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				Size	Document Number
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Main Func = HDMI



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Size		Document Number						Rev			
		LA-G714P						1.0			
Date:		Tuesday, November 13, 2018		Sheet		33		of 65			

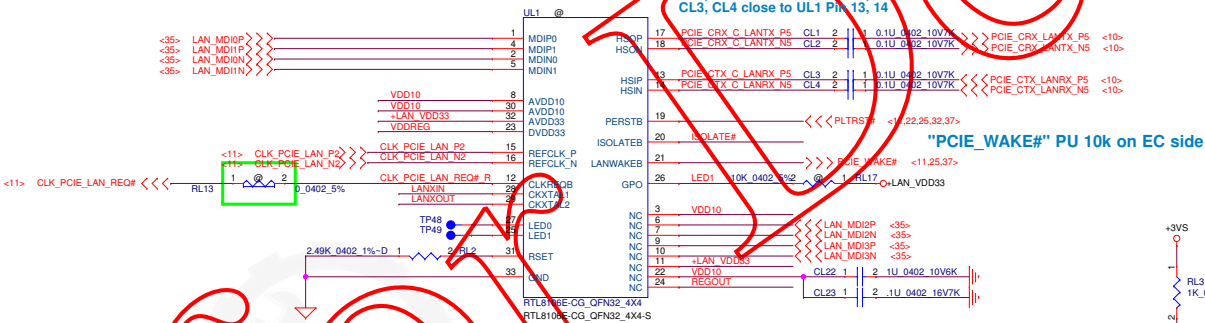


LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M

UL1 1000@
RTL8111H-CG OFN 32P E-LAN CTRL
SA000080P00

UL1 100@
RTL8106E-CG OFN32_4X4
SA000065Y00



+LAN_VDD33 Rising time (10%~90%) need
>0.5mS and <100mS.

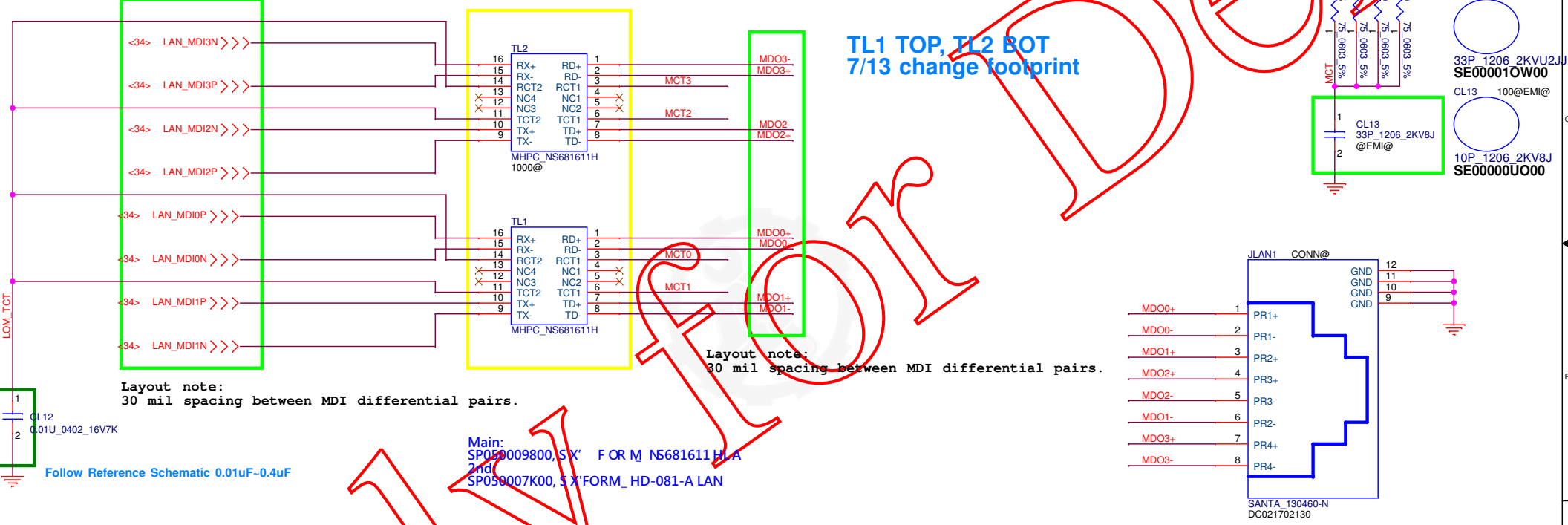
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Main Func = LAN LAN TransFormer 10/100M x2

Vinafix.com

LAN TransFormer (Giga & 10/100 co-layout)

Dont use SP050006H00 on Giga LAN SKU due to EMI test failure



Layout note:
30 mil spacing between MDI differential pairs.

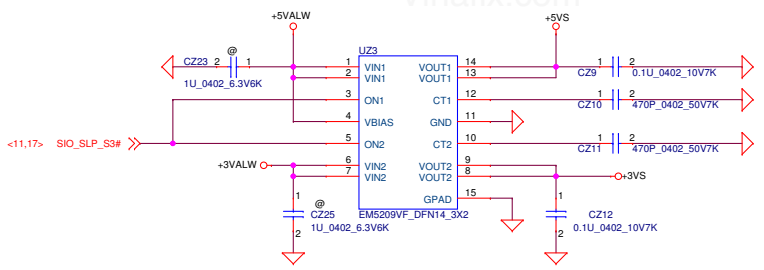
Layout note:
30 mil spacing between MDI differential pairs.

Main:
SP050009800, S X' F OR M N5681611 HLA
2nd:
SP050007K00, S X' FORM_HD-081-A LAN

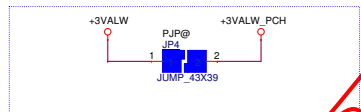
Follow Reference Schematic 0.01uF~0.4uF

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		LA-G714P		1.0	
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+5VS/+3VS for System



+3VALW_PCH for System

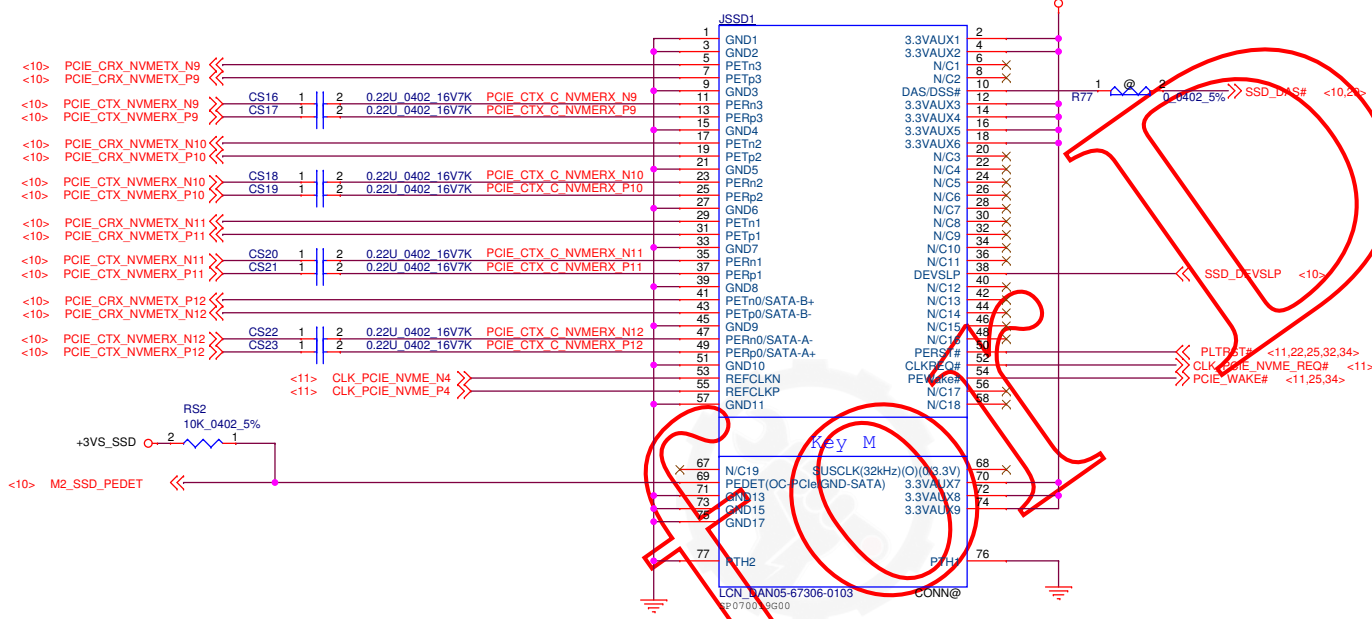
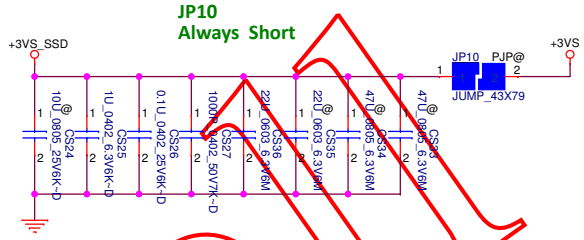


JP4 Short
for NON-DS3

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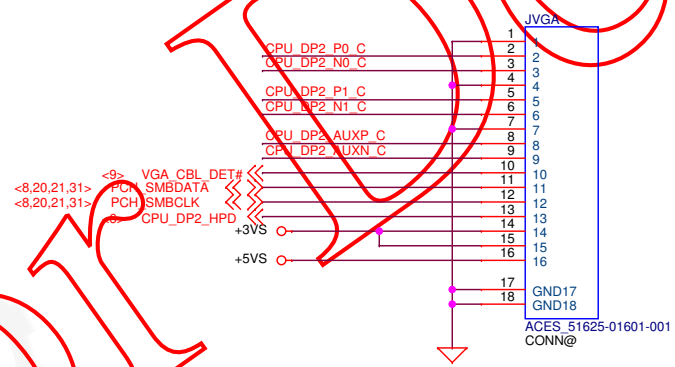
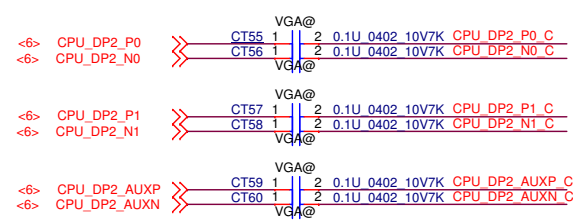
Vinafix.com

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

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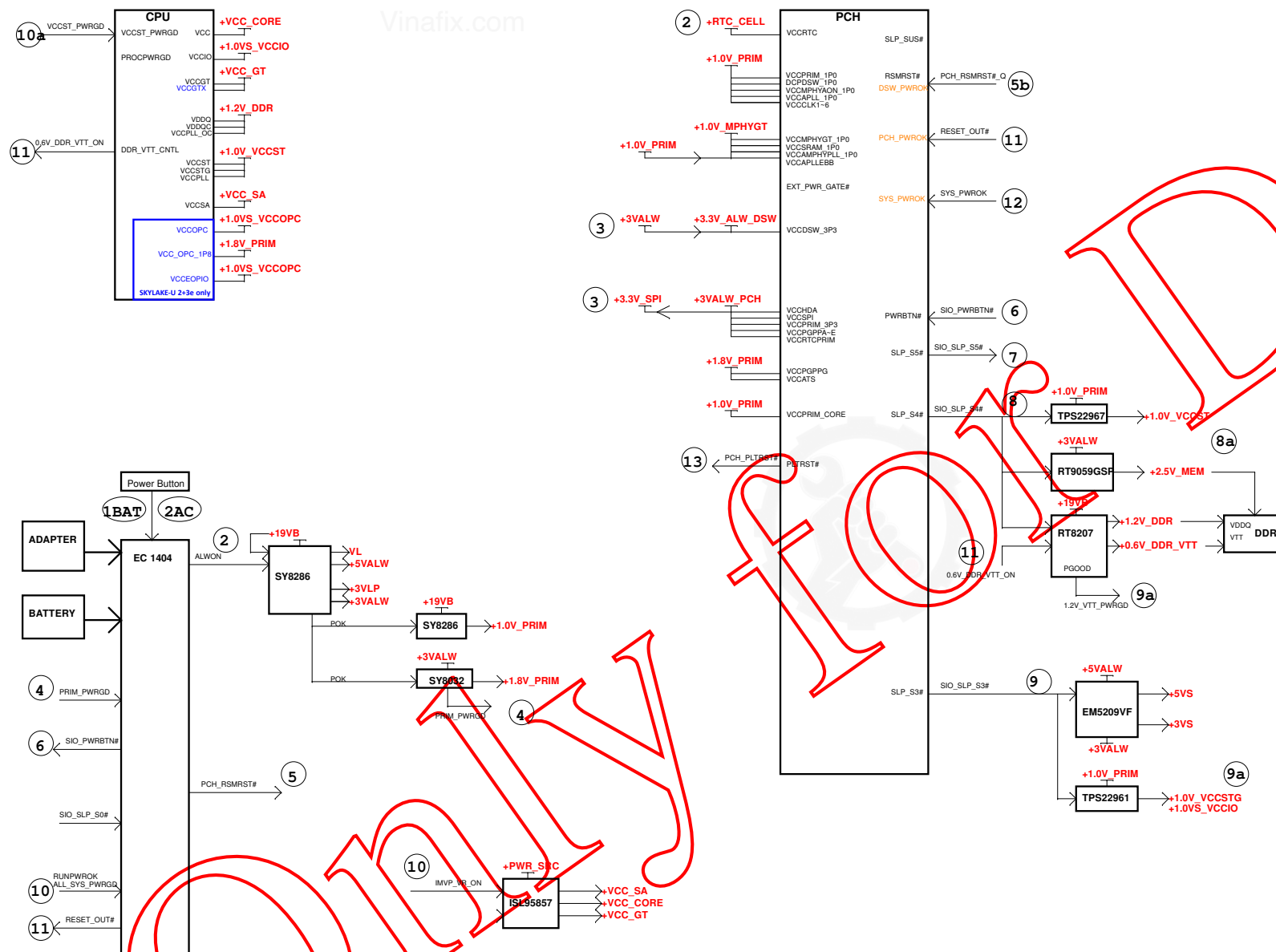
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Timing Diagram for S5 to S0 mode



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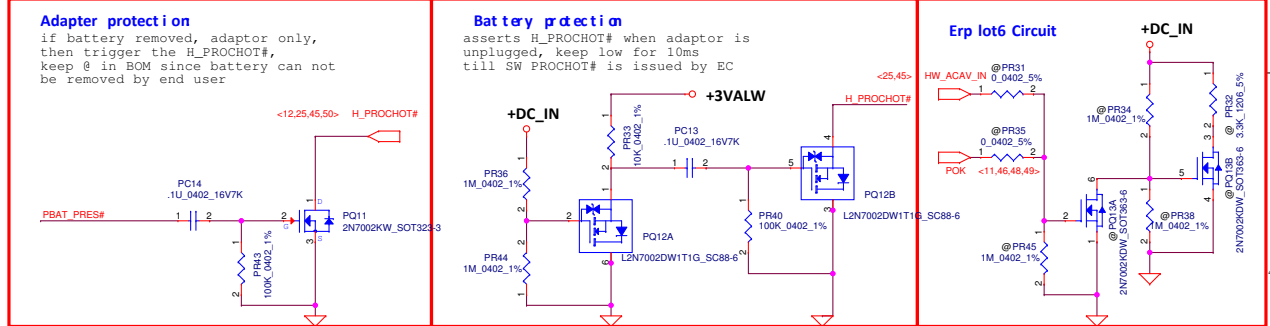
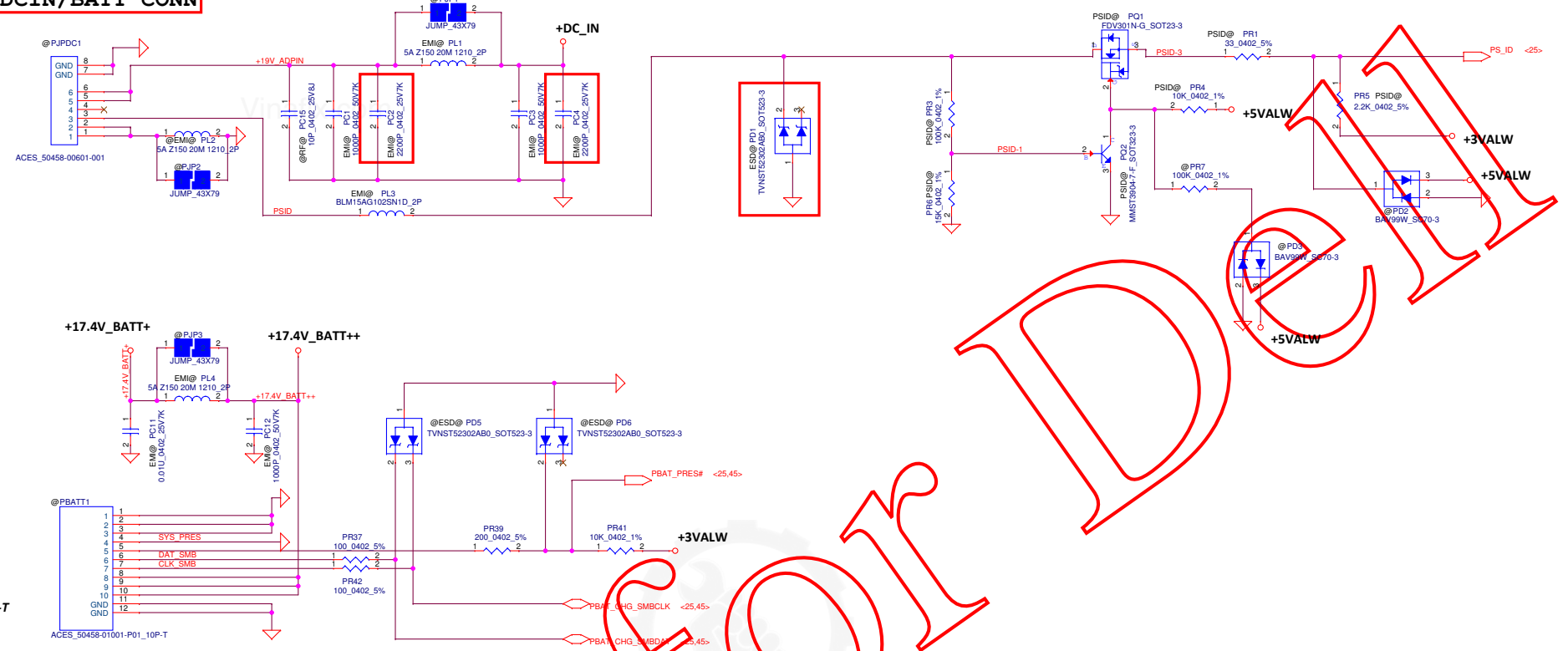
Main Func = DCIN/BATT CONN

Battery Bat Side

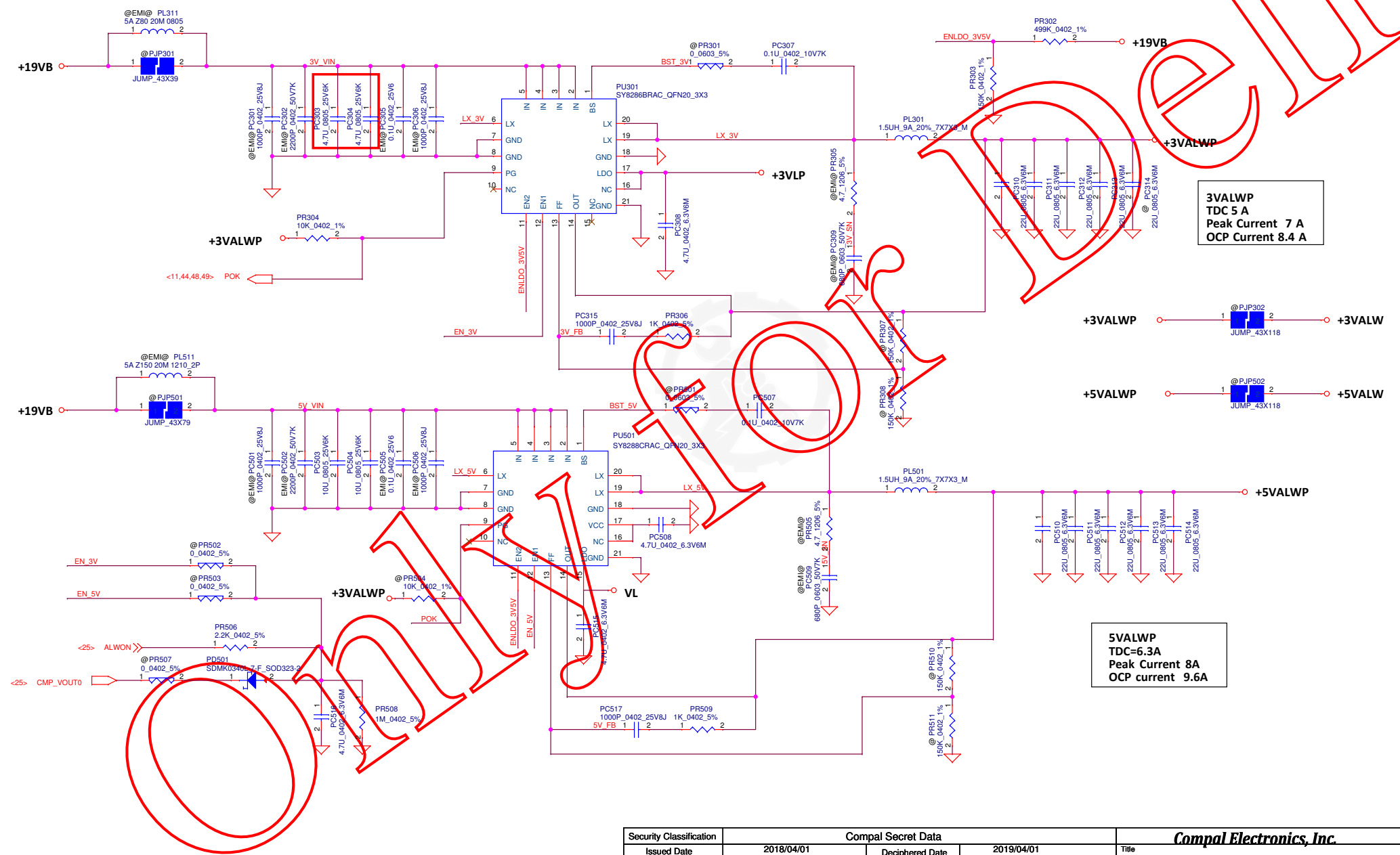
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T

ONLY FOR DESIGN



Main Func = 3.3VALWP/5VALWP

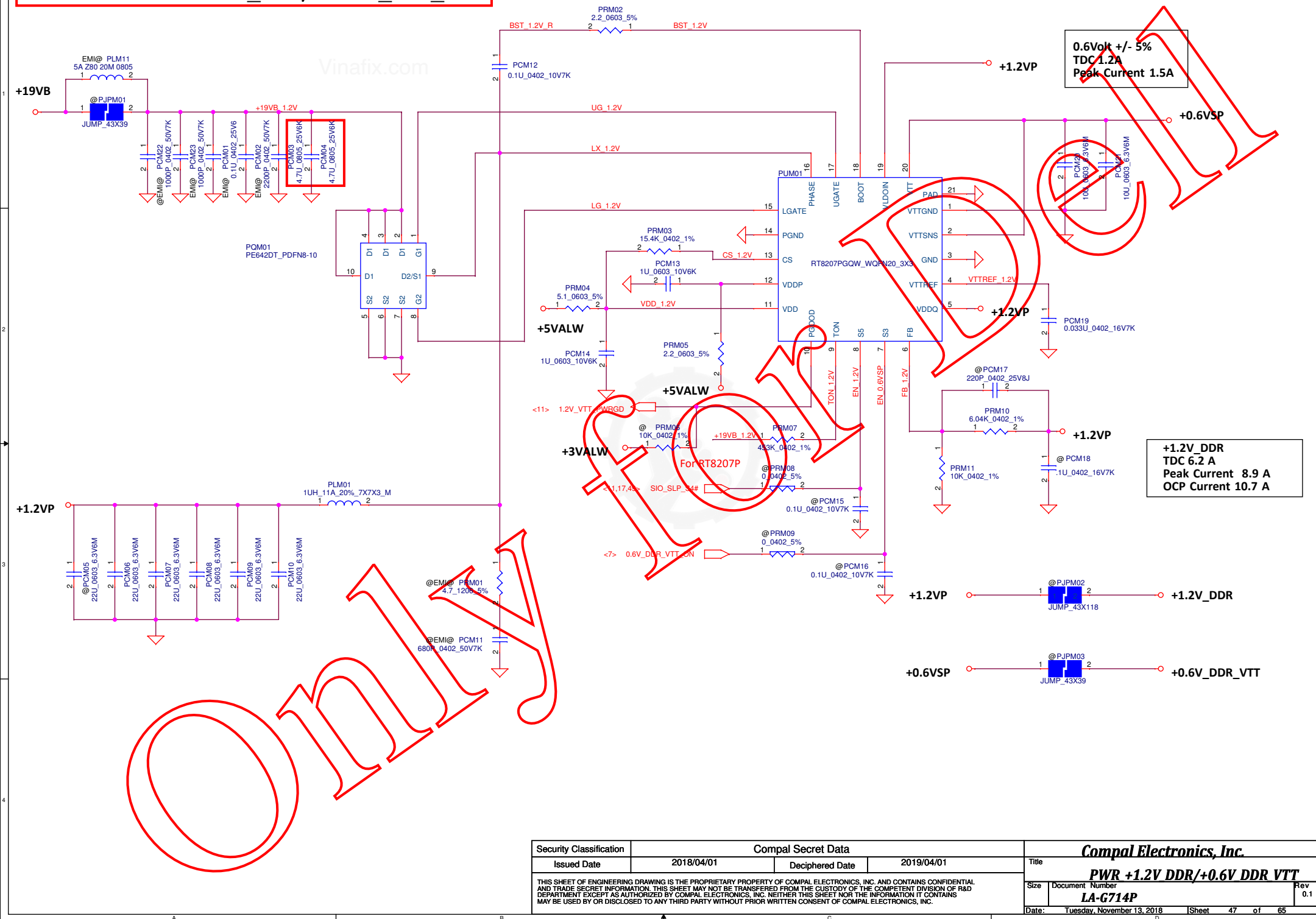


3VALWP
TDC 5 A
Peak Current 7 A
OCP Current 8.4 A

5VALWP
TDC=6.3A
Peak Current 8A
OCP current 9.6A

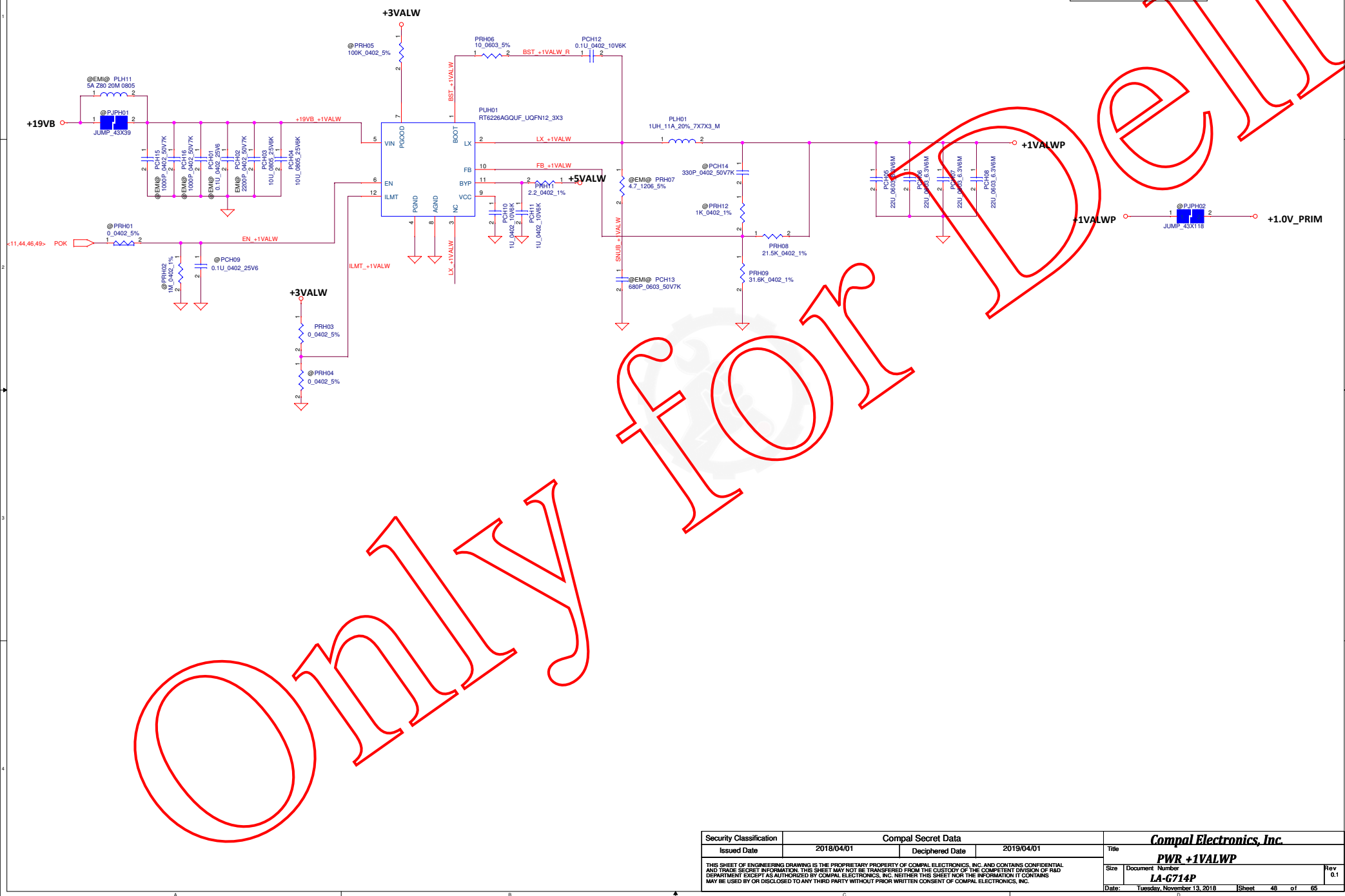
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT

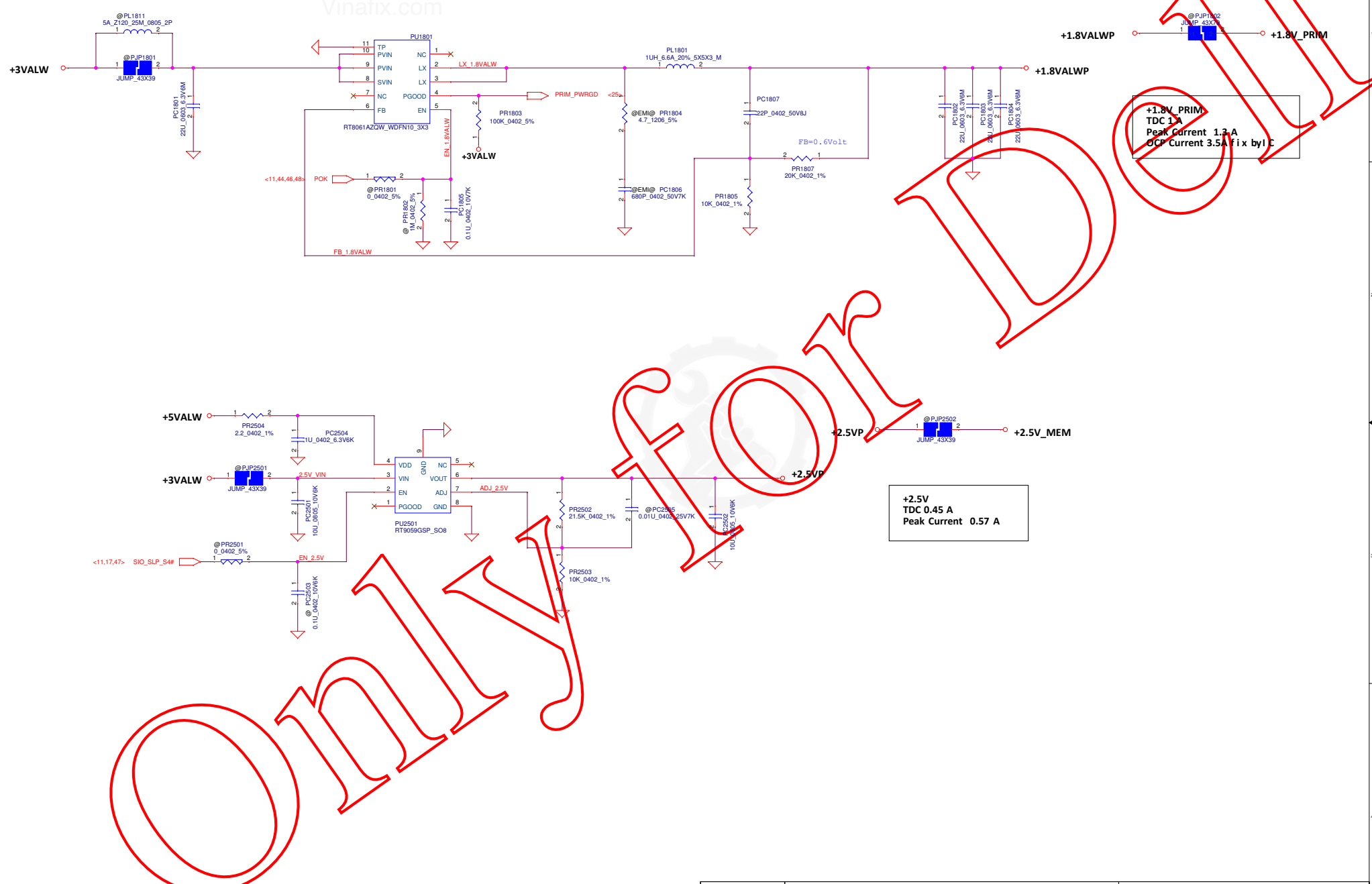


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Main Func = +1VALWP



Main Func = +1.8VALWP / +2.5VP



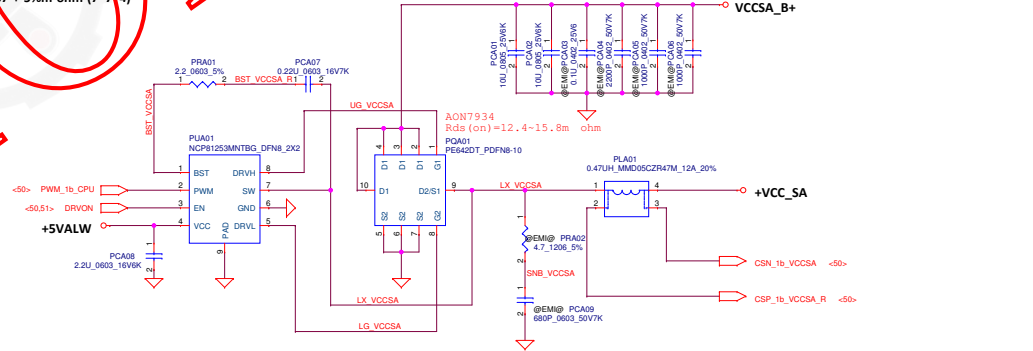
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Main Func = CPU

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Main Func = CPU/ VGA / SA MLCC



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