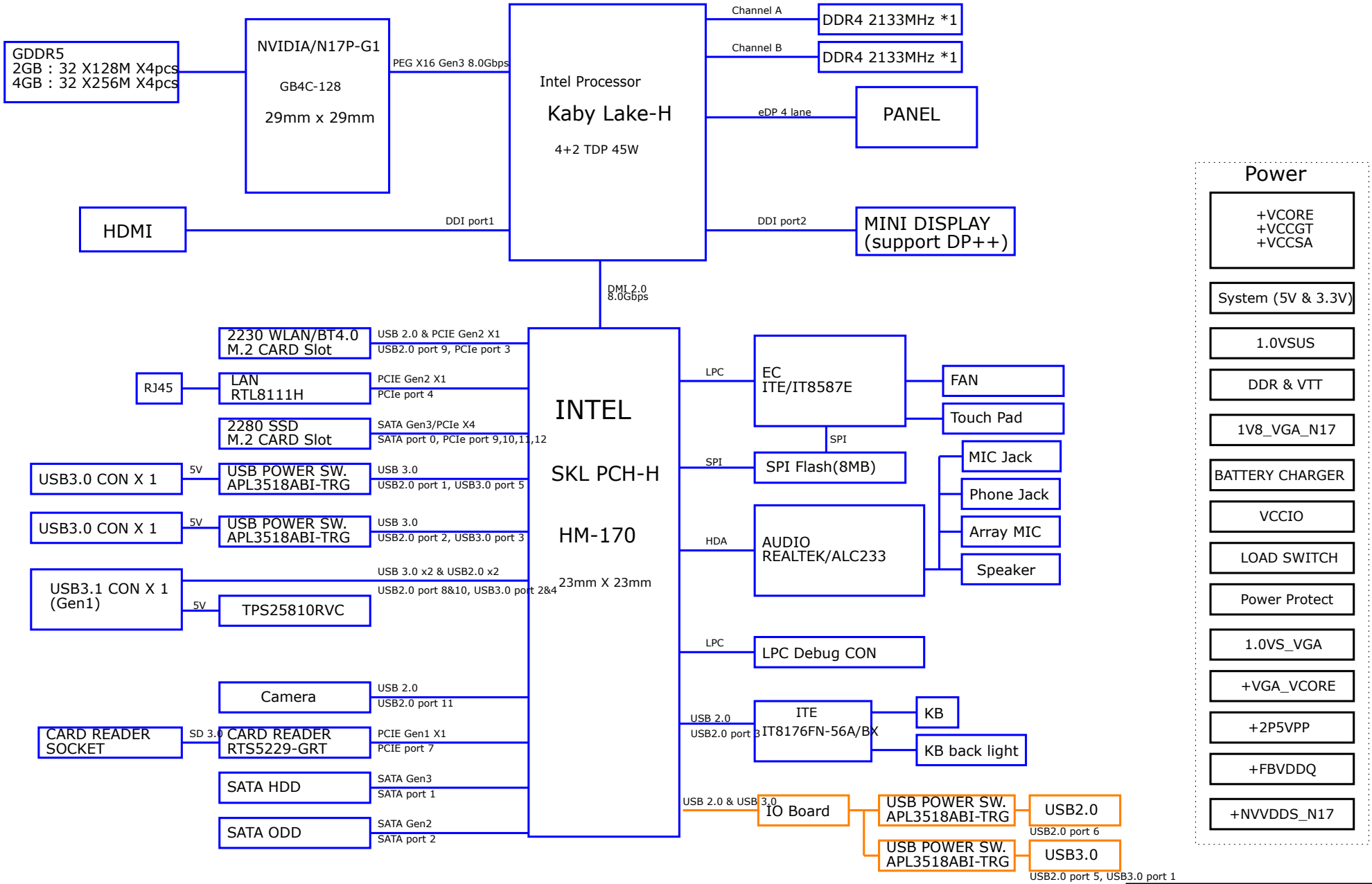
GL753 Block Diagram



Power

- +VCORE
  +VCCGT
  +VCCSA
- System (5V & 3.3V)
- 1.0VSUS
- DDR & VTT
- 1V8_VGA_N17
- BATTERY CHARGER
- VCCIO
- LOAD SWITCH
- Power Protect
- 1.0VS_VGA
- +VGA_VCORE
- +2P5VPP
- +FBVDDQ
- +NVVDDS_N17

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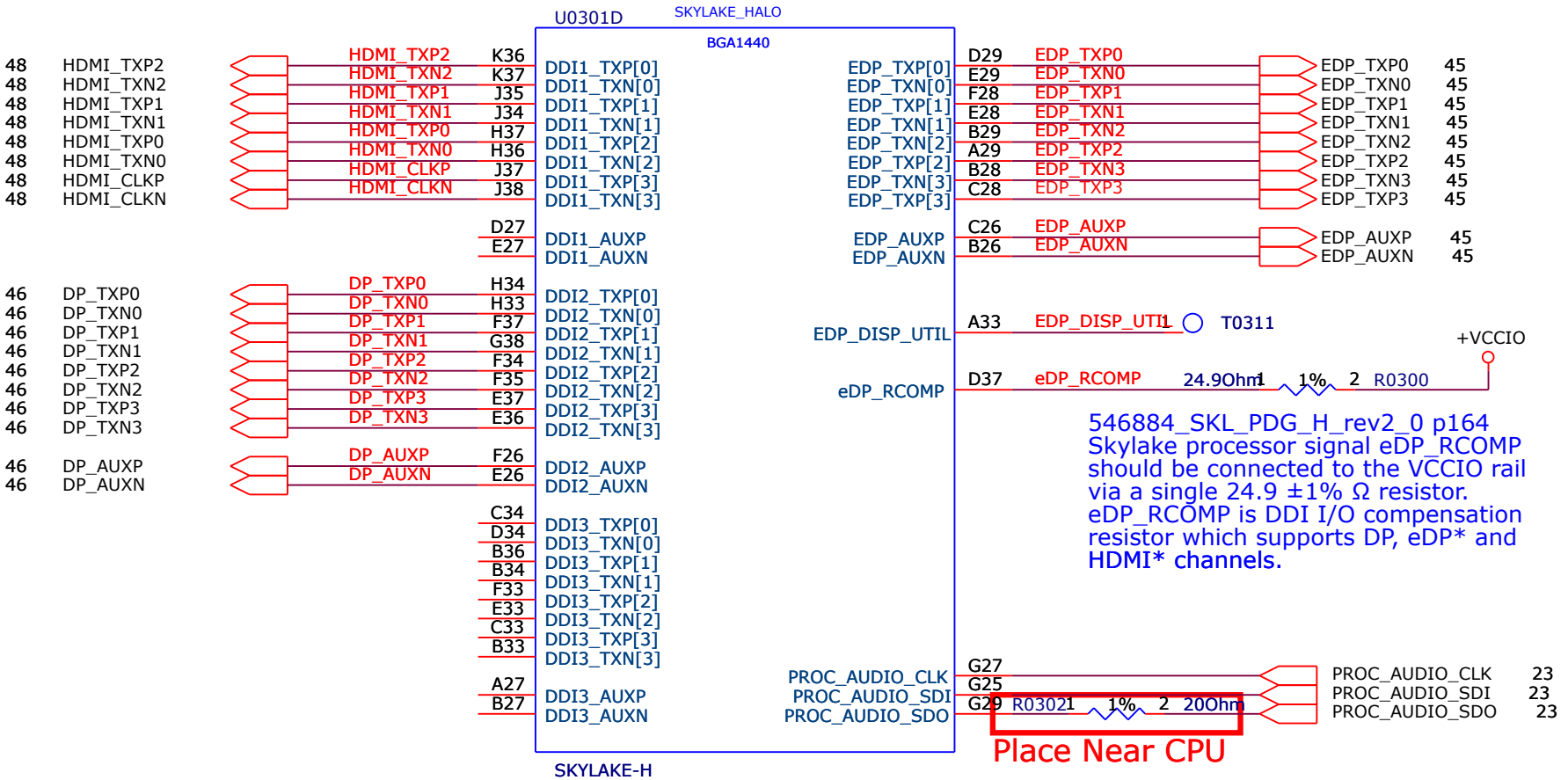
Title: BLOCK DIAGRAM
Engineer: Allen_Kuo
BG1-HW RD Center-HW RD Div.2

Size	Project Name	Rev
Custom	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 1 of 103

3.CPU_DDI/EDP



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BG1-HW RD Center-HW RD Div.2

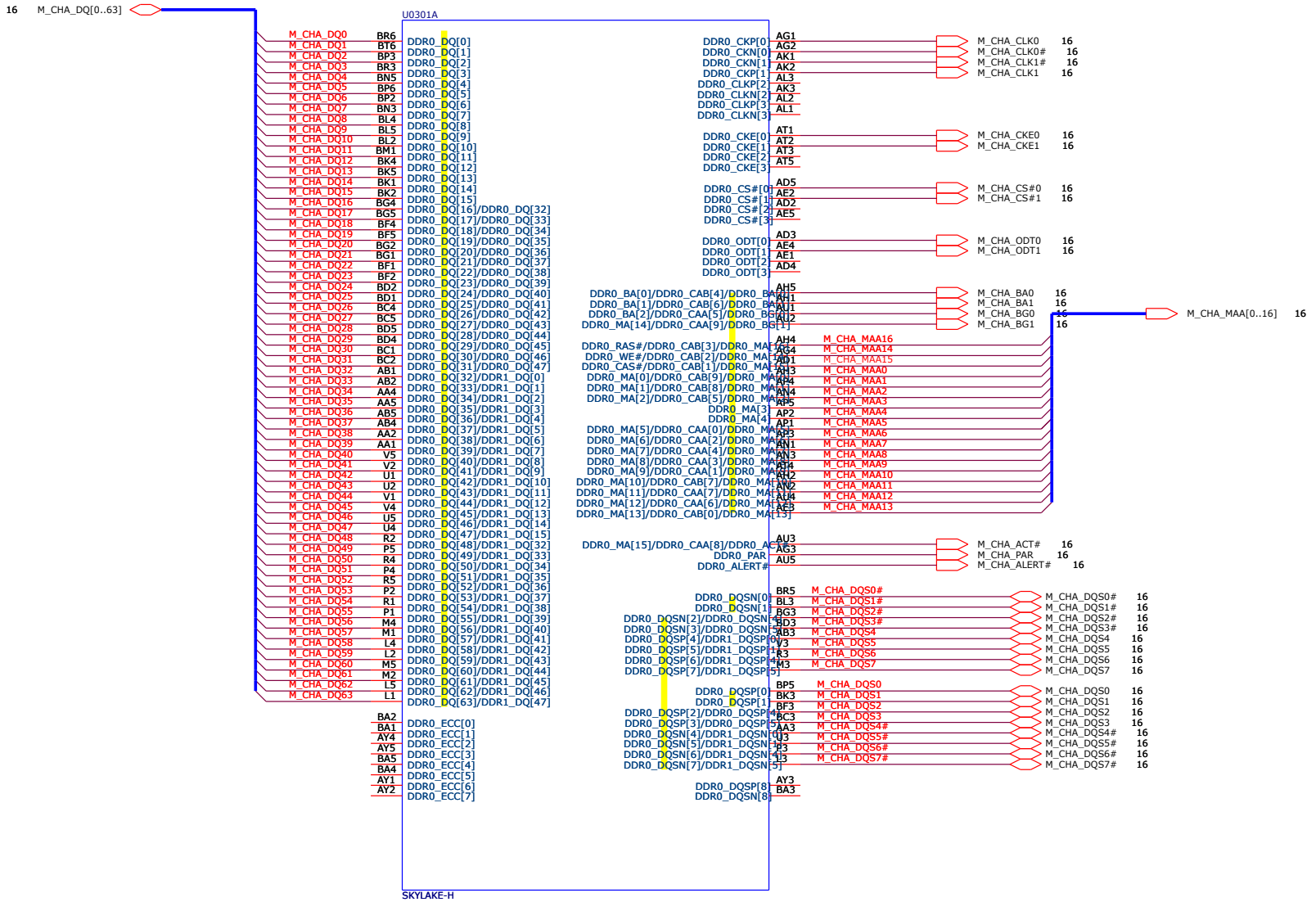
Title : CPU_DDI/EDP

Engineer: Allen_Kuo

Size	Project Name	Rev
A	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 3 of 108

04.CPU DDR4 Channel0



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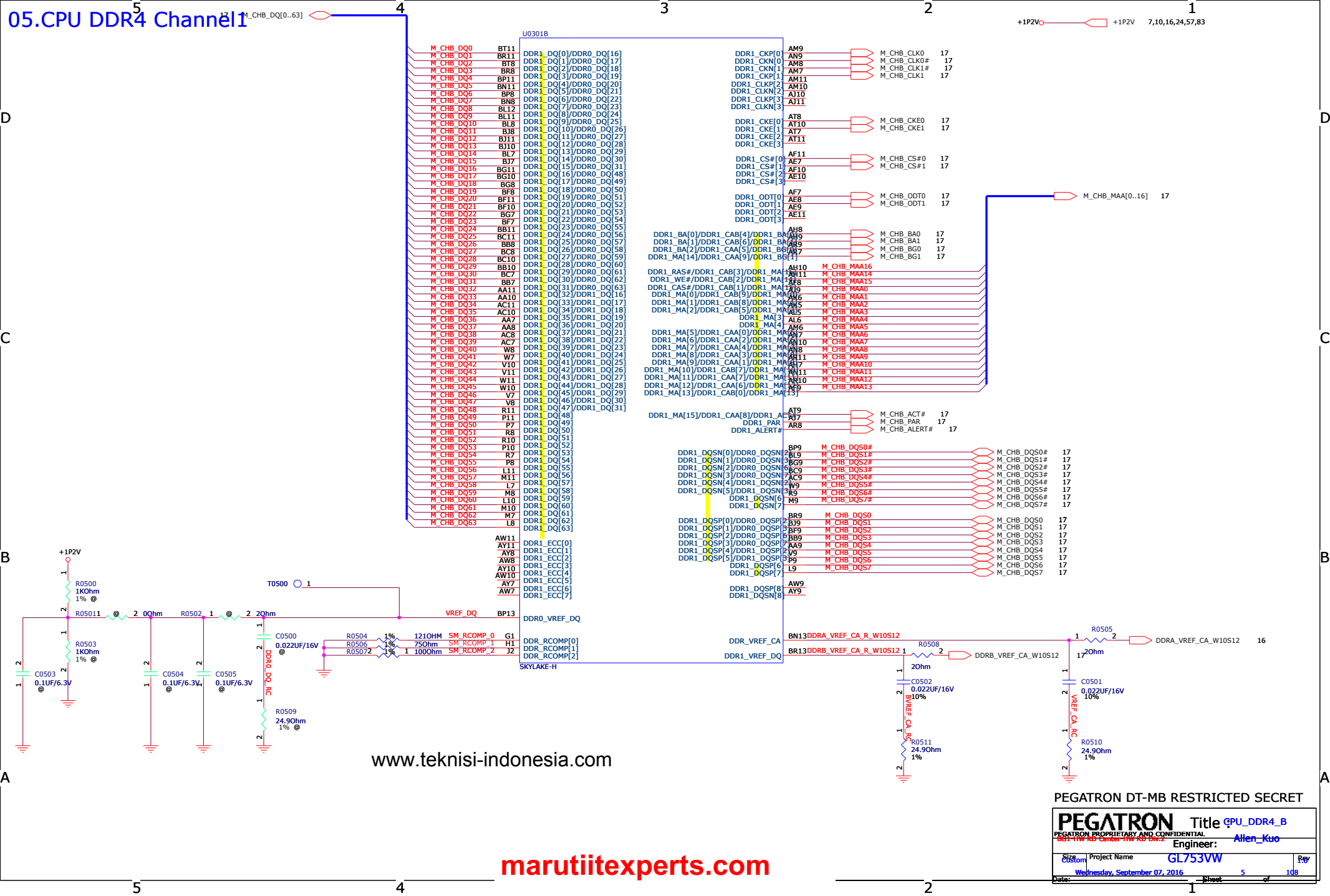
DST-HW RD Center-HW RD Div.2

Title : CPU_DDR4_A
Engineer: Allen_Kuo

Size	Project Name	Rev
A3	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 4 of 108

05.CPU DDR4 Channel1



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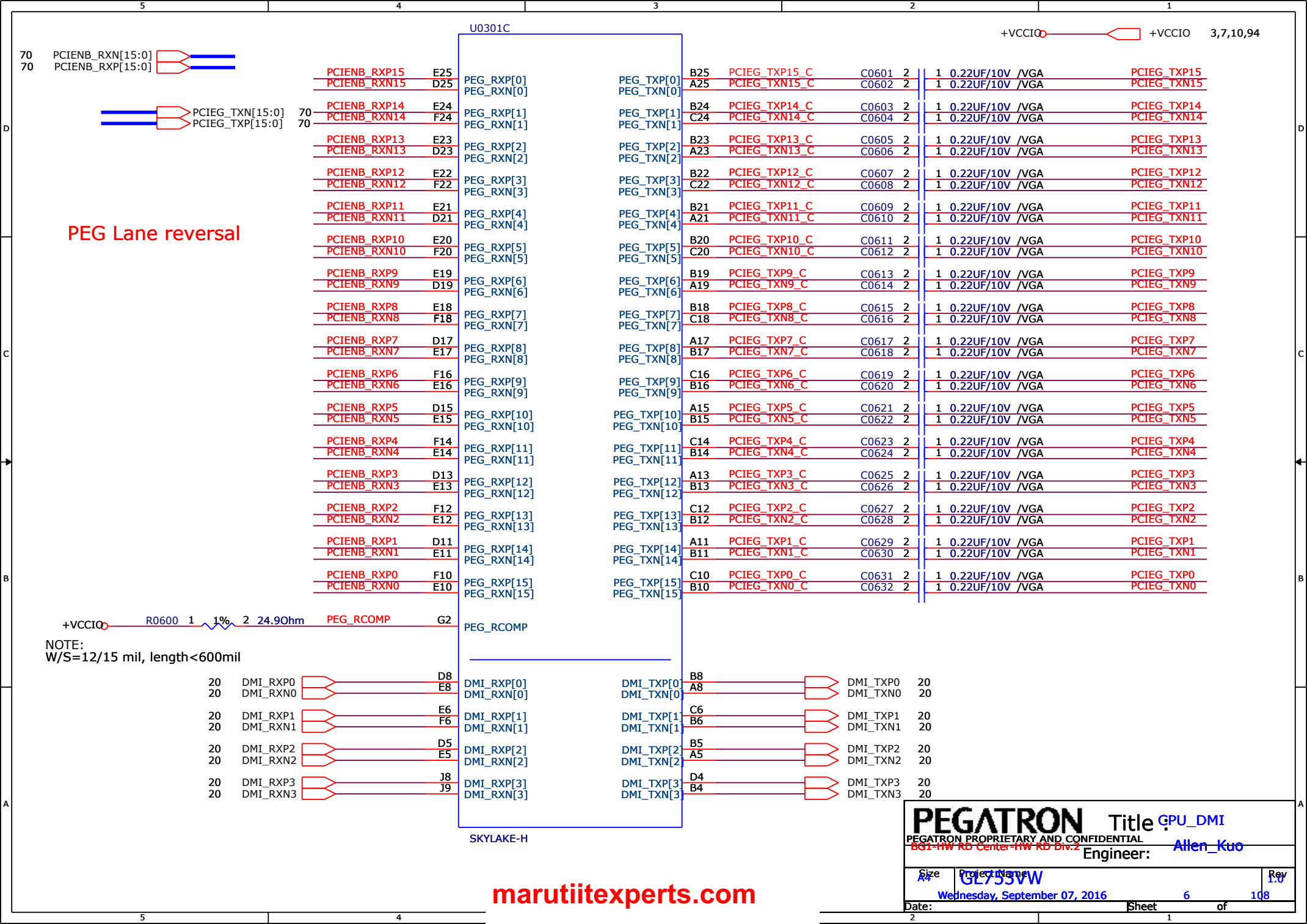
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title:	GPU_DDR4_B	
Engineer:	Allen_Kuo	
Size: Custom	Project Name: GL753VW	Rev: 1.0
Date: Wednesday, September 07, 2016	Sheet 5 of 108	



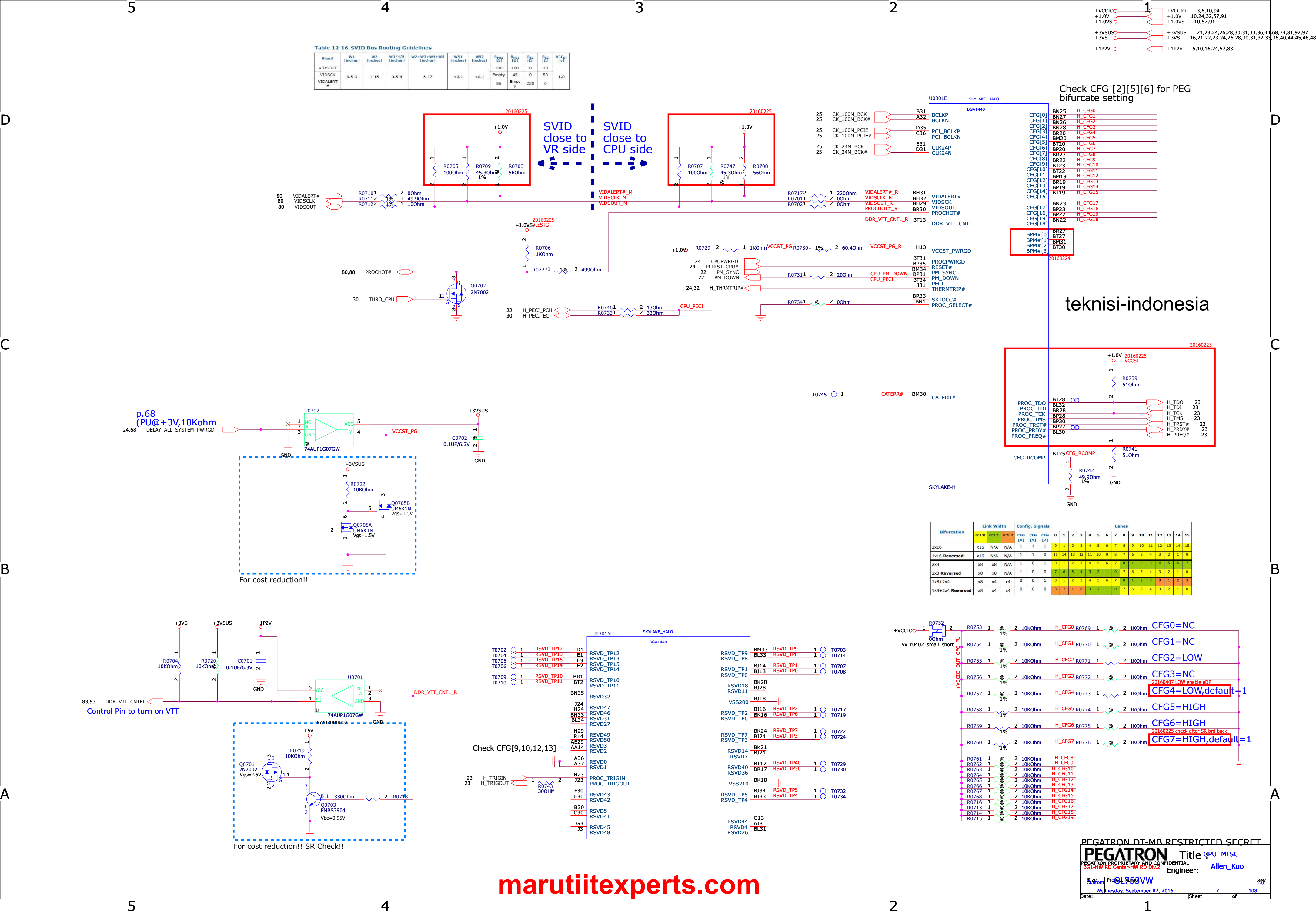


Table 12-16. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Bifurcation	Link Width			Config. Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

PEGATRON DT-MB RESTRICTED SECRET

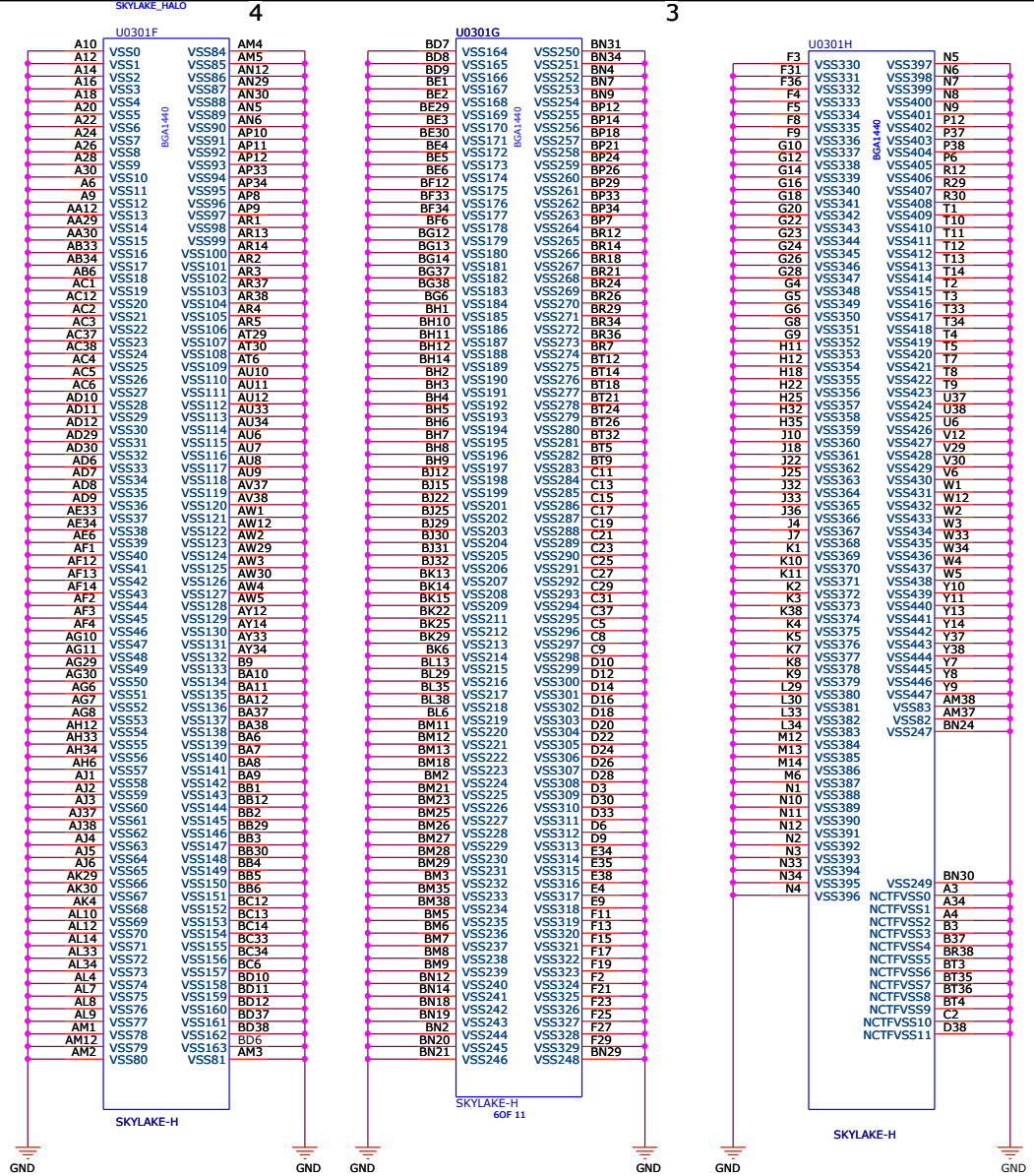
PEGATRON

Title: CPU_MISC

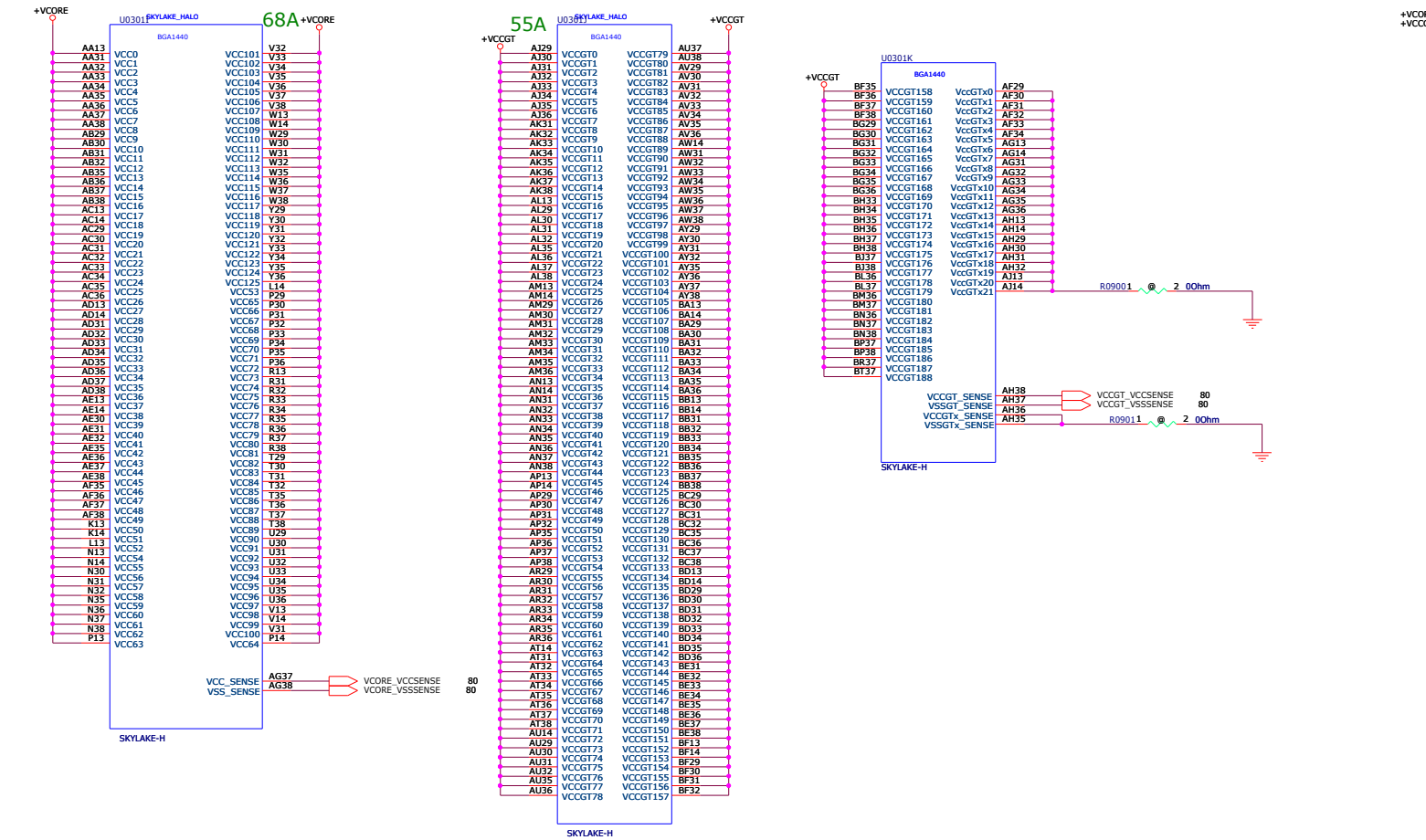
Engineer: Allen_Kuo

Size: Custom Project Name: GL753VW Rev: 1.0

Date: Wednesday, September 07, 2016 Sheet 7 of 108



Title :	CPU_VSS
Engineer:	Allen_Kuo
Size: A3	Project Name: GL753VW
Rev: 1.0	
Date: Wednesday, September 07, 2016	Sheet 8 of 108



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PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: GPU_POWER1
Engineer: Allen_Kuo
Size: C
Project Name: GE7 959W
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet 9 of 103

546884_SKL_PDG_H_rev2_0 (p.622
Skylake processor will internally power gate the VDDQ rail, system context is in suspended-to-RAM state, and SKL PCH-LP placed in Deep Sx state. Therefore, unlike previous platform, there is no need to externally gate the VDDQ rail of the **Processor.**

Seq15. VCCSA

Seq13. VDDQ

Seq14. VccIO

Seq13. VccPLL_OC

Seq10. VCCST

Seq11. VCCSTG

Seq10. VCCPLL

+VCCSA +VCCSA 80
+VCCIO +VCCIO 3,6,7,94
+1P2V +1P2V 5,7,16,24,57,83

U0301L SKYLAKE_HALO BGA1440

VCCSA: J30 K29 K30 K31 K32 K33 K34 K35 L31 L32 L35 L36 L37 L38 M29 M30 M31 M32 M33 M34 M35 M36 — VCCSA0 VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8 VCCSA9 VCCSA10 VCCSA11 VCCSA12 VCCSA13 VCCSA14 VCCSA15 VCCSA16 VCCSA17 VCCSA18 VCCSA19 VCCSA20 VCCSA21

VCCIO: AG12 G15 G17 G19 G21 H15 H16 H17 H19 H20 H21 H26 H27 J15 J16 J17 J19 J20 J21 J26 J27 — VCCIO0 VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20

VDDQ: AA6 AE12 AF5 AF6 AG5 AG9 AJ12 AL11 AP6 AP7 AR12 AR6 AT12 AW6 AY6 J5 J6 K12 K6 L12 L6 R6 T6 W6 — VDDQ0 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18 VDDQ19 VDDQ20 VDDQ21 VDDQ22 VDDQ23

VDDQC: Y12

VCCPLL_OC: BH13 G11 — VCCPLL_OC0 VCCPLL_OC1

VCCST: H30

VCCSTG: H29 G30 — VCCSTG1 VCCSTG0

VccPLL: H28 J28 — VccPLL0 VccPLL1

VCCSA_SENSE M38 — VCCSA_VCCSENSE 80
VSSSA_SENSE M37 — VCCSA_VSSSENSE 80
VCCIO_SENSE H14 — T1003
VSSIO_SENSE J14 — T1002

SKYLAKE-H

+1P2V_CPU
R1001 0Ohm
C1000 22UF/6.3V
C1001 1UF/6.3V
C1002 1UF/6.3V
+1.0V
C1003 4.7UF/10V
+1.0VS
C1004 1UF/6.3V
C1005 1UF/6.3V
+1.0V
C1006 4.7UF/10V X5R/+/-10%

U0301M SKYLAKE_HALO BGA1440

R1000 1 @ 2 0Ohm — BJ17 BJ19 BJ20 BK17 BK19 BK20 BL16 BL17 BL18 BL19 BL20 BL21 BM17 BN17 — VCCOPC0 VCCOPC1 VCCOPC2 VCCOPC3 VCCOPC4 VCCOPC5 VCCOPC6 VCCOPC7 VCCOPC8 VCCOPC9 VCCOPC10 VCCOPC11 VCCOPC12 VCCOPC13

R1002 1 @ 2 0Ohm — BJ23 BJ26 BJ27 BK23 BK26 BK27 BL23 BL24 BL25 BL26 BL27 BL28 BM24 — RSVD8 RSVD9 RSVD10 RSVD15 RSVD16 RSVD17 RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD29

R1003 1 @ 2 0Ohm — BL15 BM16 — VCCOPC_SENSE VSSOPC_SENSE

R1004 2 @ 1 100Ohm RSVD19 — BL22
R1005 2 @ 1 0Ohm RSVD28 — BM22 — RSVD19 RSVD28

R1006 1 @ 2 0Ohm — BP15 BR15 BT15 — VCCEOPIO0 VCCEOPIO1 VCCEOPIO2

R1007 1 @ 2 0Ohm — BP16 BR16 BT16 — RSVD33 RSVD35 RSVD39

R1008 1 @ 2 0Ohm — BN15 BM15 — VCCEOPIO_SENSE VSSEOPIO_SENSE

R1009 2 @ 1 100Ohm RSVD34 — BP17
R1010 2 @ 1 0Ohm RSVD30 — BN16 — RSVD34 RSVD30

R1011 1 @ 2 0Ohm — BM14 BL14 — VCC_OPC_1P8_1 VCC_OPC_1P8_0

R1012 1 @ 2 0Ohm — BJ35 BJ36 — RSVD12 RSVD13

T1000 1 — ZVM_TP AT13 — ZVM#
T1001 1 — MSM_TP AW13 — MSM#

R1013 2 @ 1 100Ohm — AU13 AY13 — ZVM2# MSM2#

OPC_RCOMP BT29 — OPC_RCOMP
OPCE_RCOMP BR25 — OPCE_RCOMP
OPCE_RCOMP2 BP25 — OPCE_RCOMP2

R1014 49.9Ohm 1%
R1015 49.9Ohm 1%
R1016 49.9Ohm 1%

SKYLAKE-H

JP1001 3MM_OPEN_5MIL
+1P2V — +1P2V_CPU

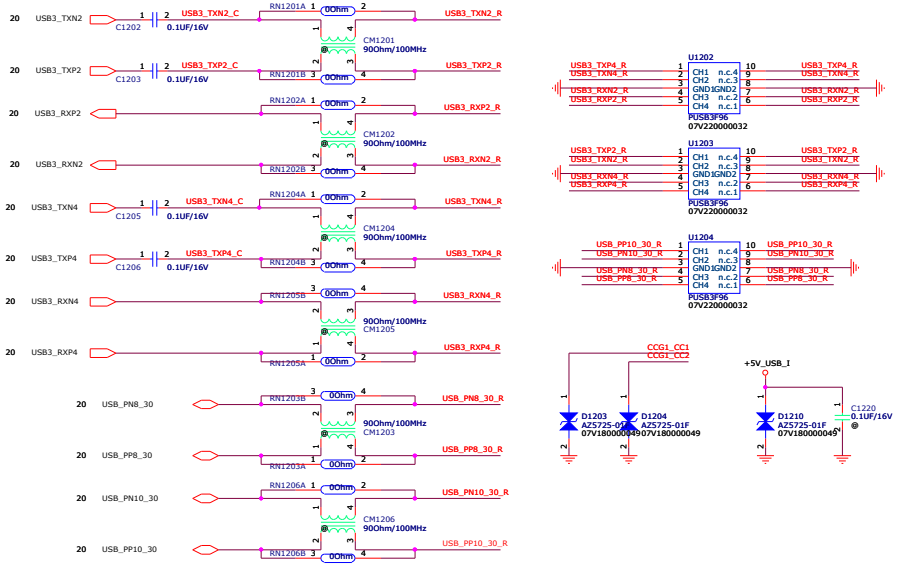
R10181 2_0Ohm vx_r0402_0ohm_small
+1P2V — +VccPLL_OC

20160307_SR no Stencil
JP1002 3MM_OPEN_5MIL
+1.0VS — +VCCIO

+1P2V_CPU
C1007 10UF/6.3V
C1008 10UF/6.3V
C1009 10UF/6.3V
C1010 10UF/6.3V
C1011 10UF/6.3V
C1012 10UF/6.3V
C1013 10UF/6.3V
C1014 10UF/6.3V
C1015 10UF/6.3V
C1016 10UF/6.3V

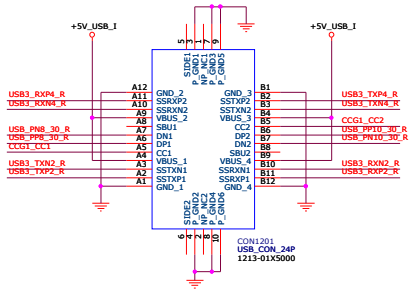
Title : CPU_POWER2
Engineer: Allen_Kuo
Size A3 | Project Name GL753VW | Rev 1.0
Date: Wednesday, September 07, 2016 | Sheet 10 of 108

Type-C

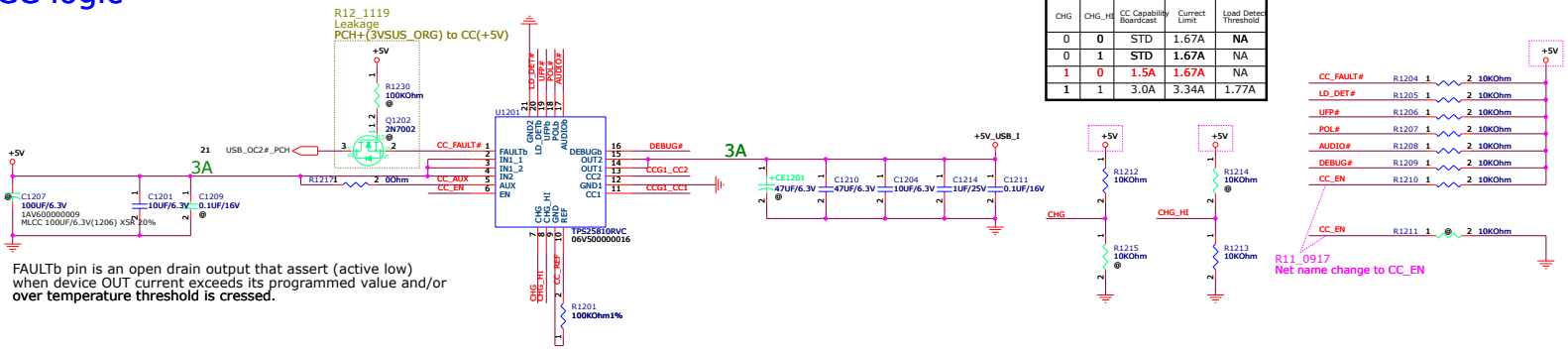


Type-C Conn.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D1+	D1-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D2-	D2+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



CC logic



FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or **over temperature threshold is cressed.**

CHG	CHG_HI	CC Capability Boardcast	Current Limit	Load Detect Threshold
0	**0**	STD	1.67A	**NA**
0	1	**STD**	**1.67A**	NA
1	**0**	**1.5A**	**1.67A**	NA
1	1	3.0A	3.34A	1.77A

PEGATRON Title : Type-C(Conn.)
PEGATRON PROPRIETARY AND CONFIDENTIAL
8G1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo
Size: Custom | Project Name: GL753VW | Rev: 1.0
Date: Wednesday, September 07, 2016 | Sheet 12 of 105

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BSI-HW RD Center-HW RD Div.2

Title : THUNDERBOLT_HDMI redriver

Engineer: Allen_Kuo

Size	Project Name	Rev
B	GL755VW	1.0

Date: Wednesday, September 07, 2016 Sheet 13 of 108

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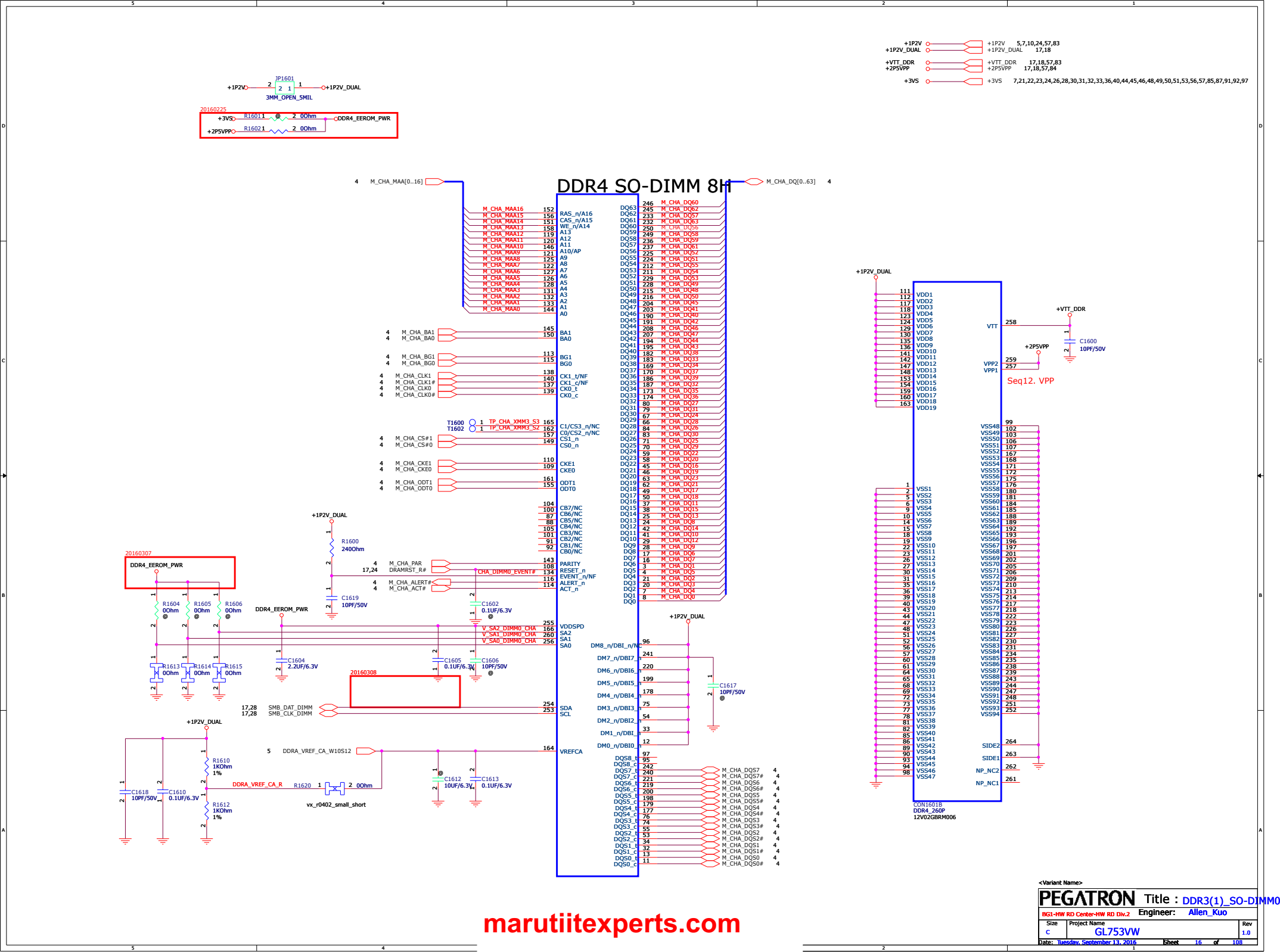
Title : THUNDERBOLT_DP redriver

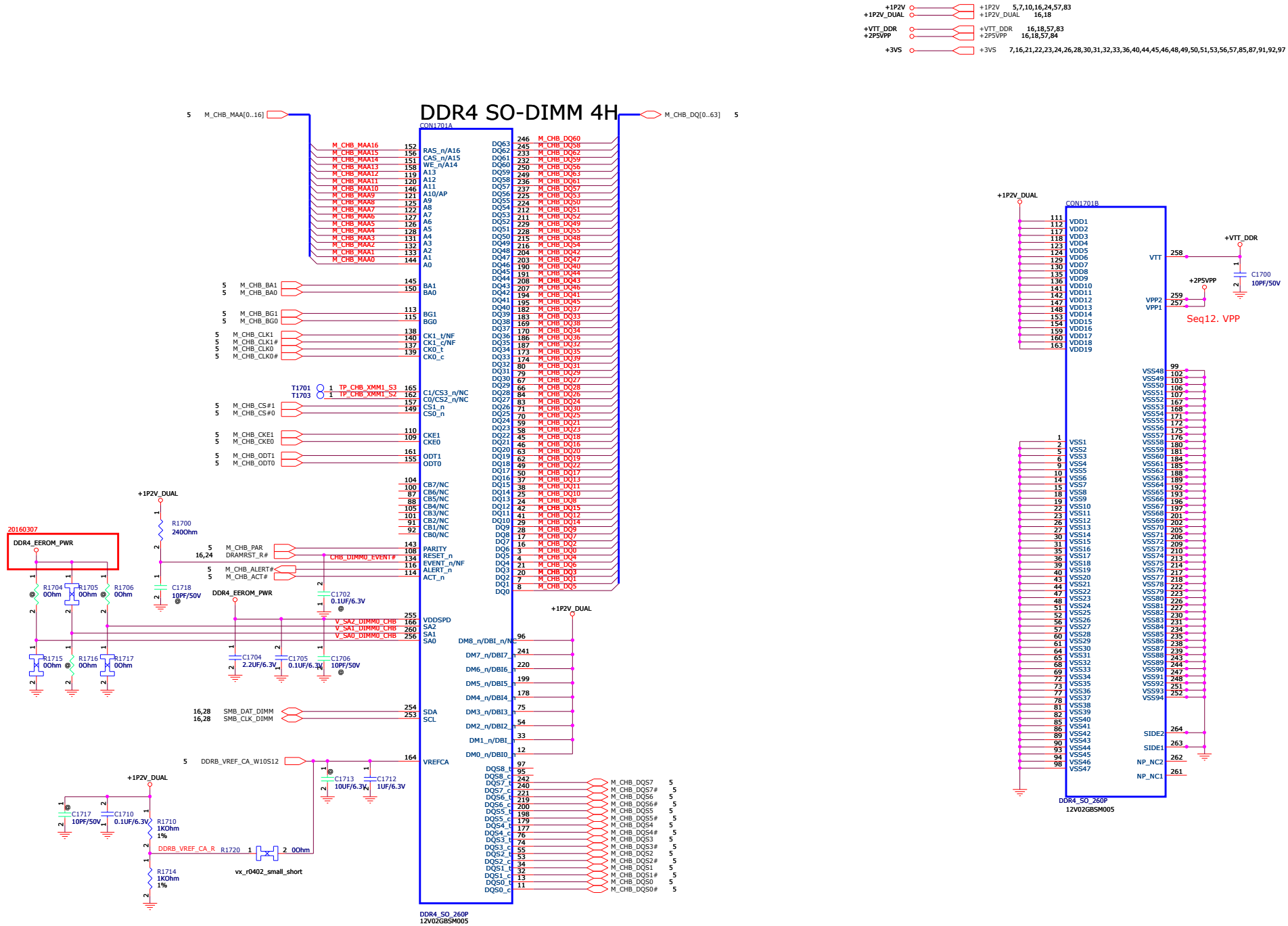
Engineer: Allen_Kuo

Size: B | Project Name: GL753VW | Rev: 1.0

Date: Wednesday, September 07, 2016 | Sheet 14 of 108



DDR4 SO-DIMM 4H



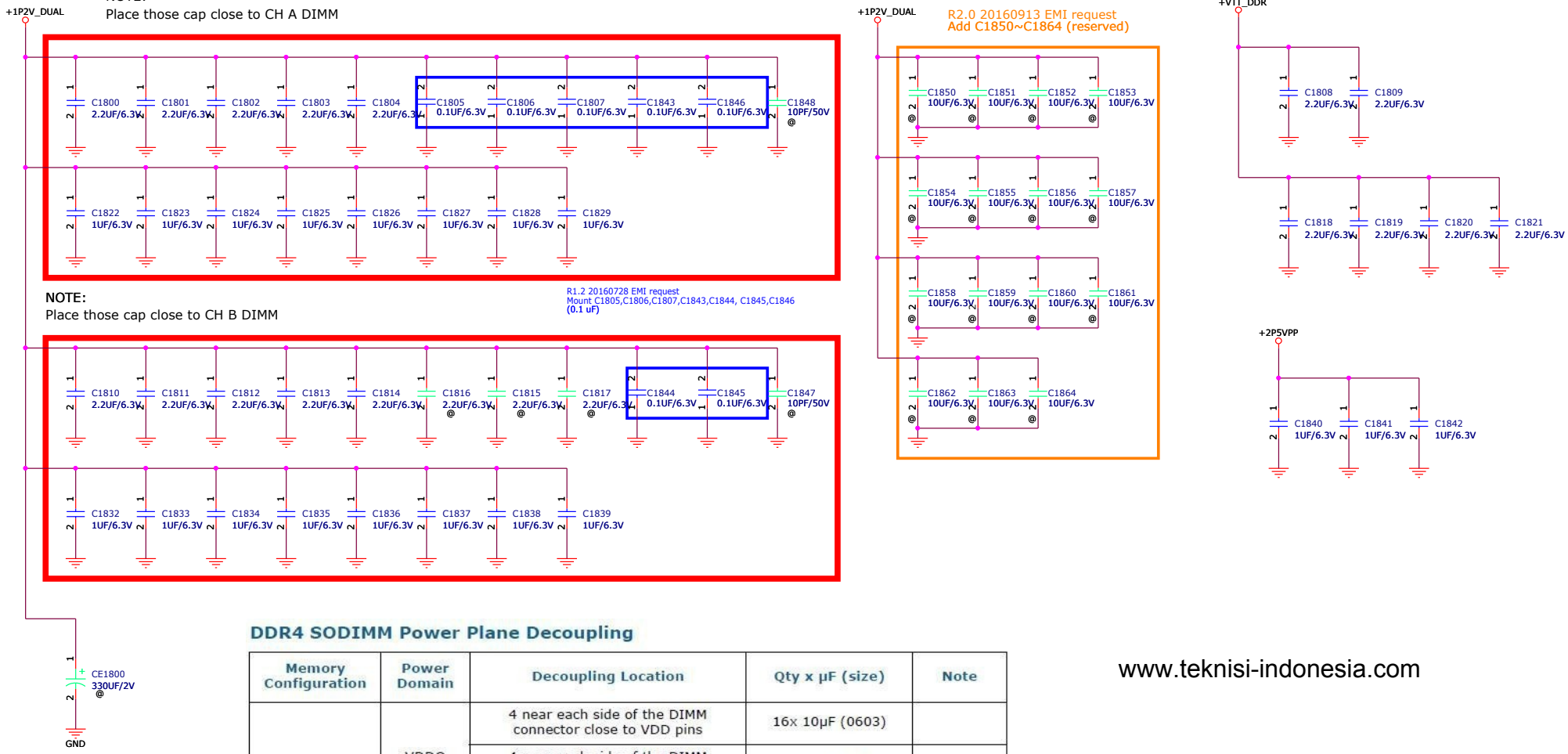
<Variant Name>

PEGATRON Title : DDR3(1)_SO-DIMM0

BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
C	GL753VW	1.0

Date: Tuesday, September 13, 2016 Sheet 17 of 108



DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1uF (0402)	
	VDDSPD	P		
		P		

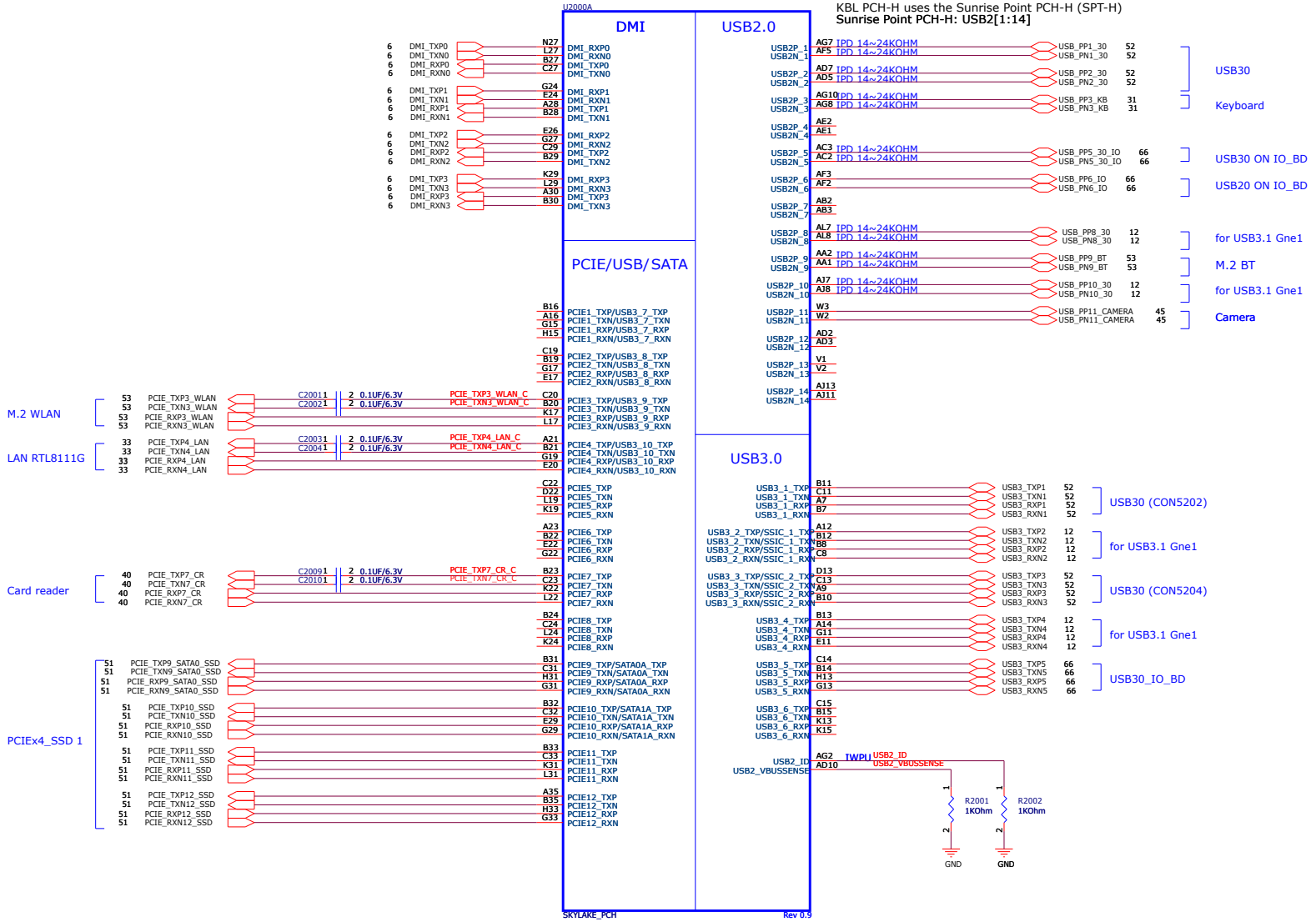
PEGATRON Title : DDR3 TERMINATION A&B

Engineer: Allen_Kuo

Size	Project Name	Rev
A3	GL753VW	1.0

Date: Tuesday, September 13, 2016 Sheet 18 of 108

NOTE:
KBL PCH-H uses the Sunrise Point PCH-H (SPT-H)
Sunrise Point PCH-H: USB2[1:14]



546884_SKL_PDG_H_rev2_0 p233 : HM170 doesn't support PCIE17-20

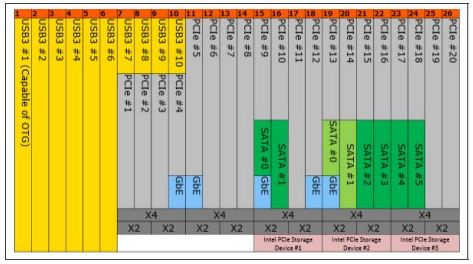


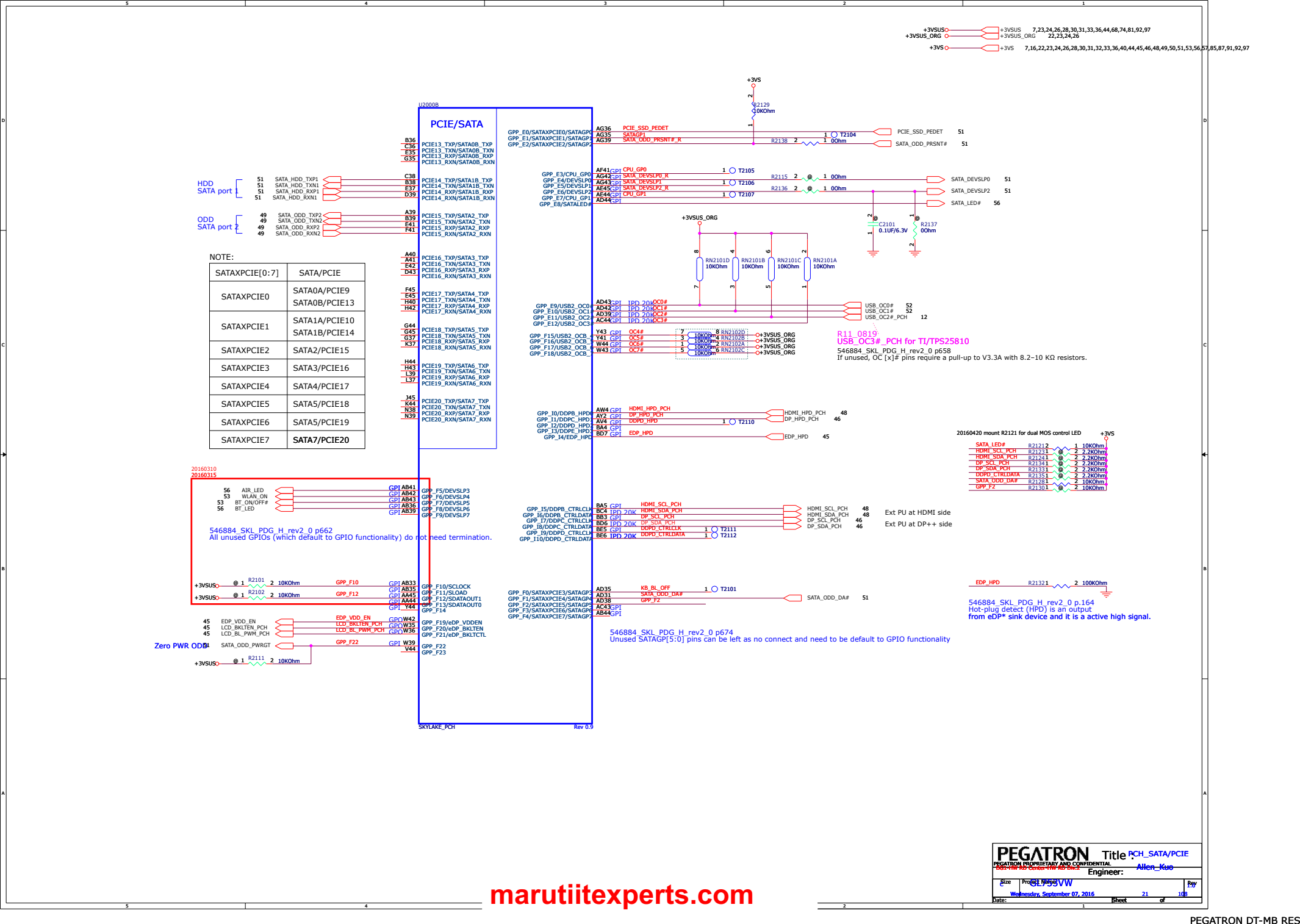
Table 1-3. PCH-H HSIO Detail (Lane 1-14)

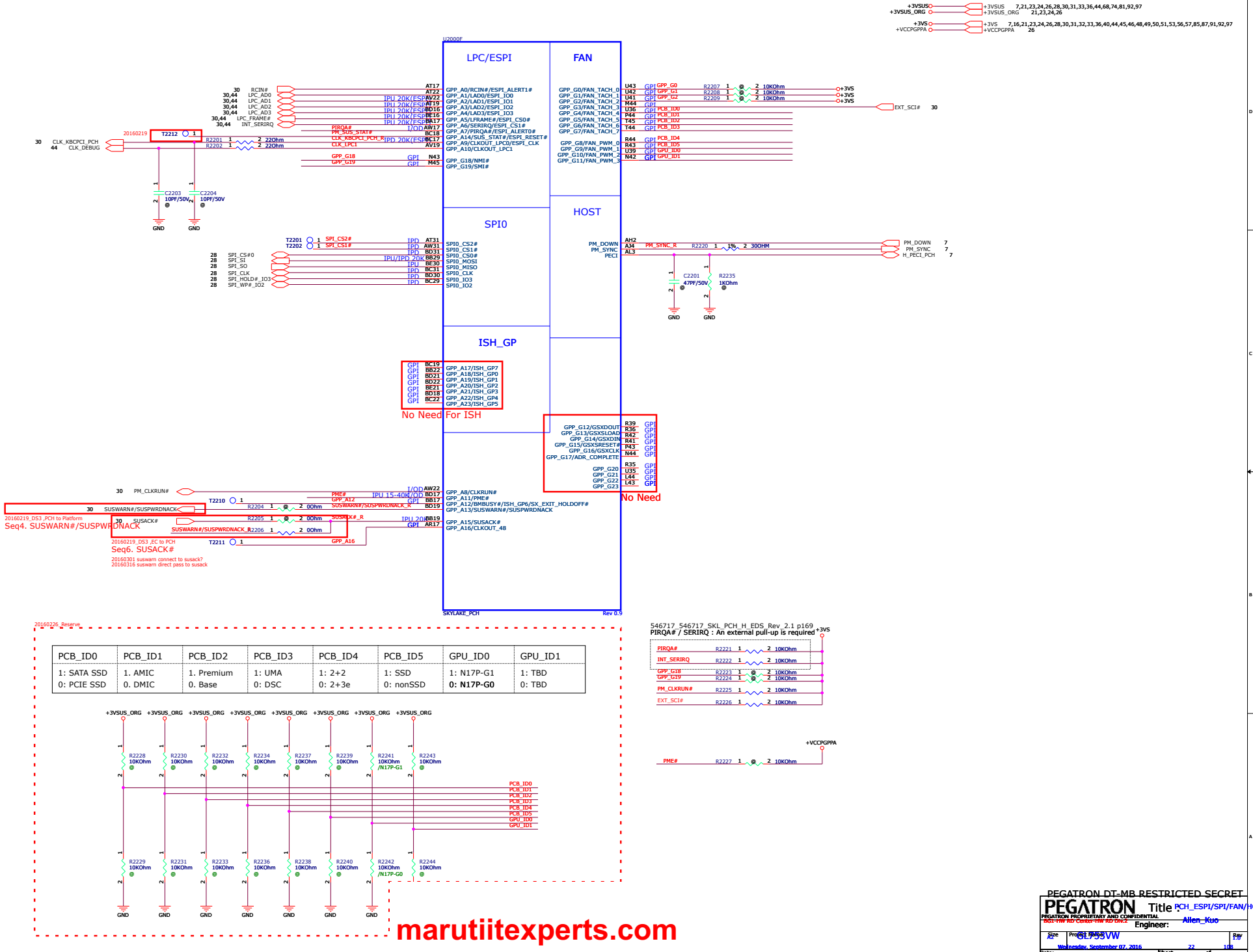
SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
HM170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15[1]	16[1]	17	18	19[1]	20[1]	21	22	23	24	25	26
HM170	PCIe/LAN /SATA0	PCIe/ LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/ LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A

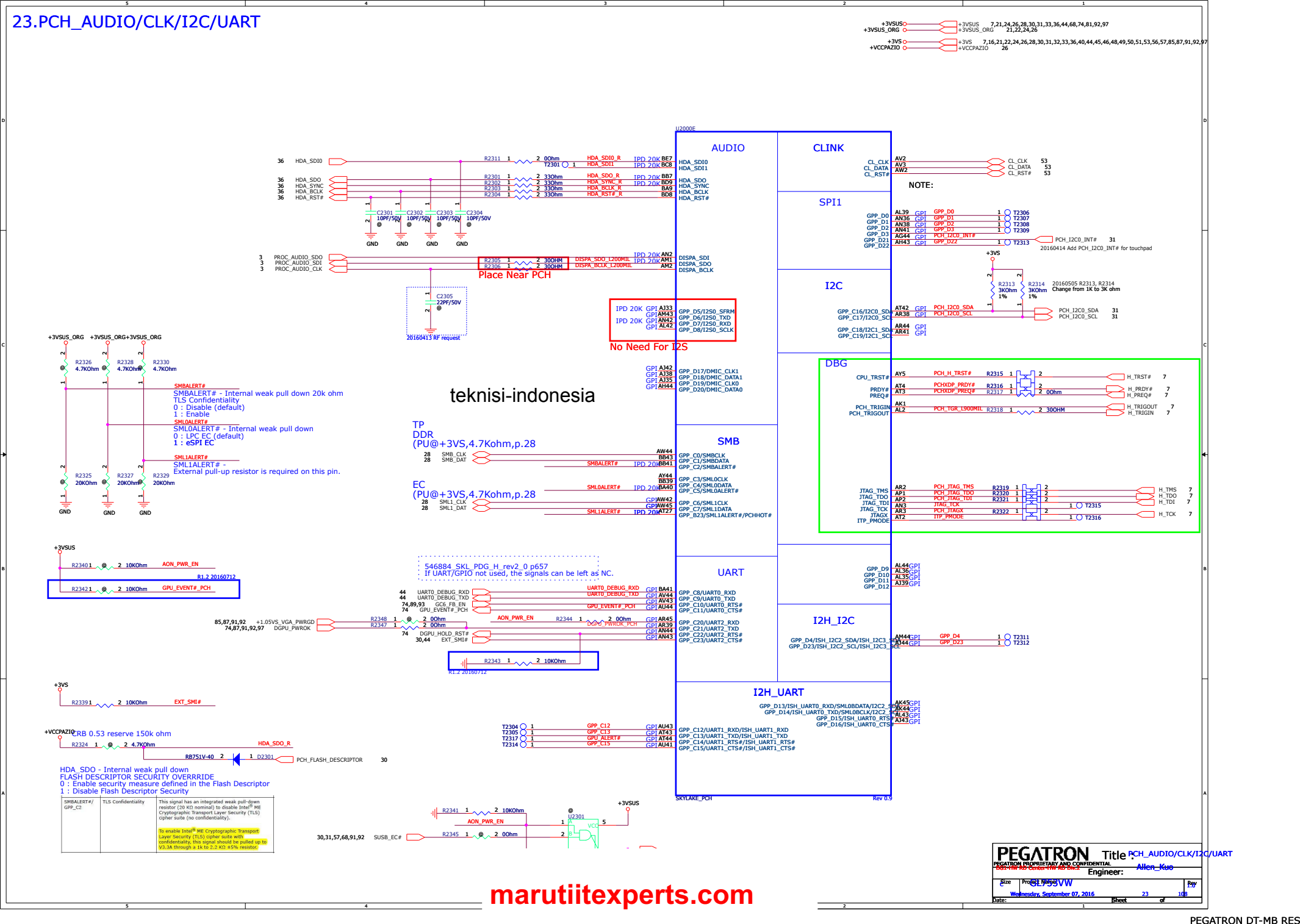
Title: PCH_DMI/PCIE
Engineer: Allen_Kuo
Size: C | Project Name: GL753VW | Rev: 1.0
Date: Wednesday, September 07, 2016 | Sheet 20 of 103

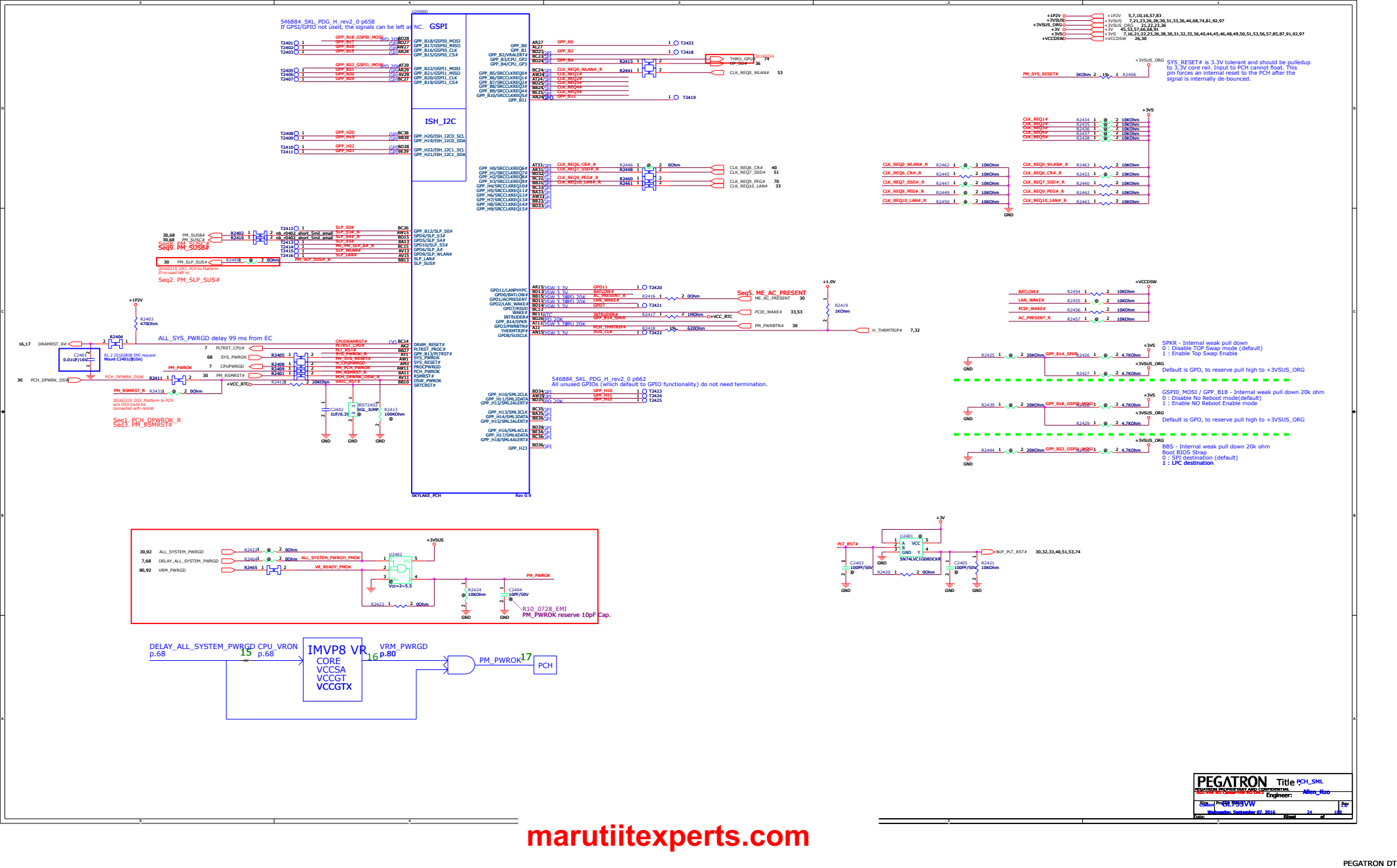


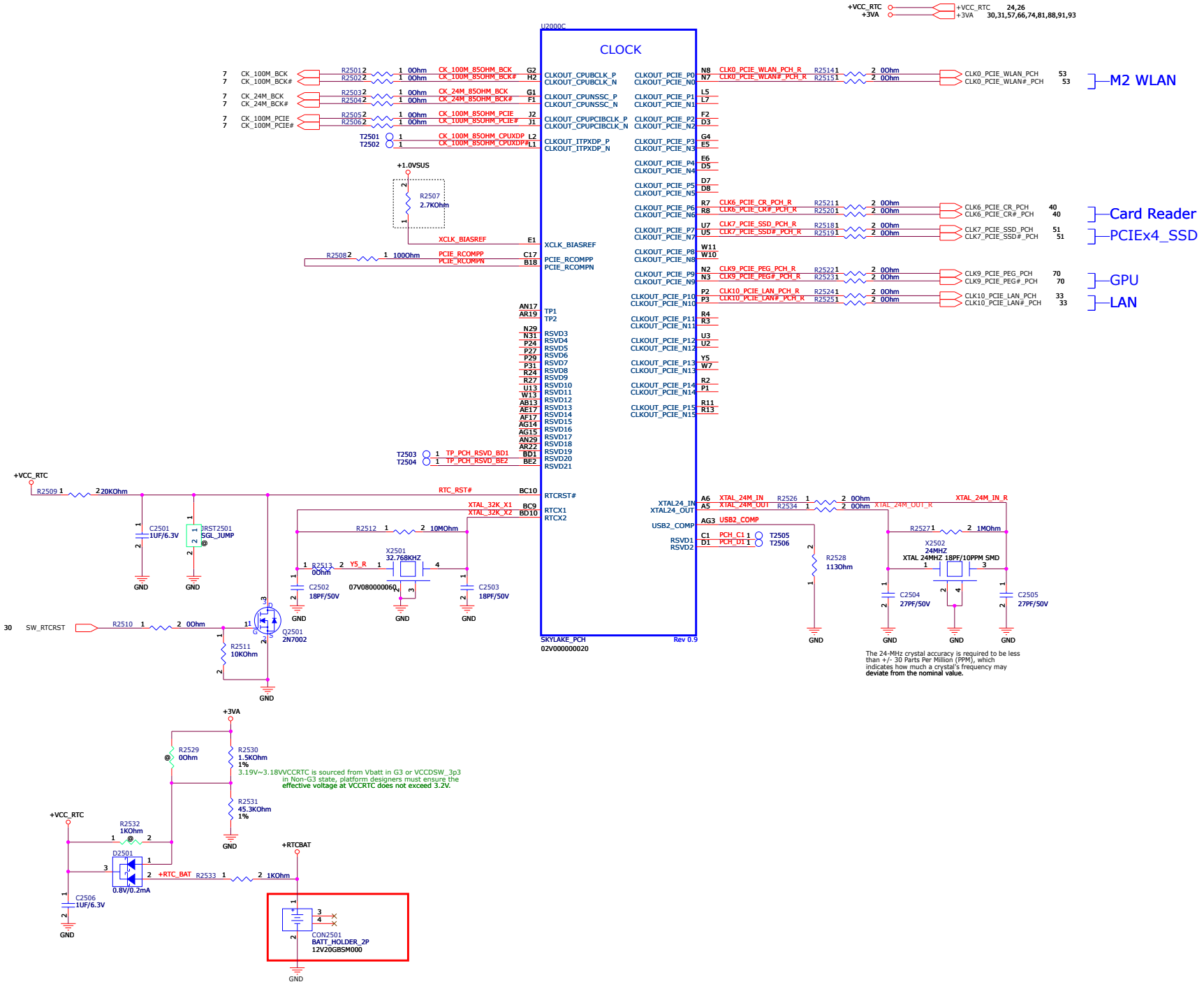


PCB_ID0	PCB_ID1	PCB_ID2	PCB_ID3	PCB_ID4	PCB_ID5	GPU_ID0	GPU_ID1
1: SATA SSD 0: PCIE SSD	1. AMIC 0. DMIC	1. Premium 0. Base	1: UMA 0: DSC	1: 2+2 0: 2+3e	1: SSD 0: nonSSD	1: N17P-G1 **0: N17P-G0**	1: TBD 0: TBD

23.PCH_AUDIO/CLK/I2C/UART







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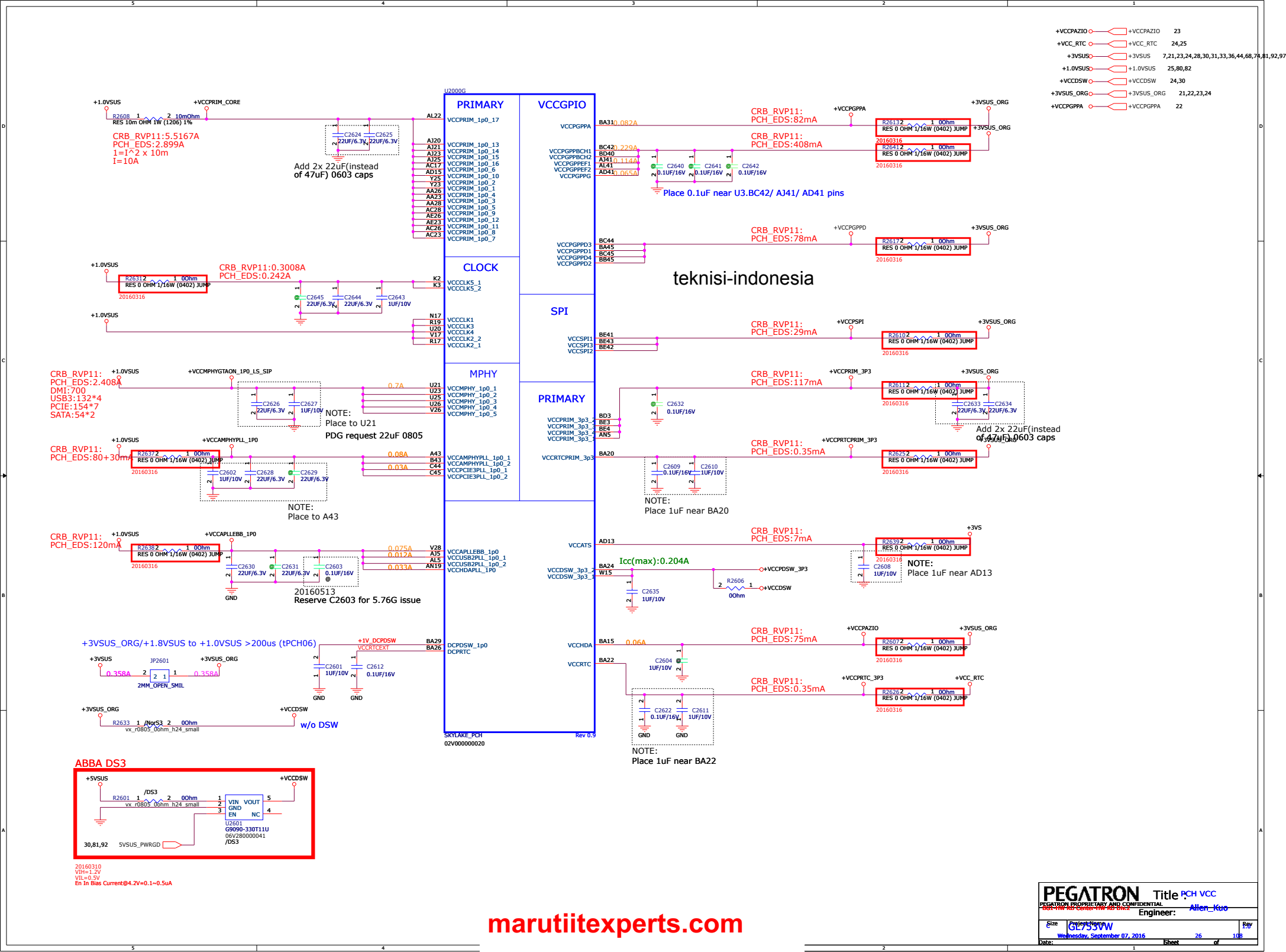
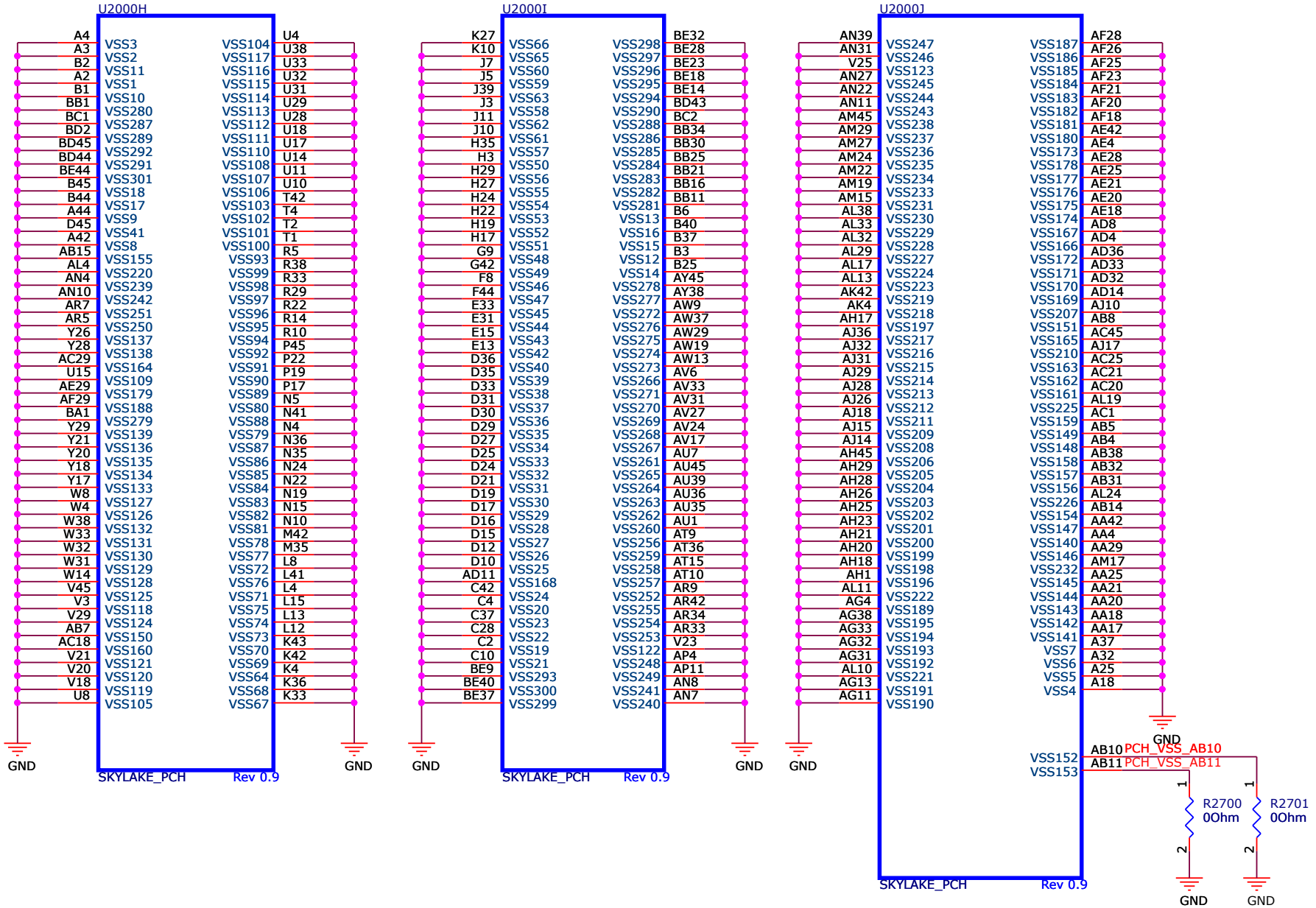
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH_CLOCK
Engineer: Allen_Kuo
Size: C
Project Name: GL753W
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet 25 of 108


+VCCPAZIO +VCCPAZIO 23
+VCC_RTC +VCC_RTC 24,25
+3VSUS +3VSUS 7,21,23,24,28,30,31,33,36,44,68,74,81,92,97
+1.0VSUS +1.0VSUS 25,80,82
+VCCDSW +VCCDSW 24,30
+3VSUS_ORG +3VSUS_ORG 21,22,23,24
+VCCPGPPA +VCCPGPPA 22
U2000G
PRIMARY
VCCGPIO
CLOCK
SPI
MPHY
PRIMARY
SKYLAKE_PCH
02V000000020
Rev 0.9
CRB_RVP11:5.5167A
PCH_EDS:2.899A
1=I^2 x 10m
I=10A
Add 2x 22uF(instead of 47uF) 0603 caps
CRB_RVP11:0.3008A
PCH_EDS:0.242A
CRB_RVP11:
PCH_EDS:2.408A
DMI:700
USB3:132*4
PCIE:154*7
SATA:54*2
NOTE:
Place to U21
PDG request 22uF 0805
CRB_RVP11:
PCH_EDS:80+30mA
NOTE:
Place to A43
CRB_RVP11:
PCH_EDS:120mA
20160513
Reserve C2603 for 5.76G issue
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)
w/o DSW
ABBA DS3
20160310
VIH=1.2V
VIL=0.5V
En In Bias Current@4.2V=0.1~0.5uA
CRB_RVP11:
PCH_EDS:82mA
CRB_RVP11:
PCH_EDS:408mA
Place 0.1uF near U3.BC42/ AJ41/ AD41 pins
CRB_RVP11:
PCH_EDS:78mA
teknisi-indonesia
CRB_RVP11:
PCH_EDS:29mA
CRB_RVP11:
PCH_EDS:117mA
Add 2x 22uF(instead of 47uF) 0603 caps
CRB_RVP11:
PCH_EDS:0.35mA
NOTE:
Place 1uF near BA20
CRB_RVP11:
PCH_EDS:7mA
Icc(max):0.204A
NOTE:
Place 1uF near AD13
CRB_RVP11:
PCH_EDS:75mA
CRB_RVP11:
PCH_EDS:0.35mA
NOTE:
Place 1uF near BA22
PEGATRON
Title: PCH VCC
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Allen_Kuo
Size: C
Project Name: GL753W
Rev: 1.0
Wednesday, September 07, 2016
Sheet 26 of 108
marutiitexperts.com



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RD Center-HW RD Div.2

Title: PCH_VSS

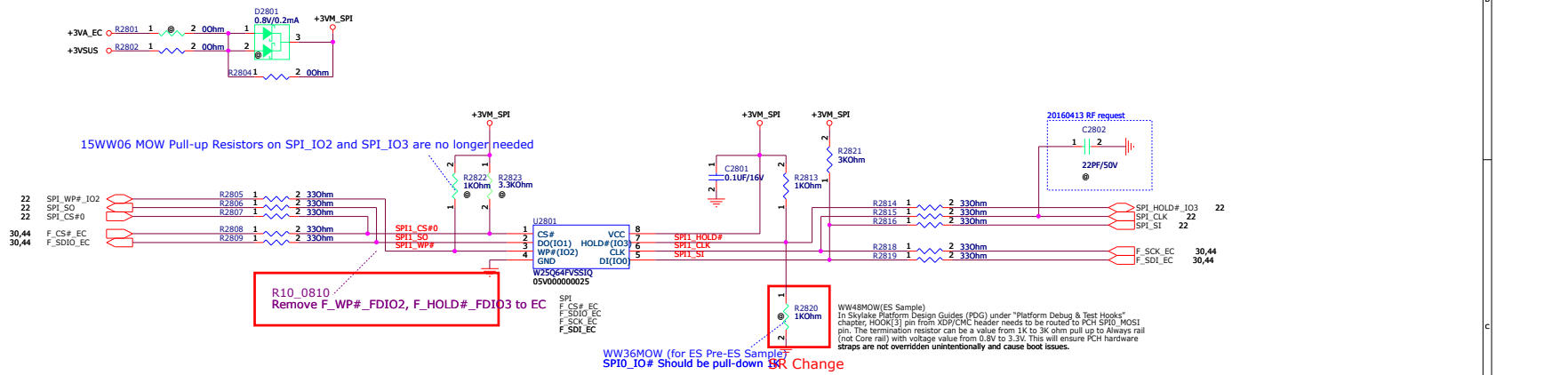
Engineer: Allen_Kuo

GL752VW

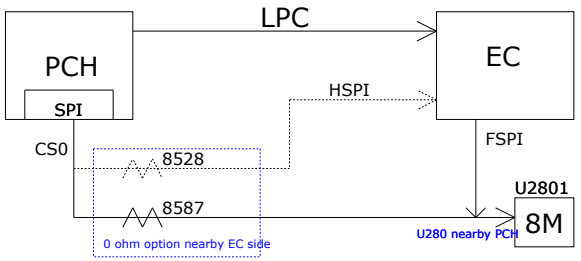
Size	Project Name	Rev
A4		1.0

Date: Wednesday, September 07, 2016 Sheet 27 of 108

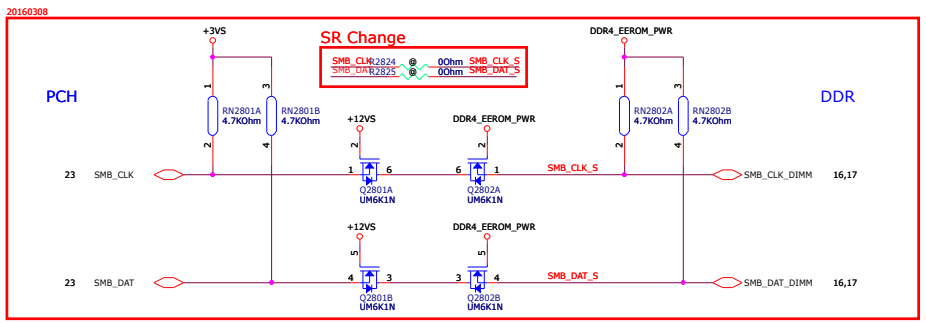
SPI ROM

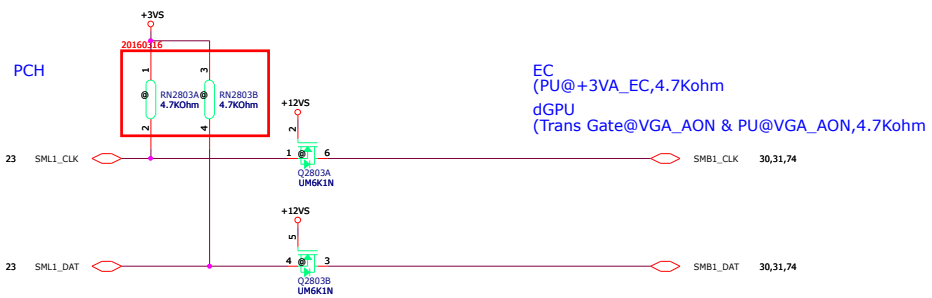


EC co-lay 8528/8587
SPI Structure

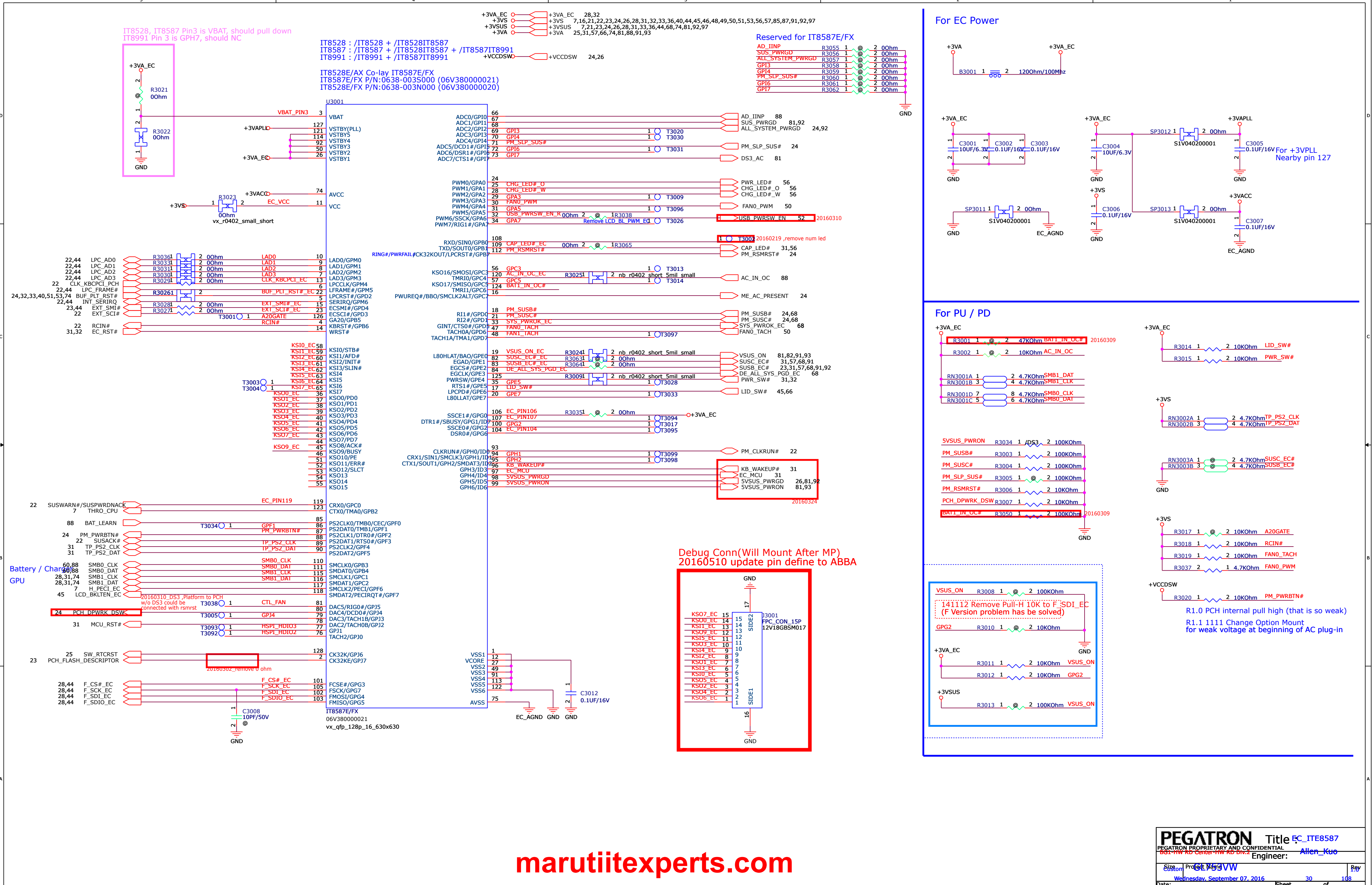


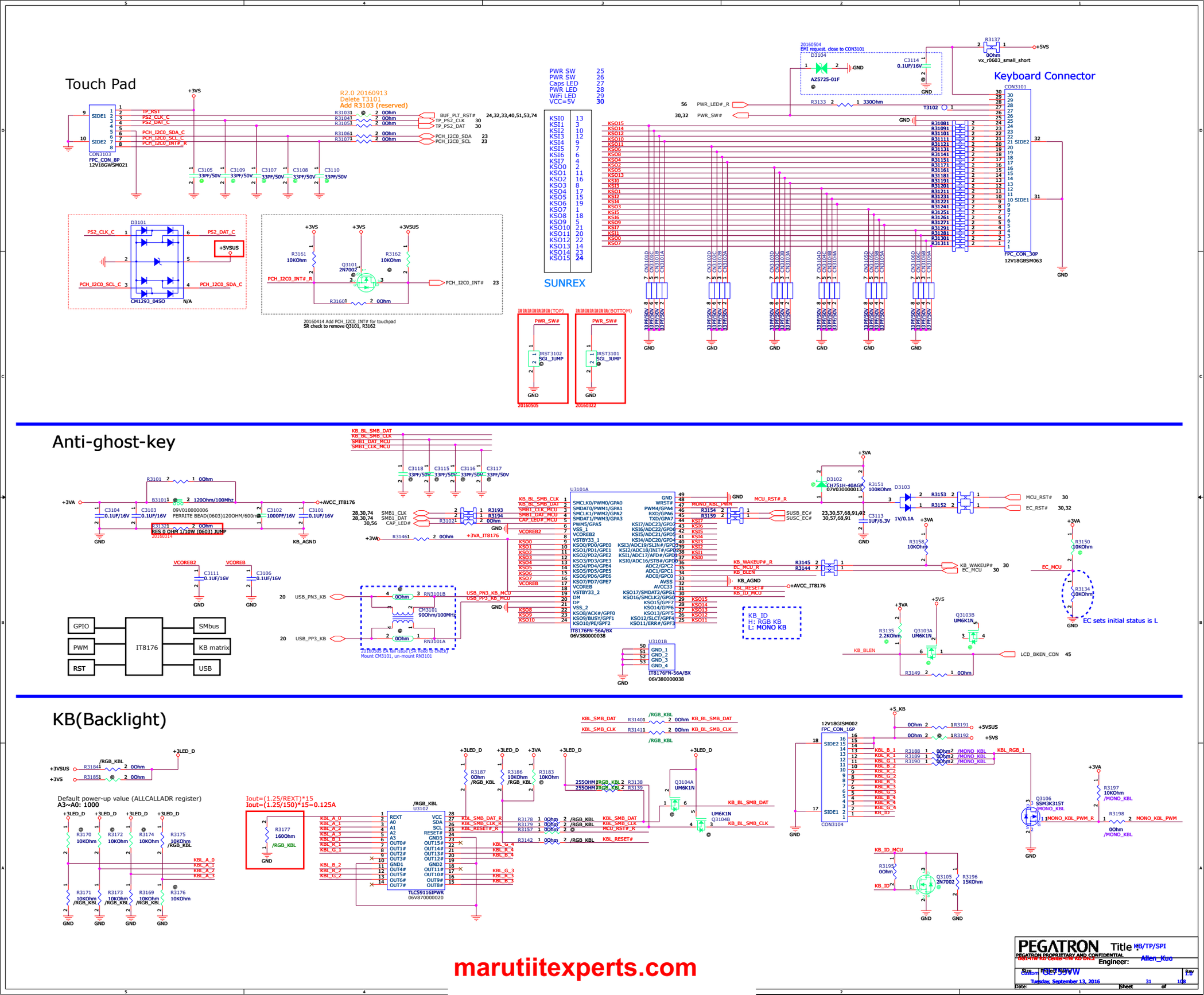
SMBus



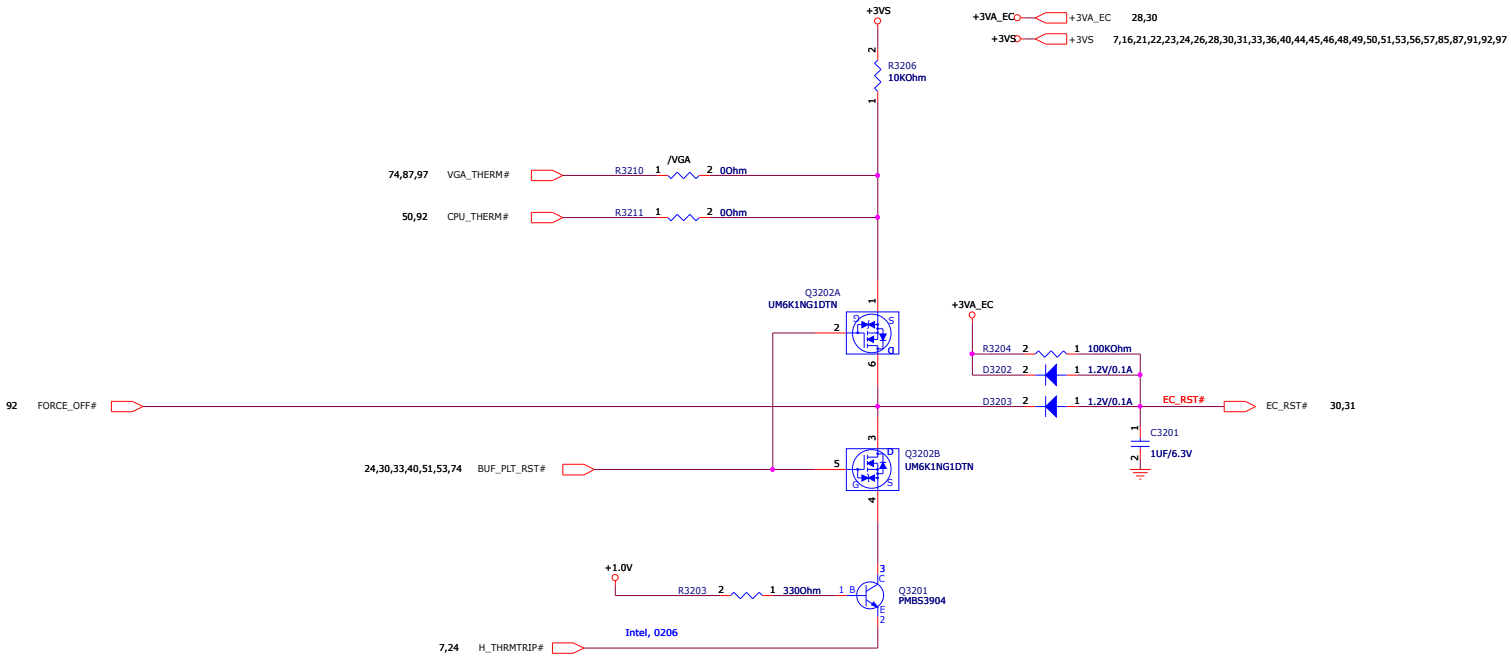


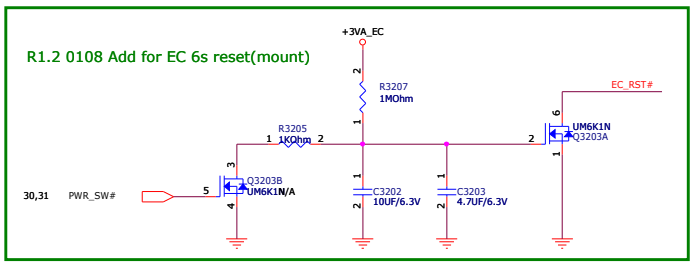
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : SPI ROM/SMbus
Engineer: Allen_Kuo
Size C
Project Name QL753W
Rev 1.0
Date: Wednesday, September 07, 2016
Sheet 28 of 108




Touch Pad
Keyboard Connector
SUNREX
Anti-ghost-key
KB(Backlight)
IT8176
GPIO
PWM
RST
SMbus
KB matrix
USB
marutiitexperts.com
PEGATRON
Title : KB/TP/SPI
Engineer: Allen_Kuo
Tuesday, September 13, 2016

Thermal Policy





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

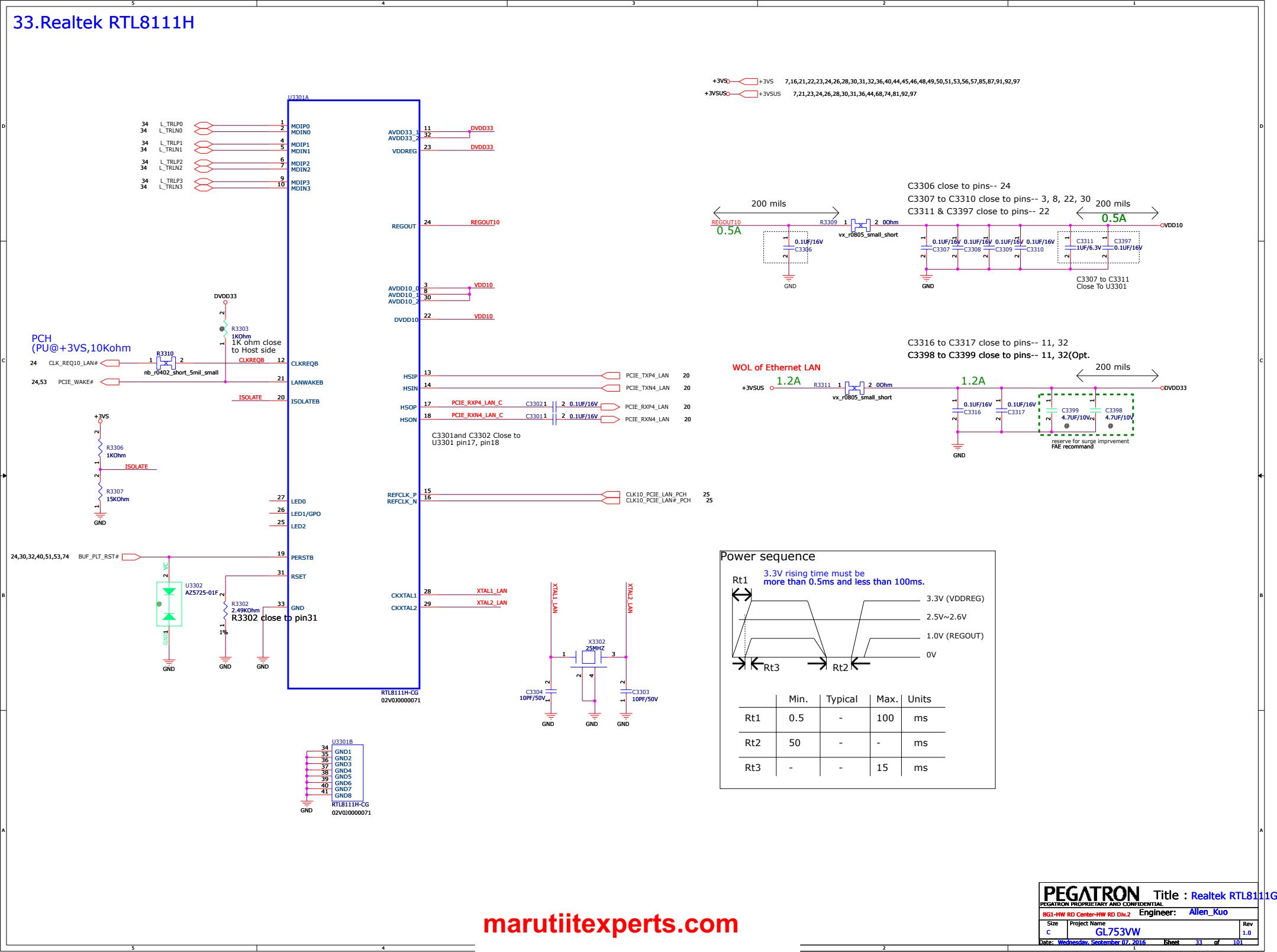
Title : RST_Reset Circuit

BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
C	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 32 of 101

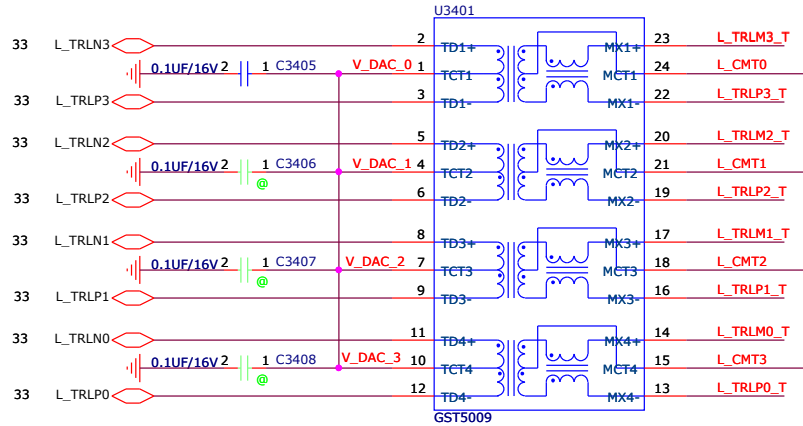
33.Realtek RTL8111H

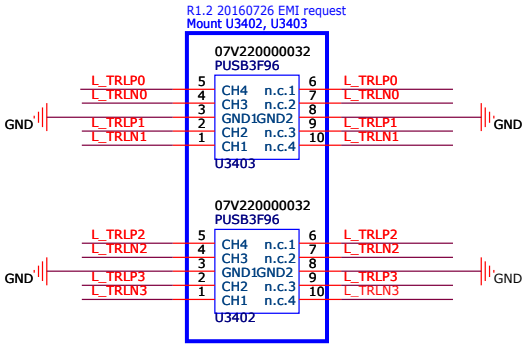


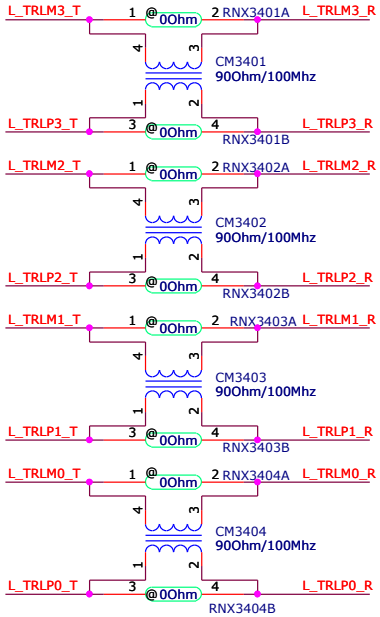
	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

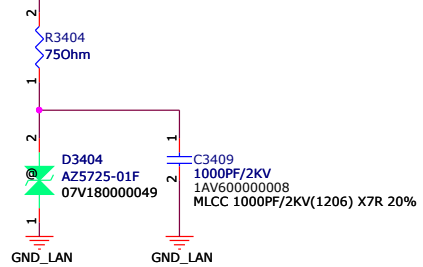
PEGATRON Title : Realtek RTL8111G
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo
Size C | Project Name GL753VW | Rev 1.0
Date: Wednesday, September 07, 2016 Sheet 33 of 101

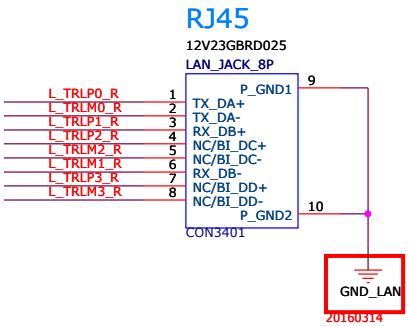
34.Transformer/RJ45

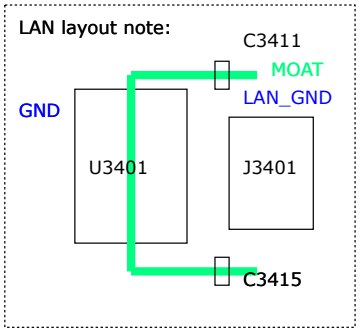


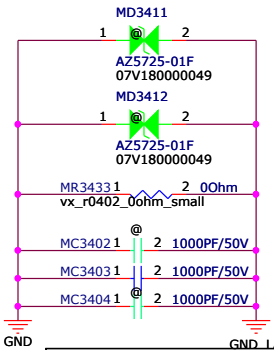












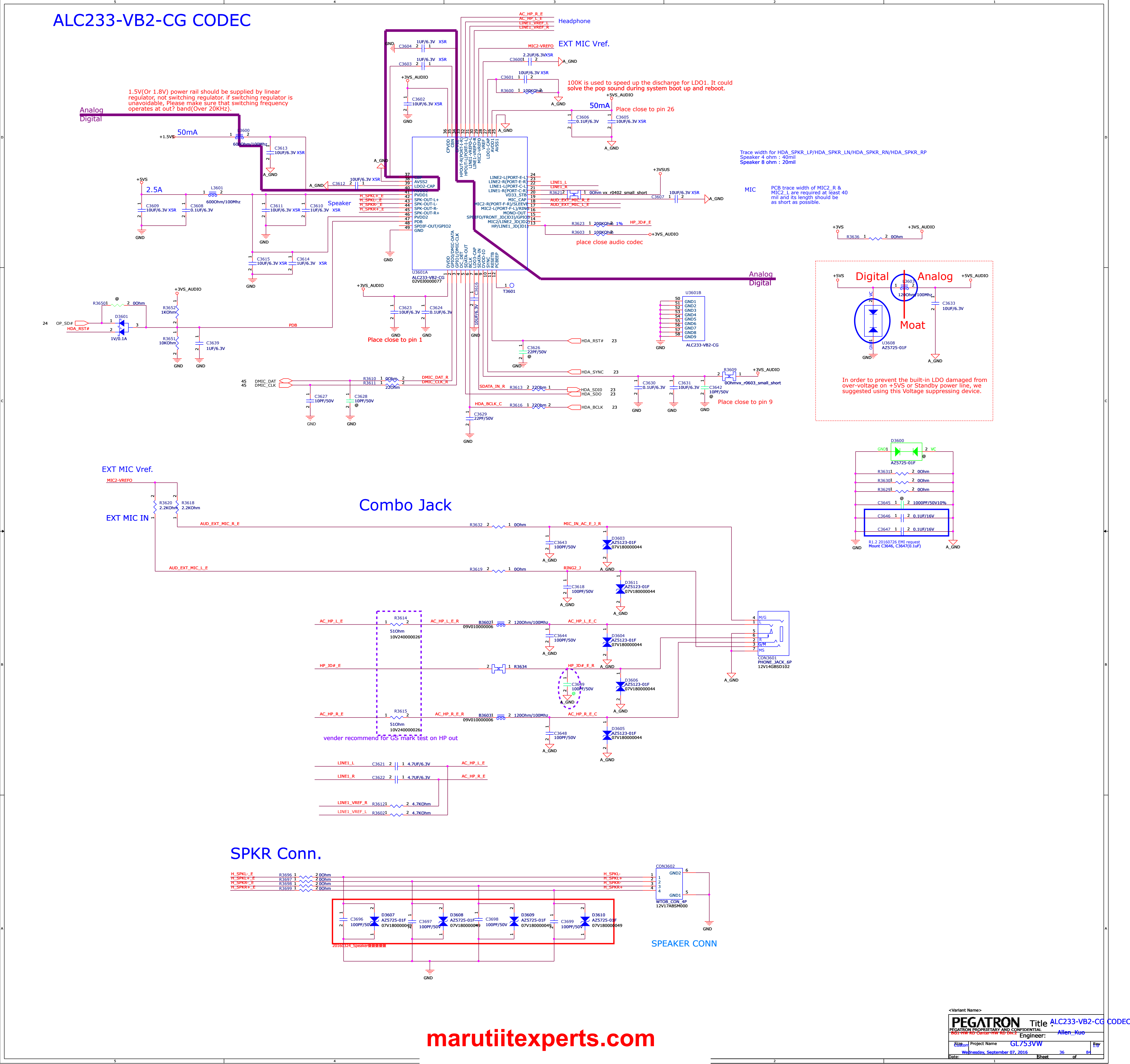
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Transformer/RJ45

BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
B	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 34 of 101



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : AUDIO Jack

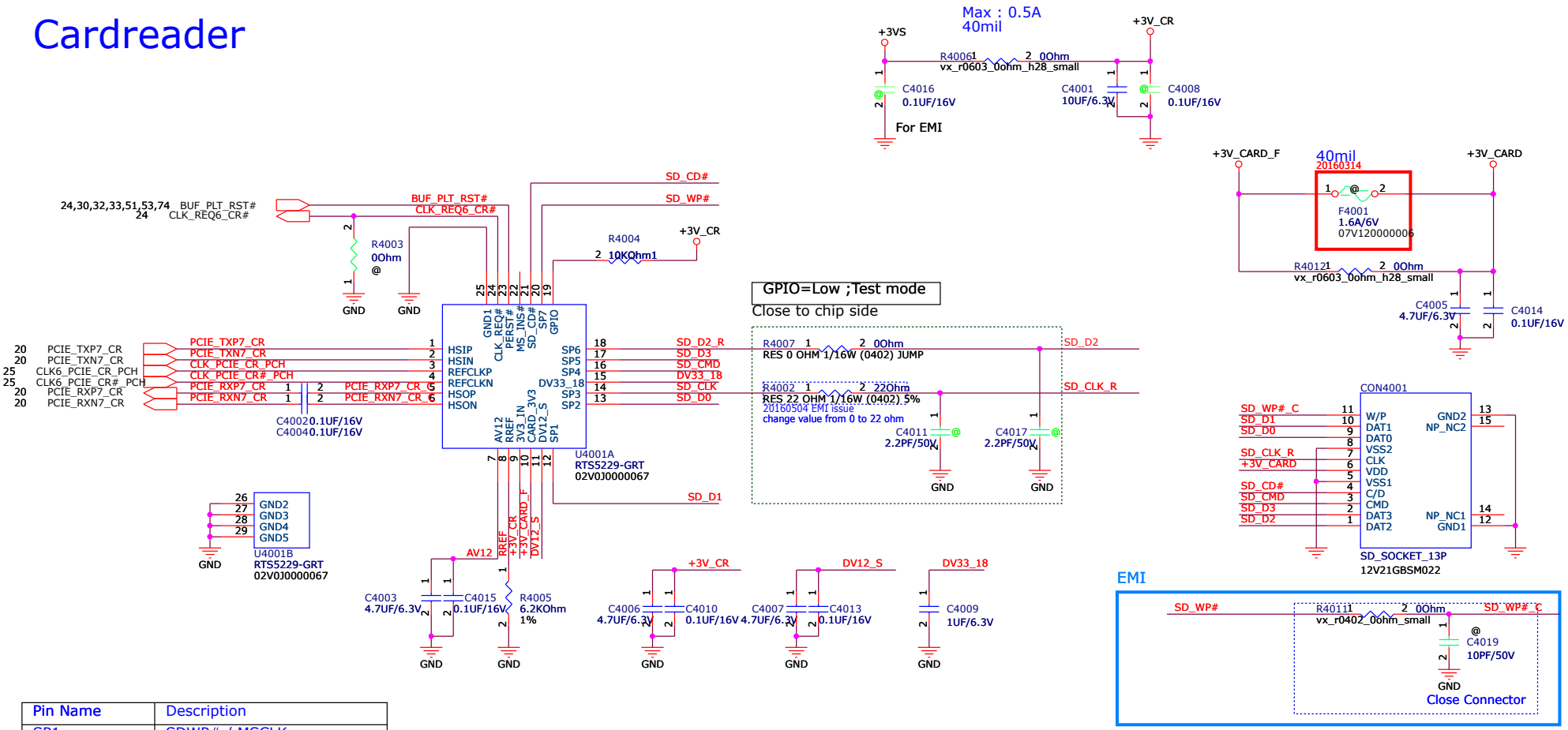
BG1-HW RD Center-HW RD Div.2

Engineer: Allen_Kuo

Size	Project Name	Rev
C	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 37 of 101

Cardreader



Pin Name	Description
SP1	SDWP# / MSCLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD_WP#	MMC_RSVD
SP3	SD_D1	
SP4	SD_D0	MMC_DAT
SP6	SD_CD#	
SP8	SD_CLK	MMC_CLK
SP10	SD_CMD	MMC_CMD
SP12	SD_D3	
SP13	SD_D2	

PEGATRON Title : RTS5138-GR

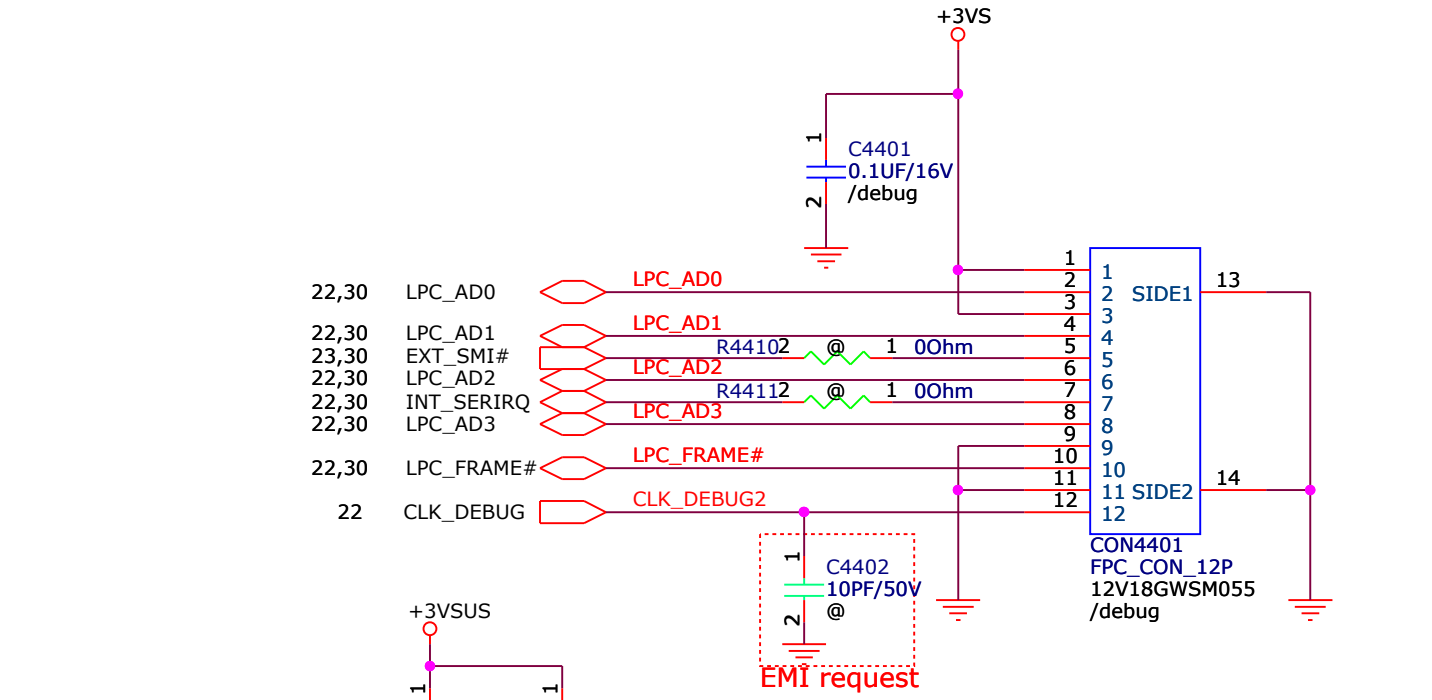
PEGATRON PROPRIETARY AND CONFIDENTIAL

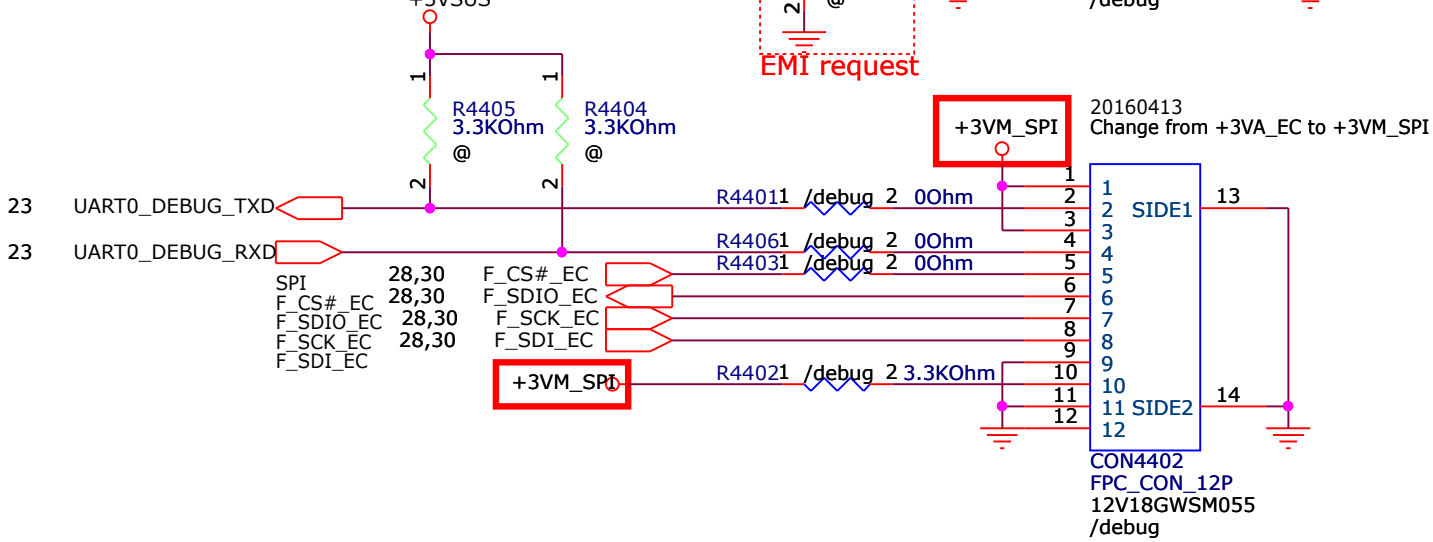
BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
B	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 40 of 101

+3VS +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,45,46,48,49,50,51,53,56,57,85,87,91,92,97





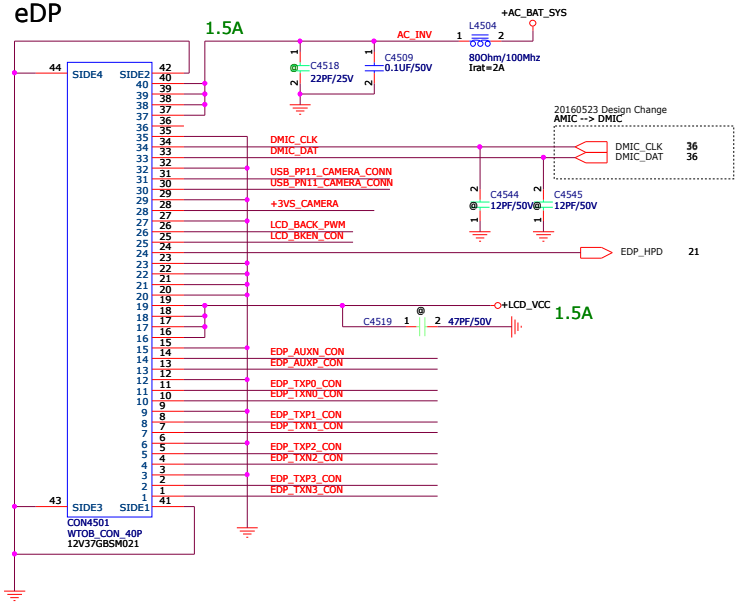
+3VM_SPI
20160413
Change from +3VA_EC to +3VM_SPI

<Variant Name>

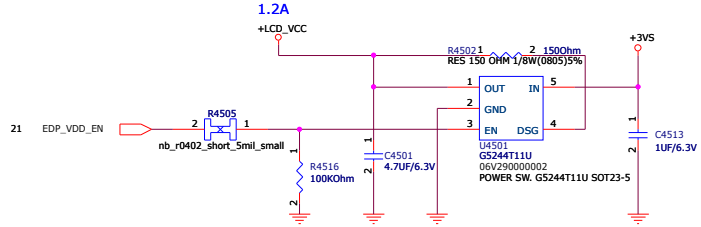
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div.2

Title: DEBUG CON
Engineer: Allen_Kuo
Size: A
Project Name: GL753VW
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet: 44 of 108

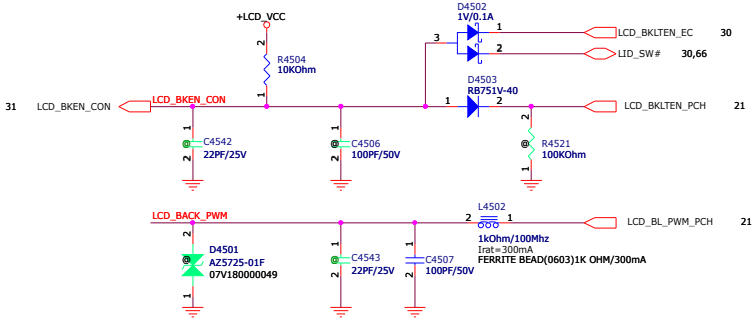
eDP

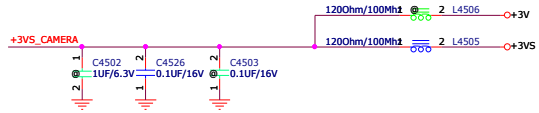


LCD VDDEN / +LED_VCC



Controll Signal



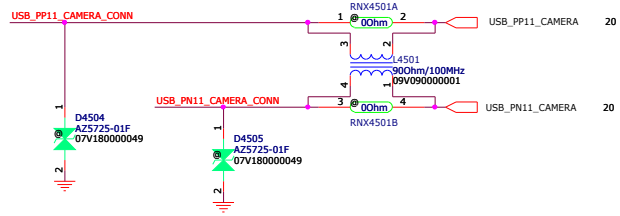


+3VS +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,46,48,49,50,51,53,56,57,85,87,91,92,97

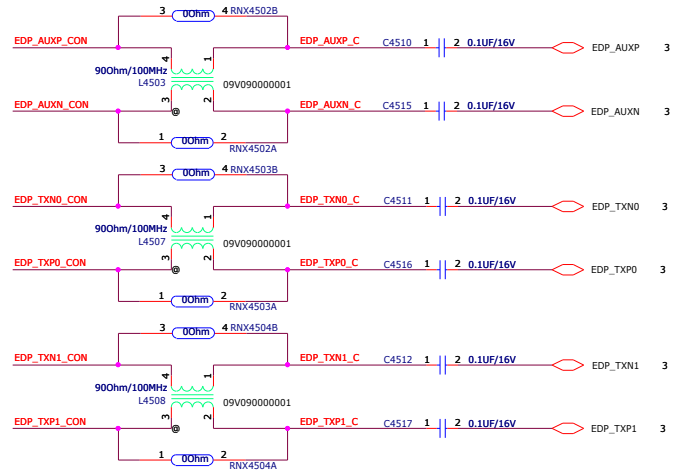
+5VS +5VS 31,36,46,48,50,51,56,57,80,87,89,91,97

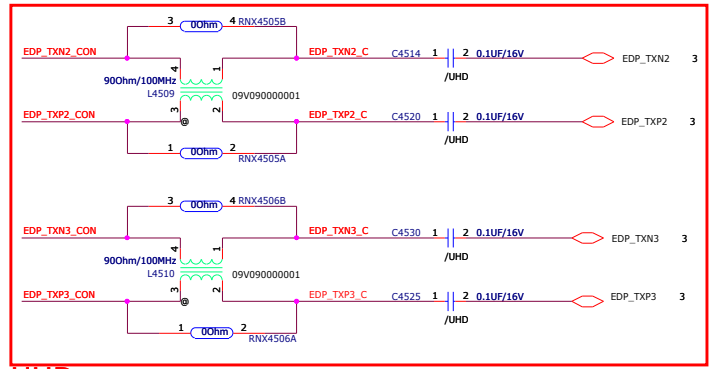
+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,87,88,89,94,97

Camera



546884_SKL_PDG_H_rev2_0 p631
The path from the processor should be AC coupled using 75~200 nF capacitor

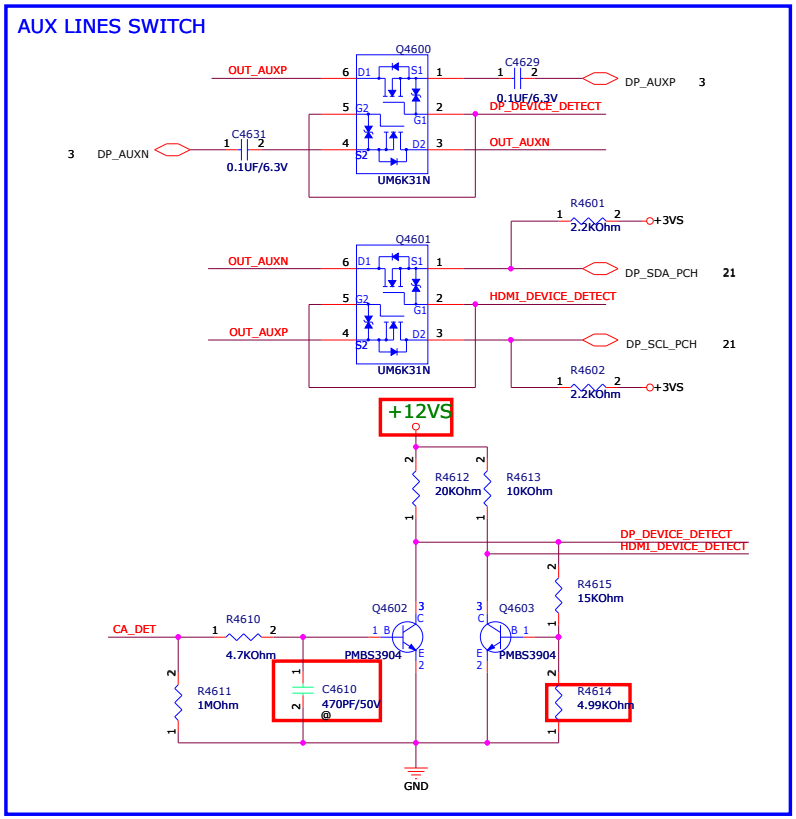


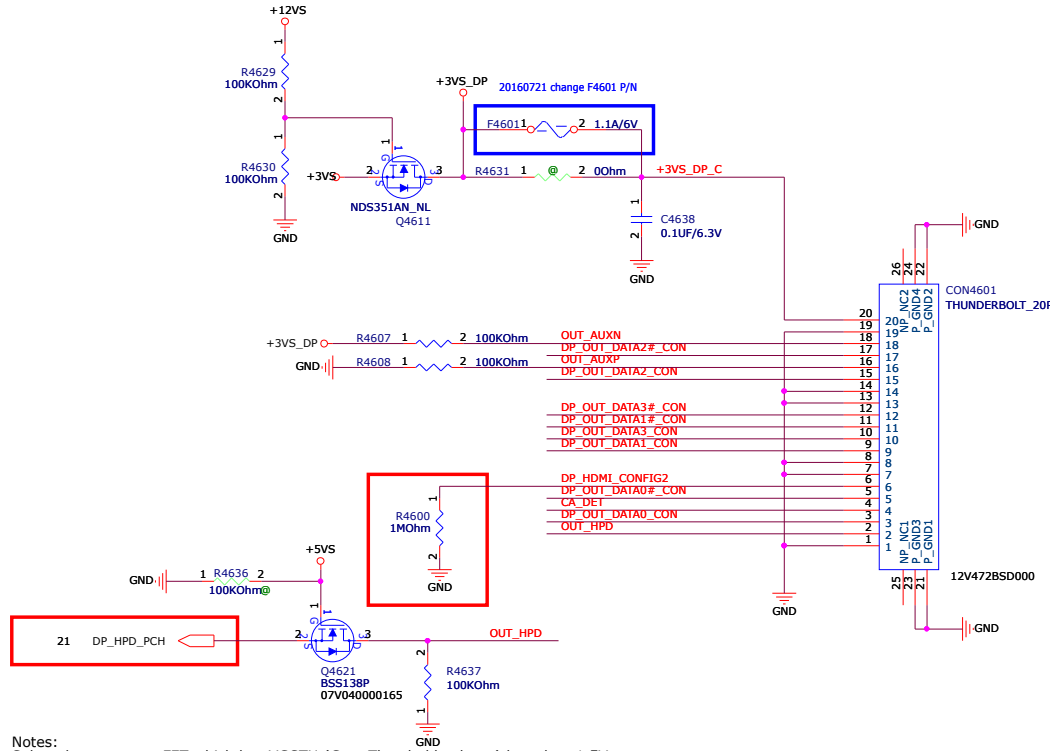


UHD

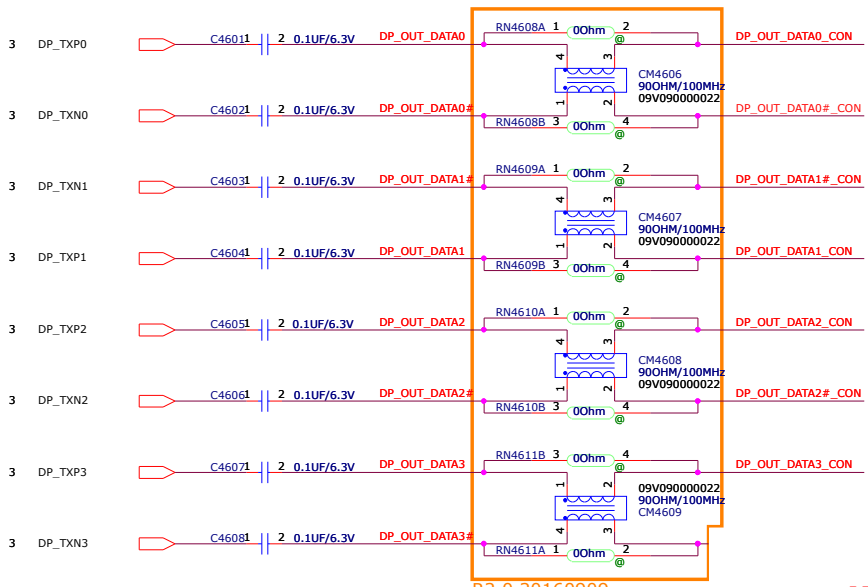
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
PEGATRON DT-MB RESTRICTED SECRET

Title : EDP/DMIC/TS/LGF
Engineer: Allen_Kuo
Size: C
Project Name: CL55VW
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet 45 of 103

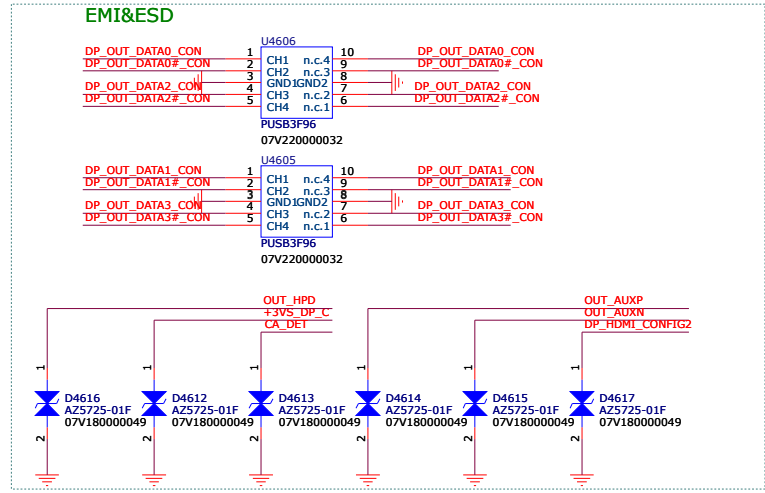




Notes:
Select the pass-gate FET which has VGSTH (Gate Threshold voltage) less than 1.5V.
The 5V supply must turn off when CPU power is turned off.

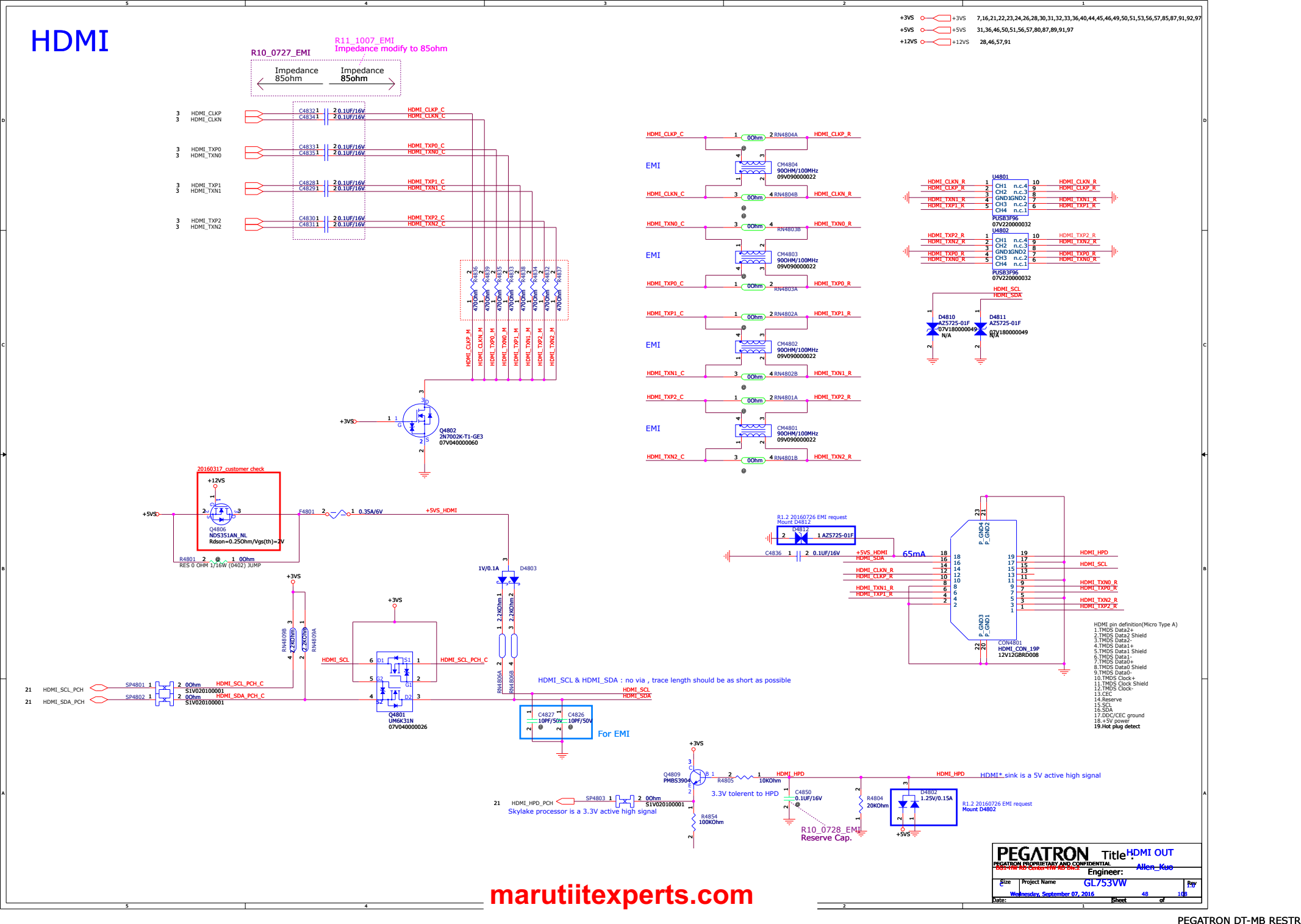


R2.0 20160909
Change Choke for EA



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: DP Multiplexer
Engineer: Allen_Kuo
Size: Custom
Project Name: GL755VW
Rev: 1.0
Date: Friday, September 09, 2016
Sheet: 46 of 103

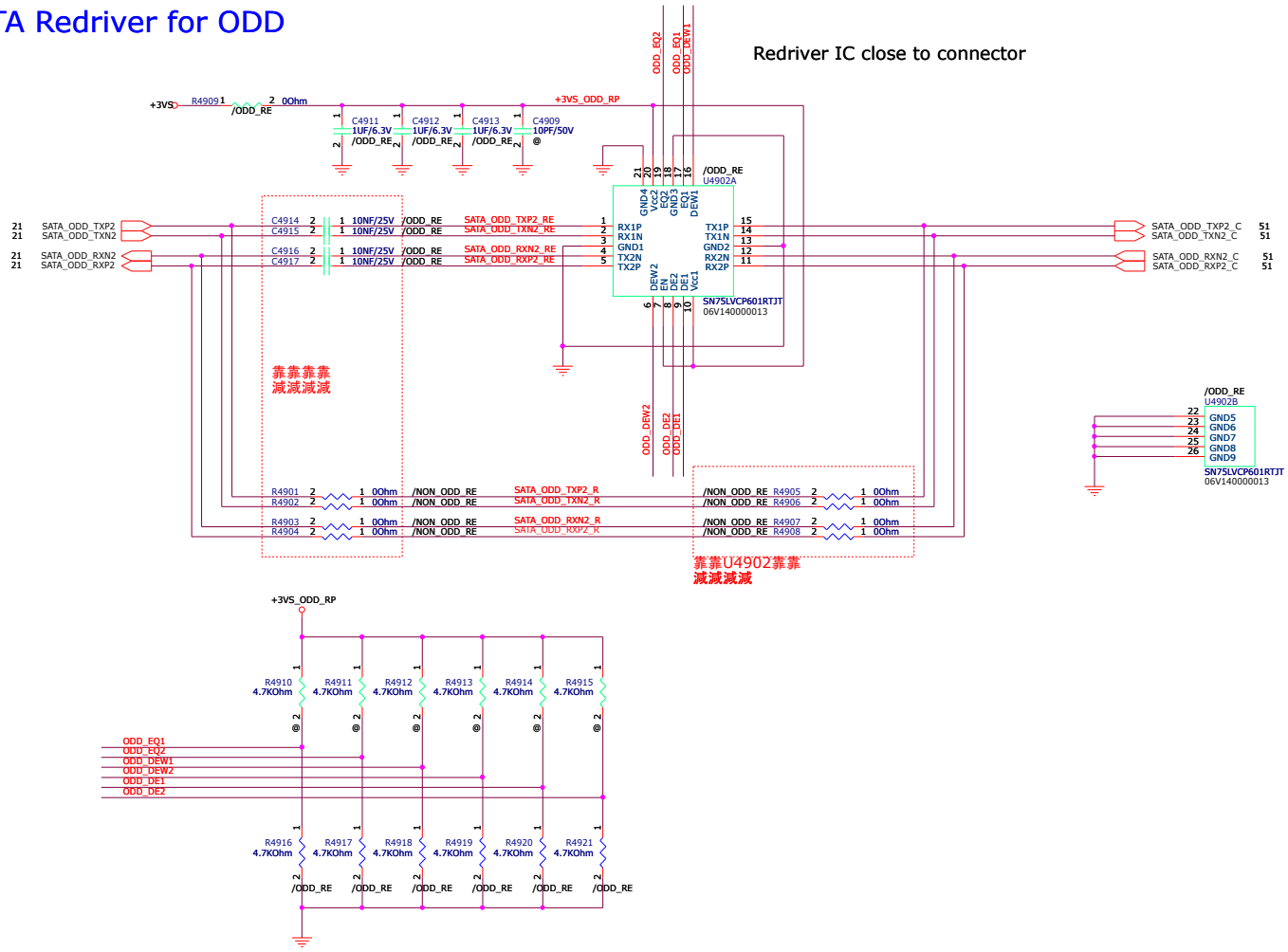
HDMI



+3VS +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,48,50,51,53,56,57,85,87,91,92,97

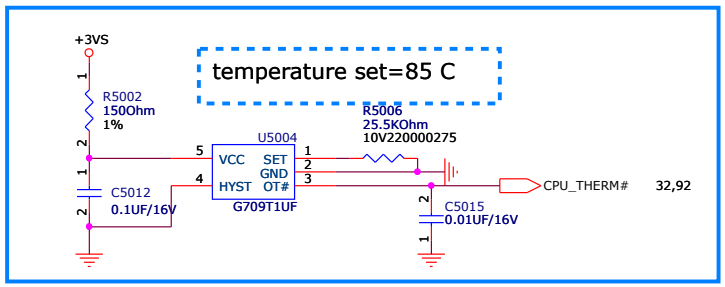
SATA Redriver for ODD

Redriver IC close to connector

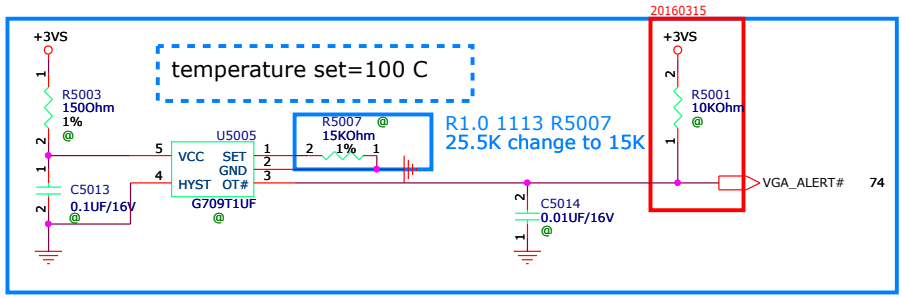


PEGATRON Title : SATA Redriver
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Engineer: Shiro_Lin
Size C | Project Name MONTBLANC | Rev 2.0
Date: Wednesday, September 07, 2016 Sheet 49 of 104

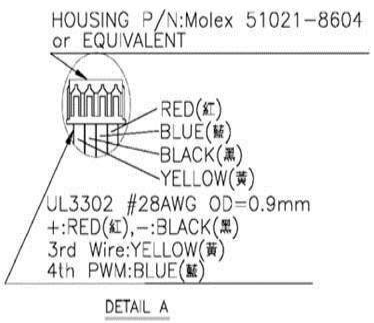
CPU Thermal Sensor

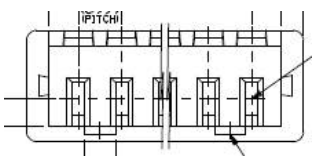


GPU Thermal Sensor

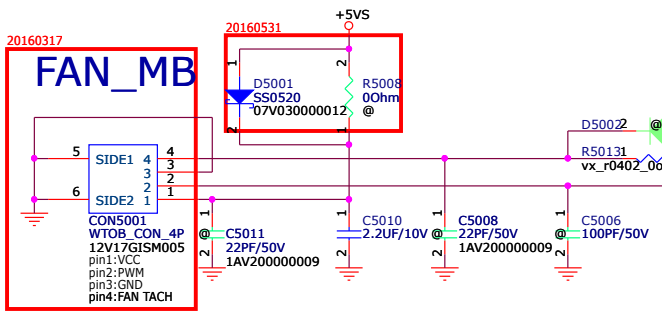


FAN_Module



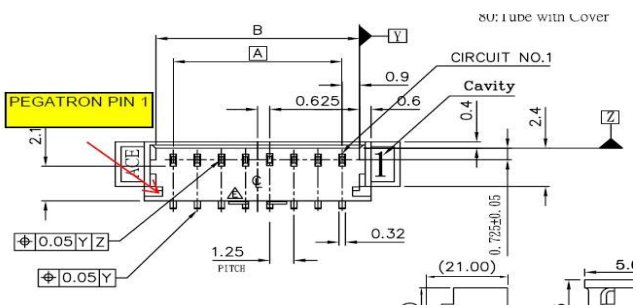


FAN_MB



EC(PU@+3VS,10Kohm

EC(PU@+3VS,4.7Kohm



teknisi-indonesia

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div.2

Title: FAN/THERMAL

Engineer: Allen_Kuo

Size	Project Name	Rev
B	GL753VW	1.0

Monday, September 12, 2016 Sheet 50 of 108

NGFF socket M PCIEx4 SSD1

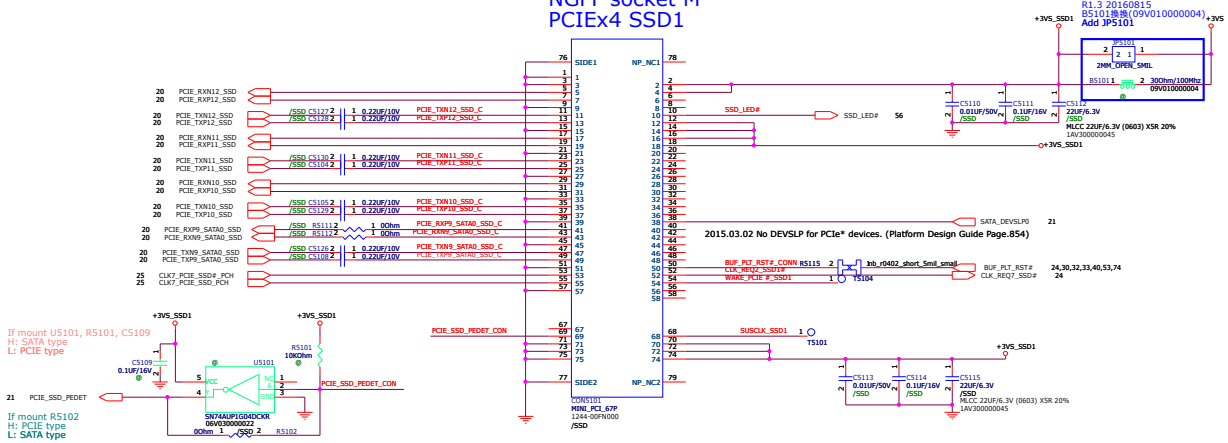


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

SATA HDD

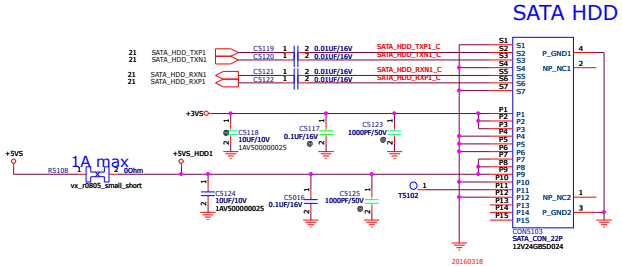
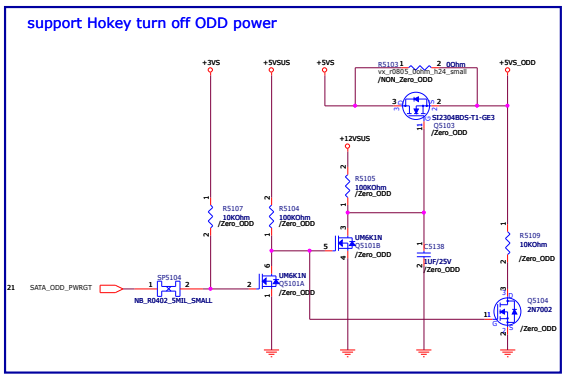


Table 5 – Standard SATA connector (3.5 inch & 2.5 inch HDD)

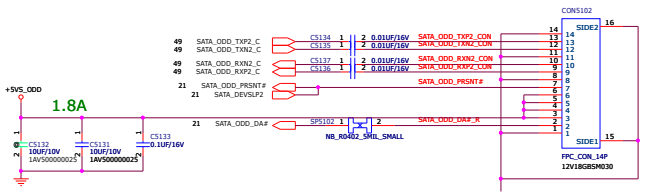
	Name	Type	Description	Cable Usage [a c]	Backplane Usage [b]
			Signal Segment Key		
Signal Segment	S1	GND	Ground	1st Mate	2nd Mate
	S2	A+	Differential Signal Pair A	2nd Mate	3rd Mate
	S3	A-		2nd Mate	3rd Mate
	S4	GND	Ground	1st Mate	2nd Mate
	S5	B-	Differential Signal Pair B	2nd Mate	3rd Mate
	S6	B+		2nd Mate	3rd Mate
	S7	GND	Ground	1st Mate	2nd Mate
			Signal Segment "L"		
			Central Connector Gap [e]		
			Power Segment "L"		
Power Segment	P1	Retired [d]		2nd Mate	3rd Mate
	P2	Retired [d]		2nd Mate	3rd Mate
	P3	DEVSLP [d]	Enter/Exit DevSleep	1st Mate	2nd Mate
	P4	GND	Ground	1st Mate	1st Mate
	P5	GND	Ground	1st Mate	2nd Mate
	P6	GND	Ground	1st Mate	2nd Mate
	P7	V_{3}	5 V Power, Pre-charge	1st Mate	2nd Mate
	P8	V_{3}	5 V Power	2nd Mate	3rd Mate
	P9	V_{3}	5 V Power	2nd Mate	3rd Mate
	P10	GND	Ground	1st Mate	2nd Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup/ Direct Head Unload / Vendor Specific [c]	2nd Mate	3rd Mate
	P12	GND	Ground	1st Mate	1st Mate
	P13	V_{12}	12 V Power, Pre-charge	1st Mate	2nd Mate
	P14	V_{12}	12 V Power	2nd Mate	3rd Mate
	P15	V_{12}	12 V Power	2nd Mate	3rd Mate
			Power Segment Key		

[a] For specific optional usage of pin P11 (see 6.13).
[b] Although the mate order is shown, hot plugging is not supported if using the cable connector receptacle.
[c] All mate sequences assume zero angular offset between connectors.
[d] The signal segment and power segment may be separate.
[e] Previous versions of this specification assigned 3.3 V to pins P1, P2 and P3. In addition, device plug pins P1, P2 and P3 were required to be tuxed together.
[f] It is recommended to have P1 and P2 connected together for the purpose of legacy functionality. Pin P3 should be a no connect if DEVSLP is not implemented.

support Hokey turn off ODD power



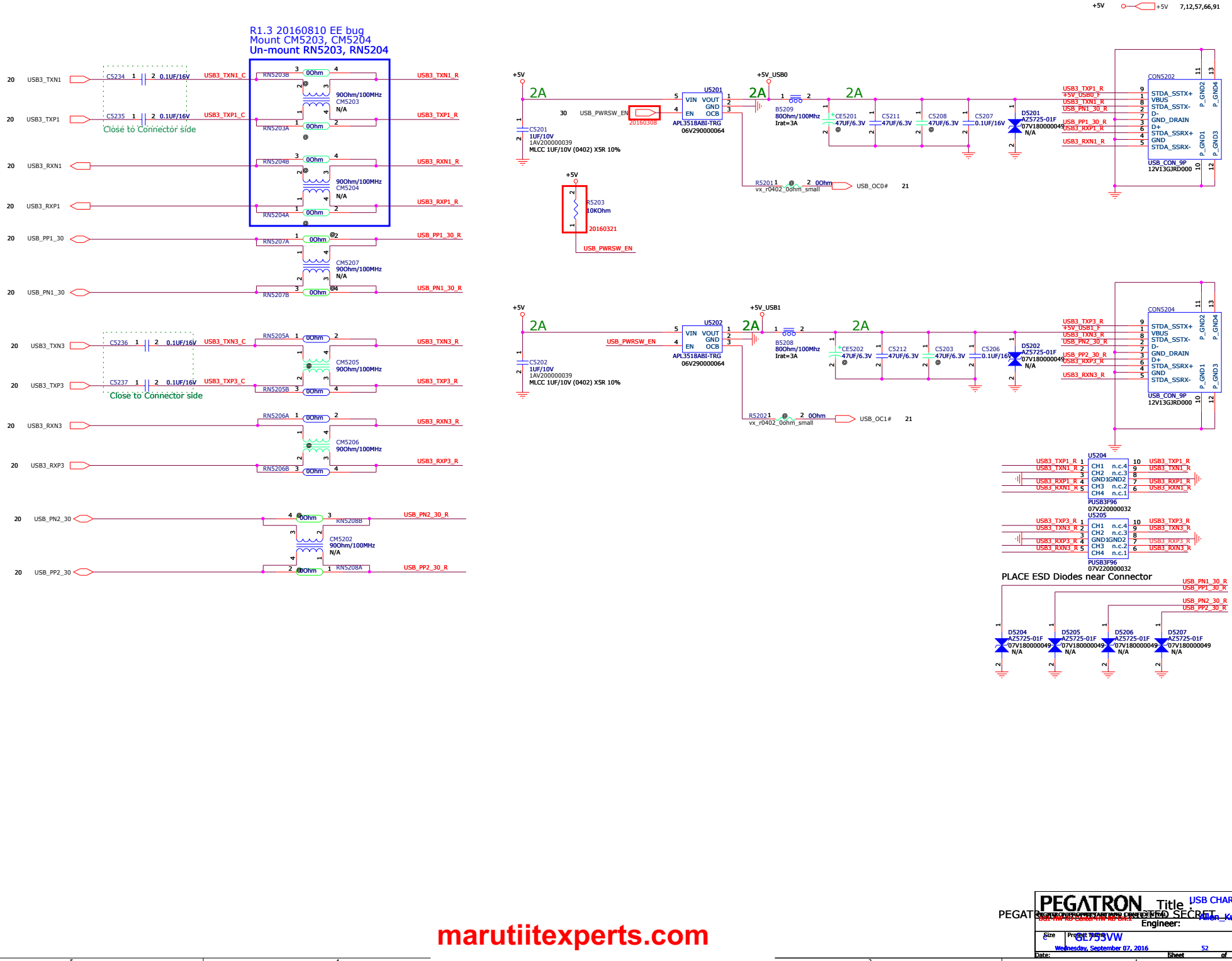
SATA ODD



<Variant Name>

PEGATRON Title: SATA/ODD/SSD
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Allen_Kuo
Size: C Project Name: GL753VW Rev
Date: Wednesday, September 07, 2016 Sheet 51 of 103

52.USB3.0


R1.3 20160810 EE bug
Mount CM5203, CM5204
Un-mount RN5203, RN5204
Close to Connector side
Close to Connector side
PLACE ESD Diodes near Connector
USB_PWRSW_EN
USB_OC0#
USB_OC1#
PUSB3F96
07V220000032
marutiitexperts.com
PEGATRON
Title
USB CHARGE IC
Engineer:
Allen_Kuo
Project Name:
CL755VW
Wednesday, September 07, 2016
52
108

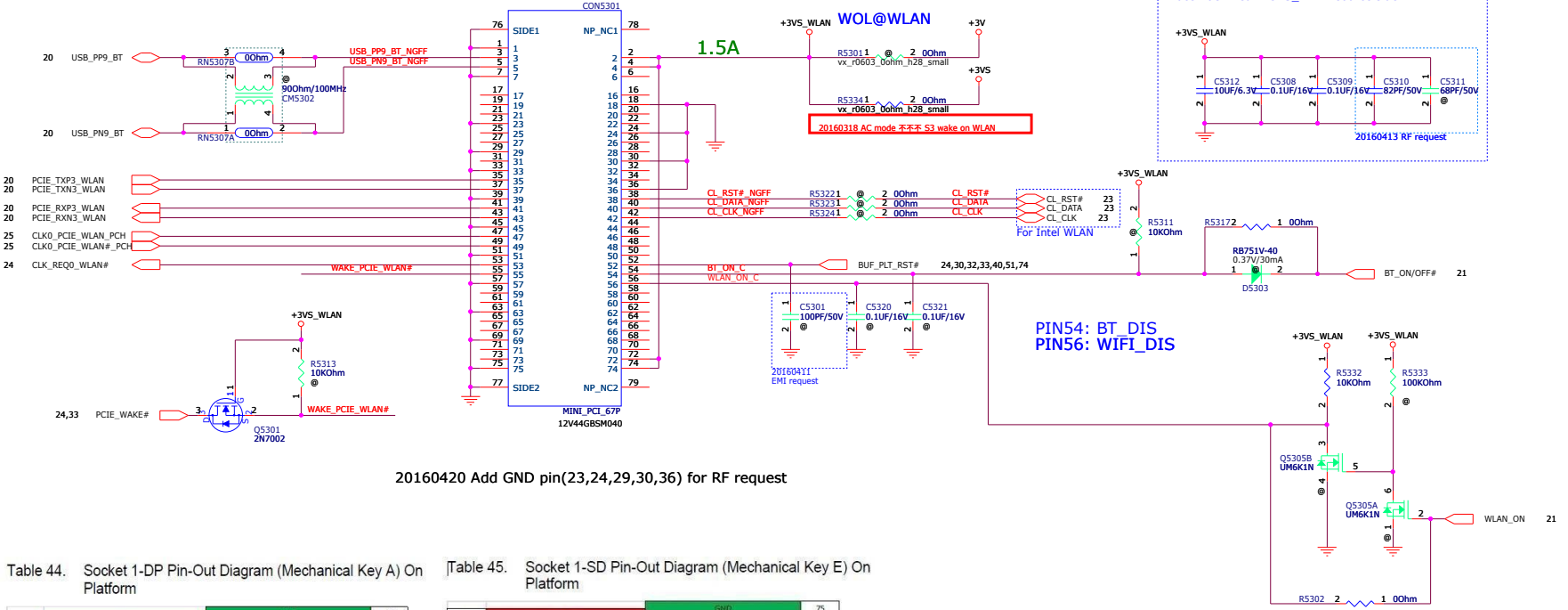
NGFF 2230 Key A_slot A(WIFI)

+3VS +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,48,49,50,51,56,57,85,87,91,92,97

+3V +3V 24,45,57,66,68,91

WLAN+BT

WLAN +3VS bypass capactor:
Place 0.1UF near pin 2,24,52,39 41(CON5301).
Place 10UF near +3VS_WLAN source side.



20160420 Add GND pin(23,24,29,30,36) for RF request

Table 44. Socket 1-DP Pin-Out Diagram (Mechanical Key A) On Platform

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (O)(0/3.3V)	PERn1	67
64	RESERVED	PERp1	65
62	ALERT# (I)(0/3.3V)	GND	63
60	I2C_CLK (O)(0/3.3V)	PETn1	61
58	I2C_DATA (IO)(0/3.3V)	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	GND	PETn0	37
34	DP_ML0p	PETp0	35
32	DP_ML0n	GND	33
30	GND	DP_HPD (I/O)(0/3.3V)	31
28	DP_ML1p	GND	29
26	DP_ML1n	DP_ML2p	27
24	GND	DP_ML2n	25
22	DP_AUXp	GND	23
20	DP_AUXn	DP_ML3p	21
18	GND	DP_ML3n	19
16	LED2# (I)(OD)	MLDIR Sense (I)	17
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
6	LED1# (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) On Platform

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/3.3V)	GND	63
60	I2C_CLK (O)(0/3.3V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/3.3V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
22	UART RXD (I)(0/1.8V)	SDIO RESET# (O)(0/1.8V)	23
20	UART WAKE# (I)(0/3.3V)	SDIO WAKE# (I)(0/1.8V)	21
18	GND	SDIO DATA3(I/O)(0/1.8V)	19
16	LED2# (I)(OD)	SDIO DATA2(I/O)(0/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA1(I/O)(0/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
10	PCM_SYNC/I2S WS (O/I)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
8	PCM_CLK/I2S SCK (O/I)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED1# (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: NGFF_WLAN
Engineer: Allen_Kuo
Size: C | Project Name: GL753VW | Rev: 1.0
Date: Wednesday, September 07, 2016 | Sheet 53 of 108

PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON

Title : LEFT USB3 CONN.

Engineer: Allen_Kuo

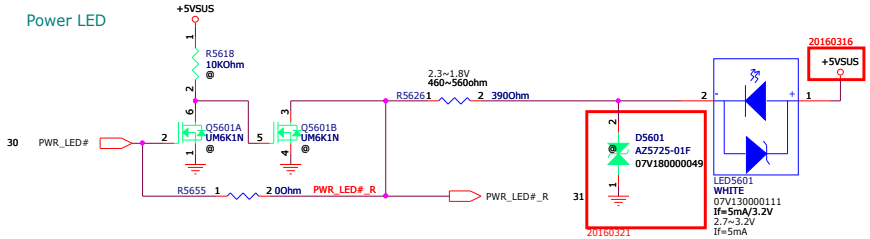
Size	Project Name	Rev
C	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 55 of 108

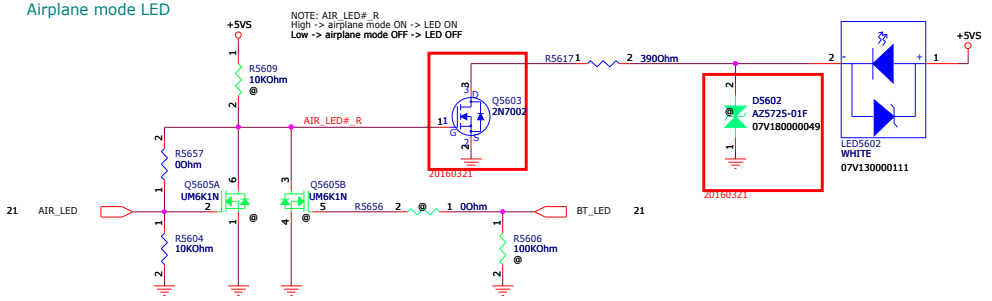
+5VSUS +5VSUS 26,31,51,81

+5VS +5VS 31,36,46,48,50,51,57,80,87,89,91,97

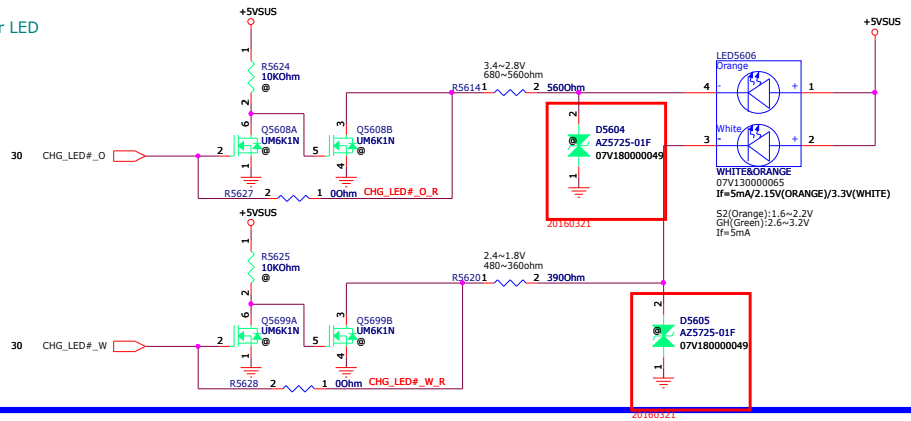
Power LED



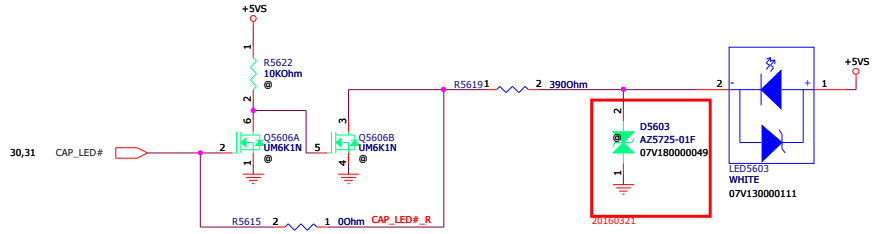
Airplane mode LED



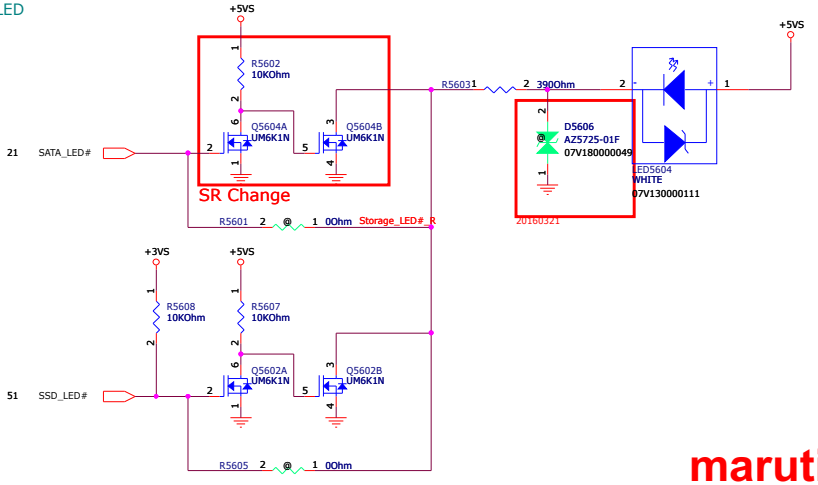
Charger LED



Caps Lock LED

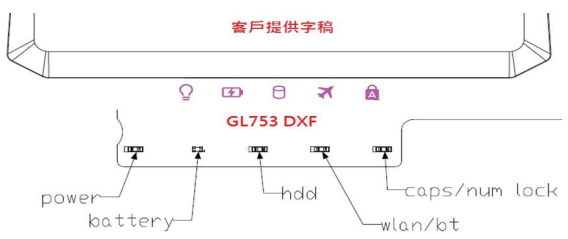


HDD LED



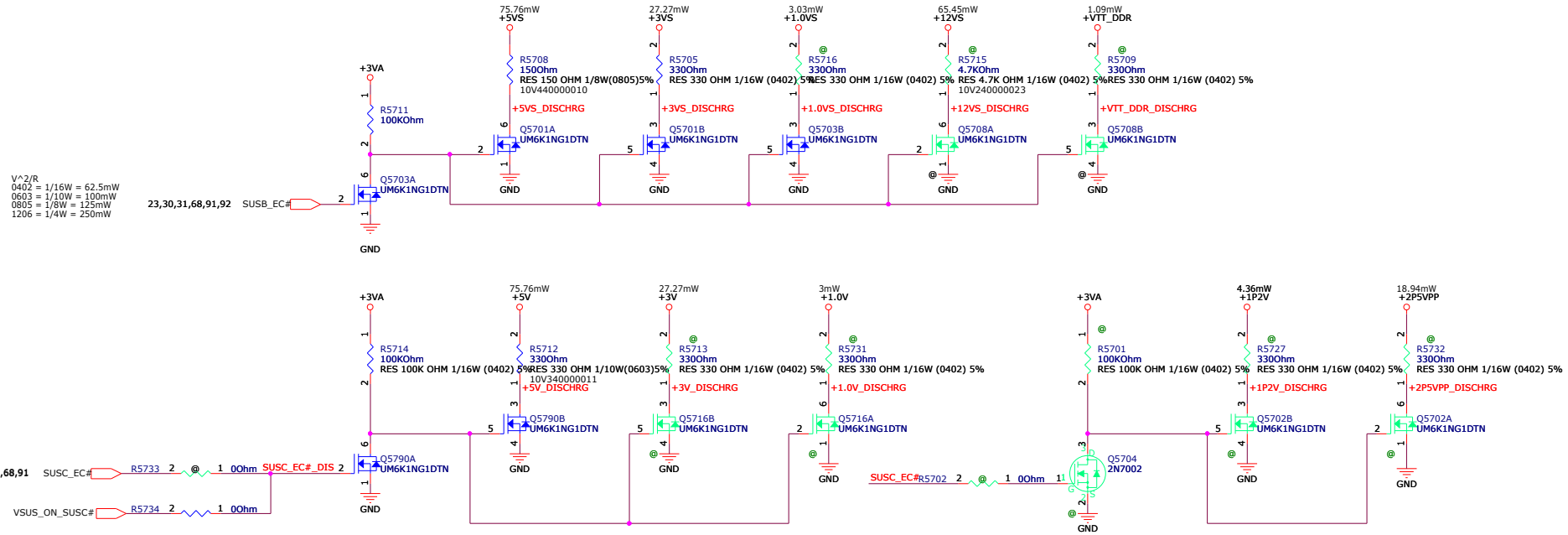
MB LED Placement
Left-->Right

PWR LED	Charger LED	HDD LED	RF LED	Caps Lock LED
LED5601	LED5606	LED5604	LED5602	LED5603



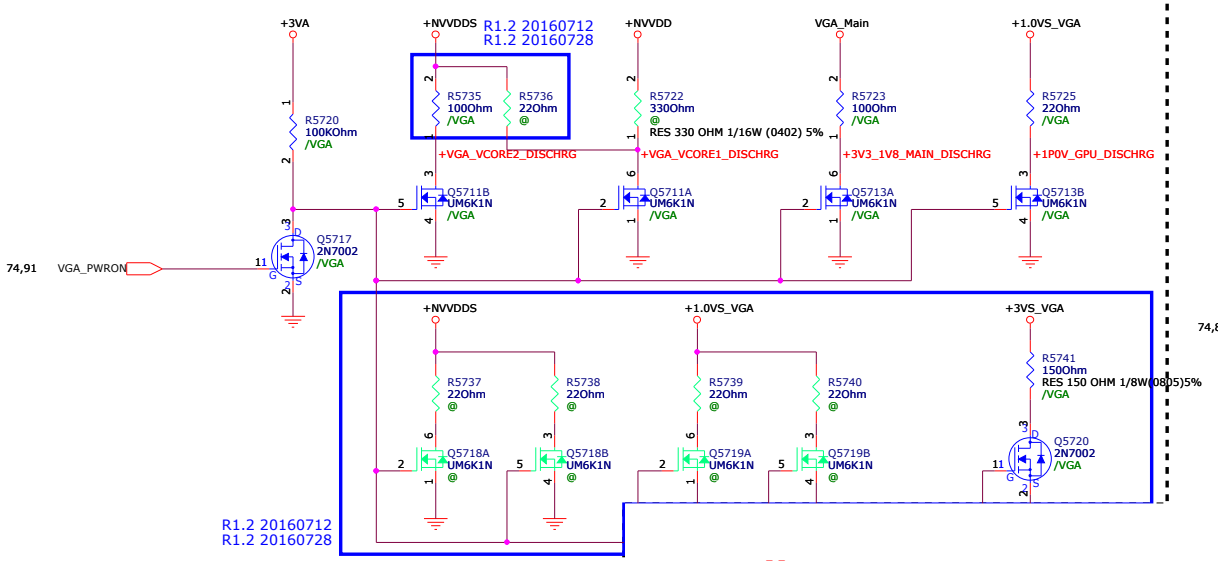
<Variant Name>

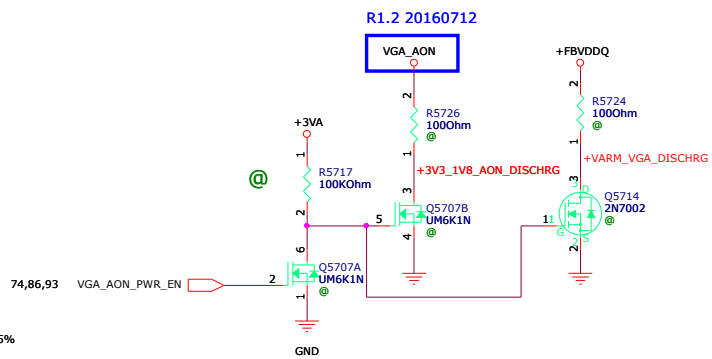
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PWR BOARD CON
Engineer: Allen_Kuo
GL753VW
Size C | Project Name | Rev 1.0
Date: Wednesday, September 07, 2016 | Sheet 56 of 108



all MOS mount for GPU Optimus function

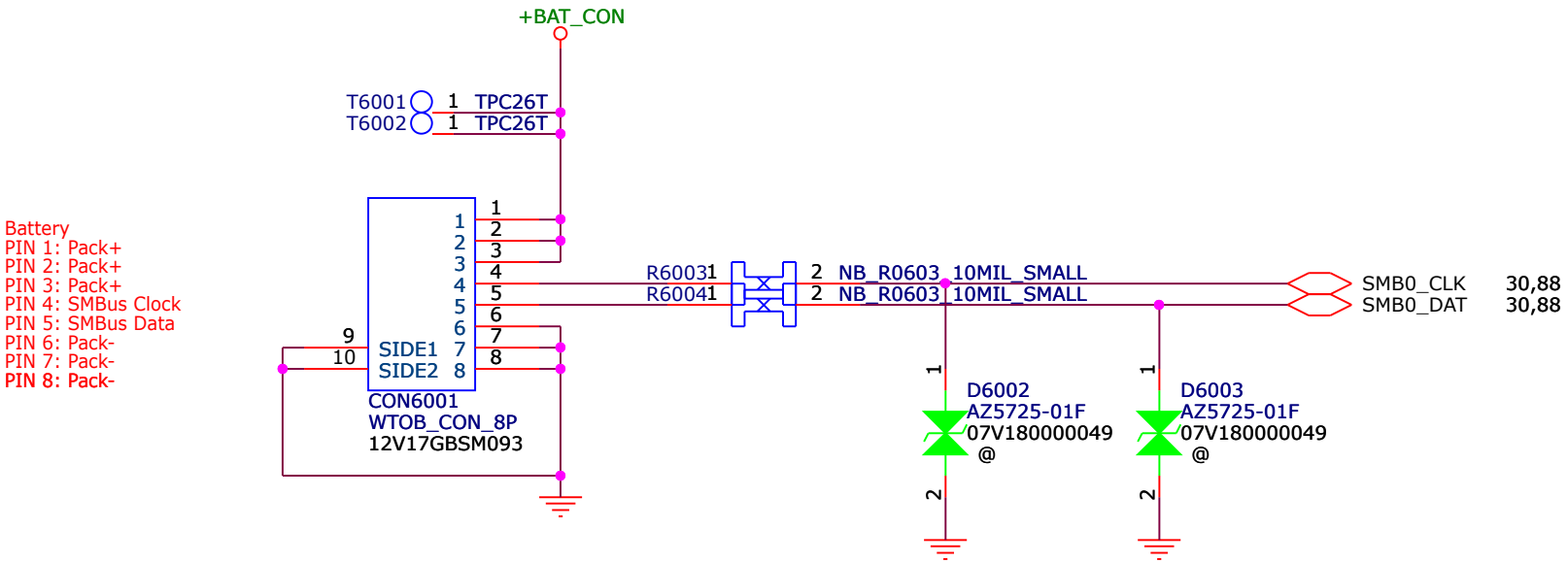
GC6 2.0 pwr rail discharge





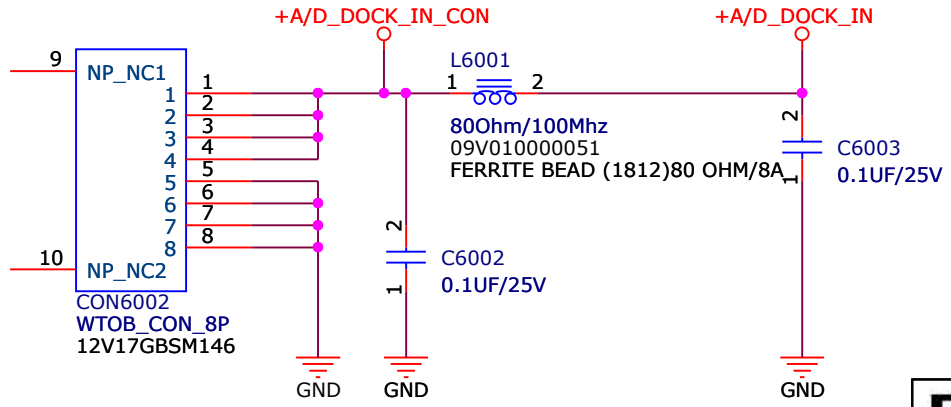
60.BATT CON/AC IN

BATTERY CONNECTOR



AC IN CONNECTOR

Adaptor
120W



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RD Center-HW RD Div.2

Title : BATT CON/AC IN

Engineer: Allen_Kuo

Size	Project Name	Rev
A	GL753VW	1.0

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Date: Sheet of

PEGATRON

Title : BOARD ID

PEGATRON PROPRIETARY AND CONFIDENTIAL

~~DO NOT COPY~~

Engineer: Allen_Kuo

Size	Project Name	Rev
C	GE75 3VW	1.0

Date: Wednesday, September 07, 2016 Sheet 61 of 108

<Variant Name>

PEGATRON Title : TPM

BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
A4	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 62 of 108

65.NUT,Screw hole,Tooling hole

CPU NUT

H6501 CT236B140D110 1308-00Q0000
H6502 CT236B140D110 1308-00Q0000
H6503 CT236B140D110 1308-00Q0000
H6504 CT236B140D110 1308-00Q0000

GND

GPU NUT

H6505 CT236B140D110 1308-00Q0000
H6506 CT236B140D110 1308-00Q0000
H6507 CT236B140D110 1308-00Q0000
H6508 CT236B140D110 1308-00Q0000

GND

PCH NUT

H6510 CT217B144D114 1308-009K000
H6511 CT217B144D114 1308-009K000

GND

Hall Sensor Brd NUT

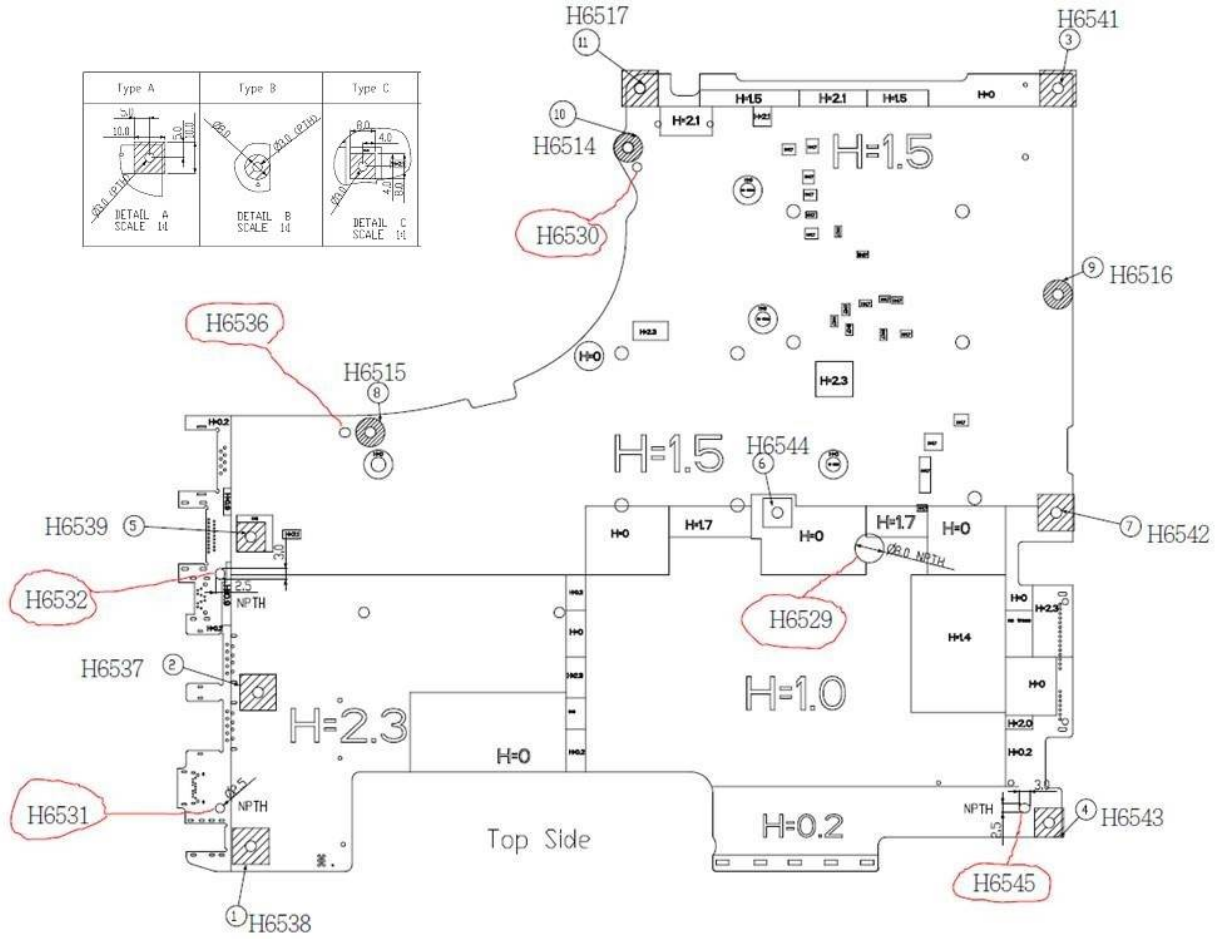
H6533 CT197B67D47 1308-00PJ000

GND

SSD NUT

H6534 CT276B195D165 1308-00FC000 ME update SSD nut 0422

GND



TOP: phi 8 drill 3 BOT: phi 8 drill 3

1 H6514 C315D118 S1V1YGCC4Z00
1 H6515 C315D118 S1V1YGCC4Z00
1 H6516 C315D118 S1V1YGCC4Z00

GND

TOP: Square 8 drill 3 BOT: phi 8 drill 3

1 H6544 ST315CB315D118 T-SH00004213
1 H6543 ST315CB315D118 T-SH00004213
1 H6539 ST315CB315D118 T-SH00004213

GND

TOP: Square 10 drill 3 BOT: phi 8 drill 3

1 H6537 ST394CB315D118 T-SH00004264
1 H6517 ST394CB315D118 T-SH00004264
1 H6541 ST394CB315D118 T-SH00004264
1 H6538 ST394CB315D118 T-SH00004264
1 H6546 ST394CB315D118 T-SH00004264

GND

TOP: Square 10 drill 3 BOT: Square 10 drill 3

H6542 1 S394D118

GND

NPTH_2.5phi

1 H6530 C98D98N temp_5262_gh15
1 H6531 C98D98N temp_5262_gh15
1 H6532 C98D98N temp_5262_gh15

NPTH_8phi

1 H6529 C315D315N T-SH00002489

NPTH_2.5 x 3 phi

1 H6545 O118X98DO118X98N T-SH00000687

NPTH_2.5 x 2.9 phi

1 H6536 O98X114DO98X114N T-SH00004210

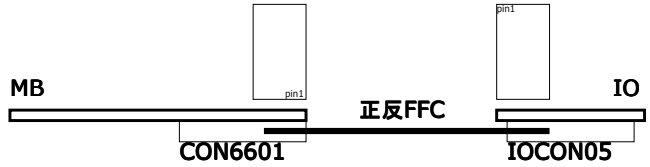
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1 HW RD Center HW RD Div.2

Title: Screw hole
Engineer: Allen_Kuo

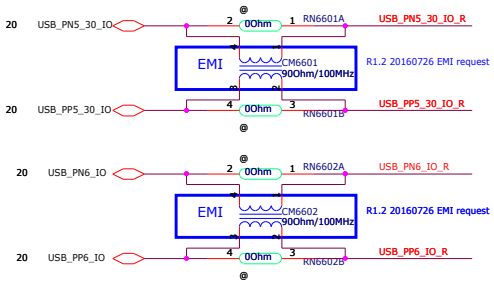
Size: Custom | Project Name: GL753VW | Rev: 1.0
Date: Wednesday, September 07, 2016 | Sheet: 65 of 108

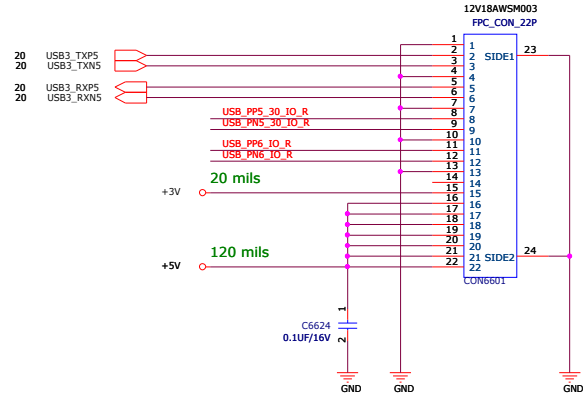
IO BD CONN. (MB SIDE)



+3V +3V 24,45,53,57,68,91
+3VA +3VA 25,30,31,57,74,81,88,91,93
+5V +5V 7,12,52,57,91

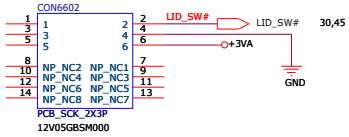
Need check pin define

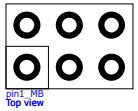




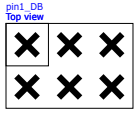
MB Side USB Re-driver (move to IO_BD side)

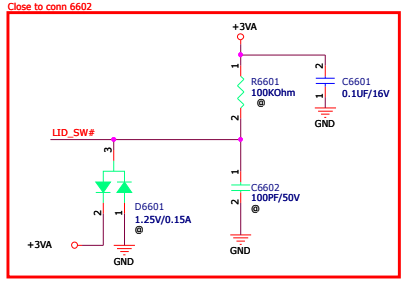
Hall sensor Conn. (MB SIDE)





CON6602 LDJ01
pin2:LID_SW# pin1:LID_SW#_H
pin4:GND pin3:GND_H
pin6:+3VA pin5:+3VA_H





+3VSUS +3VSUS 7,21,23,24,26,28,30,31,33,36,44,74,81,92,97

EC processing time (3ms~33ms)

24,30 PM_SUSB# R6801 1 2 SUSB_EC# 23,30,31,57,91,92

24,30 PM_SUSC# R6802 1 2 SUSC_EC# 30,31,57,91

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms
Delay By EC(2ms)+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R68091 nb_r0402_short_5mil_small

U6802 Vcc=2~5.5 @

+3VSUS +3V R6842 10KOhm

R6808 @100KOhm 10V240000005 GND

C6804 0.1UF/25V @ GND

R68101 nb_r0402_short_5mil_small DELAY_ALL_SYSTEM_PWRGD 7,24

R68051 nb_r0402_short_5mil_small CPU_VRON 80

For shut down Sequence
Tplt17 < 1us

PM_SUSB# D6802 1V/0.1A

EC p.30 DE_ALL_SYS_PGD_EC

PM_SUSB# p.24

DELAY_ALL_SYSTEM_PWRGD p.68

15 p.68 CPU_VRON

for PM_PWROK p.24

for VCCST_PWRGD p.7

IMVP8 VR
CORE
VCCSA
VCCGT
VCCGTX

For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK drop after PM_SUSB# before CPU_VRON to add this solution

30 SYS_PWROK_EC R68431 nb_r0402_short_5mil_small SYS_PWROK_EC_G2

U6803 Vcc=2~5.5 @

+3VSUS +3V R6841 100KOhm 10V240000005

R6806 @100KOhm 10V240000005 GND

R68041 nb_r0402_short_5mil_small SYS_PWROK 24

PM_SUSB# D6811 1V/0.1A

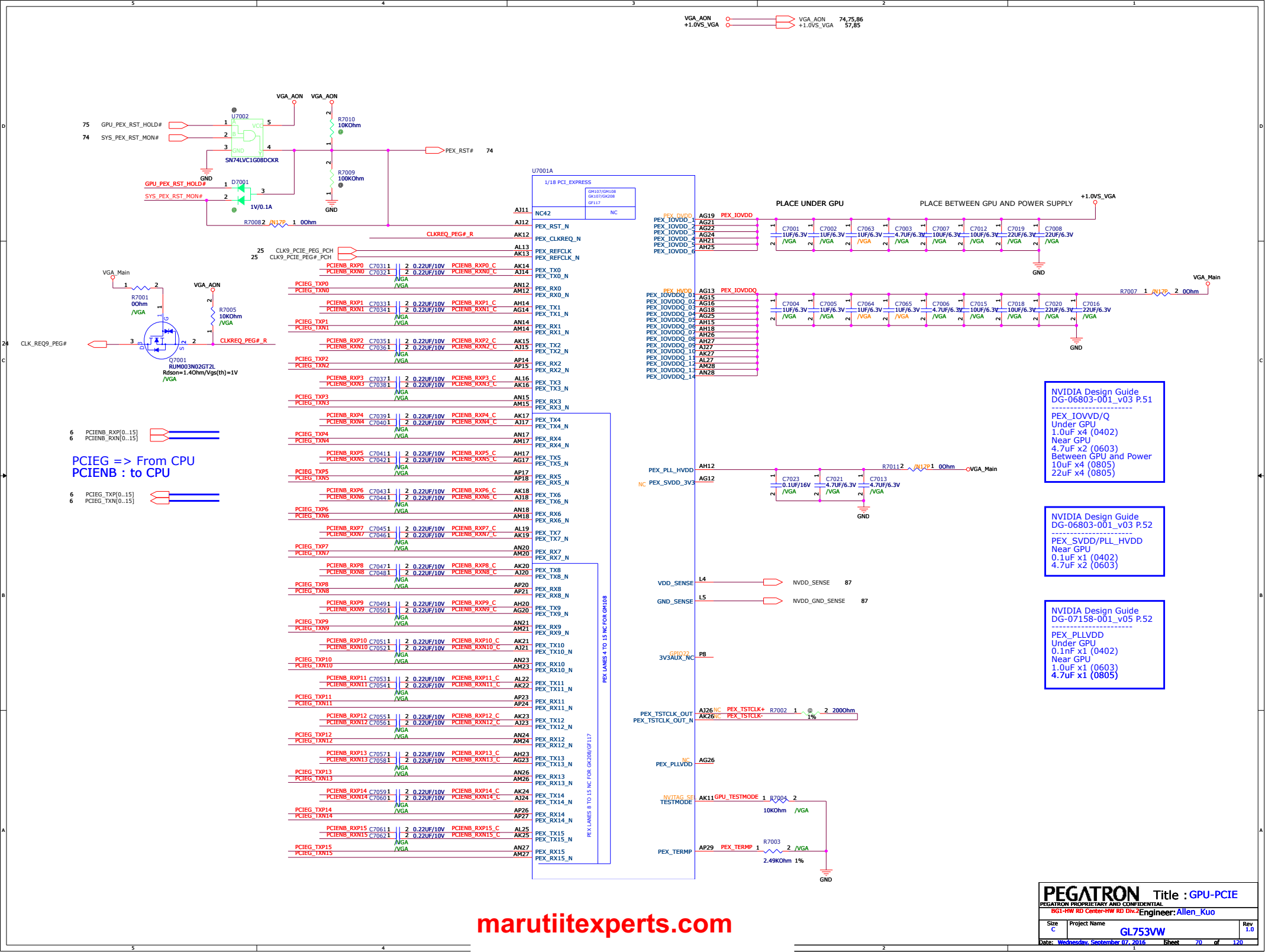
EC 20 SYS_PWROK_EC p.30

PM_SUSB# p.24

21 SYS_PWROK p.68 PCH

delay by EC, delay circuit no longer needed

PEGATRON Title : POWER Sequence
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo
Size B | Project Name GL753VW | Rev 1.0
Date: Wednesday, September 07, 2016 Sheet 68 of 101



NVIDIA Design Guide
DG-06803-001_v03 P.51

PEX_IOVVD/Q
Under GPU
1.0uF x4 (0402)
Near GPU
4.7uF x2 (0603)
Between GPU and Power
10uF x4 (0805)
22uF x4 (0805)

NVIDIA Design Guide
DG-06803-001_v03 P.52

PEX_SVDD/PLL_HVDD
Near GPU
0.1uF x1 (0402)
4.7uF x2 (0603)

NVIDIA Design Guide
DG-07158-001_v05 P.52

PEX_PLLVDD
Under GPU
0.1nF x1 (0402)
Near GPU
1.0uF x1 (0603)
4.7uF x1 (0805)

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-PCIE

BGI-HW RD Center-HW RD Div.2 Engineer: Allen_Kuo

Size	Project Name	Rev
C	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 70 of 120

I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		
I2C_1			
SMBUS			
	DDR Channel A(CON1601)		
	DDR Channel B(CON1701)		
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24735RGRR	0X09
SMBUS1 (EC)			
	THERMAL-SENSOR	G781P8F	0X4C
	GPU	N16P-GX	0X4B

<Variant Name>

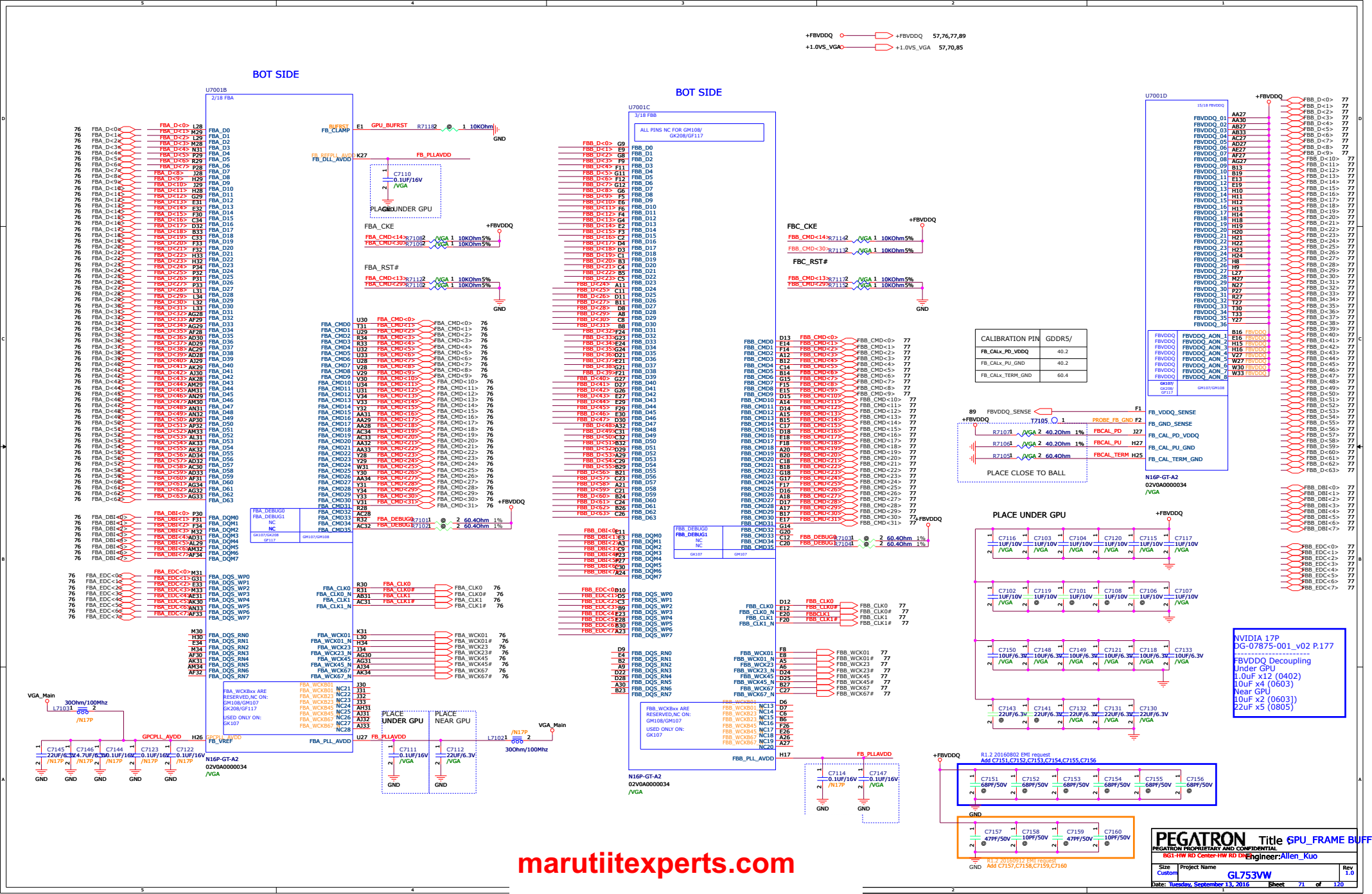
PEGATRON

Title: I2C MAP

Engineer: Allen_Kuo

Size	Project Name	Rev
A3	GL753VW	1.0

Date: Wednesday, September 07, 2016 Sheet 2 of 108


BOT SIDE
U7001B
2/18 FBA
BOT SIDE
U7001C
3/18 FBB
ALL PINS NC FOR GM108/GK208/GF117
U7001D
15/18 FBVDDQ
+FBVDDQ
+1.0VS_VGA
+FBVDDQ 57,76,77,89
+1.0VS_VGA 57,70,85
FBC_CKE
FBC_RST#
FBA_CKE
FBA_RST#
CALIBRATION PIN
GDDR5/
FB_CALx_PD_VDDQ
40.2
FB_CALx_PU_GND
40.2
FB_CALx_TERM_GND
60.4
PLACE CLOSE TO BALL
PLACE UNDER GPU
PLACE NEAR GPU
PLACE UNDER GPU
N16P-GT-A2
02V0A0000034
/VGA
N16P-GT-A2
02V0A0000034
/VGA
N16P-GT-A2
02V0A0000034
/VGA
NVIDIA 17P
DG-07875-001_v02 P.177
FBVDDQ Decoupling
Under GPU
1.0uF x12 (0402)
10uF x4 (0603)
Near GPU
10uF x2 (0603))
22uF x5 (0805)
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :GPU_FRAME BUFF
Engineer:Allen_Kuo
Project Name
GL753VW
Rev 1.0
Date: Tuesday, September 13, 2016
Sheet 71 of 120
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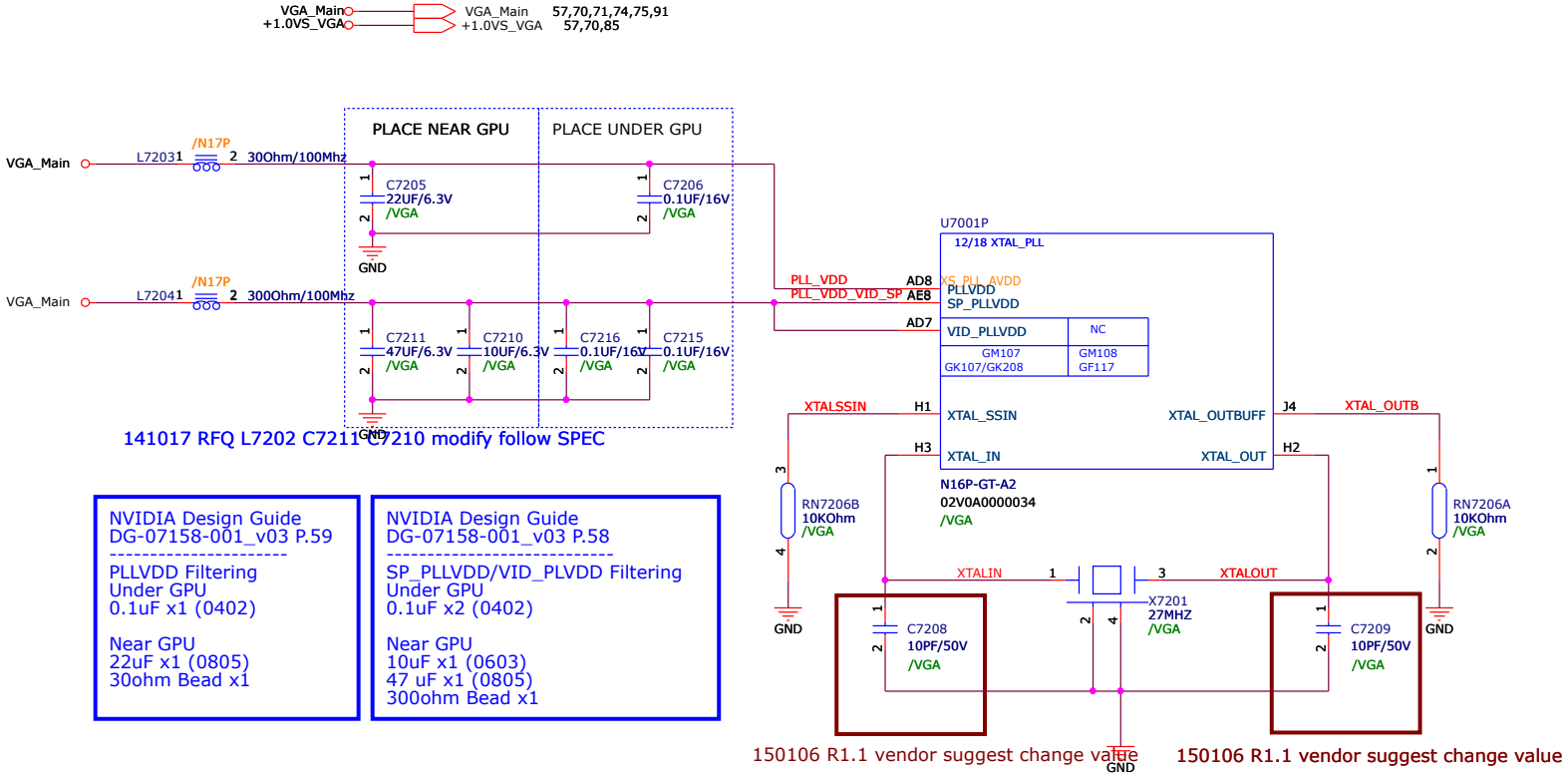


NVIDIA Design Guide
DG-07158-001_v03 P.59

PLLVDD Filtering
Under GPU
0.1uF x1 (0402)

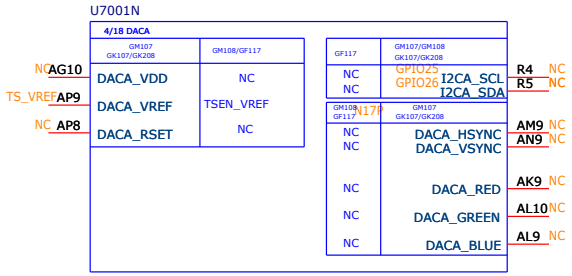
Near GPU
22uF x1 (0805)
30ohm Bead x1

NVIDIA Design Guide
DG-07158-001_v03 P.58

SP_PLLVDD/VID_PLVDD Filtering
Under GPU
0.1uF x2 (0402)

Near GPU
10uF x1 (0603)
47 uF x1 (0805)
300ohm Bead x1

CRT

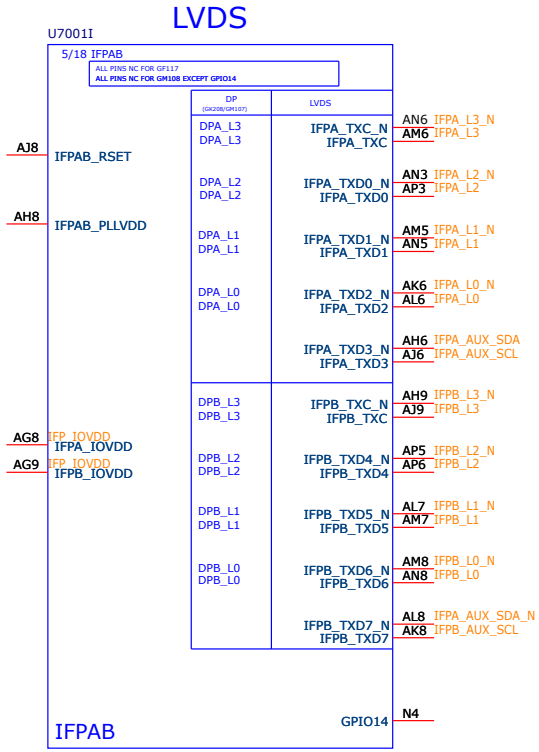


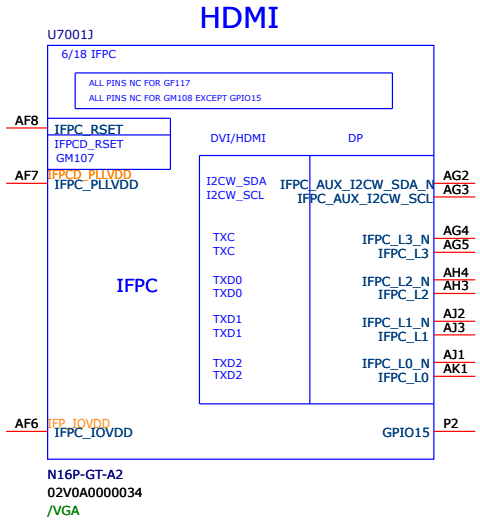
N16P-GT-A2
02V0A0000034
/VGA

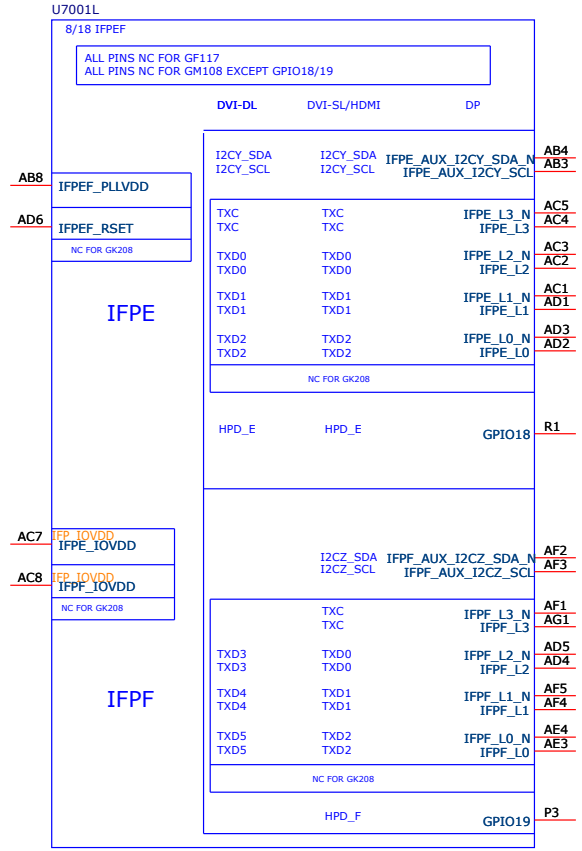
PEGATRON Title : GPU_RGB_,XTAL
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div. Engineer:Allen_Kuo

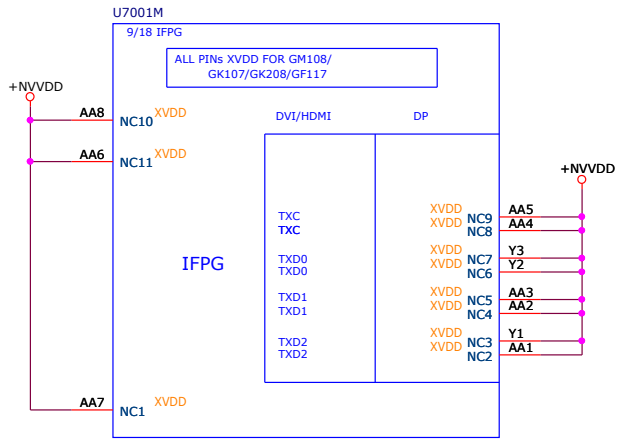
Size	Project Name	Rev
B	GL753VW	1.0

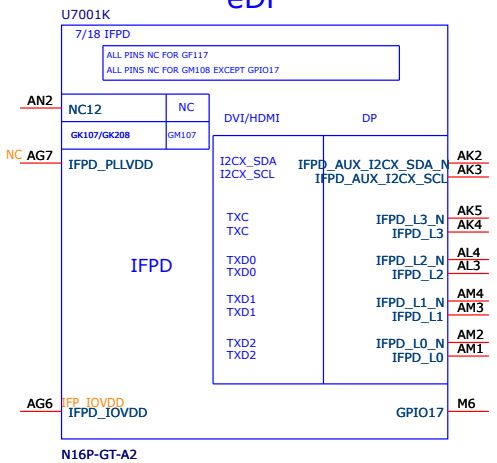
Date: Wednesday, September 07, 2016 Sheet 72 of 120











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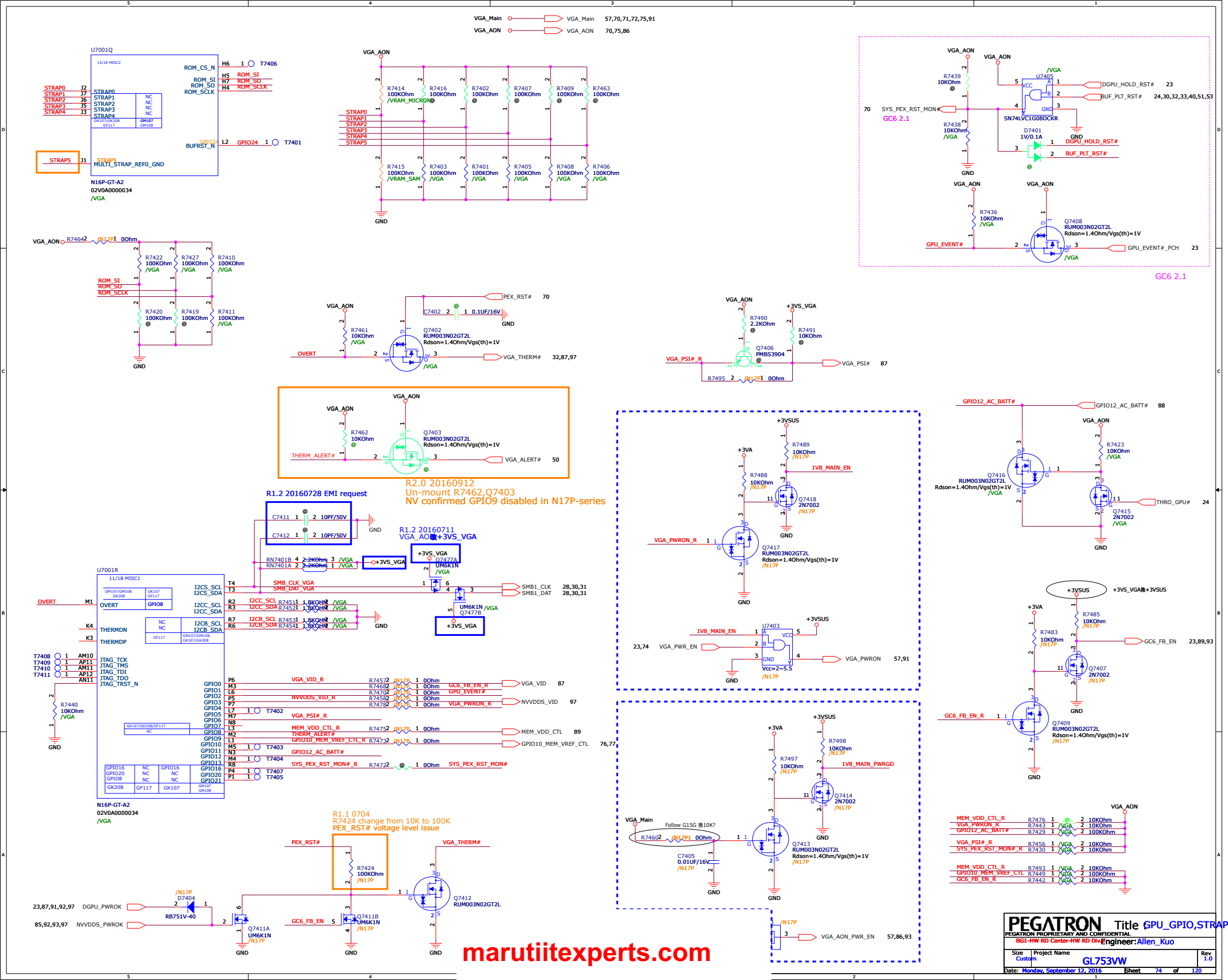
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : GPU_LVDS_HDMI
BG1-HW RD Center-HW RD Div.
Engineer: Allen_Kuo
Size: Custom
Project Name: GL753VW
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet 73 of 120


VGA_Main 57,70,71,72,75,91
VGA_AON 70,75,86
U7001Q
N16P-GT-A2
02V0A0000034
/VGA
GC6 2.1
R1.2 20160728 EMI request
R2.0 20160912
Un-mount R7462,Q7403
NV confirmed GPIO9 disabled in N17P-series
R1.2 20160711
VGA_AON +3VS_VGA
U7001R
11/18 MISC1
N16P-GT-A2
02V0A0000034
/VGA
R1.1 0704
R7424 change from 10K to 100K
PEX_RST# voltage level issue
marutiitexperts.com
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Center-HW RD Div.
Title :GPU_GPIO,STRAP
Engineer:Allen_Kuo
Size Custom
Project Name GL753VW
Rev 1.0
Date: Monday, September 12, 2016
Sheet 74 of 120

VGA_Main 57,70,71,72,74,91
VGA_AON 70,74,86
+NVVDD 57,73,87

U7001E
16/18 GND_1/2
N16P-GT-A2
02V0A0000034
/VGA

U7001F
17/18 GND_2/2
Optional CMD GNDs (2)
NC for 4-Lyr cards
N16P-GT-A2
02V0A0000034
/VGA

U7001G
14/18 NVVDD
N16P-GT-A2
02V0A0000034
/VGA

PLACE UNDER GPU

R2.0 20160912
C7568,C7569,C7511 change to 0402 package

R1.2 20160802 EMI request
Add C7587,C7588

PLACE NEAR GPU

R2.0 20160912 EMI request
Add C7589,C7590,C7591,C7592,C7593,C7594,C7595,C7505,C7506

R2.0 20160912
C7574,C7571 change to 0402 package

R1.2 20160808 Power request
Mount C7572
Mount CE7533 (1BV080000060)

NVIDIA Design Guide
DA-07679-001_v03 P.35

NVVDD Decoupling
Under GPU
4.7U x14(16) (0603)
1 U x5(9) (0402)
10U x0(3) (0603)
Near GPU
22U x5(7) (0805)
4.7U x0(6) (0603)
330U x1(2) (7343)

NVIDIA Design Guide

NVVDDS Decoupling
Under GPU
4.7U x5(5) (0603)
1 U x3(5) (0402)
Near GPU
10 U x2(2) (0805)
22 U x0(3) (0805)
330U x0(1) (7343)

U7001O
18/18 NC/VDD33
N16P-GT-A2
02V0A0000034
/VGA

PLACE UNDER GPU
PLACE NEAR GPU

NVIDIA Design Guide
DG-07158-001_v03 P.55

3V3_MAIN Decoupling
Under GPU
0.1U x2 (0402)
Near GPU
1.0U x1 (0603)
4.7U x1 (0603)

NVIDIA Design Guide
DG-07158-001_v03 P.55

3V3_AON Decoupling
Under GPU
0.1U x1 (0402)
Near GPU
1.0U x1 (0603)
4.7U x1 (0603)

GC6 2.1

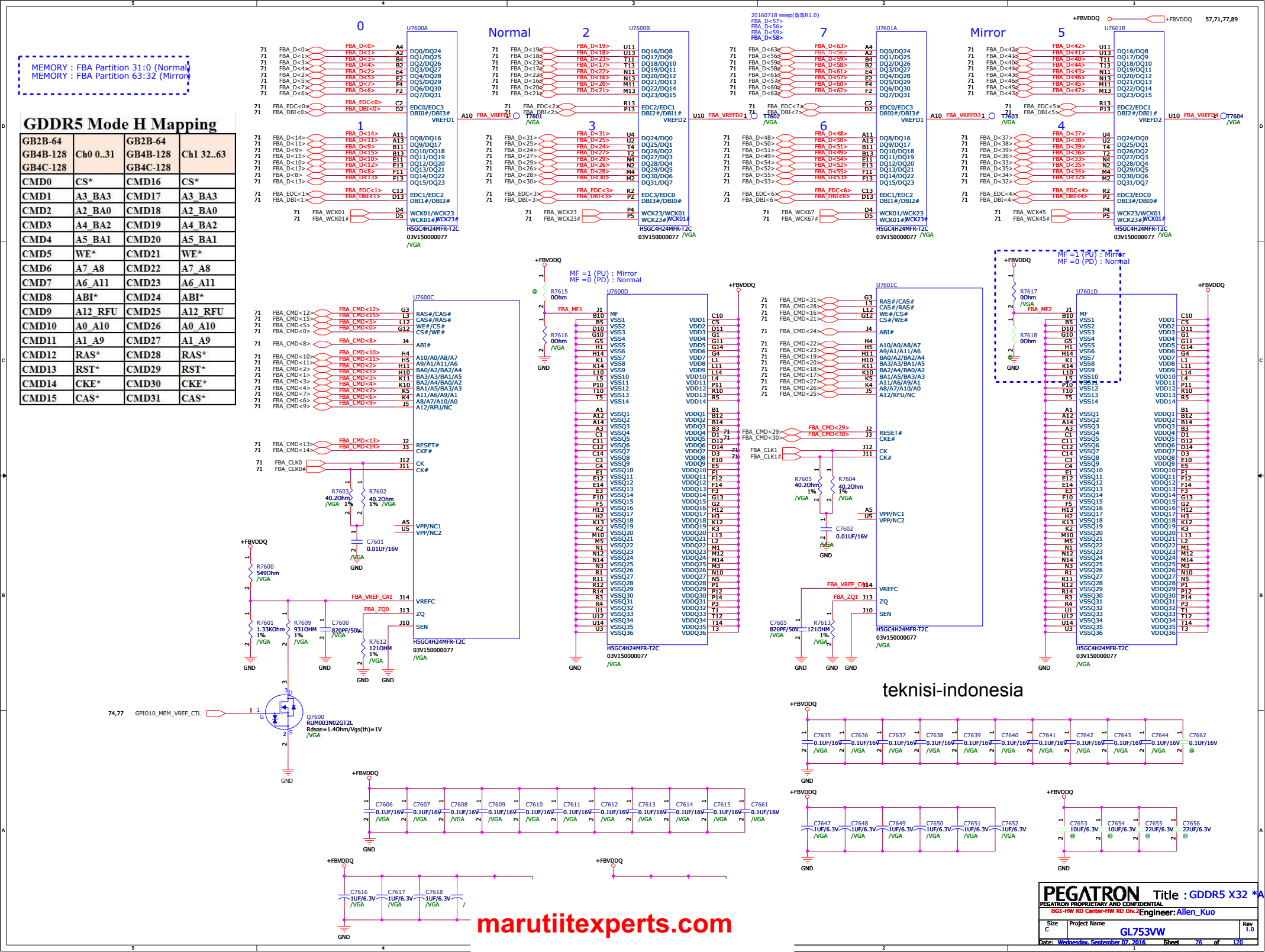
U7001H
10/18 XVDD
6P-GT-A2
V0A0000034
GA

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : GPU_Power,GND
Engineer: Allen_Kuo
BG1-HW RD Center-HW RD Div.2
Size: Custom | Project Name: GL753VW | Rev: 1.0
Date: Monday, September 12, 2016 | Sheet 75 of 120

MEMORY : FBA Partition 31:0 (Normal)
MEMORY : FBA Partition 63:32 (Mirror)

GDDR5 Mode H Mapping

GB2B-64 GB4B-128 GB4C-128	Ch0 0..31	GB2B-64 GB4B-128 GB4C-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



MEMORY : FBA Partition 31:0 (Normal)
MEMORY : FBA Partition 63:32 (Mirror)

GDDR5 Mode H Mapping

GB2B-64 GB4B-128 GB4C-128	Ch0 0..31	GB2B-64 GB4B-128 GB4C-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

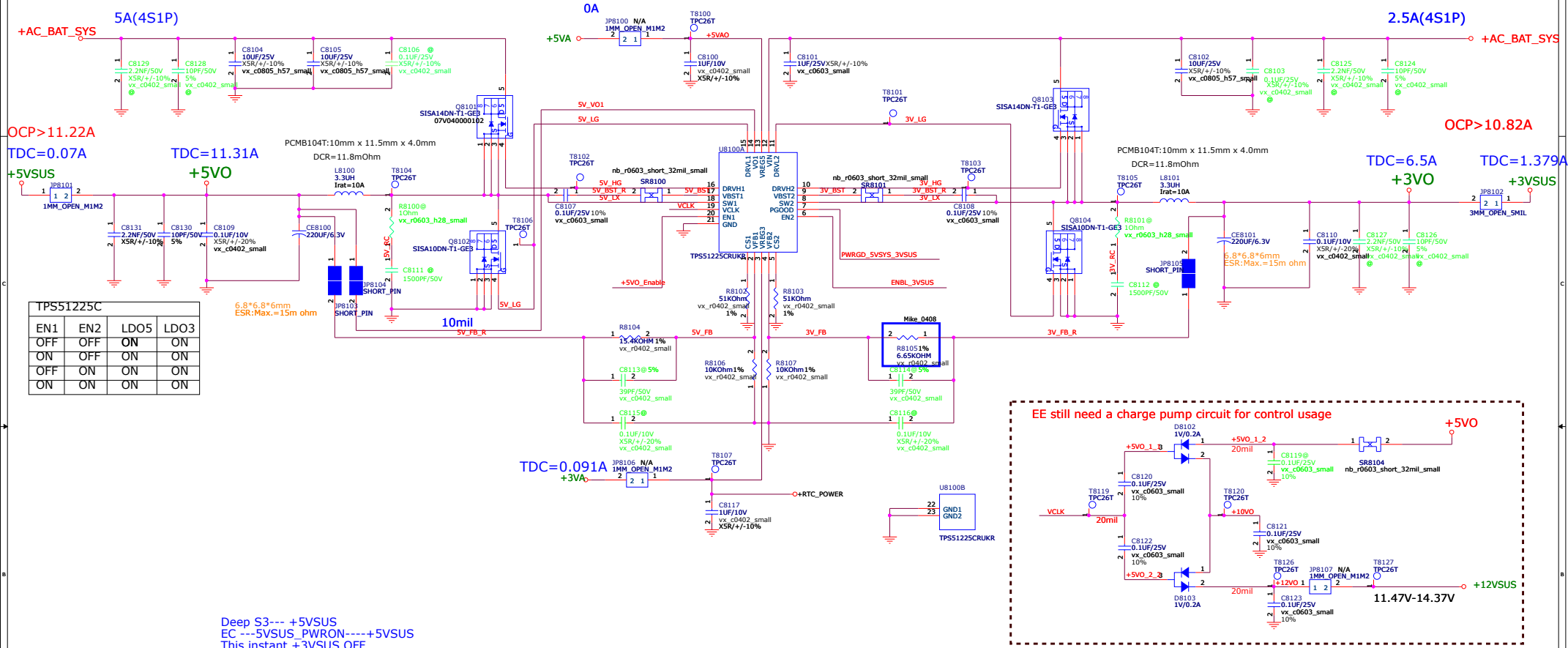
Normal

Mirror

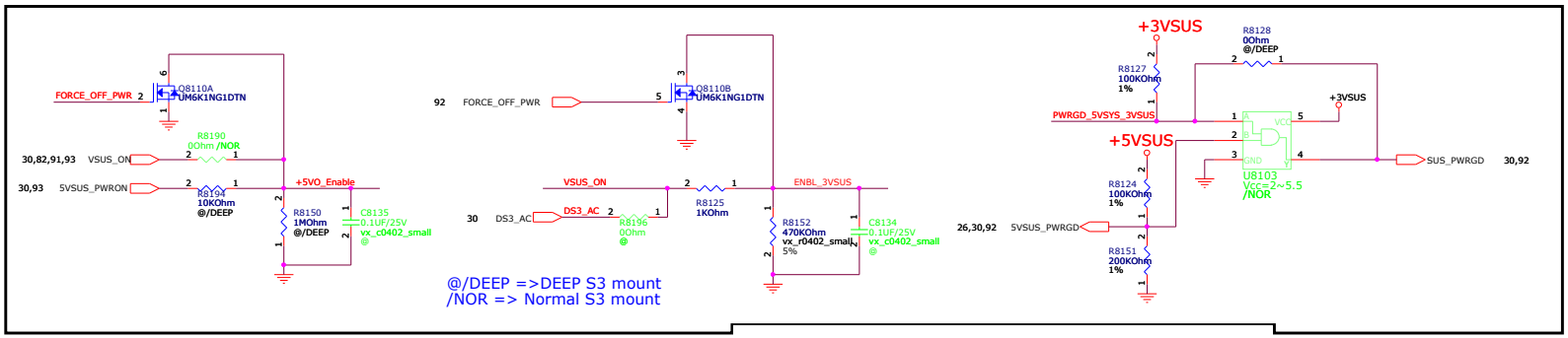
MF =1 (PU) : Mirror
MF =0 (PD) : Normal

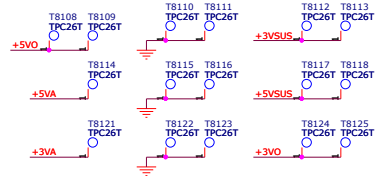
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : GDDR5 X32 *B
BG1-HW RD Center-HW RD Div.2
Engineer: Allen_Kuo
Size: C
Project Name: GL753VW
Rev: 1.0
Date: Wednesday, September 07, 2016
Sheet 77 of 120

+5VO & +3VO POWER SUPPLY



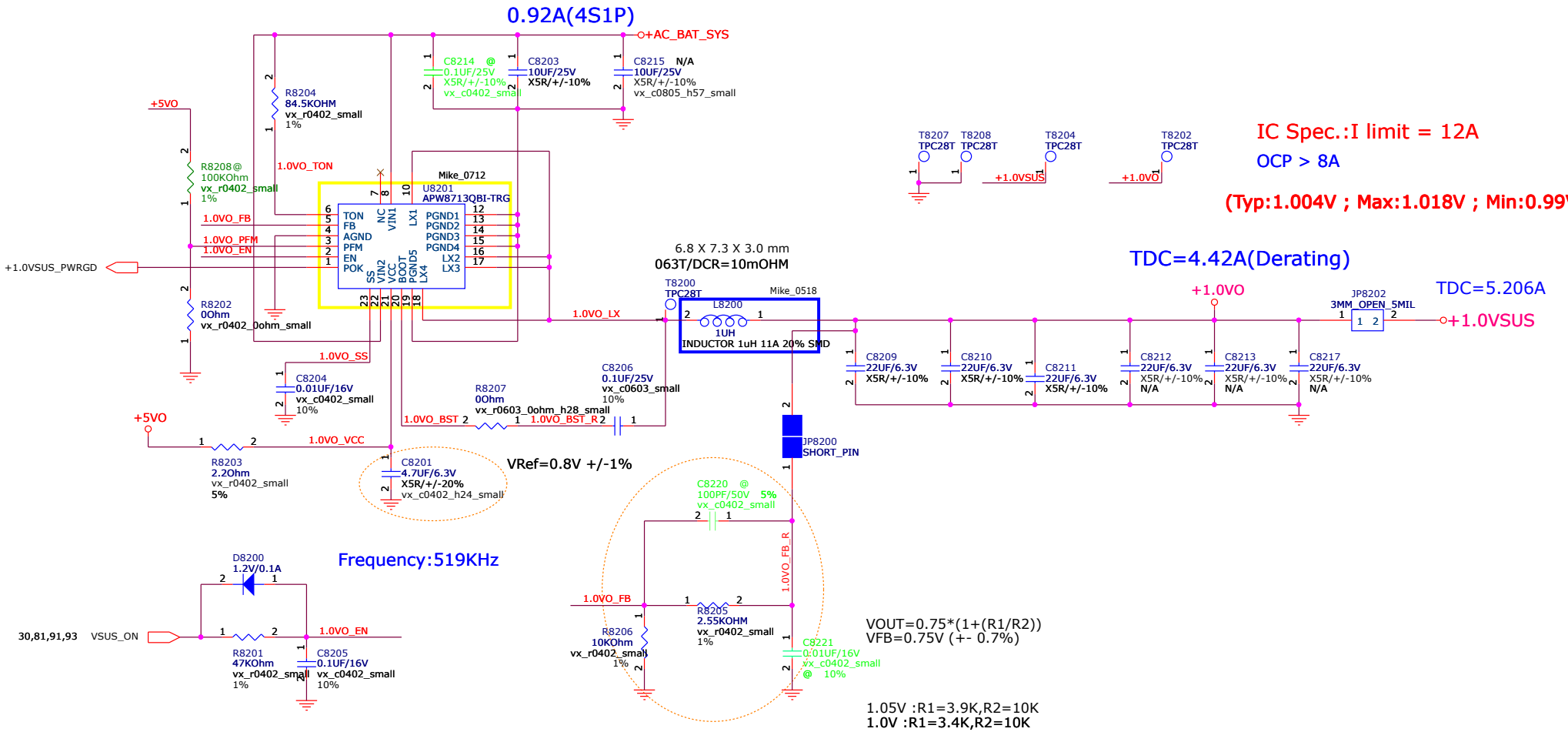
ABBA Rule





PEGATRON Title : POWER_SYSTEM
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Benson_Lin
Size: Project Name: GL753VD Rev: A00
Date: Monday, September 12, 2016 Sheet 81 of 24

1.0VSUS POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

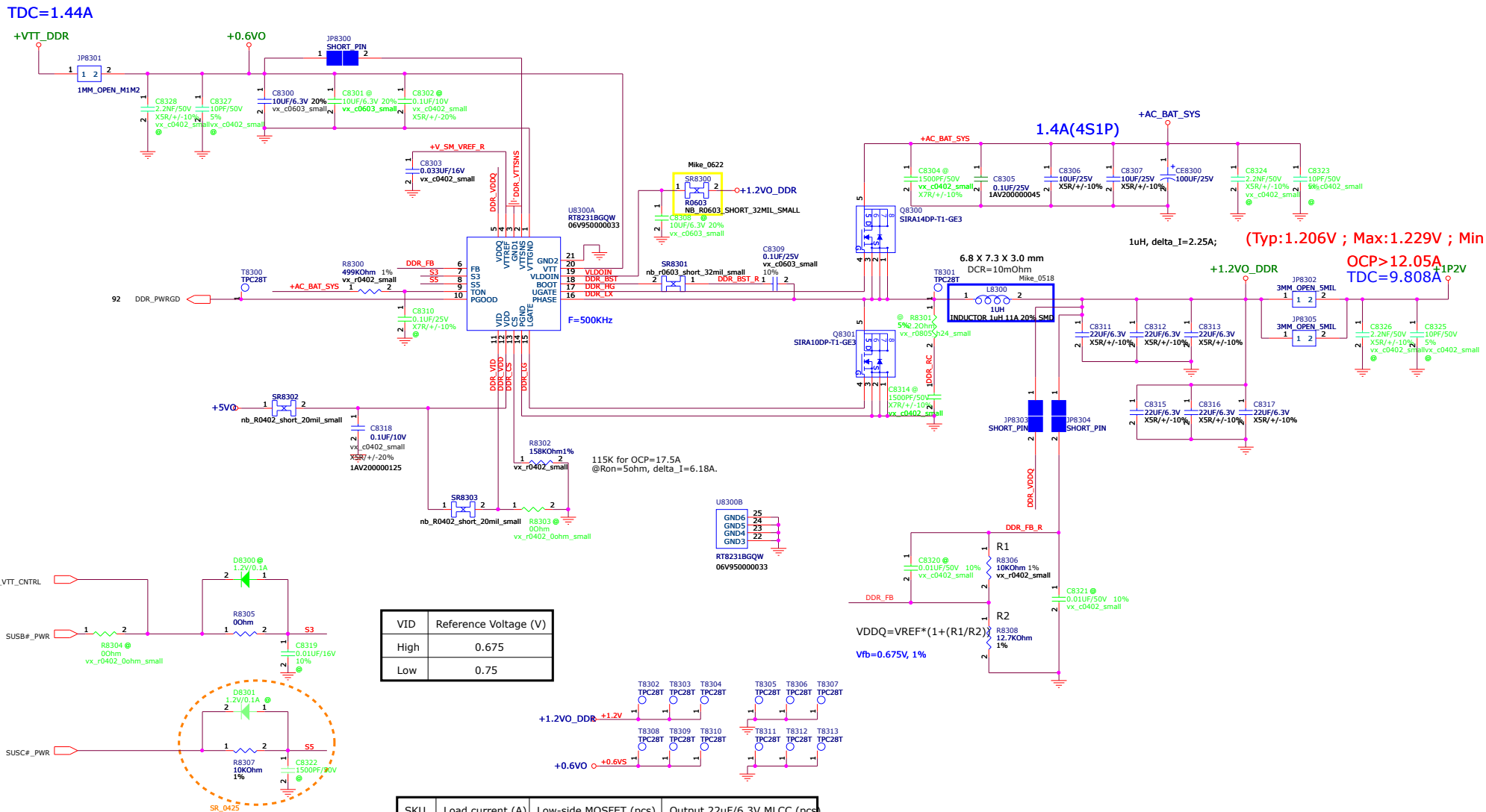
Title : POWER_+1.0VSUS

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	GL753VD	A00

Date: Monday, September 12, 2016 Sheet 82 of 24

DDR & VTT POWER SUPPLY



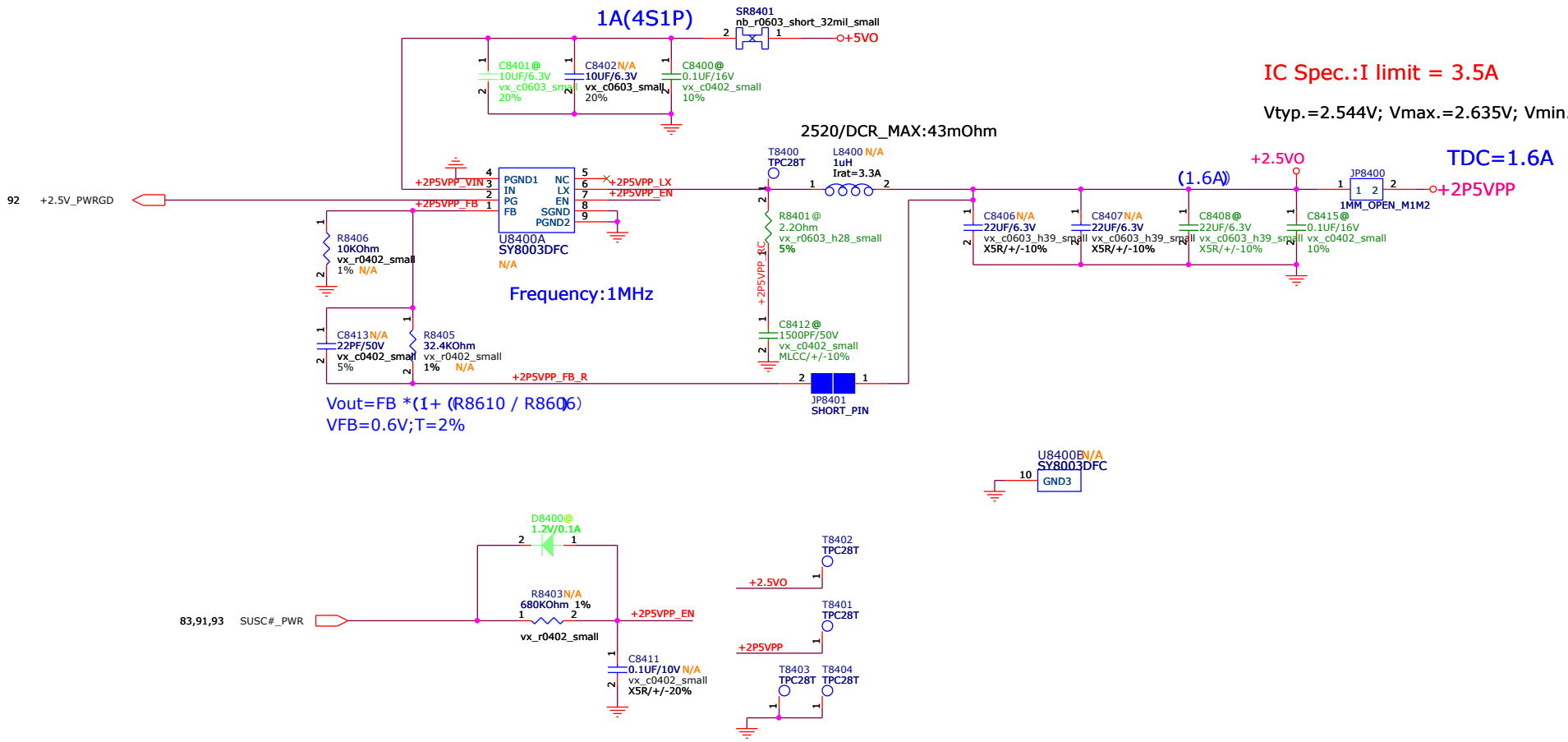
VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8		

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DDR & VTT
Engineer: Benson_Lin
Size: Custom | Project Name: GL753VD | Rev: A0X
Date: Monday, September 12, 2016 | Sheet: 83 of 24

+2.5V POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_+2.5V

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	GL753VD	A00
Date: Monday, September 12, 2016	Sheet 84 of 24	

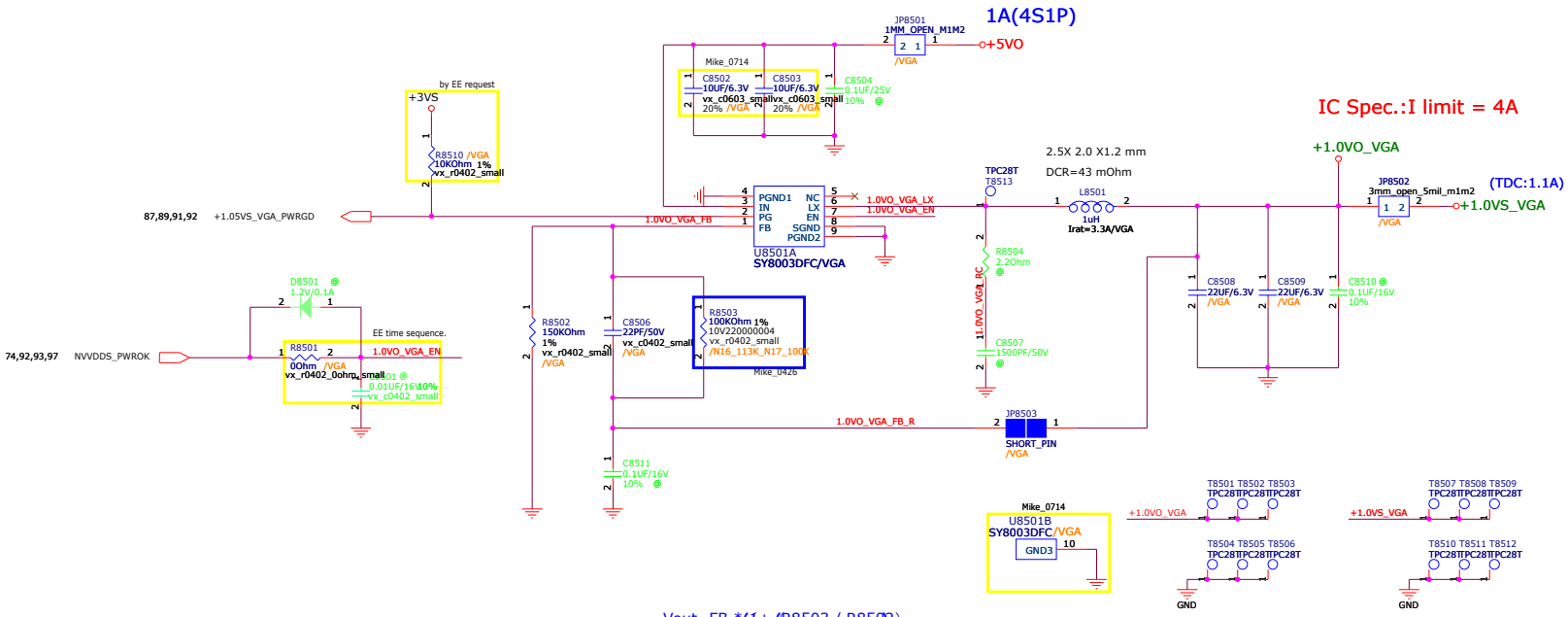
1.0VS_VGA(+1P0V_GPU) POWER SUPPLY

R8503 need to change Voltage 1V & 1.05V

+1.0VS_VGA

	N16P-GX	N17P-G1
EDP	2.9A	TBD
TDC	2.57A	3A
Voltage	1.05V	1V

R8503=113K-->Vtyp.=1.052V; Vmax.=1.077V; Vmin.=1.027V
R8503=100K-->Vtyp.=1V; Vmax.=1.023V; Vmin.=0.977V



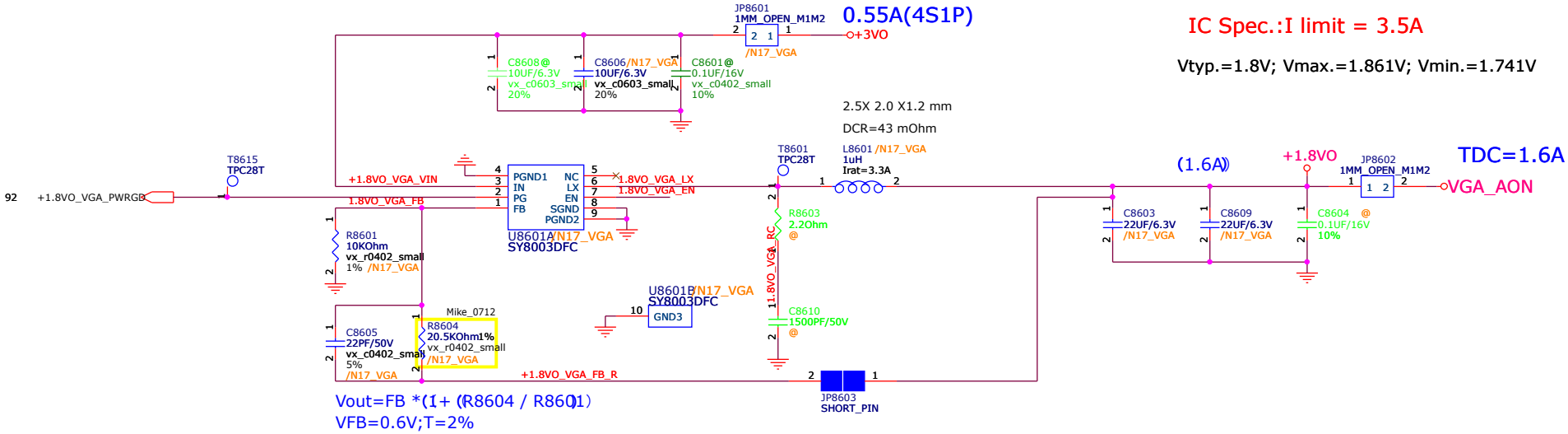
N16P-GX-->VO=1.05V; R8503=113K (10V220000401);
N17P-G1-->VO=1V; R8503=100K (10V220000004);

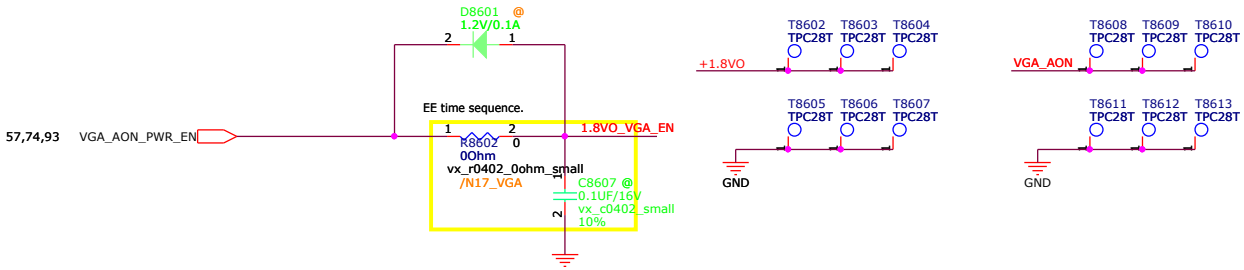
Vout=FB *(1+ (R8503 / R8502))
VFB=0.6V;T=1.5%

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_+1.0VS_VGA
Engineer: Mike_Ke
Size: Custom | Project Name: GL753VD | Rev: A00
Date: Monday, September 12, 2016 | Sheet 85 of 24

+1.8V POWER SUPPLY





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_1V8_VGA_N17

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	GL753VD	A00

Date: Monday, September 12, 2016 Sheet 86 of 24

(N17)VGA_CORE POWER SUPPLY

N16P-GX follow DG-07269

	N16P-GX Config A	N16P-GX Config B
R8700	39K	20K
R8701	39K	20K
R8702	1.5K	2K
R8704	30K	18K
R8705	1.5K	0
C8700	1.5nF	2.7nF
Vmin	0.6V	0.6V
Vmax	1.2V	1.2V
Vboot	0.875V	0.9V
VSTB	6.25mV	6.25mV

N17P-G0(G1) follow DA-07933

	N17P-G0(G1) Config
R8700	6.19K
R8701	20.5K
R8702	4.32K
R8704	16.5K
R8705	309
C8700	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

VGA_PSI#	VO_action
0~ 0.4V	1 Phase DEM
0.8 ~ 1V	1 Phase FCCM
1.4 ~ 5.5V	Active phase (2or 3 Phase)FCCM

+NVVDD

	N16P-GX	N17P-G0	N17P-G1
EDP	87A	92A	101A
TDP	51.1A	48A	58A

EDP=90A
TDC=47A
OCP:100A

499K-->300KHz

R8730:
15.4k ohm for OCP=156A_3 phase
20k ohm for OCP=141A_2 phase

R8716 mount 0 ohm
disable 3 phase

Phase 1 11.72A(4S1P)
Phase 2 11.72A(4S1P)
Phase 3 11.72A(4S1P)

PCMB064T:
DCR=1.0mOhm, +/- 7%
0.24uH
Irat=25A
INDUCTOR 0.24uH 27A 20% SMD

PLACE NEAR GPU

ESR<3mohm; Ripple:<20mV (Max.<30mV)

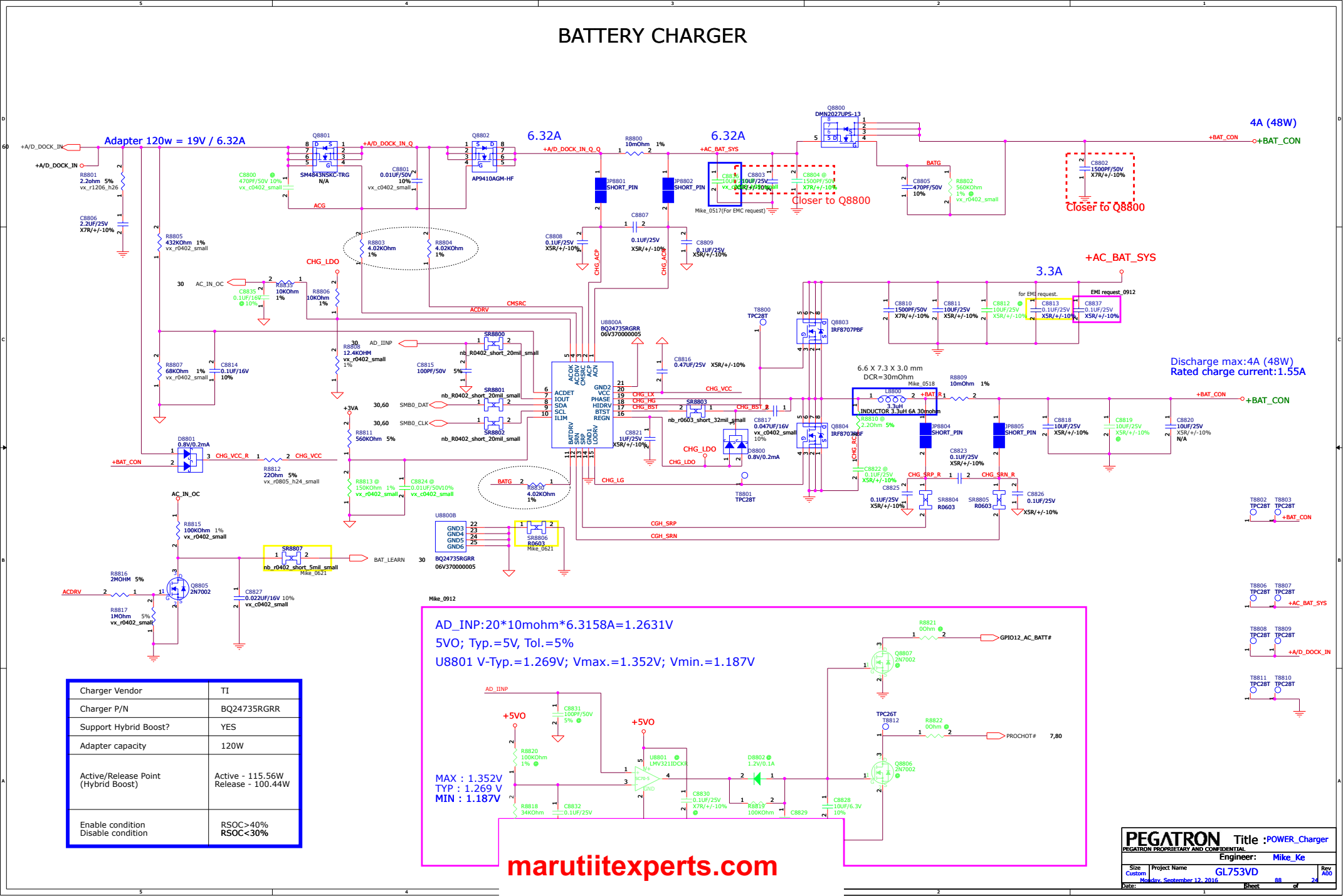
EE:N16-->(330uF/2V, 6m ohm) *1pcs
EE:N17-->(330uF/2V, 6m ohm) *2pcs

	R8751	R8752	R8720	R8719	R8718	R8716	R8753	R8754	R8755
2Phase (Phase3 parts open)	5.76k	10ohm	NC	NC	NC	0ohm	100k	10k	0ohm
3Phase	NC	NC	10k	10k	10k	NC	NC	NC	NC

(R8725 need close to U8700)

PEGATRON Title : POWER_+NVVDD
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Mike_Ke
Size: Custom | Project Name: GL753VD | Rev: A00
Date: Monday, September 12, 2016 | Sheet: 87 of 24

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24735RGRR
Support Hybrid Boost?	YES
Adapter capacity	120W
Active/Release Point (Hybrid Boost)	Active - 115.56W Release - 100.44W
Enable condition Disable condition	RSOC>40% **RSOC<30%**

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_Charger
Engineer: Mike_Ke
Size: Custom
Project Name: GL753VD
Rev: A00
Date: Monday, September 12, 2016
Sheet 88 of 24

+FBVDDQ POWER SUPPLY

	PSI Voltage Setting Operation Phase Number
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

3.23A(4S1P)

+AC_BAT_SYS

+FBVDDQ

	N16P-GX	N17P-G1	N17P-G0
EDP	11.41A	20A	20A
TDC	8.75A	11A	11A

EDP=20A
TDC=11A
OCP:25A

(Typ:1.35V ; Max:1.372V ; Min:1.327V)

+1.35VO_VGA

PCMB064T:7.3*6.8*4
DCR=1.4m ohm +/-7%

VID : DC High(>=2V)@1.55V DC Low(<=1V)@1.35V

R8902=12.7k for 1phase CCM:
PSI voltage=0.793V(typ)
0.834V(max)/0.753V(min)

VGA_AON

301K ohm for Freq=505KHz
499K ohm for Freq=300KHz

180K for OCP=30A
base on Rdson Max.

U8901A RT8816AGQW

U8901B RT8816AGQW

CRFFADJ

RREF1=4.7k
RREF2=25.5k
RBOOT=3.3k
RREFADJ=31.6k
CREFIN=1.8nF
CREFADJ=2.7nF

R8915 & R8914-->66.5K ohm-->1.35V
R8915 & R8914-->64.9K ohm-->1.347V

MEM_VDD_CTL	VO
0	1.35V
1	1.5V or 1.55V

R8900=20K & R8901=60.4K-->1.502V
R8900=20K & R8901=69.8K-->1.555V

PEGATRON Title : POWER_+FBVDDQ
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Mike_Ke
Size: Custom | Project Name: GL753VD | Rev: A00
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BATTERY IN DETECT

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_Detect

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	GL753VD	A00

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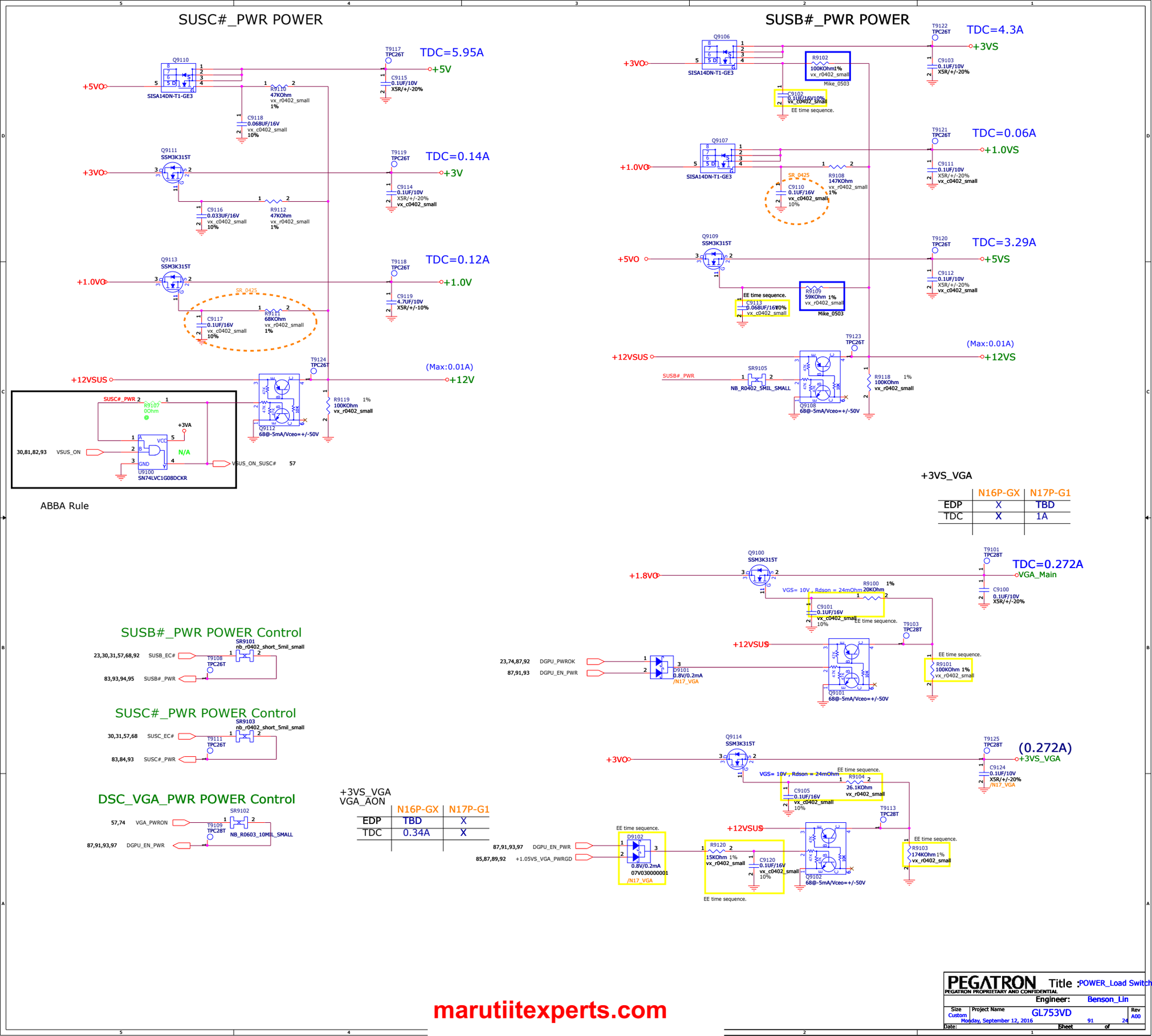
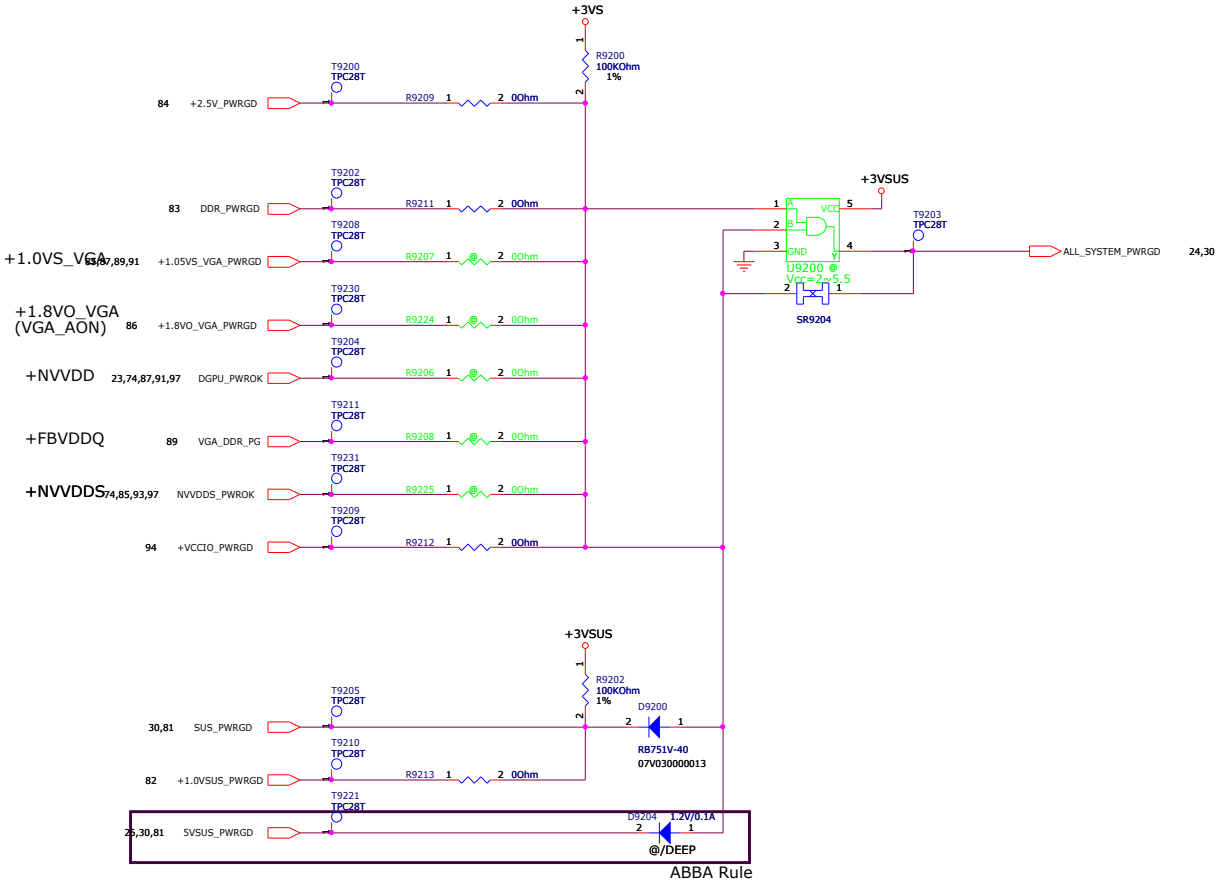
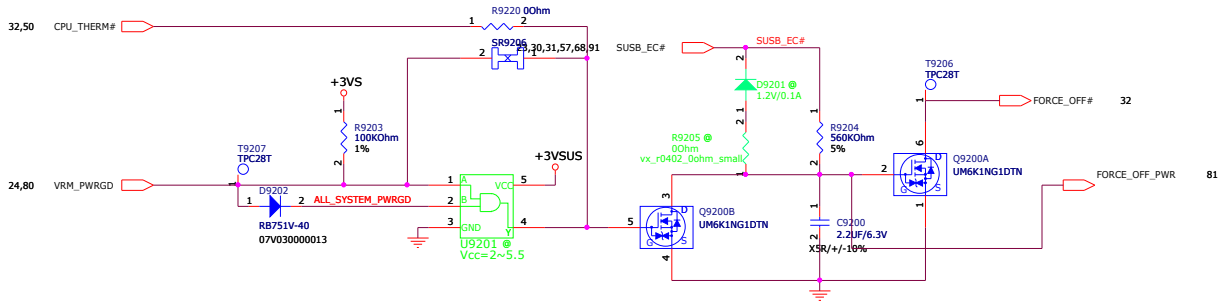


POWER GOOD DETECTER



ABBA Rule



PEGATRON Title : POWER_Protect

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Benson_Lin

Size	Project Name	Rev
C	GL753VD	A00

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+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,87,88,89,94,97

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 81

+3VA → +3VA 25,30,31,57,66,74,81,88,91

+5VO → +5VO 81,82,83,84,85,88,91,94,95

+3VO → +3VO 81,86,91,95

+1.5VO → +1.5VO 95

+5VSUS → +5VSUS 26,31,51,56,81

+3VSUS → +3VSUS 7,21,23,24,26,28,30,31,33,36,44,68,74,81,92,97

+3V → +3V 24,45,53,57,66,68,91

+5VS → +5VS 31,36,46,48,50,51,56,57,80,87,89,91,97

+3VS → +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,48,49,50,51,53,56,57,85,87,91,92,97

+1.5VS → +1.5VS 36,95

+VCORE → +VCORE 9,80

+VCCIO → +VCCIO 3,6,7,10,94

FOR POWER TEST

+3VA

JP9300 @ SGL_JUMP (1 2) → T9300 TPC28T → CPU_VRON_PWR 80

JP9301 @ SGL_JUMP (1 2) → T9301 TPC28T → SUSB#_PWR 83,91,94,95

JP9302 @ SGL_JUMP (1 2) → T9302 TPC28T → SUSC#_PWR 83,84,91

JP9303 @ SGL_JUMP (1 2) → T9303 TPC28T → VSUS_ON 30,81,82,91

VCCIO +1.5VS

JP9304 @ SGL_JUMP (1 2) → T9304 TPC28T → 5VSUS_PWRON 30,81

5VO

JP9305 @ SGL_JUMP (1 2) → T9305 TPC28T → DDR_VTT_CNTRL 7,83

VTT

JP9306 @ SGL_JUMP (1 2) → T9306 TPC28T → NVVDDS_PWROK 74,85,92,97

+1.0VS_VGA

JP9307 @ SGL_JUMP (1 2) → T9307 TPC28T → VGA_AON_PWR_EN 57,74,86

+1.8V_VGA_AON +NVVDDS

JP9308 @ SGL_JUMP (1 2) → T9308 TPC28T → DGPU_EN_PWR 87,91,97

+NVVDD

JP9309 @ SGL_JUMP (1 2) → T9309 TPC28T → GC6_FB_EN 23,74,89

+FBVDDQ

PEGATRON

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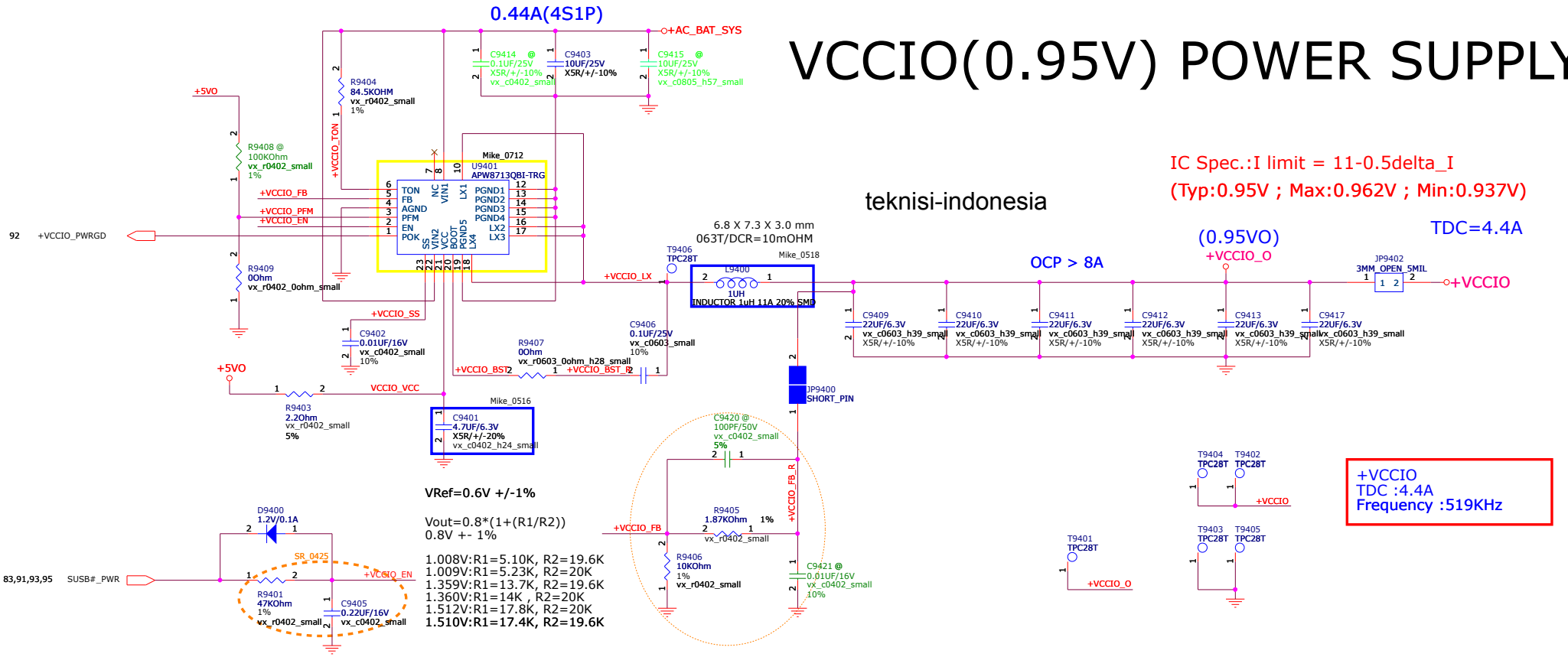
Title : POWER_Signal

Engineer: Benson_Lin

Size: Custom | Project Name: GL753VD | Rev: A00

Date: Monday, September 12, 2016 | Sheet 93 of 24

VCCIO(0.95V) POWER SUPPLY



PEGATRON
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Title : POWER_VCCIO

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	GL753VD	A00

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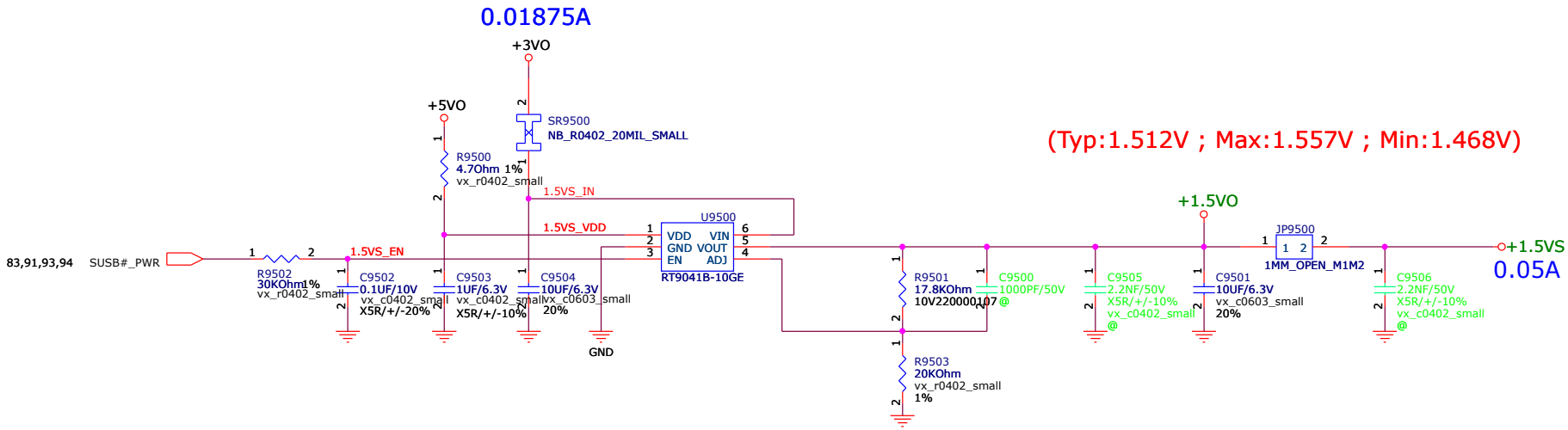
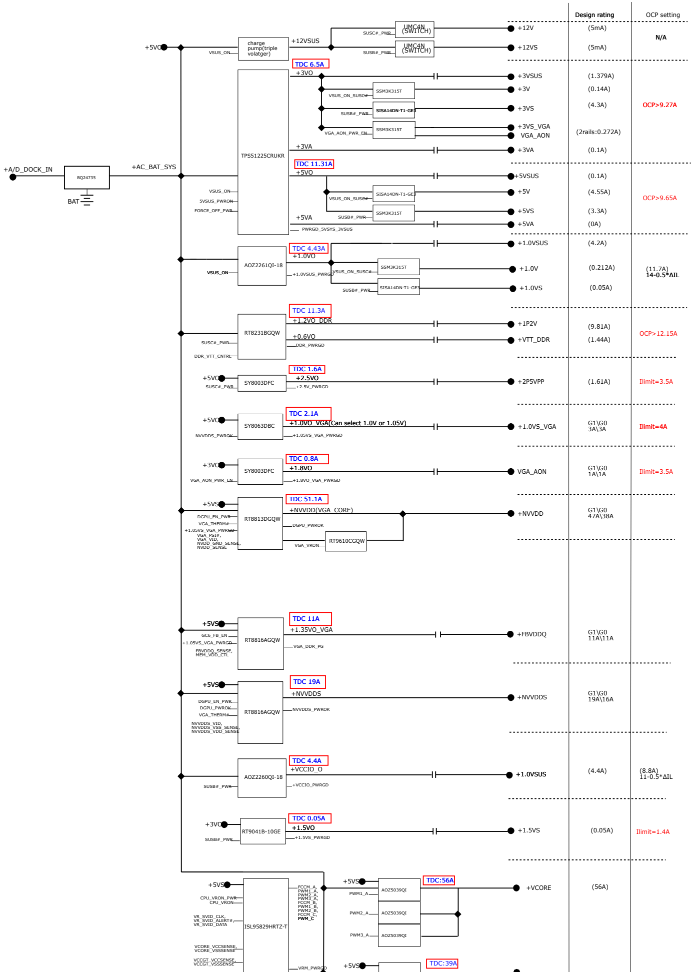
1.5V POWER SUPPLY



Vout = Vref * (1 + (R1 / R2))

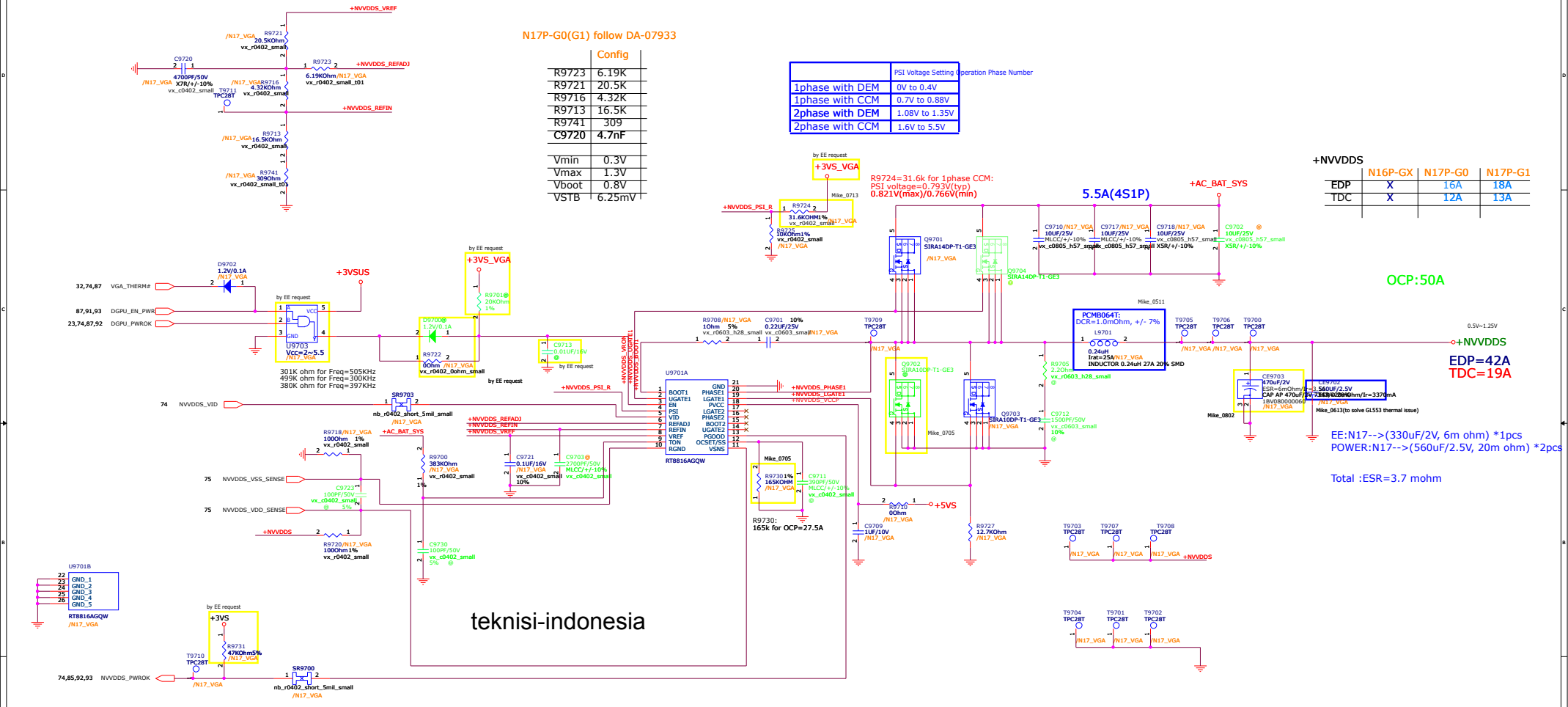
Vref=0.8V +- 2%

PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : POWER_1.5VS		
	Engineer: Mike_Ke		
Size: B	Project Name: GL753VD		Rev: A00
Date: Monday, September 12, 2016	Sheet 95 of 24		



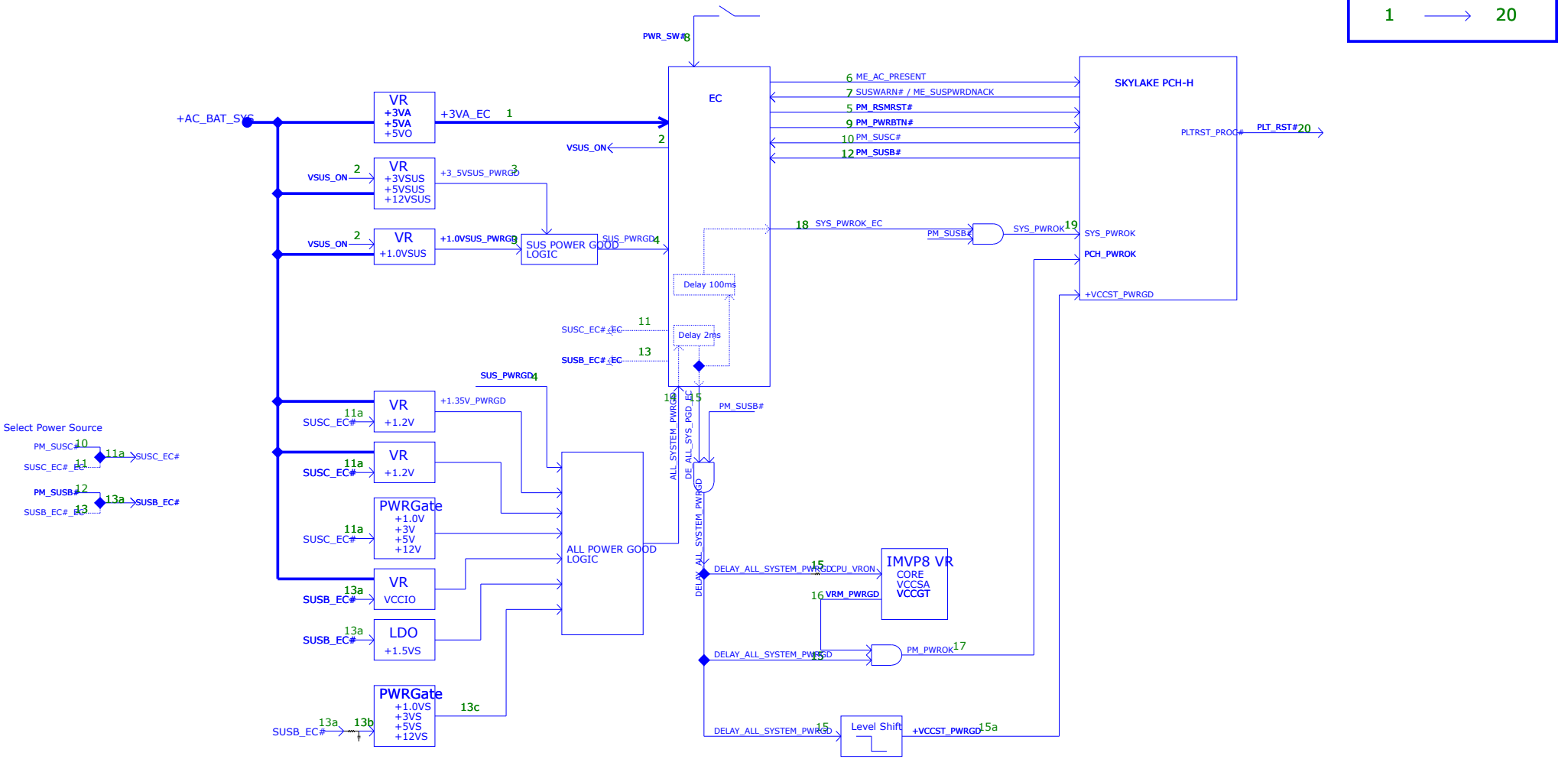
PEGATRON Title : FLOWCHART
Engineer: Mike_Ke
Project Name: GL753VD

+NVVDDS POWER SUPPLY



PEGATRON Title : POWER_+NVVDDS
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Mike_Ke
Size Custom | Project Name GL753VD | Rev A00
Date: Monday, September 12, 2016 | Sheet 97 of 24

Power On Sequence Diagram G3-S0 R0.1 (non-Deep Sx)



Title: <Title>		
Size: D	Document Number: GL753VW	Rev: 1.0
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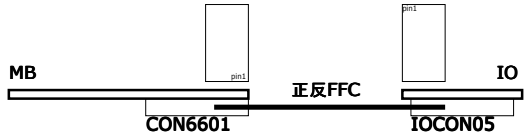
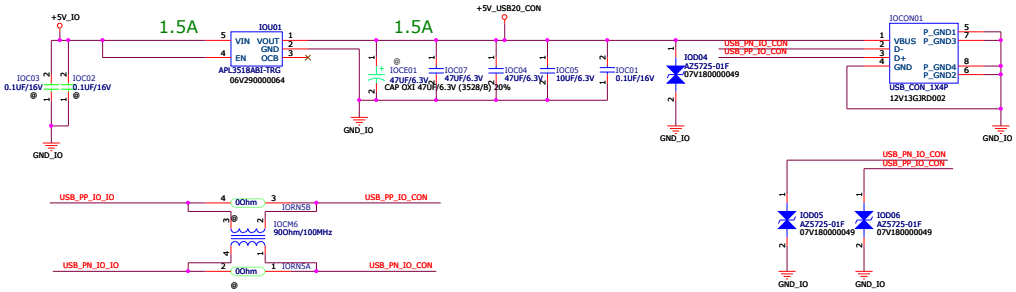
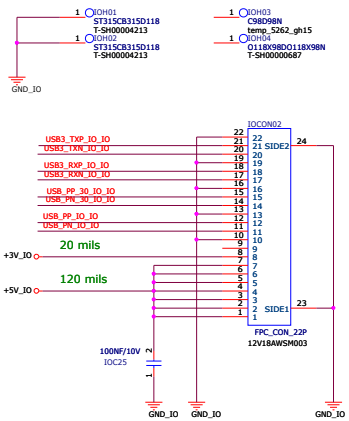
USB2.0

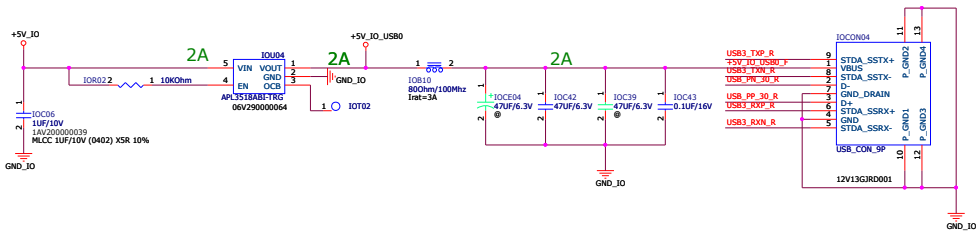


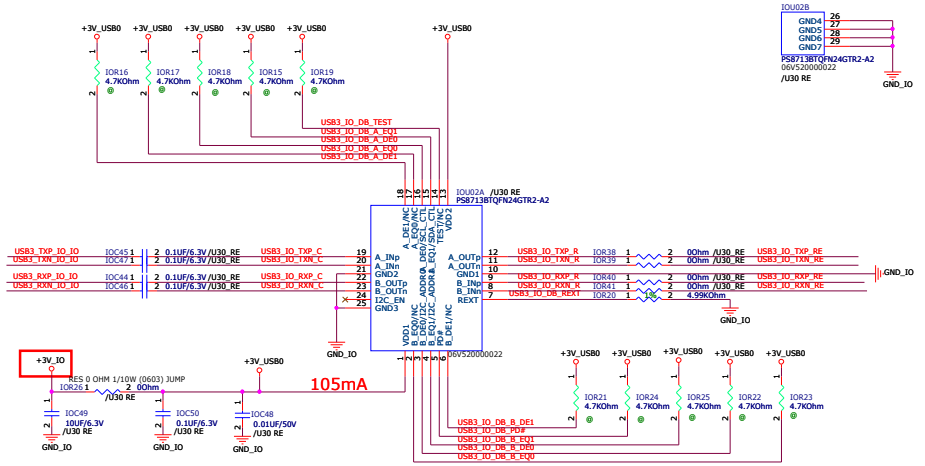


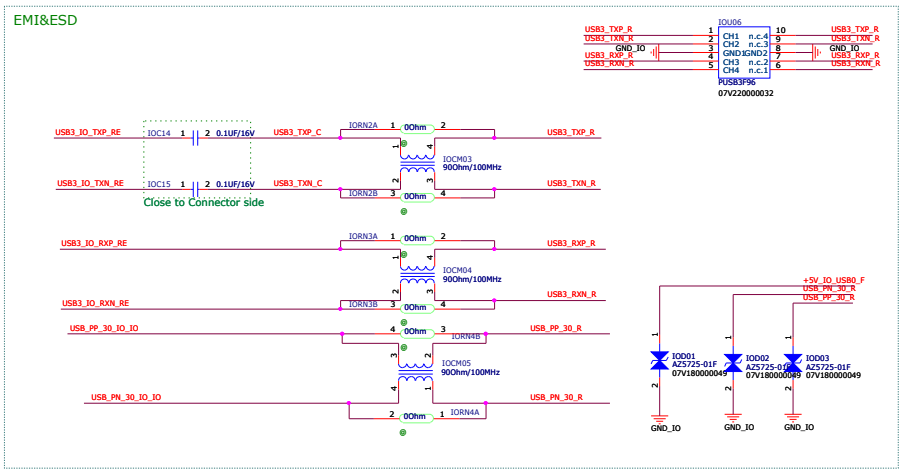


USB3.0

SB Side USB Re-driver







PEGATRON Title : IO_Small_BD
Engineer: Danny Kuo
Size: Custom | Project Name: GL553VW | Rev: 2.0
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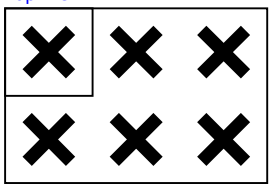
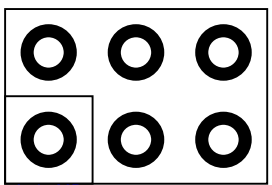
LID Switch

pin1_DB
Top view

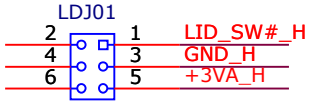


LDJ01
pin1:LID_SW#_H
pin3:GND_H
pin5:+3VA_H

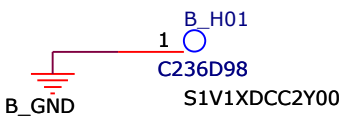
CON6602
pin2:LID_SW#
pin4:GND
pin6:+3VA



pin1_MB
Top view

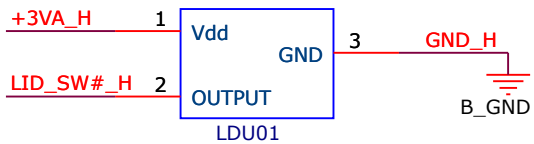


HEADER_2X3P
12V06GBSD016



C236D98
S1V1XDCC2Y00

AH180-WG-7



06V340000001

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power SW Board

Engineer: Daniel Szu

BG1-HW RD Center-HW RD Div.2-HW 3D Dept.2-RD Sec.3

Size	Project Name	Rev
A	GL553VW	1.1

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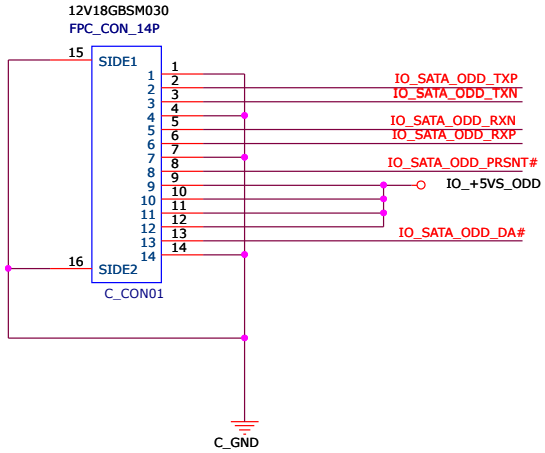

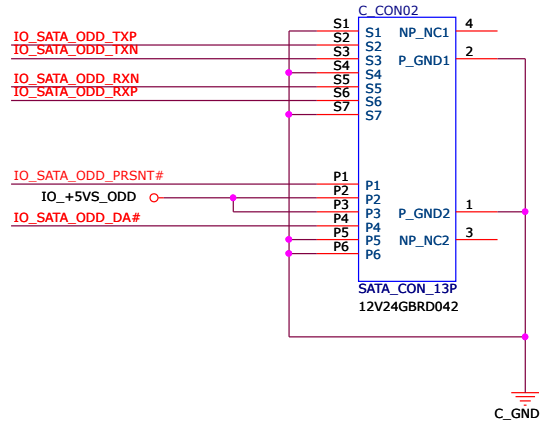

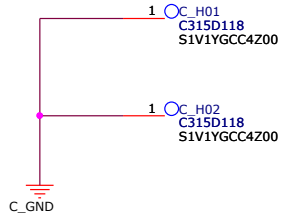

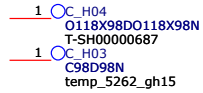

Table 5 – Standard SATA connector (3.5 inch & 2.5 inch HDD)

	Name	Type	Description	Cable Usage [b c]	Backplane Usage [c]
	Signal Segment Key				
Signal Segment	S1	GND	Ground	1st Mate	2nd Mate
	S2	A+	Differential Signal Pair A	2nd Mate	3rd Mate
	S3	A-		2nd Mate	3rd Mate
	S4	GND	Ground	1st Mate	2nd Mate
	S5	B-	Differential Signal Pair B	2nd Mate	3rd Mate
	S6	B+		2nd Mate	3rd Mate
	S7	GND	Ground	1st Mate	2nd Mate
	Signal Segment "L"				
	Central Connector Gap [a]				
	Power Segment "L"				
Power Segment	P1	Retired [e f]		2nd Mate	3rd Mate
	P2	Retired [e f]		2nd Mate	3rd Mate
	P3	DEVSLP [e]	Enter/Exit DevSleep	1st Mate	2nd Mate
	P4	GND	Ground	1st Mate	1st Mate
	P5	GND	Ground	1st Mate	2nd Mate
	P6	GND	Ground	1st Mate	2nd Mate
	P7	V_5	5 V Power, Pre-charge	1st Mate	2nd Mate
	P8	V_5	5 V Power	2nd Mate	3rd Mate
	P9	V_5	5 V Power	2nd Mate	3rd Mate
	P10	GND	Ground	1st Mate	2nd Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup/ Direct Head Unload / Vendor Specific [a]	2nd Mate	3rd Mate
	P12	GND	Ground	1st Mate	1st Mate
	P13	V_{12}	12 V Power, Pre-charge	1st Mate	2nd Mate
	P14	V_{12}	12 V Power	2nd Mate	3rd Mate
	P15	V_{12}	12 V Power	2nd Mate	3rd Mate
	Power Segment Key				

[a] For specific optional usage of pin P11 (see 6.13).
[b] Although the mate order is shown, hot plugging is not supported if using the cable connector receptacle.
[c] All mate sequences assume zero angular offset between connectors.
[d] The signal segment and power segment may be separate.
[e] Previous versions of this specification assigned 3.3 V to pins P1, P2 and P3. In addition, device plug pins P1, P2 and P3 were required to be bused together.
[f] It is recommended to have P1 and P2 connected together for the purpose of legacy functionality. Pin P3 should be a no connect if DEVSLP is not implemented.

Table 15 – Slimline device plug connector pin definition

	Name	Type	Description	Cable Usage [a b]	Backplane Usage [b]
Signal Segment	Refer to Table 5.				
	Signal Segment "L"				
	Central Connector Gap				
	Power Segment "L"				
Power Segment	P1	DP	Device Present	3rd mate	3rd mate
	P2	+5 V [e]		2nd mate	2nd mate
	P3	+5 V [e]		2nd mate	2nd mate
	P4	MD/DA	Manufacturing Diagnostic/Device Attention[d]	2nd mate	2nd mate
	P5	Gnd [c]	Ground	1st mate	1st mate
	P6	Gnd [c]	Ground	1st mate	1st mate
	Power Segment Key				

[a] All pins are in a single row with 1.00 mm (0.039 inch) pitch on the power segment portion.
[b] Ground pins in the Serial ATA Slimline device plug power segment (connector pins P5 and P6) shall be bussed together on the Serial ATA Slimline device.
[c] The connection between the Serial ATA Slimline device signal ground and power ground is vendor specific.
[d] The DP and MD/DA signals shall be referenced to the power portion ground pins, P5 and P6.
[e] The 5 V power delivery pins in the Serial ATA Slimline device plug power segment (connector pins P2 and P3) shall be bussed together in the Serial ATA Slimline device.

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
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Skylake-H42_45W (Non-OPC)

Skylake H	+VCORE	+VCCGT	+VCCSA
EDP	68A	55A	11.1A
TDC	50A	39A	10A

Rs2 & Rpu2 Resistance circuit put in EE P7
Rs2 & Rpu2 Resistance need to close VR controller

	Rs2	Rpu2
VIDALERT#	10 ohm	100 ohm
VIDSCLK	50 ohm	45 ohm
VIDSOUT	0 ohm	Empty

R8039 & R8084 100Kohm
15.8k ohm R series with 100k NTC to trip VR_HOT# is in 110 deg C
100 deg C trip VR_HOT#,R series is 14.3k ohm
120 deg C trip VR_HOT#,R series is 16.9k ohm

VID1 : 0.9V
VID2 : 0.6V
VID3 : 0.3V
Vboot : 0V
LL=2.65mohm

+VCCGT(H-line42_45W)
TDC :39A
EDC(Iccmax):55
OCP=66.2A
Frequency :583kHz
PWR Cap. :660uF(22uF*30pcs)+
470uF(470uF*1pcs)
Total Cap. :1130uF

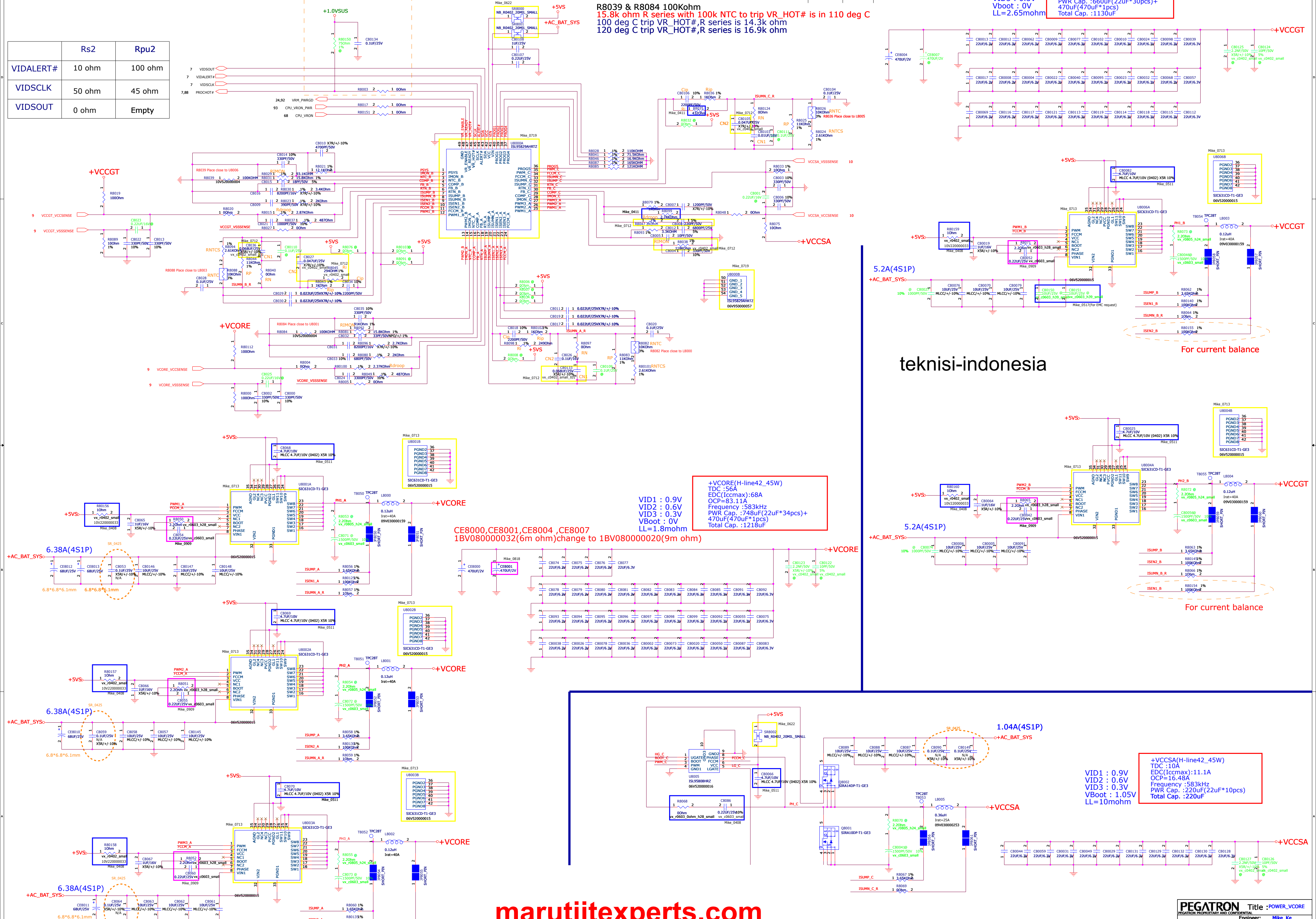
+VCORE(H-line42_45W)
TDC :56A
EDC(Iccmax):68A
OCP=83.11A
Frequency :583kHz
PWR Cap. :748uF(22uF*34pcs)+
470uF(470uF*1pcs)
Total Cap. :1218uF

VID1 : 0.9V
VID2 : 0.6V
VID3 : 0.3V
VBoot : 0V
LL=1.8mohm

CE8000,CE8001,CE8004 ,CE8007
1BV080000032(6m ohm)change to 1BV080000020(9m ohm)

+VCCSA(H-line42_45W)
TDC :10A
EDC(Iccmax):11.1A
OCP=16.48A
Frequency :583kHz
PWR Cap. :220uF(22uF*10pcs)
Total Cap. :220uF

VID1 : 0.9V
VID2 : 0.6V
VID3 : 0.3V
VBoot : 1.05V
LL=10mohm



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_VCORE
Engineer: Mike_Ke
Project Name: GL753VD
Size: Custom
Rev: A00
Date: Monday, September 12, 2016
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